A Reconfigurable GPS/Galileo Receiver Front-end for Space Applications

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A Reconfigurable GPS/Galileo Receiver Front-end for Space Applications

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To My Parents

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List of Acronyms

ADC	Analog to Digital Converter
AGC	Automatic Gain Control
AltBOC	Alternative Binary Offset Carrier
AOCS	Attitude and Control System
ASIC	Application-Specific Integrated Circuit
BJT	Bipolar Junction Transistor
BOC	Binary Offset Carrier
BPSK	Binary Phase Shift Keying
BSIM	Berkeley Short-channel Insulated-gate field-effect transistor Model
C/NAV	Commercial Navigation Message
CBOC	Composite Binary Offset Carrier
CDMA	Code Division Multiple Access
CHAMP	CHAllenging Mini-satellite Payload
CML	Current Mode Logic
CMOS	Complementary Metal-Oxide Semiconductor
CNAV	Civil Navigation Data
COTS	Commercial-Off-The-Shelf
cps	chips per second
CS	Commercial Service
D-FF	D-type Flip Flop
DAC	Digital to Analog Converter
DC	Direct Current
DLL	Delay Locked Loop
DSB-AM	Double Side Band-Amplitude Modulation
DSSS	Direct Sequence Spread Spectrum

EGNOS	European Geostationary Navigation Overlay Service
EKF	Extended Kalman Filter
ENOB	Effective Number Of Bits
ESA	European Space Agency
EU	European Union
F/NAV	Free access Navigation Message
FAA	Federal Aviation Administration
FDMA	Frequency Division Multiple Access
FLL	Frequency Locked Loop
FPM	Functional Performance Metric
GA	Ground Antennas
GAGAN	GPS Aided Geo-Augmented Navigation
GCM	Greatest Common Divisor
GIS	Geographic Information System
GLONASS	GLObal NAvigation Satellite Systems
GNC	Guidance, Navigation and Control
GNSS	Global Navigation Satellite Systems
GOCE	Gravity field and steady-state Ocean Circulation Explorer
GPS	Global Positioning Satellite System
GRACE	Gravity Recovery and Climate Experiment
I/NAV	Integrity Navigation Message
IC	Integrated Circuit
IF	Intermediate Frequency
IMU	Inertial Measurement Unit
IM	Intermodulation
IP	Intercept Point
IRR	Image Rejection Ratio
ITU-RR	International Telecommunication Union Radio Regulations
LEO	Low Earth Orbit
LNA	Low Noise Amplifier
LO	Local Oscillator

LORAN	LOng RAnge Navigation
LPF	Low-Pass Filter
LSB	Least Significant Bit
MCS	Master Control Station
MEMS	Micro Electro-Mechanical System
MOS	Metal-Oxide Semiconductor
MS	Monitor Station
MSAS	Multi-functional Satellite Augmentation System
MSB	Most Significant Bit
NCO	Numerically Controlled Oscillator
NF	Noise Figure
NMOS	N-channel Metal Oxide Semiconductor
OBC	On-Board Computer
OS	Open Service
PCB	Printed Circuit Board
PLL	Phase Locked Loop
PMOS	P-channel Metal Oxide Semiconductor
POD	Precise Orbit Determination
PRN	Pseudo Random Noise
PRS	Public Regulated Service
PSD	Power Spectral Density
PSK	Phase Shift Keying
PVT	Position, Velocity and Time
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RF	Radio Frequency
RHBD	Radiation Hardening By Design
RINEX	Receiver Independent Exchange
SAR	Search And Rescue
SAR	Successive Approximation Register
SBAS	Satellite-Based Augmentation Systems

SDR	Software Defined Radio
SEE	Single-Event Effect
SEFI	Single-Event Functional Interrupt
SEGR	Single-Event gate rupture
SEL	Single-Event Latch-up
SET	Single-Event Transient
SEU	Single-Event Upset
SFDR	Spurious Free Dynamic Range
SI	System Integrity
SIP	System In Package
SNR	Signal to Noise Ratio
SOC	System On Chip
SoL	Safety of Life
sps	symbols per second
SSB	Single Side Band
SV	Space Vehicle
SWOT	Strengths, Weaknesses, Opportunities, Threats
T-FF	T-type Flip Flop
TG	Transmission Gate
TID	Total Ionizing Doze
TM-BOC	Time-Multiplexed Binary Offset Carrier
TRL	Technology Readiness Level
TU Delft	Delft University of Technology
UCLA	University of California, Los Angeles
US	United States
UTC	Coordinated Universal Time
UWB	Ultra Wide-Band
VGA	Variable Gain Amplifier
WAAS	Wide Area Augmentation System
ZOH	Zero Order Hold

1 Overview

Where am I? Where is my target? What is the best way to reach the target? These are questions that many of us ask ourselves everyday.

During history, mankind tried to answer these questions as accurate as possible. People used natural resources, invented instruments and combined the knowledge of different disciplines to improve these answers. The results of these efforts became an important field of science and engineering called navigation. As the technology develops in different areas, the navigation technology is developed likewise and new applications and technologies are introduced.

In this thesis, novel concepts for improved navigation technologies will be developed, characterized and verified which can contribute to ongoing development in the field of navigation.

1.1 Navigation Systems

Navigation systems have developed during history starting from basic landmark detections to state-of-the-art satellite based navigation systems. Each of these navigation systems use reference points and a measurable quantity. A number of these navigation systems use natural resources as their reference points while for others, dedicated man-made systems are developed and operated. In general, navigation can be based on two approaches: using natural sources (stars, landmarks, etc.) and using man-made sources as reference points. In the following, a

brief overview of these two will be provided.

1.1.1 Navigation Using Natural Sources

Since the early ages, people have been using natural resources to find their position, their directions and to navigate. These resources are for example stars, landmarks or the Earth magnetic field. In general, navigation has been a challenging task and especially navigation at sea in early times was the main driver for the development of instruments for navigation. Instruments and tools have been developed such as maps, timers, compasses, astrolabes, sextants, gyroscopes, accelerometers, star cameras, etc. by which the user could determine his position based on the landmarks, Earth magnetic field, star charts, motion behavior and so forth whenever the information was available. Eventually, the accuracy of using these methods increased by developments in different technology areas and combining the knowledge from different disciplines. For example, keeping an accurate track of time has always been an important task in navigation which has been evolved. The usage and the accuracy requirement of time keeping has been changed from the early times where rotation of the Earth and the time dependency of the positions of the stars had to be taken into account till today where accurate timing in the order of pico-second is an essential part of the position calculation. Fig. 1.1 depicts the trend of time measurement accuracy improvement over the last 1000 years. In this figure, in order to better demonstrate the effect of technological advances, functional performance metric (FPM) of timekeeping is expressed as exponential of accuracy (1/drift) divided by volume of the timepiece since the accuracy of the clock can almost always be improved by increasing its size, even though it is not always practical [1].

An example of combining different state-of-the-art technologies to use natural resources is pulsar navigation. Pulsars, i.e. rapidly rotating neutron stars, are another natural source which can be used for navigation. However, it was not possible to use them till recently due to the lack of required technology. Pulsars are extremely fast rotating neutron stars. The typical diameter of a pulsar is about 20 km and the rotation period is in the range of milliseconds to tens of seconds. They emit ultra wide-band (UWB) electromagnetic waves which are observed as periodic pulses. Each pulsar has its own unique signature, i.e. pulse period and pulse shape, which makes it distinguishable from others. Study shows that pulsars can be used for navigation and accurate timing. There are several teams at Delft University of Technology (TU Delft), University of California, Los Angeles (UCLA) and other research institutes working to develop the technology in the fields of receiver design and signal processing for pulsar navigation [2–6].

However, the accuracy or availability of these systems using natural sources is either limited and insufficient for advanced applications or their usage is still too

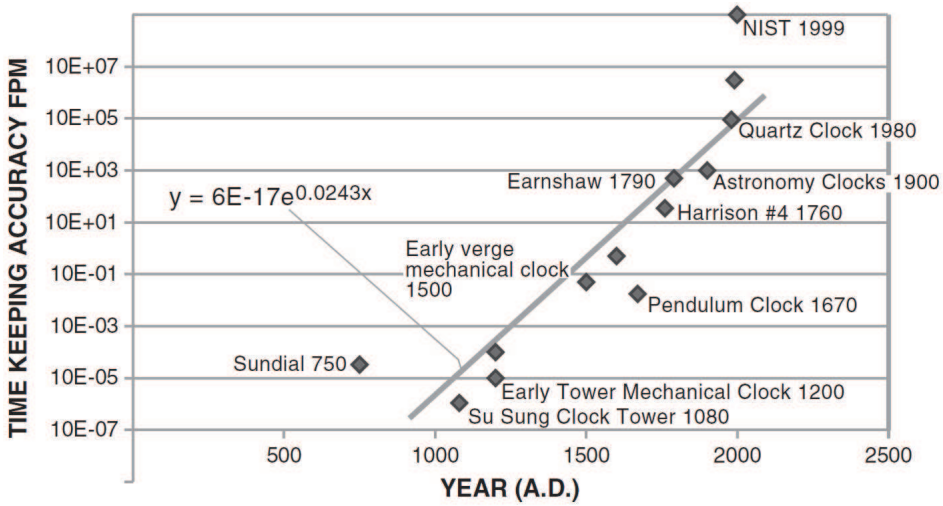


Figure 1.1: Trend of time measurement accuracy improvement over the last 1000 years [1]

complicated. Thus, new dedicated navigation systems have been developed as will be explained in the following section.

1.1.2 Navigation Using Man-made Sources

Rapid technology developments in the 20th century provided the opportunity to develop new navigation systems. Thus, new techniques were employed to develop and operate more accurate and easier-to-use navigation systems than navigation using natural sources. One of the early navigation systems was LORAN (LOng RAnge Navigation), a ground-based system. The first generation of this system, LORAN-A, was developed during the second world war by the United States (US) and was based on 40 μs pulses transmitted at 1950 kHz. The navigation error was high with position error of 28 miles ($\approx$ 45 km) in 1400 miles ($\approx$ 2253 km) flight. The next LORAN generations, LORAN-B and LORAN-C improved the absolute position accuracy to about 460 m and repeatable accuracy of about 18 - 90 m [7]. LORAN-C went out of commission in 2010 [8].

When space became accessible in the 60's of the 20th century, the next generations of the navigation systems moved towards global and space-based systems. These Global Navigation Satellite Systems (GNSS) are: NAVSTAR Global Positioning System (GPS) which is developed and operated by the US, GLObal NAvigation Satellite Systems (GLONASS) developed and operated by Russia, the Galileo satellite navigation system which is being developed by the European Union (EU) and the Compass (Beidou) satellite navigation system by China. To improve the

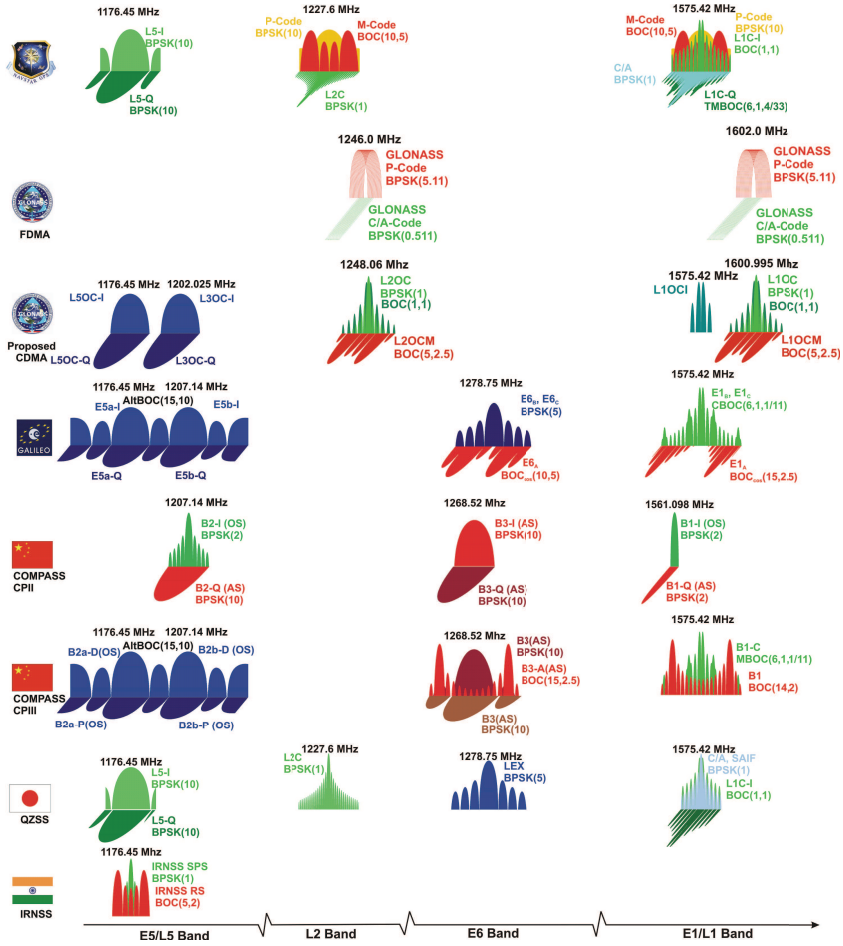


Figure 1.2: Frequency plans of GNSS systems in space [9]

performance of these GNSS systems, several satellite-based augmentation systems (SBAS) are in operation or are under development. Examples of SBAS are: the Wide Area Augmentation System (WAAS), operated by the United States Federal Aviation Administration (FAA), the European Geostationary Navigation Overlay Service (EGNOS), operated by the European Space Agency (ESA), the Multi-functional Satellite Augmentation System (MSAS) system, operated by Japan, the Quasi-Zenith Satellite System (QZSS), under development by Japan and the GPS aided geo-augmented navigation or GPS and geo-augmented navigation system (GAGAN), being developed by India. Fig. 1.2 depicts some of these space-based navigation systems with their frequency allocations.

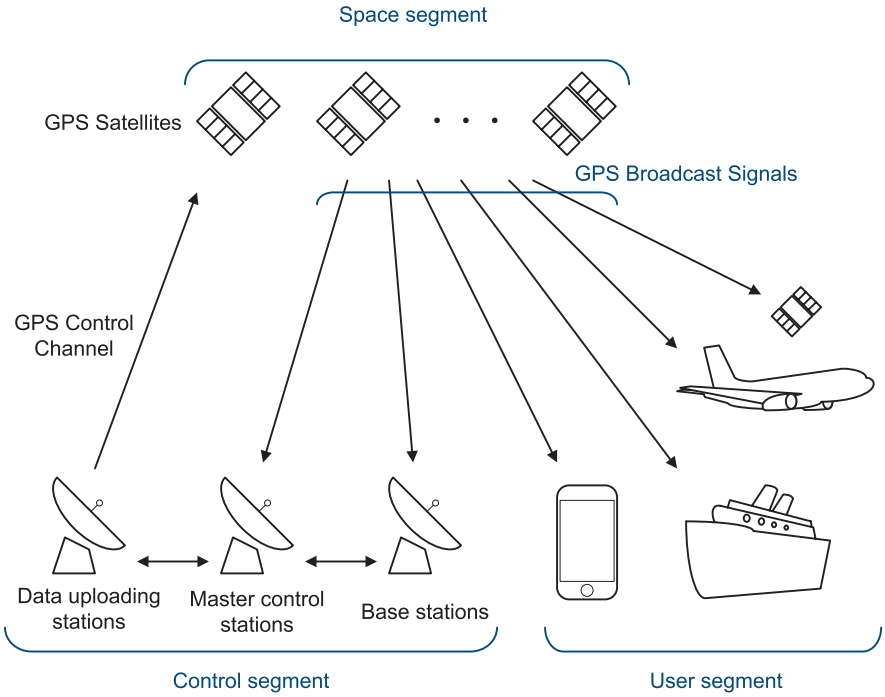


Figure 1.3: GPS system segments

1.2 Overview of GNSS Systems - GPS

The operation principle of space-based navigation systems is similar. Since GPS is the most commonly used GNSS system[1], the operation principle of GPS will be briefly described in this section.

GPS is a space-based radio-positioning and time transfer system which provides accurate position, velocity and time (PVT) information to its users. GPS consists of three major system segments: space segment, control segment and user segment as depicted in Fig. 1.3.

The space segment consists of a nominal constellation of 24 satellites in semi-synchronous orbits. The satellites are arranged in six orbital planes with an inclination angle of 55°relative to the equator and an orbital period of about 12 hours. Each orbital plane comprises four satellites with an average altitude of 20,200 km. The satellites transmit ranging signals on three frequency bands: L1 at 1575.42 MHz, L2 at 1227.6 MHz and L5 at 1176.45 MHz. The legacy satellite signals are modulated with two spreading codes: C/A code and P(Y) code with chipping

[1]GLONASS and Compass satellite navigation systems are also opening their way to the consumer market

rates of 1.023 MHz and 10.23 MHz, respectively [10]. The GPS signal structure will be explained in more detail in chapter 2.

The control segment consists of a master control station (MCS) plus monitor stations (MS) and ground antennas (GA) which are located around the Earth. The MCS is the central processing facility and monitors and manages the satellite constellation. Its functions include control of satellite station-keeping maneuvers, reconfiguring of redundant satellite equipment, regularly updating navigation messages and various other satellite health monitoring and maintenance activities. The monitor stations track all GPS satellites in view and collect ranging data from each satellite. This information is transmitted to the MCS. The ground antennas are used by MCS to upload the ephemeris and clock data to each satellite for updating their navigation message [10].

The user segment comprises systems for terrestrial, maritime, aviation and space users which all employ GPS receivers as their core component. Based on the tracking of GPS signals received from various GPS satellites simultaneously, the receiver is able, together with the timing and position information modulated on the GPS signals, to determine its position and time. Details on the navigation algorithm are described in chapter 2. The user segment systems treat the GPS information in different manners depending on their applications. In the next section, different applications will be introduced that use GPS signals (in a more general term GNSS signals) as their main input. Understanding various applications and their common and exclusive needs is important for developing the specific GNSS receiver.

1.3 GNSS Applications

GNSS signals have been primarily designed for navigation purposes, i.e. the determination of the position, velocity and time (PVT) of the receiver. By further using and investigating the GNSS signal structures as well as environmental effects on the signals, more valuable information has been found to be extractable from these signals which significantly broadens the applications of GNSS.

Some of the applications use the PVT information as their main source of information. Such applications are mainly based on positioning, navigating and time synchronization. Other applications use the indirect information, for example, velocity variations of electromagnetic waves in different media to study environmental effects or various physical models of the Earth. These applications are the result of combining different sciences such as physics, oceanography, geology, weather studies and so forth by making use of GNSS technology and its systems. In the following, a list of a selected number of these applications is compiled which will be explained briefly in this section:

- Navigation
- Timing
- Real-time tracking
- Search and rescue
- Surveying and mapping
- Agriculture
- Fun and gaming
- Earth gravity modeling
- High resolution ionosphere imaging
- Atmospheric limb sounding
- GNSS reflectometry.

The number of applications is increasing due to advances in different areas of hardware and software technologies and changing user needs. Different applications typically will use different GNSS equipment and processes depending on their needs. As an example, surveying and mapping may require differential navigation technique using advanced costly receivers and highly sophisticated software processes.

1.3.1 Navigation

The primary output of a typical GNSS receiver is the receiver's position, velocity and time. Combining this information with a digital map enables terrestrial navigation. Nowadays, many people use GPS navigators in their cars to find the correct route to their destinations. Integration of a navigator with other systems, such as mobile Internet connection, provides the fastest route to the users in real-time which saves time and fuel. Navigation using GNSS signals has improved safety and increased the time and fuel efficiency in aviation and maritime applications as well.

Space systems themselves are also users as well and benefit greatly from GNSS signals. As long as a space vehicle (SV) is within the field of view of GNSS satellites, it can use GNSS signals. The navigation output of the receiver can be used for navigation, precise orbit determination (POD), attitude determination, timing solutions, clock stability estimation, data time stamping and on-board autonomy. A low earth orbit (LEO) satellite is an example of such a space vehicle which is always in the field of view of several GNSS satellites and thus can benefit from the new technology developments of the GNSS receivers as will be discussed later.

1.3.2 Timing

GNSS signals are generated by using highly accurate atomic clocks on-board the GNSS satellites. The drift and errors of these high accuracy clocks are tracked and corrected by the GNSS control segment and are a part of the navigation data. Thus, the GNSS signals can be used for accurate correction of the receiver clock or system clock as well as tracking the time, e.g., for time tagging data [11].

1.3.3 Real-time Tracking

Logistics may be an important part of a business. There are many companies that need to know how their movable assets are distributed. For example, if a transport company can track its vehicles in real-time, it could manage its resources more efficiently. Also, for railway management, the knowledge of position of each train, service vehicles, etc. will improve its resource allocation, response time and services. There are many other situations where the concept of tracking using GNSS receivers can be beneficial [12–14].

1.3.4 Search and Rescue

In any successful rescue operation, response time is very critical. The knowledge of the location of the endangered people as well as emergency service resources, landmarks, streets and buildings reduces rescue time and potentially saves lives. Using GNSS signals helps rescue teams to faster find the location of distress and the necessary resources. Intelligently combining the position information with information from other sensors can lead to effective location prediction which can further reduce the response time even if the environment has changed, e.g. after an earthquake. In addition, Galileo search and rescue (SAR) service enables Galileo satellites to pick up signals from emergency beacons carried on ships, planes or persons and relay them to national rescue centers [15].

1.3.5 Surveying and Mapping

The system which is used to capture, store, analyze, and display geographically referenced information is called Geographic information system (GIS). GIS is an important part of navigation. Generating GIS data is a time and resource consuming task. Very complex and accurate instruments are used for this purpose. Adding GNSS technology to the surveying equipments increases their accuracy while reducing the time and labor hours. In addition, it provides additional features such as autonomous map generation which can be used to monitor changing the landmark positions during the time with higher temporal resolution [16].

1.3.6 Agriculture

In order to automate agricultural processes, position and time are two important information sets which are locally available in real-time using GNSS signals. Using GNSS receivers in the fields improves the precision of field mapping and farm planning, e.g. adding the position and time information to sampled soil. In implanting and harvesting processes, the information of position and time can be added to relevant machinery and the process can be automated which reduces man power and increases the performance of agriculture [17, 18].

1.3.7 Fun and Gaming

Availability of position and time information has also shown its value in games and social activities. Many games have been designed based on the low-cost GNSS receivers and wide accessibility to them within smart phones and electronic tablets. The type of social activities have significantly been influenced by such means. Tourism and entertainment industries, as well as many other activities, are adapting themselves to this new technology [19].

1.3.8 Earth Gravity Modeling

One of the interesting applications of the GNSS signals is the Earth gravity modeling. In order to do so, at least one LEO satellite orbits the Earth and records the raw navigation data which includes observations and ephemerides. These records are then transmitted to the ground station and processed to determine an accurate gravity model of the Earth [20, 21]. There are two types of gravity field modeling: static and temporal. Static gravity model provides the information about the general mass distribution of the earth while temporal gravity field provides the information such as accumulative continental water and water mass distribution of oceans [22]. There are currently two missions that provide data for Earth gravity modeling: Gravity Field and Steady-State Ocean Circulation Explorer (GOCE) [23] and Gravity Recovery and Climate Experiment (GRACE) [24, 25].

1.3.9 High Resolution Ionospheric Sounding

One of the layers of the Earth's atmosphere is the ionosphere which consists of charged particles (electrons and protons) generated by solar radiations. Using GNSS signals, it is possible to sound the Earth's ionosphere. The ionospheric sounding process uses the effect of the ionosphere on the GNSS signals in order to map the ionosphere. The group refractive index determines the propagation velocity of the GNSS signals in a medium [26]. The delay caused by the medium is

frequency dependent. Thus, two frequency bands are used in ionosphere sounding using GNSS signals. Since the code and data are known beforehand, the delays can be calculated and, by knowing the positions of the signal sources and receiver, the model of the ionosphere can be generated [27]. In GNSS applications where single frequency receivers are used, this ionospheric effect is a major source of error and, by utilizing the ionospheric map, this error can be largely removed [28].

1.3.10 Atmospheric Limb Sounding

Electromagnetic signals bend while passing through an atmosphere, depending on the pressure, temperature and humidity of the medium. These atmospheric parameters can be measured by using the bending property of the GNSS signals. The measurement can be performed by a LEO satellite for example. In this case, the LEO satellite is searching for GNSS signals which are transmitted at low elevation angles. Since the received GNSS signals are bent in the atmosphere as they pass through it, the parameters can be calculated by knowing the accurate position of the LEO satellite (from the GNSS signals in view) and positions of the GNSS satellites [29, 30]. One mission that has provided valuable information on atmospheric limb sounding was Challenging Mini-satellite Payload (CHAMP) satellite which completed its mission on 19th September 2010 [31].

1.3.11 GNSS Reflectometry

Measuring and monitoring the ocean and sea levels, wave height as well as the near surface wind speed and directions are of interest to meteorologists. Having these measurements in real-time provides a powerful means for disaster warning and monitoring. GNSS signals can be used for this purpose. Antennas of the GNSS receiver on-board a LEO satellite are placed in such a way that they receive both direct GNSS signals and the GNSS signals reflected from the surface of the ocean. The reflected signals are affected by the ocean level, wave height and the near surface wind speed and direction. Analyzing the characteristics of the reflected signals allows to provide those information [32–34].

1.4 GNSS Receivers in Space

In the previous sections, some applications have been introduced which rely on GNSS receivers operating in space. In addition, the current trend of commercialization of space missions calls for flexible, low-power and low-cost spacecraft. Subsystems and sensors of these spacecraft shall meet stringent criteria such as low power, small size and mass in addition to compliance to the environmental

Table 1.1: Characteristics of selected space capable GNSS receivers

Receiver model	Manufacturer	GNSS signal	Frequency bands	Power consumption [W]	Mass [g]
Phoenix [37]	DLR	GPS	L1	0.85	20
SGR-05U [38]	SSTL	GPS	L1	0.8	40
SPACENAV [39]	BAE Systems	GPS	L1	6	1600
SGR-10 [40]	SSTL	GPS	L1	5.5	950
BlackJack [41]	JPL	GPS	L1 + L2		
IGOR [42]	JPL	GPS	L1 + L2	16	4600
OEM4-G2 [43]	NovAtel	GPS	L1 + L2	2.5	85
PolaRx2 [44]	Septentrio	GPS	L1 + L2	5	120
		SBAS	L1		
TriG [45]	JPL	GPS	L1 + L2 + L5	50	6
		Galileo	E5a		

requirements for space applications. One of the most important subsystems on a satellite is the guidance, navigation and control (GNC) subsystem. The addition of GNSS receiver in the GNC subsystem of low-cost and small spacecraft improves their performance and provides new opportunities for new applications. Missions BIRD [35] and PRISMA [36] are two small satellite missions demonstrating such improvements. As mentioned earlier, extra requirements shall be considered for space capable subsystems, thus for GNSS receivers which are addressed in more details in section 2.4.2. Traditional spaceborne GNSS receivers can be bulky and power hungry. Table 1.1 provides a list of selected space capable GNSS receivers.

The results of previous studies show that commercial-off-the-shelf (COTS) integrated circuit (IC) technologies can be used to provide flexible, low-power, low-mass, low-cost and flexible solutions for spaceborne GNSS receivers [46]. Thus, by using the latest microelectronics technology, small, flexible and low-power GNSS receivers can be designed and implemented which are suitable for new space missions which is the approach of this work.

1.5 State-of-the-art IC Technology

IC technology developers in terrestrial applications have been focusing on low-power and miniaturized systems for the last decades. These new technologies have the potential to be implemented in space as well. Thus, the trend of space technology developments is also moving from high power consuming, bulky and costly systems towards low-power, small, low-cost and flexible systems.

The developments in new technologies especially in microelectronics, micro-electro-mechanical systems (MEMS) and their packaging provide opportunities for innovations in spacecraft design. Such innovations have the potential to reduce the development costs and time to market. Obtaining such ability provides a chance to define and develop new and innovative space applications. This is especially true for applications which ask for short time to market that were not feasible due to the traditionally long development times of space missions and their dedicated space capable components.

Applications drive the type of space missions. It could be a single spacecraft mission where one spacecraft is sufficient to achieve the objectives or a multi-spacecraft system which collectively performs the task [47]. In either case, the spacecraft can benefit from multi-purpose and flexible systems which can be low-power and low-cost by employing new technology. Using such spacecraft provides the opportunity of designing more sophisticated missions which can perform, e.g. even in-situ reconfiguration of the mission. One example of such system is a GNSS receiver capable of adapting the number of used frequency bands depending on its power constraint and the required accuracy. There are operation scenarios, e.g. in scientific missions, where multiple GNSS bands are essential to achieve high accuracy results which in turn means high power consumption. During the operation, it is possible that available power becomes limited. Thus, operation mode can switch to a simple single-band navigation until the nominal power is restored. Such a GNSS receiver would provide an extra degree of freedom in operation in terms of real-time accuracy-power balance. However, such flexible receivers are not yet existing.

1.5.1 Standard IC Technology in Space

Due to special environment requirements of space missions, space-qualified electronics technology is extremely expensive. This rules out the use of such technology for low-cost applications and mass production. On the other hand, developments in standard IC technologies, i.e. IC technology used in terrestrial applications, as well as the more demanding design requirements for their applications, make them promising to be used in space as well.

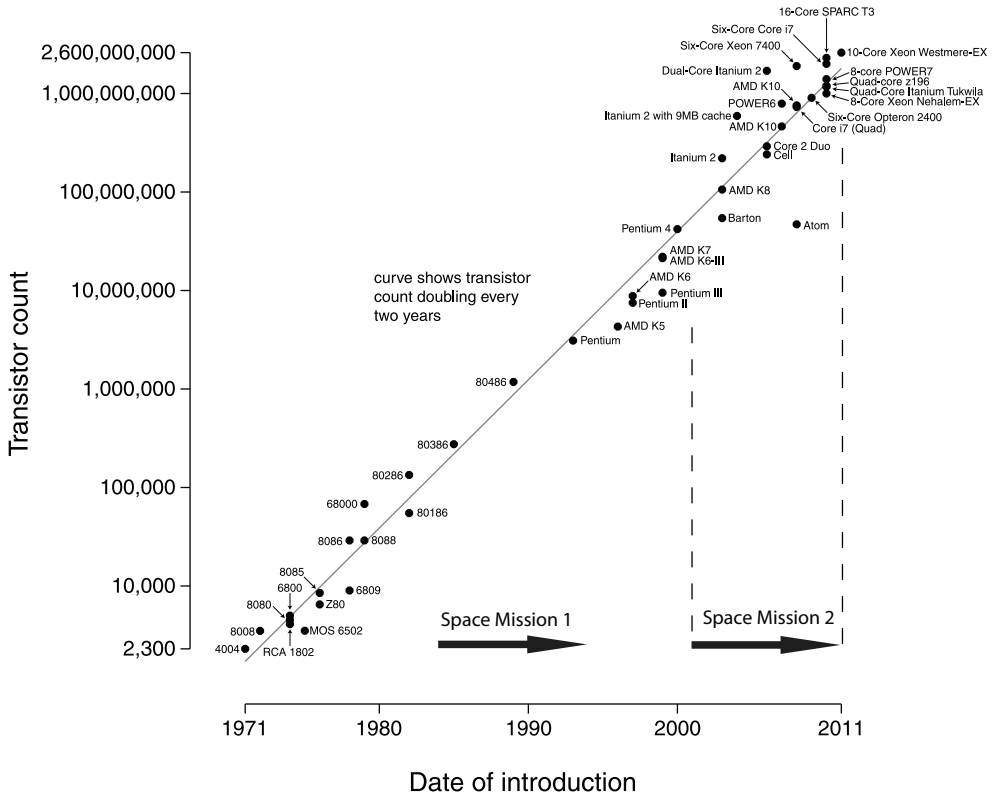


Figure 1.4: Speed of advances in IC technology in time (Moor's law) in comparison with average space mission development duration (~ 10 years)

In order to be able to use standard IC technologies in space, there are a number of parameters which shall be considered for space applications. These parameters, all together, assure the operability and fault tolerance of the spacecraft during the mission. Thermal and vacuum conditions and radiation tolerance are the most important parameters for designing electronic systems for space which will be addressed later. The dimensions of the ICs are in the range of millimeters which are very small compared to the exposed maximum sinusoidal vibration wavelength of typically larger than 3 m in air [48, 49]. The vibration effects are of mechanical nature and will not be discussed in this thesis.

1.5.2 Trends in IC Technology for Space Applications

In traditional spacecraft design, the spacecraft is divided in a number of subsystems and the payload. Each of these subsystems and payload is designed separately based on the requirements which are defined by systems engineers and

originated from requirements at mission level. The complete spacecraft is then developed by integrating all these subsystems and payload [50, 51]. In this approach, each spacecraft is custom-made and the development time is long. With development times of up to 25 years for some missions, the employed technologies would be out-dated by the time the mission is ready to launch because of the fast developments in those technologies. For example, advances in commercial IC technology have been following Moore's law which states that the number of transistors on integrated circuits doubles approximately every two years [52]. Thus, each spacecraft is designed specifically based on the state-of-the-art technology at the time of the preliminary design which may result in bulky and expensive spacecraft with moderate functionality. Fig. 1.4 depicts the speed of advances in IC technology in time (Moore's law) in comparison with average space mission development duration. Considering an average space mission development time of about 10 years, it can be observed that IC technology has faced huge development. However, this traditional design methodology is suitable for designing special and task-specific spacecraft.

The current state-of-the-art IC technology is suitable for designing components for fast time-to-market applications. This experience can be spun into space mission design. Using the standard IC technology in space applications provides opportunities to define new approaches in spacecraft design as well as many new applications based on multi-purpose, flexible, low-power and low-cost spacecraft. The trend of commercialization of space missions demands for reduction in cost as well as time-to-market of new applications to dominate the market.

In order to satisfy such demands, the spacecraft design methodology should be modified. The modifications can start at subsystems which are common in many spacecraft such as communication and navigation. Traditionally, these subsystems are part of the system bus. Since these are similar for different spacecraft, a common design can be used for them. Moreover, it is possible to add reconfigurability to the design such that a subsystem can be adapted and used for several missions. In this case, the concept of mass production, demonstrated for some missions in the past, like Iridium [53], could become feasible as common production approach [54].

Similar to other mass productions, a smart, tunable (or reconfigurable) system should be designed to cover various needs. Mass production is motivated by not only the cost reduction but also the fast time to market of new applications. The state-of-the-art technology will not drastically change during the mission design which makes it possible to use the same technology in many missions which can lead to plug-and-play design concepts. On the other hand, availability of components and design libraries can render modifications of the spacecraft faster at later stages.

Table 1.2: SWOT analysis of standard IC technology used in space

Strengths	**Weaknesses**
- Mature technology - Low cost - Fast time-to-market	- Lower radiation tolerance - Insufficient technology readiness level (TRL) for space use
Opportunities	**Threats**
- Mass production - New space applications - Plug and play design - New approaches in spacecraft design	- Acceptance by space community - Availability

Table 1.2 shows the SWOT analysis of the usage of standard IC technologies in space. The standard IC technology is used to develop millions of devices used daily in terrestrial applications from highly critical systems up to consumer electronics. Thus, it is of high maturity level. The cost of its research and development makes it an expensive technology. However, considering the huge number of units and applications using it, the final product can still be considered as low-cost. The time-to-market is reduced due to the developed experience of experts who are using standard IC technology in their application developments.

As explained previously in this section, mass production, new space applications, plug and play design and new approaches in spacecraft design are opportunities awaiting for exploration and realization.

The standard IC technology is mainly developed for terrestrial applications. Thus, harsh environmental conditions such as radiation should be taken into account when adopting it for space applications. Since it has been incorporated in a limited number of space missions, its technology readiness level (TRL) is typically still insufficient for space applications. It should be investigated when the space community is ready to accept standard IC technology as regular practice for their missions and what design concepts it would apply (e.g. redundancy FDIR). Furthermore, the extend to which non-space industries would be interested to make themselves available for such developments remains to be clarified.

1.5.3 System Integration

Printed circuit boards (PCB) are the commonly used to integrate electronic circuits of subsystems. On these PCBs, electrical and electronic (discrete) components such as connectors, fuses, resistors, capacitors, transistors, ICs, etc. are placed and connected properly. The state-of-the-art IC technology provides means to further

miniaturize the subsystems. In this way, more discrete components are integrated in chips. Ultimately, the complete subsystem can be integrated in a single chip.

There are two different ways to integrate systems on a chip. It can be system on chip (SOC) or system in package (SIP). In SOC, all subsystems are ready as IC design libraries and will be placed together in the final layout and sent for fabrication. An IC design library is a set of fully functional and tested designs which are ready to be manufactured. However, SOC requires all design libraries to be in the same IC technology process, e.g. 0.13 μm Complementary Metal-Oxide Semiconductor (CMOS) technology. Once a design library is validated in a certain CMOS technology, in most situations, it can be transferred to other feature sizes as well.

Forcing designers to follow a specific technology may increase the development time. In order to avoid such problems, SIP is a suitable solution. In SIP, different subsystems are integrated in the same IC package even though they are on separate dies. Using SIP also provides the opportunity to integrate MEMS systems in the same package. The interconnections between the subsystems can be with bond wires. Although the bond wires are secured during packaging they can be a point of failure.

As an alternative, a wireless internal communication between subsystems has been proposed in the framework of MicroNed research program [55]. In this approach, the bus, subsystems and payload will contain wireless communication units which follow the same communication protocol to establish an internal network. The complete spacecraft can be integrated by securing them in the same package. In this way, the total mass of the complete system will be a few grams and the total size will be a few square millimeters.

1.6 Thesis Objectives

In the previous sections, the trends of spacecraft electronic system development have been discussed. There are two main developments in this trend: incorporating standard IC technology in space and integrating multiple subsystems (or functions) on a single chip. The type of subsystems gathered on a chip depends on the commonalities and the relations between them.

One of the subsystems in a spacecraft is the GNC subsystem. The purpose of navigation can be one or more of the applications as introduced in section 1.3. At the time of writing this thesis, GPS and GLONASS are fully operational and Galileo and Compass are partially in operations. However, there are few receivers which can use all of these navigation systems at the same time.

As will be explained in chapter 2, GNSS receivers consist of an analog front-end and a digital back-end. The digital back-end is mainly a processor which runs

algorithms. Some functions within these algorithms, like correlation, can use implementation in dedicated hardware to increase processing speed. Thus, adding the capability of processing new GNSS signals, either from the same GNSS system in a different band or other GNSS systems, is more of a programming challenge than hardware design challenge. On the other hand, adding the same capability from the analog front-end design point of view is a hardware challenge. Most of the receivers introduced in Table 1.1 process a limited number of bands and GNSS systems. The multi-band ones are limited in band selection flexibility. In addition, the only one which processes most bands and GNSS systems, i.e. TriG, consumes 50 W which is a huge amount of power for most GNSS applications in space. The front-end plays an important role in the flexibility and total power consumption. It is important to investigate the common features in these GNSS signals which can be used to develop a single front-end to process as many GNSS signals as possible.

The research objective of this thesis is to develop a space-capable, flexible, multi-purpose, low-power and low-cost GNSS receiver front-end. This front-end shall be able to process GNSS signals from different GNSS systems and different frequency bands. The research questions addressed in this thesis are:

RQ1 - What are the commonalities between GNSS signals from different GNSS systems and different frequency bands which can be used to develop a common front-end for them?

RQ2 - What is the most suitable architecture for a space-capable, flexible, multi-purpose, low-power and low-cost front-end?

RQ3 - What are the characteristics of this architecture and how it can be verified?

RQ4 - How to implement this architecture?

The research starts with investigation of the user requirements followed by an extensive study of different GNSS signal structures. The common characteristics of different GNSS signals are investigated and an innovative front-end architecture is designed based on those characteristics. In order to design this front-end, different front-end architectures are studied and their advantages and disadvantages are analyzed taking into account the common characteristics of the GNSS signals. The best front-architecture with the possibility of resolving the drawbacks is selected. Then, an innovative solution is provided to resolve the existing drawback. The entire front-end is simulated on system level. Finally, the architecture is designed on transistor level using United Microelectronics Corporation (UMC) 0.13 μm CMOS technology and the circuit is simulated and verified. Although the front-end is developed for space applications, it can be used for terrestrial applications as well.

1.7 Thesis Structure

In this chapter, a brief overview of the navigation systems and their applications as well as the developments in new IC technologies have been introduced. In order to be able to use the GNSS signal for the above mentioned applications and to open the door for future new applications, innovative receiver hardware architectures need to be developed. In this thesis, the focus is to develop an innovative front-end architecture of a GNSS receiver for such purposes. Chapter 2 provides an overview on generic GNSS receivers and their operation principles. Chapter 3 shifts the focus on receiver front-end architectures and introduces different existing front-end architectures. The proposed innovative front-end architecture is developed and presented in chapter 4 and is explained at system level. In chapter 5, the transistor level front-end is developed and presented in detail with results and simulations. The thesis is concluded in chapter 6 with a summary of achievements, recommendations for future work and outlook.

2
GNSS Receivers

GNSS systems and their applications were introduced in the previous chapter. In this chapter, GNSS signals and receivers will be explained in more detail. The main focus will be on GPS and Galileo satellite navigation systems.

First, the fundamentals of satellite positioning will be discussed, then GPS and Galileo signals will be reviewed. In the sequel, a generic GNSS receiver architecture will be introduced. Finally, the requirements of receivers for space applications will be discussed.

2.1 Fundamentals of Satellite Positioning System

The basic concept of satellite positioning is based on trilateration. In this approach, the distance of an object from several reference points is measured. In three-dimensional space, the object is located on the intersection of surfaces of several spheres. The centers of these spheres are placed at the reference points and their radii equal the distance of each reference point to the object. In three dimensional space, at least four reference points are required to have an unambiguous solution as shown in Fig. 2.1. As depicted in this figure, two spheres intersect in a circle and a third sphere intersects with the aforementioned circle resulting in two locations. A forth measurement selects the correct location. If the vicinity of the position of the object is known and is significantly smaller than the smallest radius then three reference points are sufficient.

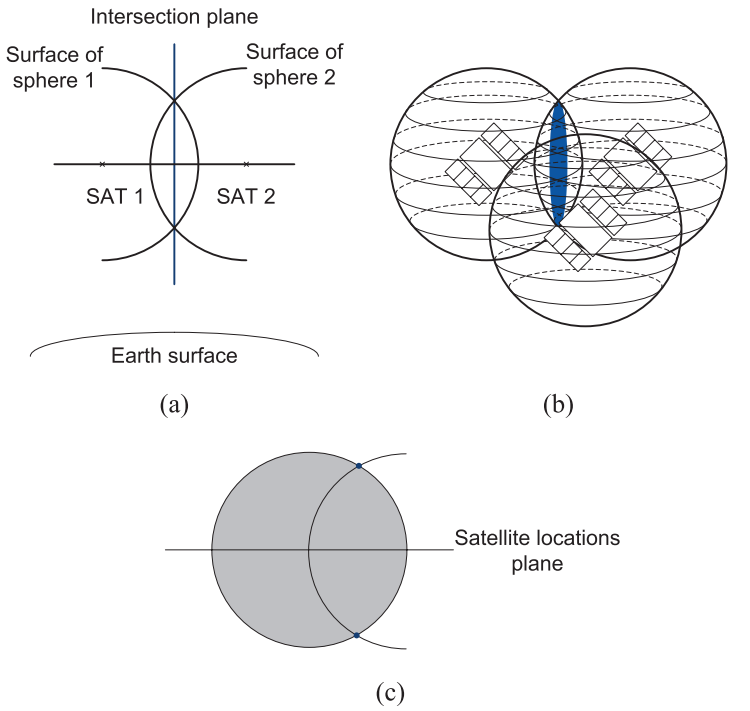


Figure 2.1: Using trilateration to find position a) cross section of two spheres and their intersection plane b) intersecting three spheres c) cross section of the third sphere intersecting with the intersection plane in (a)

In satellite navigation systems, the reference points are GNSS satellites and the distance is determined by measuring the traveling time of the signal from the satellite to receiver. The measurement is based on the time of arrival (TOA) concept [56]. In this method, the transmission time is known and the received time is measured. Thus, the traveling time of the signal can be determined. The line which connects the receiver and the satellite is called the line of sight (LOS).

For sake of simplicity, Fig. 2.2 shows the vectors in an arbitrary reference frame. In this figure, the LOS vector, $\bar{r}_i$, can be expressed by two other vectors, $\bar{u}$ and $\bar{s}_i$, where $\bar{u}$ is the vector from Earth center to the user receiver and $\bar{s}_i$ is the vector from Earth center to GNSS satellite. Thus,

$$\bar{r}_i = \bar{s}_i - \bar{u}. \tag{2.1}$$

Using vector algebra, (2.2) shows the amplitude r_i

$$r_i = \|\bar{r}_i\| = \|\bar{s}_i - \bar{u}\| \tag{2.2}$$

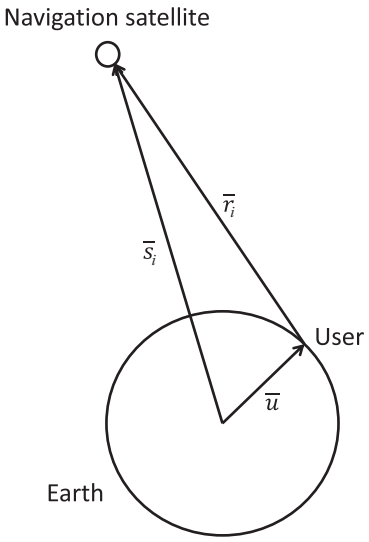


Figure 2.2: Vector representation of user position

where r_i is called the range. From this equation, it can be concluded that the position of the receiver can be determined by known satellite positions and the distance between the receiver and an appropriate number of satellites.

One way to measure the distance between the receiver and the satellite is using the transmitted radio signal from the satellites. The propagation velocity of the radio signal equals to velocity of light. Considering the traveling time of this signal to be Δt_i as shown in Fig. 2.3, the range of the i$^{\text{th}}$ satellite can be determined by

$$r_i = c(t_{1i} - t_{2i}) = c\Delta t_i \tag{2.3}$$

where t_{1i} is the transmit time of the signal of the i$^{\text{th}}$ satellite, t_{2i} is its receive time (TOA) and c is the velocity of light. However, due to finite velocity of light as well as rotation of Earth, the relative position r_i at t_{2i} is different from the true signal path. Thus, (2.1) can be written as

$$\bar{r}_i = \bar{s}_i(t_{2i} - \Delta t_i) - \bar{u}(t_{2i}). \tag{2.4}$$

The signal travel time, Δt_i, may be computed from the implicit light-time equation [57]

$$c\Delta t_i = \|\bar{s}_i(t_{2i} - \Delta t_i) - \bar{u}(t_{2i})\| \tag{2.5}$$

in an iterative manner.

In practice, there are various sources of errors that should be considered in the position determination. One of the main sources of error is the clock error of the

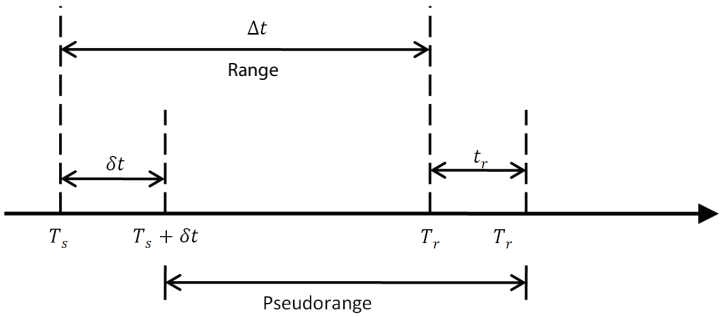


Figure 2.3: Range measurement timing relationship

navigation satellites as well as that of the receiver. All clocks should ideally be tracking the system time. Thus, the biases and drifts of the satellite clock and the receiver clock with respect to the system time should be corrected.

Taking the clock error into consideration t_{1i} should be replaced by $T_{si} + \delta t_i$ and t_{2i} by $T_{ri} + t_r$ where T_{si} is the system time at transmission of the signal from the satellite and δt_i is the satellite clock error. Furthermore, T_{ri} is the system time at which the signal reached the receiver and t_r is the receiver clock error. In practice, the calculated range is not the geometric range since it includes these clock offsets. The measured quantity, ρ_i, is called pseudorange which can be determined by

$$\begin{aligned} \rho_i &= c[(T_{ri} + t_r) - (T_{si} + \delta t_i)] \\ &= c(T_{ri} - T_{si}) + c(t_r - \delta t_i) \\ &= r_i + c(t_r - \delta t_i). \end{aligned} \tag{2.6}$$

Satellite clock errors can be corrected using the transmission clock correction parameters which are a part of navigation data. Combining (2.6) with (2.2) and using Cartesian coordinates for vectors, we have:

$$\rho_i = \sqrt{(x_{si} - x_r)^2 + (y_{si} - y_r)^2 + (z_{si} - z_r)^2} + c(t_r - \delta t_i) \tag{2.7}$$

where ρ_i is the pseudorange to the i$^{\text{th}}$ satellite, x_{si}, y_{si} and z_{si} are coordinates of the i$^{\text{th}}$ satellite and x_r, y_r and z_r are coordinates of the receiver. Equation (2.7) can be used to determine the position of the receiver. In order to find the position, at least four satellites should be in view to be able to solve for the four unknowns x_r, y_r, z_r and t_r. The satellite position and time error, i.e. x_{si}, y_{si}, z_{si} and δt_i, are provided in the ephemeris message broadcast by spacecraft.

GNSS satellites use a special signal, called pseudorandom noise (PRN) code, to measure the traveling time. PRN codes are digital sequences of zeros and ones that

are designed such that their cross-correlation is almost zero and their autocorrelation has only one large peak. It will be discussed later in this chapter how the characteristics of the PRN codes provide the opportunity to measure the traveling time.

In an ergodic random process, the time average and time autocorrelation function equal the statistical average and autocorrelation function respectively. It is mentioned in [58] that "*A series of satellites with similar and stationary ranging error statistics over successive sample intervals may be viewed as behaving in an approximately ergodic manner*". Thus for GNSS signals an ergodic random process behavior can be considered. In general, the autocorrelation, R, of an ergodic signal $S_{bb}(t)$ can be calculated by [59]

$$R(\tau) = \lim_{T\to\infty} \frac{1}{2T} \int_{-T}^{T} S_{bb}^{*}(t) S_{bb}(t+\tau)\, dt \tag{2.8}$$

where τ is the time shift and T is the time period of the signal. For a random process which is at least wide-sense stationary, the Wiener-Khintchine relations state that the power spectral density (PSD), $S(f)$, of such a process is the Fourier transform of its autocorrelation function [59]

$$S(f) = \int_{-\infty}^{\infty} R(\tau) e^{-j2\pi f\tau}\, d\tau \tag{2.9}$$

where f is frequency and τ is time.

PRN codes can be approximated by random binary codes without periodic components, although, exceptionally, the GPS C/A code does not fit this model very well. The waveform transmitted in response to each element of the PRN code sequence is known as the spreading symbol. In BPSK modulation, the spreading symbol is a rectangular function of time whose duration is T_c, also known as the chip length. The chipping rate is measured in chips per second (cps). In an ideal case, with infinite bandwidth, the transition time between two adjacent spreading symbols (chips) is zero. This is the case for the illustrated DSSS signal generation in Fig. 2.6. For a rectangular spreading symbol with infinite bandwidth, and signal amplitude $\pm A$, the power spectral density can be described by

$$S_{PRN}(f) = A^2 T_c \frac{\sin^2(\pi f T_c)}{(\pi f T_c)^2} \tag{2.10}$$

The autocorrelation function cannot have an arbitrary form as explained in [59]. Thus, based on (2.9) and (2.10) (via the Wiener-Khintchine Theorem), the autocorrelation function of an idealized PRN code is:

$$R_{PRN}(\tau) = \begin{cases} A^2(1 - \frac{|\tau|}{T_c}) & , \quad |\tau| \le T_c \\ 0 & , \quad \text{otherwise} \end{cases} . \tag{2.11}$$

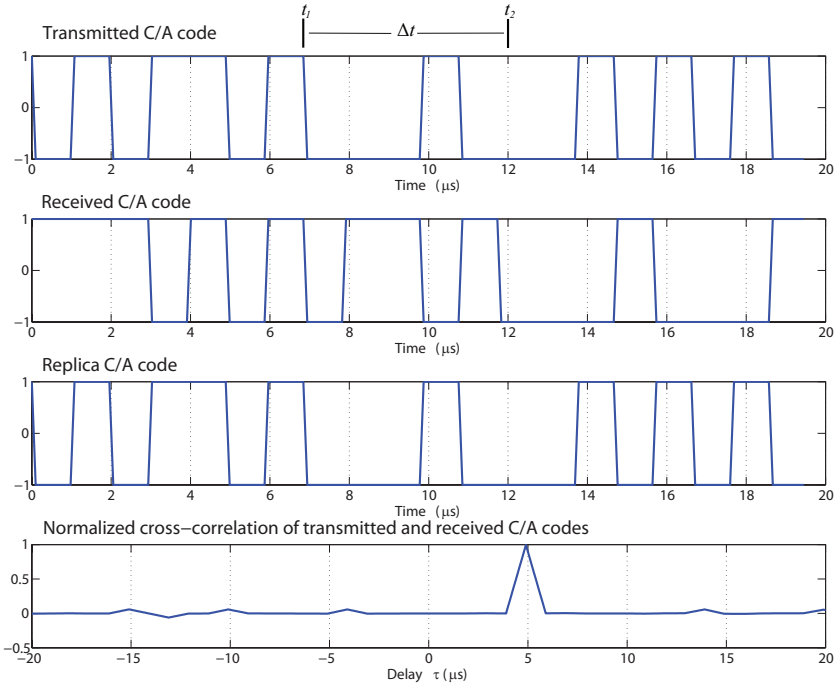


Figure 2.4: Use of replica code to determine satellite code transmission time

Satellite Navigation System providers are required to declare and limit the bandwidth of the satellite transmissions (ITU Regulations). In practice, equations (2.9) and (2.10) are modified to reflect the finite bandwidth effects.

In order to use the aforementioned property, each GNSS satellite generates a unique PRN code. A replica of this PRN code is generated in the receiver. This replica is then aligned with the received signal to determine the delay. Assuming the receiver clock is synchronized with the satellite reference clock, this delay would be equivalent to the traveling time which is shown by Δt in Fig. 2.4.

Fig. 2.4 shows how the traveling time is determined in the receiver. Fig. 2.4a shows the transmitted signal. The beginning of the PRN sequence is at t_1. The receiver receives the signal after a delay of Δt at time t_2, shown in Fig. 2.4b. Fig. 2.4c shows the replica of this PRN code which is generated in the receiver synchronous with the satellite. The cross-correlation of the received signal and the replica is calculated. The replica is shifted such that the cross-correlation results in a large peak as shown in Fig. 2.4d. This peak shows the time shift, τ, where the received signal and the replica are synchronized. This time shift is equivalent to traveling

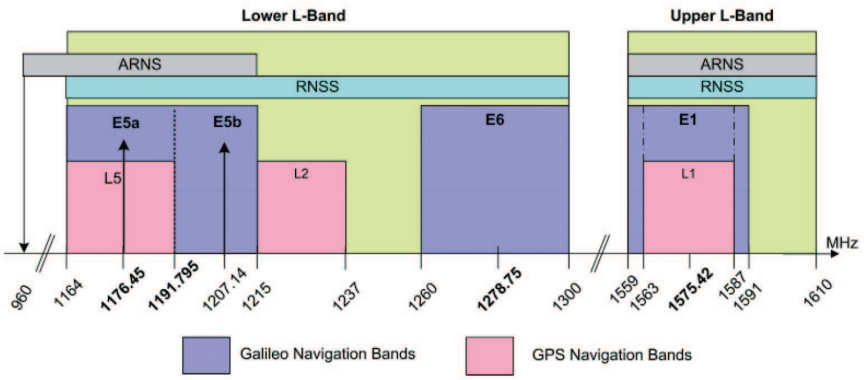


Figure 2.5: GPS and Galileo frequency plans [64]

time which is 5μs in this example.

2.2 GNSS Signals

As mentioned earlier, several countries have already launched their own GNSS system. Among them, NAVSTAR GPS from United States and GLONASS from Russia are fully operational with global coverage, Galileo from European Union will be fully operational in a few years. Other GNSS systems provide local coverage at this time.

Fig. 2.5 shows the frequency plan of GPS and Galileo systems. Current design of GPS and Galileo signals shows similarities in many ways thus, the main focus of this thesis will be on these two systems. As will be described later in this chapter, these two systems, in some bands, use the same carrier frequency and their bandwidths are very close or even the same. Their signal power levels are at the same range and their modulation is code division multiple access (CDMA).

Currently, GLONASS is using a different signal modulation. It uses frequency division multiple access (FDMA) and their frequency ranges are different from GPS and Galileo [60]. The plan for future GLONASS system is to add a new set of signals similar to GPS and Galileo, i.e. same carrier frequencies with CDMA based modulation [61–63].

In order to have the receiver front-end which can receive all the three mentioned GNSS systems, the current design of GPS and Galileo signals has the potential to share the receiver front-end while GLONASS needs a separate one. In the future, when GLONASS activates its new signals, the same receiver front-end can also be used to receive GLONASS.

2.2.1 GPS Signal Structure

In order to distinguish between the signals of GPS satellites, the information of each satellite (navigation data) is mixed with a unique PRN code and transmitted on a fixed carrier frequency. These PRN codes are chosen such that their cross-correlation is zero and their auto correlation gives a high peak when the codes are completely aligned as explained in the previous sections. This method of data transmission is called code division multiple access (CDMA).

The navigation data provides information such as transmission time, space vehicle (SV) accuracy, SV health, SV clock correction, navigation message correction table, ephemeris parameters, almanac data, Coordinated Universal Time (UTC) and ionospheric data. Navigation data is transmitted with a different symbol rates in different bands as will be discussed in the following sections.

The legacy GPS satellites transmit two types of PRN codes: coarse acquisition (C/A) code and precise (P(Y)) code. C/A code is used for civil applications and provides low accuracy positioning while P code is used for precise positioning and might be encrypted (Y code). C/A code has a chipping rate of 1.023 Mcps with a duration of 1 ms. P(Y) code has a chipping rate of 10.23 Mcps with a duration of one week. If the signal is not aligned in autocorrelation the result will be -30.1 dB for C/A code and -127.9 dB for P(Y) code [56]. Navigation data and PRN codes are transmitted using three carrier frequencies located at 1575.42 MHz (L1), 1227.6 MHz (L2) and 1176.45 MHz (L5). The structure of GPS signals will be discussed in the following.

GPS L1

CDMA modulation is also called direct sequence spread spectrum (DSSS) modulation since the frequency spectrum of the information signal is spread by a PRN code. Fig. 2.6 shows the process of generating the DSSS signal. As shown in Fig. 2.6, navigation data of the i^{th} satellite, $D_i(t) \in \{-1,+1\}$, is multiplied by its unique PRN code, $C_i(t) \in \{-1,+1\}$, and the carrier to generate the DSSS signal which is depicted in the figure on the bottom.

Equation (2.12) gives the mathematical expression of the transmitted signal at L1:

$$CA_{L1i} = \sqrt{2}AD_i(t)C_i(t)\cos(\omega_1 t) \tag{2.12}$$

where CA_{L1i} is the C/A part of the transmitted signal, A is the amplitude of the signal and ω_1 is the L1 carrier frequency. The P(Y) code is transmitted on the same frequency with 90° carrier phase shift and 3 dB less power. The mathematical ex-

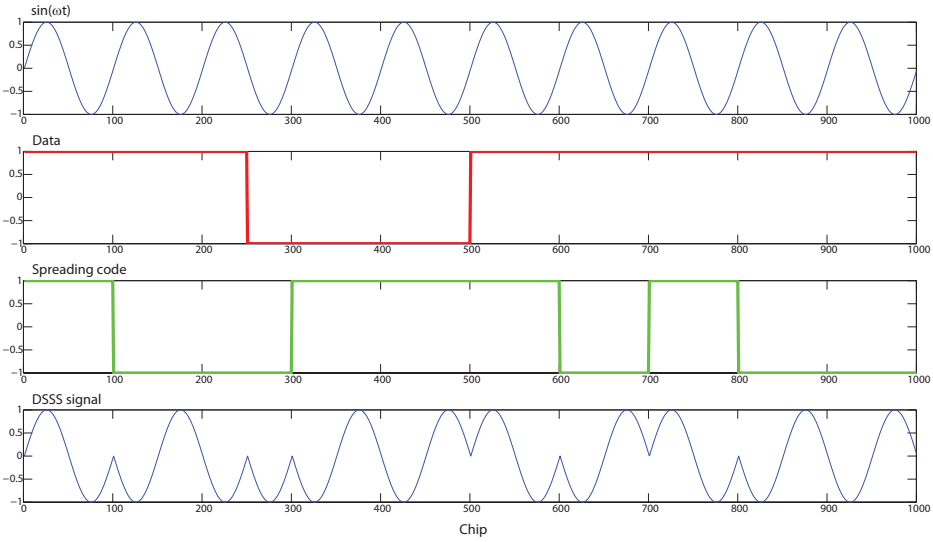


Figure 2.6: DSSS Signal generation

pression of P(Y) code is given by:

$$P_{L1i} = AD_i(t)P_i(t)\sin(\omega_1 t) \tag{2.13}$$

where P_{L1i} is the P(Y) part of the transmitted signal and $P_i(t) \in \{-1,+1\}$ is the P(Y) code. Equations (2.12) and (2.13) lead to the complete transmitted signal at L1:

$$\begin{aligned} L1_i = &\sqrt{2}AD_i(t)C_i(t)\cos(\omega_1 t) \\ &+ AD_i(t)P_i(t)\sin(\omega_1 t). \end{aligned} \tag{2.14}$$

The modernized GPS signals at L1 band will include a new civil signal (L1C) in the Block III and subsequent satellites. A military (M) code is included in the Block IIR-M and will continue in the subsequent satellites. L1C consists of two main components, L1C_{Pi} and L1C_{Di}. The former is a pilot signal which contains no navigation data and the latter includes navigation data. Each satellite has a unique third overlay code (L1C_{Oi}) which modulates the L1C_{Pi}.

L1C signal uses binary offset carrier (BOC) modulation. The BOC signals are generated by modulating the DSSS signal with an additional square sub-carrier as depicted in Fig. 2.8. It is typically denoted by BOC(m, n) where m and n are defined as

$$m = \frac{f_{sc}}{f_{ref}} \quad , \quad n = \frac{f_c}{f_{ref}} \tag{2.15}$$

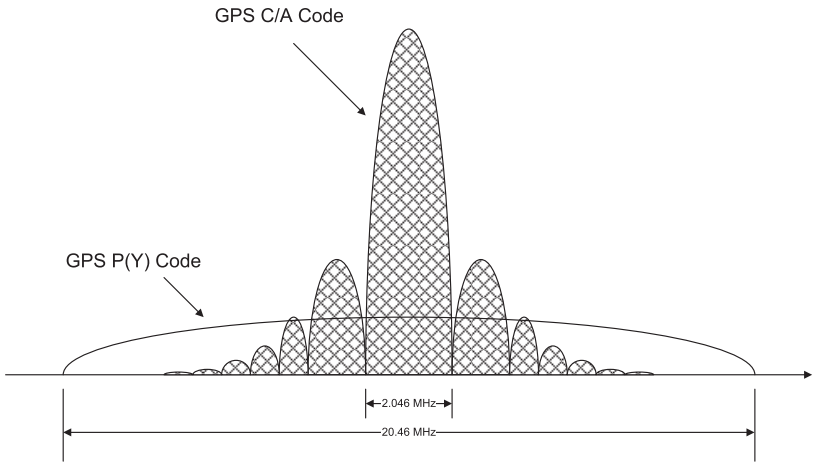


Figure 2.7: GPS C/A and P code spectrum

where f_{sc} is the sub-carrier frequency, f_c is the chipping rate and f_{ref} = 1.023 MHz is the reference chipping frequency. The frequency spectrum of the BOC(m,n) has two peaks with f_{sc} distance on each side of the carrier frequency and each with main lobe band width of $2 \times f_c$. Fig. 2.9 depicts the spectrum of BOC(1,1) signal. In this figure, the sub-carrier frequency is at 1.023 MHz and chipping rate is 1.023 MHz.

L1C$_{Di}$ uses BOC(1,1) modulation while L1C$_{Pi}$ uses time-multiplexed BOC (TMBOC) modulation. The TMBOC for L1C$_{Pi}$ is a combination of BOC(1,1) and BOC(6,1) [65].

GPS L2

The legacy GPS L2 signal consists of navigation data modulo-2 added by either P(Y) code or C/A code. The code selection is performed by ground command. There is a third selectable operation mode by ground command in which the signal only consists of P(Y) code without navigation data [66].

The signal structure is slightly changed in Block IIR-M and Block IIF and subsequent blocks of GPS satellites. New civil and military codes will be added to L2 band in quadrature-phase with the legacy L2 signal. The new L2 civil signal (L2C) can be formulated by

$$C_{L2i} = AD2_i(t)C2_i(t)\cos(\omega_2 t) \tag{2.16}$$

where $D2_i(t) \in \{-1,+1\}$ is the L2 civil navigation data (CNAV) and $C2_i(t) \in \{-1,+1\}$ is the L2C code. $D2_i(t)$ contains more accurate data than $D_i(t)$ and is transmitted

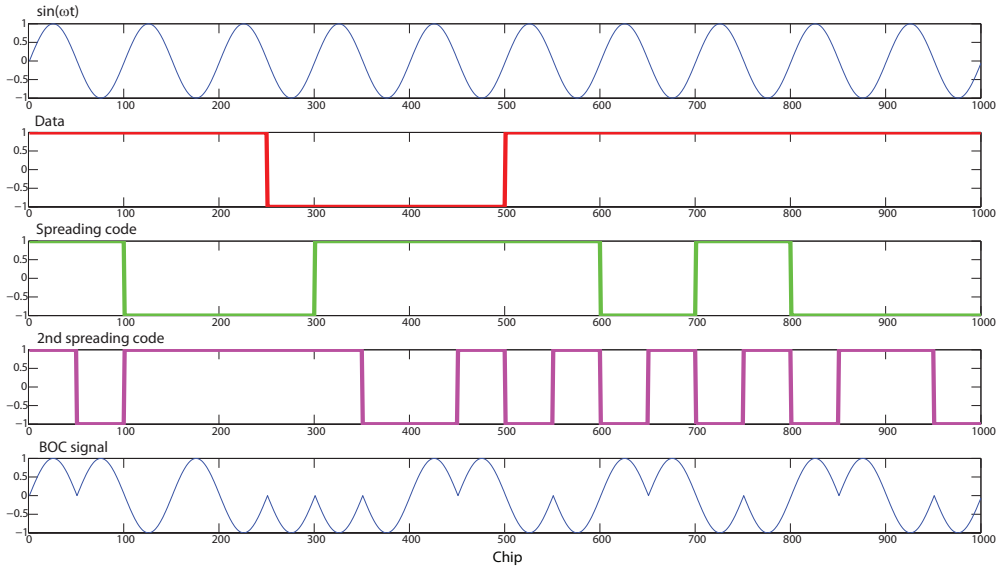


Figure 2.8: BOC signal generation

at the rate of 25 sps in L2 band. L2C code is longer than the C/A code and consists of two components: CM (civil moderate) and CL (civil long). These two codes are chip-by-chip time multiplexed to generate the L2C code. The chipping rate is 1.023 Mcps which provides the same accuracy as C/A code. However, the length of the code is significantly longer. The CM code has a length of 10230 chips and the CL code is 767250 chips long. There is an additional option to use C/A code with or without navigation data, $D_i(t)$, instead of L2C.

Considering the combination of the L2C and P(Y) codes in L2, the complete GPS L2 signal can be given by

$$\begin{aligned} L2_i = {} & AD_i(t)P_i(t)\sin(\omega_2 t) \\ & + AD_{Ci}(t)C2_i(t)\cos(\omega_2 t) \\ & + New\ military\ signal\ (M-code). \end{aligned} \tag{2.17}$$

GPS L5

The GPS L5 signal will be available in Block IIF and subsequent blocks of the GPS satellites. It is designed for civil applications and consists of two PRN codes in phase quadrature: the in-phase ($I5_i(t)$) and the quadrature-phase ($Q5_i(t)$) [67]. These codes are time synchronized and have a length of 10230 chips with 10.23 Mcps chipping rate which makes their period 1 ms. The 50 sps L5 CNAV,

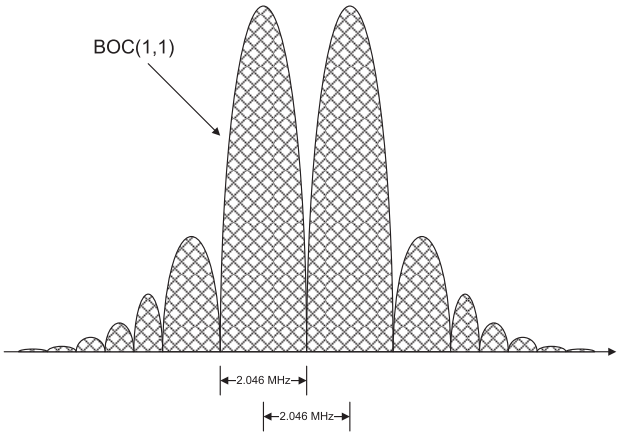


Figure 2.9: BOC(1,1) spectrum

$D_5(t)$, is $\frac{1}{2}$ convolution encoded with a forward error correction (FEC), thus the symbol rate is 100 sps. The L5 CNAV is modulated with the 10-bit Neumann-Hoffman code, $h_I(t)$, (0000110101) with 1000 sps rate. The result is modulo-2 added to the in-phase PRN code to generate $I5_i(t)$. The quadrature-phase component, $Q5_i(t)$, does not include navigation data. It is generated by modulo-2 addition of the quadrature-phase PRN code and the 20-bit Neumann-Hoffman code, $h_Q(t)$, (00001001101010011 10). The 20-bit Neumann-Hoffman code has also 1000 sps symbol rate. Equation (2.18) shows the complete GPS L5 signal:

$$\begin{aligned} L5_i = {} & AD_5(t)h_I(t)I5_i(t)\cos(\omega_5 t) \\ & + Ah_Q(t)Q5_i(t)\sin(\omega_5 t). \end{aligned} \tag{2.18}$$

2.2.2 Galileo Signal Structure

The Galileo navigation system also uses the CDMA modulation concept [68]. The signals are transmitted in three bands: E1, E6 and E5 where E5 is divided into E5a and E5b which can be used individually or combined. Each band is designed to provide a number of services which are open service (OS), safety of life (SoL), commercial service (CS) and Galileo system integrity (SI) monitoring [64]. There is also an encrypted public regulated service (PRS) [69]. Table 2.1 provides the carrier frequencies, bandwidths and the services allocated to each band.

As shown in Table 2.1 and also depicted in Fig. 2.5, E1 and E5a are transmitted on the same frequency carrier as GPS L1 and L5 respectively. This property will be used later in the design. The structure of Galileo signals will be discussed in the following.

Galileo E1

The Galileo E1 signal uses composite BOC (CBOC) modulation. CBOC modulation is similar to BOC however, instead of a single sub-carrier it incorporates two sub-carriers with different frequencies and powers. E1 CBOC signal can be formulated as

$$CBOC = \alpha BOC(1,1) \pm \beta BOC(6,1) \tag{2.19}$$

where $\alpha = \sqrt{10/11}$ and $\beta = \sqrt{1/11}$ are the power coefficients and are selected such that the total power is equal to unity.

The E1 signal consists of two components called E1-B and E1-C. The E1-B component contains PRN code and integrity navigation message (I/NAV) with 250 sps symbol rate and the E1-C only contains the PRN code thus, is called the pilot signal. These two signals are modulated onto the same carrier frequency with 50% power sharing.

Galileo E5

Galileo E5 signal consists of two main parts: E5a and E5b. Both E5a and E5b have the in-phase and the quadrature-phase components (E5a-I, E5a-Q, E5b-I and E5b-Q). The in-phase components include code and navigation data while the quadrature-phase components are pilot signals. The navigation message on E5a is a free access navigation message (F/NAV) with 50 sps symbol rate and the one on E5b is I/NAV with 250 sps symbol rate. These four signals are combined together using AltBOC(15, 10) modulation. Similar to BOC, in AltBOC(m, n), m represents the sub-carrier and n represents the chipping rate.

AltBOC can be considered as an 8-PSK modulation comprising of two independent QPSK signals. The E5 signal can be formulated as [64]

$$E5(t) = e^{j\frac{\pi}{4}k(t)}, \qquad k(t) \in \{1,2,3,4,5,6,7\} \tag{2.20}$$

Table 2.1: Galileo signal frequencies, bandwidth and services [64, 69]

Signal	Carrier frequency (MHz)	Bandwidth (MHz)	Service
E1	1575.420	24.552	OS, SoL, SI, PRS
E6	1278.750	40.920	CS, PRS
E5	1190.795	51.150	OS, SoL, SI
E5a	1176.450	20.460	OS
E5b	1207.140	20.460	OS, SoL, SI

	Input Quadruples															
E5a-I	-1	-1	-1	-1	-1	-1	-1	-1	1	1	1	1	1	1	1	1
E5b-I	-1	-1	-1	-1	1	1	1	1	-1	-1	-1	-1	1	1	1	1
E5a-Q	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1	-1	-1	1	1
E5b-Q	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1
$t' = t$ modulo $T_{s,E5}$	k according to $s_{E5}(t)=exp(jk\pi/4)$															
i_{Ts}	t'															
0	$[0, T_{s,E5}/8[$	5	4	4	3	6	3	1	2	6	5	7	2	7	8	8	1
1	$[T_{s,E5}/8, 2\ T_{s,E5}/8[$	5	4	8	3	2	3	1	2	6	5	7	6	7	4	8	1
2	$[2\ T_{s,E5}/8, 3\ T_{s,E5}/8[$	1	4	8	7	2	3	1	2	6	5	7	6	3	4	8	5
3	$[3\ T_{s,E5}/8, 4\ T_{s,E5}/8[$	1	8	8	7	2	3	1	6	2	5	7	6	3	4	4	5
4	$[4\ T_{s,E5}/8, 5\ T_{s,E5}/8[$	1	8	8	7	2	7	5	6	2	1	3	6	3	4	4	5
5	$[5\ T_{s,E5}/8, 6\ T_{s,E5}/8[$	1	8	4	7	6	7	5	6	2	1	3	2	3	8	4	5
6	$[6\ T_{s,E5}/8, 7\ T_{s,E5}/8[$	5	8	4	3	6	7	5	6	2	1	3	2	7	8	4	1
7	$[7\ T_{s,E5}/8, T_{s,E5}[$	5	4	4	3	6	7	5	2	6	1	3	2	7	8	8	1

Figure 2.10: Values of coefficient $k(t)$ used in AltBOC modulation [64]

where $k(t)$ will be selected from the look-up table given in Fig. 2.10. In this table, the sub-carrier period, $T_{s,E5}$, is divided into 8 equal intervals. The value of $k(t)$ is selected depending on the combination of E5a-I, E5a-Q, E5b-I and E5b-Q signals at that interval.

Galileo E6

Galileo E6 signal consists of two parts: E6-B and E6-C which are modulated onto the same carrier frequency using BPSK modulation and each contribute 50% to the total output signal power. E6-B includes commercial navigation message (C/NAV) with a 1000 sps symbol rate and the PRN code with 5.115 Mcps while the E6-C is a pilot signal with the same chipping rate PRN code.

2.3 GNSS Receiver Architecture

GNSS signals are digital signals in nature. However, in order to be transmitted in long distances, i.e. from the GNSS satellite to Earth, they should be modulated on an analog high frequency carrier signal also known as radio frequency (RF) signal. Table 2.2 shows the carrier signal frequencies for different GNSS satellites.

A generic GNSS receiver consists of two main parts: an analog front-end and a digital back-end. Some receivers may be coupled with other sensors, like inertial

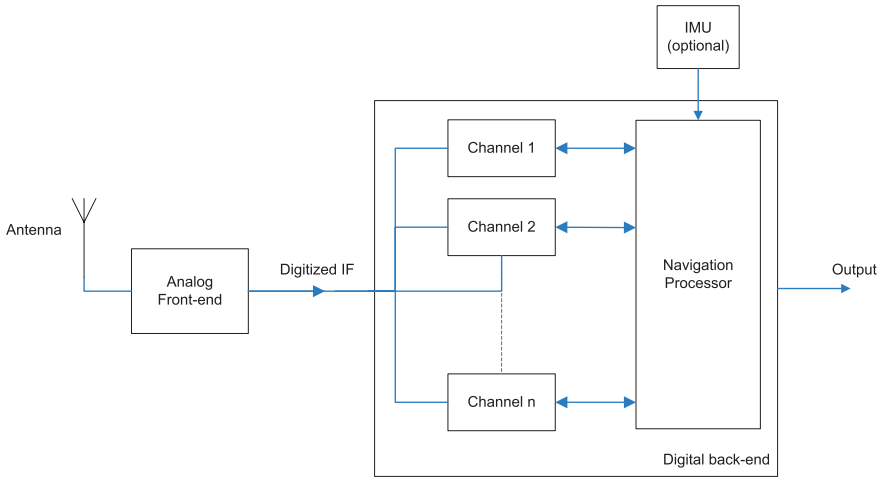


Figure 2.11: A generic GNSS block diagram

measurement unit (IMU) as shown in Fig. 2.11. The received GNSS signal power is lower than the thermal noise floor and usually includes out-of-band interferences. The analog front-end filters the signal from these interferences, amplifies the signal and down-converts it to an intermediate frequency (IF) or baseband. This signal is then digitized and sent to the digital back-end for further processing. In the following, an overview of the digital back-end will be provided and the analog front-end will be discussed in more detail in the upcoming chapters.

2.3.1 Digital Back-end Architecture

In a generic GNSS receiver, the digital back-end receives the digitized IF signal and provides the navigation solution, raw data and auxiliary information. The digital back-end consists of two main parts, channels and navigation processor. Channels find the code and carrier phase of signals from selected satellites and provide them to the navigation processor. Each channel tracks one PRN signal at a time. It

Table 2.2: GNSS Carrier frequencies [MHz] of selected GNSS [61, 64–67, 70, 71]

GPS	**Galileo**	**GLONASS** (future)	**EGNOS**	**WAAS**
L1 = 1575.42	E1 = 1575.42	L1 = 1575.42	L1 = 1575.42	L1 = 1575.42
L2 = 1227.60	E6 = 1278.75	L2 = 1242.00	-	-
L5 = 1176.45	E5a = 1176.45	L3 = 1207.14		
-	E5b = 1207.14	L5 = 1176.45		

was shown previously that at least four satellites should be tracked at each time to generate the navigation solution. This means that the receiver should have at least four channels. Nowadays, a common GPS receiver has at least 12 channels.

The navigation processor calculates the pseudoranges and provides them at the output. Usually, the output also includes carrier phase and Doppler shift of all channels, e.g. in a receiver independent exchange (RINEX) format. This information is used for real-time or off-line calculation of position, velocity and time (PVT). In advanced GNSS receivers, PVT solution is performed in real-time and estimation algorithms such as extended Kalman filter (EKF) are used in the navigation processor for their calculations as well as incorporating information from external aids such as Inertial Measurement Unit (IMU).

Since the concept of digital back-end operation is similar for GPS and Galileo systems, the GPS L1 C/A code is used in the rest of this section to explain the operation of the digital back-end.

Channel Block Diagram

All channels receive the digitized IF signal as their input. The IF signal for GPS L1 of ith satellite can be expressed by

$$IF_i = A_i D_i(t) C_i(t) \cos((\omega_{IF} + \omega_{di})t + \phi_i) \tag{2.21}$$

where IF_i is the IF signal corresponding to the ith satellite, A_i is the amplitude of the signal, $D_i(t)$ and $C_i(t)$ are navigation data and C/A code of the ith satellite respectively, ω_{IF} is the IF frequency, ω_{di} is the Doppler shift relative to the ith satellite and ϕ_i is its carrier phase.

The channel consists of two parts: the code and the carrier tracking loops. The code tracking loop uses delay locked loop (DLL) to track codes and the carrier tracking loop uses a digital mixer, frequency locked loop (FLL) and phase locked loop (PLL) to track the carrier while removing the IF and the Doppler frequencies. Fig. 2.12 shows the block diagram of one channel. In this figure, code loop blocks are connected by solid lines and carrier loop blocks are connected by dashed lines.

The IF signal needs to be down-converted to baseband to be used in PVT calculation. The digital mixer multiplies the IF signal with $\cos((\omega_{IF} + \hat{\omega}_{di})t + \hat{\phi}_i)$ and $\sin((\omega_{IF} + \hat{\omega}_{di})t + \hat{\phi}_i)$ where $\hat{\omega}_{di}$ and $\hat{\phi}_i$ are the estimated carrier Doppler frequency and carrier phase of the GPS signal of the ith satellite. The results are the in-phase (I) and the quadrature-phase (Q) baseband signals which will be used in the code and carrier tracking loops. Estimation of Doppler frequency and phase is a part of carrier tracking loop which will be explained later.

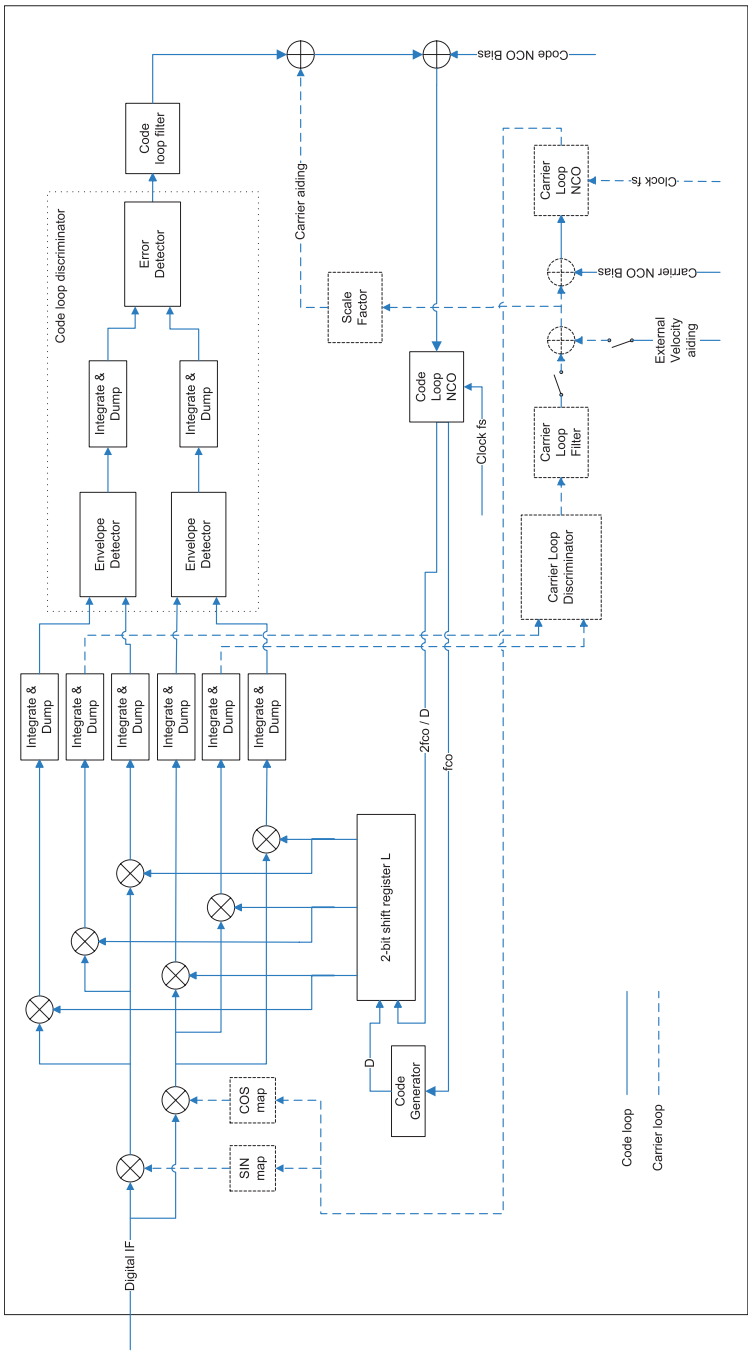


Figure 2.12: GPS block diagram code and carrier tracking loops

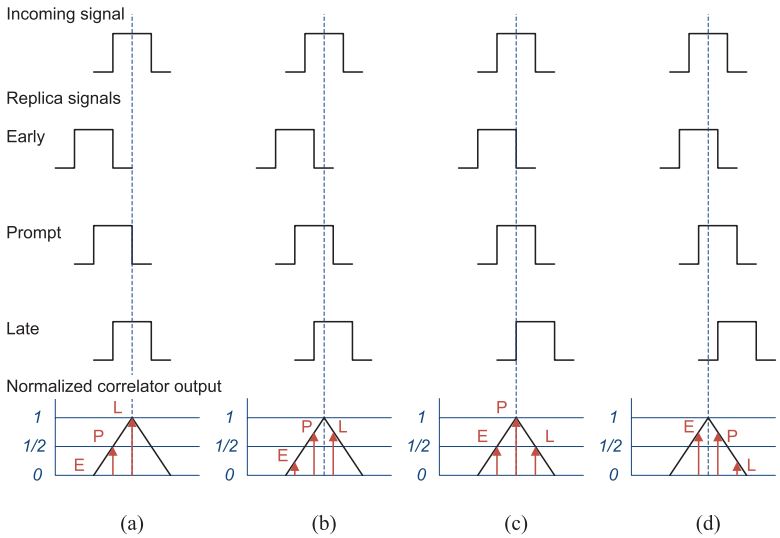


Figure 2.13: Code correlation phases: (a) replica code $\frac{1}{2}$ - chip early, (b) replica code $\frac{1}{4}$ - chip early, (c) replica code aligned, and (d) replica code $\frac{1}{4}$ - chip late

Code Tracking

Correlation is the basis of code tracking. It was mentioned earlier that PRN codes are designed to have a single peak in their autocorrelation while their cross-correlation with other PRN codes is almost zero. In order to track a satellite, each channel tracks one satellite or one PRN. The replica of the PRN is generated locally, synchronous to the satellite and is shifted in time up to the point where the cross-correlation of the received code and the replica produces a peak. Then the DLL tracks the PRN code. The DLL consists of three correlators (early, prompt and late), code loop discriminator, code loop filter and numerically controlled oscillator (NCO).

Three replica codes are generated in the channel: early (E), prompt (P) and late (L). These three codes are generated by a 2-bit shift register as shown in Fig. 2.12. These are the same codes, however, with a predetermined shift in time. This shift is algorithm dependent but typically is $\frac{1}{2}$ chip. In this case the clock frequency of the shift register is double the clock frequency of the replica code generator, f_{co}. Thus the shift register receives the replica code and generates the early, prompt and late codes. The clock signals are generated by NCO and are corrected for the Doppler shift of the code by the DLL.

The aim of tracking loop is to align the received code with the prompt replica. Thus the early, prompt and late codes are correlated with I and Q signals individually. In Fig. 2.12, the combination of a digital mixer and the “Integrate &

Dump" block connected to it build the correlator. The six correlators generate early, prompt and late correlation results for I and Q signals. The outputs of the correlators are sent to the "code loop discriminator" block. The discriminator is the algorithm which finds the deviation of the code alignment with the desired condition. A list of commonly used discriminators can be found in [56].

Depending of the discriminator algorithm, the response time and lock holding margin will be different. Fig. 2.13 shows the code tracking process. For the sake of clarity only one chip is demonstrated. In this process, an "early minus late envelope" code discriminator is used. This algorithm can be expressed by

$$D = \frac{1}{2}\frac{E-L}{E+L} \tag{2.22}$$

with

$$E = \sqrt{I_E^2 + Q_E^2} \quad , \quad L = \sqrt{I_L^2 + Q_L^2} \tag{2.23}$$

where E and L are the early and late correlation envelopes, respectively. This code loop discriminator, D, calculates the difference of the envelopes of the early and late correlation. The result represents the error in the alignment of the prompt code with incoming code. The rest of the loop corrects the delay to minimize this error.

In Fig. 2.13b, the output of the discriminator is $\frac{1}{4} - \frac{3}{4} = -\frac{1}{2}$ which means that the prompt replica should be delayed (negative output). In Fig. 2.13d, the discriminator output is $\frac{3}{4} - \frac{1}{4} = \frac{1}{2}$ which indicates that the prompt replica is delayed too much (positive output). The negative feedback in the DLL keeps this output as close to zero as possible as shown in Fig. 2.13c.

2.3.2 Carrier Tracking Loop

Fig. 2.12 shows also the carrier tracking loop by dashed lines. In this loop, the IF (plus Doppler) is removed from the digitized IF signal and I and Q baseband signals are generated. As mentioned previously, this process is performed by a digital mixer which multiplies the locally generated IF (plus Doppler) signal with the incoming IF signal. The outputs of prompt correlators are sent to the carrier loop discriminator. Depending on the operation mode of the loop, this discriminator can be a PLL, Costas PLL or FLL. The list of these discriminators can be found in [56]. The output of the discriminator is filtered and fed to a carrier NCO to correct the locally generated IF (plus Doppler).

PLL and Costas PLL lock on phase while FLL tracks the frequency changes. Selection of PLL or FLL depends on the accuracy and the required response time during the operation. When the receiver does not know the exact position of data transition boundaries during the initial signal acquisition, maintaining the frequency

lock is easier than the phase lock. The phase tracking loop, however, provides more accurate result than the frequency tracking loop while dynamic stress tolerance of frequency tracking loop is better than phase tracking loop.

Since a GNSS receiver should be able to handle dynamic stress while providing high tracking accuracy, a compromise should be made to balance these two situations. One solution is to intelligently transit between FLL and PLL discriminators. When using an FLL discriminator, short integration time and wide-band carrier loop filter should be used while when using a PLL discriminator, long integration time and narrow-band carrier loop filter are engaged in the process. In order to use pure PLL, the navigation data should be wiped off from the signal. A Costas PLL is insensitive to navigation data. However, the drawback of using it is the 6 dB loss in tracking threshold.

The receiver should know the navigation data in order to perform the data wipe-off process. The complete navigation data can be received either from the signal or from an external source. In case of tracking GPS L1, in the first 12.5 minutes after locking to signal, the complete navigation data can be stored in the receiver's memory. The receiver can use this navigation data until it has been changed significantly by the GNSS satellite.

2.4 Space Capable GNSS Receivers

In general, to design a GNSS receiver, there are a number of general requirements on which the design is based upon. If the receiver is considered for use in space some of the requirements will change and new requirements are introduced taking into account the effect of the space conditions and environment. In this section these requirements are reviewed and the quantitative values are summarized in Table 4.2.

2.4.1 General Requirements

There are a number of standard design parameters in any receiver design procedure which are defined based on the application requirements. These key parameters are noise figure (NF), out of band interferences, linearity and environmental effects such as temperature variations and radiation exposure. In the following, the design parameters which are common in all applications will be introduced and the ones which are changed due to operations in space will be discussed in section 2.4.2.

Receiver Noise Figure

The noise figure, NF, is a measure of added noise by the receiver and is commonly defined by

$$NF = 10\log\left(\frac{SNR_{in}}{SNR_{\text{out}}}\right) \tag{2.24}$$

where SNR_{in} and SNR_{out} are the input and the output signal to noise ratios respectively. In the receiver chain, the noise figure and the gain of the first active block, the low noise amplifier (LNA), have dominant effects on the total receiver noise behavior. Designing a very low noise and high gain LNA is a necessity of the design. However, flicker noise of the following stages should be taken into account during the design, especially, when the bandwidth is extended to very low frequencies (near DC) during the process.

The minimum signal power of the GNSS signal on Earth is around -130 dBm [64, 66]. The thermal noise floor for GNSS signals can be determined by

$$N_0 = kTB \tag{2.25}$$

where k is the Boltzmann constant, T is the absolute temperature and B is the double-sided signal bandwidth. For example, the thermal noise floor is about -110 dBm for the GPS L1 C/A code with a bandwidth of 2.046 MHz at room temperature. This can be determined for all GNSS signals by inserting their bandwidth in (2.25). It can be observed that the signal level is already below the thermal noise floor thus the noise behavior of the receiver is very important.

Linearity

In the receiver chain, there are several filters to reject the out-of-band frequencies. Frequency response of these filters should be sharp enough to attenuate the out-of-band frequencies while passing the desired band with minimum loss. The phase of the signal is an important source of information. Thus, the phase response is another important design parameter in the filter design for the GNSS receiver. It is important that the filters have a linear phase response in the desired frequency bands to achieve a constant group delay. Otherwise the nonlinear effect of phase response will introduce phase error which degrades the navigation solution accuracy.

All active elements show a nonlinear behavior in practice. This behavior should be considered during the receiver front-end design process. However, in order to reduce the complication during the design, the behavior of the nonlinear components are approximated with linear models during the design process and the depth of the approximation is defined by the application.

In a nonlinear system, $y = f(x)$, the input-output relation can be expressed by its Taylor series given by

$$y = \alpha_1(x - X_0) + \alpha_2(x - X_0)^2 + \alpha_3(x - X_0)^3 + ... \tag{2.26}$$

where x and y are the input and output of the system, X_0 is the linearization point and α_n is the Taylor series coefficient of the n$^{\text{th}}$ term defined by

$$\alpha_n = \frac{1}{n!}\frac{d^n y}{dx^n}\bigg|_{x=X_0}. \tag{2.27}$$

When the active components are working at much lower frequencies than their transient frequency, f_T, considering up to the third order term would be sufficient in nonlinear analysis. However, if the operating frequency of the active components gets close to their f_T, then the higher order terms should also be included in the analysis. Considering the GNSS frequencies and the very high f_T of the new IC technologies, nonlinearities up to 3$^{\text{rd}}$ order are taken into account for analysis and design in the following.

If the input is a single tone sinusoidal signal, i.e. $x(t) = A\cos(\omega t)$, then the output can be expressed by

$$\begin{aligned} y(t) &\approx \alpha_1 A\cos(\omega t) + \alpha_2 A^2\cos^2(\omega t) + \alpha_3 A^3\cos^3(\omega t) \\ &= \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right)\cos(\omega t) + \frac{\alpha_2 A^2}{2}\cos(2\omega t) + \frac{\alpha_3 A^3}{4}\cos(3\omega t) \end{aligned} \tag{2.28}$$

where A is the input signal amplitude and ω is its frequency.

In (2.28), a DC term in addition to the fundamental signal and the second and third order harmonics (terms with twice and triple the input frequency) are present. Different effects could be dominant depending on the sign of the Taylor coefficients and the amplitude of the signal. When the signal amplitude increases, the effect of negative Taylor coefficients in the higher order harmonics becomes visible and compresses the signal [72]. In RF circuit design, the design parameter referred to as "1-dB compression point" represents this effect and is defined as the input power where the small signal gain is reduced by 1 dB as shown in Fig. 2.14.

The interferences are mainly outside the signal band and are filtered as much as possible. However, because of imperfections of the filters, the residues can pass through them. These residues may be mixed together (intermodulated) because of the nonlinear behavior of the active parts. The effect of intermodulations becomes serious when the interference signals become larger or their filtering becomes poorer. These intermodulations can fall into the signal band and disturb the signal.

If a two tone signal, $x(t) = A_1\cos(\omega_1 t) + A_2\cos(\omega_2 t)$, is fed to the input in (2.26) then, amongst others, terms with $\omega_1 \pm \omega_2$, $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$ frequencies will

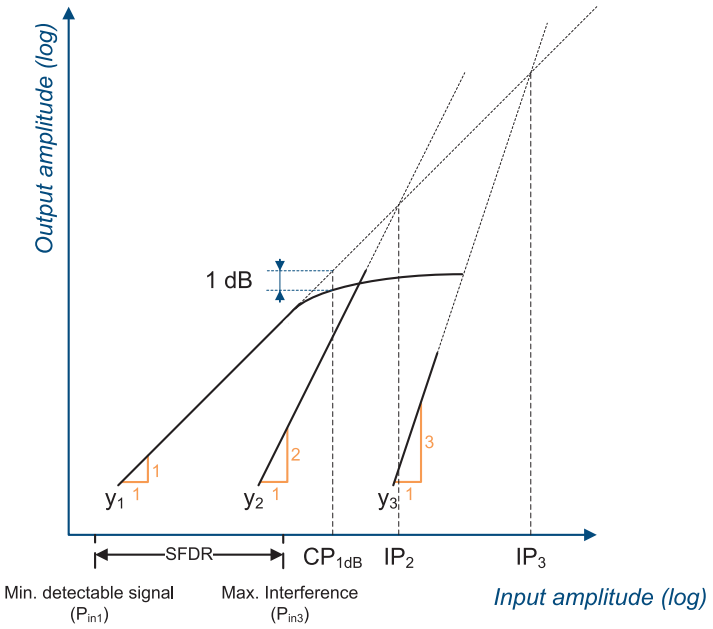


Figure 2.14: 1-dB compression point, Intercept points and spurious free dynamic range

be present in the output. These terms are given in (2.29). The terms with $\omega_1 \pm \omega_2$ frequency in this equation are the second order intermodulation (IM2) and the terms with $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$ frequencies are the third order intermodulation (IM3).

$$\begin{aligned} y(t) = \ldots &+ \alpha_2 A_1 A_2 \cos((\omega_1+\omega_2)t) + \alpha_2 A_1 A_2 \cos((\omega_1-\omega_2)t) \\ &+ \frac{3\alpha_3 A_1^2 A_2}{4}\cos((2\omega_1+\omega_2)t) + \frac{3\alpha_3 A_1^2 A_2}{4}\cos((2\omega_1-\omega_2)t) \\ &+ \frac{3\alpha_3 A_2^2 A_1}{4}\cos((2\omega_2+\omega_1)t) + \frac{3\alpha_3 A_2^2 A_1}{4}\cos((2\omega_2-\omega_1)t) + \ldots . \end{aligned} \tag{2.29}$$

The third order intermodulation appears around the carrier frequency and the second order intermodulation appears near DC. The effect of IM3 shows itself at high frequency sections of the circuit which are working around their input carrier frequency. The effect of IM2 becomes severe in sections of the circuit which change the signal carrier frequency to very low frequency such as mixers in a direct conversion receiver architecture. There are several approaches to reduce the effect of even-order harmonics, thus the IM2, in a direct conversion receiver. As a common approach, fully differential circuits are used which reduce the even-order nonlinearity by the expense of increased power consumption. There are other ap-

proaches which have been proposed such as even-order harmonic reduction loop presented in [73].

The measures of IM2 and IM3 are calculated by means of the 2nd and 3rd order intercept points, or IP2 and IP3 respectively. The nth order input referred intercept point (IIPn) is defined as the input power at which in the nonlinear transfer function, the nth order nonlinear term has the same contribution as the fundamental term to the output. Fig. 2.14 shows the 2nd and 3rd order intercept points, IP2 and IP3.

The fundamental gain is not disturbed until the 2nd and 3rd order nonlinear terms become higher than the noise floor. Spurious free dynamic range (SFDR) is defined as the difference (in dB) between maximum interference power and minimum detectable input signal power as shown in Fig. 2.14 by P_{in3} and P_{in1} respectively. SFDR represents the maximum relative level of interferers that a receiver can tolerate while producing an acceptable signal quality from a small input level [72]. The relation between IIP3, P_{in1}, P_{in3} and SFDR can be derived from Fig. 2.14 as

$$IIP3 = \frac{1}{2}(3P_{in3} - P_{in1}) = \frac{1}{2}(3SFDR + 2P_{in1}). \tag{2.30}$$

Digitization

The last block in the front-end is the analog to digital converter (ADC). The down-converted analog signal is converted to digital for further processing by ADC. The typical input voltage range of an ADC is 200 mV. The resolution of ADC is application dependent and defines the quantization noise which reduces the SNR. It has been shown that for GPS and Galileo signals, more than 4-bit output resolution does not improve the degradation caused by the effect of quantization noise [74, 75]. The sampling rate of the ADC depends on the signal bandwidth and for Nyquist sampling ADCs should meet the Nyquist criteria as given by (3.1).

Component Matching

Depending on the receiver architecture, the received signal may be divided into in-phase (I) and quadrature-phase (Q) components. These two signals are essential to find the carrier phase of GNSS signal. The carrier phase is proportional to the arc-tangent of the ratio of amplitudes of Q and I signals. In the direct conversion receiver, the effect of mismatches in I and Q signal paths will cause an erroneous relation between the amplitude ratios and the carrier phase value. This can be overcome by using matching techniques in the IC layout design to achieve the best matching between components and to achieve best possible carrier phase accuracy.

Navigation Accuracy

One specific requirement for GNSS receivers is the accuracy of navigation solution. The accuracy of navigation solution may be affected by various error sources. For example, the tracking performance of a Phase Lock Loop (PLL) is affected by the influence of thermal noise, dynamic stress error and oscillator phase [76]. In addition to oscillator noise, filtering and quantization error influence the navigation solution [77],

Although the navigation solution is a back-end process, the front-end plays an important role in this process since it prepares the the back-end input. The added noise by the front-end (noise figure) may degrade the result. The effect of component mismatch can show itself as inaccurate quadrature outputs which is important in carrier phase tracking. Filters in the front-end and especially their group delay affects the zero-crossing of the PRN code. The front-end oscillator phase noise is directly added to the received carrier phase and quantization noise degrades the signal. Thus, it is important that the total noise level of the front-end, noise figure and oscillator phase noise, are kept at minimum and filter phase responses be linear. As was mentioned before, the effect of quantization noise is at minimum for resolutions of 4-bits and more in GPS and Galileo receiver front-ends.

2.4.2 Requirements for Operation in Space

The space environment requests for additional design constraints than what already has been addressed. Interferences, high dynamics, high temperature gradients, radiation exposure, vacuum conditions and vibration need to be taken into account in the design. The criteria of these requirements are application dependent and usually add more restrictions to the design. In this section, specific requirements for designing GNSS receivers for low Earth orbit (LEO) satellite application will be investigated.

Operation Modes

It was explained in chapter 1 that there are different applications for GNSS receivers. Some of those applications are performed in space such as navigation, Earth gravity monitoring, ionospheric modeling and so forth.

In each of these applications, the critical determining factor depends on the operation scenario. Accuracy and power consumption are the two main factors that should be considered. Thus, it is important that the receiver is able to adjust its performance for different scenarios. For example, a receiver may provide limited data to save power. As the accuracy requirement of derived parameters would

no longer be satisfied, e.g. the on-board position accuracy, more channels or frequency bands should be activated which results in a better accuracy at the expense of increasing power consumption.

Another example is a scientific mission which requires multi-frequency GNSS measurements. In such mission, the power consumption is relatively high. During the operation, there could be situations where the available power is temporarily insufficient for such measurement, e.g., if the satellite enters eclipse. Thus, the receiver, depending on the defined scenario, could change its operation mode from high accuracy all-channel scientific measurement to low accuracy single channel navigation mode to satisfy the basic requirements of the mission until the available power is back to nominal.

Considering the need of adaptation to different operation modes in order to implement the required flexibility, reconfigurability is an important requirement not only for the GNSS receiver back-end but also for its front-end.

High Velocity

The velocity of the space vehicles relative to GNSS satellites can be much higher than for terrestrial applications. For example, a LEO satellite orbiting the Earth at an altitude of 650 km, has an inertial velocity of about 7200 m/s. Considering this high velocity and the velocity of the GNSS satellites, the relative velocity in some cases would be even higher. The consequence is the higher Doppler shift of the incoming signal compared to terrestrial application. The frequency change would be more than 37.8 kHz for the above mentioned LEO satellite at L1 frequency. Thus, the receiver must account for this Doppler shift in its frequency search.

The high velocity of the space vehicle also means much shorter visibility of the GNSS satellites than available for terrestrial applications which requires for higher number of channels for parallel satellite search.

Interferences

The signal interferences are different for LEO satellites compared to terrestrial applications. The sources of interference can be divided into three categories; space to Earth signals, Earth to space signals and terrestrial signals. The International Telecommunication Union radio regulations (ITU-RR) [78] define the maximum allowable transmitted power in different frequency bands which can be used in order to determine the requirements.

Looking at the GNSS band, i.e. 1 - 10 GHz, based on article 21 of ITU-RR, the maximum power flux-density of a signal transmitted from space, at the surface

of Earth (space to Earth signal) is -116 dBW/m^2, which is much smaller than the maximum Earth station interferences as will be shown later. For transmissions from Earth in a frequency range of 1-10 GHz, this maximum power is +35 dBW. This comprises the GNSS band which is 1-2 GHz. Article 21.3 of the ITU-RR states: *The maximum equivalent isotropically radiated power (e.i.r.p.) of a station in the fixed or mobile service shall not exceed +55 dBW.* Also the article 21.8 of the ITU-RR determines the transmission angle for terrestrial transmitters must be maximum +5° with respect to horizon [78].

Based on the maximum transmission angle, the line of sight (LOS) between a terrestrial transmitter and the LEO satellite is about 2800 km for a satellite at the altitude of 600 km. Free space loss, L_s, is defined by

$$L_s = -10\log\left(\frac{\lambda}{4\pi l}\right)^2 \tag{2.31}$$

where λ is the wavelength of the signal and l is the LOS distance. Free space loss at 1 GHz for the above mentioned LOS would be 161.4 dB. The received power at the LEO satellite, P_r, can be calculated from

$$P_r = P_t + L_a + L_s \tag{2.32}$$

where P_t is the transmitted power and L_a is the auxiliary loss which is considered to be 3 dB. In the worst case, where the transmitter is using its maximum capacity, i.e. P_t = +55 dBW, the maximum received power will be -76.4 dBm. This means that the receiver should be able to handle this input power without causing any saturation and nonlinearity. However, temporary interferences can happen due to high power Earth to satellite communications. In the worst case, when the LOS is 600 km, the interference power is increased by almost 13 dB. This means that transient interferences with maximum power of -66 dBm should not damage the receiver.

Considering the received signal and interference power levels, SFDR of the front-end should be more than 64 dB. This will result in a third order input referred intercept point (IIP3) of -37 dBm for LNA based on (2.30).

Temperature Variation

The operating temperature of an IC affects its behavior. Thus, the changes in the parameters due to the temperature variation shall be considered during the design. Parameters, such as the threshold voltage of the complementary metal oxide semiconductor (CMOS) transistors, the characteristics of the diodes, the values of the resistors and capacitors, are examples of the temperature-dependent design parameters.

Measurements from previous missions show that the temperature variation on the surface of a LEO satellite can range from -170°C to +160°C measured in GOCE mission [79] while the temperature inside the satellite can range from -10°C to +25°C measured in Delfi-C3 [80]. Thus, the variations inside the satellite are similar to terrestrial applications except for their high gradient. The average temperature change period for a LEO satellite orbiting at 600 km is about 96.69 minutes [50].

Radiation

The electronic devices are exposed to higher amount of radiation in the space environment than on Earth since most of the radiation is absorbed by the atmosphere. Different types of radiation are present in space; namely protons, electrons, neutrons, heavy ions, high energy charged particles (proton, Helium nuclei and ionized nuclei), X-ray and gamma ray [81]. Table 2.3 provides an overview of various radiation sources in space with their radiation type.

Different radiation particles interact with the electronic circuits in a different manner. Photons, depending on their energy, can have the following effects: photoelectric effect, Compton scattering and pair production. Neutrons can be absorbed in the material or cause elastic or inelastic scattering. Charged particles can cause ionization or electromagnetic radiation.

The radiation effects can be categorized as cumulative effects and single event effects (SEE). In cumulative effects, the electronic circuits are damaged either by the total ionizing doze (TID) or displacement. When the electronic devices are exposed to protons and electrons for a long period of time, the insulating layers may trap charges which can lead to shift in their parameters such as gate voltage threshold in metal-oxide semiconductor (MOS) transistors. Also, TID may produce inter-

Table 2.3: Radiation types and their sources [81]

	Protons	Electrons	Neutrons	Heavy ions	High energy charged particles	X-ray	Gamma-ray
Solar flare	+			+		+	+
Solar wind	+	+		+			
Galactic cosmic rays	+				+		
Cosmic ray shower			+				

face changes that can significantly increase the leakage current of the device [82]. In the long run, TID can cause permanent functional damage to the device. Displacement damage happens when the device is exposed to non-ionized particles. This causes displacement of atoms. The overall effect is a change in minority carrier lifetime and increased light absorption. The single event effects can be produced by direct ionization or by secondary particles. The result is disturbance in the functionality of the device and could be temporary or permanent. The temporary effects can be recovered, e.g. by software reset or temporary shutting down the device. The temporary effects are single-event transient (SET), single-event upset (SEU), single-event functional interrupt (SEFI). The permanent damages are single-event latch-up (SEL) and single-event gate rupture (SEGR).

There have been a number of experiments to evaluate COTS technology for operations in space. The TID test results presented in [83] on four COTS GPS receivers: DLR Orion, DLR Phoenix, NovAtel OEM4-G2L and Spetentrio PolaRx2, show that these receivers are suitable for operation in LEO satellites. Phoenix GPS receiver is on-board several spacecraft such as PROBA-2, PRISMA, Flying Laptop, TET-1, XSat and RSSP microsatellites [84].

However, radiation is less damaging in standard CMOS technologies with gate lengths of less than 180 nm [85]. Additionally, radiation damages can be reduced by using lower operating voltages as well as employing special layout design techniques referred to as radiation hardening by design (RHBD) [81, 86].

Antenna

An antenna receives the GNSS signals and feeds the front-end. For the purpose of continuous operation, the GNSS satellites shall be in the field of view of the antenna. This adds extra requirements on the number of antennas in use, their arrangement and the attitude control of the spacecraft. For example PRISMA satellites use two GPS antennas on each spacecraft to handle non-zenith pointing attitudes [36].

On the other hand the received noise power by the antenna, may vary depending on the noise sources in its view as well as its operating temperature. This affects the sensitivity of the complete receiver. However, the main front-end design parameter affected by this is the total gain. The front-end shall be able to adjust its gain to avoid saturation at the output.

Vacuum

As long as the electronic devices are working in an environment with a temperature variation within the operating range of the IC, the effect of vacuum shows

itself on the IC packaging rather than the input-output characteristic. Since the standard ICs are packaged at 1 atm pressure, outgassing occurs as the package is exposed to vacuum [87, 88]. Depending on the packaging material, outgassing occurs at different rates. This effect can damage the packaging structure. Thus, the packaging material shall be selected such that in a defined mission period, the integrity of the packaging is not lost.

Vibration

During the launch of the space vehicle, vibration and acoustic pressure become important. Thus, the space vehicle and its components must be designed in compliance with the launch vibration and acoustic specifications. There are several tests to assure the survival of the components during the launch. These tests are acoustics test, random and sinusoidal vibration test and shock test. The maximum frequency for acoustic test is 10 kHz and for random vibration is 2 kHz [48, 49]. Thus, the minimum wavelength of the incident waves would be about 34 mm considering the traveling speed of acoustic waves in air. Since the traveling speed of acoustic waves in other materials is larger, the resulting wavelength will also be larger. Considering this wavelength the IC packaging, its connections to the PCB and the PCB itself should be designed to be able to withstand such operating conditions.

2.5 Summary

In this chapter, following a brief explanation of the fundamentals of satellite positioning system, different GNSS signals and their structures have been introduced. Then, a generic GNSS receiver architecture and its building blocks have been introduced. As this thesis particularly considers the development of GNSS receiver front-end for space applications, the requirements of a space capable GNSS receiver have been presented. In the following chapter, different architectures of the GNSS receiver front-end will be explained and the proposed front-end architecture will be developed and presented.

3

GNSS Receiver Front-end Architectures

Since the discovery of the electromagnetic waves and the invention of the first radio in the 19^{th} century [89], different receiver architectures have been introduced. The continuous developments in the radio technology and the changes in their properties made some of the architectures more popular in different periods of time. The introduction of vacuum tubes and subsequently, the transistors and integrated circuit (IC) changed the preferred radio architecture [90]. The fast improvements of the semiconductor technology and the introduction of high-speed digital systems provided the opportunities for new radio architectures.

The radio systems moved from fully analog to mixed signal systems which are also referred to as software defined radio (SDR) [91]. In most SDR receiver architectures, the received signal is filtered and down-converted to either an intermediate frequency (IF) or baseband and the remainder of the process is performed in the digital domain. Thus, an SDR receiver consists of two main parts, the (analog) front-end and the (digital) back-end. The GNSS receiver is one of the well known and widely used examples of SDR receivers.

The analog front-end is the critical part of the SDR receiver. It determines the sensitivity and the selectivity of the receiver. Thus, it is crucial to design a high performance front-end. In this chapter, an overview of different front-end architectures will be presented followed by the comparison of their properties. Then, the proposed novel radio receiver front-end architecture will be developed and its unique characteristics will be discussed.

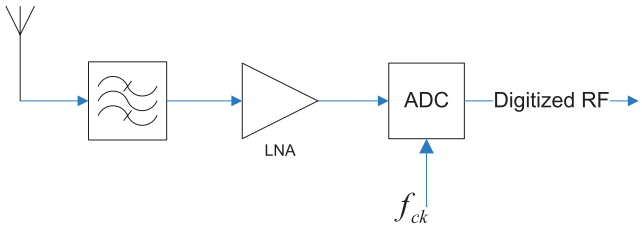


Figure 3.1: Direct sampling architecture

3.1 Existing Radio Receiver Front-end Architectures

Different radio receiver architectures have been developed in the past. Each architecture has its own advantages and disadvantages which makes it suitable for different applications. An overview of these architectures is provided in this section.

3.1.1 Direct Sampling

The developments in IC technologies allow to design very high speed analog to digital converters (ADC). Since SDR digitally receiver performs the final processing, it is possible to use such high speed ADCs to sample the radio frequency (RF) signals directly. This method reduces the complexity of the front-end and limits it to a filter, a low noise amplifier (LNA) and an ADC. This architecture is shown in Fig. 3.1.

The Nyquist criteria dictates that in order to avoid aliasing and to be able to reconstruct a sampled signal, the sampling frequency, f_s, shall be higher than twice the upper frequency limit in the signal band, f_u, [92]:

$$f_s \geq 2f_u. \tag{3.1}$$

In (3.1), the equality holds only when there is no frequency component at f_u. The direct sampling receiver which follows the Nyquist criteria is called RF (Nyquist) sampling receiver. In GNSS receivers L1 band has the highest carrier frequency. Thus, considering this architecture for the GPS L1 C/A signal, the minimum clock frequency should be higher than 3.1744 GHz. Working at such high frequency requires a very high speed ADC as well as a very powerful processor. Ideally in an SDR, it it desirable that the process be performed at baseband. The baseband signal usually has a much lower bandwidth compared to the carrier frequency. Thus, sampling at such high frequency only increases the burden on the processor and its power consumption.

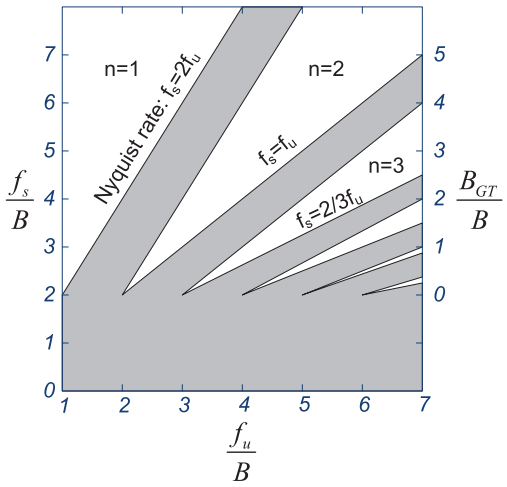


Figure 3.2: The allowed and disallowed (shaded area) uniform sampling rates versus the band position

A solution has been proposed in order to reduce the sampling frequency [93,94]. In this approach which is called sub-sampling or bandpass sampling, the sampling frequency is determined by (3.2) and an anti-aliasing filtering needs to be applied to the sampled signal to reshape it. In order to have acceptable uniform sampling rates, the following condition shall be satisfied [93]:

$$\frac{2f_u}{n} \leq f_s \leq \frac{2f_L}{n-1} \tag{3.2}$$

where f_L is the lower frequency limit and n is an integer given by

$$1 \leq n \leq \left\lfloor \frac{f_u}{B} \right\rfloor \tag{3.3}$$

where B is the signal bandwidth. The equations (3.2) and (3.3) are depicted graphically in Fig. 3.2. In order to be able to reconstruct the signal with an anti-aliasing filter, the sampling frequencies shall be selected from inside the wedges. The Nyquist criteria is a special case of (3.2) where $n = 1$ and the anti-aliasing filter will be a low-pass filter. However, in the bandpass sampling, the signal to noise ratio is not preserved due to the out of band noise aliasing [95].

Compared to other types of receivers which will be described later, RF (Nyquist) sampling and bandpass sampling receivers show higher susceptibility to clock aperture jitter, distortion, noise figure and linearity degradation and increase in power consumption [95].

In the RF sampling receiver, jitter reduces the signal to noise ratio (SNR) which in turn decreases the effective number of bits (ENOB) of the ADC [95]. In the band-

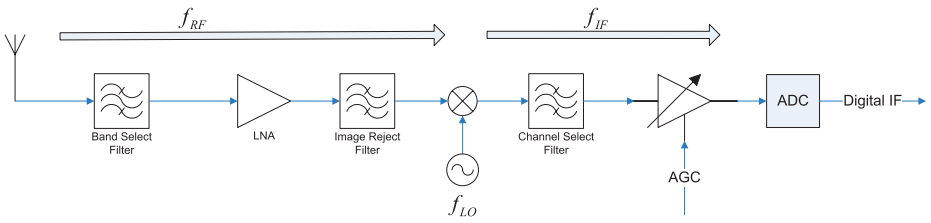


Figure 3.3: Heterodyne architecture

pass sampling receiver, the aperture jitter generates extra frequency components in the desired band which can cause an additional degradation in its performance. However, these frequencies can be mitigated by using a proper anti-aliasing filtering [93, 94].

In a bandpass sampling receiver, the noise is folded to the Nyquist band from the multiples of the sampling frequency. The potential of the noise aliasing is increased as the ratio of the sampling frequency, f_s, to the upper frequency limit, f_u, is decreased, thus the requirements of the anti-aliasing filter become stricter. However, using a bandpass filter prior to the bandpass sampling improves the noise performance by reducing the out-of-band noises. Aliasing increases the number of tones in the spectrum of the Nyquist band. In the bandpass sampling, the number of aliased tones is increased. Thus, bandpass sampling receivers show poorer linearity performance compared to RF sampling receivers [95].

Although the direct sampling architecture reduces the complexity of the front-end, the amplification should be realized in the RF band, i.e. by the LNA. It is generally difficult to combine high gain with good linearity at high frequencies. This is caused by limitations in IC fabrication technologies such as parasitics as well as lower intrinsic gain of the transistors at high frequencies.

The direct sampling receivers show a better reconfigurability than IF or baseband sampling receivers since they use a programmable digital signal processor for most of their operation. However, if an ASIC is designed for the processing then this flexibility would be limited.

3.1.2 Heterodyne

Directly sampling the RF signal has, as described above, a number of drawbacks which render this an inefficient solution. Reducing the required gain of the LNA improves the linearity behavior. Reducing the carrier frequency relaxes the ADC design and the required processing power. The heterodyne architecture provides a solution by lowering the carrier frequency and distributing the gain throughout the circuit.

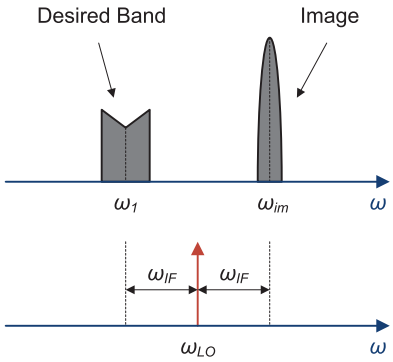


Figure 3.4: Image frequency

In the heterodyne architecture, as depicted in Fig. 3.3, first the out-of-band interference signals are filtered by the band-select filter which is placed after the antenna. Then, the carrier frequency is reduced to an intermediate frequency (IF). Thus, the requirements for the ADC and the back-end processor are relaxed compared to the direct sampling architecture. Since the gain can be distributed in the receiver, the requirements on the LNA are also relaxed which provides a better linearity with lower power consumption. In the architecture depicted in Fig. 3.3, the down-conversion to the IF is performed in a single step. As will be discussed later, there are other configurations of heterodyne architecture which use multiple steps of down-conversion.

In the heterodyne architecture the process of down-conversion is performed by mixing (multiplying) the received RF signal, $A_{RF}\cos(2\pi f_{RF}t)$, with a sine wave generated locally by a local oscillator (LO), $\cos(2\pi f_{LO}t)$, or a square wave with the same fundamental frequency (f_{LO}). This process will produce two signals; one at $f_{RF}+f_{LO}$ frequency and the other one at $f_{RF}-f_{LO}$

$$\begin{aligned} &A_{RF}\cos(2\pi f_{RF}t+\phi_{RF})\times\cos(2\pi f_{LO}t)= \\ &\tfrac{A_{RF}}{2}\left[\cos(2\pi(f_{RF}-f_{LO})t+\phi_{RF})+\cos(2\pi(f_{RF}+f_{LO})t+\phi_{RF})\right] \end{aligned} \tag{3.4}$$

where f_{LO} is the local oscillator frequency and A_{RF}, f_{RF} and ϕ_{RF} are the amplitude, frequency and phase of the RF signal, respectively. The high frequency of the result is filtered and the remaining low frequency is the IF signal

$$IF=\frac{A_{RF}}{2}\cos(2\pi f_{IF}t+\phi_{RF}) \tag{3.5}$$

$$f_{IF}=|f_{RF}-f_{LO}|. \tag{3.6}$$

In (3.5), IF is the IF signal and f_{IF} is the IF frequency defined by (3.6). From (3.6), it can be concluded that f_{IF} can be generated by two frequencies. One frequency is

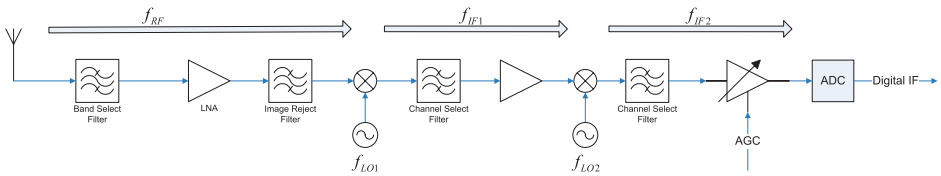


Figure 3.5: Dual-IF Heterodyne architecture

f_{RF} and the other one is the image of f_{RF} with respect to f_{LO}. This image frequency (f_{IM}) is placed at $f_{LO} - f_{IF}$ if $f_{LO} < f_{RF}$ and at $f_{LO} + f_{IF}$ if $f_{LO} > f_{RF}$. Fig. 3.4 depicts the image frequency when $f_{LO} > f_{RF}$.

The band-select filter may not have a very high selectivity, which is indicated by the quality factor or Q-factor. Thus, the out-of-band interference residuals, including the image signal, could remain in the received signal. The most straightforward approach to suppress the image signal is using an image reject filter before the down-conversion mixer as depicted in Fig. 3.3. The image rejection in this method depends on the quality of the filter and usually the image signal is not completely removed.

In the single step down-conversion heterodyne architecture, the trade-off between sensitivity (image rejection) and selectivity (channel selection) often proves to be severe. If the IF frequency is high then the image can be suppressed but the complete channel selection is difficult and vice versa. Using multiple down-conversions with distributed filtering and amplification can be a solution for such a problem [72]. However, in the dual-IF as well as multiple-IF architectures, there are image frequencies at each stage of down-conversion. A dual-IF heterodyne architecture is depicted in Fig. 3.5.

There are several approaches to overcome the problem of image signals such as Hartley [96] and Weaver architectures [97]. The Hilbert transform states that if the spectrum of a narrow-band signal is multiplied by $G(\omega) = -j\text{sgn}(\omega)$, where $\text{sgn}(\omega)$ is the sign function, then the signal phase is shifted by 90° [98]. Both Hartley and Weaver architectures use this property and combine quadrature signals with phase shifting to remove the image signal. These architectures are shown in Fig. 3.6.

Details of operation of Hartley and Weaver architectures can be found in [72, 96, 97]. Since these architectures use I and Q signals, they are susceptible to I-Q mismatches. Any mismatch in the I and Q paths will result in the decreasing of the image rejection ratio (IRR). It is worth mentioning that in both architectures carrier phase and Doppler shift are preserved in the IF signal. However, if the Hartley architecture is implemented by the RC-CR phase shifter then there will be a 45° phase shift at IF.

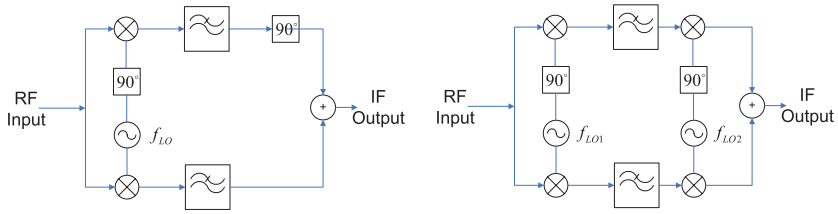


Figure 3.6: Hartley architecture (left) Weaver architecture (right)

3.1.3 Direct Conversion (Zero-IF or Homodyne)

If the local oscillator generates the same frequency as the RF input signal in a heterodyne architecture then the two generated output frequencies will be at baseband and at twice the RF frequency as given by

$$A_{RF}\cos(2\pi f_{RF}t+\phi_{RF})\times\cos(2\pi f_{RF}t)= \\ \frac{A_{RF}}{2}\left[\cos(\phi_{RF})+\cos(2\pi(2f_{RF})t+\phi_{RF})\right]. \tag{3.7}$$

In this case, this architecture is called “direct conversion”, “Zero-IF”or homodyne. By incorporating a low-pass filter at the output of the zero-IF architecture, it will only contain the baseband signal. Zero-IF is the simplest architecture for analog down-conversion. The number of blocks is less than heterodyne and since most of them are working at baseband, this architecture is more amenable to monolithic integration. The frequencies of the local oscillator and the RF carrier are equal in this architecture thus, it does not suffer from the image frequency problem.

In practice, the carrier signal of each satellite would experience a time-varying Doppler shift, f_{Di}. In the zero-IF architecture, the Doppler frequency of each carrier is transferred directly to the output. Thus, the carrier Doppler frequency should be removed in the back-end as well as the Doppler frequency of each PRN code and navigation data. The effect of the Doppler frequency, PRN codes and

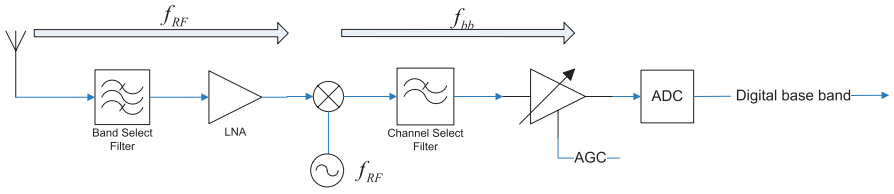


Figure 3.7: Direct conversion architecture

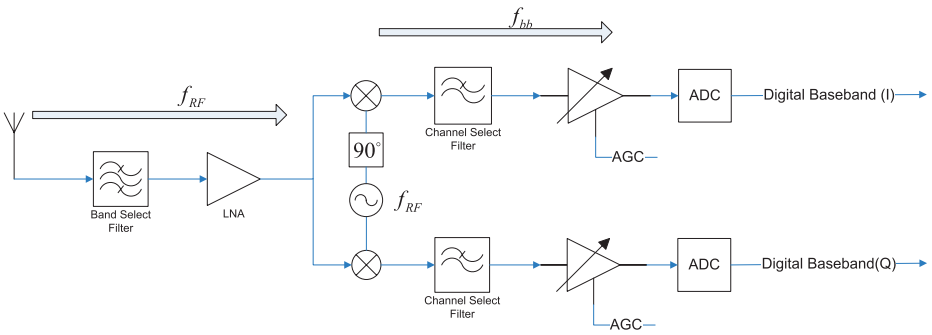


Figure 3.8: Quadrature direct conversion architecture

navigation data is within A_{RF}. The output of the front-end including Doppler can be described by

$$\frac{A_{RF}}{2}\left[\cos(2\pi f_{Di}\,t+\phi_{RF})+\cos(2\pi(2f_{RF}+f_{Di})\,t+\phi_{RF})\right]. \tag{3.8}$$

Fig. 3.7 shows the zero-IF architecture. The basic configuration is suitable for modulations where the information modulates the amplitude of the carrier, for example a double-sideband amplitude modulated (DSB-AM) signal. If the phase or frequency of the carrier contains any information then a quadrature configuration is necessary. Fig. 3.8 depicts the quadrature zero-IF architecture.

The GNSS signal is a good example for the case in which the carrier phase contains information as explained in chapter 2. Including GPS L1 carrier phase in (2.12), it can be written as:

$$CA_{L1i}=\sqrt{2}AD_i(t)C_i(t)\cos(2\pi f_1\,t+\phi_{1i}) \tag{3.9}$$

where CA_{L1i} is the L1 C/A code, A is the amplitude of signal, $D_i(t)$ is the navigation data, $C_i(t)$ is the C/A code, f_1 is the L1 carrier frequency and ϕ_{1i} is the L1 carrier phase of the i$^{\text{th}}$ satellite. It can be concluded from (3.7) that the carrier phase affects the amplitude of the baseband output of the zero-IF architecture and needs an accurate amplitude reference for detection. However, using a quadrature zero-IF architecture eliminates the need of an accurate amplitude reference as shown by (3.10) and (3.11).

$$\begin{cases} A_{L1i}\cos(\omega_1 t+\phi_1)\times\cos(\omega_1 t) \\ A_{L1i}\cos(\omega_1 t+\phi_1)\times\sin(\omega_1 t) \end{cases} \overset{LPF}{\Longrightarrow} \begin{cases} \frac{A_{L1i}}{2}\cos(\phi_1) = I_i \\ -\frac{A_{L1i}}{2}\sin(\phi_1) = Q_i \end{cases} \tag{3.10}$$

In (3.10), $A_{L1i}=\sqrt{2}AD_i(t)C_i(t)$ and LPF stands for low-pass filter. The transfer function of a low-pass filter, $H(\omega)$, is such that it is transparent for the frequencies

lower than its corner frequency, ω_c, and the signals with higher frequencies than the corner frequency are blocked.

Based on the result of (3.10), the carrier phase of the GPS L1 signal can be calculated from

$$\phi_i = \arctan(\frac{-Q_i}{I_i}). \tag{3.11}$$

In CDMA systems such as GPS and Galileo where multiple satellites are transmitting at the same frequency, (3.11) is calculated after correlation [56]. Thus, the carrier phase of each channel is determined by

$$\phi_i = \arctan(\frac{-Q_{Pi}}{I_{Pi}}) \tag{3.12}$$

where I_{Pi} and Q_{Pi} are the outputs of the I and Q prompt correlators as explained in section 2.3.2.

The zero-IF architecture is favorable due to its potential for small size, low-power and low-cost front-end design. However, there are a number of drawbacks which should be addressed. Main challenges in designing a zero-IF front-end are the DC offset, even order distortion, local oscillator (LO) leakage, I and Q mismatches and the flicker noise [72].

Some of the mentioned challenges show themselves if the mixer in the zero-IF architecture shows a poor port to port isolation; those are the DC offset, even order distortion and the LO leakage.

If the isolation between LO port and RF port is poor, the LO signal which usually is a strong sine or square wave will leak to the RF port and returns to the mixer as RF signal. Since the leaked signal is in phase with the LO signal, from (3.7) it can be concluded that there will be a considerable DC component at the output of the mixer. The same holds when there is a large interferer that leaks from RF port to LO port. This phenomena is called “self mixing”. Fig. 3.9 shows these two situations. If the reverse transmission coefficient of the LNA is low then the LO signal can leak to the antenna and cause interference for close-by systems which are working at the same frequency range.

In section 2.4, different types of nonlinearities were discussed. The effect of the even order nonlinearity of the LNA shows itself at the output of the mixer when the isolation between its RF port and output port is poor. In Fig. 3.10, the effect of the 2^{nd} order intermodulation, IM2, is shown. In this case, there is a term with a frequency of $|\omega_1 - \omega_2|$ at the output of the LNA as given by (2.29). In an ideal case this low frequency will be translated to very high frequency by the mixer and will be filtered afterwards. However, in case of poor RF to output isolation, this very low frequency appears directly at the output of the mixer, hence within the information band.

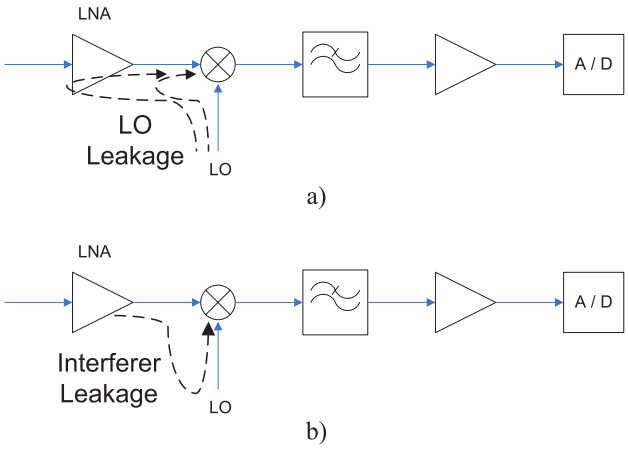


Figure 3.9: Self-mixing of a) LO signal b) a strong interferer

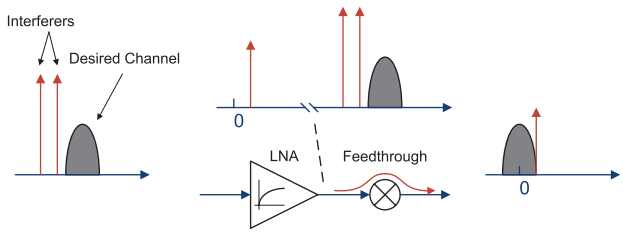


Figure 3.10: Effect of even order distortion

In the quadrature zero-IF, the I-Q mismatch provides another source of error. It can show itself in gain mismatch, phase mismatch or a combination of both. The scale factor of the I and Q paths will be different if the gain mismatch happens, hence shows an error in the I and Q signal ratio. The oscillator phase mismatch shows itself as disturbances in I and Q signals since fractions of data pulses from each path are transferred to the other. This degrades the SNR as depicted in Fig. 3.11.

Flicker noise or $1/f$ noise is a very low frequency noise which starts from almost DC and extends to the point where thermal noise becomes dominant. The flicker noise can be approximated by the function $1/f$. When the signal band extends to near zero frequency, SNR will be affected by the flicker noise. CMOS transistors generate higher flicker noise than other IC technologies such as bipolar junction transistors (BJT) and Si-Ge transistors [99–101]. Employing high-pass filter after the mixer [102, 103], applying chopping technique [104], incorporating very large devices in the amplifier stages after mixer and proper change in the mixer design are a number of solutions to the flicker noise problem. In the next chapter

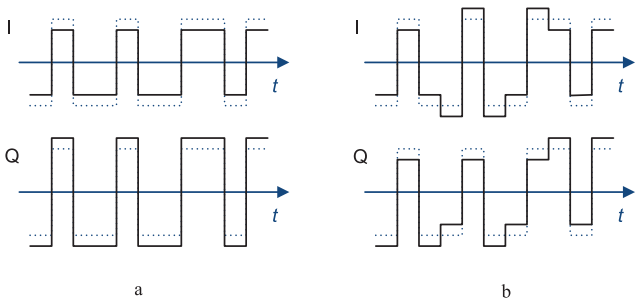


Figure 3.11: Effect of I-Q mismatch on the quadrature zero-IF output a) gain mismatch b) phase mismatch

a novel mixer design is introduced which provides a solution to the DC offset and the flicker noise problems.

3.1.4 Front-end Architecture Comparison

In the previous sections, three different RF receiver front-end architectures have been introduced. These architectures are direct sampling, heterodyne and zero-IF. In this section, their properties are compared and summarized in Table 3.1.

Table 3.1: Comparison of different front-end architectures

	Direct sampling	**Heterodyne**	**Zero-IF**
Circuit complexity	low	high	low
Amplification band	RF	IF	BB
Aliasing	yes[1]	no	no
Image problem	no	yes	no
Filter	complex	complex	simple
Flicker noise	no	no	yes
DC offset	no	no	yes
2^{nd} order nonlinearity	no	no	yes
3^{rd} order nonlinearity	yes[2]	yes	yes
I-Q mismatch	no	yes	yes
Processing power	high	moderate	low
Power consumption	high	moderate	low
Reconfigurability	full	limited	limited
Chip area	small	large	small

[1] especially in sub-sampling
[2] in LNA

The received signals must be amplified. As GPS and Galileo signals are weak signals they need to be amplified by about 120 dB. In each architecture, this amplification occurs at different part of the circuit thus, at different frequency. In the direct sampling architecture, the LNA provides the whole gain while in heterodyne and zero-IF architectures, the amplification is distributed in the front-end. The zero-IF has the advantage that the amplification happens largely at baseband which makes it more favorable.

Direct sampling uses either Nyquist sampling or bandpass sampling. For Nyquist sampling, the sampling frequency is extremely high which results in a very high power consumption and processing power. In the latter case, the sampling frequency is much lower however, aliasing becomes a dominant problem. On the other hand, the image frequency is one of the main challenges in the heterodyne architecture. Because of aliasing and the image frequency problem in the direct sampling architecture and heterodyne architectures respectively, they require complex filters which increases the complexity of their circuits.

The effect of flicker noise becomes serious when the operating frequency of the CMOS transistors reaches near DC value. This happens in zero-IF architecture where the signal is directly down-converted to DC. Another effect which appears in the zero-IF architecture is the DC offset generated as the result of signal leakage. In the next chapter, a novel approach will be introduced to solve the flicker noise and DC offset problems of zero-IF receivers.

All circuits show non-ideal behaviors. It is important that the architecture is designed such that it reduces the effect of these non-ideal behaviors. One form of these behaviors is nonlinearity as discussed in 2.4.1. The 2^{nd} and 3^{rd} order nonlinearity are the dominant effects. The 3^{rd} order nonlinearity is present in all architectures while, as was explained in section 3.1.3, the 2^{nd} order nonlinearity shows itself mainly in zero-IF.

It is advantageous to use a quadrature architecture. However, the matching of the paths is important to realize the benefit of such design. Moreover, matching becomes important when using differential amplifier and mixers in the design. Thus, heterodyne and zero-IF architectures could suffer from I-Q mismatch.

Considering that the direct sampling architecture relies on a processor to perform most of the receiver tasks such as filtering and down-conversion, the processing power is very high in this architecture. The heterodyne architecture provides the digitized output at IF frequency thus, requires lower data rate and less processing power. The processing power is the least for zero-IF architecture which provides the digitized output at baseband. The total power consumption is determined by both the front-end and the back-end. The zero-IF architecture has the potential to have the lowest power consumption due to its simple front-end architecture and lower back-end operating frequency and the direct sampling can

Table 3.2: Pugh matrix for selecting the front-end architecture (+1: favorable, 0: acceptable, -1: unfavorable)

	Weight	**Direct sampling**	**Heterodyne**	**Zero-IF**
Circuit complexity	1	+1	-1	+1
Amplification band	1	-1	0	+1
Aliasing	1	-1	+1	+1
Image problem	1	+1	-1	+1
Filter	1	-1	-1	+1
Flicker noise	1	+1	+1	-1
DC offset	1	+1	+1	-1
2^{nd} order nonlinearity	1	+1	+1	-1
3^{rd} order nonlinearity	1	-1	-1	-1
I-Q mismatch	1	+1	-1	-1
Processing power	3	-1	0	+1
Power consumption	3	-1	0	+1
Reconfigurability	3	+1	0	0
Chip area	2	+1	-1	+1
Σ		**+1**	**-3**	**+8**

have the highest power consumption due to its very high back-end operating frequency [95].

The direct sampling architecture uses software to operate and, if designed to be re-programmable, can be fully reconfigured. The other two architectures can be designed to have limited reconfigurability only. An example of such reconfigurable zero-IF architecture is proposed in Fig. 3.12.

It can be concluded that the heterodyne architecture has the most complex circuit among these architectures. It requires multiple down-conversion steps, complex filtering and a moderate speed ADC which in total has more building blocks than the others. The direct sampling consists of mainly an LNA, complex filter, high speed ADC and high power processor. The zero-IF contains one down-conversion block, simple filters and low speed ADC.

The chip area of the direct sampling front-end is small since it consists of LNA and filter. The zero-IF architecture has more building blocks. However, compared to heterodyne architecture, occupies considerably less area.

In many GNSS applications, e.g. in nano-satellites, a flexible, low-power and low-cost solution is required as explained in section 1.3 and section 2.4.2. In order to determine which architecture is best suited for these applications, a Pugh matrix is generated. In this matrix, each property has a weight in the range of 1 to 3 where 1 represents an ordinary property and 3 represents an important prop-

erty. For each architecture, the properties are represented by "+1", "0" and "-1". The properties which are favorable are given "+1" and the ones which are unfavorable are given "-1". The properties which are acceptable are replaced by "0". It can be concluded from Table 3.2 that zero-IF architecture is the most suitable architecture for our purpose. As explained previously, the main obstacles are the DC-offset and the flicker noise. Tackling these problems is an interesting research topic which is the focus of this work. In the next chapters, a new and innovative solution is provided in full analytical details along with verification based on extensive simulation.

3.2 Proposed Front-end Architecture

It was concluded in the previous section that the zero-IF architecture is the most suitable architecture for the GNSS receiver front-end. Based on this conclusion and the properties of the GNSS signals, a reconfigurable GPS/Galileo receiver front-end is proposed. It was explained in section 2.2 that the GPS and Galileo signals have similar properties that make them suitable for sharing the front-end. The two main properties are using CDMA modulation and sharing the carrier frequency. GPS L1 and Galileo E1 are transmitted at 1575.42 MHz carrier frequency and GPS L5 and Galileo E5a have the same carrier frequency of 1176.450 MHz. This property is used to fulfill the reconfigurability requirement of the receiver front-end as discussed in 2.4.2. Also, as will be explained in section 4.3, the mixers are designed such that the two main drawbacks of the zero-IF architecture, i.e. DC-offset and flicker noise are overcome.

Fig. 3.12 shows the new front-end architecture. In this front-end, three individual paths are placed in parallel. Each path is a complete quadrature zero-IF receiver front-end. The only difference between them is their local oscillator frequencies. The remainder of the circuit is repeated which makes the design process fast and more efficient. One path is used for GPS L1 and Galileo E1, another one is used for GPS L2C and the third path is used for GPS L5 and Galileo E5a.

The advantage of this architecture is that, if necessary, it only requires an additional path to process an extra band, e.g. E5b, since the paths are identical. As an additional flexibility option, tunable local oscillators can be used to select the carrier frequency of each band.

Each path consists of an LNA and a band select filter, a quadrature zero-IF mixer, a quadrature local oscillator and for each I and Q branches, a low-pass filter, baseband amplifier, automatic gain control (AGC) and a reconfigurable 4-bit ADC.

Having three separate paths provides the flexibility of the antenna selection. It can have a multi-band antenna or a wide-band antenna connected to the front-

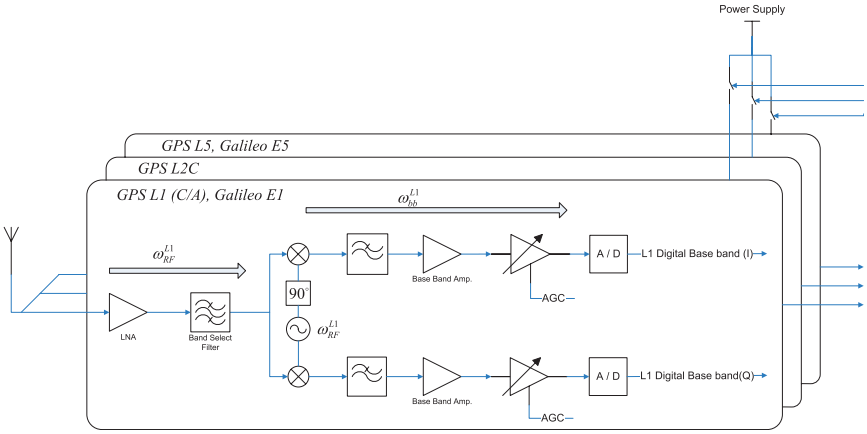


Figure 3.12: Proposed GPS/Galileo receiver front-end architecture

end using a splitter and band-pass filters or three separate antennas connected to each path or a combination of them.

3.2.1 Proposed Front-end Characteristics

This receiver front-end provides flexibility during operations. As it was explained previously, LEO satellites would be operating in different scenarios. In some operation modes, the power consumption is crucial while in some others, the accuracy is important. Scientific GNSS applications require as many signal bands as possible to improve the quality of their analyses. On the other hand, in navigation applications, the number of the signal bands is decided by the required positioning and navigation accuracy. By using the proposed architecture, the receiver has the capability to provide all available signal bands and change the operation mode, e.g. during the shortage of power, to low accuracy.

In order to achieve this flexibility, each path has an enable switch which can turn it on or off depending on the number of the required signals. Also the ADC is de-

Table 3.3: The ADC operation modes and their sampling frequencies

Mode	**Sampling**	**Path 1**		**Path 2**	**Path 3**	
	freq. [MS/s]	GPS L1	Galileo E1	GPS L2C	GPS L5	Galileo E5a
M1	3.125	+	+	+		
M2	6.250	+	+	+		
M3	12.500	+	+	+		
M4	25.000	+	+	+	+	+

signed to have four sampling rate modes to provide the necessary sampling rate depending on the selected signals. Based on the selected signal and the accuracy requirement, it is possible to select between 3.125 MS/s, 6.25 MS/s, 12.5 MS/s and 25 MS/s. Table 3.3 gives an overview of different modes of operation and their sampling frequencies. The ADC of each path is able to select its required mode of operation independently by receiving the command from on-board computer (OBC), e.g. through the back-end.

If the receiver is working only with GPS L1 then it is reasonable to work in mode M1 with a sampling frequency of 3.125 MS/s to meet the Nyquist criteria. Galileo E1 is CBOC where the main power is within the BOC(1, 1) modulation. Thus, mode M1 can be used although the signal power is reduced. Mode M2 with sampling frequency of 6.25 MS/s can also be used as an option to improve the signal processing, for example increasing the signal power by taking more side lobes into account. Mode M3 is more suitable for Galileo E1 since this mode covers the complete CBOC frequency band. When full capacity of path 1 is used, i.e. all codes of GPS L1 and Galileo E1, the ADC should work at mode M4 where sampling frequency meets the Nyquist criteria.

Activating path 2 is similar to using path 1. If path 3 is activated then the corresponding ADC should only be working in mode M4 to meet the Nyquist criteria for GPS L5 and Galileo E5a.

3.2.2 Integrated Receiver Architecture

This architecture provides an excellent flexibility in terms of resource allocation and relaxes the requirements of the digital back-end. Based on the requirements of each mode of operation, the digital processor can optimize its performance for that operation scenario. The back-end processor can work at its full power to track all of the available satellites in all channels, which consumes high power, or work at low power mode to track only the necessary number of satellites.

Fig. 3.13 shows the integration of the analog front-end and the digital back-end.

The three front-end paths provide their baseband digitized signal individually to the back-end. The back-end, depending on the mode of operation, searches for the satellite signals and assigns channels to track the acquired satellite signals. Since the number of available satellite signals will be more than for a normal single band receiver, the number of allocated channels should be higher in order to track as many satellites as possible.

The OBC defines the mode of operation of the receiver and sends the commands to the back-end which allocates the number of channels and selects the required front-end paths. The number of channels can be allocated dynamically in order to achieve back-end flexibility. The operation principle of each channel was ex-

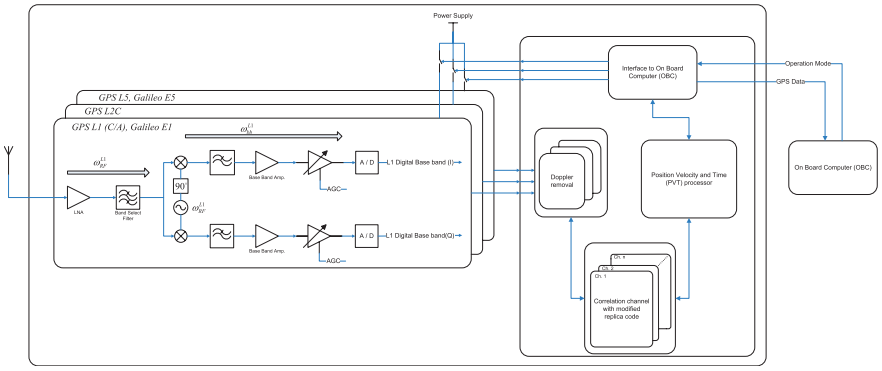


Figure 3.13: Proposed GPS/Galileo receiver front-end architecture

plained in section 2.3.1.

The main difference of the proposed system with the one explained in section 2.3.1 is that here, the signals are at baseband instead of IF. However, the Doppler shift of each satellite signal will be present and should be extracted for each channel separately. The calculated raw data (pseudorange, Doppler shift, carrier phase, etc.) is then transferred to the PVT processor to generate the navigation solution and depending on the operation mode, the raw data or the PVT solution will be transmitted to the OBC or attitude and orbit control system (AOCS) depending on the satellite subsystem architecture.

3.3 Summary

This chapter provided an overview of the three main receiver front-end architectures, i.e. direct sampling, heterodyne and zero-IF. The advantages and disadvantages of these architectures were discussed. After a thorough comparison, it was concluded that an architecture based on zero-IF is the most suitable for this application. Based on this conclusion, a reconfigurable front-end architecture has been proposed which can process GPS (L1, L2C and L5) and Galileo (E1 and E5a) signals. The main challenges of this architecture are the DC-offset and flicker noise which will be tackled in section 4.3. The following chapters will cover the development of this receiver front-end building blocks.

4

Front-end Receiver Circuit Design

In the previous chapters, the basics of GNSS receivers have been discussed followed by an introduction of the possible receiver front-end architectures. Finally, the most suitable architecture, i.e. zero-IF, was selected to be used in the design. In this chapter, the detailed design procedure of the building blocks of the receiver front-end is presented.

There are different architectures for each block of the front-end. Thus, the most suitable should be selected for this application and, where possible, innovative solution be provided. In this chapter, it is assumed that the signal is passed through the band select filter and is amplified by the LNA. In the following the design procedures of the mixer, baseband amplifier, oscillator and the ADC are explained in detail. Since standard LNA and AGC solutions are suitable for this architecture, their design are excluded from this thesis.

4.1 IC Technology Selection

Before starting the circuit design, it is important to select the appropriate IC technology. In selecting the IC technology, three constraints are considered: suitable for space applications, widely practiced by consumer electronics and cost efficient. TU Delft is a member of EUROPRACTICE [105] and has access to state-of-the-art IC technologies for education and research purposes at reduced cost. Thus, the first two constraints are taken into account in selecting the IC technology from the available technologies. The list of available technologies through EUROPRAC-

Table 4.1: List of available IC technologies through EUROPRACTICE [105]

Foundry	Feature size	Technology
ON Semiconductor (formerly AMIS)	0.7 μm, 0.5 μm and 0.35 μm	CMOS logic and mixed
ams	0.8 μm - 0.18 μm	CMOS logic and mixed
IHP	0.25 μm - 0.18 μm	SiGe:C BiCMOS
LFoundry	0.15 μm	Low Power and RF CMOS
TSMC	0.25 μm, 0.18 μm, 0.13 μm, 90 nm, 65 nm and 40 nm	CMOS logic and mixed
UMC	0.25 μm, 0.18 μm, 0.13 μm, 90 nm and 65 nm	CMOS logic and mixed

TICE with their specifications are provided in Table 4.1.

It was mentioned in section 2.4.2 that the feature size of the COTS CMOS technology suitable for space applications shall be less than 0.18 μm. Thus, considering technology feature sizes for logic and mixed signal CMOS technology of each foundry as given in Table 4.1, foundries TSMC and UMC provide such technologies. Since smaller feature sizes are more expensive and 0.13 μm is widely used in consumer electronics, UMC 0.13 μm is selected for its better accessibility and lower price as compared to TSMC 0.13 μm.

4.2 System Level Specifications

The process of receiver design starts with defining the requirements of the system and the parameters of each building block. This receiver front-end is aimed to be used for both GPS and Galileo signal reception. Thus, the following requirements shall be satisfied:

NAV-FE-00 The front-end sensitivity shall be better than -133 dBm.

NAV-FE-01 The front-end shall be able to process L1, L2C, L5, E1 and E5a frequency bands.

NAV-FE-02 The front-end shall be reconfigurable in terms of frequency bands.

NAV-FE-03 The front-end output shall be 4-bit digital with reconfigurable sampling frequency.

NAV-FE-04 The total noise figure (NF) shall be less than 2 dB.

NAV-FE-05 The total Gain shall be 120 dB.

NAV-FE-06 The group delay shall be constant (linear phase response).

NAV-FE-07 The front-end shall be radiation tolerant.

NAV-FE-08 The operating temperature of the front-end shall cover $-40°C$ to $+85°C$.

In order to satisfy these requirements, the link budget is calculated. The link budget defines the specifications of each building block and is calculated such that the total behavior of the system satisfies the requirements. In this part, the link budget of the first path of the front-end architecture, as introduced in chapter 3, is calculated which processes the L1/E1 band.

The link budget is summarized in Table 4.2. In this table all the parameters of the building blocks are listed. Each row of the table is a design parameter. The columns show the building blocks and for each column the relevant rows are filled. The definitions of the parameters were introduced in section 2.4. The specifications defined in a link budget are noise factor (noise figure), IIP3, SFDR, gain, input frequency and bandwidth, phase noise, input power and target power consumption. The main blocks of each path of the receiver front-end are LNA, Mixer, oscillator, baseband amplifier, AGC and ADC.

The noise factor is a parameter which shows how much noise is added to the signal by the system, i.e. the receiver front-end in this case. When the noise factor is given in dB, it is called noise figure. The requirement NAV-FE-04 dictates that the total noise figure of the front-end shall not exceed 2 dB. The noise contribution of each block to the total noise figure of the front-end follows the relation [72]

$$NF = 10\log\left(F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1}}\right) \tag{4.1}$$

where F_n and G_n are the noise factors and the gains of the stage n respectively. It can be concluded from (4.1) that the gain of the first stage of the front-end determines how much the noise of the following stages will affect the total noise figure of the system. It is desired to have maximum gain at the first stage. However, this is not practical due to distortion and nonlinearities. The typical gain of an LNA (including band select filter) is about 15 - 20 dB and noise figure of less than 2 dB can be achieved by using technologies such as SiGe [99, 100]. The gain of each stage in link budget in Table 4.2 is the typical gain of stage except for the mixer. As will be shown in section 4.3 and section 5.2, the proposed mixer for this front-end has unique characteristics. A noise figure of less than 10 dB can be achieved by this mixer and the conversion gain can be higher than 60 dB. Because of this very high gain, the noise performance of the baseband amplifier and AGC has no effect. The noise figure and gain of each block is given in Table 4.2 resulting to the total noise figure of the front-end to be 2.25 dB.

Based on the ITU regulations mentioned in section 2.4.2, it was concluded that the SFDR of the receiver shall be at least 64 dB and IIP3 of the LNA (including

band-select filter) shall be -37 dBm. Since the out-of-band interferers are removed by the LNA and band-select filter, the SFDR of the following stages are set to 20 dB which is the difference between the noise floor and the received signal. The IIP3 of the rest of the blocks are calculated by (2.30) and presented in Table 4.2.

The input frequency of the LNA and mixer is the carrier RF frequency which is 1.57542 GHz for the first path. The blocks following the mixer shall work at baseband. The frequency of the oscillator shall be equal to the RF carrier frequency. The bandwidth of the LNA and mixer shall be at least 6.138 MHz to maximize the received energy of the GPS C/A and E1 OS codes. However, the system target is to use full capacity of the GPS and Galileo signals thus, the bandwidth shall be 24.552 MHz. The following stages shall operate at half this bandwidth, i.e. 12.276 MHz, since they are operating in baseband.

The oscillator shall be quadrature and its phase noise shall not exceed -110 dBc/Hz at 1 MHz which is a phase noise of a typical quadrature LC oscillator. The ADC shall have 4-bit and be reconfigurable to be able to support various sampling rates. In the following sections, the selected architecture of each building block is developed.

4.3 Mixer

It has been explained in section 3.1.3 that the mixer is the most critical block of the zero-IF architecture. In this section, an introduction to different mixer architectures is given followed by an innovative mixer circuit which provides a solution to both the DC offset and the flicker noise problems of the zero-IF architecture.

As mentioned before, the LNA amplifies the received RF signal. The output of the LNA is centered at the carrier frequency. In general, to use the information of this signal, it should be down-converted to baseband for final processing. The mixer performs the process of the frequency change. A mixer is a 3-port electronic element with two inputs and one output. The output is the multiplication of the inputs.

In general, mixers consist of semiconductor switches and filters. Mixers can be divided into two categories, passive and active. Passive mixers do not consume static power. Thus, their conversion gain is less than 0 dB (typically -4 dB [72]) which increases the influence of the noise of the next stage, i.e. the baseband amplifier, significantly. Active mixers use biased transistors thus, consume static power while having a conversion gain of typically 10 dB [106]. An example of passive and active mixers is depicted in Fig. 4.1a and Fig. 4.1b respectively.

Table 4.2: GPS/Galileo receiver front-end link budget

	LNA	**Band Select Filter**	**Quadrature Oscillator**	**Mixer**	**Low-pass Filter**	**Baseband Amplifier**	**VGA**	**ADC**	**Complete Front-end**
Noise Figure [dB]	2	3	-	10	3	4	4	-	2.25
Gain [dB]	23	-3	-	60	-3	30	13	-	120
IIP3 [dBm]	-37	100	-	-80	100	-20	7	-	-104
SFDR [dB]	64	64	-	20	100	20	20	-	64
Operation frequency [MHz]	1575.42	1575.42	1575.42	1575.42	Baseband	Baseband	Baseband	-	1575.42
Bandwidth [MHz]	24.552	24.552		24.552	12.276	12.276	12.276	12.276	24.552
Phase noise [dBc/Hz @1MHz]	-	-	-110	-	-	-	-	-	-
Input power [dBm]	-133	-130	-	-110	-50	-53	-23	-3	-133
Power consumption [μW]	<20000	-	<10000	<40000	-	<300	<300	<100	<75000

When the switching transistors of the mixer are biased at a nonzero drain current, they contribute flicker noise to the output [107, 108]. The flicker noise is proportional to the channel current and inversely proportional to the transistor length [109]. Thus, passive mixers generate very low flicker noise while active mixers introduce flicker noise especially, when designed by CMOS transistors. The linearity of the passive mixers is better than their active counterparts [101,110]. Thus, a passive mixer is usually the preferred choice for zero-IF architectures. However, this increases the burden on the baseband amplifier to have a higher gain and very low noise. A comparison of passive and active mixer architectures is summarized in Table 4.3.

To solve this problem, a special active mixer architecture is required such that it will not suffer from flicker noise and 2^{nd} order nonlinearity. As will be explained later in this section, a novel mixer structure is proposed which bypasses the DC offset and the flicker noise problems while providing a zero-IF output. This mixer is based on the double balanced Gilbert mixer and provides a very high gain.

Table 4.3: Comparison of passive and active mixer architectures

	Passive	**Active**
Amplification	no	yes
Flicker noise	no	yes
nonlinearity	no	yes
Power consumption	dynamic	static
Chip area	small	moderate

4.3.1 Mixer Design Constraints

Table 4.2 provided the summary of the parameters of each building block according to the application requirements. The key parameters that drive the mixer design are the noise figure, gain and the nonlinearity.

Based on the link budget calculation, the GPS/Galileo signal power at the input of the mixer will be -110 dBm. This is equivalent to 1 μV considering a 50 Ω input impedance. To achieve the full scale swing at the input of the ADC, i.e. 150 mV, a total gain of 106 dB should be achieved by the mixer, baseband amplifier and the AGC. The more gain the mixer provides, the more relaxed the noise requirements of the baseband amplifier will be. Thus, the mixer is designed to have a higher gain than what is calculated in the link budget. The noise figure and the linearity performances are targeted as calculated in the link budget.

The nominal thermal noise floor for GPS/Galileo signal with 2.046 MHz bandwidth at the receiver input is -111 dBm. In designing the mixer, the GPS/Galileo

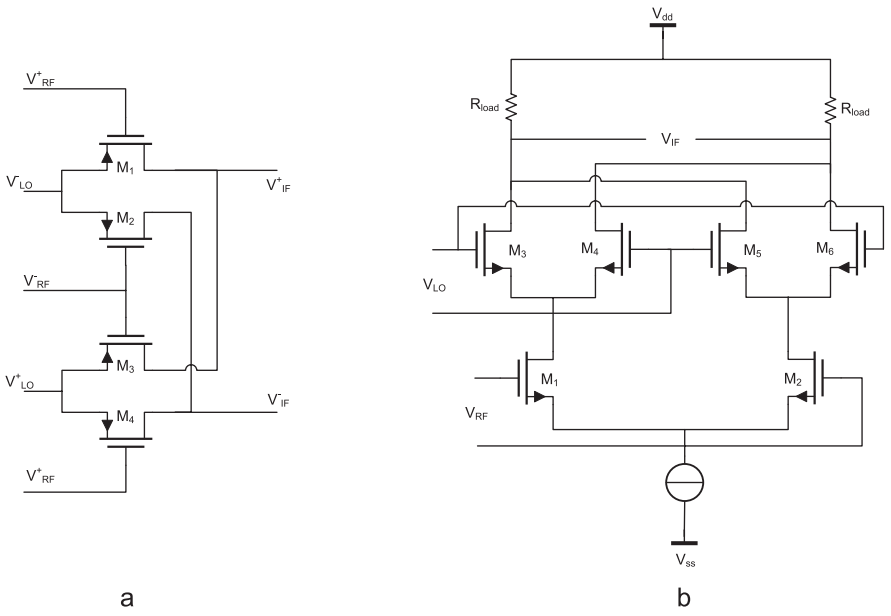


Figure 4.1: Passive and active mixers: a) Passive (CMOS) mixer b) active (double balanced Gilbert) mixer

signal level is considered to assure the required mixer sensitivity. However, in determining the total gain of the receiver, the input noise power shall be considered which includes thermal noise and sky noise which may vary depending on the antenna orientation.

4.3.2 Proposed Solution

There have been several attempts to solve the above mentioned problems [102–104, 111]. Considering the advantages and disadvantages of the previous approaches, a novel architecture is proposed which is a combination of different techniques to overcome the aforementioned problems. Fig. 4.2 shows this architecture [112]. This architecture contains four signal paths. The proper combination of their outputs generates the in-phase and quadrature-phase baseband signals, I_{BB} and Q_{BB} respectively.

Fig. 4.3 graphically depicts the down-conversion process. In this figure, frequency is shown by the horizontal axis and the vertical axis represents the conversion procedure. The RF frequency is shown by color yellow and the IF and baseband frequencies are depicted by colors green and blue respectively. The down-conversion happens in two steps. In the first step the signal is down-converted to an internal intermediate frequency (IF) by the high frequency (HF) mixers using a

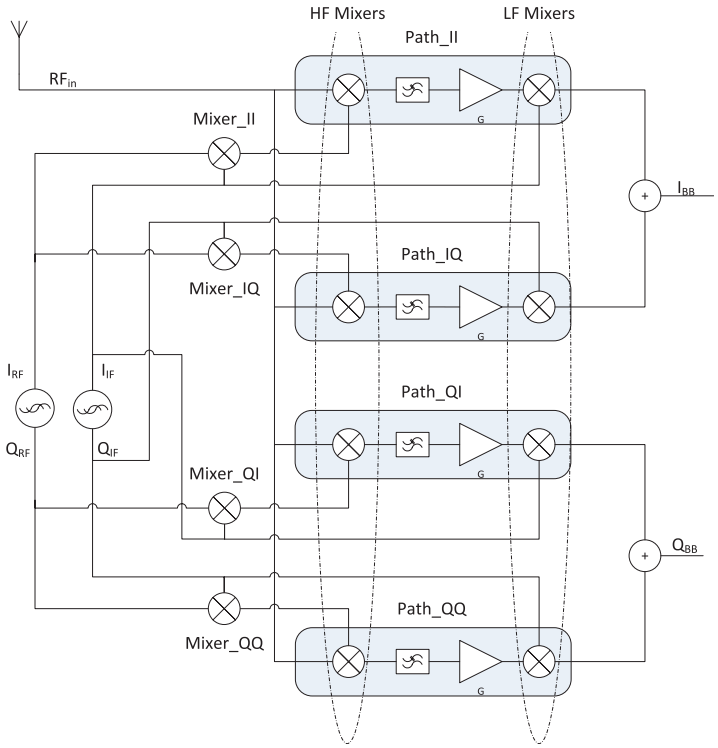


Figure 4.2: Proposed mixer architecture

dual-tone oscillator signal which is shown by yellow-green oval. This process generates four quadrature signals at IF. These signals are amplified and filtered which results to bypassing the flicker noise and DC offset of the first mixer. In the second step it is down-converted to baseband by the low frequency (LF) mixers.

Since after the first step, the signal is at IF it will not be affected by the flicker noise and possible DC offset of the HF mixers. The IF signal is amplified and due to the bandpass characteristic of the IF amplifier, the flicker noise and the possible DC offset are filtered. In this way, the high frequency component of the HF mixers are also removed.

The remaining flicker noise, in addition to the flicker noise generated by the IF amplifier, will be up-converted to a higher frequency by the LF mixers. The signal has already been amplified significantly. Thus, the flicker noise and the possible DC offset of the second mixer stage will not have a considerable effect on the SNR of the baseband output.

In this mixer architecture, there are two local quadrature oscillators: LO1 and LO2. The LO1 frequency shall be equal to RF carrier frequency and the LO2 fre-

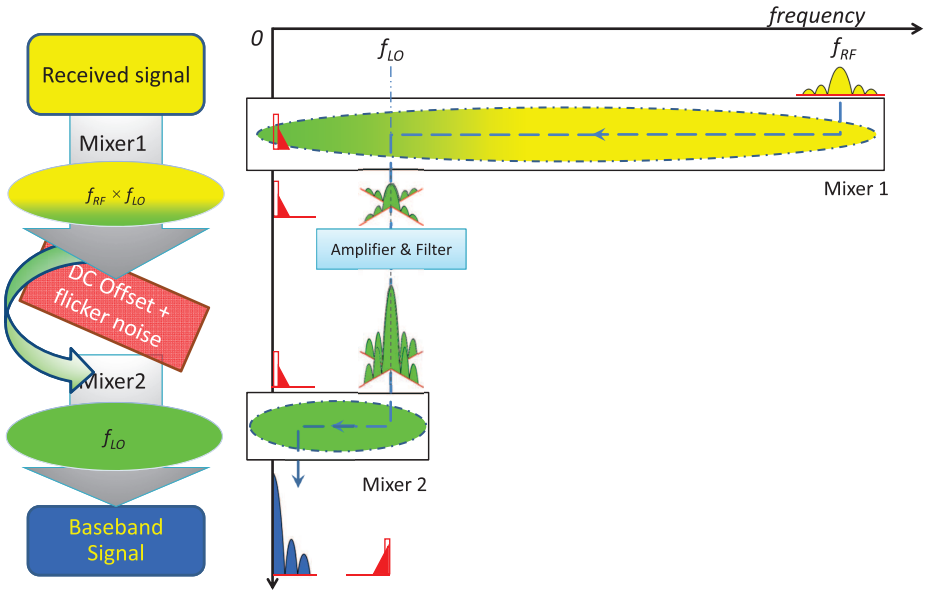


Figure 4.3: Conversion process by the proposed mixer. The horizontal axis is frequency and the conversion process is depicted next to the vertical axis. RF, IF and baseband signals are distinguishable by colors yellow, green and blue respectively. DC offset and flicker noise are depicted by white and red colors.

quency is equal to the IF frequency:

$$\omega_{LO1} = \omega_{RF} \tag{4.2}$$

$$\omega_{LO2} = \omega_{IF} \tag{4.3}$$

where ω_{LO1}, ω_{LO2}, ω_{RF} and ω_{IF} are the LO1, LO2, RF and IF frequencies respectively.

In this architecture, the baseband output is independent of the IF frequency as long as it falls within the bandwidth of the IF amplifiers. This provides the flexibility that any variation of the LO2 frequency will not affect the output signal and will remain at baseband.

Traditionally in multi-step down conversion mixers, the first local oscillator is a single tone with either $\omega_{RF} + \omega_{IF}$ or $\omega_{RF} - \omega_{IF}$ frequencies. When this tone is multiplied by the received signal, the resulting output will be centered at ω_{IF} and $\omega_{RF} + \omega_{IF}$ or at ω_{IF} and $\omega_{RF} - \omega_{IF}$ respectively. In the proposed architecture, a

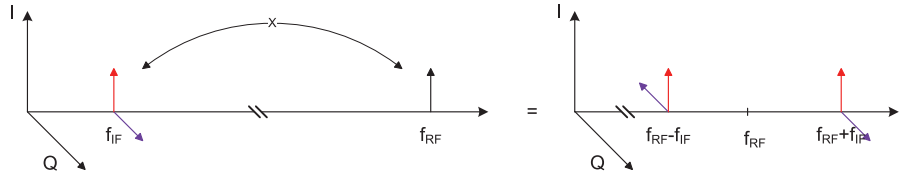


Figure 4.4: Frequency spectrum of the dual-tone oscillator inputs of the HF mixers in Path_II and Path_IQ

dual tone oscillator signal is used which employs both $\omega_{RF}-\omega_{IF}$ and $\omega_{RF}+\omega_{IF}$ to improve the performance.

As depicted in Fig. 4.2, the LF mixers are directly fed by either the in-phase or the quadrature-phase outputs of LO2 (I_{IF} and Q_{IF}). The HF mixers on the other hand, are fed with dual-tone signals which are generated by mixing the in-phase and the quadrature-phase outputs of LO1 (I_{RF} and Q_{RF}) with I_{IF} and Q_{IF}. Thus, the four dual-tone signals that are fed to the HF mixers are as following:

$$\begin{cases} M_{II}: \cos(\omega_{RF}t)\times\cos(\omega_{IF}t) = \frac{1}{2}\left[+\cos((\omega_{RF}-\omega_{IF})t)+\cos((\omega_{RF}+\omega_{IF})t)\right] \\ M_{IQ}: \cos(\omega_{RF}t)\times\sin(\omega_{IF}t) = \frac{1}{2}\left[-\sin((\omega_{RF}-\omega_{IF})t)+\sin((\omega_{RF}+\omega_{IF})t)\right] \\ M_{QI}: \sin(\omega_{RF}t)\times\cos(\omega_{IF}t) = \frac{1}{2}\left[+\sin((\omega_{RF}-\omega_{IF})t)+\sin((\omega_{RF}+\omega_{IF})t)\right] \\ M_{QQ}: \sin(\omega_{RF}t)\times\sin(\omega_{IF}t) = \frac{1}{2}\left[+\cos((\omega_{RF}-\omega_{IF})t)-\cos((\omega_{RF}+\omega_{IF})t)\right] \end{cases} \tag{4.4}$$

where M_{xx} are the names of the operations corresponding to the mixers shown in Fig. 4.2.

Fig. 4.4 depicts the resulting spectrum of the first two operations in (4.4), M_{II} (red) and M_{IQ} (blue). These two use I_{RF} with both I_{IF} and Q_{IF} to generate the dual-tone oscillator signals for Path_II and Path_IQ. In the following, these two paths are considered in the calculations to generate the I_{BB} signal. A similar approach can be used to generate the Q_{BB} signal by using M_{QI} and M_{QQ} operations of (4.4).

In paths II and IQ, first the received signal, $A_{RF}\cos(\omega_{RF}t+\phi)$, is mixed with the signals given in (4.4) to generate the internal IF signal. These signals, after low-pass filtering, can be expressed by:

$$\begin{cases} IF_{II} = \dfrac{A_{RF}}{4}\left[\cos(\omega_{IF}t+\phi)+\cos(\omega_{IF}t-\phi)\right] \\ IF_{IQ} = \dfrac{A_{RF}}{4}\left[\sin(\omega_{IF}t+\phi)+\sin(\omega_{IF}t-\phi)\right] \end{cases} \tag{4.5}$$

where IF_{II} and IF_{IQ} are the IF signals at II and IQ paths. These signals will be amplified by the IF amplifiers and will be mixed with I_{IF} and Q_{IF} respectively. The result is:

$$\begin{cases} BB_{II} = \dfrac{A_{RF}}{8}\left[2\cos(\phi) + \cos(2\omega_{IF}t - \phi) + \cos(2\omega_{IF}t + \phi)\right] \\ \\ BB_{IQ} = \dfrac{A_{RF}}{8}\left[2\cos(\phi) - \cos(2\omega_{IF}t - \phi) - \cos(2\omega_{IF}t + \phi)\right] \end{cases} \tag{4.6}$$

where BB_{II} and BB_{IQ} are the baseband signals of the II and IQ paths. The final baseband signal is achieved by adding these two signals:

$$I_{BB} = BB_{II} + BB_{IQ} = \frac{A_{RF}}{2}\cos(\phi) \tag{4.7}$$

where I_{BB} is the in-phase baseband signal. Similarly the baseband quadrature-phase signal, Q_{BB}, can be calculated by adding the signals of the paths QI and QQ. The result will be:

$$Q_{BB} = BB_{QI} + BB_{QQ} = \frac{A_{RF}}{2}\sin(\phi) \tag{4.8}$$

where BB_{QI} and BB_{QQ} are the baseband signals of the QI and QQ paths respectively. The image signals which are placed at $\omega_{RF} \pm 2\omega_{IF}$ are also canceled during these multiplications and summations.

The matching of the gain and phase of the different paths in this mixer are two important factors in accurate baseband construction. The effect of gain mismatch shows itself in the process of filtering by summation and the accuracy of the baseband amplitude. In the above discussion that Path_II and Path_IQ are considered. If the gains of these paths are not exactly the same then the residual of the high frequency components, i.e. at $2\omega_{IF}$, remains in the baseband output. Assuming a gain mismatch of ϵ_I, (4.6) can be written as

$$\begin{cases} BB_{II} = \dfrac{A_{RF}}{8}\left[2\cos(\phi) + \cos(2\omega_{IF}t - \phi) + \cos(2\omega_{IF}t + \phi)\right] \\ \\ BB_{IQ} = \dfrac{A_{RF}(1+\epsilon_I)}{8}\left[2\cos(\phi) - \cos(2\omega_{IF}t - \phi) - \cos(2\omega_{IF}t + \phi)\right]. \end{cases} \tag{4.9}$$

Table 4.4: The truth table of an exclusive-or (XOR) logic gate

Input 1	Input 2	Output
0	0	0
0	1	1
1	0	1
1	1	0

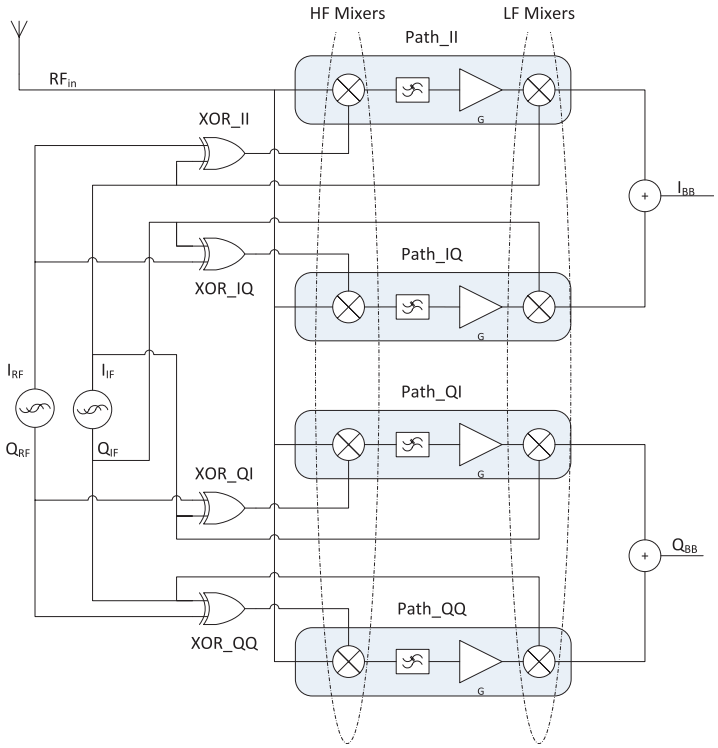


Figure 4.5: Proposed mixer architecture with digital implementation

In this case the resulting baseband signal will become

$$I_{BB} = \frac{(2+\epsilon_I)A_{RF}}{4}\cos(\phi) - \frac{(\epsilon_I)A_{RF}}{8}\big(\cos(2\omega_{IF}t-\phi)+\cos(2\omega_{IF}t+\phi)\big) \qquad (4.10)$$

which includes high frequency components. In addition, the accuracy of the amplitude of the baseband signal is disturbed by $\epsilon_I/4$. The same holds for Q_{BB}. It includes high frequency components in addition to an amplitude error of $\epsilon_Q/4$. The result of the amplitude errors is inaccuracy in the carrier phase measurements as introduced by (3.12).

The phase mismatch results in code phase error. The phase mismatch can be caused by mismatch in bandwidths of the paths resulting in different group delays. If the bandwidths of the paths are different, the slope of the phase response will not be the same which results in code phase error. The code phase error can also appear when the center frequencies of the frequency responses are not the same. In this case, the phase shifts applied to different frequencies will not be the same in both paths. However, the amount of the mismatch can be reduced by matching techniques in IC layout design to limit the error within an acceptable range.

The RF oscillator, LO1, may show some offset from the nominal value. The effect of this offset is similar to an additional Doppler shift. This offset is directly transferred to the output. This property can be beneficial to set an offset such that all Doppler shifts are positive.

To achieve a better linearity and performance, usually the oscillators are designed to generate square waves with the same fundamental frequency as the single tone oscillators [113]. Thus, the oscillator outputs can be treated as digital signals which provides the opportunity to simplify the design. In this case, the mixers Mixer_II, Mixer_IQ, Mixer_QI and Mixer_QQ can be replaced by a two input exclusive-or (XOR) logic gate. The truth table of a two input XOR gate is given in Table 4.4. From the table, it can be concluded that the output is the multiplication of its inputs, considering a one-to-one map of $\{0,1\}$ to $\{+1,-1\}$.

Since the power consumption of the XOR gate is dynamic, its average power consumption is considerably lower than that of a mixer circuit. The XOR also occupies less chip area which provides the added benefit of reducing the cost. Fig. 4.5 depicts the mixer architecture with this improvement.

As it was mentioned earlier, the oscillators are independent. However, it is possible to generate the low frequency oscillator signal from the high frequency oscillator by using a "divide by N" circuit. This circuit is a digital circuit. Thus, it has a dynamic power consumption. Its average power consumption will be less than an oscillator with static biasing current. Its chip area will also be less than an individual low frequency oscillator which reduces the fabrication cost further. The inaccuracy of the output frequency of the divider circuit has no effect on the baseband signal since the dual-tone signal is generated by both LO1 and LO2 oscillator signals and any variation in the LO2 signal will be canceled in the following stages, i.e. 2^{nd} mixer and adder. The architecture with frequency divider is depicted in Fig. 4.6.

Innovative Aspects

This mixer tackles the flicker noise and DC offset problems of the zero-IF architecture. It employs a unique combination of two quadrature oscillator signals to be used in the down-conversion process. The dual-tone structure of this signal makes it possible to use a combination of low-pass filtering and signal addition to generate the baseband signal and filter all undesirable signals.

Translating the RF signal to an internal IF frequency prevents the destructive effect of the flicker noise and DC offset of the first mixer on the signal. Amplification of the signal at IF reduces the effect of the flicker noise and DC offset of the second stage mixer by increasing the SNR. The second mixing up-converts the remaining flicker noise of the previous stages to higher frequencies which will be filtered af-

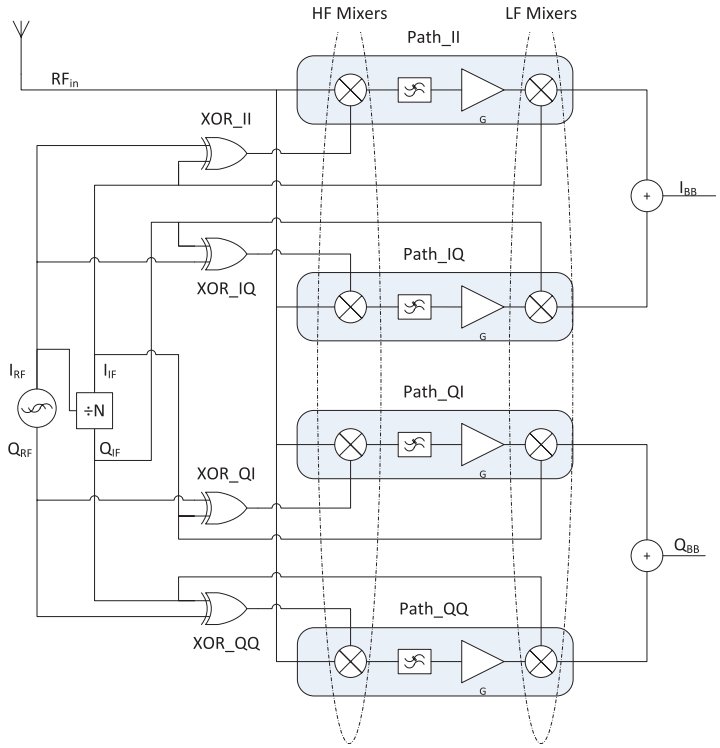


Figure 4.6: Proposed mixer architecture with frequency divider implementation

terwards. Since the baseband signal has been considerably amplified, the flicker noise of the baseband amplifier has a negligible effect on the signal. This architecture also makes monolithic chip design feasible as no complex and external filtering is required.

4.4 Oscillator

The mixer receives a sine or a square wave at one of its inputs. An oscillator is the circuit which generates this sine or square wave with a determined frequency. Its frequency could be designed to be fixed or tunable within a certain range.

There are several approaches in designing an oscillator. The three commonly used on-chip oscillators are ring oscillators, LC oscillators and relaxation oscillators. Each approach uses a specific characteristic of the circuit to generate the oscillation.

The ring oscillator consists of an odd number of inverters connected in a ring

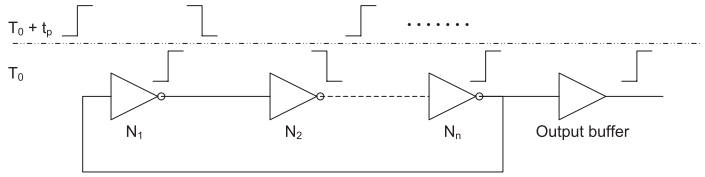


Figure 4.7: Ring Oscillator

as depicted in Fig. 4.7. The figure shows the outputs of each inverter stage at T_0 and $T_0 + t_p$ where T_0 is the starting time and t_p is the oscillating period. As shown in Fig. 4.7, when the output of inverter N_1 is high, the output of the next inverter, N_2, is low. This process continues until the output of the n^{th} inverter (which is the input of the first inverter) is high which turns the inverter N_1 to low (at $T_0 + t_p$) and the following inverters start to toggle their outputs. The output can be taken from any of the outputs and is usually buffered. The frequency of the oscillator depends on the number of the inverters and their propagation delays, t_d, which is mainly determined by the size of their transistors. The frequency of the ring oscillator, f_{ring}, can be determined by:

$$\begin{aligned} t_p &= t_{d1} + t_{d2} + ... + t_{dn} \\ f_{\text{ring}} &= \frac{1}{t_p}. \end{aligned} \tag{4.11}$$

The chip area used by the ring oscillator is smaller, its power consumption is lower and its tunable frequency range is wider than LC oscillators which is attractive for low cost chip design [114]. However, the drawback is the poor phase noise performance which makes it unsuitable for applications which require accurate frequencies [115].

LC oscillators are working based on LC resonators and negative transconductance (Negative g_m) circuit [72]. The parallel combination of an inductor and a capacitor, i.e. LC tank, shows a frequency dependent impedance. Ideally, the impedance becomes infinite at resonance frequency, ω_{res}. This frequency for an inductor with inductance L_1 and a capacitor with capacitance C_1 is calculated by

$$\omega_{\text{res}} = \frac{1}{\sqrt{L_1 C_1}}. \tag{4.12}$$

Ideally, the quality factor, Q, should be infinite. Thus, a current impulse would cause this circuit to oscillate indefinitely. However, in practice, inductors (and capacitors) suffer from parasitics which introduce energy loss and a reduction of the quality factor. In a simplified model, the parasitics can be considered as a series

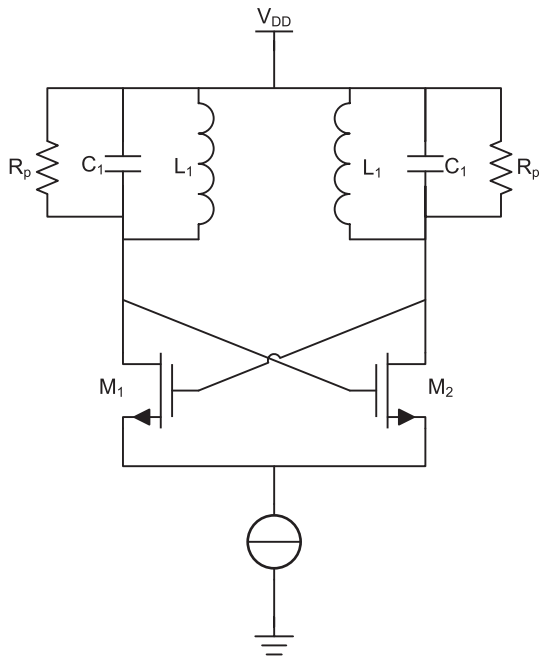


Figure 4.8: A cross-coupled LC oscillator

resistance R_s with the inductor and the quality factor of the inductance is defined by [72]

$$Q = \frac{L_1 \omega}{R_s}. \tag{4.13}$$

To simplify the design process, the series resistance can be converted to an equivalent parallel resistance, R_p, using the following relation [72]:

$$R_p \approx \frac{L_1^2 \omega^2}{R_s} = Q^2 R_s \tag{4.14}$$

The oscillating behavior can be achieved by canceling the effect of R_p. Placing a negative resistance, $-R_p$, in parallel with the LC tank will cause the parallel resistance become infinity at resonance frequency ($R_p \parallel -R_p = \infty$). The negative resistance can be achieved by using a positive feedback network when the loop gain is sufficiently negative. Fig. 4.8 depicts a cross-coupled LC oscillator. The negative resistance is the output impedance of the transistor pairs. The oscillation starts when the condition, $R_p \geq 1/g_m$, is satisfied [72].

The relaxation oscillator is an inductorless oscillator and can be easily implemented on chip in monolithic form. It is commonly used in frequency synthesizer

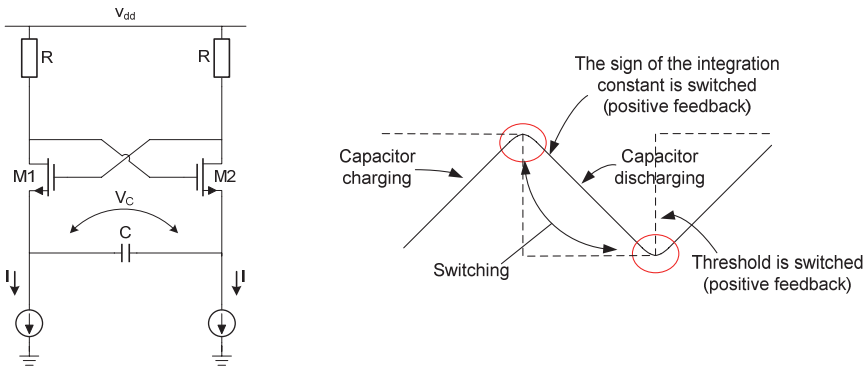


Figure 4.9: a) Relaxation Oscillator b) Capacitor voltage behavior

design. The circuit is widely used in applications such as voltage- and current-controlled oscillators for PLLs and I/Q cross-coupled oscillators [116].

Fig. 4.9a depicts the schematic of the relaxation oscillator. It operates based on charging and discharging of the timing capacitor, C, with a constant current, I_0. Fig. 4.9b depicts the voltage across the timing capacitor, V_C. As shown in this figure, the timing capacitor is charged with a constant rate to the maximum value, $V_{\max}$, at which the transistors switch their status. Thus, the sign of the voltage across the timing capacitor is changed. The switching voltage for a CMOS relaxation oscillator can be determined by [117]

$$\begin{aligned} V_{\max} &= \frac{8}{175}\sqrt{\frac{2}{35}}\frac{I_0}{g_m}(\Delta^2-\Delta-6)\sqrt{\Delta-3} \\ \Delta &= \sqrt{70Rg_m-61} \end{aligned} \tag{4.15}$$

where I_0 is the biasing current of each transistor, R is the resistive load and g_m is the transconductance of the transistors. The circuit operates as a negative feedback while $|V_C| < V_{\max}$ which causes the stable charging. As soon as $|V_C|$ reaches $V_{\max}$, the circuit behavior is changed to positive feedback and the transistors switch their status, V_C changes polarity, the charging current changes its direction and the circuit returns to negative feedback configuration [116].

The oscillation frequency is proportional to the slope of the voltage variation of the timing capacitor. In practice it can be assumed that the timing capacitor is charged with a constant current. Thus, the voltage change across the capacitor is proportional to the charging current and inversely proportional to the capacitance. The details of parameters can be found in [117–120]. In a very simple form

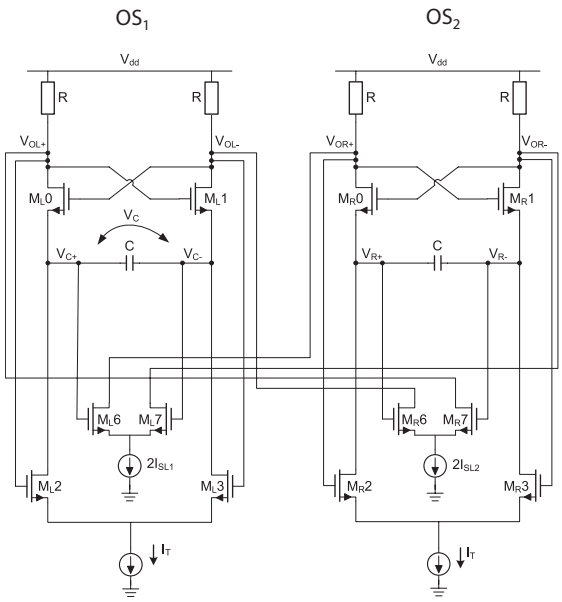


Figure 4.10: Cross coupled Relaxation Oscillator

the oscillation frequency can be determined by [117]

$$\omega_{\text{osc}} = 2\pi\left(\frac{I_0}{4CV_{\text{max}}}\right). \tag{4.16}$$

The receiver architecture requires two quadrature oscillators. As depicted in Fig. 4.10, the quadrature relaxation oscillator can be realized by cross-coupling two relaxation oscillators. The soft-limiter differential pairs, $M_{L6,7}$ and $M_{R6,7}$, sense the capacitor voltages in their respective oscillator. Their differential outputs are connected to the output of the other oscillator to couple the two oscillators.

When the capacitor voltage, e.g. V_{C1}, crosses the zero value its soft-limiter output is changed which forces the output of the other oscillator to toggle. The result will be that V_{C2} changes charging direction and when it passes zero its soft-limiter output will force the output of the first oscillator to toggle resulting in change in charging direction of C_1 and the process continues. Fig. 4.11 shows this process [118,119]. This configuration results in very accurate quadrature outputs with exactly the same frequency. The gain of the soft-limiter should be high to minimize phase errors however, at the same time, should be low enough to maximize the achievable frequency [116].

Cross-coupling the relaxation oscillator improves the circuit behavior compared to stand alone relaxation oscillator. It increases the precision of the oscillation frequency and guarantees that the two outputs are exactly in quadrature [118, 119].

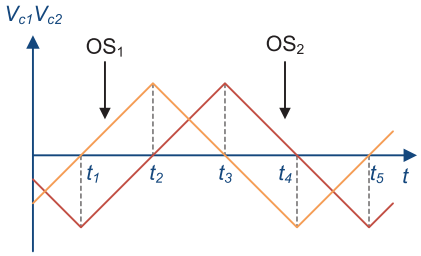


Figure 4.11: Voltage variation of the capacitors of a cross-coupled relaxation oscillator

The effects of non-idealities such as mismatches are attenuated by the feedback mechanism in this configuration. Even though a single relaxation oscillator has a poorer phase noise performance than an LC oscillator, the phase noise of the cross-coupled configuration is comparable to the cross-coupled LC oscillators [120].

The GPS/Galileo carrier phase measurement accuracy depends on how accurately the I and Q signals are generated. The effect of the phase error of these signals appears in (4.4) which consequently introduces errors in the outputs (4.7) and (4.8). These outputs determine the carrier phase measurement as given by (3.11).

Table 4.5 provides a comparison list of the three introduced oscillator types. Considering importance of the phase accuracy in carrier phase measurement and the chip area constraint as mentioned earlier, i.e. inductor-less design, the best choice of oscillator is a first order relaxation oscillator. This type of oscillator is easily implemented in monolithic form.

4.5 Amplifier

An amplifier is one of the main blocks of the receiver front-end. As given in Table 4.2 and by including the filter losses, the signal should be amplified 126 dB in total. This amplification is distributed among LNA, Mixer, baseband amplifier and VGA.

Table 4.5: Comparison of different oscillator architectures

	Ring osc.	**LC osc.**	**Relaxation osc.**
Phase noise	poor	good	good (cross-coupled)
Power consumption	dynamic	static	static
Chip area	small	large	moderate

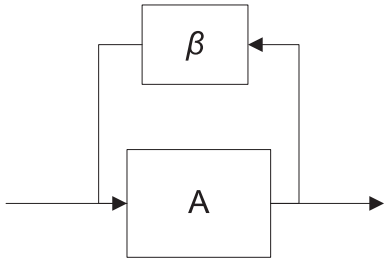


Figure 4.12: Feedback system

In this section the IF and baseband amplifiers will be discussed. The IF amplifiers are required in the mixer architecture and the baseband amplifiers are placed after the mixers. In amplifier design three main parameters should be taken into account: noise, bandwidth and distortion [121]. These three parameters can be tackled in an orthogonal manner as discussed in [122].

The total noise is determined by the noise and gain of the first stage in an amplifier. The IF amplifier must be low noise. However, the signal is already amplified by the LNA and the first stage of the mixer which relaxes the noise requirement of the IF amplifier. As explained in section 4.3.2, the flicker noise does not fall within the signal band during IF amplification. Thus, it can be ignored in the noise calculation of the IF amplifier.

The transient frequency, f_T, of the transistors of the technology is defined as the frequency at which the current gain of the transistor is unity. This parameter has an important influence on determining the bandwidth of the amplifier. Higher f_T implies a potential for higher bandwidth. Other than f_T, parasitics and the topology of the amplifier determine its bandwidth.

Distortion or nonlinearity is another important factor in amplifier design. Other than harmonic and intermodulation distortion, explained in section 2.4.1, clipping distortion should be prevented in the amplifier. Clipping can occur in any of the transistor stages within the amplifier and happens when the operating point of the transistor is shifted out of the saturation in CMOS transistors. This could occur by incorrect biasing or unexpected load behavior.

When the frequency of the signal is much lower than f_T of the transistor, the amplifier can be designed by using linear feedback. Fig. 4.12 depicts a general linear negative feedback system. The total transfer function of the system, A_t, can be expressed by [122]

$$A_t = \frac{A}{1 - A\beta} \tag{4.17}$$

where A is the open loop gain and β is the gain of the feedback network. The loop

gain, L, is defined by:

$$L = A\beta. \tag{4.18}$$

The characteristic equation of the system is defined as $1 - L$ by which the behavior of the system is analyzed [122]. Having a feedback system provides the opportunity to have an accurate transfer. In such a case, the transfer can be determined by the feedback. This can be achieved when the loop gain is high. Since the transfer is determined by the feedback, to have an accurate transfer function, the open loop gain should be increased as much as possible. When the condition $A\beta \gg 1$ is satisfied, the total transfer function can be written as

$$A_{t\infty} = \frac{1}{\beta}. \tag{4.19}$$

However, if the open loop gain can not be increased sufficiently then using feedback network does not provide any advantage. In such cases the required gain can be achieved by the open loop gain.

If the bandwidth of the IF amplifier is extended to DC, then the same design can be used for the baseband amplifier. The signal has already been amplified such that the flicker noise of the baseband amplifier has negligible effect on the SNR. In the next chapter, the details of the IF and baseband amplifier design will be explained.

4.6 Analog to Digital Converter

The last stage in the front-end is the ADC. The ADC receives the analog signal at the input and delivers its digital equivalent at the output. There are different ADC architectures: sigma-delta (Σ-Δ), successive approximation register (SAR), pipeline, folding + interpolating and flash ADC. Each of these architectures is suitable for a certain range of applications. Fig. 4.13 depicts different ADC architectures and their operation regions in term of sampling rate (speed) and resolution. Table 4.6 provides an overview of latency, speed, accuracy and chip area of each ADC architecture.

As depicted in Fig. 4.13 as well as Table 4.6, the sigma-delta (Σ-Δ) ADC is suitable for high resolution and low sampling rate while occupying medium chip area and showing high latency. However, its accuracy is high. The SAR ADC architecture operates on higher sampling rate with above average accuracy while showing low latency and occupies low area. The pipeline architecture goes higher in sampling rate with above average accuracy but shows high latency and occupies average area. There is an overlap between sampling rate of pipeline and SAR architectures.

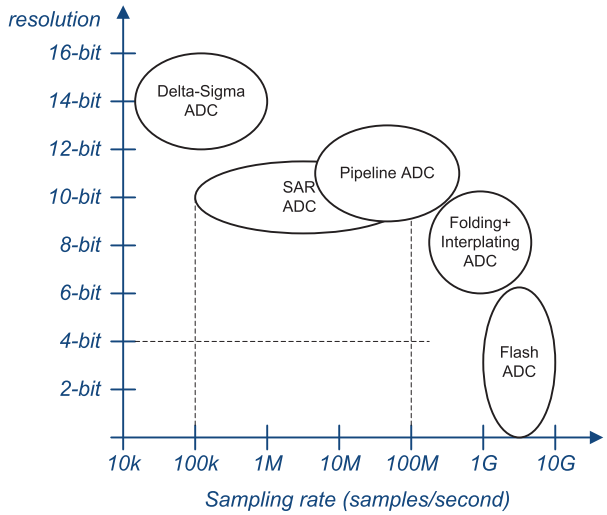


Figure 4.13: Comparison of ADC architectures vs. resolution and sample rate [123]

The folding + interpolation architecture operates on the higher border sampling rate of the pipeline with average accuracy. Its latency is low while it occupies large area. The flash architecture has the highest sampling rate with low latency. However, its accuracy is low and the area is high.

The SAR and pipeline ADCs are covering the moderate sampling rate and resolution. As explained in section 3.2.1, a 4-bit ADC with maximum sampling rate of 25 MS/s is required. By extrapolating the regions to the lower resolution area and considering their latency and chip area, it can be concluded that a SAR ADC is the most suitable ADC architecture for our receiver front-end.

Table 4.6: Comparison of different ADC architectures [123]

Architecture	**Latency**	**Speed**	**Accuracy**	**Area**
Flash	Low	High	Low	High
SAR	Low	Low-medium	Medium-high	Low
Folding + interpolating	Low	Medium-high	Medium	High
Σ-Δ	High	Low	High	Medium
Pipeline	High	Medium-high	Medium-high	Medium

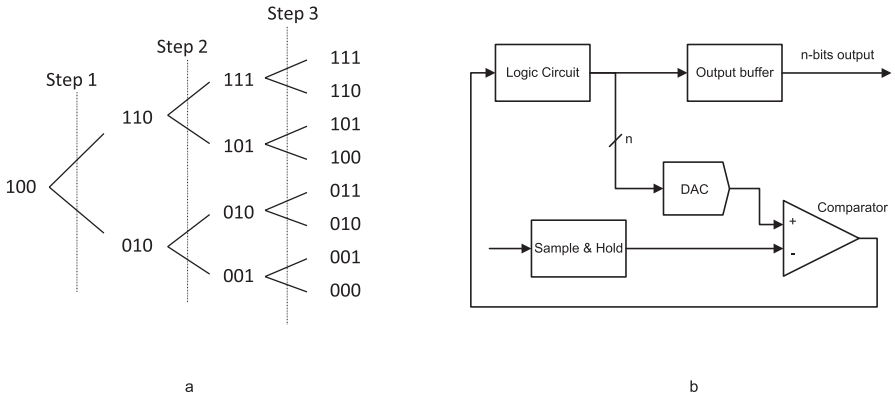


Figure 4.14: a) Binary tree, b) SAR ADC block diagram

4.6.1 Principle of Operation of SAR ADC

The SAR ADC operates based on the binary tree search [124]. A three step binary tree is depicted in Fig. 4.14a. At each step, two branches are generated from each value of the previous step in the search process. At the beginning of the conversion process, the most significant bit (MSB) or bit n of the starting value is set to "1" while the other bits are set to "0". From this starting point two branches are generated. The values of branches differ in the MSB while bit $n-1$ is set to "1" and the rest are set to zero. In the next step, two branches are generated from each value of the previous step. In the values of the new branches with the same root, the bit $n-2$ is set to "1" while the values of bit $n-1$ differ and the rest of the bits remain unchanged. This process continues until all the least significant bits (LSB) are properly set. The number of steps required to complete the binary tree equals to the number of bits.

By using this approach, the digital equivalent of the input signal can be concluded in n steps which is equal to the resolution of the ADC. This means that the output will be ready after n internal operations. Thus, the clock frequency of the SAR ADC should be n times the sampling rate.

The block diagram of the SAR ADC is depicted in Fig. 4.14b. In this configuration, the analog signal is sampled by the sample and hold (SH) block. At the sampling time, the logic circuit is set to the starting value of the binary tree. This value is converted to analog by the digital to analog converter (DAC) block. The output of the DAC is compared with the input signal by the comparator and the comparison result is fed back to the logic circuit. The logic circuit generates the new value of the binary tree for each step taking into account the value in the previous step. This process is repeated n times before the next sampling and the result is stored

in the output buffer.

4.7 Summary

In this chapter, the system level specifications of the receiver front-end has been developed and determined. For each building block of the front-end architecture, different architectures were introduced and the most suitable architecture was selected for each block. Zero-IF is the most suitable architecture for the mixer. Implementing this architecture has two obstacles, i.e. flicker noise and DC-offset. Thus, a novel architecture has been introduced for the mixer which does not suffer from these two problems. A quadrature relaxation oscillator is selected for the local oscillator and SAR ADC is selected to digitize the output. In the next chapter, the detailed design of each block is presented along with simulation results.

5

GPS/Galileo Receiver Front-end Development

The previous chapters covered the principles of GNSS navigation systems and the receiver design. In this chapter, the detailed design of the proposed receiver front-end is presented. In the following, the mixer, IF amplifier, oscillator and ADC blocks of the front-end receiver will be designed and simulated within a frame of the applied design methodologies and tools and conclusions from the design process.

5.1 Design Methodology and Tools

The development process began by defining requirements. For this purpose, in addition to a literature study, several meetings were arranged with potential users to collect their needs. The requirements were generated based on users' input and potentials of the state-of-the-art IC technology. An in-depth study was performed to extract the characteristics of different GNSS systems. Based on this information, during the development process, the entire analytical model of the architecture has been developed which is given in chapters 3 and 4.

The IC development process requires simulation tools in order to verify the design. The design process includes two levels of simulations: system level and detailed design. Two powerful software used for such purpose are MATLAB/Simulink and Cadence/Spectre. MATLAB/Simulink provides a platform to simulate systems

as well as implementing algorithms and solving equations. Cadence/Spectre is a very powerful circuit design tool used for both system level and detailed design. Before using simulation tools for verification, all design parameters are calculated by using the respective equations and then verified by simulation.

The critical block of this front-end is the mixer. Thus, the design procedure starts with verifying the mixer architecture through simulations on system level. For this simulation, the MATLAB/Simulink software is used. The effects of noise and non-linearity are not included in the blocks to clearly demonstrate the functionality of the mixer architecture. However, all these effects are included in the detailed design and thoroughly simulated.

After verification of the mixer functionality, its building blocks, including IF amplifier, will be designed in detail such that its design specifications, provided in Table 4.2, are satisfied. During the detailed design, the MATLAB and Cadence/Spectre software are employed. MATLAB is used for equation solving and Cadence is used for circuit design and simulation. Finally, the ideal blocks are replaced by the designed blocks in Cadence and the complete mixer is simulated and verified by Spectre.

The other front-end blocks in the design sequence are the oscillator and ADC. Since the selected architectures of the oscillator and ADC are already proposed and verified in the literature [119, 125], their design starts directly on transistor level followed by simulation and verification.

It was mentioned in chapter 4 that the standard LNA and AGC solutions are suitable for this architecture. Thus, their designs are excluded from this thesis. The complete layout and chip fabrication was however not possible as part of the thesis due to time and cost constraints.

MATLAB/Simulink

MATLAB is a programming platform with many valuable toolboxes which include predefined functions. Simulink is a part of MATLAB which provides graphical environment to build systems by placing and connecting its building blocks and simulate the system. It is possible to use MATLAB functions within Simulink blocks which provides more flexibility. There are many blocks and functions which are ready to use which increases the design speed.

In this work, the mixer architecture is constructed using building blocks of Simulink and its functionality is simulated and verified. For this purpose, libraries and toolboxes such as Signal Processing Blockset, Simulink Extras, Math Operations, Sources and Sinks were used. The outputs are used in MATLAB for further analysis. Where necessary, MATLAB programs are developed to solve equations which are used to derive design parameters and transistor sizes as well as input-

output relations.

Cadence/Spectre

Cadence is a very powerful circuit design software. It provides a platform to develop a complete electronic system from system level design up to detailed design, including transistor level and IC layout design. Schematics of the circuits are drawn in a graphic environment and parameters of each component are set. The components in the circuit can be ideal, technology dependent or a combination of both. This feature helps to design the circuit first by ideal components and eventually replace them by technology specific components as well as to diagnose abnormal behavior of the circuit.

Spectre is one of the simulation engines of Cadence which is used for simulation. It provides various simulation platforms such as transient, periodic steady state (PSS) and noise analysis.

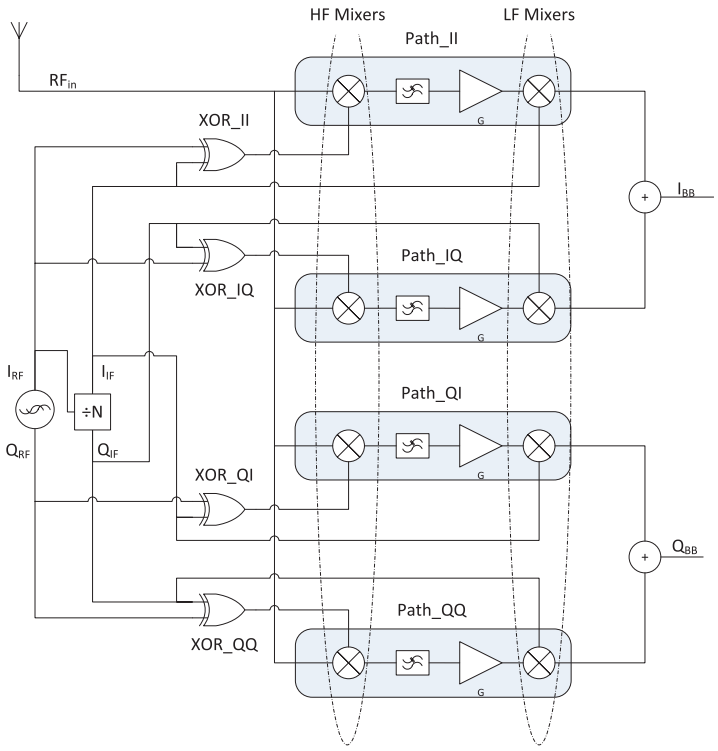


Figure 5.1: Proposed mixer architecture with frequency divider implementation

Table 5.1: Mixer design specifications

Design specification	Target
Noise Figure [dB]	< 10
IIP3 [dBm]	-80
SFDR [dB]	20
Gain [dB]	60
Operation frequency [MHz]	1575.42
Bandwidth [MHz]	24.552
Input power [dBm]	-110
Power consumption [mW]	< 40
Supply voltage [V]	1.2

5.2 Mixer

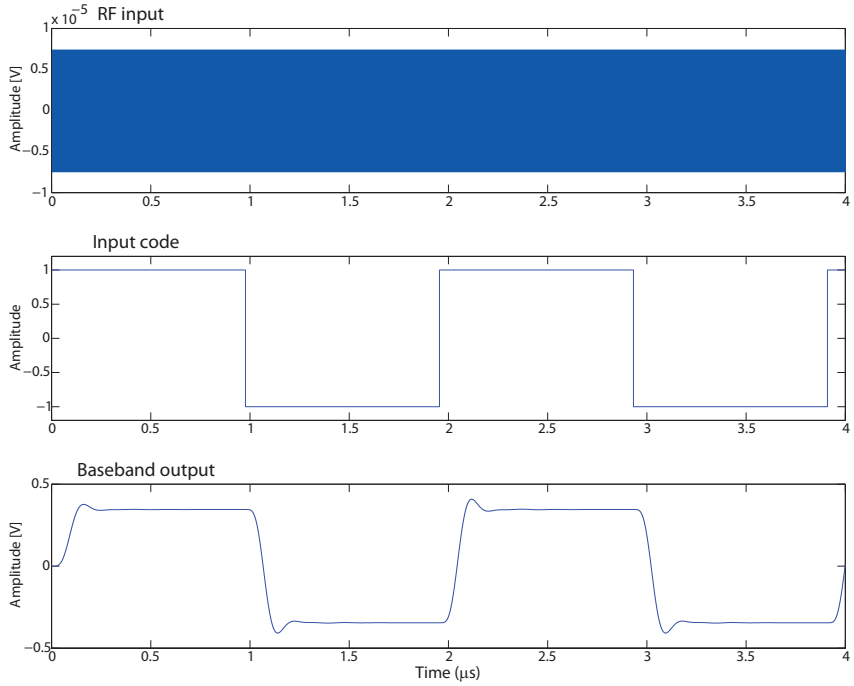


Figure 5.2: System level simulation of the Zero IF mixer. RF input, input code and baseband output is shown on the top, middle and bottom figure.

In section 4.3.2, an innovative mixer architecture for zero-IF receivers has been introduced. In this section, the detailed design of this mixer is provided starting with high level simulations. The high level architecture is depicted in Fig. 5.1. Ta-

ble 5.1 shows the mixer specifications extracted from Table 4.2. In the following sections, the system level simulation followed by detailed design and simulations are presented.

5.2.1 System Level Simulation

In order to validate the architecture depicted in Fig. 5.1, it is simulated in MATLAB. In this simulation, the input is the GPS L1 (carrier + code) signal. The outputs are the I and Q baseband code signals. Fig. 5.2 depicts the outputs when the input signal is in phase with the local oscillator. It can be observed that the transitions in the output data correspond to the code transitions or phase changes in the received signal. The slope and damping oscillations appearing at each data transition is due to the filtering effects of the circuits.

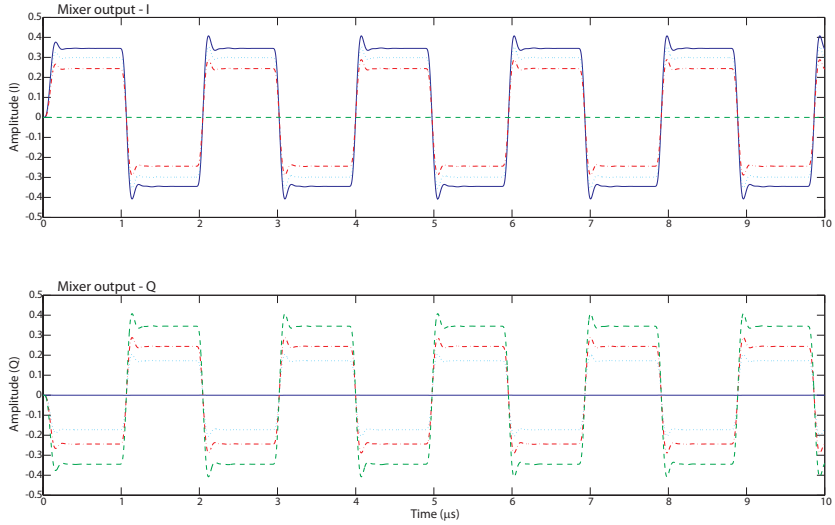


Figure 5.3: Output of the Zero IF mixer at different carrier phases, θ_{RF}. $\theta_{RF} = 0°$ is presented by solid blue line, $\theta_{RF} = 30°$ is shown by dotted cyan line, $\theta_{RF} = 45°$ is presented by dash dotted red line and $\theta_{RF} = 60°$ is shown by dashed green line.

As depicted in Fig. 5.1, this architecture only uses low-pass filters. The IF amplifier has a bandpass behavior. Thus, the low-pass filters can be implemented as a part of the IF amplifiers and no external filtering is necessary to achieve the baseband outputs. Since the IF amplifier acts as a bandpass filter, the cut-off frequency of the high-pass region can be designed to remove the effect of the possible DC offset and flicker noise generated by the HF mixers.

To show that the architecture also provides the information of the carrier phase, θ_{RF}, in the output, the input phase is swept from 0°to 360°. In this simulation the

effect of noise and component mismatch are excluded to focus on carrier phase reconstruction process. Fig. 5.3 depicts four outputs corresponding to input signals with carrier phases of 0°, 30°, 45°and 90°relative to the phase of local oscillator. The amplitudes of in-phase and quadrature-phase baseband signals, I_{BB} and Q_{BB} respectively, depend on the carrier phase considering the local oscillator phase as reference. The variations of these amplitudes follow the relation provided by (3.11) as explained in section 3.1.3. For example, it can be observed form Fig. 5.3 that the amplitude of I_{BB} is maximum and Q_{BB} is zero for $\theta_{RF} = 0$. The amplitude values of the signals in Fig. 5.3 are used to reconstruct the input phase values according to (3.11) and are presented in Table 5.2. The deviation of the reconstructed values in the 4^{th} column from the input phase is due to the computational limitations of the simulator. However, the simulation results enables us to verify that architecture.

Table 5.2: Simulation of carrier phase reconstruction from the baseband output signal using (3.11)

Ideal Carrier phase (θ_{RF})	**Amplitude I**	**Amplitude Q**	$\tan^{-1}(\frac{-Q}{I})$
0°	0.345	1.23×10^{-7}	1.993×10^{-5}°
30°	0.2988	−0.1725	29.998°
45°	0.244	−0.244	45.000°
90°	-1.23×10^{-7}	−0.345	89.999°

5.2.2 Mixer Design Details

As depicted in Fig. 5.1, the mixer contains a number of building blocks which are repeated in the design. These blocks are:

1. HF mixer
2. LF mixer
3. XOR
4. IF amplifier.

In this section, each block is designed and simulated in detail. The complete mixer specifications are summarized in Table 5.1 for reference.

HF Mixer

Since this mixer architecture removes the effect of the flicker noise and DC offset as explained in section 4.3.2, active mixers can be used for HF mixer in order to

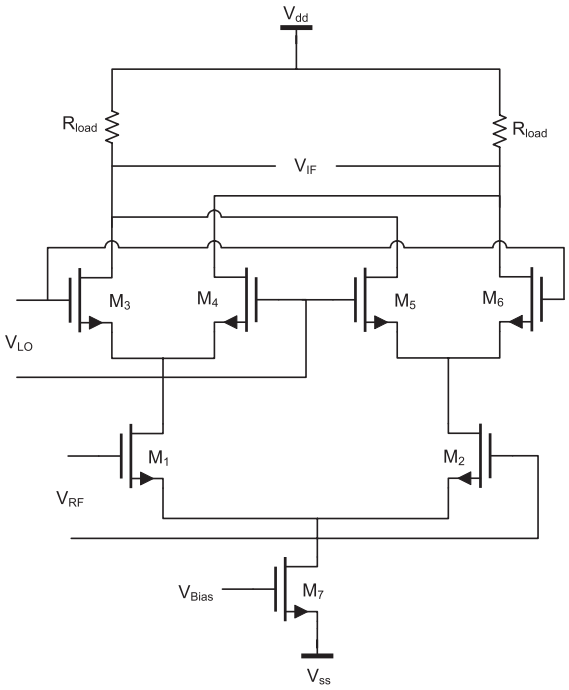


Figure 5.4: The double balanced Gilbert mixer

achieve higher conversion gains. Thus, the HF mixer is designed using the double balanced Gilbert mixer configuration depicted in Fig. 5.4.

The double balanced Gilbert mixer consists of four stages. The first stage is the differential transconductance input. This stage can be distinguished in Fig. 5.4 by M1-M2 transistors. The RF input signal is connected to this stage. The second stage is the switching stage which is formed by M3 to M6 transistors. The local oscillator is connected to this stage. The third and fourth stages are the load and the biasing current source which are shown by R_{load} resistor and M7 transistor respectively. The output is taken differentially from the load resistors.

In the double balanced Gilbert mixer the DC supply, V_{dd}, should be divided between four cascoded stages. These stages are the load resistance, the switching stage, the RF stage and the current source. The transistors must be working in saturation in the Gilbert mixer. Thus, the condition to work in saturation must be satisfied [107].

The single side band (SSB) noise figure of a double balanced Gilbert mixer, ne-

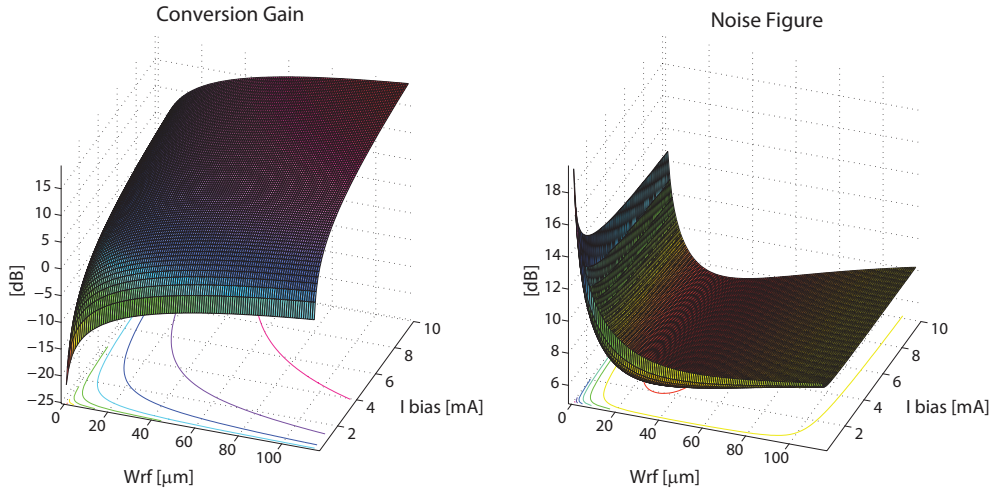


Figure 5.5: Resulting conversion gain from (5.2) (left) and noise figure from (5.1) (right) as a function of biasing current and RF transistor width

glecting the effect of flicker noise, is [107]

$$NF_{(\mathrm{SSB})} = 10\log\left[\frac{\alpha}{c^2} + \frac{2(\gamma_{rf} + r_{\mathrm{g,rf}})\alpha g_{m,rf} + \gamma_{sw}\bar{G} + 4r_{g,sw}\bar{G}^2 + \dfrac{1}{R_L}}{R_S c^2 g_{m,rf}^2}\right] \tag{5.1}$$

where $c(=2/\pi)$ is the conversion gain of the switching stage with square wave input, α is the local oscillator waveform power which is equal to 1 for a square wave signal, γ is equal to 2/3 for long channel transistors and increases for short channel transistors, $r_{\mathrm{g,rf}}$ and $g_{m,rf}$ are the gate resistance and the transconductance of the RF stage transistors respectively, $r_{g,sw}$ is the gate resistance of the switching stage transistors, $\bar{G}$ is the time average of the transconductance of the switching pair and R_S and R_L are the source and load resistances respectively.

If a band-pass filter is used at the input, which filters the out of band noise, then the term α/c^2 in (5.1) becomes one. In case of double side band signal, the noise figure is reduced by 3 dB [107].

Typical conversion gain of a double-balanced Gilbert mixer is around 10 dB [106]. In the double balanced Gilbert mixer the transistors are working in the saturation region. Thus, its conversion gain, CG, and IIP3 can be approximated by [126]

$$CG \approx \frac{2}{\pi} R_L \sqrt{K_n I_{\mathrm{bias}}} \tag{5.2}$$

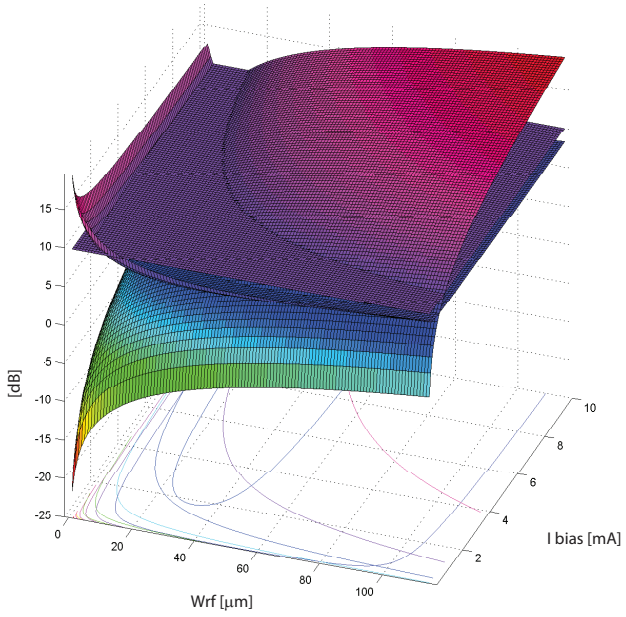


Figure 5.6: Intersecting conversion gain and noise figure with a 10 dB plane

$$IIP3 \approx 4\sqrt{\frac{2}{3}\frac{I_{\text{bias}}}{K_n}} \tag{5.3}$$

$$\text{and} \quad K_n = \frac{W}{L}\mu_n C_{ox}$$

where μ_n is the mobility of the electrons, C_{ox} is the gate oxide capacitance per unit area, W and L are the width and the length of the RF stage transistors respectively, R_L is the load resistance and I_{bias} is the biasing current of the mixer.

The two main design parameters for noise figure and conversion gain as well as linearity are the biasing current, I_{bias}, and the width of the RF stage transistors, W_{rf}. From equations (5.1) to (5.3), it can be concluded that if the biasing current is kept constant then increasing the width of the RF stage transistors increases the conversion gain and reduces the noise figure. However, the drawbacks are the

Table 5.3: Selected parameter values and the resulting noise figure, conversion gain and IIP3 of HF mixer

L	W_{sw}	W_{rf}	R_L	I_{bias}	**NF**	**CG**	**IIP3**
0.12 μm	7.2 μm	57.6 μm	200 Ω	4 mA	6.36 dB	12.16 dB	17.12 dBm

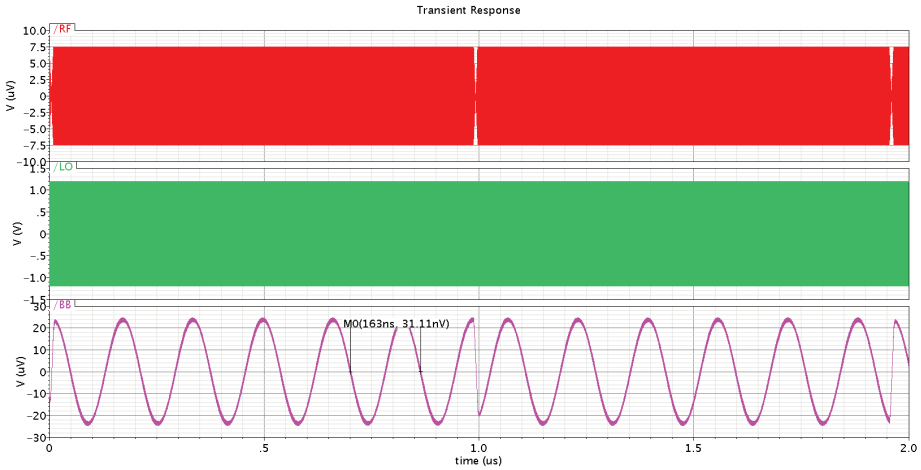


Figure 5.7: Transient response of the HF mixer. The RF input, oscillator signal and the mixer output are shown in top, middle and bottom figures

degradation of the IIP3 and high-frequency response of the RF stage transistors. Increasing the biasing current will improve both gain and linearity. Thus, a balance between these specifications should be achieved which suits the application.

In order to find the proper values of the biasing current and RF transistor width, these two parameters are swept and noise figure, conversion gain and IIP3 are calculated from equations (5.1) to (5.3). The biasing current is varied from 0.1 mA to 10 mA and the transistor width is swept from 1 μm to 115 μm. In this sweep, length of the transistors is kept constant at its minimum value, i.e. L = 0.12 μm, as well as the load resistance, $R_L = 200\ \Omega$, and switching transistor width, $W_{sw} = 7.2\ \mu$m.

Fig. 5.5a and Fig. 5.5b depict the calculated conversion gain and the noise figure respectively. It can be observed in Fig. 5.5a that the conversion gain increases as both biasing current and RF transistor width increase. The noise figure on the other hand, shows another behavior as depicted in Fig. 5.5b. The noise figure decreases by increasing the biasing current. However, by increasing the RF transistor width, the noise figure initially decreases and afterwards increases again. This is due to the fact that $r_{\mathrm{g,rf}}$, $g_{m,rf}$ and $\bar{G}$ depend on W_{rf}. Thus, the RF transistor width shall be selected around the minimum of this curve.

The IIP3 for the sweeping range is always higher than -2 dBm which is far better than what is required in Table 5.1. The noise figure shall be less than 10 dB and the conversion gain shall be larger than 10 dB as defined in Table 5.1. Thus, the two graphs are intersected with a horizontal plane at 10 dB and the acceptable set is extracted. Fig. 5.6 depicts this intersection. The selected parameter values and the resulting noise figure (NF), conversion gain (CG) and IIP3 are given in Table 5.3

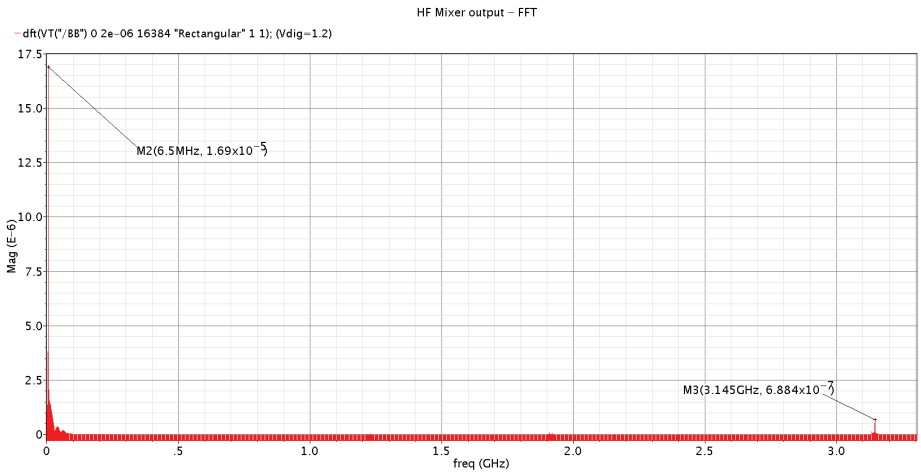


Figure 5.8: Frequency spectrum of the HF mixer output

In order to suppress the high frequency component of the mixer output, i.e. $\omega_{rf}+\omega_{lo}$, a first order low-pass filter is placed at the output. This filter is realized by a capacitor placed in parallel with the load resistance. For GPS L1, considering the local IF frequency at 1.57542 GHz/2^8 = 6.154 MHz, the local oscillator frequency will be 1.569266 GHz. Thus, the high frequency component of the HF mixer output will be centered at 3.144686 GHz. To have a symmetric output, it is important that the capacitors are matched which means the size of the capacitors should be large enough to reduce the mismatch variance, $\sigma^2_{\Delta C/C}$. Thus, the largest unit capacitor in the technology is selected. The value of this unit capacitor is 1.1366 pF. Considering the load resistance, $R_L = 200\ \Omega$, the cut-off frequency will be 4.4 GHz which is too high. Thus, 10 capacitors are placed in parallel to reduce the cut-off frequency by a factor of 10. The mismatch variance will be less than 0.01% [127] and the cut-off frequency of the resulting low-pass filter is 440 MHz which reduces the high frequency component by 14 dB.

The HF mixer performance is simulated in Cadence to verify the compliance of the HF mixer with the design specifications. The simulation results are given in the following.

Since this mixer is designed for a GPS/Galileo receiver, the applied input signal in the simulation is designed to have a behavior as close to the PRN modulated carrier of the GPS/Galileo signal as possible. Thus, a sine wave carrier modulated by a square wave is applied to the input. The carrier frequency is 1.57542 GHz (GPS L1/Galileo E1) and the frequency of the square wave is 511.5 kHz (corresponding to the chipping rate of the C/A code, i.e. 1.023 MHz).

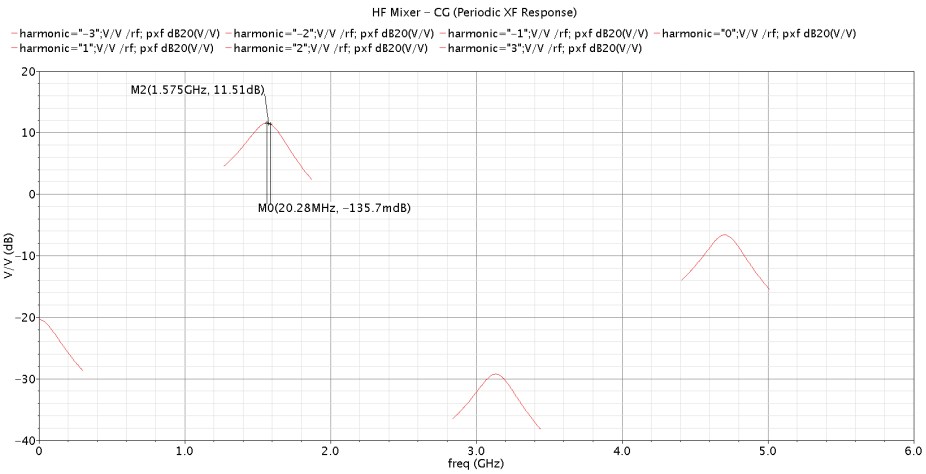


Figure 5.9: Conversion gain of the HF mixer

In order to make the simulation more efficient, especially for periodic steady state simulations, the internal IF frequency is selected to be 6 times the chipping rate, i.e. 6.138 MHz, which is very close to the selected internal IF frequency as was discussed in the beginning of this section, i.e. 6.154 MHz. In this case, the 1st harmonic will be 2.046 MHz.

The received signal has been amplified and filtered by the LNA and bandpass filter before arriving to the mixer. Thus, for the input signal of the HF mixer in the transient simulation, a voltage source with a peak amplitude of 7.5 μV is placed which is the equivalence of the signal at the mixer input considering a 50 Ω matching impedance.

The transient response of the HF mixer is depicted in Fig. 5.7. The upper signal is the modulated RF input. The transition of the PRN code in the RF signal can be detected easily due to the rise and fall time of the code. The signal in the middle is the oscillator signal. The mixer performance is improved by using a square wave oscillator [126]. Thus, a square wave oscillator signal is used. The signal shown at the bottom of the figure is the output of the HF mixer. It can be observed that the frequency is 6.138 MHz and the PRN transition occurs at the same position as in the RF signal. The high frequency component of the output is also filtered.

Fig. 5.8 depicts the fast Fourier transform of the output signal. The peak amplitude of the IF output signal is 23.88 μV (16.9 μV_{rms}). Thus the conversion gain based on transition analysis is $20\log(23.88\mu V/7.5\mu V)$ = 10.06 dB. This value is lower than calculation result provided in Table 5.3 since (5.2) is an approximation. However, it meets the requirement of CG $\geq$ 10 dB. As will be shown later it

is in agreement with the conversion gain value based on the periodic steady state simulation. The amplitude of the high frequency component is 973 nV (688 nV_{rms}) which is 27.8 dB lower than the IF frequency component. Fig. 5.9 depicts the conversion gain of the HF mixer determined by periodic steady state analysis.

Fig. 5.9 depicts the conversion gain of the HF mixer. From Fig. 5.9, it can be observed that the conversion gain of frequencies around 1.57542 GHz is 11.5 dB and is relatively constant within the 20 MHz bandwidth. The conversion gains of other frequencies are considerably lower.

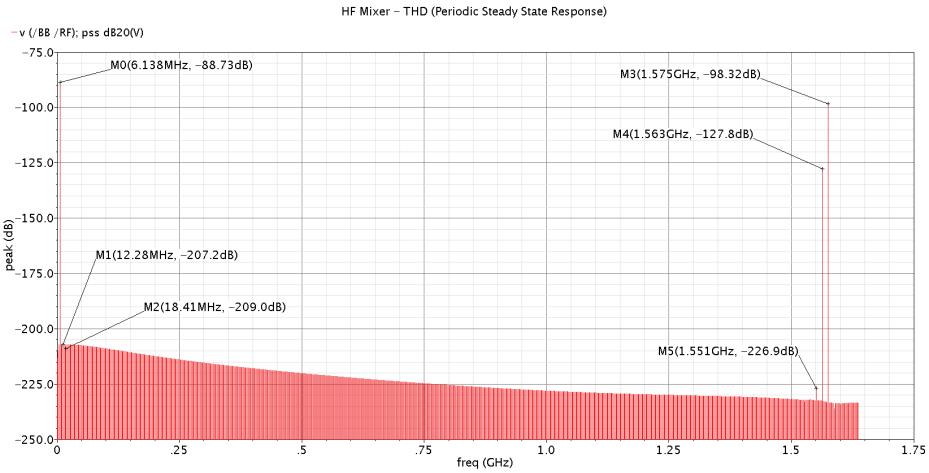


Figure 5.10: Harmonic distortion of the HF Mixer

The total harmonic distortion (THD) is defined as the ratio of the sum of the powers of higher harmonics (usually the 2^{nd} and 3^{rd} harmonics) to the power of the fundamental frequency at the output and can be calculated by [128]

$$THD = 10\log\left(\frac{h_2^2 + h_3^2}{h_1^2}\right) \tag{5.4}$$

where h_1 is the amplitude of the fundamental frequency of the output and h_2 and h_3 are the amplitudes of the 2^{nd} and 3^{rd} harmonics at the output. Fig. 5.10 depicts the simulated harmonics of the HF mixer. The THD is -116.27 dB which is calculated from the values shown in this figure.

The noise figure of the HF mixer is depicted in Fig. 5.11. The noise figure at L1 frequency is 3.5 dB. The noise figure is less than 10 dB from 175.4 kHz up to 4.367 GHz. The noise figure of the complete mixer is determined mainly by the first stage which is the HF mixer. Since the total noise figure must be less than 10 dB, this mixer is well within the specifications for the complete signal band. As can be observed, the flicker noise is dominant for frequencies less than 175.4 kHz.

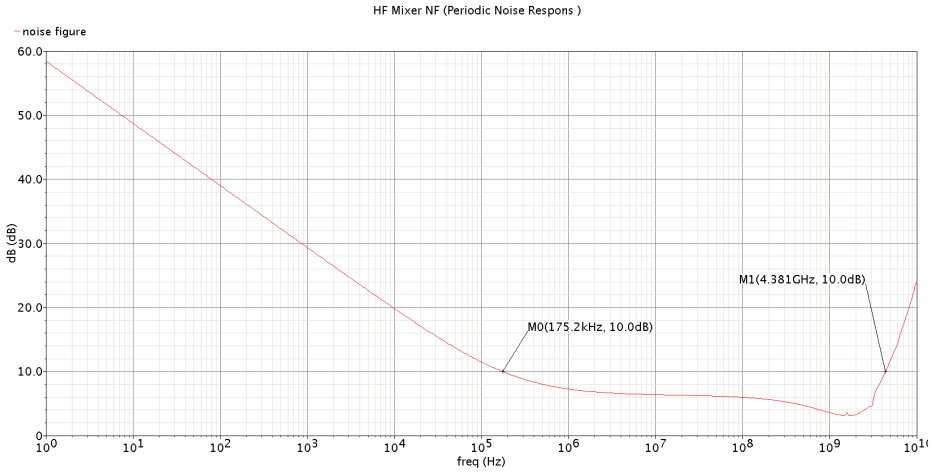


Figure 5.11: Noise figure of the HF Mixer

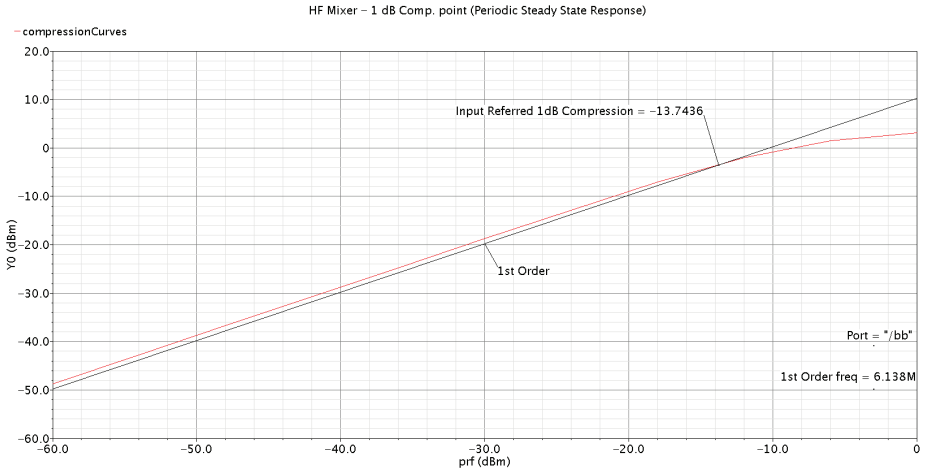


Figure 5.12: 1-dB compression point of HF Mixer

Fig. 5.12 depicts the input referred 1-dB compression point of the HF mixer. In order to determine the 1-dB compression point, the input power is swept while the input frequency is set to the center frequency and the input-output relation is calculated. The relation is linear with a slope of one. At certain input power, the output starts to deviate from the linear pattern and the gain drops. The 1-dB compression point is where the deviation in the gain reaches 1 dB. This point for the designed circuit is at -13.6684 dBm.

The 3rd order intercept point (IP3) is where the effect of the third harmonic be-

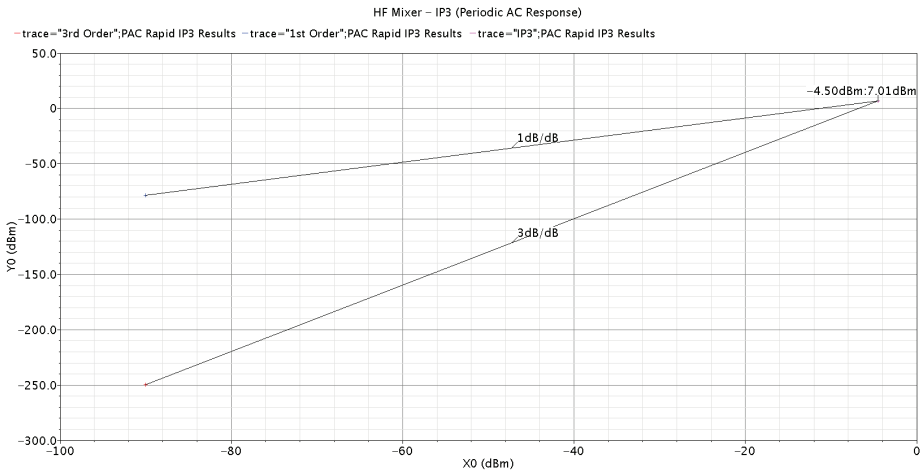


Figure 5.13: 3rd order intercept point of the HF mixer

comes dominant in the output. For the IP3 simulation, the input source generates a two-tone signal. It consists of two signals with the same power but with two different frequencies. One frequency is the same as the frequency of the received signal. The other frequency is selected such that the down-conversion of its 3rd order intermodulation with the first frequency falls within the output frequency band. The 3rd order intermodulation frequency, f_{IM3}, can be determined by

$$\begin{aligned} f_{\text{IM3}} &= 2f_1 - f_2, \text{ or} \\ f_{\text{IM3}} &= 2f_2 - f_1 \end{aligned} \tag{5.5}$$

where f_1 and f_2 are the two input frequency tones. Applying these two frequencies at the input, the output is calculated by sweeping the power of the two-tone input. The input-output relation for f_1 is linear as expected. The other input-output relation belongs to the response to the f_{IM3}. The slope of the linear section of this response is 3. Both responses are drawn in a graph and the linear sections are extrapolated until they intersect. The intersection is the IP3 point.

For this simulation, $f_1 = 1.57542$ GHz and $f_2 = f_1 + 20.46$ MHz are selected. Thus, $f_{\text{IM3}} = 14.322$ MHz which is inside the IF band. Based on these frequencies, the IP3 of the HF mixer is simulated and the result is depicted in Fig. 5.13. The value of the input referred IP3 (IIP3) is -4.50 dBm. This value is lower than calculation result provided in Table 5.3 since (5.3) is an approximation.

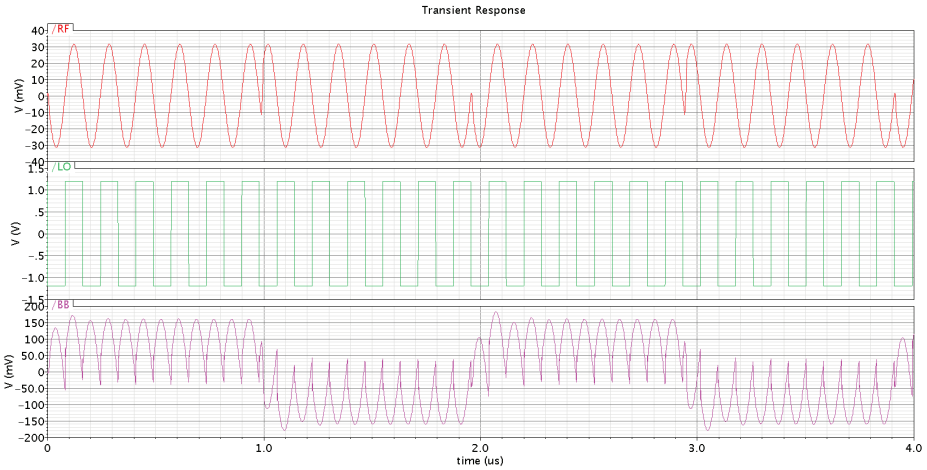


Figure 5.14: Transient response of the LF mixer

LF Mixer

The LF mixer down-converts the internal IF signal to baseband. The output of the LF mixer is summed up with another LF mixer output as explained in section 4.3.2. This operation is performed by current addition. To use current addition, two LF mixers, e.g. in Path_II and Path_IQ, share their loads. In this way their outputs are connected in parallel resulting in output current addition. It is possible to use the same transistor sizes as for the HF mixers. Since the noise of the LF mixer is not critical, its biasing current can be reduced. In this design, the LF mixer is biased with 150 μA which results in an NF of about 20 dB as will be shown later in this section.

The IF frequency is 6.154 MHz. Thus, the LF oscillator frequency must be the same. Since the simulator uses the common divisors of the input frequencies for simulation, it is best to select the input frequencies such that their greatest common divisor (GCM) is at least as high as the smallest input frequency. In this way, the common divisor can be adjusted for different simulation resolutions easily. Thus, for simulating the LF mixer circuit, the input is modulated with 511.5 kHz square wave in order to simulate the C/A code (1.023 MHz chipping rate) and the IF frequency is selected to be the closest integer multiple of 1.023 MHz to 6.154 MHz, i.e. 6.138 MHz, which results to GCM of IF frequency and RF frequency of 2.046 MHz which is twice the smallest input frequency.

The transient response is depicted in Fig. 5.14. In this figure, the output is not filtered and the high frequency component is present. As discussed in section 4.3.2, the outputs of the LF mixer of path_II and Path_IQ are added in order to eliminate

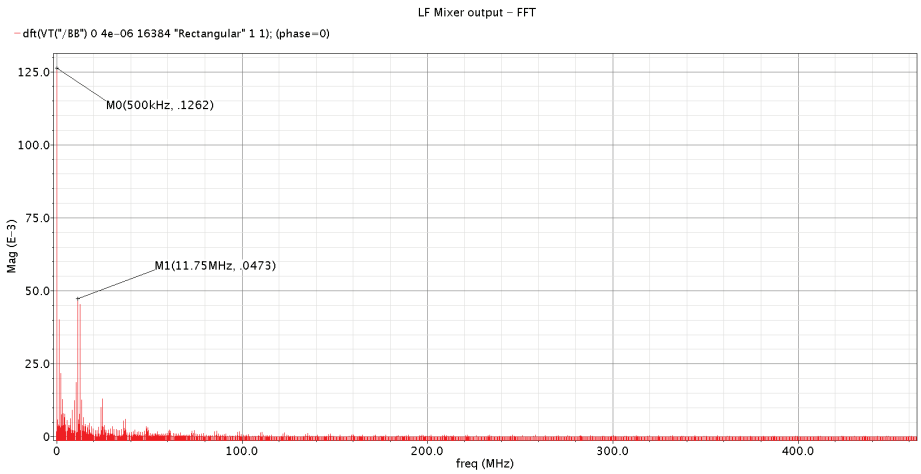


Figure 5.15: Frequency spectrum of the LF mixer output

the high frequency component. The Fourier transform of the output signal is depicted in Fig. 5.15. It can be observed that the 500 kHz frequency component has the highest amplitude. The second highest frequency component in amplitude belongs to the twice the oscillator frequency. This term will be eliminated during the signal summation.

The conversion gain of the LF mixer is depicted in Fig. 5.16. The conversion gain is calculated for a bandwidth of 2 MHz. The peak value is 16.32 dB at 6.138 MHz. It reduces to 15.15 dB at the lower frequency corner of the bandwidth.

The noise figure of the LF mixer is depicted in Fig. 5.17. The minimum noise figure is 22.1 dB. The noise figure is less than 25 dB from 834.7 kHz up to 2.951 MHz. The flicker noise is dominant for frequencies less than 834.7 kHz. The maximum noise figure of the LF mixer is at 6.138 MHz due to up-conversion of the flicker noise. This value is 49.37 dB. However, due to the high gain of the previous stages (the HF mixer and IF amplifier), such a high noise figure value has very limited effect on the total NF of the complete mixer structure.

Fig. 5.18 depicts the input referred 1-dB compression point of the LF mixer. The gain of the circuit behaves linearly for low input powers and compresses for 1 dB at the input power of -18.0712 dBm after which the gain is saturating. The input signal of the LF mixer, after amplification by the previous stages, has a value of -30 dBm which leaves about 12 dBm headroom for possible input variations.

For simulating IP3, a two tone signal with frequencies f_1 = 6.238 MHz and f_2 = 6.638 MHz is used. Thus, f_{IM3} = 300 kHz which is inside the baseband. Based on these frequencies, the IP3 of the LF mixer is simulated and the result is depicted in

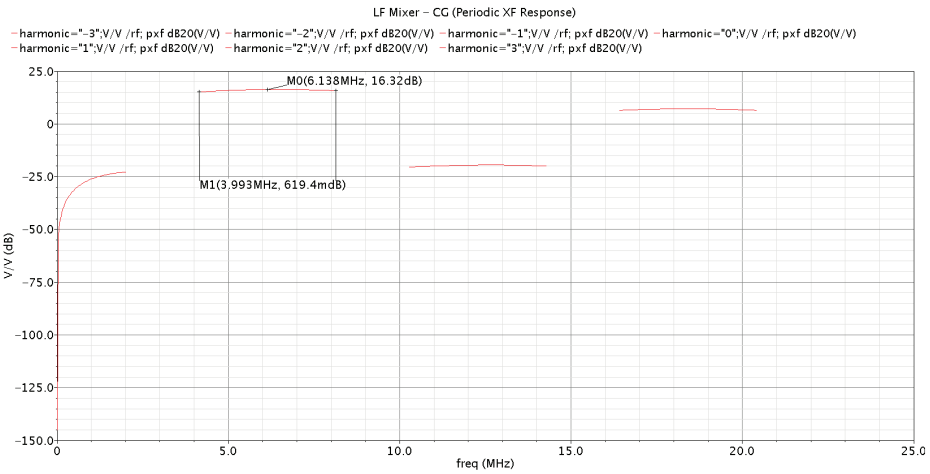


Figure 5.16: Conversion gain of the LF mixer

Fig. 5.19. The value of the input referred IP3 (IIP3) is -6.24 dBm.

The 2nd order intercept point (IP2) is where the effect of the second harmonic becomes dominant in the output. As explained in section 3.1.3, the 2nd harmonic becomes important in zero-IF mixer. Thus, IP2 is also studied for the LF mixer to ensure its correct performance. In IP2 simulation, a two-tone signal is used. One signal has the same frequency as the input signal and the other frequency is selected in such a way that the down-conversion of its 2nd order intermodulation with the first frequency falls within the output frequency band. The 2nd order intermodulation frequency, f_{IM2}, is determined by

$$f_{IM2} = |f_1 - f_2| \tag{5.6}$$

where f_1 and f_2 are the two input frequency tones. Applying these two frequencies at the input, the output is calculated by sweeping the power of the two-tone input. The input-output relation for f_1 is linear as expected. The other input-output relation belongs to the response to the f_{IM2}. The slope of the linear section of this response is 2. Both responses are drawn in a graph and the linear sections are extrapolated until they intersect. The intersection is the IP2 point.

For this simulation, f_1 = 6.238 MHz and f_2 = 6.638 MHz are selected. Thus, f_{IM2} = 400 kHz which is inside the baseband. Based on these frequencies, the IP2 of the HF mixer is simulated and the result is depicted in Fig. 5.20. The value of the input referred IP2 (IIP2) is 96.37 dBm.

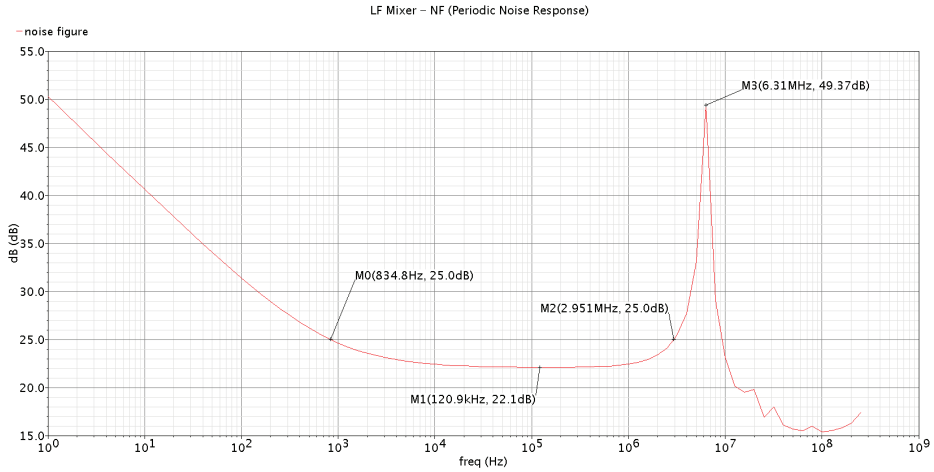


Figure 5.17: Noise figure of the LF Mixer

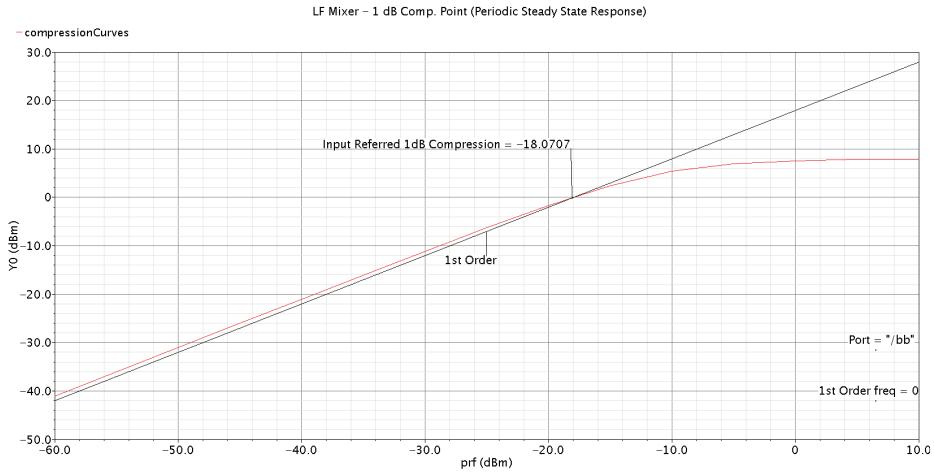


Figure 5.18: 1-dB compression point of LF Mixer

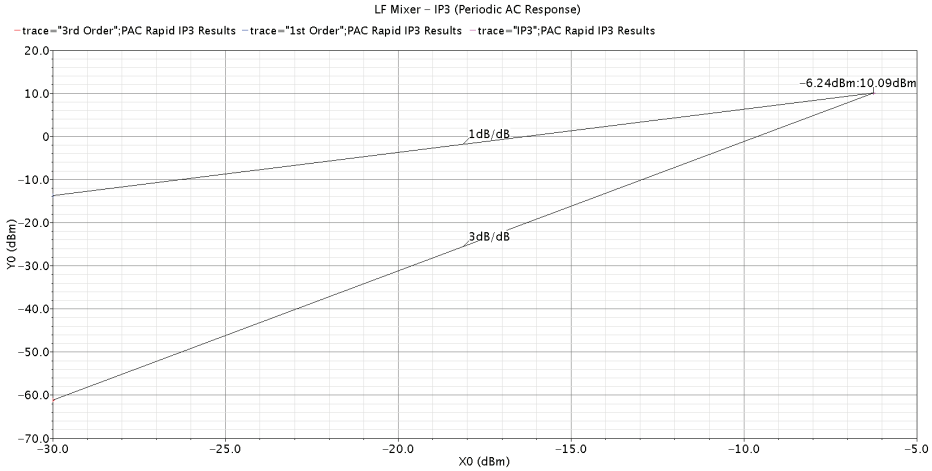


Figure 5.19: 3rd order intercept point of the HF mixer

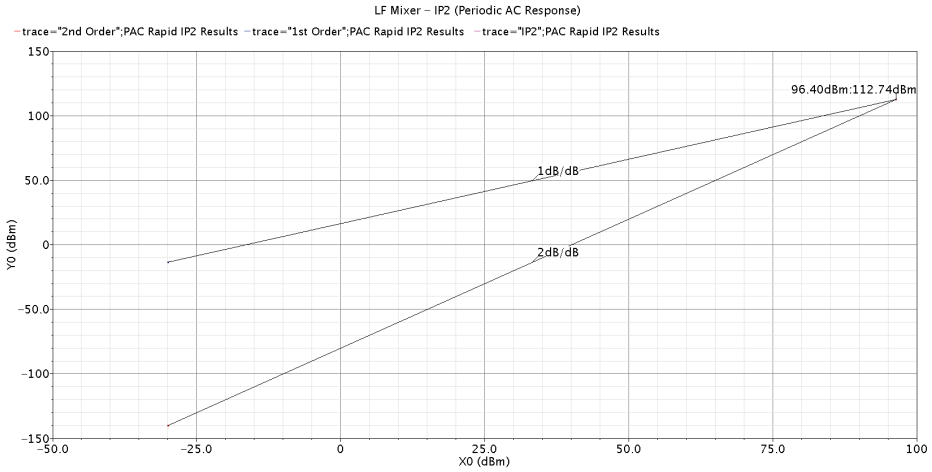


Figure 5.20: 2nd order intercept point of the LF mixer

XOR

As explained in section 4.3.2, the third mixer in this architecture, which multiplies the two oscillator signals, can be implemented by an XOR gate. Since the oscillator outputs are square waves, logic gates can be used to simplify the design. The logic gates can be implemented either by current mode logic (CML) circuits or regular CMOS logic circuits. The CML circuits work with differential signals which is suitable for operation in noisy environments and prevents generating digital switching noise [129]. However, they consist of more transistors compared to CMOS logic and their power consumption is static. Thus, the average power consumption of CML circuits compared to CMOS logic circuits becomes considerably higher, especially, when the frequency is variable in the circuit, e.g. in frequency dividers which will be discussed later in section 5.3. Thus, CMOS logic circuits are used in this design.

Fig. 5.21 depicts a CMOS XOR logic circuit. In order to achieve uniformity in the design, all combinational logic circuits are implemented by NAND-NAND stages. The transistor implementation of an inverter and NAND gate are depicted in Fig. 5.22a and Fig. 5.22b respectively. As shown in Fig. 5.22, NAND gate and inverter comprise of NMOS and PMOS transistors. The NMOS and PMOS transistors should have similar switching speed to give symmetric outputs during rise and fall transitions. Thus, the size of the NMOS transistors should be the smallest size, i.e. W = 0.16 μm and L = 0.12 μm, to gain the maximum speed. Achieving the same transition speed for PMOS transistors means that they have the same threshold voltage and react similar to NMOS transistors. This condition can be expressed by

$$\mu_n C_{ox}\left(\frac{W}{L}\right)_n = \mu_p C_{ox}\left(\frac{W}{L}\right)_p \tag{5.7}$$

where $\mu_{n,p}$ are mobilities of electrons/holes, C_{ox} is the gate oxide capacitance per unit area and $(W/L)_{n,p}$ are the aspect ratio of NMOS/PMOS. The length of the transistors should be minimum to achieve the highest f_T. Since the mobility of the electrons is almost 3 times the mobility of the holes, the width of the PMOS transistors shall be selected to be 3 times the width of NMOS transistors in order to achieve the same speed. Thus, the PMOS size will be W = 0.48 μm and L = 0.12 μm.

The output of each XOR should drive the HF mixers. Thus, the load of the XOR is the gate-source capacitance, C_{gs}, of the switching transistors. From the BSIM3 model of CMOS transistors, C_{gs} is determined by [130]

$$C_{gs} = C_{ox} W L \times \frac{2}{3}\frac{1+2\alpha}{(1+\alpha)^2} \tag{5.8}$$

where α is the saturation index which is zero when drain-source voltage, V_{DS}, exceeds its value at saturation, $V_{DS,\text{sat}}$, i.e., $V_{DS} \geq V_{DS,\text{sat}}$. Considering the arrange-

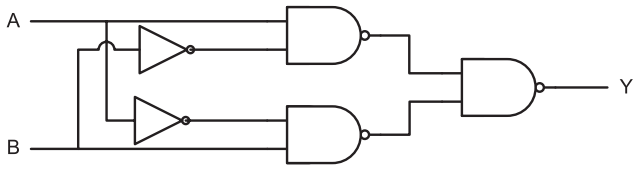


Figure 5.21: Logic implementation of an XOR circuit

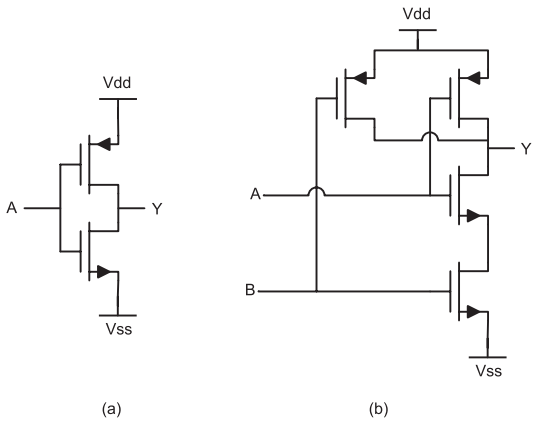


Figure 5.22: Transistor level implementation of a) inverter b) NAND gate

ment of the switching transistors in a double balanced Gilbert mixer, the equivalent load capacitance will be C_{gs}. Based on transistor sizings of the HF mixer, the output load is 10.9 fF. The output of the XOR should be able to drive this capacitor. The current required to charge/discharge this capacitor is determined by the required rise and fall time of the switching signal which itself is defined by the frequency of this signal.

Considering the size of the switching transistors of the HF mixers and the fact that their inputs should be differential, a buffer stage is required to supply the required current to drive the switching mixers and convert the signal to differential. This is done by the single to differential converter (S2D) circuit depicted in Fig. 5.23 which also acts as the buffer.

The S2D block is designed using regular CMOS inverters. The input is buffered by two inverters in series. The buffered input is inverted once more to generate the complementary output. Ideally the rising and falling edges of a square wave signal is desired to be as steep as possible. However, the S2D should be able to drive the HF and LF mixer inputs which have capacitive input impedances.

In digital circuits, when the output of the circuit can not drive the input of the

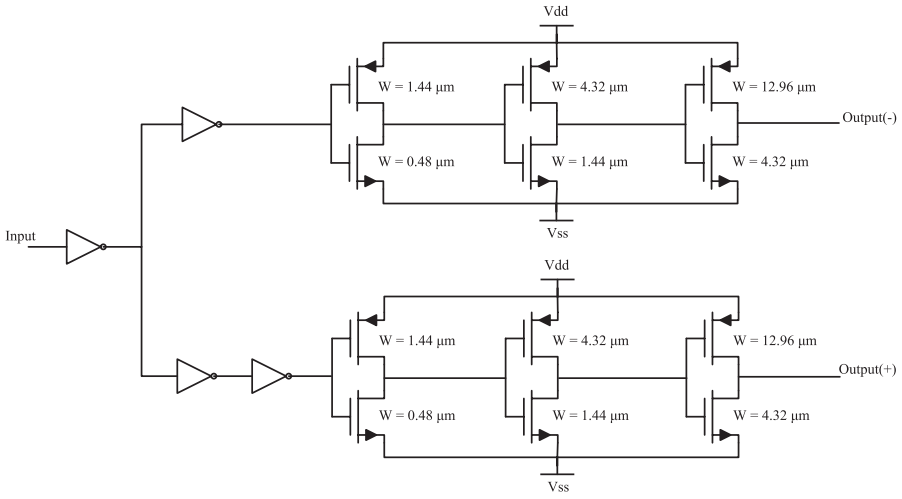


Figure 5.23: Single to differential converter

next stage, a buffer is used. This buffer can be implemented by cascading inverters. In this case the W/L ratios of transistors are increased by taper factor, β. If N is the number of inverter stages then the optimum number of stages and optimum β can be determined by [131]

$$\begin{aligned} N_{\text{opt}} &= \ln\left(\frac{C_L}{C_0}\right) \\ \beta_{\text{opt}} &= \left(\frac{C_L}{C_0}\right)^{[1/\ln(C_L/C_0)]} \end{aligned} \tag{5.9}$$

where C_0 is the input capacitance of the minimum size transistor and C_L is the load capacitance. The buffer is driving the HF and LF mixers. Thus, the load capacitance is the C_{gs} of the switching stage transistors of the mixers which is equal to 10.9 fF. The C_{gs} of the smallest transistor is 0.162 fF. Thus, using (5.9) results to N = 3 and $\beta \approx 3$.

IF Amplifier

The mixer includes an amplifier to amplify the internal IF signal. The behavior of the amplifier should preserve the characteristics of the desired signal. Prior to the amplifier, the signal has been amplified by the LNA and down-converted to IF and amplified by the HF mixer. The output of the HF mixer is fed to the IF amplifier. This signal contains both the IF and remaining of the high frequency components resulting from mixing procedure. Thus, the high frequency part should be

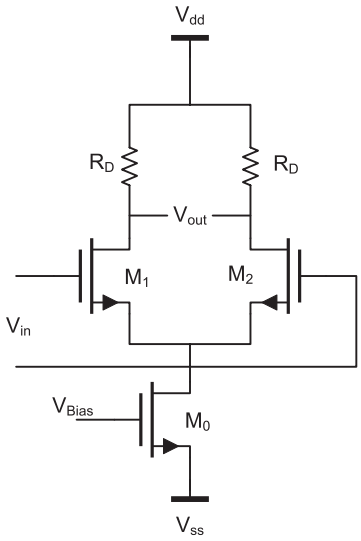


Figure 5.24: Differential amplifier with resistive load

removed and the IF part should be amplified. The effect of the flicker noise and the DC offset of the LF mixer will decrease as the gain of the IF amplifier increases. The suppression of the possible existing flicker noise and DC offset at the input should also be included. Thus, the IF amplifier shall show a bandpass behavior.

The noise behavior of the IF amplifier is important. Because of the structure of the mixer, the generated flicker noise will be up converted to higher frequencies by the LF mixer. Thus, flicker noise will not be included in the SNR calculations of the IF amplifier.

In order to design an amplifier, it is important to have the proper topology. Both the HF mixer output and the LF mixer input are differential voltages. Thus, a voltage to voltage topology needs to be considered for the IF amplifier.

In section 4.5, the structure of the feedback amplifier was discussed. In order to have a negative feedback amplifier, the loop gain should be very high which means that the forward gain, A, must be very high based on the condition leading to (4.19). Thus, if a very high forward gain can not be achieved then an open loop amplifier with limited gain A must be used. In this case the gain is not determined by the accurate feedback but by the active components.

The frequency compensation of amplifiers with more than three stages becomes too complicated since the number of poles in the frequency response of the amplifier increases with the number of stages [122]. If the gain of the forward path with three stages is not high enough to implement the feedback amplifier then two or more double stage amplifiers in cascade could be used. In this case, the amplifiers

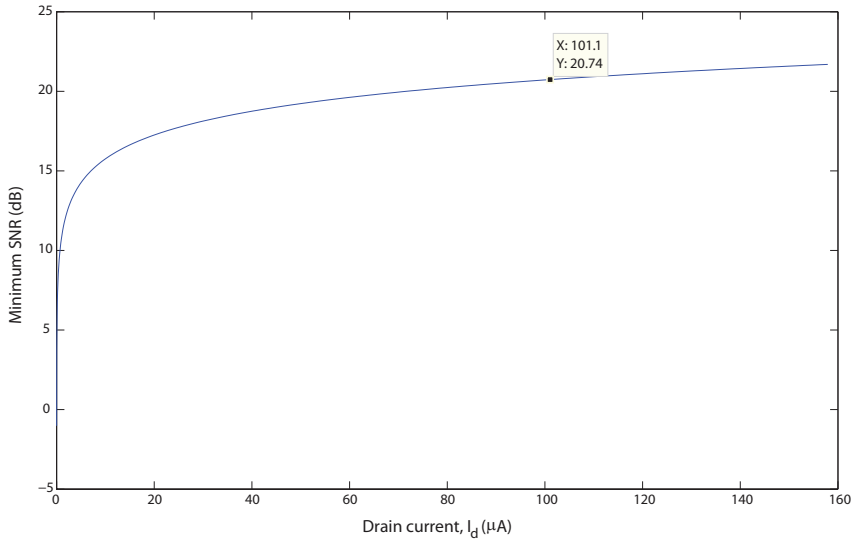


Figure 5.25: SNR of a differential pair in different biasing currents for $W = 200$ μm and $L = 0.12$ μm

are connected using coupling capacitors. In this way, the frequency behavior of each amplifier can be analyzed independently.

The design parameters of a CMOS transistor are its gate width, W, gate length, L, and gate-source voltage, V_{GS}, which is determined by its biasing current, I_D. These parameters determine the behavior of the transistor for certain technology. The transconductance of an NMOS transistor is expressed by [121]

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th}) \tag{5.10}$$

where μ_n is the mobility of the electrons, C_{ox} is the gate oxide capacitance per unit area and V_{th} is the threshold voltage of the transistor.

The amplifier load can be either active or passive. If the amplifier is implemented by NMOS transistors then the active load comprises of two PMOS transistor connected in a current mirror structure. The advantage of this approach is less area occupation. However, it requires complementary circuits for each stage to keep the loads symmetric which increases the complexity of the circuit. The passive load is usually a resistor which requires no extra circuitry. Thus, resistive load is selected for the differential pair in order to have accurate gain and reduce the complexity and sensitivity of the amplifier. Fig. 5.24 depicts a single stage differential amplifier. The input and output voltages are shown by V_{in} and V_{out} respectively. The differential amplifier includes a current source to provide the biasing current. This current source is implemented by the transistor M0. The transistors

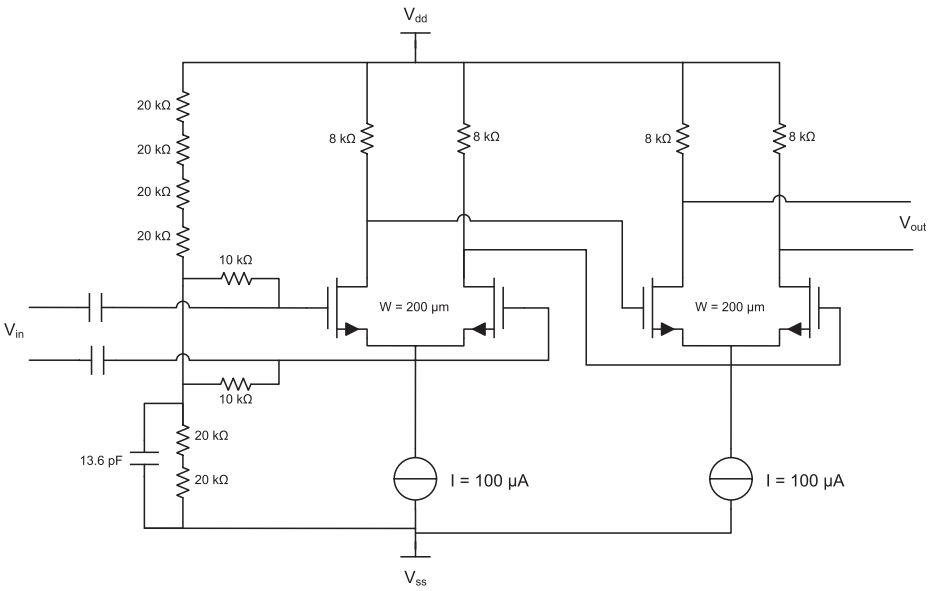


Figure 5.26: Designed differential amplifier

M1 and M2 form the differential pair. For correct operation of the differential amplifier, the transistors must be biased correctly. For NMOS transistors to operate in the saturation region, the condition

$$V_{DS} > V_{GS} - V_{th} \tag{5.11}$$

shall be satisfied. By selecting $V_{DS} \approx V_{th}$ it is assured that condition is satisfied even with variations in V_{GS}. Selecting the overhead voltage of transistors to be 200 mV, will leave 800 mV for the load resistance. Thus, the load resistance will be

$$R_D = \frac{0.8}{I_D} \ [\Omega]. \tag{5.12}$$

The mismatch of the two input transistors in the differential pair shall be taken into account during the transistor sizing. Any difference in the threshold voltages causes DC offset at the input which will be amplified and may saturate the output. The variance of the mismatch of the threshold voltage of two CMOS transistors,$\sigma^2_{V_{th}}$, is inversely proportional to the area of the transistors [132]. Considering the conversion gains of the HF and LF mixers, the gain of the IF amplifier shall be 32 dB to achieve the overall 60 dB mixer gain. Since the voltage across the load resistance is designed to be 800 mV, input offset of 22.2 mV will saturate the output. In order to prevent saturation due to mismatch, the maximum tolerable input DC offset is selected to be 50% of this value or 11 mV. To ensure that

the probability of the DC offset caused by the mismatch being less than 11 mV is higher that 96.6%, the transistor sizes should be selected such that $3\sigma_{V_{th}} < 11$ mV. From the UMC technology data sheet, in order to satisfy this condition with the smallest gate length, i.e. $L = 0.12$ μm, the transistor width must be at least 200 μm. Thus, $W = 200$ μm is selected.

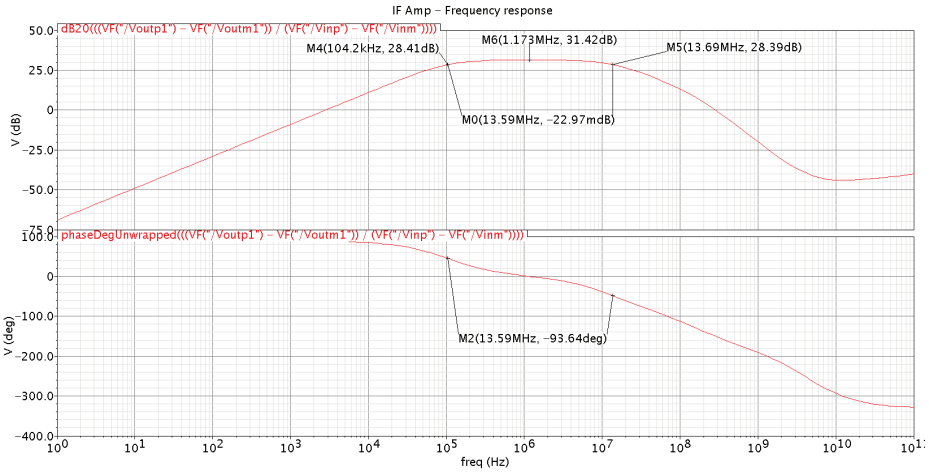


Figure 5.27: Frequency response of a single IF amplifier

The biasing current of the first stage can be determined by the SNR of the amplifier since the noise of the amplifier is mainly determined by its first stage. The input voltage of the amplifier which has been amplified by the LNA and the HF mixer, is about 6.3 μV based on the nominal received power of the GPS/Galileo signal. From the requirements of the mixer, in order to reduce the effect of the amplifier noise, the SNR shall be at least 20 dB. The voltage input noise equivalent of a CMOS differential pair, $\overline{v_n^2}$, can be calculated by [121]

$$\overline{v_n^2} = 8kT\left(\frac{2}{3g_m} + \frac{1}{g_m^2 R_D}\right)B \tag{5.13}$$

where k is the Boltzmann constant, T is the operating absolute temperature and B is the signal bandwidth. Fig. 5.25 depicts the SNR of the differential stage for different drain currents for 20 MHz signal bandwidth. It can be observed that for drain currents higher than 71 μA, the SNR is higher than 20 dB. Thus, $I_D = 100$ μA is selected which corresponds to a SNR = 20.74 dB to allow 30% error margin in biasing current. The SNR will be 10 dB higher for 2 MHz bandwidth signal (e.g. C/A code).

Based on this drain current value and (5.12), the load resistor value will be 8 kΩ. Considering the requirements for matching, the minimum width of a resistor for

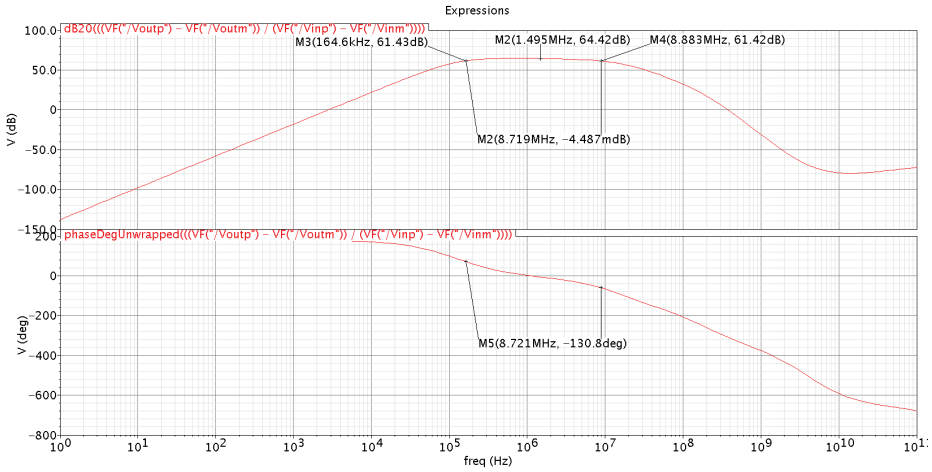


Figure 5.28: Total frequency response of two cascaded IF amplifiers

precise matching shall be at least 200% of the minimum width of the resistors in the technology. In any case, the width shall not be less than 1 μm [132]. Thus, based on thes conditions and the minimum width of the resistors in this technology, the dimensions of the load resistor will be 8.02 μm by 1 μm from the technology data sheet [133].

The gain of the differential pair, A_{diff}, with a resistive load R_D as depicted in Fig. 5.24, is determined by [121]

$$A_{\text{diff}} = g_m R_D. \tag{5.14}$$

which leads to $A_{\text{diff}} \approx 6$ for the designed differential pair. Thus, the required high gain to use a feedback structure is only achieved by adding more than 3 stages. Since its frequency compensation would be impractical, a cascade of two double stage open loop amplifiers will be used instead.

Fig. 5.26 depicts the designed amplifier circuit. In this circuit, the biasing resistors are formed using an even number of unit resistors. The unit resistors are 1 μm by 14.26 μm in order to achieve better matching. The gate biasing circuit is implemented by a resistive divider to provide the correct gate voltage of the differential pair. Since the gate of the NMOS transistor draws no current at steady state, the divider output is connected to both gates with two 10 kΩ resistors. In this way, area is saved by using only one divider. The connecting resistors are high enough not to cause leakage between two inputs. The IF amplifier input is isolated from the previous blocks by a pair of coupling capacitors. The output of the voltage divider is connected to ground by a 13.6 pF capacitor to protect the biasing from transient high frequency disturbances by forming a low-pass filter with 300 kHz corner fre-

quency.

The frequency response of the IF amplifier is shown in Fig. 5.27. The bandwidth of this amplifier is 13.65 MHz and the gain is 31.41 dB. This is sufficient to meet the link budget. However, it is possible to increase the gain of the IF amplifier by adding one more stage in cascade to further reduce the effect of flicker noise and DC offset of the LF mixer. Thus, two amplifiers are placed in cascade. The band-pass behavior of the amplifier ensures that the flicker noise of the previous stage is attenuated. In addition, possible DC offset generated in the HF mixer will not affect the signal path. The total frequency response of the cascade amplifiers is depicted in Fig. 5.28. The total gain is 64.42 dB with the bandwidth of 8.72 MHz. The gain satisfies the gain requirements and the bandwidth satisfies the requirements for GPS C/A code and Galileo E1 OS code.

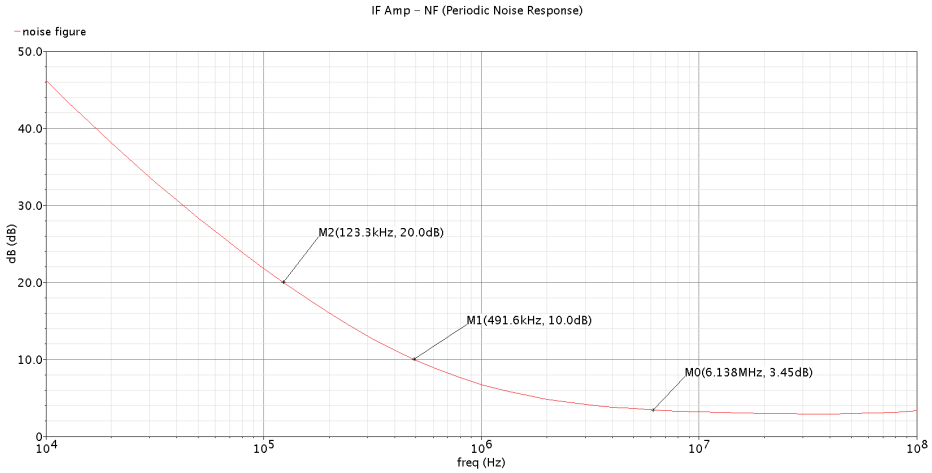


Figure 5.29: Noise figure of the IF amplifier

The noise figure of the IF amplifier is depicted in Fig. 5.29. The noise figure is 3.45 dB at 6.138 MHz and is less than 10 dB from 491.5 kHz. The flicker noise is dominant for frequencies less than 491.5 kHz which is out of the signal band.

Fig. 5.30 depicts the 1-dB compression point of the IF amplifier. The 1-dB compression point is -71.71 dBm. The input signal of the IF amplifier is expected to have a value of -100 dBm which leaves about 28 dBm headroom for possible input variations.

For simulating IP3, $f_1 = 6.138$ MHz and $f_2 = 7.161$ MHz are selected. Thus, from (5.5), $f_{IM3} = 5.115$ MHz which is inside the IF band. Based on these frequencies, the IP3 of the IF amplifier is simulated and the result is depicted in Fig. 5.31. The value of the input referred IP3 (IIP3) is -61.68 dBm.

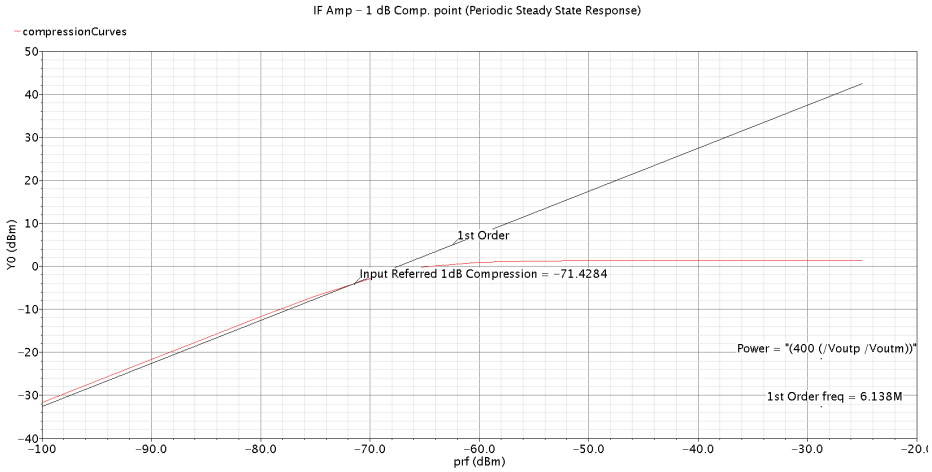


Figure 5.30: 1-dB compression point of IF amplifier

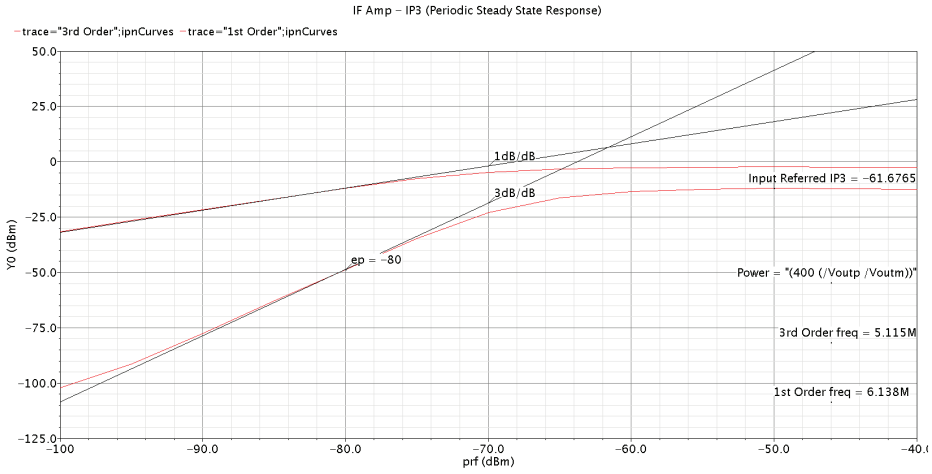


Figure 5.31: 3rd order intercept point of the IF amplifier

Complete Mixer Performance

In this section the building blocks of the mixer architecture have been designed and individually verified. In the following, the complete mixer is simulated and the performance is verified.

The mixer consists of 3 main blocks (HF mixer, IF amplifier and LF mixer) placed in cascade. The total noise figure of the mixer can be calculated by

$$NF = 10\log\left(F_{HF} + \frac{F_{IF}-1}{G_{HF}} + \frac{F_{LF}-1}{G_{HF}G_{IF}}\right) \tag{5.15}$$

where F_{HF}, F_{IF} and F_{LF} are the noise factors of the HF mixer, IF amplifier and the LF mixer respectively and G_{HF} and G_{IF} are the conversion gain of the HF mixer and the gain of the IF amplifier respectively. It can be concluded that the effect of the noise figure of the HF mixer on the total noise figure is the highest and the effect of the noise figure of the LF mixer is the lowest. Considering the noise figure values of the 3 blocks that were extracted from the simulation results, the total noise figure of the mixer is 3.66 dB. A clear advantage of this architecture is that because of the very high gain of the IF amplifier, the total noise figure value increases only to 3.67 dB when the noise figure of the LF mixer goes as high as 50 dB due to the flicker noise.

The total IIP3 of the mixer, $IIP3_{\text{total}}$, is determined by the IIP3 of each block and can be calculated by

$$\frac{1}{IIP3_{\text{total}}} = \frac{1}{IIP3_{HF}} + \frac{G_{HF}}{IIP3_{IF}} + \frac{G_{HF}G_{IF}}{IIP3_{LF}} \tag{5.16}$$

where $IIP3_{HF}$, $IIP3_{IF}$ and $IIP3_{LF}$ are the IIP3 of the HF mixer, IF amplifier and the LF mixer respectively. Thus, the total IIP3 of the mixer is -83 dBm.

The transient response of the mixer is depicted in Fig. 5.32. In this part of the simulation, the input voltage source is the GPS L1 carrier + C/A code with an amplitude of 7.5 μV. The local oscillator signal is a square wave at 1.57542 GHz in-phase with the input carrier. The figure on the right depicts the transient response of the mixer. The in-phase and quadrature outputs are named "VbbOutI" and "VbbOutQ" respectively. This output includes no extra filtering. The high frequency component which is present in the output is due to the different transistor speeds in the adder circuit. Because of this difference in speed, the addition is not performed simultaneously thus, resulting to this high frequency component at the output. Another effect which is observed is that the quadrature output is not zero as expected. This is due to the delay which is generated in the buffer of S2D block. Since this is a systematic phase shift, it can be determined and included in the algorithm during the calibration process. The zero crossing of both I and Q output signals occur at 1.033 μs which shows a delay of 55.4 ns compared to the C/A code

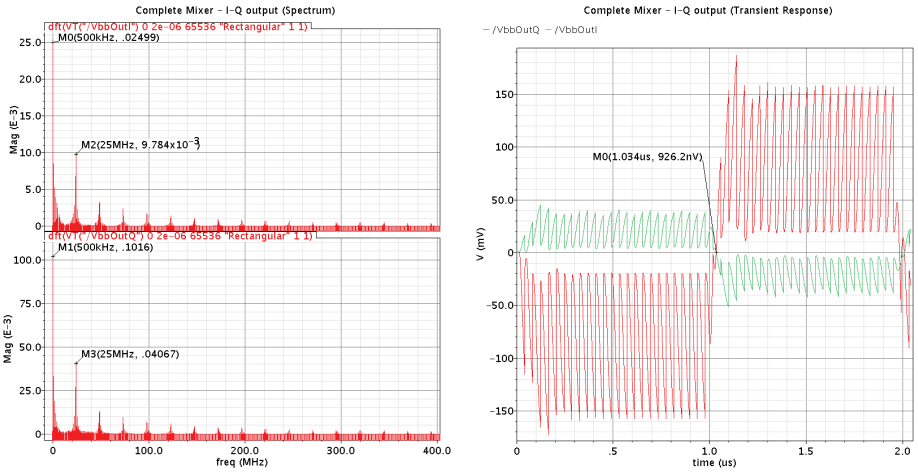


Figure 5.32: Frequency spectrum (left) and the transient response (right) of the output of the complete mixer

chip length which is due to initial transition. The code length in the rest of the simulation equals to the code chip length, i.e. 977.5 μs.

The left figure in Fig. 5.32, depicts the Fourier transform of the output signals. The amplitude of the output signal of each output at 500 Hz (rounded by the simulator) is the amplitude of the in-phase and quadrature code signals which are 102.6 mV and 21.45 mV respectively as depicted in this figure. Thus, the systematic phase error can be determined by (3.11) and equals to 11.81°. The high frequency component visible in the output is at 25 MHz which corresponds to four times the IF frequency, i.e. 6.154 MHz (rounded by simulator). This is in agreement with the fact that the summation interval is every quarter of the IF frequency due to the four oscillator signals and four paths that are defined in the architecture. Since the maximum baseband signal bandwidth is 12.276 MHz, this component will be filtered in the baseband amplifier and has no effect on the desired signal.

The total conversion gain of the mixer is 92.54 dB by which only about 10 dB is required for the gain of baseband amplifier and AGC. Thus, the baseband amplifier can be omitted and only the AGC be used. The very high gain of this mixer assures that the noise of the AGC has no influence on the overall noise behavior of the receiver. Based on the simulation results, the total average power consumption of the complete mixer is about 34 mW.

Table 5.4 summarizes the target design specifications of the mixer and what has been achieved. It can be concluded that all target specifications are met except for the bandwidth. This is due to the bandwidth of the IF amplifier. However, the achieved bandwidth satisfies the requirement for processing GPS L1 C/A and

Table 5.4: Comparison of target and achieved mixer design specifications

Design specification	**Target**	**Achieved**
Noise Figure [dB]	< 10	3.66
IIP3 [dBm]	-80	-83
SFDR [dB]	20	22.2
Gain [dB]	60	92.54
Operation frequency [MHz]	1575.42	1575.42
Bandwidth [MHz]	24.552	12.276
Input power [dBm]	-110	-110
Power consumption [mW]	< 40	34
Supply voltage [V]	1.2	1.2

Galileo E1 OS. To be able to comply with requirement NAV-FE-01, the bandwidth shall be increased to at least 25 MHz.

The total conversion gain of the mixer is 92.54 dB which is 32.54 dB higher that the target. This gain is achieved by cascading two IF amplifiers. As mentioned previously, using only one IF amplifier would also satisfy the gain requirement. However, the effect of the flicker noise and DC offset of the LF mixer will be increased. Thus, two IF amplifier stages are selected.

5.3 Oscillator

In this architecture, two oscillators are required for the complete operation: a high frequency (HF) and a low frequency (LF) oscillator. As explained in section 4.3.2, the LF oscillator can be implemented by using a frequency divider to divide the frequency of the HF oscillator. In this way, the LF oscillator follows the frequency variations of the HF oscillator and the final result is independent of these variations. Thus, in this section an HF oscillator and a divider is designed to generate the required signals.

Based on the conclusions of section 4.4, a cross coupled relaxation oscillator is selected for this design. Fig. 5.33 depicts the circuit of the designed relaxation oscillator.

As discussed in section 4.4, the relaxation oscillator operates based on the charging and discharging the timing capacitor. Based on (4.16), the oscillating frequency is inversely proportional to the timing capacitor value and maximum voltage swing across it and is proportional to the biasing current. For oscillation frequency of 1.57542 GHz, e.g. L1, considering $V_{\max} = 400$ mV, the values of the biasing current and timing capacitor will be $I_0 = 3.15$ mA and $C = 1.25$ pF.

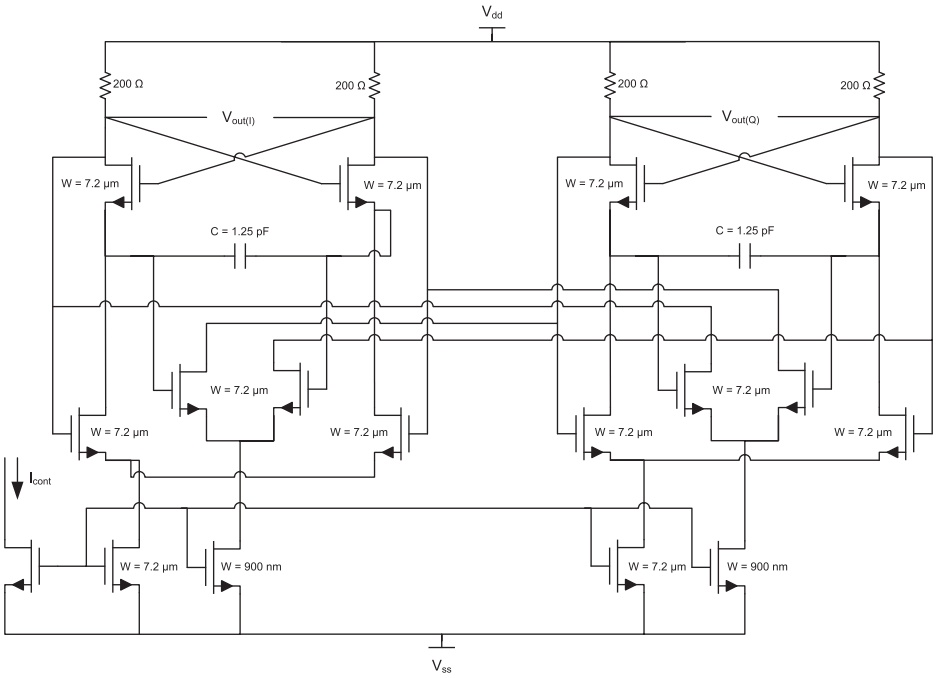


Figure 5.33: Quadrature relaxation oscillator circuit

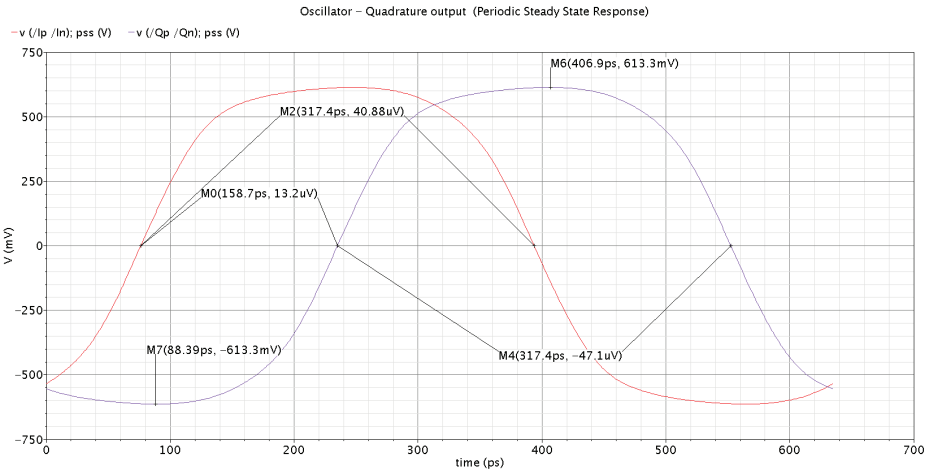


Figure 5.34: Designed oscillator output signals

The transistor sizes shall be small enough that it does not influence the value of the timing transistors while their matching conditions are also satisfied. The total

combinations of the capacitors of the core transistors in parallel with the timing capacitor equals to $C_{gs}/2$. Thus, the condition $C_{gs} < 100C$ is considered for the sizing. Since the length of the transistors are kept at its minimum value to gain the maximum f_T, the design parameter is the width of the transistors based on (5.8). The selected width of the four core oscillator transistors is W = 7.2 μm. The standard deviation of the threshold voltages will be $\sigma_{V_{th}}$ = 5.57 mV. Similarly the coupling transistors are also selected to have the same size.

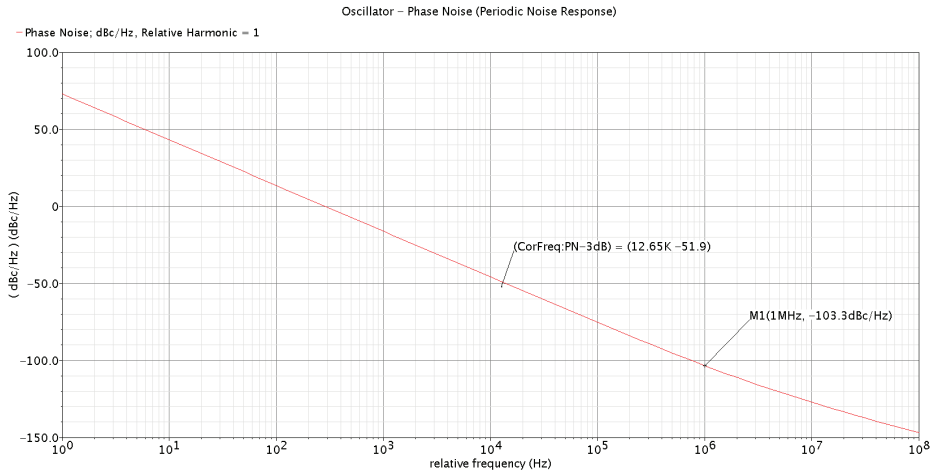


Figure 5.35: Phase noise of the designed oscillator

Fig. 5.34 depicts the in-phase (I) and quadrature (Q) output signals of the designed oscillator. The period of both signals are 634.8 ps which correspond to 1.5753 GHz. The time delay between I and Q signals is 158.7 ps which corresponds to 90°phase shift and their peak amplitudes are 611.2 mV. Fig. 5.35 depicts the phase noise of the oscillator. The phase noise is -103.3 dBc/Hz at 1 MHz.

As depicted in Fig. 5.36, the frequency can be controlled by the control current in the range of 1.41 GHz to 1.68 GHz. The control voltage varies between 400 mV and 470 mV. This control voltage can be implemented by a current mirror to linearly control the frequency. The total average power consumption of the oscillator is about 10 mW.

A frequency divider is a circuit which divides its input frequency by a predetermined number. The simplest approach is to divide the input frequency by powers of 2. In order to do so, T-type flip flops (T-FF) are used. A T-FF is formed when the complementary output of a D-flip flop (D-FF) is connected to its input. In this way, the output of the circuit is toggled at each clock pulse. Thus, connecting the input signal to the clock of the T-FF will generate a signal with half the frequency

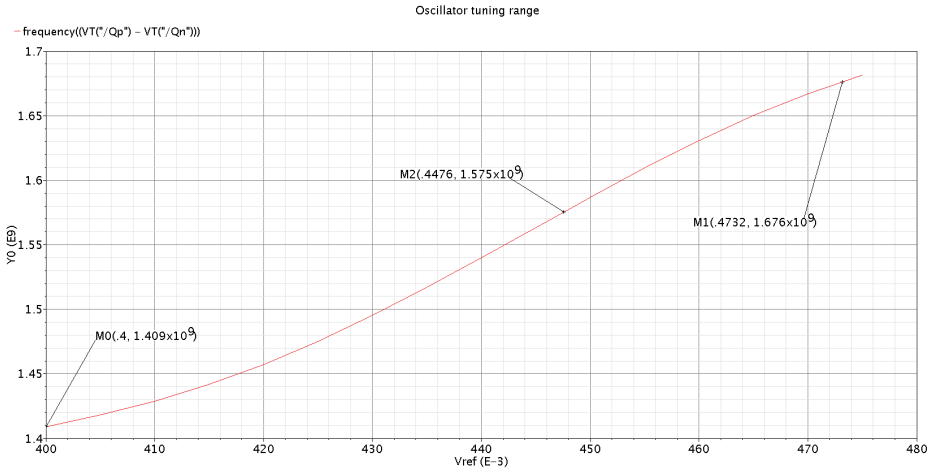


Figure 5.36: Tuning frequency range of the designed oscillator

at the output. In order to generate the oscillator signal for the LF mixer, 8 T-FFs are connected such that the output of each stage is connected to the clock of the next. In this way the input frequency can be divided by 2^8. The input of the divider is taken from the in-phase output of the HF oscillator. To generate the quadrature LF output, the 8^{th} stage includes two T-FFs. One receives the output of the 7^{th} stage directly at its clock input to generate in-phase signal. The other one receives the complementary output of the 7^{th} stage. The quadrature signal is taken from the latter. The divider circuit and the I and Q output signals are depicted in Fig. 5.37 and Fig. 5.38 respectively.

The mixers operate with differential signals and the HF oscillator generates dif-

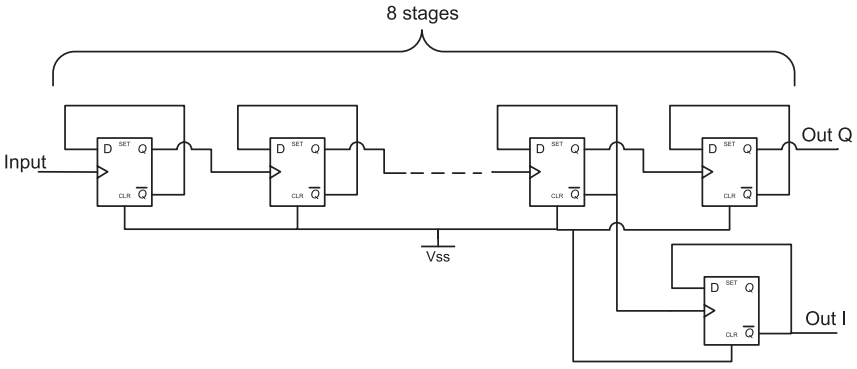


Figure 5.37: 2^8 I-Q frequency divider circuit

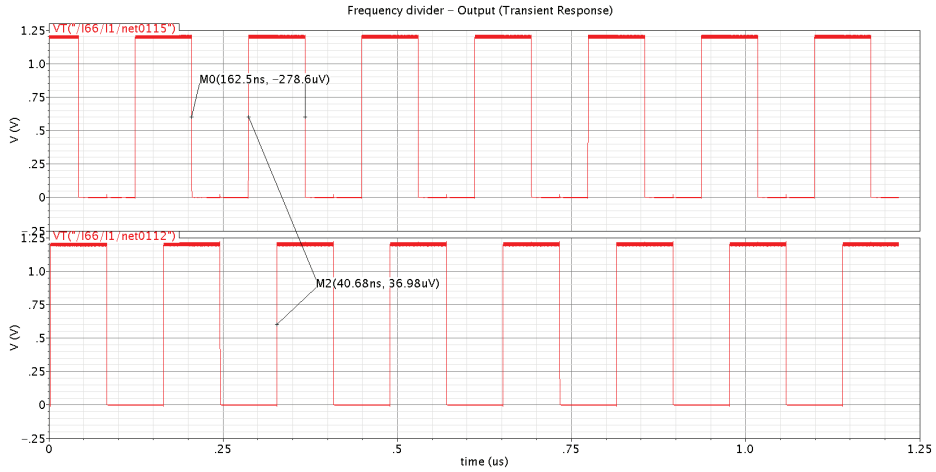


Figure 5.38: I output (top) and Q output (bottom) of the 2^8 I-Q frequency divider

ferential outputs. To design the divider, there are two approaches; one is using only differential circuits, i.e. incorporating CML and the other is using regular CMOS logic circuits with conversions from differential to single-ended signals at the input and single-ended to differential at the output.

The dynamic power consumption of the regular CMOS logic circuits increases with frequency. Thus, for the circuits operating at very high frequencies, it is reasonable to use CML circuits since the power consumption is static, i.e. independent of the operating frequency. However, in the divider circuit the operating frequency of the circuit reduces after each stage which results in the reduction of the dynamic power consumption. Thus, the total power consumption of the divider is less when using regular CMOS logic.

On the other hand, the CML requires larger transistors than regular CMOS logic to ensure that the matching requirements are met. Considering the above mentioned arguments, a regular CMOS logic divider is used in this design. In this configuration, the input of the divider is single-ended while the output of the oscillator is differential. Thus, the divider requires a differential to single conversion. This is achieved by using a comparator. The differential output of the oscillator is connected to the inputs of the comparator. The comparator output is used in the rest of the divider circuit. The details of the comparator design is given in section 5.4.2. The comparator is designed to be sensitive to very low voltage differences (> 10 mV). Thus, the oscillator does not require to be rail-to-rail and a wide range of oscillator outputs can be applied which gives a flexibility in the design, e.g. to apply an external highly accurate oscillator.

Table 5.5: Comparison of target and achieved oscillator design specifications

Design specification	Target	Achieved
Phase noise [dBc/Hz @1MHz]	-110	-103.3
Operation frequency [MHz]	1575.42	1575.42
Power consumption [mW]	< 10	10
Supply voltage [V]	1.2	1.2

The divider itself is designed based on regular CMOS logic circuit. The transistor lengths are 0.12 μm. The width of NMOS transistors are 0.16 μm and the width of the PMOS transistors are 0.48 μm which is 3 times the width of the NMOS transistors to achieve the same speed due to mobility differences of the majority carriers as explained in section 5.2.2.

As it was explained previously in section 4.3.2, one mixer is implemented by an XOR. Considering that the XOR is also implemented by regular CMOS logic, the comparator output can be sent to both XOR and divider. The other input of the XOR is connected to the output of the divider.

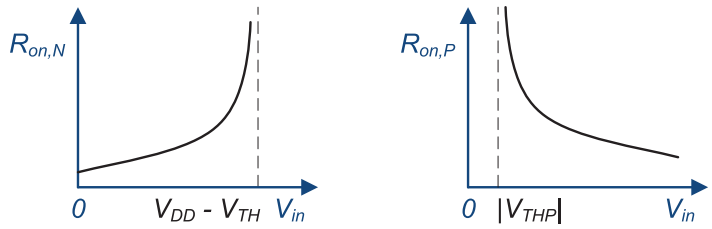
The output of the XOR goes to the HF mixer and the output of the divider is the low frequency oscillator signal which should be connected to the LF mixer. Thus, the XOR and divider outputs must be converted to differential. This step is done by single to differential (S2D) converter as discussed in section 5.2.2.

Table 5.5 summarizes the target design specifications of the oscillator and what has been achieved. The oscillation frequency is achieved. The phase noise is close to the target value. The phase noise can be reduced further by increasing the soft-limiting coupling currents [120].

5.4 ADC Design Details

The final stage of the front-end is the ADC. Based on the conclusions in section 4.6, the suitable ADC type for this application is the SAR ADC. As depicted in Fig. 4.14, the SAR ADC consists of a sample and hold, DAC, comparator, logic circuit and an output buffer. The design details of each block are given in this section.

Table 5.6 summarizes the specifications of the ADC as determined in section 4.6. The full range of the ADC shall be 150 mV with 4 bits resolution. This leads to an LSB of 9.4 mV. Thus, the designed minimum input range shall be 4 mV which is less than half the LSB. The maximum input signal bandwidth shall be 12.276 MHz. Considering the Nyquist criteria, the sampling rate shall be higher than 24.552 MHz. Thus, sampling frequency of 25 MHz is selected.



(a) (b)

Figure 5.39: On resistance of a) NMOS and b) PMOS devices as a function of input voltage

5.4.1 Sample and Hold

The ADC requires some time to converge to the solution. During this period its input shall be kept constant. Thus, the input signal is sampled and stored during the converging time.

The sample and hold circuit consists of a sampling switch and a hold circuit. The hold circuit is represented by its output behavior which is described by a polynomial function [134]. The order of this polynomial function is the order of the hold circuit. For this application, a zero order hold (ZOH) circuit is suitable since the sampled value must not change. The ZOH circuit is implemented by a switch and a capacitor. The switch connects the input of the sample and hold circuit to the output and the capacitor is connected between the output and ground (V_{ss}). The value of this capacitor must be such that the voltage drop level of the capacitor is less than (1/2 LSB) during the ADC operation.

The switch can be implemented by CMOS transistors. When a CMOS transistor is off it acts as an open circuit. If the CMOS transistor is working in the deep triode region, i.e. $V_{DS} \ll 2(V_{GS} - V_{th})$, then it can operate as a voltage controlled resistor. The resistor connecting its source and drain, $R_{on,N}$, is controlled by the

Table 5.6: List of ADC requirements

Requirement	**Value**
Full range [mV]	150
Resolution [bits]	4
Minimum input voltage (V_{min}) [mV]	4 ($< \frac{1}{2}$ LSB)
Input signal bandwidth [MHz]	12.276

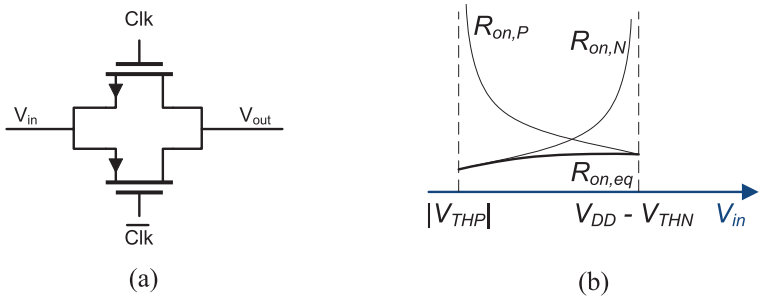


Figure 5.40: Complementary switch or transmission gate (TG) (a) on-resistance of the TG (b)

gate-source voltage, V_{GS}. For an NMOS, R_{on} can be calculated by [121]

$$R_{on,N} = \frac{1}{\mu_n C_{ox}(W/L)(V_{GS} - V_{th})}. \tag{5.17}$$

In the sample and hold circuit, the input voltage is stored in the capacitor. Using a CMOS transistor in the deep triode region produces a very low voltage drop due to its low on-resistance. However, as can be concluded from (5.17), the on-resistance is dependent on V_{GS} and since V_G is either V_{dd} or V_{ss} for NMOS and PMOS transistors respectively, the on-resistance depends on the source voltage which is the input voltage, V_{in}. Fig. 5.39 depicts the dependence of R_{on} to the V_{in} for NMOS and PMOS transistors. This nonlinear behavior affects the sampled voltage when the on-resistance increases as V_{in} gets closer to $|V_{th}|$. This behavior increases the error in the stored value.

This effect can be canceled by connecting the resistances of the NMOS and PMOS transistors in parallel. This configuration, depicted in Fig. 5.40a, is called complementary switch or transmission gate (TG). Fig. 5.40b shows the equivalent on-resistance of the TG, $R_{on,eq}$, and can be calculated by

$$R_{on,eq} = R_{on,N} \parallel R_{on,P} \tag{5.18}$$

where $R_{on,N}$ and $R_{on,P}$ are the on-resistances of the NMOS and PMOS respectively.

Considering the fact that the gate of the NMOS transistor is connected to V_{dd} to turn it on and the gate of the PMOS is connected to ground (V_{ss}), the condition for $R_{on,eq}$ be independent of V_{in} can be extracted from (5.17) and (5.18) as

$$\mu_n C_{ox}\left(\frac{W}{L}\right)_N = \mu_p C_{ox}\left(\frac{W}{L}\right)_P. \tag{5.19}$$

As mentioned previously, the mobility of electrons is usually between 2 to 3 times the mobility of holes depending on the technology. Thus, the ratio of the widths of

the PMOS and NMOS transistors are the design parameters to satisfy the condition in (5.19). This condition is met by selecting the width of the PMOS to be 3 times the width of the NMOS for this technology. Furthermore, the input voltage level shall be between $|V_{th,P}|$ and $V_{dd} - V_{th}$, preferably around $V_{dd}/2$, to reduce errors due to mismatches.

The size of TG transistors should be selected as large as possible to reduce the on-resistance. On the other hand, large transistors mean large C_{gs}. The sampling clock is generated by the output buffer and is buffered with unit size inverters. Thus, cascade inverter buffer must be placed to drive the TG if the size of its transistors are large. This buffer generates delay which affects the timing and sampling synchronization. It was shown in section 5.2.2 that the optimum taper factor of the cascaded inverter buffer is equal to 3. From (5.9) can be concluded that if the transistor size is increased by factor 9 then only two buffer stages are required. Thus, the width of the NMOS will be 1.44 μm and the width of the PMOS transistor will be 4.32 μm based on (5.19). In this case for PMOS a three stage buffer is required which is favorable since the signal driving the PMOS is the inverse of the one driving NMOS. The resulting equivalent resistance of the TG is about 680 Ω.

The capacitance of the hold capacitor, C_H, shall be small enough to be charged within the sampling period, i.e. 10 ns, and large enough to hold the charge during the hold time. This means that it shall be much larger (> 100 times) than the input capacitance of the comparator (≈ 12 fF as is designed in section 5.4.2). Thus, the capacitance of 1.45 pF is selected. The resulting time constant of the sample and hold circuit is $\tau = R_{on,eq}C_H = 986$ ps which corresponds to charging time of 4.93 ns.

Fig. 5.41 depicts the simulation result of the designed sample and hold circuit. The figure on top includes the input ramp and the output of the sample and hold circuit. The figure on the bottom depicts the sampling clock. As it can be observed, the input is sampled at each high level of the sampling clock and the output remains constant until the next high level of the clock input. The sampling starts at the rising edge of the clock and stops at the falling edge where hold time starts. The hold stops at the next rising clock edge.

The small disturbances in the sampled signal during the hold time is caused by the output signal of the DAC. As will be explained in section 5.4.3, the output of the DAC is pulled down to zero at each clock pulse to discharge all the capacitors. This produces a trail of zero values at the input of the comparator which reflects itself on the other comparator input. This effect can be removed by adding a unity gain voltage buffer at the output of the sample and hold circuit and adding an independent biasing circuit for the comparator. In this case, the capacitance of the hold capacitor can also be reduced.

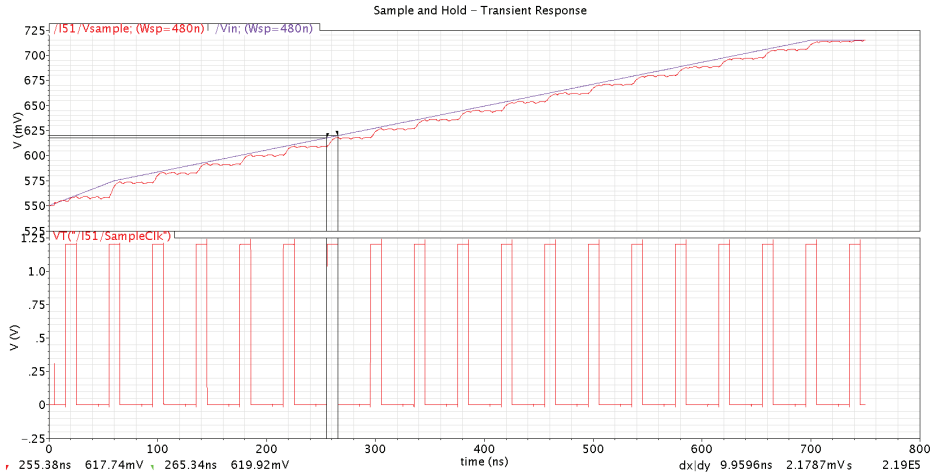


Figure 5.41: Sample and hold simulation result. The top figure is the input and the sample and hold output. The bottom figure depicts the sampling clock

5.4.2 Comparator

The comparator is a differential amplifier (same principle as Fig. 5.24) with a very high gain which compares its two inputs and depending on which one is higher determines its output. The output of the comparator has two states: positive and negative. In the positive state, the output value equals to the positive supply voltage and in the negative state, it equals to ground or negative supply voltage (in case of dual-supply circuit). The output will be positive if the positive input is higher than the negative input and will be negative if the negative input is higher than the positive input.

The first stage of the comparator determines its SNR. The voltage input noise equivalent of a CMOS differential pair can be calculated by [121]

$$\overline{v_n^2} = 8kT\left(\frac{2}{3g_m} + \frac{1}{g_m^2 R_D}\right) + \left(\frac{2K}{C_{ox}WL}\right)\frac{1}{f} \tag{5.20}$$

where k is the Boltzmann constant, T is the operating temperature, g_m is the transconductance of the transistors, R_D is the load resistance, K is a technology dependent coefficient, C_{ox} is the gate oxide capacitance per unit area, f is frequency and W and L are the gate width and length of the differential pair transistors respectively.

Using the UMC 0.13 technology parameters and considering R_D very high so that

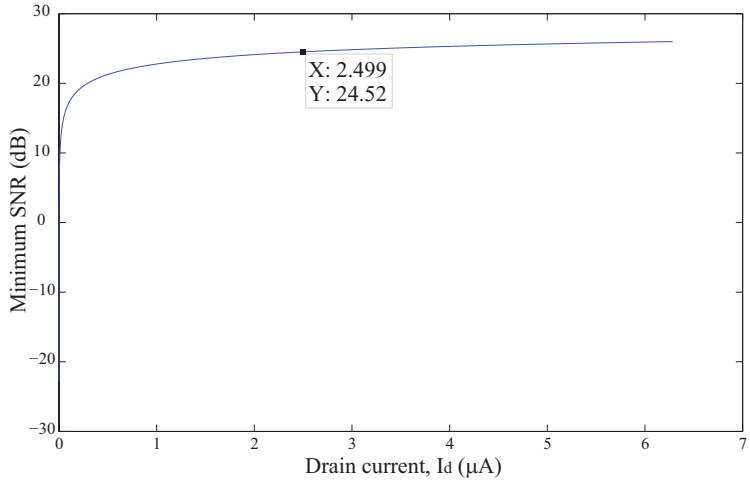


Figure 5.42: Minimum SNR vs. NMOS drain current in a differential pair with the smallest transistor size (W = 160 nm and L = 120 nm) and the input signal bandwidth of 100 MHz

its effect on $\overline{v_n^2}$ is negligible, the SNR_{min} is calculated by

$$SNR_{\text{min}} = 10\log\left(\frac{V_{\text{min}}^2}{\overline{v_n^2}}\right) \tag{5.21}$$

where V_{min} is the minimum detectable signal defined in Table 5.6.

The values of SNR_{min} for different drain currents (I_d) are depicted in Fig. 5.42. In this graph, the smallest transistor size (W = 0.16 μm and L = 0.12 μm) and the input signal bandwidth of 100 MHz is considered which is equivalent to the internal clock frequency of the ADC operating at maximum sampling speed. For the drain currents higher than 1.8 μA, the SNR_{min} is higher than 24 dB. Thus, I_d = 2.5 μA is selected for each transistor of the first stage differential pair. The exact transistor size of the first stage will be larger and is determined by the allowed input mismatch error. Using larger transistors increases the SNR_{min} value.

In differential amplifiers, the mismatch between the threshold voltage (V_{th}) of the two amplifier transistors results in a DC offset. This offset could, in turn, result in an incorrect output value or locking the output independent of the input. In order to avoid such problems, it is important to achieve best possible matching. Aside from the geometric effects in matching which should be taken into account during the layout design, the matching also depends on the transistor size. Each IC technology provides the area dependent mismatch model for each of its transistor

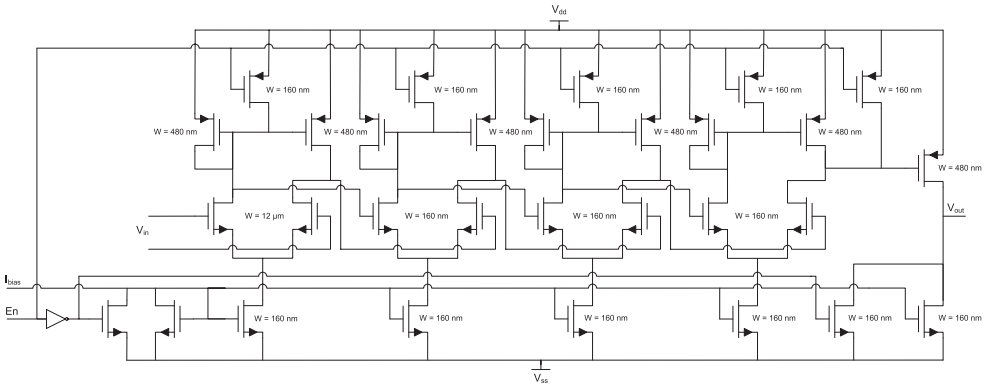


Figure 5.43: Designed comparator for SAR ADC

types. The variance of V_{th} is inversely proportional to the transistor area [132]

$$\sigma^2_{V_{th}} = \frac{A}{WL} \tag{5.22}$$

where A is the proportionality coefficient. To ensure that the V_{th} mismatch of the first stage of the comparator is small relative to the minimum detectable signal, the 3σ value of V_{th} should be less than $V_{\min}$ or

$$3\sigma_{V_{th}} < V_{\min}. \tag{5.23}$$

Considering the given $V_{\min}$ = 4 mV, the transistor size of the differential pair of the first stage should be W = 126 μm and L = 0.12 μm to achieve the required matching criteria based on the UMC 0.13 technology document [135]. However, these are very large transistors which dramatically increase the response time of the comparator.

Thus, to maintain the comparator speed (using smaller transistor size), either the equivalent voltage of the LSB should be increased (lower DAC resolution) or the reduction in the ADC speed should be accepted.

As a compromise between speed and accuracy, W = 12 μm and L = 0.12 μm are chosen from the design manual which leads to $3\sigma_{V_{th}}$ = 12.9 mV. This means that there is a 30% chance that the LSB is inaccurate due to possible input mismatch. This resolution is still acceptable since the degradation due to the quantization noise is increased only by 0.2 dB [74, 75] in the worst case. The amplification of the first stage is sufficient to keep the rest of the differential pairs at minimum size since their mismatch will be negligible compared to their input voltages. In this way, the high speed of the comparator is maintained.

The gain of the differential pair, A_{diff}, with a resistive load, R_D, can be determined by

$$A_{\text{diff}} = g_m R_D. \tag{5.24}$$

However, using a resistive load occupies a very large area. Since symmetric output is not important in this case, an active load can be used without extra circuitry in order to reduce the area. In this design, a PMOS current mirror is used as the active load. The width of the PMOS transistors is selected to be 3 times the minimum width of the technology to compensate for the mobility of the majority carriers (holes). The PMOS current mirror shows 350 kΩ resistance at V_{gs} = 400 mV and I_d = 2.5 μA operating point. Thus, the gain of the first stage will be 42 dB.

The load of the comparator is an inverter. Fig. 5.22a depicts the transistor implementation of an inverter. Since its output is either connected to V_{dd} or V_{ss}, the gate drain capacitors of PMOS (C_{gdP}) and NMOS (C_{gdN}) are in parallel. The gate source capacitors of the PMOS (C_{gsP}) and the NMOS (C_{gsN}) are both connected to the input from one side and to V_{dd} and V_{ss} from the other side respectively; thus, connected in parallel. The input impedance of the inverter, $Z_{in_{\text{NOT}}}$, can be calculated by:

$$\begin{aligned} C_{in_{\text{NOT}}} &= C_{gsP} + C_{gdP} + C_{gsN} + C_{gdN} \\ Z_{in_{\text{NOT}}} &= \frac{1}{j\omega C_{in_{\text{NOT}}}} \end{aligned} \tag{5.25}$$

where $C_{in_{\text{NOT}}}$ is the equivalent input capacitor of the inverter. The input capacitance of the designed inverter in this technology is 24 fF. The last stage of the comparator should be able to deliver the required current to the load for fast operations.

The designed comparator is depicted in Fig. 5.43. In order to simulate its performance, a ramp voltage is applied to the reference input (the negative input). A sine wave is added to the ramp and is connected to the positive input. In this way, the input is varied within the full input range and the output is toggled with the maximum operating frequency of the comparator. The ramp starts at 575 mV and ends at 715 mV which is the full range of the DAC output as will be explained in the following section. The amplitude of the sine wave is selected to be the minimum detectable input of the ADC from Table 5.6, i.e. 4 mV. Since the DAC is operating with the positive edge of the clock frequency, its output varies with half this frequency, i.e. 50 MHz, which is the frequency of the sine wave in this simulation.

Fig. 5.44 depicts the output of the comparator. It can be observed that the output switches to positive when the sine wave is higher than the ramp and becomes zero when the sine wave is lower than the ramp. The input offset is about ±2 mV which is half the minimum detectable input of the ADC.

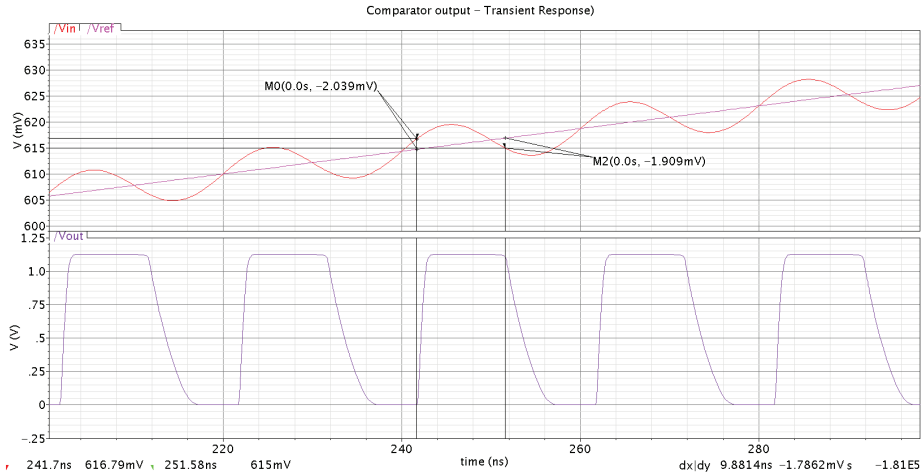


Figure 5.44: Comparator output for a ramp and ramp+sine inputs

5.4.3 Digital to Analog Converter (DAC)

As explained previously in section section 4.6, at each step of the binary tree the result is compared with the input signal. Since the binary tree generates digital values, they should be converted to analog to be compared with the input signal. This task is performed by the digital to analog converter (DAC). There are several DAC implementations [136]. Fig. 5.45 depicts an R-2R resistive ladder DAC and a capacitive DAC.

The operation concept of the resistive and capacitive DACs, depicted in Fig. 5.45, is based on voltage division between a number of series and parallel components connected between output and V_{dd} and output and V_{ss} based on the input bit configuration.

In the R-2R resistive ladder DAC (Fig. 5.45a) n resistors are connected between the output and V_{ss} in series. The resistances of the series resistors are the same (R) except for the the resistor connected to V_{ss} which must be twice the resistance of the rest of the series resistors ($2R$). This configuration provides n junctions including the output. The input bits are connected to these junctions by resistors with values of $2R$. The voltage equivalent of the full scale and LSB can be determined by [136]

$$V_{FS_R} = \left(1 - \frac{1}{2^n}\right) V_{dd}$$
$$V_{\mathrm{LSB}_R} = \frac{1}{2^n} V_{dd}. \tag{5.26}$$

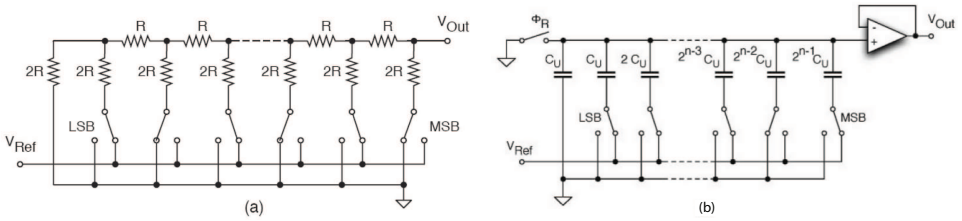


Figure 5.45: a) Resistive ladder b) capacitive DAC circuits [136]

In the capacitive DAC shown in Fig. 5.45b, one capacitor is connecting the output to V_{ss}. The capacitance of this capacitor, C_{ref}, acts as the reference to determine the values of the other capacitors. The rest of the capacitors are connected between the input bits and the output. The value of the capacitor connecting bit i to the output, C_i, is determined by [136]

$$C_i = 2^i C_{\text{ref}} \quad , \quad i \in \{0, 1, ..., n-1\}. \tag{5.27}$$

The voltage equivalent of the full scale and LSB of this configuration can be determined by

$$\begin{aligned} V_{FS_C} &= \left(1 - \frac{1}{2^n}\right) V_{dd} \\ V_{\text{LSB}_C} &= \frac{1}{2^n} V_{dd}. \end{aligned} \tag{5.28}$$

Theoretically, both DACs provide the desired output. However, there are some practical differences which makes one more favorable than the other. The capacitive DACs require to nullify the charge of each capacitor at each clock cycle which increases the circuit complexity compared to the resistive DACs. On the other hand, matching of the capacitors is about 2 orders of magnitude better than resistors in this technology [132] which provides a more accurate result.

In addition, simulations show that the average power consumption of both DAC types are in the same range while large resistors inject thermal noise in the circuit. Thus, a capacitive DAC is more suitable for this design.

Fig. 5.46 shows the complete implementation of the capacitive DAC. Based on Table 5.6, the input signal has a range of 150 mV. The comparator input requires a biasing voltage of 600 mV. Thus, the DAC output range should be from 600 mV to 750 mV. In order to achieve this operating range, a 7-bit DAC is designed with MSB connected to V_{dd} and bits 5 and 6 connected to V_{ss}.

The capacitive DAC requires nullifiers to nullify the charges of the capacitors at the beginning of each clock cycle. These nullifiers are implemented by NMOS

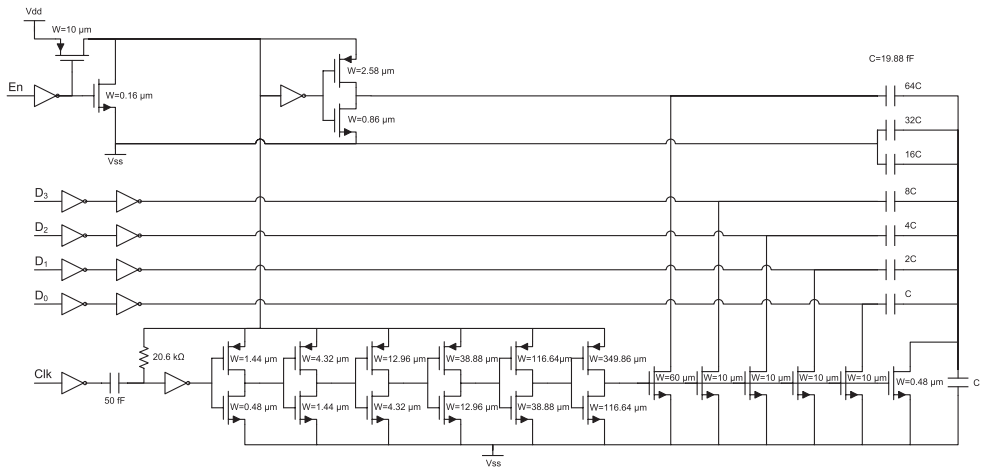


Figure 5.46: 4-bit capacitive DAC circuit

transistors. The output which is the common node of all capacitors is connected to the drain of an NMOS transistor. The other pin of each capacitor is connected to the drain of individual NMOS transistors. The gate of all these nullifier transistors are connected to the internal reset. The internal reset is implemented by an RC circuit connected to the clock input. At each clock positive edge, the RC circuit generates a narrow pulse which is used for internal rest. The nullifier transistors are large transistors to show a small on-resistance and be able to drain the charges of the capacitors in a very short time. Since the C_{gs} of nullifier transistors are all in parallel, they form a large capacitance. This capacitance is the load of the internal reset circuit. Thus, a cascade buffer is used between them. The number of stages and β can be determined by (5.9). The total load capacitance in this configuration is 101.63 fF. Thus, N = 6 and $\beta = 3$.

The designed DAC simulation is depicted in Fig. 5.47. In this simulation, the clock frequency is set to maximum, i.e. 100 MHz and the four digital inputs (LSB to MSB) are fed with square wave signals with frequencies of 50 MHz, 25 MHz, 12.5 MHz and 6.25 MHz respectively. Thus, the DAC input is decrementing starting from 15 and ending at 0.

As depicted in Fig. 5.47, the DAC output is nullified at each rising edge of the clock and then converges to the analog equivalent of the input. Based on the simulation results, the full range is 134.7 mV. The average value of LSB of the DAC is 8.75 mV.

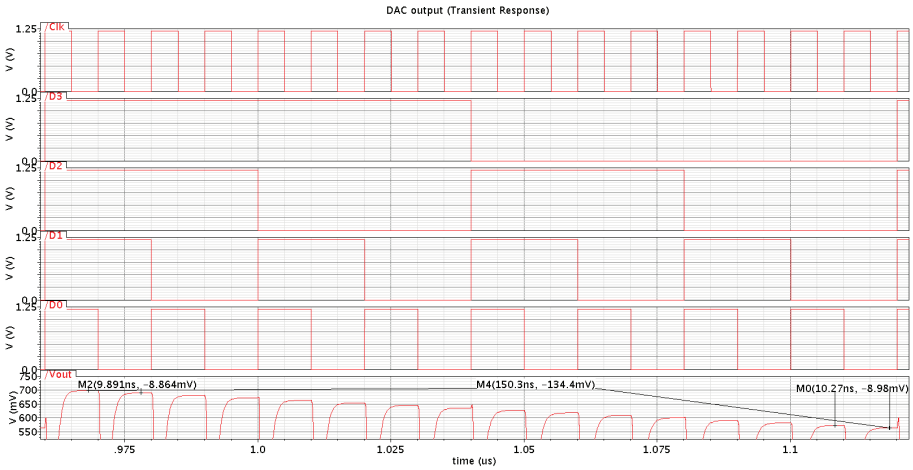


Figure 5.47: Results from the 4-bit capacitive DAC simulation

Logic Circuit

As mentioned previously, the SAR ADC uses the binary tree search to converge to the result. The value selection process is performed by the logic circuit. Since the ADC has 4 bits resolution a 4 stage binary tree is required. In order to implement the 4 stage binary tree, a sequential logic circuit is required which consists of a combinational logic unit (CLU) and a memory unit (MU). The CLU receives five input signals which are named D_{0-3} and $\overline{U}/D$ and delivers four outputs named Q_{0-3}. The MU is a 4-bit parallel-in parallel-out (PIPO) register and is initialized by "1000" at each positive edge of the sampling clock. The value of the MU changes at each positive edge of the internal clock which is 4 times the sampling clock frequency. The outputs of the MU are fed back to the CLU as well as connected to the output buffer. The fifth input of the CLU, $\overline{U}/D$, is connected to the output of the comparator.

The CLU block is designed by generating the truth table and simplifying it by the Karnaugh map method [137]. The result in terms of sum of products is

$$\begin{aligned} Q_0 &= \sum(2,6,10,14,18,22,26,30) \\ Q_1 &= \sum(2,4,6,10,12,14,20,28) \\ Q_2 &= \sum(4,6,8,12,14,22,24,30) \\ Q_3 &= \sum(0,1,3,5,7,8,9,10,11,12,13,14,15,16,17,19,21,23,25, \\ &\quad 26,27,28,29,30,31). \end{aligned} \tag{5.29}$$

The logic circuit is designed to work with positive edge of the clock. The conver-

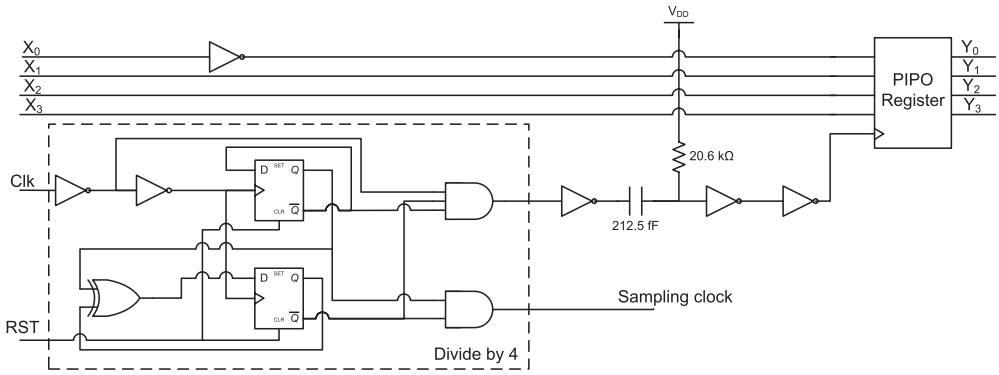


Figure 5.48: Output buffer of the designed SAR ADC

sion process converges in four steps. Thus, the valid output is the 4^{th} value of the MU. This value is buffered in the output buffer at the negative edge of every 4^{th} internal clock to incorporate the delays.

Output Buffer

The ADC output during operations must remain unchanged. A buffer is placed at the output to keep the valid output value during the convergence process. The output buffer circuit is depicted in Fig. 5.48. The inputs of the buffer are the outputs of the logic circuit, X_{0-3}. The LSB of the output is the invert of the output of the comparator in the 4^{th} step.

In order to generate the proper signal to save the 4^{th} step value in the output buffer and generate the sampling clock, a divide by 4 circuit is used. This divide by 4 circuit has two complementary outputs. One output is used for sampling the ADC input and the other one is triggering the output PIPO register to save the converged result. The latter is delayed by an RC circuit to ensure that the output of the logic circuit is stabilized.

In these digital circuits, all the input ports are buffered by two cascaded inverters to have a fixed fan-in. The outputs are buffered, if necessary, to provide the necessary fan-out.

5.4.4 Complete ADC Simulation

A ramp signal is applied to the input of ADC for its simulation. The sampling frequency is set to maximum, i.e. 25 MHz, which correspond to sampling period of 40 ns. Since the full range of a 4-bits ADC includes 16 steps, the ramp length should

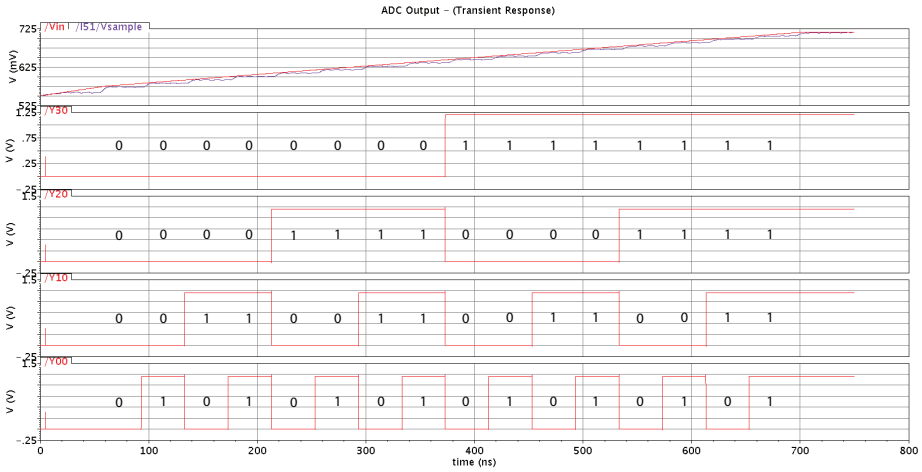


Figure 5.49: ADC output for a ramp input. The top figure is the input signal and the sampled input. The four below figures are the digital outputs, MSB on top and LSB at bottom.

be 640 ns. The full range of the designed ADC and the LSB of its DAC are 140 mV and 8.75 mV respectively as mentioned in section 5.4.3. Thus, a ramp is applied which starts at 575 mV and ends at 715 mV in 640 ns.

The ADC simulation result is depicted in Fig. 5.49. The top figure is the input ramp and its sampled signal. The other four figures at the bottom are the ADC digital outputs with MSB on top and LSB at bottom. The digital equivalent of each signal level is also depicted in Fig. 5.49 to ease the visualization.

The slope of the ramp is such that at each sampling point the input is increased by one LSB, i.e. 8.75 mV. Thus, the resulting digital output is incremented at each sampling time.

The power consumption of the ADC depends on its sampling rate. Simulation shows that the total power consumption of the designed ADC is about 80 μW at 25 MS/s.

Table 5.7 summarizes the target design specifications of the ADC and what has been achieved. The designed ADC meets all the requirements.

5.5 Experiences on the Design

This work was an effort requiring two disciplines, electronics engineering and space systems engineering. Coming with a background from electronics industry,

Table 5.7: Comparison of target and achieved ADC design specifications

Design specification	**Target**	**Achieved**
Full range [mV]	150	140
Resolution [bits]	4	4
Minimum input voltage (V_{min}) [mV]	4 ($< \frac{1}{2}$ LSB)	2
Input signal bandwidth [MHz]	12.276	12.5
Power consumption [μW]	< 100	80
Supply voltage [V]	1.2	1.2

it was very challenging, while interesting, to satisfy the needs of both disciplines. Their approaches to tackle problems from identification to analysis and development are different which is a reflection of the approaches in their industries. Both have their own advantages and deficiencies which can be regarded as complementary and, although project dependent, combination of their methods can improve the total efficiency.

The development process started by defining requirements. For this purpose, in addition to a literature study, several meetings were arranged with potential users to collect their needs. The requirements were generated based on users' input and potentials of technology. The problems were identified and the block with the most potential of improvement, i.e. the mixer, has been determined.

The available software, Cadence and MATLAB, were together powerful enough to cover all the needs of the development process and their simulation results can be used for verification. However, Cadence, though powerful, is not a very user-friendly software. Thus, this necessitated a strong supporting team to increase development speed.

The proposed zero-IF mixer architecture was developed in cooperation with SystematIC B.V.. During the system level verification process, it was discovered that around the same time a similar idea has been patented [104] using only one path for down-conversion, i.e. Path_II in Fig. 4.2. Although the proposed architecture is different from what was patented, it prevented us from filing a patent.

After the detailed design of each block, an extensive simulation was performed to verify the design. Corner simulation is a part of this simulations where variations of parameters due to process and environment are taken into account and individual simulations are run for each corner. Afterwards the layout of the circuit is designed. Cadence has the ability to extract the circuit from the layout and simulate it to verify its operations. In this step, parasitics are taken into account and modifications shall be made to the design to make sure it is working properly. This final layout is then fabricated. The parameters of the fabricated hardware is then measured to validate the design.

In this work, verification simulations, including several corner simulations, were performed and the ADC layout was designed. Further steps were not completed as part of the PhD project due to time and cost restrictions.

5.6 Summary

In this chapter, development tools and design methodology was introduced and four main blocks of the proposed architecture for a GPS/Galileo receiver front-end have been developed. These building blocks are mixer, IF and baseband amplifier, oscillator and ADC.

A novel innovative architecture has been proposed and developed for the zero-IF mixer. Thus, its design begins with system level simulation to verify its functionality. After this verification, the mixer has been designed in detail and the transistor level circuit is developed, simulated and verified. In this novel mixer, the problem of flicker noise and DC-offset which are the two major obstacles in using zero-IF mixers are solved while meeting most of the requirements presented in Table 5.1. Due to the bandwidth limitation of the designed IF amplifier, this front-end can only process the GPS C/A code and E1 OS code. However, by replacing the IF amplifier with the one with higher bandwidth, i.e. 25 MHz, full capacity of the GPS and Galileo signals can be exploited. Following the mixer the quadrature relaxation oscillator has been designed and simulated which performs compliant to the requirements. The ADC is designed at the final section of this chapter and meets all the requirements as defined in Table 5.6. At the end an overview of the design experience is explained.

In the previous chapters, the main blocks of the proposed receiver front-end have been developed. In the following chapter, the thesis will be concluded and recommendations and outlooks will be presented.

6

Conclusions and Recommendations

6.1 Motivation and Objectives

A Global Navigation Satellite System (GNSS) receiver has in the past primarily been used for navigation purposes. However, as the number of available GNSS systems has increased, the potential of introducing new applications using these systems has also increased. GNSS signals are used in a number of applications other than navigation such as timing, real-time tracking, search and rescue, surveying and mapping, agriculture, fun and gaming, Earth gravity modeling, high resolution ionosphere imaging, atmospheric limb sounding and GNSS reflectometry. These applications became possible due to the availability of different GNSS signals in different frequency bands.

The capability of using several GNSS systems ensures that the application is not interrupted as long as at least one system is operational. There are already several GNSS systems fully operational such as NAVSTAR Global Positioning System (GPS), GLObal NAvigation Satellite Systems (GLONASS), or under development such as the Galileo satellite navigation system and Compass (Beidou).

In applications which use GNSS signals, the availability of several GNSS systems can,e.g., improve the robustness of the application and increase the tolerance of the application to signal degradations. Such applications can also benefit from (self-)calibration and increased accuracy.

The applications which rely only on one particular GNSS system are facing a sin-

gle point of failure due to such dependency. Thus, redundancy is crucial for such applications. If the GNSS receiver can operate with more than one GNSS system, the application becomes more robust and its performance can be improved.

On the other hand, extensive research and developments in state-of-the-art integrated circuit (IC) technology facilitates the integration of complex systems in a very compact and efficient manner. This miniaturization can be spun into space applications which are very complex systems by itself. It was argued in chapter 1 that standard IC technology nowadays has the potential to be incorporated in space applications. Using this potential leads to new approaches in spacecraft design as well as potentially new space applications which may require short time-to-market.

However, space applications demand extra requirements in comparison to terrestrial applications which shall be satisfied. These requirements, amongst others, include operation modes, high dynamics, interferences and environmental requirements, such as related to temperature, radiations, vacuum and vibration. Thus, when using state-of-the-art IC technology in space, these requirements need to be considered as well. Multi-purpose and flexible subsystems provide the capability of adaptive operation modes to spacecraft. Using such spacecraft provides the opportunity of designing more sophisticated missions which can perform, e.g., even in-situ reconfigurations of the mission. The flexibility of subsystems in terms of operations is considered to be important for power efficiency as well. Thus, such future spacecraft subsystems shall be multi-purpose, flexible, low-power and low-cost whenever feasible. One example of such a subsystem is guidance, navigation and control (GNC) subsystem which employs a GNSS receiver. Thus, the GNSS receiver itself shall be multi-purpose, flexible, low-power and low-cost and shall be capable of processing multiple GNSS systems and integrated in a single package. This feature renders them multi-purpose and adding the possibility of reconfiguration, e.g. in terms of the number of processed GNSS bands, gives them the flexibility to operate in various operation scenarios. Such receivers could be used, e.g., in highly miniaturized satellites such as micro-, nano- and pico-satellites and improve their performance accordingly.

As explained in chapter 2, GNSS receivers consist of an analog front-end and a digital back-end. The digital back-end can be programmed to process the signals of different GNSS systems. Thus, adding a new GNSS system is more of a programming challenge than a hardware design challenge. However, designing a single receiver front-end which can receive multiple GNSS signals is an interesting hardware development challenge which is still not available for space applications and holds exciting prospects. Thus, the research objectives of this thesis was to develop a space-capable, flexible, multi-purpose, low-power and low-cost GNSS receiver front-end. This front-end shall be able to process GNSS signals from different GNSS systems and different frequency bands. The research questions which

were answered during this research are:

RQ1 - What are the commonalities between GNSS signals from different GNSS systems and different frequency bands which can be used to develop a common front-end for them?

RQ2 - What is the most suitable architecture for a space-capable, flexible, multi-purpose, low-power and low-cost front-end?

RQ3 - What are the characteristics of this architecture and how it can be verified?

RQ4 - How to implement this architecture?

6.2 Summary and Results

The development process of the GNSS receiver front-end began by defining requirements. For this purpose, in addition to a literature study, several meetings were arranged with potential users to collect their needs. The requirements were generated based on users' input and potentials of the state-of-the-art IC technology. An in-depth study was performed to extract the characteristics of different GNSS systems. Then, all existing receiver front-end architectures have been studied and the most promising architecture for space-capable, flexible, low-power and low-cost GNSS receiver, i.e. zero-IF, has been determined using trade-off techniques. Following the identification of the obstacles of the selected architecture, i.e. flicker noise and DC-offset, innovative solutions to solve these problems were provided. These two obstacles mainly prevent the wide usage of zero-IF architecture in CMOS technology. The provided solution benefits both space and terrestrial applications. As a result of this solution, an innovative multi-purpose and flexible GNSS receiver front-end architecture based on zero-IF has, for the first time, been developed and characterized. The flexibility of the proposed architecture in terms of operations is considered to be important for power efficiency.

Four blocks of the front-end, mixer, IF amplifier, oscillator and ADC, were designed in transistor level. After the detailed design of each block, extensive simulations were performed for verification of the design. The available software, Cadence and MATLAB, were together powerful enough to cover all the needs of the development process and the simulation results are reliable to be used for verification. (RQ3)

The in-depth study of GNSS signals, presented in chapter 2, shows that GNSS signals have commonalities that can be used in designing a multi-GNSS receiver front-end. At this time, GPS is using binary phase shift keying (BPSK) modulation for spreading the signal spectrum. Galileo is using binary offset carrier (BOC)

modulation as well as Compass. GLONASS is using FDMA modulation. The trend of GNSS signals is towards using BOC modulation. New GPS signals will be using BOC. GLONASS is in the process of changing its signals to BOC modulation. Using BOC modulation enables GNSS signals to share carrier frequencies while maintaining their bandwidths. Thus, BOC will be the common modulation scheme of the future GNSS signals. Therefore, the common characteristics of most of the GNSS signals are their type of modulation, carrier frequencies and bandwidths (RQ1).

The multi-GNSS receiver front-end, developed in this thesis, can be flexible such that it processes the necessary signals depending on the specific application and its requirements. The advantage of the reconfigurability presents itself when different operating modes are expected and limitations in available power and data handling are present. In this case, the number of applications that can use this receiver increases. Thus, by using the same receiver for many different applications, production cost for such generic receivers can drop and the concept of mass production becomes viable.

The high-level architecture proposed in this thesis will enable this flexibility. In this architecture, one complete down-conversion path is placed for each GNSS band with enable/disable capabilities and analog-to-digital converters (ADC) with configurable sampling rates. Thus, the system can determine the number of GNSS bands it uses and adapt the front-end and processing power consumption as well as the amount of data generation which can also provide flexibility to data communication. Such a flexible approach to the operations of GNSS receivers is, certainly for space applications, highly innovative and new to the best of the writer's knowledge.

In order to find the best down-conversion architecture for each path, an extensive study on different front-end architectures was performed and presented in chapter 3. Comparing direct-sampling, heterodyne and zero-IF architectures, the zero-IF architecture was clearly the superior architecture, resulting from the outcome of the comparison and trade-off process (RQ2).

The Zero-IF receives the RF signal at the input and provides the baseband signal at the output. The same circuit can be used for all paths. The only difference is the oscillator frequency which shall be equal to the nominal carrier frequency of the band. The zero-IF architecture consists of LNA, mixer, (quadrature) oscillator, low-pass filter, baseband amplifier, variable gain amplifier (VGA) and ADC. In this thesis, the critical blocks of the zero-IF receiver are designed and simulated. These blocks are the mixer, the IF amplifier, the oscillator and the ADC.

However, in order to be able to use this architecture, two major problems of the zero-IF mixers had to be solved. These two problems are the flicker noise and DC-offset. Traditional zero-IF mixers use an external capacitor to realize a high-

pass filter to remove the DC-offset and flicker noise. This approach is not suitable for single chip IC design since it requires an external component. In addition, for BPSK signals, where the peak energy is at the carrier frequency, the high-pass filter will reduce the energy of the signal and the performance degrades depending on its corner frequency. BOC signals are immune to this effect since their peak energy is at the subcarrier frequency.

In this thesis, a novel architecture for zero-IF mixers has been developed which enables the expansion of the applications of zero-IF receivers which were facing limitations due to flicker noise and DC-offset. In this mixer architecture, a special analog signal processing is applied to remove the effect of the flicker noise and DC-offset. It uses the chopping technique with two double-sided quadrature oscillator signals. This combination shifts the carrier frequency to several in-phase and quadrature-phase IF frequencies which can be amplified without the effect of the flicker noise and DC-offset. The incorporated signal processing technique eliminates the need for complicated filter design since the intermediate signals are designed such that the baseband can be generated by a simple signal addition after the second down-conversion.

The mixer performs most of the amplification of the receiver. All the filters are first-order low-pass filters and no external component is required. The total power consumption of the designed mixer is about 34 mW with a 92.54 dB conversion gain. As a result, the applications of this innovative mixer is neither limited to space applications of GNSS receivers nor to GNSS receivers itself. It can be incorporated in many other receiver front-ends which may have considerable impact on technology, applications and business aspects of receiver front-ends in general.

In addition to the mixer, a complete quadrature oscillator has been designed in this thesis. Ring oscillator, LC oscillator and relaxation oscillator are the three different commonly used oscillators in the designs. They have been studied and the quadrature relaxation oscillator has been selected after comparison and a trade-off process.

The quadrature relaxation oscillator is an inductor-less first-order oscillator. Its performance is comparable to quadrature LC oscillator while consuming less area. Another advantage of the relaxation oscillator is that its frequency has a linear relation with its biasing current which relaxes the constraints of the PLL design. The simulated phase noise of the designed oscillator is -103.3 dBc/Hz at 1 MHz and its power consumption is about 10 mW.

The final block of the receiver chain is the ADC. There are different ADC architectures: sigma-delta (Σ-Δ), successive approximation register (SAR), pipeline, folding + interpolating and flash ADC. Since the output is at baseband, the sampling frequency is moderate and a SAR ADC is suitable for this application.

The ADC is designed for the maximum sampling rate, i.e. 25 MS/s, ensuring that

the ADC is operational at all defined sampling frequencies. The power consumption of the ADC depends on the sampling frequency and decreases as the sampling frequency is reduced. The power consumption of the designed ADC at highest sampling rate is about 80 μW. The designed ADC was simulated in all corners and operates at all corners. The ADC layout has also been designed (RQ4).

6.3 Recommendations

In this thesis, the major problems of developing a zero-IF receiver front-end have been addressed and solved. However, there are a few blocks remaining to be designed and some minor design improvements are required in order to arrive at a complete and functional front-end.

The complete front-end path includes also the LNA which must be developed. Since in this design a standard LNA has been assumed, the front-end architecture is not dependent on a special performance of the LNA.

The IF amplifiers, which have been designed in this thesis, are suitable for GNSS signals with low chip rate such as GPS C/A code and Galileo OS code. In order to exploit the full capacity of all GNSS signals, the bandwidth of the IF amplifiers must increase from 8.72 MHz to 25 MHz using frequency compensation techniques. The linearity of the designed IF amplifier meets the requirements for the GNSS receiver front-end. However, improving its linearity will improve the overall performance of the receiver.

The adder circuit of the mixer is generating spurious frequency due to different operation speeds of the transistors. Improving the adder circuit such that the spurious frequencies are eliminated will improve the accuracy of the amplitudes of the in-phase and quadrature baseband signal and thus the accuracy of the carrier phase measurement.

In very high accuracy GNSS receivers, the accuracy of the navigation solution depends on the accuracy of the carrier phase measurement. Thus, the effect of the front-end on the code and carrier phase must be taken into account. Oscillator phase noise is added to carrier phase measurement. Also, the nonlinearity of the front-end can show itself as amplitude compression or spurious frequency which, in turn, can affect the I-Q amplitudes and thus the carrier phase measurement. A study needs to be performed to analyze the effect of the oscillator phase noise and front-end linearity on the code and carrier phase solutions.

Finally, in order to characterize the effect of component mismatches, especially phase mismatches in different paths of the mixer, on the behavior of the front-end, a full corner simulations must be run. In addition, the complete circuit layout should be designed for tape-out and measurement. This was not possible in this

thesis due to time and cost constraints.

6.4 Outlook

A huge investment in terms of financial and research effort enters in terrestrial technology development. The end-user can afford the cost of using such state-of-the-art technology since, as a result of mass production, the expenses are distributed among the huge number of end-users.

Designing multi-function and reconfigurable chips increases the number of applications which can incorporate them. There is a large overlap between terrestrial and space systems as they share similar functionalities such as navigation, communication, processing units and interfaces in their subsystems. However, the development approaches of these industries are different. Space industry can benefit from development approaches practiced in other industries. It holds in particular for the development of small satellites which can be less risk adverse.

The rapid developments of state-of-the-art IC technologies allows a spin-in for space applications. Due to the overlap between terrestrial and space functionalities, mass production of subsystems which includes such functions becomes a viable choice. As a result, using these technologies benefits new space applications by contributing to a faster design of new space missions, better functionality, less mass and power consumption as well as reducing their time-to-market.

This thesis has shown how a multi-GNSS receiver front-end can be integrated in a single chip. This research can eventually be extended to entire subsystems of highly miniaturized spacecraft such as GNC, communication, on-board data handling and attitude determination and control. This work can thus be regarded as an example of how miniaturization can improve the development schedule, mission cost and performance of future space missions. Moreover, it can contribute through the realization of highly miniaturized, highly integrated systems to a new paradigm on how future space missions are being developed.

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Summary

The trend of space technology developments is moving from high power consuming, bulky and costly systems towards low-power, small, low-cost and flexible systems. Thus, the spacecraft can benefit from multi-purpose and flexible systems which can be low-power and low-cost by employing new technology. One example of such system is a GNSS receiver capable of adapting the number of used frequency bands depending on its power constraint and the required accuracy.

In the past, a Global Navigation Satellite System (GNSS) receiver has primarily been used for navigation purposes. However, as the number of available GNSS systems has increased, the potential of introducing new applications using these systems has also increased. Such applications become more robust and their performance can be improved if the GNSS receiver can operate with more than one GNSS system.

On the other hand, extensive research and developments in state-of-the-art integrated circuit (IC) technology facilitates the integration of complex systems in a very compact and efficient manner. This miniaturization can be spun into space applications which are very complex systems by itself. Using this potential leads to new approaches in spacecraft design as well as potentially new space applications which may require short time-to-market.

The research objective of this thesis is to develop a space-capable, flexible, multi-purpose, low-power and low-cost GNSS receiver front-end. This front-end shall be able to process GNSS signals from different GNSS systems and different frequency bands.

In chapter 1, an overview of navigation systems along with applications of GNSS systems is presented. This chapter also provides and introduction to state-of-the-art IC technology and its advantages and disadvantages for using it in space. Thesis objectives and research questions conclude this chapter.

Chapter 2 covers the fundamentals of satellite positioning system and provides a detailed explanation of GPS and Galileo signal structures followed by investigating a generic GNSS receiver architecture. This chapter is concluded with explanation of requirements for designing a space capable GNSS receiver.

In chapter 3, existing radio receiver front-end architectures are reviewed and compared. The most suitable architecture, i.e. zero-IF, is selected. Finally, an innovative and flexible architecture for GNSS receiver front-end based on zero-IF is proposed.

Chapter 4 begins with technology selection and calculations of link budget of the proposed receiver front-end. It is followed by reviewing various implementations

of building blocks of the front-end and their comparison. In this chapter an innovative mixer architecture for zero-IF architecture is proposed which overcomes its two main problems, the DC offset and flicker noise. The chapter concludes by selecting the most suitable circuits for mixer, quadrature oscillator and analog to digital converter (ADC) for this receiver front-end.

In chapter 5, the circuits of the mixer, quadrature oscillator, amplifier and ADC are developed in transistor level followed by verification simulations. The results of the simulations verify the expected behavior of the proposed mixer as well as the quadrature oscillator, amplifier and ADC. The thesis is concluded in chapter 6 with summary of the results, recommendations and future outlook.

Samenvatting

De trend in de ontwikkeling in ruimtevaarttechnologie verplaatst zich van energie-slurpende, omvangrijke en dure systemen naar energiezuinige, kleine, goedkope en flexibel inzetbare systemen. Ruimtevaartuigen kunnen daardoor gebruik maken van flexibel inzetbare systemen die door het gebruik van nieuwe technologieën weinig energie verbruiken en ook erg goedkoop zijn. Een voorbeeld hiervan is een GNSS ontvanger die het aantal gebruikte frequentiebanden dynamisch aanpast, afhankelijk van zijn beschikbare hoeveelheid energie, alsook de vereiste nauwkeurigheid.

Vroeger werden GNSS (Global Navigation Satellite System) ontvangers voornamelijk gebruikt om mee te navigeren. Met het toenemen van het aantal beschikbare GNSS systemen is echter ook de mogelijkheid voor gebruik in nieuwe toepassingen, gebruikmakend van deze systemen, toegenomen. Deze toepassingen kunnen robuuster worden, en ook hun prestaties kunnen worden verbeterd als de gebruikte GNSS ontvanger meerdere GNSS systemen kan ontvangen.

Aan de andere kant staan de vele ontwikkelingen in state-of-the-art IC technieken de integratie van complexe systemen toe op een zeer compacte en efficiënte manier. Deze miniaturizeringsslag kan op zijn beurt weer geïntroduceerd worden voor gebruik in ruimtevaarttoepassingen, hetgeen op zichzelf al erg complexe systemen zijn. Het gebruik van deze ontwikkelingen leidt tot nieuwe manieren om ruimtetuigen te ontwerpen, en leidt mogelijk ook tot nieuwe toepassingen binnen de ruimtevaart die mogelijk voordeel hebben van een kortere "time-to-market".

Het doel van deze thesis is de ontwikkeling van een goedkope, flexibel inzetbare, energiezuinige GNSS ontvanger front-end, die geschikt is voor gebruik in de ruimte. Deze front-end zal in staat zijn om signalen van verscheidene GNSS systemen op verschillende frequentiebanden te verwerken.

In het hoofdstuk 1 wordt een overzicht gegeven van de verschillende GNSS navigatiesystemen en hun toepassingen. Dit hoofdstuk geeft ook een inleiding tot hoogtechnologische IC-technologieën en hun voor- en nadelen voor gebruik in de ruimte. Het hoofdstuk wordt afgesloten door de gestelde doelen voor deze thesis en de gestelde onderzoeksvragen.

Het hoofdstuk 2 verslaat de basis van satelliet-navigatie-systemen, en geeft een gedetailleerde verklaring van de signaal-opbouw van de GPS en Galileo signalen, gevolgd door een bechrijving van een generieke GNSS ontvanger-architectuur. Dit hoofdstuk wordt afgesloten door een beschrijving van de vereisten voor het ontwerp van een GNSS ontvanger, die geschikt is voor gebruik in de ruimte.

In het hoofdstuk genaamd 3 worden bestaande radio-ontvanger front-ends beschreven en vergeleken. De geschiktste architectuur, de zogenaamde zero-IF architectuur werd gekozen. Uiteindelijk wordt een innovatieve en flexibel inzetbare architectuur voor een GNSS ontvanger front-end gepresenteerd.

In het hoofdstuk genaamd 4 wordt een proces-technologie geselecteerd, en worden er link-budgets berekend voor de voorgestelde front-end. Hierna volgt een overzicht van de verschillende mogelijke implementaties van de bouwstenen die nodig zijn voor de front-end, die vervolgens worden vergeleken. In dit hoofdstuk wordt een innovatieve architectuur voor een mixer voor een zero-IF front-end voorgesteld, die twee van de grootste problemen met zo een architectuur oplost. Dit zijn met name DC offset en zogenaamde flicker noise. Het hoofdstuk eindigt met het selecteren van de geschiktste circuits voor de mixer, de quadratuur-oscillator en de analoog-naar-digitaal-omzetter (ADC) voor deze front-end.

In het hoofdstuk 5, worden de circuits voor de mixer, de quadratuur-oscillator, de versterkers en de ADC op transistorniveau beschreven. Daarna volgen simulaties ter verificatie. De resultaten van deze simulaties verifiëren het verwachtte gedrag van de voorgestelde mixer, net als het gedrag van de quadartuur-oscillator, de versterker en de ADC. De thesis eindigt met het hoofdstuk 6, met een samenvatting van de resultaten, enkele aanbevelingen en een blik op de toekomst.

List of Publications

International Journals

1. P. J. Buist, S. Engelen, A. Noroozi, P. Sundaramoorthy, S. Verhagen and C. J. M. Verhoeven, **Overview of Pulsar Navigation: Past, Present and Future Trends**, *Journal of Navigation (Washington)*, Vol. 58, Issue 2, 2011, pp. 153-164

International Conferences

1. A. Noroozi, C. J. M. Verhoeven, G. L. E. Monna, E. K. A. Gill, F. Stelwagen, R. Kearey and E. Wiek, **Flexible single chip solutions for highly integrated miniaturized spacecraft**, *62nd International Astronautical Congress*, Cape Town, South Africa, 2011

2. P. J. Buist, S. Engelen, A. Noroozi, P. Sundaramoorthy, S. Verhagen and C. J. M. Verhoeven, **Principles and Potential of Pulsar Navigation**, *24th International Technical Meeting of The Satellite Division of the Institute of Navigation (ION GNSS 2011)*, Manassas, VA, USA, 2011

3. A. Noroozi, C. J. M. Verhoeven, G. L. E. Monna and E. K. A. Gill, **A concurrent GPS/Galileo direct conversion receiver front-end for space applications**, *ProRisc 2010*, Veldhoven, The Netherlands, 2010.

4. A. Noroozi, G. L. E. Monna, C. J. M. Verhoeven, E. K. A. Gill, **A Direct Conversion GPS/Galileo Receiver Front-end for Space Applications**, *NAVITEC 2010, 5th ESA Workshop on Satellite Navigation Technologies*, ESA/ESTEC, Noordwijk, The Netherlands, 8-10 December 2010

5. A. Noroozi, C. J. M. Verhoeven, G. L. E. Monna and E. K. A. Gill, **A Reconfigurable Multi-band GNSS Receiver Front-end for Space Applications: System Level Considerations**, *ProRISC/IEEE Workshop on Semiconductors, Circuits, Systems and Signal Processing*, Veldhoven, The Netherlands, 2008.

6. A. Noroozi, C. J. M. Verhoeven, G. L. E. Monna, E. K. A. Gill, **A Reconfigurable Multi-band GNSS Receiver Front-end for Space Applications**, *NAVITEC 2008, 4th ESA Workshop on Satellite Navigation Technologies*, ESA/ESTEC, Noordwijk, The Netherlands, 10-12 December 2008

7. R. Heusdens, S. Engelen, P. J. Buist, A. Noroozi, P. P. Sundaramoorthy, C. J. M. Verhoeven, M. Bentum and E. K. A. Gill, **Match filtering approach for signal acquisition in radio-pulsar navigation**, *63rd International Astronautical Congress*, Napels, Italy, 2012.

8. F. Belien, S. Engelen, A. Noroozi and C. J. M. Verhoeven, **Autonomous Navigation for Trans - Lunar Nano-Satellite Missions**, *62nd International Astronautical Congress*, Cape Town, South Africa, 2011

9. C. J. M. Verhoeven, S. Engelen, A. Noroozi, P. Sundaramoorthy, M. Bentum, R. Meijer and G. L. E. Monna, **Emerging Eco-System: Nano Satellite Swarms and Large Satellites**, *62nd International Astronautical Congress*, Cape Town, South Africa, 2011

10. J. Guo, J. Bouwmeester, E. Gill, A. Noroozi, C.J.M. Verhoeven, J. Rotteveel, J. Leijtens, R. Tijsterman, B. Sanders, **Miniaturized Dutch Spacecraft based on MicroSystem Technology**, *7th ESA Round-Table on MNT for Space Applications*, ESA/ESTEC, Noordwijk, The Netherlands, 13-16 September 2010

11. A. Noroozi, L. Ha, P. van Dalen, A. Maas, S. de Raedt, P. Poulakis, B. Foing, **A Small lunar Rover for Reconnaissance in the Framework of ExoGeoLab Project, System Level Design**, *European Geoscience Union General Assembly*, Vienna, Austria, 2009

12. B. H. Foing , J. Page, P. Poulakis, G. Visentin, A. Noroozi, E. Gill, P. Batenburg, G. G. Drijkoningen, E. C. Slob,M. Guglielmi, M. Freire, R. Walker, M. Sabbatini, V. Pletser, E. Monaghan, L. Boche-Sauvan, R. Ernst, J. Oosthoek, S. Peters, A. Borst, P. Mahapatra, D. Wills, C. Thiel, L. Wendt, C. Gross, J. P. Lebreton, T. Zegers, C. Stoker, J. Zhavaleta, P. Sarrazin, C. Blake, C. McKay, P. Ehrenfreund, A. Chicarro, D. Koschny, J. Vago, H. Svedhem and G. Davies, **Exogeolab Lander/Rover Instruments and EuroGeoMars MDRS campaign**, *40th Lunar and Planetary Science Conference*, The Woodlands, Texas, USA, 2009.

13. A. Haddadi , A. Noroozi, C. J. M. Verhoeven and E. K. A. Gill, **A Novel Structured Mathematical Framework for Parallel Processing in Cooperative Satellite Swarms**, *ISSCAA 2008, 2nd International Symposium on Systems and Control in Aerospace and Astronautics*, Shenzhen, China, 10-12 Dec 2008

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Delft, July 2013

Curriculum Vitae

Arash Noroozi was born in Tehran, Iran on 23rd April 1974. He received his B.Sc. in 1998 from Shahid Beheshti University, Tehran, Iran. He worked as R&D engineer in RASA Co. Tehran, Iran from 1998 till 1999 where he gained experience in analog and digital electronic system design and computer programming. He was promoted to project manager in 1999 and he was leader of the electronic design team and supervisor of production and assembly facilities. In October 2002, he joined Shuttle Pars Trading Co. (SPT) as technical consultant to expand his expertise in the industrial and commercial fields. He gained experience in the fields of industrial communication protocols, automation, distributed sensors, field instrumentation and fire and gas detection systems. The last six months at SPT. he worked as the head of safety and automation department before he continued his studies in 2004.

In October 2004, he went to Budapest University of Technology and Economics (BUTE) to continue his education. In September 2005, he joined Delft University of Technology (TU Delft) as a masters student and received his M.Sc. in July 2007 in microelectronics. He joined the chair of Space Systems Engineering (SSE) of the Faculty of Aerospace Engineering to pursue his Ph.D. in September the same year. His research was to design an integrated front-end for GPS and Galileo navigation systems for space applications. In addition to his core research during his PhD, he was introduced to the idea of pulsar navigation and worked partly on this topic as well. In September 2012, he co-founded ELPASYS to develop hardware and software systems. His interests are system development and integration (hardware and software), electronics for space, pulsar navigation, pulsar receivers and space commercialization.