A Low-Cost Universal Integrated Interface for Capacitive Sensors

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To my family

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CHAPTER 1

Introduction

1-1 Capacitive-sensor systems

Capacitive sensor elements can be applied in many applications to measure many different types of signals such as displacement, proximity, humidity, acceleration, liquid level, gas concentration, etc., [1], [2]. They can be implemented on printed-circuit boards [3], glass substrates, silicon chips, or other types of material [4]. Because the electrodes of a capacitive sensor element do not need to be in mechanical contact with each other, they are suited for small-range contact-less sensing [3]. The attractive properties of capacitive sensors are that they consume very little power, that their cross sensitivity to temperature is very low, and that shielding stray electric fields is less complex than shielding, for instance, inductive sensors from magnetic disturbances [2]. The main drawbacks of capacitive sensors concern their sensitivity to contamination and condensation, and their sensitivity to Electro-Magnetic Interference (EMI). However, in this thesis we will show that some of these drawbacks can be overcome by proper design.

Depending on the application, capacitive sensor can be floating (i.e. sensors in which neither of the electrodes is grounded) or grounded (i.e. sensors in which one of the electrodes is grounded) [5]. Based on the properties of the electrode structure and the dielectric material, the electrical properties of capacitive sensors can differ significantly. For instance, they can demonstrate pure capacitive behavior or have resistive leakage [6]. Their values can range from less than one pF up to hundreds of pF or even to nF. Sometimes their values can change very fast, such as in displacement sensors for servo systems, while in other applications their values can be semi-static. Besides the aforementioned sensor conditions, the effects of parasitic capacitances of the connecting wires should also be taken into account.

At present, a number of interface ICs for capacitive sensors can be found in the market. Examples of such interfaces are the capacitance-to-digital converters for floating capacitors AD7745 and AD7746 of Analog Devices [7], and the AD7747 for grounded capacitors. Additionally, the same company offers the AD7150, which is a low-power (300 μW) capacitive-sensors interface. With all of these interfaces, the maximum capacitance that can be measured amounts to 8 pF, while the maximum allowable parasitic capacitance is 100 pF. The measurement results of all of these interfaces are very sensitive to the effects of resistive leakage.

Another capacitive-sensor interface in the market is the MS3110 of Irvin sensors [8]. For this interface, the range for the input capacitances is limited to only 10 pF.

The work presented in this thesis concerns an interface that is based on and is complementary to Smartec's UTI (Universal Transducer Interface) [9]. For the capacitive modes of the UTI some major limitations are:

1. High sensitivity to resistive leakage currents;
2. The interface is only suited for floating capacitors and not for grounded ones;

3. The input ranges for the capacitive modes are programmable for only three discrete levels: 2pF, 12 pF and 300 pF, while for the 300 pF range the excitation voltage is decreased, which decreases the resolution;
4. The fastest data acquisition rate is up to 100 samples per second.

Due to the severe limitations of these interfaces, they are only suitable for a very limited number of applications. For instance, in many applications the range of capacitance values does not fit into the dynamic ranges of these interfaces. Moreover, the cable parasitic capacitance can be much larger than what these interfaces can handle. In many applications, the required data acquisition rate is much higher than what is offered by these interfaces. To solve these problems, in this thesis a universal interface for capacitive sensor with improved performance is introduced.

1-2 A universal interface for capacitive sensors

In order to achieve the best performance, we need to optimize the interface for each specific application. This means that for each application we should develop different electronic circuits. From an economical point of view, this approach is not attractive. Moreover, it requires the effort of many highly-specialized expertise. To solve this problem, this thesis describes a flexible universal interface which can be used for different applications. The main part of the interface is common to all applications. The main difference is implemented in a relatively small part: the front-end. Figure 1-1 shows a block diagram of this interface.

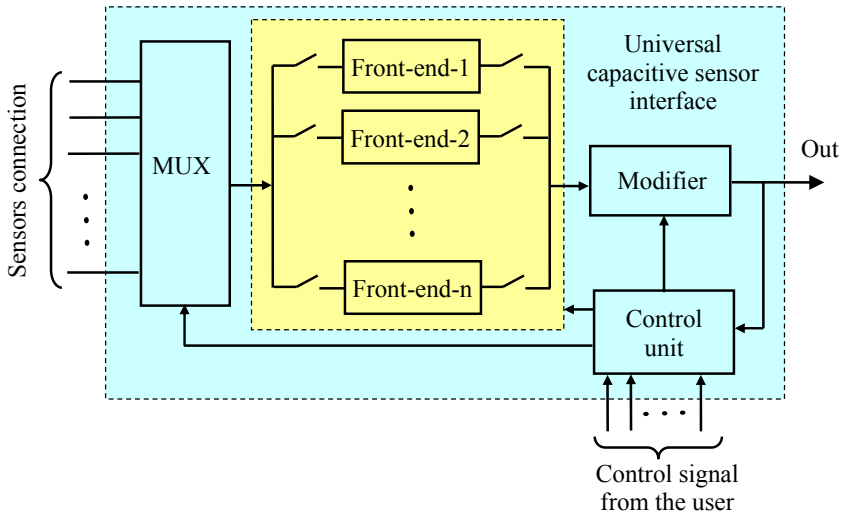

Fig. 1-1: The universal capacitive sensor interface.

Just with a logic control signal that can be set by the user, the measurement configuration is modified for different applications and has the following properties:

- This interface is suited for both floating and grounded capacitive sensors;
- It has also a front-end for leakage-immune measurements of floating capacitors;
- It can be optimized for short or long connection cables;
- The input dynamic range is adjustable over a wide range;

- The excitation voltage can be chosen by the user;
- The period and measurement times can be chosen for optimum values, which are application-dependent.

All these options make the proposed interface suitable for a wide variety of capacitive sensor applications.

1-3 Statement of the problems

The objective of the work presented in this thesis is to design an integrated universal capacitive sensor interface with emphasis on maximizing the performance in relation to the costs. To begin with, some typical applications and sensor elements are considered for this design. Next, the electrical properties of the capacitive sensors are characterized as accurately as possible. Then, the most important interface requirements for different applications are considered. The final step is to make a trade-off between the number of modes, the number of control signals, and the performance. A further increase in the number of modes will decrease the user friendliness and increase the test-related costs. Therefore, the number of modes should be kept to a minimum, with a minimum sacrifice of performance and application range.

1-4 Organization of this thesis

The text in this thesis is organized as follows:

- Chapter 2 covers general physical aspects of capacitive sensors.
- Chapter 3 deals with the concepts for capacitance measurements.
- Chapter 4 presents a detailed analysis of the applied circuits.
- The design presented in chapter 5, are based on the analysis presented in chapter 4 together with an experimental evaluation.
- A novel interface with negative feedback is introduced in chapter 6, together with an experimental evaluation.
- Chapter 7 deals with interface circuits for leaky capacitive sensors, along with an experimental evaluation.
- The analysis and design of a switched capacitor front-end for grounded capacitive sensors is presented in chapter 8, together with an experimental evaluation.
- Chapter 9 covers the original contribution in this work.
- A brief overview of some basic measurement principles is presented in Appendix A.

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CHAPTER 2

Physical principles of capacitive sensors

2-1 The concept of capacitance

Capacitors belong to the oldest types of electrical devices [1]. The capacitor was invented in 1746 by Cuneus and Mussenbroek, who worked at the University of Leiden, and was originally called the 'Leidsche fles'. For a good, fundamental understanding of the concept of capacitance we have to reconsider the original definition of capacitance given by Maxwell in 1873 [2]. If we have a configuration made up of any number of electrodes (Fig. 2-1), then the capacitance between two of the electrodes (say, *i* and *j*) is given by the quotient of the charge induced on one of the electrodes due to the potential difference between the two electrodes, and that difference in potential. When written as an equation this gives:

$$C_{ij} = \frac{Q_{ij}}{V_i - V_j}, \tag{2-1}$$

where C_{ij} is the capacitance between electrodes *i* and *j*; Q_{ij} is the charge on electrode *i* (and in contrasting form on *j*) induced by the potential difference (V_i - V_j); and V_i and V_j are the potentials on electrodes *i* and *j*, respectively. For all the other electrodes (except *i* and *j*) not their potential, but their presence contributes to the capacitance between the electrodes *i* and *j*.

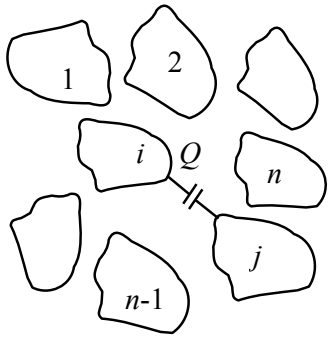

Fig. 2-1: Fundamental representation of capacitance between conductors.

When only the capacitance between two of the conductors is of interest, the presence of other conductors is an undesirable complication. To deal with this, it is customary to distinguish between two-terminal and multi-terminal capacitors and their measurements.

In a two-terminal capacitor (Fig. 2-2(a)) the somewhat indefinite contributions of the other conductors to the capacitance of interest might be negligible/acceptable. To reduce their influence, one of the conductors of primary interest surrounds the other one, so that the capacitance between them is independent of the location of all other bodies except for those in the vicinity of the terminals.

A three-terminal capacitor (Fig. 2-2(b)) represents the common situation of two active electrodes surrounded by a shield conductor. The direct capacitance C_x between the two active

electrodes is the capacitance of interest. When shielded leads are used, this capacitance is independent of the location of all other conductors except for that of the shield.

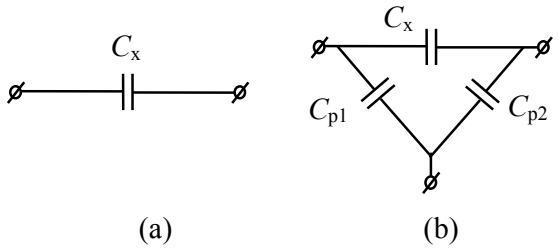

Fig. 2-2: (a) Two and (b) three-terminal capacitors.

In the case of just two electrodes, the capacitance depends on their size, shape, distance, and the permittivity of the medium. When these parameters are actually known, the capacitance between the electrodes can be calculated. However, analytical calculations are only applicable for simple structures. In general, a finite element method (FEM) is used to find an approximated solution. Fortunately, in capacitive sensors, we are usually interested in *changes* of capacitances as caused by a measurand rather than in *absolute values* of these capacitances. When designing electrode structures, care should be taken to determine precisely how the measurand influences the capacitance. This often leads to electrode structures that have a high degree of similarity with flat electrodes, which are often in parallel, flat or cylindrical planes. Because this thesis is dedicated to electronic interfaces for measuring capacitive sensors, a study focusing on the details of capacitive-sensor structures is beyond the scope of this work. Yet, understanding the basic principles of capacitive sensor will help in designing a better measurement system. Therefore, the basic principles of these sensors will be reviewed here.

2-2 Structures of capacitive sensors

The simplest structure of a capacitive sensor is that of two flat parallel plates with area A and distance d (Fig. 2-3).

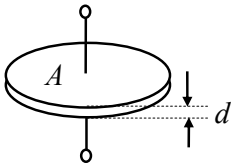

Fig. 2-3: A capacitor with flat, parallel plates.

When d is much smaller than the plate dimensions, the value of the capacitance can be approximated as:

$$C = \varepsilon_r \varepsilon_0 \frac{A}{d}, \tag{2-2}$$

where ε_0 is the permittivity of the vacuum ($\varepsilon_0 = 8.85 \times 10^{-12}$ F/m), and ε_r is the relative permittivity of the dielectric in between the two electrodes.

Equation (2-2) is only valid for that condition specified. Yet, also for other types of capacitors, the capacitance value increases with an increase in the effective area or the

permittivity of the medium, and decreases with an increase in the effective distance. Accordingly, three types of capacitive sensors can be distinguished:

- Capacitive sensors with fixed values of A and d, where the measurand modifies the dielectric properties (ε-type);
- Capacitive sensors with fixed values of A and ε, where the measurand modifies the distance (D-type);
- Capacitive sensors with fixed values of d and ε, where the measurand modifies the effective area (A-type).

Since relative permittivity is not a very fundamental quantity, and can be either temperature-dependent, inhomogeneous or anisotropic for certain materials, the accuracy of ε-type sensor is limited.

The D-type capacitive sensors are very effective for short-range displacement measurements. However, sensitivity decreases significantly with increasing distance. In contrast to this, an A-type can also be used for very large measurement ranges.

Some example of the three different types of capacitive sensors will now be discussed.

2-2-1 The D-type capacitive sensors

As mentioned in the previous section, the value of parallel-plate capacitors can be calculated with Equation 2-2, provided that the distance d between the two plates is much smaller than the dimensions of the plates itself. However, due to fringes of the fields (Fig. 2-4(a)), the actual capacitance value is always slightly larger than the one calculated. Since this difference depends on the distance d, fringe fields can cause non-linearity in the measurement. Another problem with the structure of figure 2-4(a) concerns its sensitivity to lateral movement. This problem can be solved simply by making one of the plates bigger (Fig. 2-4(b)). The homogeneity of the electric field can be significantly improved by incorporating guard rings into the sensor (Fig. 2-4(c)), as suggested by Thomson [3]. A guard ring is an electrode that encloses the sensing electrode; the two electrodes are separated by an insulator but operated at the same electric potential. For high accuracy, the width of the guard electrodes should be 3 to 5 times larger than the electrode distance d [1].

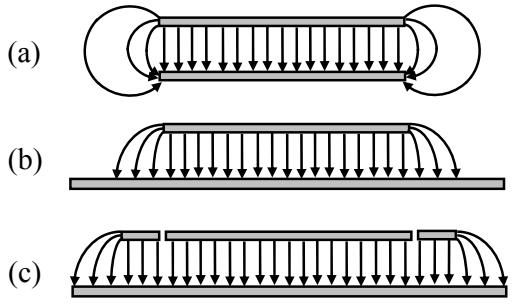

Fig. 2-4: A capacitive displacement sensor: (a) simple parallel-plate capacitor, (b) parallel-plate capacitor insensitive to lateral movement, (c) parallel-plate capacitor with guard ring.

As will be shown in chapter 3, one way to measure a capacitor is to drive one terminal of the capacitor with a voltage source and to measure the induced charge or current at the other terminal (floating capacitive sensor). Then, in unshielded capacitive sensors (Fig. 2-5(a)), in addition to the real excitation terminal of the capacitor, any interfering voltage $V_{\text{interfere.}}$

connected to neighboring conductors (Fig. 2-5(a)) can induce charge as well. Shielding the whole system will remove this effect. However, usually this is not applicable. As an alternative, the reading terminal can be shielded (Fig. 2-5(b)), which can remove the main part of the interference. Filtering in the electronic circuit can further reduce the effect of interfering signals if they are in different frequencies.

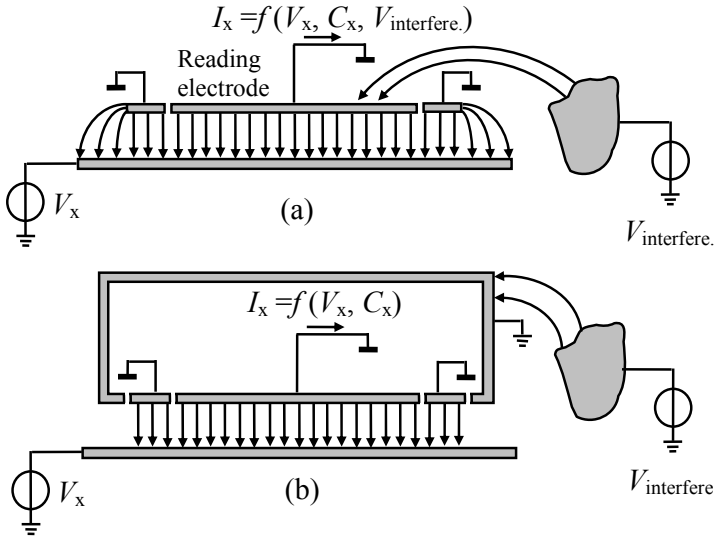

Fig. 2-5: Reading a capacitive displacement sensor (a) with and (b) without shielding.

The *D*-type capacitive displacement sensors are sometimes divided into the categories: single and dual plate [4]. Single-electrode capacitive sensors (Fig. 2-6) use a conductive target surface as a second electrode. The size of the sensor head can be different and is chosen in relation to the target range and the target shape [5]. In single-plate capacitive sensors, the contra electrode (the target) is usually connected to ground. In that case the measurement concept of figure 2-5 cannot be applied. The measurement of such grounded capacitive sensors will be discussed in chapter 8.

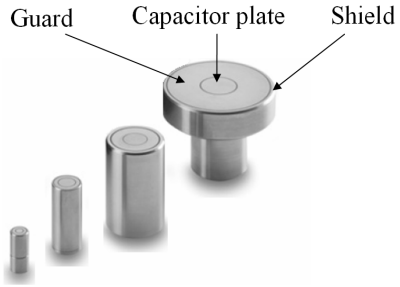

Fig. 2-6. Capacitive sensor heads for displacement measurement. For different target ranges and shapes different sizes are available (with courtesy of micro-epsilon).

Since the accuracy of single-electrode capacitive sensors depends on the quality of the target surface, which is usually less flat than that of the sensor head, for high accuracy, dual-plate capacitive sensors (Fig. 2-7) are preferable.

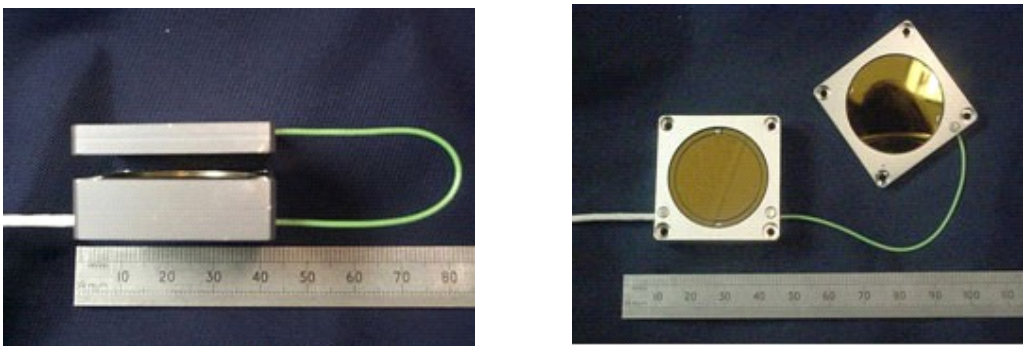

Fig. 2-7: Dual plate capacitive sensor for displacement measurement (courtesy of Queensgate Instruments).

Moreover, in dual-plate capacitive sensors, both electrodes are available, so that the capacitance can be read by special interface circuits that are intrinsically immune to stray capacitances [6].

2-2-2 The A-type capacitive sensors

The *A*-type capacitive sensors have been investigated extensively by, for instance, de Jong [8], Zhu [7], and Li [9]. Figure 2-8(a) shows a capacitive motion encoder [10] the principle of which is based on the measurement of area variations. While the pick-up plate (plate C) moves from left to right, the effective area between plate A and plate C (i.e. the associated capacitance, C_{AC}) decreases. At the same time the capacitance C_{CB} between plate B and plate C increases. When the pick-up plate moves from the right end to the left end, the output voltage V_o of the buffer amplifier (Fig. 2-8(b)) changes from the excitation voltage $V_{exc.}$ to zero. The structure of figure 2-8(a) is sensitive to tilt in two axes: The effect of tilt around the vertical (y) axis can be minimized by using a smaller pickup width. However, tilt around the horizontal (x) axis causes a large error in the measured position. To reduce this error, the modified ramp pattern of figure 2-8(c) can be used. It can be seen that close to the right and the left end, the pickup voltage is a nonlinear function of the position [10]. However, with the pattern shown in figure 2-8(d), this nonlinearity problem can be reduced [10]. Similar to the *d*-type capacitive sensor, we need guard and shield electrodes around the pickup plate.

The accuracy of *A*-type capacitive sensors highly depends on the mechanical accuracy. The major mechanical non-idealities originate from the non-idealities of the electrodes, such as non-flatness of the electrode surface, obliqueness, deformation, frayed edges, and gaps [9].

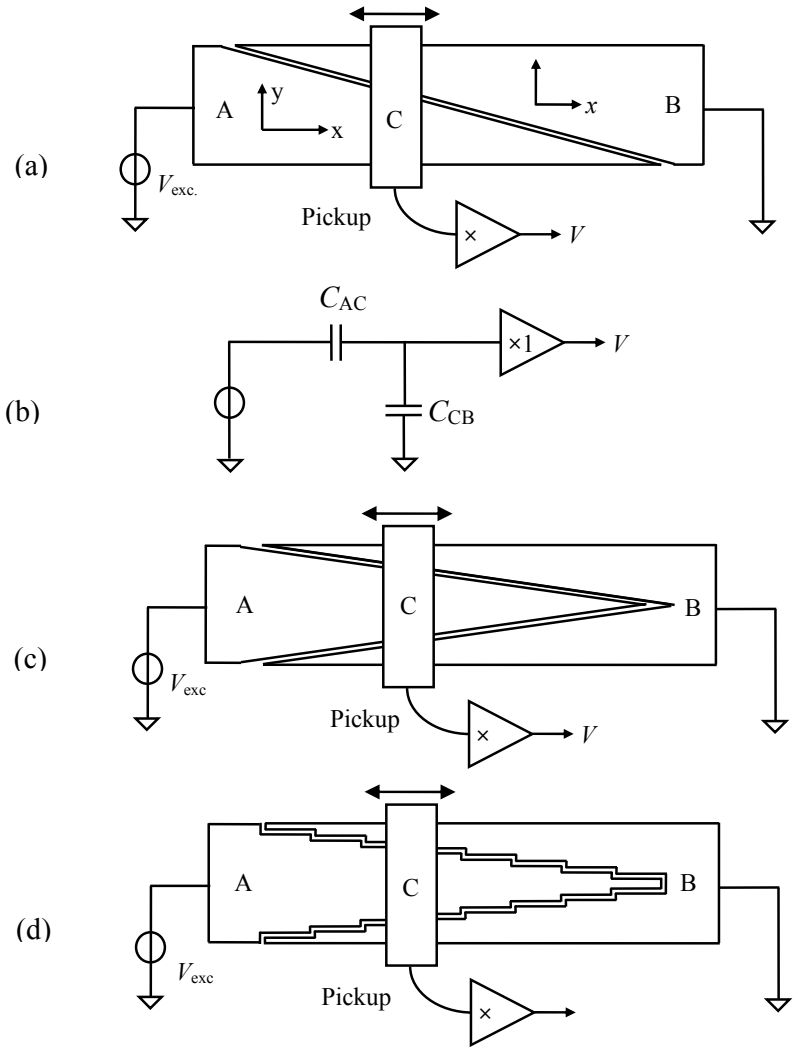

Fig. 2-8: A capacitive motion encoder according to [10]: (a) Basic structure, (b) the electrical equivalent circuit, (c) a modified structure which is immune to tilt around the horizontal (x) axis, and (d) a modified version with less nonlinearity at the ends.

2-2-3 ε-type capacitive sensors

The ε-type capacitive sensors may be used to characterize materials or to determine the position of the interface between various types of liquids. Well-known examples of such sensors are capacitive humidity sensors and liquid level gauges. In these sensors resistive leakage can be an important issue, which needs to be considered in interface design.

Figure 2-9 shows an example of a liquid-level gauge [11] which is used to measure the level of conductive liquids. The isolated probe and the conductive-liquid can be considered as two plates of a capacitor, while the electrode isolation layer acts as the dielectric medium. With a set of dual probe, non-conductive-liquid levels can also be detected. In this case, the two probes act as the two electrodes of a capacitor and the non-conductive liquid acts as the dielectric medium.

Fig. 2-9: A capacitive level sensor, reproduced with permission of Omega engineering, INC, Stamford, CT 06907 USA, WWW.OMEGA.COM.

The probe, which can be rigid or flexible [11], commonly employs conducting wire insulated with polytetrafluoroethene, PTFE (Teflon). In the case of conductive liquid in conductive fluid vessels, the use of insulated wire is inevitable. Flexible probes must be used when there is insufficient clearance for a rigid probe, or in applications that demand very long lengths. Rigid probes offer higher stability, especially in turbulent systems [11].

The use of a capacitance array implemented with a large number of segmented electrodes [8] can improve the repeatability, resolution, and even functionality of the sensor. In segmented capacitive level gauges, a first-course level measurement is performed by a fast measurement. Next, a more accurate (fine) measurement is performed using interpolation of the capacitances of the electrodes close by the liquid-gas interface [8], [12]. With a single-electrode capacitive probe, only one interface, usually the interface of liquid with air, can be measured. However, with a segmented capacitive probe, more than one interface, for instance the interface between water and oil at the bottom of the tank and the interface between oil and air at the top, can be measured with one probe. Figure 2-10 shows the installation of a segmented capacitive level sensor to measure these interfaces in a storage tank.

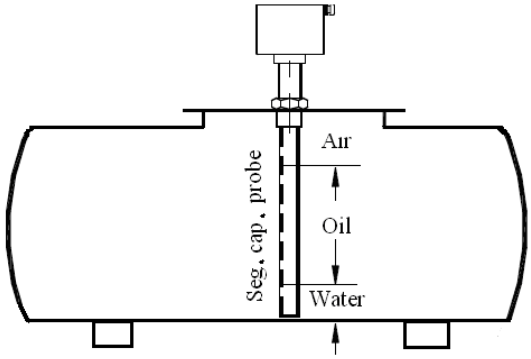

Fig. 2-10: Installation of a segmented capacitive level sensor to measure the two interfaces between water, oil and air.

2-3 Differential capacitive sensor

In some applications, the change in capacitance value due to a measurand is much less than the sensor rest (offset) capacitance [13]. When this offset capacitance is not stable, this will cause a resolution problem. A possible solution for this problem can be found in the use of differential capacitive sensors. As an example, figure 2-11 shows a differential capacitive sensor for a MEMS accelerometer with capacitive readout [13]. In addition to reducing the resolution problem, the applied half-a-bridge structure has the advantages of CM rejection of interfering effects, including temperature drift.

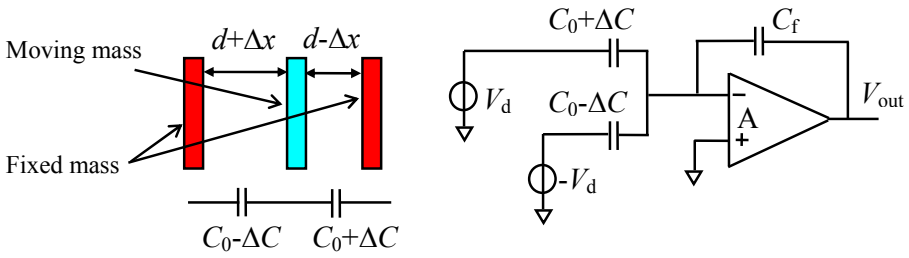

Fig. 2-11: (a) MEMS accelerometer and (b) the read-out circuit.

2-4 Stability of capacitive sensor

Environmental changes such as temperature, humidity and pressure will change the capacitance value. Since controlling these environmental factors is not simple in most measurement systems, the stability of the sensor is limited. Therefore, amongst other causes, environmental changes limit the minimum detectable variation of the measurand.

The sensitivity of a capacitance value to these parameters comes from both the thermal expansion of the electrodes or their distance, and the sensitivity of dielectric constant to environmental parameters. Most common metals and alloys have a temperature coefficient of linear expansion in the range of $(9 \text{ to } 29)\times10^{-6}$/ºC [14].

Moreover, the dielectric constant is quite sensitive to temperature, humidity and pressure. For instance, as their basic property, some capacitive humidity sensors use the ε-dependency on humidity. A capacitive sensor with air as the dielectric constant (which is quite stable) is quite simple to build and has many applications. The sensitivity of the dielectric constant of air to temperature, humidity and pressure, amounts to about 5×10^{-6}/ºC, 1.4×10^{-6}/%RH and 100×10^{-6}/atm, respectively [10, p. 73]. Even these small sensitivities can limit the accuracy of the sensor.

The environmental effects can be compensated by either differential structure (section 2-3), or by building a reference capacitor that is similar to the sense capacitors and using a balanced bridge detector [15] with auto-calibration [16].

2-5 The effect of connection cables on capacitive sensors

In addition to the capacitive sensor itself, the connection cable also needs to be shielded. Figure 2-5(b) shows the case for when both the receiving electrode of capacitive sensor and the current detector (electronic interface) are within a shielded box. However, often the electronic interface is far from the sensor. In that case, at least the current sensing wire needs

to be shielded (Fig. 2-12).

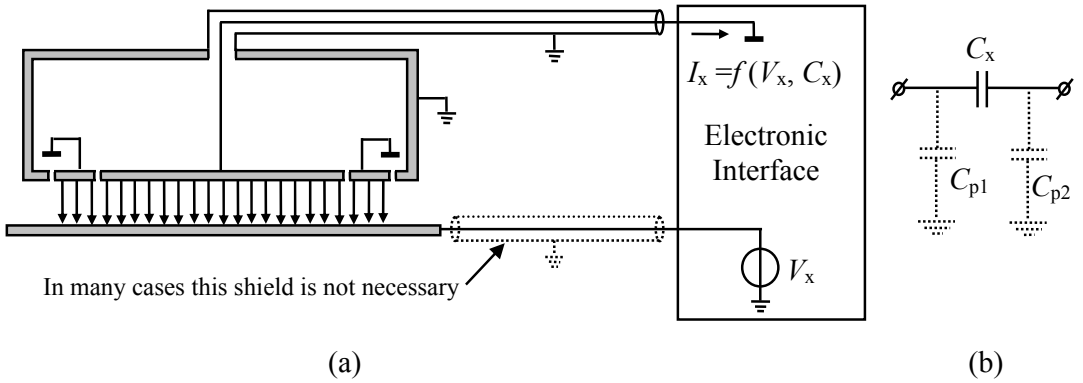

Fig. 2-12: (a) Floating capacitive sensor with shielded connection cable and (b) the first order equivalent circuit.

Floating capacitors can be measured with interface circuits that are intrinsically immune to parasitic capacitances to the ground [6]. However, in the case of a grounded capacitive sensor, the shield should be connected to the same potential as the core using active guarding (Fig. 2-13) [6, 17]. The concept of active guarding is explained with more detail in chapter 8.

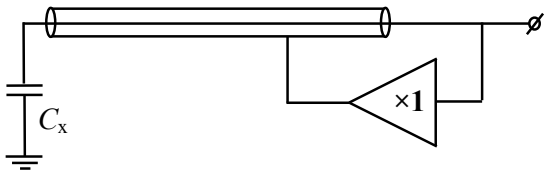

Fig. 2-13: Active guarding for a grounded capacitive sensor.

2-6 Conclusion

The basic principles of capacitive sensors have been presented. The concepts of two-terminal and three-terminal capacitor were explained. A short explanation about shielding and guarding was presented. Three different types of capacitive sensor –*A*-type, *D*-type and *ε*-type– were shown together with some examples. Segmented and differential capacitive sensors and their benefits were also discussed. Finally, shielding requirements of connection cables and the concept of active guard for grounded capacitive sensor were referred to.

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CHAPTER 3

Measurement Techniques for Capacitances

3-1 Introduction

This chapter discusses basic principles of techniques used to measure capacitances with high precision and with a high immunity for the effects of parasitics. When implementing these techniques in a universal sensor interface, the design challenges are:

1. In most cases, the sensor capacitance value is very low, in the range of a few pF or less;
2. Often it is necessary to measure a small sensor capacitor in the presence of much larger parasitic ones;
3. Often complete shielding of capacitive sensors is not possible (Fig. 2-5(b)). In that case, they can easily pick up interference from their environment. As a result, the amount of interference needs to be reduced with appropriate filtering techinques;
4. In sensors with a large signal bandwidth, it is rather challenging to achieve the required resolution.

It will be shown that using new circuit techniques together with IC technology, most of the problems can be overcome while still using low-cost interface technology.

3-2 Excitation and A-D conversion

To measure a sensor capacitance, we need to excite the capacitor with a voltage or a current. In principle, the excitation signal can have any type of waveform. However, usually either sine waves or square waves are used. Therefore, we will compare two types of the capacitance measurement system: with sine-wave excitation and with square-wave excitation.

Measurement systems based on sine-wave excitation can have a high resolution, but meeting the requirements of cost minimization, power [3] and maximization of flexibility is difficult. Therefore, we focus on capacitance measurement based on square-wave excitation. In that case, the interface circuit can be implemented using switched-capacitor (SC) techniques. Since SC circuits are implemented with switches and capacitors, CMOS technology is highly suited for such implementations. Moreover, the complexity and power dissipation of SC circuits are quite low.

For sensor systems, the signal bandwidth is rather moderate. However, often a high resolution and a high accuracy are required. To perform analog-to-digital (A-D) conversion, the best option is to use the principles of indirect conversion [4, 5, 6 and 7]. Two popular indirect conversion principles are a) those of sigma-delta converters [6], and b) the conversion of the analog signal to a period time and then digitizing the period time with a counter [8, 9]. In the following sections, we will summarize these basic principles as they are applied to capacitance-to-digital conversion. In this chapter we will limit ourselves to the case of floating capacitors.

3-2-1 Capacitance measurement based on sigma-delta converter.

Figure 3-1(a) shows a basic circuit diagram of a sigma-delta converter.

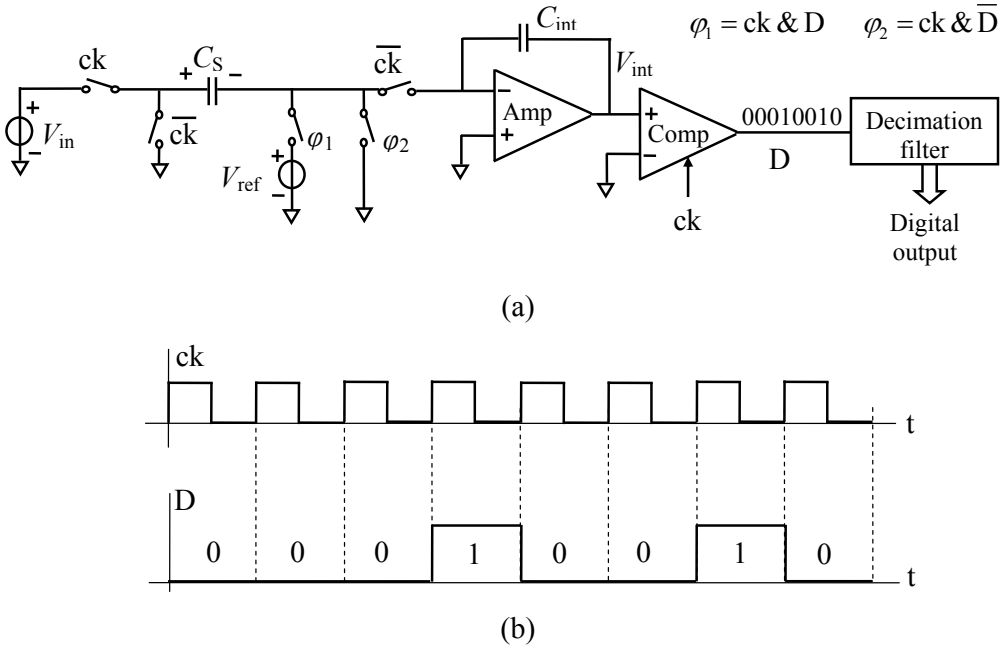


Fig. 3-1: Principles of a Sigma-Delta ADC: (a) a circuit diagram and (b) some related signals.

To understand how the circuit works, let us suppose that at $t = 0$, the integrator output is negative, and $V_{ref} > V_{in}$. Consequently, the comparator output voltage in the first clock cycle is zero. During this first clock cycle, the sampling capacitor C_S is charged to V_{in} and on the descending edge of ck, this charge is transferred to integrator capacitor C_{int}, which increase the integrator output voltage to jump with the value of $C_S V_{in}/C_{int}$. As long as the integrator output is negative, this process is repeated and finally brings the integrator output voltage to the positive level. With the first clock pulse after that, the charge of C_S (V_{in} - V_{ref}) is transferred to C_{int}, with which the above assumption ($V_{ref} > V_{in}$) renders the integrator output voltage negative. Since the amounts of charge transferred by V_{in} and V_{ref} should ultimately compensate each other, in a long stream of zeros and ones, the ratio of number of ones to the total clock cycle is equal to the ratio of V_{in}/ V_{ref}. Extracting this ratio is done by a decimation filter. To eliminate the resulting quantization noise, we need a large number of clock cycles to do the conversion. However, the quantization noise can be decreased using a higher-order loop filter (noise shaping) [6].

With a simple circuit modification, the *voltage*-to-digital converter (VDC) of figure 3-1(a) can be used as a *capacitance*-to-digital converter (CDC). The modified circuit is shown in figure 3-2.

When the comparator output is zero (low), the charge of $C_x V_{ref}$ is transferred to C_{int}, and when the comparator output is one (high), the charge $(C_x - C_{ref})\ V_{ref}$ is transferred to C_{int}. Therefore, because of charge balancing at the integrator input, in a long stream of zeros and ones, the ratio of the number of ones and the total number of clock cycles equals the ratio of C_x / C_{ref}. This principle has been used in the chips AD7745, AD7746, AD7747 and AD7150 of Analog Devices [10].

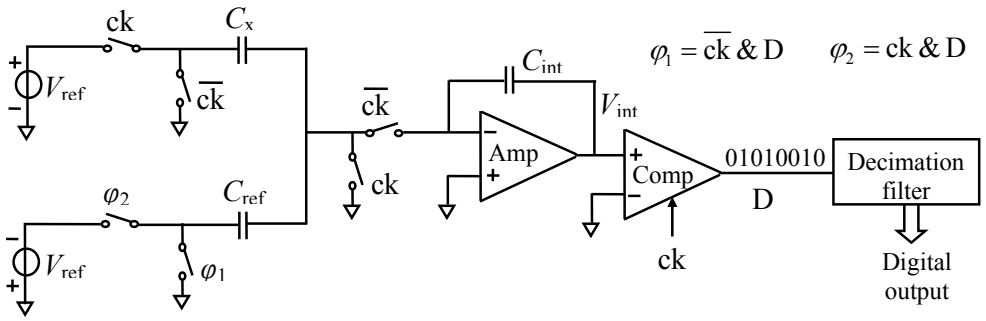


Fig. 3-2: A capacitance-to-digital converter (CDC) using sigma-delta principles.

3-2-2 Capacitance measurement based on a period modulator.

In this method the sensor capacitance is used in a free-running (relaxation) oscillator. The variation-in-capacitance values modulate the period of the oscillator output signal [8, 9]. This period can easily be digitized by a counter which is usually implemented in a microcontroller. In this way, the conversion of a capacitance value into a period time is very straightforward. However, as we will see in chapter 4, section 4-3, using a capacitance-to-voltage converter (CVC) in front of the free running oscillator for a universal interface has some distinctive advantages. In this case, the oscillator acts as a voltage-to-period convertor (VPC). The corresponding block diagram of the resulting capacitance-to-digital converter (CDC) is shown in figure 3-3.

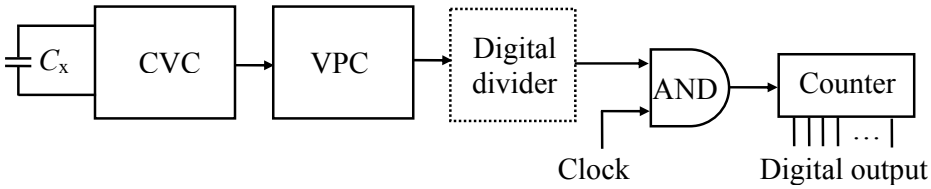


Fig. 3-3: The block diagram of a capacitance-to-digital converter (CDC) using a period modulator (VPC).

To achieve p bits of resolution, it is necessary that:

$$f_{clock} \geq \frac{2^p}{T_{max}}, \tag{3-1}$$

where T_{max} is the maximum value of the output period. For instance for T_{max} = 100 µs and 13 bits of resolution, the clock frequency should be higher than 80 MHz[1]. Usually, the sensor signal bandwidth is quite low. Therefore, a digital divider (Fig. 3-3) can be applied after the oscillator to decrease the oscillator frequency to the required data-acquisition rate. For instance, supposing a sensor signal bandwidth of 100 Hz, the oscillator frequency can also be decreased to 100 Hz. In that case, a clock frequency of 800 kHz would be enough to obtain 13 bits of resolution. It should be mentioned that due to different practical limitations, such as leakage current and reducing the values of on-chip capacitances, in most applications the oscillator frequency will be much higher than the sensor-signal bandwidth.

[1] Since we do not want to consume the whole error budget for the quantization noise, using a counting clock with a frequency of, for instance, 200 MHz will be better.

3-3 Circuit and system-level techniques

In this section, the major circuit and system-level techniques used in our interface are briefly explained.

3-3-1 Auto-calibration.

Auto-calibration is used to reduce the effects of systematic errors and of low-frequency noise. The principle of this technique can be understood by considering a linear system for which it holds that:

$$y = ax + b, \tag{3-2}$$

where x and y are the input and output signals of the system, respectively, and a and b are the transfer parameters of the linear system. The parameters a and b can be set by the designer. Therefore, it may have been said that by measuring the system output y and knowing the parameters a and b, the system input x can be extracted. However, problems occur when these parameters are not well-know or when they drift with time or temperature.

The undesired effects of transfer-parameter changes can be eliminated in various way, for instance by auto-calibration [3]. During auto-calibration, a sufficient number of reference signals $x_{\mathrm{ref},i}$ are measured in exactly the same way as the sensor signal x_{s} that has to be measured. For a linear system (Eq. 3-2), two reference signals are sufficient [3]. For two references and the sensor signal we have:

$$y_{\mathrm{ref},1} = ax_{\mathrm{ref},1} + b, \tag{3-3}$$

$$y_{\mathrm{ref},2} = ax_{\mathrm{ref},2} + b, \tag{3-4}$$

$$y_{\mathrm{s}} = ax_{\mathrm{s}} + b. \tag{3-5}$$

The sensor signal can be extracted as:

$$x_{\mathrm{s}} = M\left(x_{\mathrm{ref2}} - x_{\mathrm{ref1}}\right) + x_{\mathrm{ref1}}, \tag{3-6}$$

where for M it holds that:

$$M = \frac{y_{\mathrm{s}} - y_{\mathrm{ref1}}}{y_{\mathrm{ref2}} - y_{\mathrm{ref1}}}. \tag{3-7}$$

Note that M and consequently the derived values of x_{s} are independent of a and b and are thus immune from any variation in these parameters, as long as these values do not change during a single measurement cycle.

As a non-ideality, this system can show some nonlinearity. To minimize the effect of this nonlinearity it is better to select $x_{\mathrm{ref},1}$ and $x_{\mathrm{ref},2}$ to be almost equal to the minimum and maximum value of sensor signal. However, for the sake of simplicity, it might be convenient to select one reference to be zero ($x_{\mathrm{ref},1}$ =0) and the other one ($x_{\mathrm{ref},2}$ = x_{ref}) at the maximum value of the sensor signal. Therefore:

$$x_{\mathrm{s}} = Mx_{\mathrm{ref}}. \tag{3-8}$$

With auto-calibration, in addition to the effects of thermal drift and uncertainty in the parameters a and b, the effect of input-independent, switch-charge injections can also be removed.

3-3-2 Two-port measurement technique.

For the designer of capacitive sensor systems, understanding the two-port measurement technique [3] is very important. This technique is applied to eliminate the parasitic effects of connecting wires. In one version of this technique the effect of the parasitic series impedance of wires is eliminated, which is important for low-ohmic passive sensing elements, such as Pt100 resistors. In another version of the two-port measurement technique, the effect of parasitic shunting impedances of the connection wires is eliminated. This technique is important for high-ohmic passive sensing elements, such as our capacitive sensors. Figure 3-4 shows the concept of the later technique, which is used to measure a high-ohmic sensing element with impedance Z_x. The parasitic capacitances C_{p1} and C_{p2} of the cables of the sensing element connected to their shields can be much larger than the sensor capacitance, which with an impropriate connection can pose large problems. In the setup of figure 3-4, this problem is solved by using a low-ohmic excitation and a low-ohmic current read-out. The current through Z_{p1} does not effect the measurement of I_{sense}, while the current through Z_{p2} is negligible. Therefore, for the measurement of capacitive sensors, excitation with a low-ohmic voltage source and detection with a low-ohmic current meter should be chosen. In that case, the effect of parasitic capacitances of the connecting wires to their shields is eliminated.

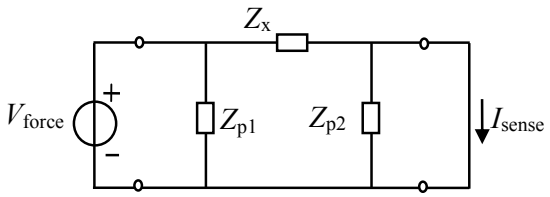


Fig. 3-4: The concept of the two-port measurement technique for high-ohmic sensor impedance Z_x.

3-3-3 Chopper.

Most sensor output signals are located in the low-frequency band, where many interfering signals such as op-amp offset, 1/*f* noise, and main-supply interferences are also located. A good way to separate the sensor signal from the above-mentioned undesired interfering signals is to modulate the sensor signal to a higher frequency, so that it can be processed to eliminate 1/*f* noise, offset and main-supply interference. After required processing, it can be demodulated back to the baseband frequency.

Modulation can easily be performed with choppers (Fig. 3-5). The two choppers act as a modulator and a demodulator, respectively. After the second chopper the original input signal is demodulated and amplified with a factor A, while the op-amp input noise and offset are chopped by the square wave signal $m(t)$ with chopping frequency f_{ch}=1/T. A low-pass filter removes these modulated offset at the chopper signals [11].

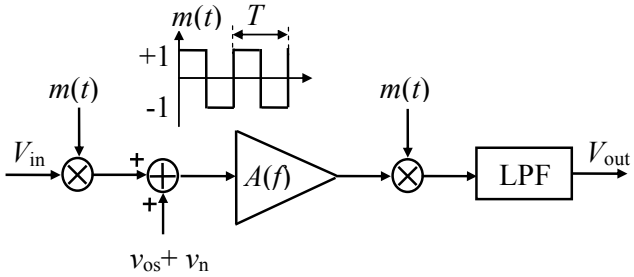


Fig. 3-5: A chopper amplifier.

In our design, we use a chopper signal that is fully synchronized with the input voltage V_{in}. As compared to the chopper in figure 3-5, this has the important advantage of no remaining ripple. The chopper applied has the additional advantage of using the (+ - - +) principle described in [8, 9]. The applied chopper will be described in section 3-4 and in depth in chapter 4, section 4.6.1.1.

3-4 The technique selected for the capacitive-sensor interfaces

From the two methods for indirect A/D conversion –sigma-delta and period-modulated methods– we selected the latter. Some of the reasons for this selection are:

1. Simplicity. In many modern control systems, there is at least one microcontroller; therefore, digitization and any further filtering can be performed without extra cost. It means that extra counter and filtering are not necessary in our interface.
2. Spread of power consumption. Usually, in order to eliminate noise, interference, etc., the analog signal needs to be converted to digital as soon as possible. In the system shown in figure 3-3, the analog-to-digital conversion takes place in the counter. In fact, before the counter, the period-modulated signal is a sampled analog signal. However, in the voltage domain, which determines its sensitivity to noise and interference, the signal is digital. Because the frequency of the signal is in the same range as the bandwidth of the sensor signal, with the maximum frequency of a few kHz, it can be transferred via a long cable without any problems. This is very important, for instance, in sensor heads which are very sensitive to thermal expansion [12]. In this case, the interface can be attached to the sensor head in order to minimize the effect of the parasitic capacitance of the sensor cable. The more energy-consuming part of the signal processing can be performed far away from the sensitive parts. In the case of a sigma-delta converter, sending high-frequency bit-streams via a long cable is not easy.
3. Compatibility with UTI [13]. Many users of UTI believe that the UTI is very user-friendly. However, its maximum data acquisition rate is only about 80 Hz. Moreover, the UTI is suited for neither grounded nor leaky capacitors. Last but not least, for many applications its resolution and linearity are not sufficient.

3-4-1 The structure of the interface

Figure 3-6(a) shows the block diagram of the interface which is based on figure 3-3 with an additional multiplexer to perform auto-calibration.

Figure 3-6(b) shows the interface output signal. Auto-calibration, a two-port measurement technique and chopping are used. Our work is based on the work presented in [8, 9]. However, we added dedicated front-ends for grounded capacitors (see chapter 8) and leaky capacitors (see chapter 7). In addition to that, in this project the interface properties were improved with respect to the features of noise, nonlinearity and measurement speed.

According to the three-signal auto-calibration technique (section 3-3-1), a single measurement cycle consists of three phases: two phases to measure the two reference capacitor C_{ref1} and C_{ref2}, and a third one to measure the sensor capacitor C_x. The time intervals T_{ref1}, T_{ref2} and T_x, are the output signals that correspond to the values of C_{ref1}, C_{ref2} and C_x, according to the equations:

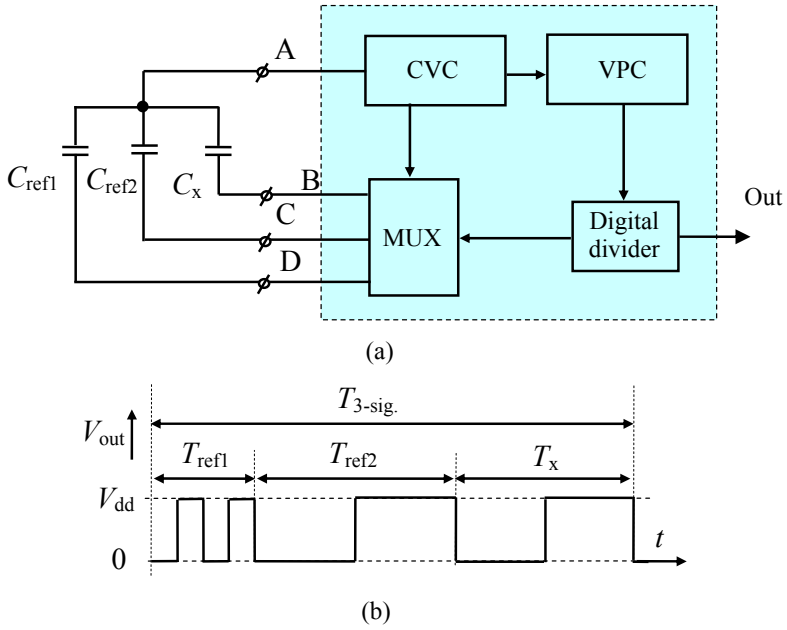


Fig. 3-6: (a) Simplified diagram of the interface structure for floating capacitors;
(b) the interface output signal [8, 9].

$$T_{ref1} = aC_{ref1} + b, \tag{3-9}$$

$$T_{ref2} = aC_{ref2} + b, \tag{3-10}$$

$$T_x = aC_x + b, . \tag{3-11}$$

By measuring the lengths of the three different periods, and knowing the values of the two reference capacitors, the value of C_x can be calculated according to the equation:

$$C_x = \left(\frac{T_x - T_{ref1}}{T_{ref2} - T_{ref1}} \right) \left(C_{ref2} - C_{ref1} \right) + C_{ref1} . \tag{3-12}$$

For identification purposes, time interval T_{ref1} is split into two short periods [8, 9].

Equations (3-9) to (3-12) are valid when the applied capacitance-to-time conversion is linear. To reduce the effect of resolution limitations caused by noise and interference, C_{ref1} and C_{ref2} should be selected to be close to the minimum and maximum value of the sensor capacitance C_x. However, for convenience and to eliminate an (expensive) reference capacitor, one reference capacitor is often set at zero.

3-4-2 Capacitance-to-voltage converter (CVC)

Figure 3-7(a) shows the CVC for floating capacitors [8, 9]. Some important signals are shown in figure 3-7 (b). The reasons for creating the output voltage as shown in figure 3-7(b) can be found in [8, 9].

In order to prevent the loss of any charge, S_r is opened before the occurrence of the transition in the drive voltage V_{drive}. In this CVC the drive voltage has two levels: 0 V and V_{dd}. During the sampling phase ph_1, S_r is closed, and the voltage $V_{drive} - V_{dd}/2$ is sampled on C_x. At the

end of phase 1 (ph_1), S_r is opened. Next, at the beginning of ph_2 (the charge-transfer phase), because the drive-voltage rise from 0V to V_{dd}, a charge C_xV_{dd} is pumped into C_f, which results in a voltage drop of $V_x = C_xV_{dd} / C_f$ at the output. The other parts of the CVC output voltage $V_{o\text{-}cvc}$ can be found in a similar way.

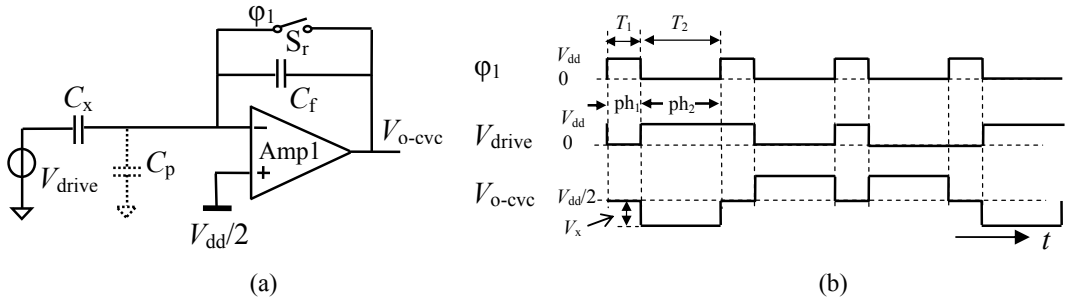


Fig. 3-7: (a) The CVC for a high-quality floating capacitor and (b) the related signals.

During ph_2, the DC voltage across C_x is not zero but $V_{dd}/2$, which causes the circuit of figure 3-7(a) to be sensitive to resistive leakage of C_x. In chapter 4, section 4-2 and in depth in chapter 7, we will show how this front-end can be modified to be leakage-immune.

Moreover, the presence of amplifier offset v_{io} will cause asymmetry in the CVC output voltage (Fig. 3-8); however, it can easily be proven that the peak-to-peak value of this output voltage is independent of amplifier offset. In section 3-4-3 it will be shown that the output of the VPC is proportional to the peak-to-peak of CVC output voltage.

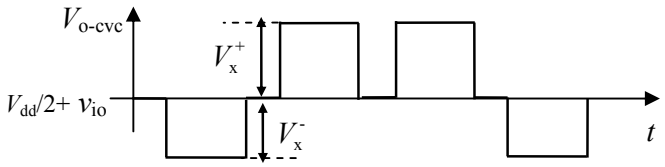


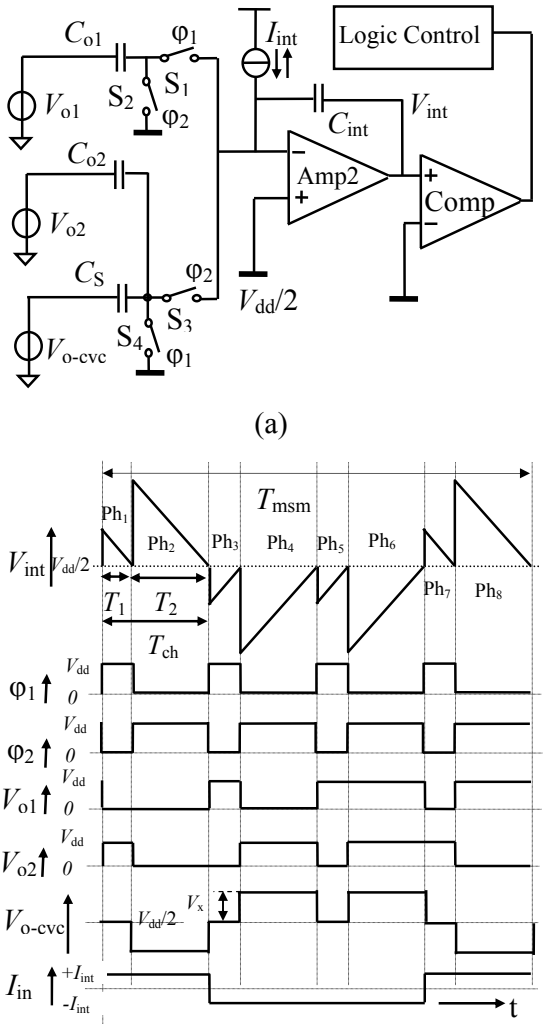
Fig. 3-8: The CVC output voltage at the presence of amplifier offset.

3-4-3 Voltage-to-period converter (VPC)

Figure 3-9(a) shows the principle of the voltage-to-period converter (VPC) [8, 9]. Figure 3-9(b) shows some important signals.

The voltages V_{o1} and V_{o2} are block-shaped and have voltage levels of 0 or V_{dd}. At the start of phase 1 (Ph1), the charge of $Q_1 = V_{dd}C_{o1}$ of C_{o1} is pumped into the integrator capacitor. Next, this charge is removed by integrating I_{int}. At the start of Ph2, the summed charge Q_2 of C_{o2} and C_s, which equals $V_{dd}\,C_{o2} + V_x\,C_S$, is pumped into the integrator capacitor. This charge is also removed by integrating I_{int}. This procedure is repeated with inverted polarities and current directions, which completely eliminates the effect of the offset voltage of Amp2. In this way the principle of a synchronous chopper is implemented according to the principles described in [8, 9]. Four of these events complete the measurement cycle within a time interval T_{msm} (Fig. 3-9(b)). This time interval represents the output signal of the converter, which amounts to:

$$T_{msm} = \frac{4\left(V_{dd}\left(C_{o1}+C_{o2}\right)+V_xC_S\right)}{I_{int}}. \qquad (3\text{-}13)$$



(a)

(b)

Fig. 3-9: (a) The voltage-to-period converter and (b) the most important signals.

In the case of an asymmetrical CVC output voltage, with the same analysis, it can be proven that:

$$T_{msm} = \frac{2\left(2V_{dd}\left(C_{o1}+C_{o2}\right)+\left(V_x^+ + V_x^-\right)C_S\right)}{I_{int}}, \tag{3-14}$$

where V_x^+ and V_x^- are shown in figure 3-8. It means that the VPC output is proportional to the peak-to-peak value of CVC output voltage.

The output signal of the capacitance-to-voltage converter (CVC) is also proportional to the supply voltage V_{dd} ($V_x = C_x V_{dd}/C_f$). In order to make the measurement time T_{msm} independent of the supply voltage, the integrating current I_{int} should also be proportional to the supply voltage.

3-5 Some important characteristics of the interface

Compared to other types of interfaces, the interface presented in figure 3-6 has some attractive features which are quite important for our universal-capacitive sensor interface. Two of them (simplicity and spread of power consumption) have already been discussed in section 4-4, some otheres will be summarized in this section.

3-5-1 Flexibility.

Flexibility is necessary to make the interface suitable for a wide range of applications. For instance, the interface needs to be flexible in terms of optimizing the range of the interface for capacitive sensors from 1pF to 1 nF; the data-acquisition rate from 20 Hz up to 10 kHz; for various types of external elements, for instance, grounded, floating or leaky capacitive sensor and also for different ranges of parasitic capacitance. In chapter 4 we will show how simple it is for the user to modify the designed interface for a specific application.

3-5-2 Stability.

Due to auto-calibration, the stability of the measurement is quite high. As a consequence, the output signal is immune to the effects of aging and changes of the interface temperature as long as these changes are not significant during the time $T_{3\text{-sig.}}$ (Fig. 3-6(b)) of a single measurement.

3-5-3 No error due to ripple.

In the chopper configuration of figure 3-5, the signal at the input of the low-pass filter is the amplified input signal with the modulated offset voltage on top. A low-pass filter (LPF) is used to remove the modulated offset. However, depending on the ratio of the chopping frequency and the bandwidth of the LPF, part of the modulated offset will appear at the output as ripple. In many applications, decreasing this ripple is an important issue and several techniques to reduce its amplitude can be found in the literature [14, 15]. However, in our system the chopper action is completely synchronized with the excitation signal so that no residual effects of ripple remaining. When, for instance, the amplifier offset decreases the time interval in phase 1 and phase 2, it will increase the time interval the same amount in phase 3 and phase 4. Therefore, the sum of time interval in phase 1 to phase 4 is completely offset-free. More details will be discussed in chapter 4, section 4-6-1-1.

3-5-4 No error due to clock feedthrough and switch-charge injection.

In the next discussion we deal with the effects of switch-channel charge injection, although the discussion is also valid for switch-clock feedthrough [16]. Moreover, since our discussion is valid regardless of the switch type (NMOS, PMOS or CMOS switch), we do not specify the polarity of the charges.

In most switched-capacitor circuits, the effect of switch-charge injection is an important issue. For instance in a typical chopper, as depicted in figure 3-5, there is some error due to residual offset which originates from a mismatch between the input-chopper switches. Therefore, the charge injections do not fully compensate each other. This causes a spike voltage, as shown in figure 3-10 at the input of the LPF (Fig. 3-5) [17]. The average of these spikes appears as residual offset at the output of the LPF. The amount of this residual offset depends on the

level of mismatches and also on the source impedance. This effect causes the residual offset of the chopper amplifiers.

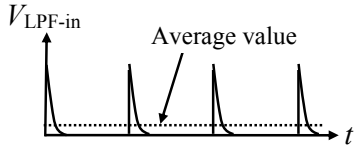


Fig. 3-10: The spike voltage at the input of LPF caused by clock feedthrough and switch-charge injection.

The chopper in our system, which is based on the synchronous (+ - - +) principle described in [8, 9], is implemented by inverting the drive voltage and integrator current. It has been shown [8, 9] that this way of chopping in combination with auto calibration removes any residual effect of clock feedthrough and switch-charge injection of all switches in our interface.

For instance, when the reset switch S_r in figure 3-7(a) is switched to the OFF position, some charge is pumped into the feedback capacitor C_f. When S_r is ON, the channel voltage is always $V_{dd}/2$. Therefore for all switching events in the OFF position, the switch charge injection is the same. Therefore, this effect cannot change the peak-to-peak value of the CVC output V_+ - V_- (Fig. 3-11). Consequently, this effect is removed by chopper. Moreover, because the situation is exactly the same for the three different input capacitors C_{ref1}, C_{ref2} and C_x, any residual effect will be removed by auto-calibration.

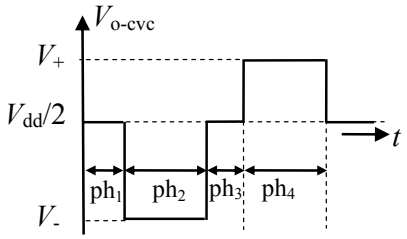


Fig. 3-11: The CVC output voltage, at the presence of clock feedthrough and switch-charge injection of reset switch S_r.

For switches S_1 to S_4 in the VPC (Fig. 3-9(a)) it can be shown that there is a first-order compensation for the charge injection of switches S_1 and S_3. However, due to mismatch of these two switches, there will be some residual charge injection in each phase. If we consider one complete measurement cycle T_{msm}, the total charge pumped to the negative input of the CVC amplifier from each of these switches is compensated by the amount of charge drawn from this node by the same switch at the opposite transition. In other words, the switch-charge injection of these two switches will not affect the measurement cycle T_{msm}, in principle. For switches S_2 and S_4, however, the conditions are different. Because at the moment of switching ON, the required channel charge is provided by the bias voltage $V_{dd}/2$, while at the moment of switching OFF, the channel charge will be pumped to the right side of the capacitors C_{o1}, C_{o2} and C_S, and then to the integrator capacitor C_{int}. Since these charges are always in the same direction, their effect is removed by the chopper, and further suppressed by auto-calibration.

3-6 Conclusion

In this chapter we showed two different methods of capacitance measurement: the sigma-delta method, and the period-modulated or oscillator-based method. It was shown that the period-modulators have the attractive features of being simple and flexible. Furthermore, a number of important measurement techniques to be applied for high-performance sensor interfaces were briefly presented. These techniques include auto-calibration, two-port method and chopping. It was shown that the chopper action is synchronized with the input voltage, which enables removal of the offset voltage effects of the op-amp without leaving any ripple. Moreover, it appears that the effects of switch-charge injection are fully eliminated by the combined effects of chopping and auto-calibration.

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CHAPTER 4

A Universal Interface for Capacitive Sensors

4-1 Introduction

To design an interface for capacitive sensors the requirements and constraints related to the proposed applications should be taken into account. For the interface, the sensor element is an external component. However, the electrical properties of the element interact with those of the interface itself. For instance, depending on the application, capacitive sensors can be electrically floating or grounded [1]. They can show pure capacitive behavior or have resistive leakage [2]. Their values can be in a wide range from less than one pF up to hundreds of pF or even a few nF. In some cases their values can change very fast, and in other cases their values are semi-static. For different applications, the parasitic capacitances of the connecting wires can also be very different. Using an interface which could simply be optimized for the aforementioned applications would be a cost-effective solution.

The universal interface for capacitive sensors is designed to cover the following selected group of capacitive sensors:

1. Capacitive sensors with electrically-floating electrodes.
2. Capacitive sensors with one grounded electrode.
3. Leaky capacitive sensors.
4. Capacitive sensors with a rapid response time and a high accuracy.

One of the target specifications for this interface is that it should be possible to set the range at any value up to 1 nF. For specific modes, it should be possible to vary the measurement time from about 100 μs to 50 ms. Furthermore, for other modes it is preferable that cable lengths up to 30 meters can be handled.

For a specific sensor system, the error budget can be divided over different error sources such as nonlinearity, limited resolution, offset, finite settling time, etc.. However, when designing a universal interface, making an error budget is not possible. For the main part, this is because parts of the errors originate from the sensor side and the chip-designer does not know the sensor details. Even when the sensor is ideal, before registering the sensor signal characteristic, such as the dynamic range, the bandwidth, etc., it is not possible for the interface designer to make an error budget for the whole system.

There are different sources of error [Appendix A]. In our design, ,error sources such as gain errors, offset errors, drift errors, and many others are suppressed significantly using auto-calibration. However, nonlinearity errors and resolution errors cannot be suppressed by this technique. Moreover, in capacitance measurements, the effect of PCB parasitic capacitances at the connection terminals of the capacitors can cause gain and offset errors which cannot be suppressed by auto-calibration. This is because during an auto-calibration cycle, these parasitic capacitances are not constant. Therefore, as will be shown in this chapter, the three main sources of error are nonlinearity, noise and parasitic capacitances at the connection terminals. It should be mentioned that in many applications we are not interested in absolute accuracy. In such cases, offset errors or gain errors are not important anymore.

Our work is based on the work presented in [3, 4]. However, we added dedicated front-ends for grounded capacitors and leaky capacitors. Moreover, in this work we focused on minimization of the three aforementioned sources of error independently: nonlinearity error, resolution error and error caused by PCB parasitic capacitances.

Section 4-2 discusses the interface architecture. Section 4-3 discusses various options to change the range of the interface in order to match it with the range of sensor capacitances. Section 4-4 deals with issues such as the optimal frequency value of the excitation signal to achieve the fastest measurement while maintaining the systematic error in range. Section 4-5 focuses on the requirements for the comparator in the applied relaxation oscillator. An extended noise analysis of the interface is presented in section 4-6. Section 4-7 discusses the errors caused by PCB parasitic capacitances and a method to reduce these errors. The nonlinearity errors are discussed in section 4-8.

4-2 The interface

Figure 4-1 shows the block diagram of the interface which is based on Figure 3-6(a). The three main differences of this structure compared to the general structure shown in Figure 3-6(a) are:

1. There are three different CVCs for high-quality floating capacitive sensors, floating leaky capacitive sensors, and grounded capacitive sensors;
2. The frequency of the oscillator VPC can be set by the user;
3. The divider can be programmed.

And of course we have a control unit which accepts different digital input from the user for proper setting of the interface for that specific application. The control unit contains some logic to provide different signals, such as φ_1, φ_2, V_{o1}, V_{o2}, with the switching of I_{int} (Fig. 3-9). At the command of the user, the control unit selects the proper front-end and then powers-down the others. To set the measurement speed to correspond to the sensor signal bandwidth at each measurement phase, the frequency of the output signal is divided so that the time interval T_{msm} of a specific phase is multiplied by $N=2^n$. In our design, the value of n can be set by the user in four values 1, 3, 5 and 7, which correspond to *very fast*, *fast*, *slow* and *very slow* measurement modes, respectively.

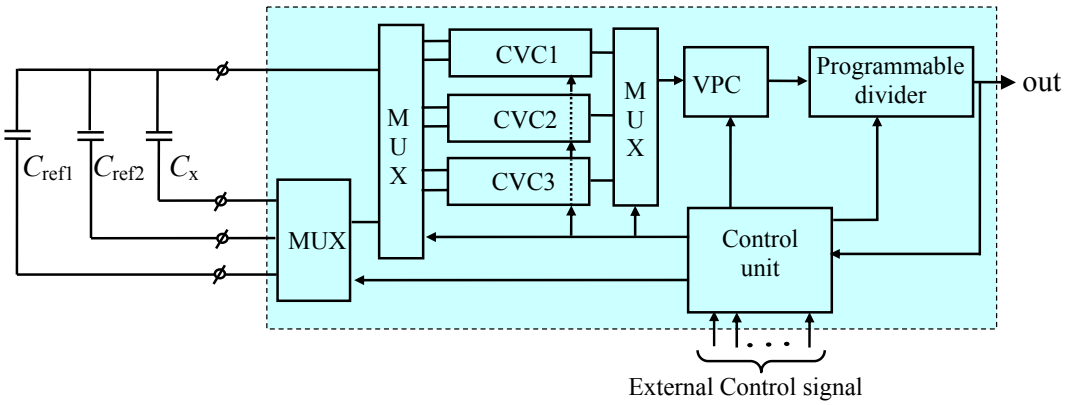

Fig. 4-1: The main structure of the interface for floating capacitor.

For leaky capacitive sensors it is possible to modify the drive voltage so that the DC voltage across the sensor capacitance equals zero during the charge-transfer phase, which would make the modified circuit immune to the leakage. Figure 4-2 shows the CVC, which is exactly the same as figure 3-9 with a modified drive [5, 6].

In this case, the sampled voltage on C_x, instead of being V_{dd}, is $V_{dd}/2$. Therefore, the resolution is one bit lower. This is the main reason that we use this modification only in the mode for leaky capacitors. The complete analysis of a leakage-immune measurement for capacitive sensors is presented in chapter 7.

Due to the parasitic capacitances of the connecting cables and their shielding, the sensor has parasitic capacitances. Figure 4-3 shows these parasitic capacitances for a floating and grounded capacitive sensor with capacitance C_x.

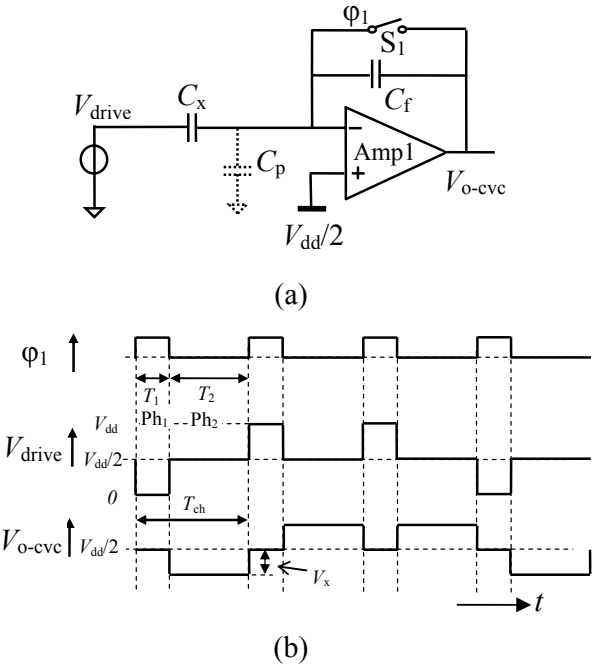

Fig. 4-2: (a) The CVC for leaky floating capacitor and (b) the related signals.

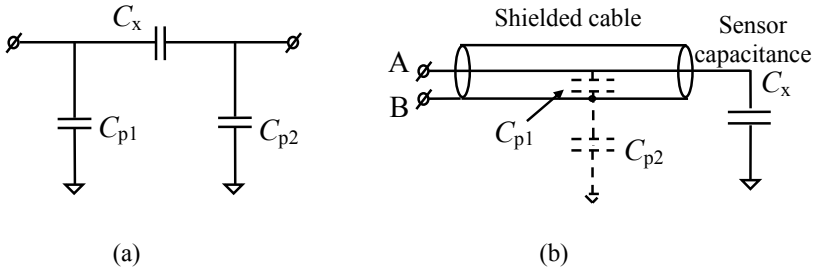

Fig. 4-3: The sensor capacitance with parasitic capacitances for (a) floating and (b) grounded sensors.

In order to measure a floating capacitor C_x that is independent from the influence of parasitic capacitances C_{p1} and C_{p2}, the sensor can be driven by a voltage source and the sensor current can be read with a low-ohmic current meter (see the two-port measurement, chapter 3, section 3-3-2).

The two-port measurement method cannot be applied to a grounded capacitive sensor. When the shield of the connecting cable (Fig. 4-3(b)) is simply connected to ground, then the capacitance from the core to the shield C_{p1} shunts the sensor capacitance C_x. It can be argued that when the value of this capacitance is constant, any change in C_x appears in node A on the other side of the cable. However, this causes several problems. The most important problems are: a) the value of C_{p1} is not well-defined and depends on temperature, mechanical stress and movement, which makes the measurement highly inaccurate; b) usually C_{p1} is much larger than C_x, therefore a relative change of C_x would cause a much smaller relative change of $C_{p1}+C_x$, which would decrease the resolution; and c) the system always needs to be recalibrated for different lengths of cables. The standard way to solve these problems is to use active guarding [7]. In this method, the core voltage is fed back to the shield using a buffer amplifier. Instead of feedback, feed-forward can also be applied for active guarding. In this specific case, applying feed-forward has the advantage of simplicity and better stability. In chapter 8, the various techniques for active guarding will be explained in more detail. In the remainder of this chapter, the discussion will be focused on high-quality floating capacitive sensors.

4-3 Capacitance range

By looking at the CVC (Fig. 4-2(a)), it is clear that the range of the input capacitance can be changed by changing the feedback capacitor C_f. The next stage–the voltage-to-period converter–can be optimized independent from the input-capacitance range. An additional off-chip capacitor can be used for this stage, which might not initially seem user-friendly, but has the following distinct advantages:

1. From figure 4-2 it is clear that in the case of a rail-to-rail CVC amplifier, it should hold that $C_f > 2C_x$. However, for a large value of the sensor capacitor, C_f becomes too big to be integrated on-chip. Instead of using an off-chip capacitor we can reduce the drive voltage [6]. However, this would decrease the signal-to-noise ratio and therefore decrease the resolution.
2. In the case of on-chip capacitors C_f, extra pins are needed to select the discrete capacitance ranges. In practice, we can only select a few discrete ranges, which means that usually we cannot use the whole dynamic range. However, if we use an off-chip capacitor, then C_f can be selected based on the actual value of $C_{x\text{-}max}$ so that the whole dynamic range can be used.

Now, the reason for using a capacitor-to-voltage converter prior to the voltage-to-period converter can easily be explained. In principle, converting the capacitor to time can be very straightforward. For instance, in the voltage-to-period converter (Fig. 3-9(a)) we can replace the sampling capacitor C_S with input capacitor C_x and drive it with the same voltage as we drive the capacitor C_{o2}. However in that case, to reconfigure the circuit for a specific input capacitance range, the capacitors C_{o1}, C_{o2}, C_{int} and the current source I_{int} should be changed accordingly. For a universal interface, this is the main reason to use a CVC prior to the VPC. Yet, for specific cases, the second approach could have advantages with respect to power consumption and linearity. In chapter 6, these two advantages are explained in more detail.

Using an off-chip capacitor for C_f also has two disadvantages:

1. The parasitic capacitance C_{pf} of the PCB wiring. Actually the effect of this parasitic capacitance can be removed by auto-calibration. However, since the quality of this parasitic capacitance, which depends on the PCB material, is rather poor, this parasitic capacitor can cause problems. For instance, the dielectric absorption of this

parasitic capacitance [8] can have different effects on the output period for C_{ref1}, C_{ref2} and C_x. Consequently, auto-calibration does not fully eliminate its effect.

2. The effect of the nonlinearity of the external capacitor on the interface characteristics. In the case of the same capacitor as in C_f and C_S (Fig. 4-2(a) and 3-11(a)), their voltage dependency can fully cancel each other, but in the case of external capacitor as C_f, their different voltage dependency can create nonlinearity. This is discussed with more detail in section 4-8-2.

The final error caused by the dielectric absorption of the parasitic capacitance of the PCB depends on the ratio of this parasitic to the main capacitor, C_{pf}/C_f. Since the value of parasitic capacitance is almost independent from C_f, the error is more significant for a smaller C_f. Therefore, there is already an on-chip capacitor of 3.3 pF used as C_f. This means that for an input capacitance range of up to 1 pF, there is no need for an external capacitor, thus the two pins of feedback capacitor can be disconnected from the PCB. However for a larger input capacitance range we need to add an extra external capacitor as C_f. The effect of PCB parasitic capacitance can be decreased by using a better quality (i.e. more expensive) dielectric material.

Designing a high-performance CVC amplifier for a wide range of input capacitances, for instance from 1 pF to 1 nF, is almost impossible. Therefore, in our design we have divided the whole range into two subranges: C_x < 33pF and C_x < 1nF. These two subranges can be selected by a pin called CRS.

4-4 Oscillator frequency

As shown in figure 4-2(b), different signals and different frequencies can be distinguished. The highest frequency is that of φ_1, which equals $1/(T_1 + T_2)$. This frequency is used for the chopper, which is called the chopper frequency f_{ch}, while the corresponding period time $T_{ch} = T_1 + T_2$ is called the chopper period. The chopper frequency is input-dependent. For zero input and assuming that $C_{o1} = C_{o2} = C_o$, the chopper frequency $f_{ch\text{-}0}$ amounts to:

$$f_{ch\text{-}0} = \frac{1}{2T_1} = \frac{I_{int}}{2V_{DD}C_o}. \qquad (4\text{-}1)$$

The interface is designed in such a way that, at the beginning of time interval T_1, with V_{dd} = 5 V, (Fig. 3-9(b)) the voltage step in V_{int} is 0.5 V. Furthermore, at the beginning of the time interval T_2, this step is 2 V for the maximum input voltage $V_{o\text{-}cvc,max}$. With these voltage steps, linearity is guaranteed along with an acceptable dynamic range. In this condition the time interval T_2 can change from its minimum value, which is equal to T_1, to its maximum value, which is four times the value of T_1. Therefore, the chopper frequency can change from $f_{ch\text{-}0}$ for zero input, to the $0.4\,f_{ch\text{-}0}$ for maximum input.

Increasing the chopper frequency f_{ch} decreases the measurement time. Especially for very fast measurements, this is a desirable feature. Moreover, increasing the chopper frequency results in a better suppression of flicker noise and mains interference.

In switched-capacitor circuits, the maximum frequency is limited by the required accuracy [9]. If the system requires an m-bit performance, then the settling error at the output must be less than half an LSB. This requires that the condition:

$$e^{-T_2/\tau_{CT}} \le 2^{m+1}, \qquad (4\text{-}2)$$

must be met, which is equivalent to:

$$T_2 \geq (m+1)\tau_{CT} \ln 2, \tag{4-3}$$

where τ_{CT} is the charge-transfer-time constant. It should be mentioned that three-signal auto-calibration compensates for a part of the settling error. However, for offset, reference and input measurements, the time intervals T_2 are different, meaning that this compensation cannot be guaranteed. Therefore, the positive effect of auto-calibration on the settling error is ignored.

Since T_2 depends on input capacitance C_x, equation 4-3 should be valid for the minimum value of T_2, which is equal to T_1. Therefore, it should hold that:

$$T_1 \geq (m+1)\tau_{CT} \ln 2\,. \tag{4-4}$$

When the amplifiers in the CVC and in the integrator have the same open-loop bandwidth, then due to the parasitic capacitances of the sensor and the connecting cables, the CVC will limit the upper-limit of the frequency. To calculate the charge-transfer-time constant let us consider the circuit of figure 4-4, which shows the relevant part of the CVC. In this figure, C_L is the input capacitance of the next stage, which is the sampling capacitor of the VPC, and C_p is the parasitic capacitance of the sensor and/or cable on the amplifier side. On the drive side, the effect of the sensor parasitic capacitance can be eliminated simply by using an excitation voltage source with low output impedance.

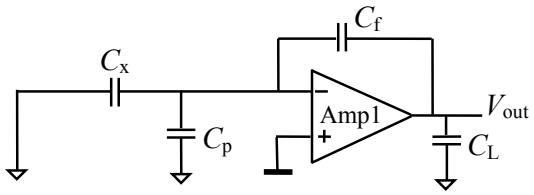

Fig. 4-4: The relevant part of the CVC to calculate the charge-transfer-time constant.

When the CVC amplifier is implemented with a one-stage OTA, the charge-transfer-time constant $\tau_{CT,OTA}$ will be:

$$\tau_{CT,OTA} = \frac{C_f C_{in} + C_f C_L + C_{in} C_L}{g_m C_f}, \tag{4-5}$$

where $C_{in} = C_p + C_x$ and g_m is the transconductance of the OTA.

As an alternative, the amplifier could be implemented with an op-amp consisting of an OTA with a buffer stage. This amplifier can be modeled as shown in figure 4-5. In this case, for the CVC charge-transfer-time constant $\tau_{CT,Op\text{-}Amp}$, it can be found that:

$$\tau_{CT,Op\text{-}Amp} = \frac{(C_f + C_{in})C_C}{g_m C_f}, \tag{4-6}$$

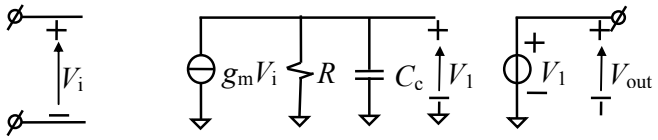

Fig. 4-5: Op-amp structure with an OTA followed by a voltage follower.

where C_c is the internal compensation capacitor. The value of C_c should be selected in such a way that the amplifier remains stable for the whole range of the input capacitors C_x and C_p and therefore also C_f.

When comparing the two types of amplifiers, in our design and for any range of input capacitances ,we have:

$$\tau_{CT,op\text{-}amp} \leq \tau_{CT,OTA}. \tag{4-7}$$

Therefore, for the CVC we chose to use an op-amp. The shortest time constant is obtained for C_p = 0pF. However, in practical cases, the parasitic capacitance C_p will have a value between a few tens of pF to a few hundreds of pF. Therefore, for small sensor capacitances with maximum values $C_{x,max}$ up to a few pF, the $C_p/C_{x,max}$ ratio will be in the range of about 10 to 100.

When $10C_{x,max} < C_p < 100C_{x,max}$, and supposing that $C_f = 2C_{x,max}$, with equation 4-6 it is found that:

$$6.5\frac{C_c}{g_m} \leq \tau_{CT(op\text{-}amp)} \leq 51.5\frac{C_c}{g_m}. \tag{4-8}$$

For interfaces for the case of UTI [10], which its frequency cannot be optimized for the actual value of the parasitic capacitance C_p, the worst case should be considered. For such interfaces with, for instance, a 14-bit accuracy, combining equations 4-4 and 4-8 yields the condition:

$$T_1 \geq 85/f_{u\text{-}CVC}, \tag{4-9}$$

where $f_{u\text{-}CVC}$ is the unity-gain bandwidth of the CVC amplifier for which it holds that:

$$f_{u\text{-}CVC} = \frac{g_{m\_CVC}}{2\pi C_c}. \tag{4-10}$$

Example 4-0: When f_u=10 MHz, equation 4-9 yields $T_1 > 8.5\mu s$. In this case, in the very fast mode (N=2), and when $T_2 = 4T_1$ for both the reference and the input measurement, one measurement including three-signal auto-calibration will take about 0.8 ms. However, if the user can select a larger integration current (Fig. 3-9(a)), then in the case of a small parasitic capacitance $C_p = 10C_{x,max}$, the measurement can be executed about eight times faster. In this case, a measurement can be completed within 100 μs, which is our target for the very-fast mode.

The integrator should have enough bandwidth to allow a fast enough speed. However, when selecting a lower integration current, one might prefer to limit the integrator bandwidth accordingly in order to eliminate the out-of-band noise. However, in our design, out-of-band noise is filtered instead by a band-limited comparator.

4-5 The band-limited comparator

In order to find the requirement of the comparator in our system (Fig. 3-9(a)), some general points about the relation of noise and comparator are discussed here, while the details of this analysis will be presented in Section 4-6-1-3. Figure 4-6 shows the integrator output voltage and corresponding comparator output voltage for the moment that the integrator output voltage crosses the noisy comparator threshold voltage.

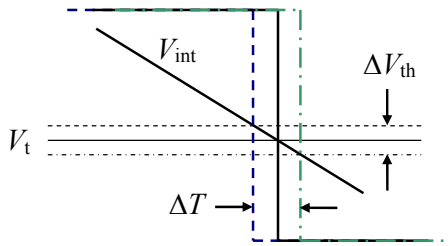

Fig. 4-6: Jitter caused by the noise of comparator.

It simply can be seen that the jitter ΔT, which is caused by the comparator noise, is inversely proportional to the slope in the integrator output voltage. Accordingly, the jitter J_{vnc} caused by the equivalent input noise voltage v_{nc} of the comparator can be calculated as:

$$J_{vnc} = \frac{v_{nc}}{\partial V_{int}/\partial t} = \frac{v_{nc} C_{int}}{I_{int}}. \tag{4-11}$$

A standard comparator is usually thought of as cascaded wide-bandwidth, high-gain input stages and a Schmitt trigger. The first gain stage of a cascaded amplifier typically dominates its input-referred noise and sets the comparator noise bandwidth. The input-referred noise of such an amplifier can be rather large [11]. It can be so high that in our application it can dominate the noise performance of the interface [12, 13].

In our interface, comparator delay is not a big issue. For the main part, the effect of comparator delay is removed by auto-calibration. For this reason, there is no need for a fast comparator. Therefore, instead of using a standard comparator, a preamplifier with limited and controllable bandwidth followed by a Schmitt trigger is used (Fig. 4-7). When the preamplifier has enough gain, which is the case in our design, the Schmitt trigger noise is negligible. The delay caused by the Schmitt trigger is much less than that caused by the preamplifier. Therefore, the delay of Schmitt trigger is negligible.

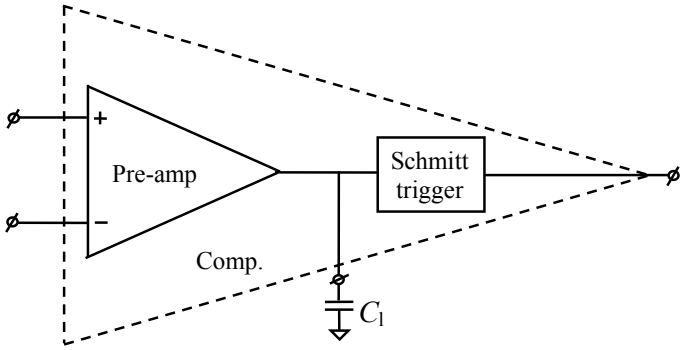

Fig. 4-7: A comparator with limited and controllable bandwidth.

Further on in this section it is shown that the delay time of the comparator depends on the slope of the input signal and the comparator bandwidth. Therefore, the comparator delay is constant for all phases of our measurements. Figure 4-8 shows the integrator output voltage for two cases: with an ideal comparator and with a comparator with a considerable delay.

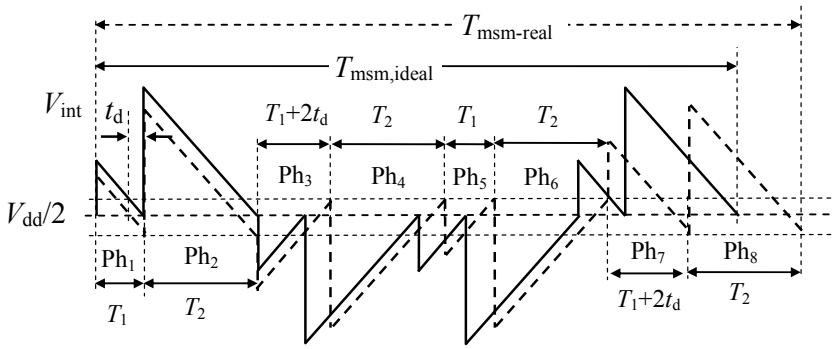

Fig. 4-8: The integrator output voltages in two cases (a) with an ideal comparator (solid line) and (b) with a comparator with a considerable delay (dashed line).

In figure 4-8, a notable phenomenon can be observed, which happens in phases 3 and 7. In these two phases the time is expanded by a value of $2t_d$, where t_d is the delay of the comparator with the limited bandwidth. For the other phases, the comparator delay had no effect on the time intervals. Altogether, in the case of a comparator with limited bandwidth, the time interval of a measurement cycle is $4t_d$ longer than in the case of an ideal comparator. Since t_d just depends on the input slope and not on the amplitude, applying three-signal auto-calibration will eliminate its effect (which can be concluded from Eq. 3-11).

Yet, the comparator delay can cause several other problems. First of all, by increasing this delay, the oscillator cannot continue its oscillation. To understand this, consider the case that $t_d > T_1$, (Fig. 4-9(a)), in which case, for instance, in phase 5 after the jumps in the integrator output, the value of the oscillator does not reach the threshold voltage of the comparator (Fig. 4-9(a)) and the oscillator stops oscillating. Figure 4-9(b) shows the case that $T_1/2<t_d < T_1$, where the integrator output voltage crosses the threshold voltage $V_{dd}/2$ of the comparator, but the comparator does not have enough time to respond after the next crossing.

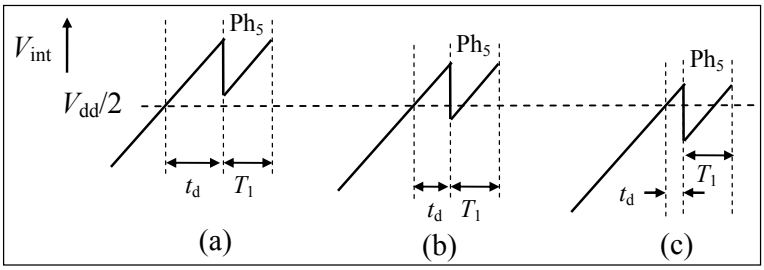

Fig. 4-9: The integrator output voltages around phase 5, in three cases: (a) $t_d > T_1$, (b) $T_1/2<t_d < T_1$, and (c) $t_d <T_1/2$.

Therefore the condition for oscillation is (Fig. 4-9(c)):

$$t_d \le \frac{T_1}{2}, \tag{4-12}$$

For oscillation, the condition $t_d < T_1/2$ is sufficient. However, there is still another feature to be considered: In section 4-6-1-1, it will be shown that the best low-frequency suppression is obtained if the four consecutive samples (ph_1+ph_2, ph_3+ph_4, ph_5+ph_6, ph_7+ph_8) occur in equal time intervals. However, the delay of the comparator clearly makes these time intervals different and therefore decreases the low-frequency suppression of the interface.

For further consideration it is useful to explore the relation between the comparator bandwidth and its delay. In a standard comparator this relation can be very complex. This is because usually the bandwidth is mainly determined by the first stage, while the delay is determined by all stages including digital ones. However, in our case, since both the delay and bandwidth is determined by the first stage, finding this relation is straightforward.

Figure 4-10 shows the case in which initially the integrator output voltage is lower than the threshold voltage of the comparator. When the integrator output voltage is still far from the comparator threshold voltage, the output voltage of the preamplifier (Fig. 4-7) is in the LOW state. However, when the integrator output voltage approaches the comparator threshold-voltage, the preamplifier arrives in its linear region. With a high-gain preamplifier, the transition starts at $v_{\text{i-pa}} = V_{\text{in}} - V_{\text{th}} \approx 0$ V.

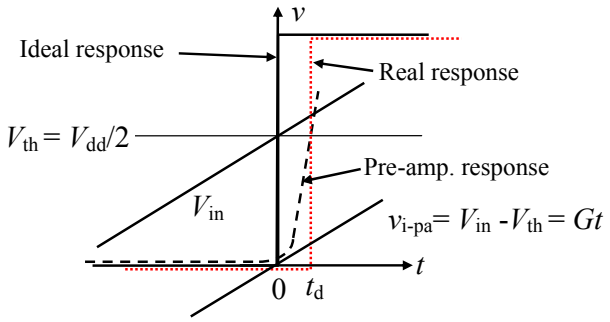

Fig. 4-10: The transient moment at the preamplifier output.

When we suppose that the preamplifier is a one-pole system (Fig. 4-11), then its ramp response can be calculated as:

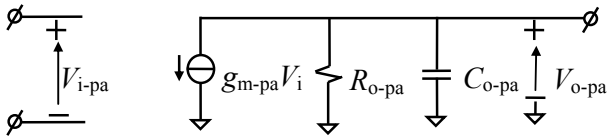

Fig. 4-11: The preamplifier of the comparator.

$$V_{\text{o-pa}}(\text{s}) = \frac{a_{\text{0-pa}}}{1 + \text{s}\tau_{\text{pa}}} V_{\text{i-pa}}(\text{s}), \tag{4-13}$$

where,

$$\tau_{\text{pa}} = R_{\text{o-pa}} C_{\text{o-pa}} \tag{4-14}$$

$$a_{\text{0-pa}} = g_{\text{m-pa}} R_{\text{o-pa}} \tag{4-15}$$

$$v_{\text{i-pa}}(t) = Gt\ \text{u}(t) \quad \Rightarrow \quad V_{\text{i-pa}}(\text{s}) = \frac{G}{\text{s}^2}, \tag{4-16}$$

where G = $\delta v_{\text{i-pa}}/\delta t$, and u($t$) is the unit function. From these equations, for the preamplifier output voltage $v_{\text{o}}(t)$ it is found that:

$$v_{\text{o-pa}}(t) = a_{0-pa} G\left(t - \tau_{\text{pa}}\left(1 - \text{e}^{-t/\tau_{\text{pa}}}\right)\right). \tag{4-17}$$

For $t_d << \tau_{pa}$, which is the case in our design, equation 4-17 can be approximated as:

$$v_{o\text{-}pa}(t) = \frac{a_{0\text{-}pa} G}{2\tau_{pa}} t^2. \tag{4-18}$$

Therefore, for the case of $t_d << \tau_{pa}$, the comparator acts as an integrator [11].

The time delay t_d can be extracted from the following calculation:

$$v_{o\text{-}pa}(t_d) = \frac{a_{0\text{-}pa} G}{2\tau_{pa}} t_d^{\,2} = V_{dd}/2. \tag{4-19}$$

The result is:

$$t_d = \sqrt{V_{dd}/\omega_{u\text{-}pa} G}, \tag{4-20}$$

where

$$\omega_{u\text{-}pa} = \frac{a_{0\text{-}pa}}{\tau_{pa}}. \tag{4-21}$$

The slope of the preamplifier output voltage at the time of threshold crossing can be found as:

$$\left.\frac{\partial v_{o\text{-}pa}(t)}{\partial t}\right|_{t=t_d} = a_0 G\left(1 - e^{-t_d/\tau_{pa}}\right) \approx a_0 G\, t_d/\tau_{pa} = \sqrt{\omega_{u\text{-}pa} G V_{dd}}. \tag{4-22}$$

Example 4-1: With V_{dd}= 5 V, T_1 = 5 µs and G =10^5 V/s, and with equation 4-12 we find that for the preamplifier it is necessary that t_d < 2.5 µs. According to equation 4-20, this yields f_u > 1.3 MHz. If f_u = 2 MHz, then from equations 4-20 and 4-22 it is found that t_d = 2 µs and $\partial v_o(t)/\partial t = 2.5\times10^6$ V/s. These calculations are valid if and only if $t_d << \tau_{pa}$. If f_u = 2 MHz and, for instance, a_0 =200, with equations 4-21 we find that τ_{pa} = 16 µs. These figures show that in this case we can apply the approximation.

4-6 Noise analysis of the interface

In this sub-section the noise analysis of the interface is presented. In many electronic systems, due to the presence of amplification of the first stage, only the noise of this first stage is important. However, in our interface, which is shown in figure 4-12, the drive voltage of the first stage has the amplitude of the supply voltage V_{dd}. Therefore not only there is no voltage amplification in the first stage (CVC), but there is even some attenuations. Additionally, it appears that not only the noise of the CVC amplifier, but also the the integrator amplifier (Amp2), the comparator, the noise of bias voltage (V_{dd}/2), the integrator-current source, and even kT/C, noise caused by the switched capacitor can be important (Fig. 4-12) for the overall noise performance of the interface. Yet, for the case that the parasitic capacitance C_p of the sensor is very large ($C_p >> C_x$), the noise of the CVC amplifier will dominate the overall noise performance of the interface.

For the various noise sources the interface acts as a filter with different bandwidths. For the noise analysis, understanding these filtering effects is very important. Therefore, we will discuss the different filtering effects of the chopper, the integrator, the band-limited comparator and the effect of applying auto-calibration.

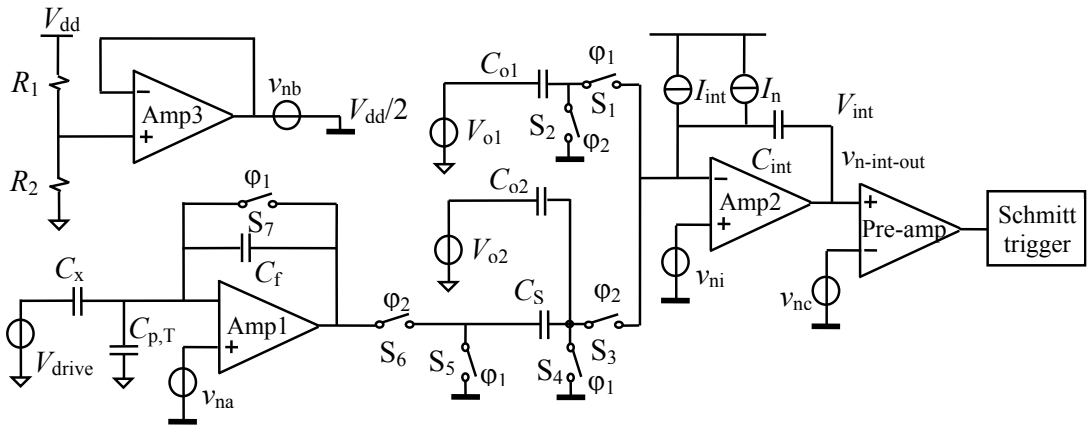

Fig. 4-12: The related part of the interface for the noise analysis.

With respect to the noise bandwidth, three different categories of noise can be distinguished in our interface as follows:

1) The noise of integrator-current source with $B_n = 1/T_{out}$, where T_{out} represents the output periods T_{off}, T_{ref} or T_x (Fig. 3-6(b)).
2) The sampled noise with $B_n = 1/2T_{ch}$ (Fig. 4-2(b)).
3) The noise in the continuous state with $B_n >> 1/2T_{ch}$.

In section 4-6-1 we will explain different filtering effects and then in section 4-6-2 we will analyze the effect of different noise sources based on their bandwidth and the filtering which is applied to them.

4-6-1 Filtering effects in the interface

4-6-1-1 Filtering effect of the chopper with frequency divider

The frequency response $H_1(f)$ of the applied chopper for each measurement cycle T_{msm} can be found to be:

$$H_1(f) = \sum_{k=0}^{3} a_k e^{-2\pi j f T_{ch}} \tag{4-23}$$

where $T_{ch} = T_1 + T_2$ (Fig. 3-9(b)) is the chopper period and a is a vector with the value of (1, -1, -1, 1). Taking into account the applied frequency division, the output period is the summation of 2^n measurement cycles. The frequency response $H_2(f)$ of the chopper with frequency divider is:

$$H_2(f) = \sum_{k=0}^{2^{n+2}-1} c_k e^{-2\pi j k f T_{ch}}, \tag{4-24}$$

where c is a vector with the value of:

$$c = [1,-1,-1,1,1,-1,-1,1,...,1,-1,-1,1]. \tag{4-25}$$

The absolute value of $H_2(f)$ versus the normalized frequency fT_{ch}, for n =1 and n =3, is depicted in figure 4-13.

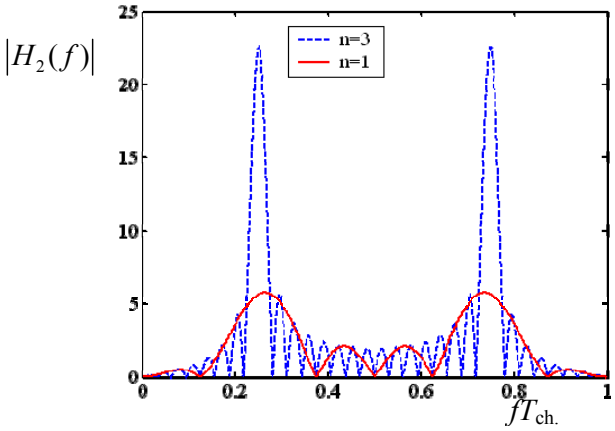

Fig. 4-13: The frequency response of applied chopper with frequency divider.

Now it is easy to understand the advantage of the applied chopper as compared to a simple (+ - + -) chopper. Figure 4-14 shows a comparison of the frequency response of these two choppers for n = 3. Note that the low-frequency suppression of the applied chopper is much more efficient than that of the simple chopper. To illustrate this, let us suppose that T_{ch} = 10µs. Then, for instance at fT_{ch} = 0.1, the frequency f would be 10 kHz. From the zoomed part of the figure it is clear that the low-frequency suppression of the applied chopper below 10 kHz is slightly better than that of the simple chopper. However, for 50 Hz interference of the main supply for the advanced chopper, the suppression is about 1.6×10^{-4} as compared to 5×10^{-2} for the simple chopper.

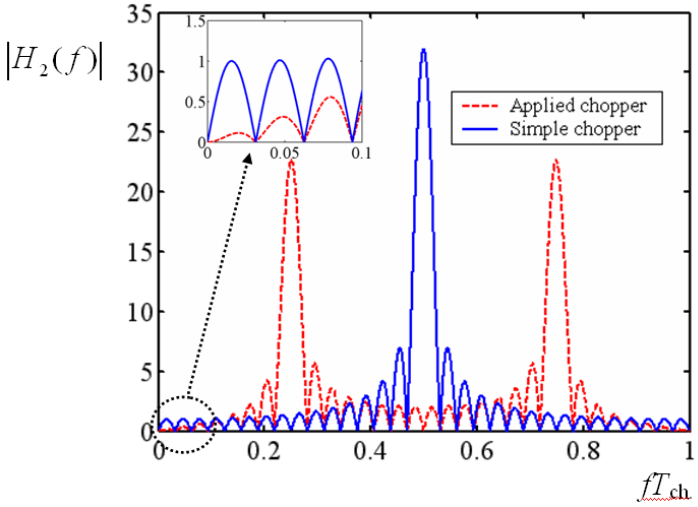

Fig. 4-14: Comparison of $H_2(f)$ for applied chopper to simple chopper.

Understanding this is even possible without any mathematics [7]. For instance let us consider an interfering signal with a frequency much less than the chopping frequency. Therefore, the interference signal is either rising or declining, but not both rising and declining. Figure 4-15 depicts this interfering signal with a dashed curve, while the four sampling moments are indicated with the vertical arrows. Since we are talking about an interfering signal with a frequency much lower than $1/T_{ch}$, the dashed curve is close to a straight line. It is clear that if we approximate the curve with a straight line, that the applied chopper after demodulation

completely removes the effect of interference, while in the case of a simple chopper there is a residual effect. Also, in the case of a small curvature, the applied chopper will remove the effect of this interfering signal much better than a simple chopper. From the figure it can also be understood that the highest low-frequency suppression is achieved if the time intervals between the four samples are equal.

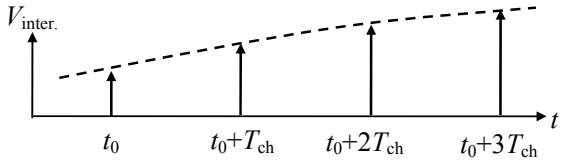

Fig. 4-15: Graphical explanation of the advantage of the applied chopper as compared to a simple chopper for suppression of very low-frequency interference.

4-6-1-2 Filtering effect of integration

In this section, we want to find the amount of voltage noise at the integrator output caused by integration of a noisy current in a specific time T_{int}. Let us consider one component of the noise based on the Bennet model [14]. It is clear that if the integration time T_{int} equals an integer number of the period of the noise component, then the effect of this component on the integrator output is zero. Moreover, components with a frequency $f << 1/T_{int}$ act almost as DC components and create the maximum voltage noise ($V_n=I_nT_{int}/C_{int}$) at the integration output. However, the high-frequency component, with $f >> 1/T_{int}$, will not have a significant contribution to the integrator-output voltage noise because most of the time its positive and negative effect cancel each other and only very little positive or negative effect remains at the end of the period. Mathematically, integrating a noise current for a fixed amount of time is analogous to filtering with a sinc filter in the frequency domain [15]. The corresponding transfer function $H_3(f)$ is:

$$H_3\left(f,T_{int}\right)=\frac{T_{int}}{C_{int}}\frac{\sin\left(\pi fT_{int}\right)}{\pi fT_{int}}=\frac{T_{int}}{C_{int}}\operatorname{sinc}\left(fT_{int}\right). \qquad (4\text{-}26)$$

In terms of power we have to square this transfer function. Figure 4-16 shows the sinc^2 function as a function of the frequency.

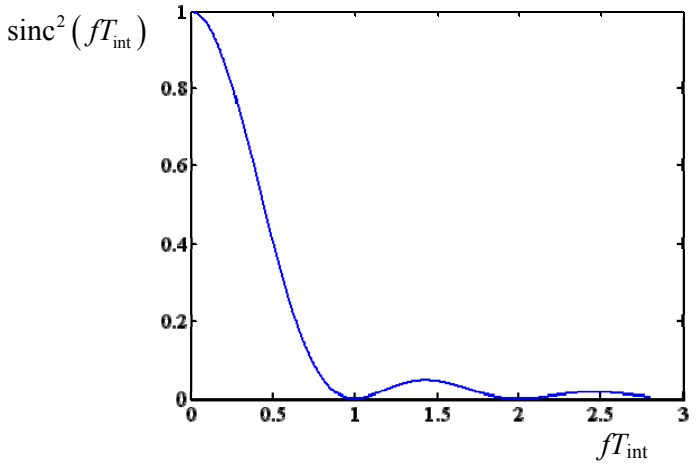

Fig. 4-16: The squared transfer function of the sinc filter.

Note, that for frequencies higher than $1/T_{int}$, that there is a significant suppression. For instance for T_{int}= 1ms, only the noise components <1 kHz are relevant.

Therefore, the voltage noise can be found as:

$$v_n(T_{int}) = \frac{T_{int}}{C_{int}} \sqrt{\int_0^\infty S_{in}(f)\,\mathrm{sinc}^2(fT_{int})\,df}\,, \tag{4-27}$$

where $S_{in}(f)$ is the noise spectral density of the integrator-current source (Fig. 3-9(a)). In the case of white noise this results in:

$$v_n(T_{int}) = \frac{T_{int}}{C_{int}} \sqrt{S_{in}(f)\int_0^\infty \mathrm{sinc}^2(fT_{int})\,df}\,. \tag{4-28}$$

For the integral of the sinc^2 function it holds that:

$$\int_0^\infty \mathrm{sinc}^2(fT_{int})\,df = \frac{1}{2T_{int}}. \tag{4-29}$$

So that,

$$v_n(T_{int}) = \frac{T_{int}}{C_{int}} \sqrt{\frac{S_{in}(f)}{2T_{int}}}\,. \tag{4-30}$$

4-6-1-3 Filtering effect of band limitation of the comparator

In this section we will consider the filtering effect of the comparator on the voltage noise at its input. As mentioned in section 4-5, when the comparator enters its linear region, it acts as an integrator. Therefore, in the frequency domain it behaves as a sinc filter with the bandwidth of $1/2t_d$, where t_d is the delay time of the comparator, or in other words: t_d is the time when the comparator is in its linear region and acts as an integrator.

The current spectral noise density at the output of the comparator preamplifier amounts to:

$$S_{in\text{-}pa} = g_{m\text{-}pa}^2 S_{vn\text{-}comp\text{-}in}\,, \tag{4-31}$$

where $g_{m\text{-}pa}$ is the transconductance of the preamplifier (Fig. 4-11) in the comparator, and $S_{vn\text{-}comp\text{-}in}$ is the noise spectral density at the input of the comparator including the noise from the previous stage and the comparator itself. This noise passes through the integration filter. The squared transfer function of this filter is:

$$H_4^2(f) = \frac{t_d^2}{C_{o\text{-}pa}^2}\left(\frac{\sin(\pi f t_d)}{\pi f t_d}\right)^2. \tag{4-32}$$

This transfer function is shown in Fig. 4-17.

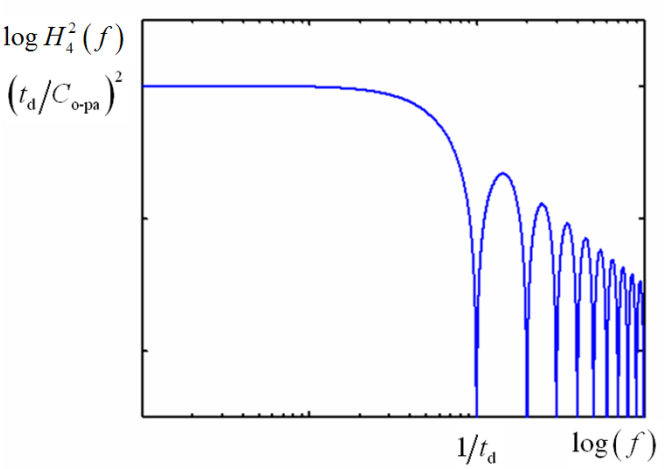

Fig. 4-17. Filtering effect of the comparator.

For a spectral density $S_{in\text{-}pa}(f)$ of the input voltage, the squared noise voltage at the output of the preamplifier amounts to:

$$\overline{v_{no\text{-}pa}^2} = \int_{f=0}^{\infty} S_{in\text{-}pa}(f) H_4^2(f)\, df. \tag{4-33}$$

Considering white noise, combining equations 4-29 and 4-31 with 4-33 results in:

$$\overline{v_{no\text{-}pa}^2} = g_{m\text{-}pa}^2 S_{vn\text{-}comp\text{-}in} \frac{t_d}{2C_{o\text{-}pa}^2}. \tag{4-34}$$

Using equations 4-11, 4-20, 4-22 and 4-34, the jitter caused by the noise at the input of the comparator $j_{vn\text{-}comp\text{-}in}$ can be calculated as:

$$J_{vn\text{-}comp\text{-}in}^2 = \frac{S_{vn\text{-}comp\text{-}in}\sqrt{\omega_{u\text{-}pa}/4V_{dd}}}{G^{3/2}}. \tag{4-35}$$

The jitter caused by white noise at the comparator input can also be calculated as:

$$J_{vn\text{-}comp\text{-}in}^2 = \frac{S_{vn\text{-}comp\text{-}in} B_{n\text{-}comp\text{-}e}}{G^2}, \tag{4-36}$$

Comparing equation 4-35 to 4-36 and considering equation 4-20, the effective noise bandwidth of the comparator $B_{n\text{-}comp\text{-}e}$ equals:

$$B_{n\text{-}comp\text{-}e} = \frac{1}{2}\sqrt{\frac{G\omega_{u\text{-}pa}}{V_{dd}}} = \frac{1}{2t_d}. \tag{4-37}$$

At the input of the comparator, two types of noise can be distinguished: (a) the noise from sources with a bandwidth of $B_n << B_{n\text{-}comp\text{-}e}$, (b) the noise from sources with a bandwidth of $B_n \geq B_{n\text{-}comp\text{-}e}$. For sources with a lower bandwidth, we calculate the jitter from the equivalent noise found at the input or the output of the comparator. However, for those with a higher bandwidth, we will first calculate the noise spectrum after filtering by the comparator transfer function $H_4(f)$ and then calculate the jitter at the output of comparator preamplifier.

For the condition $B_n << B_{n\text{-}comp\text{-}e} = 1/2t_d$, as discussed in section 4-5, the jitter caused by the input noise voltage $v_{n\text{-}comp\text{-}in}$ calculated at the input of the comparator equals:

$$J^{\text{in}}_{v\text{n-comp-in}} = \frac{v_{\text{n-comp-in}}}{G} = \frac{1}{G}\sqrt{\int_0^{B_\text{n}} S_{v\text{n-comp-in}}\,\mathrm{d}f} \tag{4-38}$$

For the same noise source, the equivalent jitter at the output of the pre-amplifier can be calculated as follows:

For noise with a limited noise bandwidth $B_\text{n} << 1/t_\text{d}$, the filter transfer function from equations 4-32 can be replaced by its low-frequency value: $(t_\text{d}\ /C_{\text{o-pa}})^2$. With this and using equations 4-32 to 4-34, for the noise at the output of the pre-amplifier in the comparator it is found that:

$$\overline{v^2_{\text{no-pa}}} = \left(\frac{t_d\, g_{\text{m-pa}}}{C_{\text{o-pa}}}\right)^2 \int_0^{B_\text{n}} S_{v\text{n-comp-in}}\,\mathrm{d}f\,. \tag{4-39}$$

The jitter caused by the input noise voltage $v_{\text{n-comp-in}}$ calculated at the output of the comparator equals:

$$J^{\text{out}}_{v\text{n-comp-in}} = \frac{v_{\text{no-pa}}}{\left.\dfrac{\partial v_{\text{o-pa}}(t)}{\partial t}\right|_{t=t_\text{d}}} \tag{4-40}$$

Combining equations 4-20, 4-22, and 4-39 into equation 4-40 yields the same result as that of equation 4-38. As expected, for the noise sources with $B_\text{n} << 1/t_\text{d}$, the jitter can be calculated at the input or at the output of the comparator.

4-6-1-4 Filtering effect of auto-calibration including integration

Except for the noise coming from integrator current, all noise sources are chopped and therefore there is no need to focus on their low-frequency component. However, as figure 4-16 shows, the low-frequency noise can simply pass through a sinc filter. Therefore the low-frequency flicker noise of the current source can cause low-frequency fluctuation in the output period. In this section, we want to show that some part of this fluctuation also can be removed by auto-calibration.

According to equation 3-12 the final measurement result M amounts to:

$$M = \frac{T_\text{x} - T_{\text{ref1}}}{T_{\text{ref2}} - T_{\text{ref1}}}\ . \tag{4-41}$$

Thus once the jitter of the individual period is known, the effect on M should be established. Let us suppose that one complete measurement time, including three-signal auto-calibration $T_{3\text{-sig.}}$ (Fig. 3-6(b)), takes 10 ms. Then it is clear that very low-frequency drift, for instance thermal drift of I_int, affects T_{ref1}, T_{ref2} and T_x with the same multiplicative error. Consequently, the effect on M is eliminated. However, fluctuations caused by flicker noise of the integrator-current can have a higher frequency. In order to see how well auto-calibration can remove the effects of this noise, we need to extract the frequency response of auto-calibration.

The effect of the current noise on the standard deviation of M can be found as:

$$\sigma_M = M_{\text{exact}}\sqrt{\int_{f=0}^{\infty} \frac{S_{i_n}(f)}{I^2_\text{int}} H_5^2(f)\,df} \tag{4-42}$$

where M_{exact} is the value of M in the absence of this noise, $S_{i_n}(f)$ is the spectral density of the noise of the current source, and $H_5(f)$ is the frequency response of the integrator including three-signal auto-calibration.

Figure 4-18 shows the calculated transfer function $H_5(f)$ for the case that the three concatenated measurement time intervals T_{ref1}, T_{ref2} and T_x take 2 ms, 5 ms and 3 ms, respectively. As is shown, the frequency response has a maximum of around $1/T_{3\text{-sig}}$. The maximum response and the corresponding frequency depend on the values of T_{ref1}, T_{ref2} and T_x. Signal components with a frequency below $1/T_{3\text{-sig.}}$ are suppressed by auto-calibration, and those with a frequency higher than $1/T_{3\text{-sig.}}$ are suppressed by integration, or in the other words, by the sinc filter.

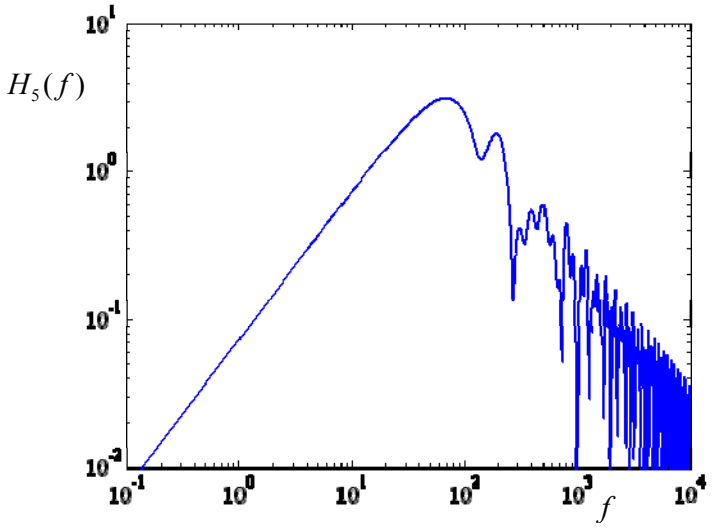

Fig. 4-18: Calculated transfer function $H_5(f)$, representing the filtering effect of the integrator including three-signal auto-calibration.

4-6-2 Effect of the different noise sources on the output jitter

As mentioned above, it makes sense to distinguish two types of noise at the input of the comparator: (a) the noise with bandwidth much lower than the effective noise bandwidth of the comparator $B_{n\text{-comp-e,}}$ and (b) noise with a bandwidth comparable to or higher than the effective noise bandwidth of the comparator. All sampled noise, which has a bandwidth of $f_s/2$, along with the noise of the integrator current, which is filtered by the sinc filter (Eq. 4-26), are found in the first type and their effect on jitter can be calculated at the comparator input. However, for the noise of the CVC amplifier, the integrator amplifier, and the comparator in the continuous state, the effect of comparator filter $H_4(f)$ should first be taken into account so that next the jitter at the output of comparator preamplifier can be found.

4-6-2-1 Calculation of jitter in the output period caused by the noise in the integrator current.

Figure 4-19 shows the circuit diagram of the applied integrator-current source together with a part of the integrator. To suppress low-frequency interference (section 4-6-1-1), the magnitudes of these two currents should be equal. For the implementation shown in figure 4-19(a), the required matching can be achieved by using layout-matching techniques [3, 4]. With respect to the integrator-current source, the main difference of our implementation with

that in the UTI is found in the implementation of the bias voltage V_{bias} (Fig. 4-19(b) and (c)). In the UTI this bias voltage is made with a diode-connected NMOS transistor biased with a supply-independent current source. In that implementation the bias voltage is supply-independent, and therefore the integrator-current source is also supply-independent. With this condition the measurement time T_{msm} (Eq. 3-13) is supply-dependent. Moreover in the UTI, due to the current mirror with a small pmos transistor (16µ/2µ), the flicker-noise corner frequency of current source, is about 500 Hz. However, for the integrator current noise the only low-frequency filtering is that resulting from auto-calibration. In order to remove the flicker noise of current source it is necessary that $f_c < 1/T_{3\text{-sig}}$. For the designs presented in [16] and chapter 8, the current-source implementation is the same as in the UTI. Consequently, the resolution is limited by the integrator-current source. However, in chapter 5 a new implementation (Fig. 4-19(c)) is introduced in which a major noise reduction is achieved in the following ways:

1. The current source is redesigned for a flicker-noise corner frequency $f_c < 1/T_{3\text{-sig}}$ for all different modes.
2. The current is supply-dependent, which removes part of the supply dependency of the pumped charge. Therefore the measurement period T_{msm} (Eq. 3-13) is less supply-dependent than, for instance, the UTI. It is not difficult to design a current source to be proportional to the supply voltage which fully removes the supply dependency of the pumped charge and therefore makes the measurement period T_{msm} (Eq. 3-13) supply-independent.
3. Part of the source resistors can be bypassed by switches, which creates four binary steps in the integrator current I_{int}.

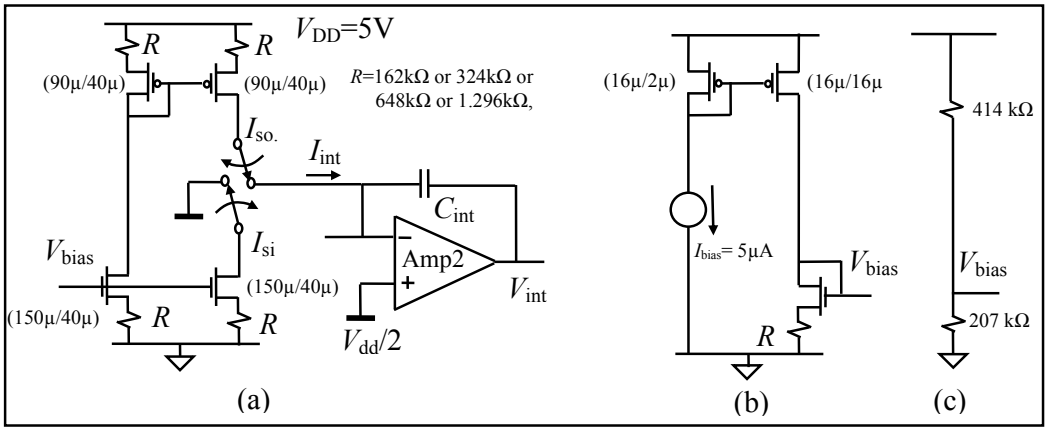

Fig. 4-19: Circuit diagrams of (a) the applied integrator-current source I_{so} and current sink I_{si}, (b) bias voltage implemented in UTI and (c) bias voltage with very low flicker noise.

One complete output period T_{out} includes $NT_{msm}= 4\ NT_{ch}$ (Fig 3-9(b) and section 4-2). As shown in figure 3-9(b) each current source is being integrated for the period of $2T_{ch}$ and then switched to another one. Only at the beginning and at the end of one output period do we have a single integration period T_{ch}. To simplify the calculation, we suppose that each current source is being integrated for the time interval of $2T_{ch}$ for the entire period T_{out} without introducing significant error.

In the time domain the noise currents $I_{si}(t)$ and $I_{so}(t)$ can be written as:

$$I_{si}(t) = I_{DC} + i_{n,si}(t) \tag{4-43}$$

$$I_{so}(t) = I_{DC} + i_{n,so}(t), \tag{4-44}$$

where I_{DC} is the noiseless current, and $i_{n,si}(t)$ and $i_{n,so}(t)$ are the noise components in the current sink and source, respectively. In this section, we suppose that all parts in our interface are noiseless. Now, we will calculate the effect of the noise components of the integrator current on the output jitter. Due to the noise of the integrator current, there is jitter at each decision time. For simplicity we suppose that the polarity of the integrator current is controlled by an ideal clock and calculate the noise voltage at the integrator output at the end of the period NT_{msm}. By having this noise voltage and the voltage slope $\delta V_{int}/\ \delta t$ at the integrator output, the jitter at the end of the period can be calculated. In reality there is no such voltage noise and therefore we name it corresponding noise voltage. With this assumption the corresponding noise voltage at the end of the period $T_{out} = 4\,NT_{ch}$ is equal to:

$$v_{n,Tout,corresp.} = \frac{1}{C_{int}} \sum_{k=0}^{N-1} \left(\int_{4kT_{ch}}^{(4k+2)T_{ch}} i_{n,so}(t)\,dt + \int_{(4k+2)T_{ch}}^{(4k+4)T_{ch}} i_{n,si}(t)\,dt \right). \tag{4-45}$$

This equation can also be rewritten as:

$$v_{n,Tout,corresp.} = \frac{1}{C_{int}} \sum_{k=0}^{N-1} \int_{0}^{2T_{ch}} \left(i_{n,so}(t+4kT_{ch}) + i_{n,si}(t+(4k+2)T_{ch}) \right) dt\,. \tag{4-46}$$

If we assume that the noise in the current source and the current sink are uncorrelated, the modeled noise voltage in the frequency domain can be calculated as follows:

$$\begin{aligned} S_{vn,Tout,corresp.}(j\omega) &= \frac{S_{in,so}(j\omega) + S_{in,si}(j\omega)}{C_{int}^2} \left(2T_{ch}\,\mathrm{sinc}(2T_{ch}f) \sum_{k=0}^{N-1} e^{j4\omega T_{ch}} \right)^2 \\ &= \frac{S_{in,so}(j\omega) + S_{in,si}(j\omega)}{C_{int}^2} \left(2T_{ch}\,\mathrm{sinc}(2T_{ch}f) \frac{\sin(\pi f T_{out})}{\sin(4\pi f T_{ch})} \right)^2 \\ &= \frac{S_{in,so}(j\omega) + S_{in,si}(j\omega)}{C_{int}^2} \left(\frac{T_{out}}{2} \frac{\mathrm{sinc}(fT_{out})}{\cos(2\pi f T_{ch})} \right)^2 . \end{aligned} \tag{4-47}$$

Therefore, the modeled voltage noise is calculated as:

$$\begin{aligned} v_{n,Tout,corresp.} &= \sqrt{\int_0^\infty S_{vn,Tout,modeled}(j2\pi f)\,df}\,. \\ &= \frac{T_{out}}{C_{int}} \sqrt{\int_0^\infty \frac{S_{in,so}(j\omega) + S_{in,si}(j\omega)}{2} \left(\frac{\mathrm{sinc}(fT_{out})}{\sqrt{2}\cos(2\pi f T_{ch})} \right)^2 df}\,. \end{aligned} \tag{4-48}$$

With the spectral densities $S_{in,so}(j\omega)$ and $S_{in,si}(j\omega)$ of the noise components in the current source and sink, respectively, the modeled voltage noise can be calculated as follows.

In the case of white noise, equation 4-48 can be simplified as:

$$v_{n,Tout,corresp.} = \frac{T_{out}}{C_{int}} \sqrt{\frac{S_{in,so}(j\omega) + S_{in,si}(j\omega)}{2} \int_0^\infty \left(\frac{\mathrm{sinc}(fT_{out})}{\sqrt{2}\cos(2\pi f T_{ch})} \right)^2 df}\,. \tag{4-49}$$

Independent of the ratio of T_{out}/T_{ch}, the result of integral is equal to:

$$\int_0^{\infty}\left(\frac{\operatorname{sinc}\left(fT_{\text{out}}\right)}{\sqrt{2}\cos\left(2\pi fT_{\text{ch}}\right)}\right)^2 \mathrm{d}f = \frac{1}{2T_{\text{out}}}. \tag{4-50}$$

Substitution of equation 4-50 into 4-49 results in:

$$v_{\text{n,Tout,corresp.}} = \frac{T_{\text{out}}}{C_{\text{int}}}\sqrt{\frac{S_{in,\text{so}}\left(\mathrm{j}\omega\right)+S_{in,\text{si}}\left(\mathrm{j}\omega\right)}{4T_{\text{out}}}}. \tag{4-51}$$

Note the similarity of this equation with equation 4-30; this similarity can be explained from the fact that the voltage noise caused by the integration of two uncorrelated, white-noise currents is the same as the voltage noise caused by continuous integration of a white-noise current with an average noise-power spectral density.

Since the noise of the integrator current is filtered by the integrator (Eq. 4-26), the bandwidth of the modelled voltage noise caused by the noisy integration current at the input of the comparator is smaller than the bandwidth of the integration filter of the comparator pre-amplifier. Therefore, the jitter caused by the noisy integrator current J_{in} can be calculated at the input of the comparator (section 4-6-1-3). Therefore:

$$J_{\text{in}}\left(T_{\text{out}}\right) = \frac{v_{\text{n,Tout,modeled}}}{\partial V_{\text{int}}/\partial t} = \frac{C_{\text{int}}}{I_{\text{int}}}v_{\text{n,Tout,modeled}}. \tag{4-52}$$

Substitution of equation 4-51 into 4-52 results in:

$$J_{\text{in}}\left(T_{\text{out}}\right) = \frac{T_{\text{out}}}{I_{\text{int}}}\sqrt{\int_0^{\infty}\frac{S_{in,\text{so}}\left(\mathrm{j}\omega\right)+S_{in,\text{si}}\left(\mathrm{j}\omega\right)}{4T_{\text{out}}}}. \tag{4-53}$$

The noise of the current sources of figure 4-19(a) can be reduced by increasing the voltage drop across the resistors. Since the voltage at the negative input of the Amp2 is equal to $V_{\text{DD}}/2$, and because there are very small spikes only during the transients, there is quite a large voltage-room for this voltage drop across the resistors. In this situation, and ignoring the noise in bias voltage V_{bias}, the noise spectral density $S_{\text{in,si}}$ of the thermal noise of the sink current amounts to:

$$S_{\text{in,si}} \approx \frac{4kT}{R}, \tag{4-54}$$

where k is Boltzmann's constant and T is the absolute temperature of the resistor. The spectral density $S_{\text{in,so}}$ of the thermal noise of the source current is equal to:

$$S_{\text{in,so}} \approx \frac{12kT}{R}. \tag{4-55}$$

Increasing the current in left branch in figure 4-19(a) by increasing the W/L ratio of these transistors and simultaneously decreasing the value of related resistor with the same factor, the noise spectral density of the current source $S_{\text{in,so}}$ can be decreased to the level of noise spectral density of the current sink $S_{\text{in,si}}$.

If we suppose that the flicker-noise corner frequencies of the current source and current sink are less than $1/2T_{\text{3-sig.}}$ (Fig. 3-6(b)), then the effect of flicker noise will be eliminated by auto-calibration. In that case, we can apply equation 4-53.

Substitution of equations 4-53 and 4-55 with equation 4-54 and 4-55 results in:

$$J_{\text{in}}\left(T_{\text{out}}\right)=\frac{T_{\text{out}}}{I_{\text{int}}}\sqrt{\frac{4kT}{RT_{\text{out}}}}. \tag{4-56}$$

The relative jitter ξ_{in} amounts to:

$$\xi_{in}=\frac{J_{\text{in}}\left(T_{\text{out}}\right)}{T_{\text{out}}}=\frac{1}{I_{\text{int}}}\sqrt{\frac{4kT}{RT_{\text{out}}}}. \tag{4-57}$$

Example 4-2: For C_{o1}= C_{o2}= 1pF, C_S=10 pF, V_{dd}=5V, $V_{o\text{-}cvc}$= 1.5 V, I_{int} =1µA, R=700kΩ and N=32, along with equation 3-12, we find that T_{out} = $NT_{msm,}$= 3.2ms. In this case, for the jitter and relative jitter, equations 4-56 and 4-57 yield 8.3ns and 2.6 ×10^{-6}, respectively.

Equation 4-57 can be rewritten as:

$$\xi_{in}=\sqrt{\frac{4kT}{RI_{\text{int}}T_{\text{out}}I_{\text{int}}}}=\sqrt{\frac{4kT}{V_{\text{R}}Q_{\text{tot}}}} \tag{4-58}$$

where V_R is the voltage drop across the resistors R (Fig. 4-19(a)) and Q_{tot} is the total charge pumped into the integrator capacitor during the time interval T_{out}. For the circuit of figure 3-9(a), the charge Q_{tot} can simply be calculated as:

$$Q_{\text{tot}}=4N\left(V_{\text{dd}}\left(C_{\text{o1}}+C_{\text{o2}}\right)+V_{\text{o-cvc}}C_{\text{S}}\right). \tag{4-59}$$

Let us suppose that we increase the current in the circuit of figure 4-19(a) by decreasing the resistance R. In that case, the voltage over the resistors V_R and therefore also the relative jitter will almost remain constant. At the same time increasing the integration current I_{int}, will decrease the measurement time. Therefore, it can be concluded, that for a fixed measurement time, an increase in the integration current I_{int} will decrease the relative jitter caused by the noise of the integration current. It should be mentioned that the level of the integrator current (0.5µA to 4 µA) is much less than that of the supply current of the total chip (about 1 mA). Therefore, increasing the integrator current will hardly affect the power consumption.

4-6-2-2 Calculation of jitter in the output period as caused by noise in the sampling and charge-transfer circuit.

Let us consider the circuit of figure 4-20, which shows the sampling mode.

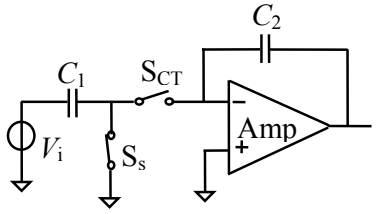

Fig. 4-20: The circuit diagram for the calculation of noise in sampling mode.

The noise produced by the thermal noise in the switch ON resistance $R_{on\text{-}s}$ of switch S_s is filtered with a time constant $R_{on\text{-}s}C_1$. The single-sided noise spectral density over the capacitor C_1 would be:

$$S_{v_n}(f) = \frac{4kTR_{\text{on-s}}}{1+(2\pi f R_{\text{on-s}} C_1)}, \tag{4-60}$$

where $R_{\text{on-s}}$ is the ON resistance of the switch S_s. Here we supposed that the output resistance of the voltage source V_i is zero, otherwise it can be included in switch ON resistance $R_{\text{on-s}}$. In this case, the mean-square value $\overline{v_{n1}^2}$ of the voltage noise on the capacitor C_1 amounts to:

$$\overline{v_{n1}^2} = \int_0^\infty S_{v_n}(f)\,df = \frac{kT}{C_1}. \tag{4-61}$$

This amount of noise is frozen in the capacitor. The same result can be found by considering the noise bandwidth of a first-order system which is л/2 times the signal bandwidth, for which the voltage noise on the capacitor is found to be [9]:

$$\overline{v_{n1}^2} = S_{v_n}(f)\frac{\pi}{2}\frac{1}{2\pi R_{\text{on-s}} C_1} = \frac{S_{v_n}(f)}{4\tau} = \frac{kT}{C_1} \tag{4-62}$$

This calculation shows that with respect to noise there is no restriction on the size of switch S_s. Yet, to achieve a certain settling accuracy, the switches should be large enough.

Now, consider the same circuit as figure 4-20 but in the charge-transfer mode. In the charge-transfer mode the input voltage is zero. For convenience, the circuit of figure 4-20 in charge-transfer mode is redrawn (Fig. 4-21). Let us suppose that the amplifier is an OTA with transconductance g_m.

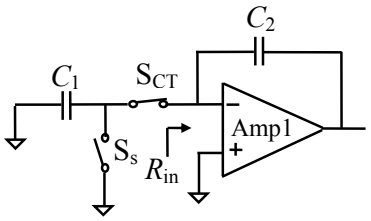

Fig. 4-21: The circuit diagram for the calculation of noise in charge-transfer mode.

In this circuit the total noise on capacitor C_1 caused by the switch S_{CT} is [9]:

$$\overline{v_{n2}^2} = \frac{S_{v_n}(f)}{4\tau} = \frac{4kTR_{\text{on-CT}}}{4(R_{\text{on-CT}} + 1/g_m)C_1} = \frac{kT/C_1}{1+1/(g_m R_{\text{on-CT}})} \tag{4-63}$$

Therefore only part of the noise generated by the switch ON resistance will pass through the system. In other words: in the charge-transfer mode, the noise bandwidth is not necessarily determined by the switch ON resistance. For the case that:

$$g_m R_{\text{on-CT}} << 1, \tag{4-64}$$

the condition of which can simply be satisfied by large switches, it holds that:

$$\overline{v_{n2}^2} << \overline{v_{n1}^2}. \tag{4-65}$$

Thus the size of the charge-transfer switches S_{CT} should be designed for a sufficiently low $R_{\text{ON-CT}}$ because this can decrease their noise contribution significantly.

For convenience the complete interface is redrawn in figure 4-22(a). Also the integrator output voltage is shown in figure 4-22(b).

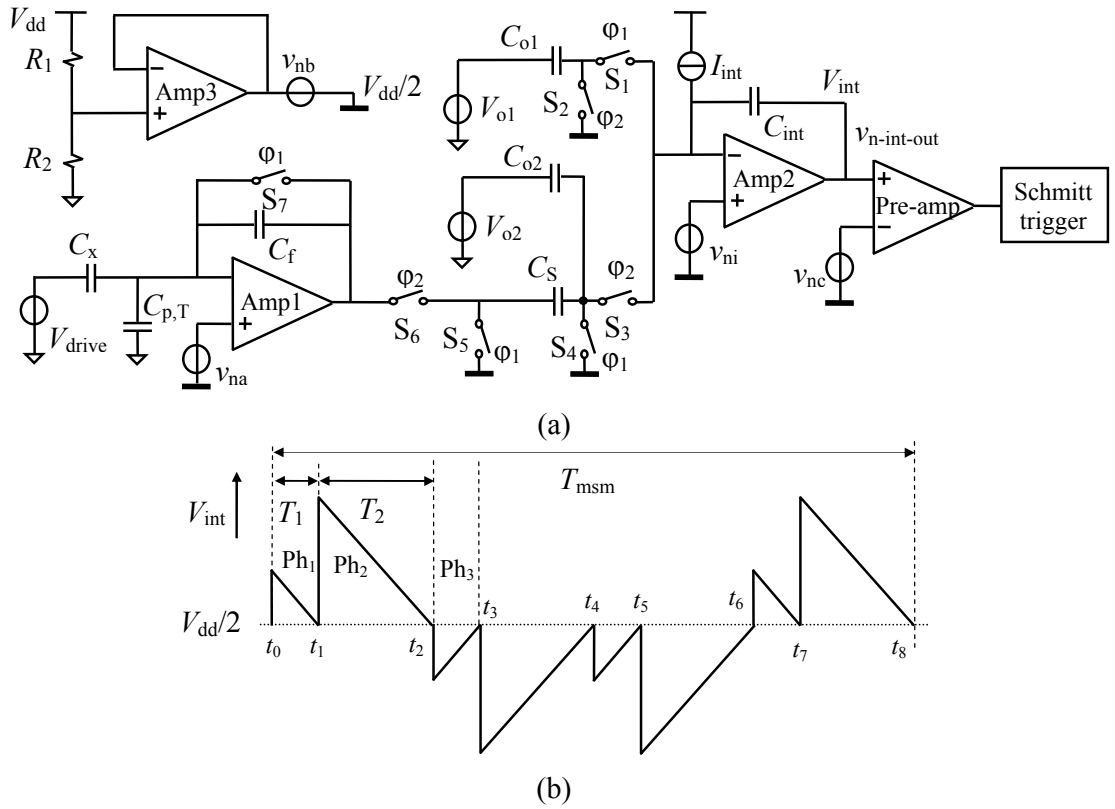

Fig. 4-22: (a) The related part of the interface for the noise analysis and (b) the integrator output voltage.

In phase 1 (Fig. 4-22(b)), as soon as switch S_1 is closed, the charge of $q_1=V_{dd}C_{o1}$ is pumped into the integrator capacitor and is removed by the integration of I_{int}. However, besides the desired charge, $q_1=V_{dd}C_{o1}$, the noise charge of:

$$\overline{q_{n1,s}} = \sqrt{kTC_{o1}}, \tag{4-66}$$

is also pumped into the integrator capacitor, where $\overline{q_{n1,s}}$ is the standard deviation of the sampling-noise charge in phase 1. As discussed above, the noise of the switch ON resistance in the charge-transfer mode is negligible. Similarly, for phase 2 we have:

$$\overline{q_{n2,s}} = \sqrt{kT\left(C_{o2}+C_S\right)}. \tag{4-67}$$

For the total sampling-noise charge pumped into the integrator capacitor in the output period $T_{out} = NT_{msm}$ it holds that:

$$\overline{q_{nT,s}\left(T_{out}\right)} = \sqrt{4NkT\left(C_{o1}+C_{o2}+C_S\right)}. \tag{4-68}$$

The corresponding jitter J_s in the output period caused by sampling is:

$$J_s = \frac{\sqrt{4NkT\left(C_{o1}+C_{o2}+C_S\right)}}{I_{int}}. \tag{4-69}$$

Then, using equations 3-13 and 4-69 for the relative jitter ξ_s in $T_{out,}$ as caused by sampling, it is found that:

$$\xi_S = \frac{\sqrt{kT\left(C_{o1}+C_{o2}+C_S\right)/4N}}{\left(V_{dd}\left(C_{o1}+C_{o2}\right)+V_{o\text{-}cvc}C_S\right)}. \tag{4-70}$$

Example 4-3: For the conditions mentioned in example 4-2 (C_{o1}= C_{o2}= 1pF, C_S=10 pF, V_{dd}=5V, $V_{o\text{-}cvc}$= 1.5 V, I_{int} =1μA, and N=32) the jitter and relative jitter amount to 2.5 ns and 7×10^{-7}, respectively.

4-6-2-3 Calculation of jitter in output period that is caused by the sampled noise voltage at the input of the capacitor-to-voltage converter CVC.

Figure 4-23 shows the CVC in the sampling phase (phase 1) including the equivalent noise voltage at its input.

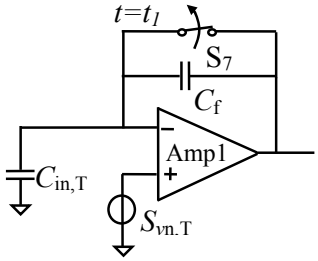

Fig. 4-23: The interface part used for analysis of the effect of the CVC equivalent input-noise voltage for phase 1.

In figure 4-23 the capacitor $C_{in,T}$ is the total capacitance at this node, which is equal to:

$$C_{in,T} = C_x + C_{ref1} + C_{ref2} + C_p\,. \tag{4-71}$$

Also:

$$S_{vn,T} = S_{vna} + S_{vnb} \approx S_{vna}\,, \tag{4-72}$$

where $S_{vn,b}$ is the voltage noise-spectral density of the reference voltage "Half V_{DD}" (HVDD), and $S_{vn,a}$ is the input referred voltage noise-spectral density of the CVC amplifier. As compared to the effect of the CVC amplifier, the noise of HVDD is negligible. This can easily be realized by using a large off-chip capacitor of, for instance, 100 nF on the HVDD pin, which is available for the user.

The flicker-noise component in $S_{vn,a}$ is removed by the applied chopper. If we suppose that the amplifier is an OTA with transconductance g_m, similar to equation 4-62, for the remaining thermal noise we find that:

$$\overline{v_n^2} = \frac{S_{vna}(f)}{4\tau} = \frac{S_{vna}(f)\,g_{m,CVC}}{4C_{in,T}}\,. \tag{4-73}$$

At the time t=t_1, when switch S_7 is opened, the noise charge q_n freezes at capacitor $C_{in,T}$. The mean-squared value of this noise amounts to:

$$\overline{q_n^2} = \frac{S_{vna}(f)\,g_{m,CVC}C_{in,T}}{4}\,. \tag{4-74}$$

Next, both the signal charge $C_{in}V_{dd}$, where C_{in} is one of the three input capacitor C_{ref1}, C_{ref2} or C_x, and the noise charge are pumped into C_f. The mean-squared value of the corresponding noise at the output of the CVC in phase 2 is equal to:

$$\overline{v_{\text{no-CVC}}^2} = \frac{S_{vna}(f)\, g_{m,CVC} C_{in,T}}{4C_f^2}. \tag{4-75}$$

Then the related charge noise pumped into integrator capacitor C_{int} at one chopper period equals:

$$\overline{q_{n,Tch}^2} = \overline{v_{\text{no-CVC}}^2} C_s^2 \tag{4-76}$$

where C_S is the sampling capacitor (Fig. 4-22(a)). For one complete output period $T_{out}=4NT_{ch}$, the total charge noise can be approximately calculated as:

$$\overline{q_{n,Tout}^2} = 4N\overline{q_{n,Tch}^2}. \tag{4-77}$$

The jitter caused by this charge noise is equal to:

$$\overline{J_{\text{CVC-sample}}^2} = \frac{\overline{q_{n,Tout}^2}}{I_{int}^2}. \tag{4-78}$$

Combining equation 4-75, 4-76 and 4-78 results in:

$$J_{\text{CVC-sampled}} = \sqrt{N \frac{S_{vna}(f)\, g_{m,CVC} C_{in} C_S^2}{C_f^2 I_{int}^2}}. \tag{4-79}$$

Example 4-4: For the conditions mentioned in example 4-2 (C_S=10 pF, V_{dd}=5V, I_{int} =1μA, and N= 32) and with $g_{m,CVC}$ = 1 mA/V, C_f = 3.3pF, C_x = 0.5 pF, C_{ref2} = 1 pF, C_{ref1} = 0 pF and S_{vna} = 10^{-16}V^2/Hz (10 nV/√Hz), the period time T_{ref} equals 3.2 ms, which is equal to that mentioned in examples 4-2 and 4-3. For C_p = 50pF, the jitter and relative jitter on T_{ref} amount to 39 ns and 1.2 ×10^{-5}, respectively.

4-6-2-4 Calculation of jitter in output period caused by the sampled noise voltage of integrator amplifier.

Figure 4-24 shows the integrator in phase 1 (Ph1 in Fig. 4-22(b)). For the sake of simplicity, let us suppose that the comparator is noise-free. The input-referred noise of the integrator amplifier will appear at the integrator output and will change the deciding moment of the comparator, which will cause jitter in time interval T_1 (Fig. 4-22(b)). We will analyze this effect in sub-section 4-6-2-5.

Besides the aforementioned jitter, this voltage noise $v_{ni,ph1}$ is also sampled both in C_{o1} and C_{int}. The sampled noise in input capacitor C_{o1} does not have any further effect, since after sampling this capacitor is recharged by a voltage source. However, the sampled noise in C_{int} will remain and thus it affects the next time interval. In this section we will analyze this effect.

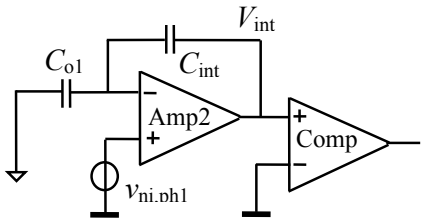

Fig. 4-24: The interface part used for analysis of integrator sampled noise voltage.

At the deciding moment, the voltage at the integrator output is $V_{dd}/2$ (as is explained in section 4-5 due to comparator delay this voltage is not exactly $V_{dd}/2$ but this does not affect the noise contribution). Because of the infinite amplifier gain, the voltage at the inverting input of the integrator amplifier will follow that of the non-inverting input. Therefore, the voltage sampled in integrator capacitor C_{int} equals $v_{ni,ph1}$.

In the case of white noise (flicker noise can be removed by chopper), $v_{ni,ph1}$ can be calculated as:

$$\overline{v_{vni,ph1}^2} = \frac{S_{vni}}{4\tau} = \frac{S_{vni} g_{m,int}}{4C_{o1}}, \tag{4-80}$$

where $g_{m,int}$ is the transconductance of OTA. The spectral noise density S_{vni} equals [9]:

$$S_{vni} = \alpha \frac{16}{3} \frac{kT}{g_{m,int}}. \tag{4-81}$$

For an optimized design, in which mainly the two input transistors of the differential amplifier contribute to the input-referred noise, it holds that $\alpha \approx 1$. For less-optimized OTA designs, α can reach up to about 2.

For phase 2 (the next phase), the jitter caused by this sampled noise equals:

$$j_{vni,ph1\rightarrow ph2} = \frac{v_{ni,ph1} C_{int}}{I_{int}}, . \tag{4-82}$$

Similar to phase 1, noise from phase 2 will cause jitter in phase 3 (Fig. 4-22(b)), where it holds that:

$$\overline{v_{vni,ph2}^2} = \frac{S_{vni} g_{m,int}}{4\left(C_{o2} + C_s\right)}, \tag{4-83}$$

and:

$$J_{vni,ph2\rightarrow ph3} = \frac{v_{ni,ph2} C_{int}}{I_{int}}. \tag{4-84}$$

The jitter expressed by equations 4-82 and 4-84 causes jitter $J_{vni,s}(T_{out})$ in the output period $T_{out}=4NT_{ch}$, where it holds that:

$$J_{vni,s}\left(T_{out}\right) = 2\sqrt{N\left(j_{vni,ph1\rightarrow ph2}^2 + j_{vni,ph2\rightarrow ph3}^2\right)}. \tag{4-85}$$

Example 4-5: For the same conditions of the previous example (C_S=10 pF, V_{dd}=5V, I_{int} =1μA and N= 32) and with $g_{m,int}$ = 0.3 mA/V, C_{int}= 10pF and S_{vni} = 3×10^{-16}V^2/Hz (v_{ni} = 17 nV/√Hz),

the time period T_{ref} equals 3.2 ms. Based on equations 4-80 and 4-83, the sampled voltage noise in phase 1 and phase 2 equals 150 nV and 45 nV, respectively. With equations 4-82 and 4-84, the jitter caused by these sampled noise is found to be 1.5 ns and 0.45 ns, respectively. Finally, the jitter caused by these sampled noises (Eq. 4-85) and relative jitter during T_{ref} amount to 18 ns and 5.6 $\times 10^{-6}$, respectively.

4-6-2-5 Calculation of jitter in the output period caused by the noise voltage of the CVC amplifier, the integrator amplifier, and the comparator in the continuous state.

Let us first consider the effect of the noise v_{nc} of comparator while supposing that the ramp voltage at the output of the integrator is noise-free. With this condition, a noise of the threshold voltage $V_{DD}/2$, for instance at the end of phase 1, can cause jitter during the time period T_1 but this noise cannot affect the time interval $T_1 + T_2$ (Fig. 4-25) [17]. However, this is not the case for the moment that the slope of the integrator output is changed: Similar to the effect depicted in figure 4-8, in this case the effect of jitter is also doubled (Fig. 4-25). However, this is not a fundamental source of error, because it can simply be removed in a fully differential structure, by swapping the capacitors that reverse the polarity of the state of the integrator during chopping [18]. In that case, as in a single-slope integrator (without chopping), only the jitter at the final deciding moment is important. In that case, when using p period, the relative jitter is decreased by a factor of p.

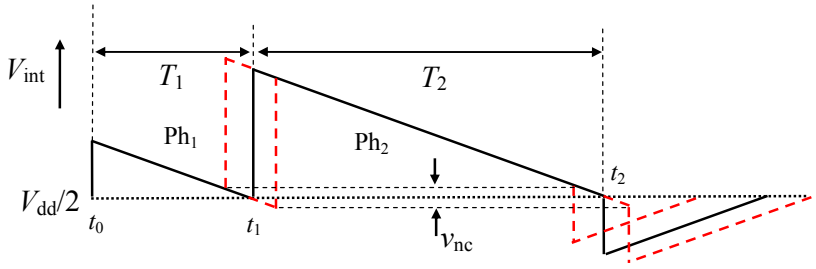

Fig. 4-25: The integrator output voltage for the case of a noisy comparator threshold voltage.

In our system, we did not compensate for the effect of chopping, which would yield more noise: By ignoring correlation, the jitter at each measurement cycle T_{msm} (Fig. 4-22) can be found as:

$$J_{Tmsm,vnc} = 2\sqrt{2}\, j_{vnc} \qquad (4\text{-}86)$$

Since there are 8 deciding moments in one measurement cycle T_{msm}, the result of equation 4-86 would be the same as in the case if the jitter at each deciding moment mattered and if we had to handle the uncorrelated jitter effects per period. In other words, in our system, using the p period decreases the relative jitter by a factor of $\sqrt{p}$.

In the continuous mode, the effects of noise of the CVC amplifier Amp1 and integrator amplifier Amp 2 (Fig. 4-22(a)) can be calculated in the same way as that of the comparator. As it is mentioned at the beginning of section 4-6-2, the noise of the CVC amplifier, the integrator amplifier and the comparator in the continuous state (phase 2) need to be calculated at the output of the comparator preamplifier, which is where the circuit of figure 4-22(a) can be simplified, as depicted in figure 4-26.

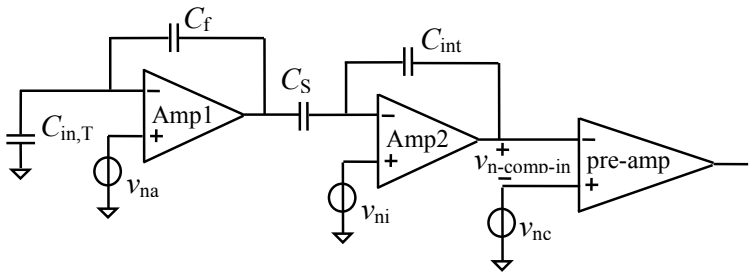

Fig. 4-26: Block diagram of the interface in phase 2 for calculating the noise at the integrator output.

The noise at the input of the comparator is due to the sum of the noise voltage at the integrator output plus the equivalent input noise voltage of the comparator itself. Let us suppose that the total spectral noise density at the input of the comparator is $S_{vn\text{-}comp\text{-}in}$. If this noise is dominated by the noise at the integrator output but not by the comparator noise itself, the voltage spectral noise density in phase 1 is much lower than in phase 2. Firstly this is because in phase 1, the CVC is disconnected and the noise gain of integrator amplifier is $1+ C_{o1} / C_{int} \approx 1$, compared to $1+ (C_{o1} + C_S) / C_{int} \approx 2$ in phase 2. Therefore, we will ignore the effect of noise in phase 1.

If we ignore the phenomena explained by figure 4-25, and suppose that at each 4 decision moment we have uncorrelated jitter, to find the final jitter we need a correction factor of $\sqrt{2}$.

The spectral noise density at the input of the comparator in phase 2 can be written as:

$$S_{vn\text{-}comp\text{-}in}(f) = S_{vna}(f) H_{vna}^2(f) + S_{vni}(f) H_{vni}^2(f) + S_{vnc}(f), \qquad (4\text{-}87)$$

where $H_{vna}(f)$ and $H_{vni}(f)$ are the transfer functions for v_{na} and v_{ni}, respectively, to the integrator output. Due to the parasitic capacitance at the input of the CVC amplifier, and because C_{int} and C_S are in the same range, the closed-loop bandwidth of the integrator Amp2 is larger than that of the CVC amplifier Amp1. Therefore, the transfer function from the CVC output to the integrator output can be considered a DC gain of C_{int}/C_S. In this condition, with one stage OTA as the CVC amplifier we have:

$$H_{vna}(f) = \frac{(C_S/C_{int})(C_f + C_{in})/C_f}{1 + j2\pi f \dfrac{C_f C_S + C_S C_{in} + C_f C_{in}}{g_{m\text{-}CVC} C_f}}. \qquad (4\text{-}88)$$

Moreover, for the integrator amplifier we have:

$$H_{vni}(f) = \frac{(C_{int} + C_S)/C_{int}}{1 + j2\pi f\, C_S / g_{m\text{-}int}}. \qquad (4\text{-}89)$$

As shown in section 4-5, in the case that $t_d << \tau_{pa}$, an OTA preamplifier in the comparator acts as an integrator. The integration time t_d is the time interval from the starting moment that the preamplifier enters its linear region up to the decision time (Fig. 4-10). The jitter caused by the voltage noise at the comparator input in continuous mode can be calculated in the following way:

The spectral noise density of the output current $i_{n\text{-}pa}$ of the comparator OTA preamplifier with transconductance $g_{m\text{-}pa}$ is:

$$S_{in\text{-}pa} = g_{m\text{-}pa}^2 S_{vn\text{-}comp\text{-}in}, \quad . \qquad (4\text{-}90)$$

This noise is filtered by the integration filter with transfer function $H_4(f)$ (Fig. 4-17). Then, according to equation 4-33, the mean-squared value of the corresponding noise voltage at the preamplifier output is:

$$\overline{v_{\text{no-pa}}^2} = \int_{f=f_{\min}}^{f=\infty} S_{i\text{n-pa}}(f) H_4^2(f)\,\mathrm{d}f. \tag{4-91}$$

In the case of flicker noise, the integration cannot start from zero because the noise power is infinite. The minimum frequency $f_{\min}$ equals the reciprocal value of the measurement time T_{out}. Noise with a frequency lower than $1/T_{\text{out}}$ behaves like drift, which is eliminated by auto-calibration.
With white noise, the noise bandwidth is $1/2t_{\text{d}}$, meaning that the voltage noise at the output of the preamplifier can be calculated as:

$$\overline{v_{\text{no-pa}}^2} = S_{i\text{n-pa}} \frac{t_{\text{d}}^2}{C_{\text{o-pa}}^2} \frac{1}{2t_{\text{d}}}. \tag{4-92}$$

Then the jitter at one deciding moment $J_{v\text{n-comp-in}}$ is equal to:

$$J_{v\text{n-comp-in}}(T_{\text{ch}}) = \frac{v_{\text{no-pa}}}{\partial v_{\text{o-pa}} / \partial t}. \tag{4-93}$$

Combining equations 4-90, 4-92, 4-93 and 4-22, gives:

$$J_{v\text{n-comp-in}}(T_{\text{ch}}) = \sqrt{\frac{S_{v\text{n-comp-in}} t_{\text{d}} \omega_{\text{u-pa}}}{2GV_{\text{dd}}}}. \tag{4-94}$$

For N measurement cycles, the jitter in the output period $T_{\text{out}} = NT_{\text{msm}} = 4NT_{\text{ch}}$, including the correction factor $\sqrt{2}$, equals:

$$J_{v\text{n-comp-in}}(T_{\text{out}}) = 2\sqrt{2N} \sqrt{\frac{S_{v\text{n-comp-in}} t_{\text{d}} \omega_{\text{u-pa}}}{2GV_{\text{dd}}}}. \tag{4-95}$$

Equation 4-95 shows the amount of the jitter in output period caused by white noise at the input of the comparator. However, the noise at the input of the comparator is not white. Figure 4-27 shows a block diagram of the part of the interface used for the present noise analysis, which is the part extending from the input of the comparator preamplifier to the final jitter in the output period. As can be seen, first the equivalent noise voltage $v_{\text{n-comp-in}}$ at the output of the integrator is converted into the current $i_{\text{n-pa}}$. Then, this current is low-pass filtered by the integration filter with transfer function $H_4(f)$ (Eq. 4-32), which results in the output noise voltage v_{no}. During each chopper period, this noise voltage is sampled. According to equation 4-22, the corresponding jitter is found by dividing by the voltage slope S_{o} at the preamplifier output. Finally, the jitter is found after averaging over different chopper periods by multiplying the signal with the digital-filter transfer function $H_2(f)$, as given by equation 4-24, which represents the jitter over one full measurement time interval T_{out}. And finally the multiplication factor $\sqrt{2}$ is the correction factor, which was explained above.

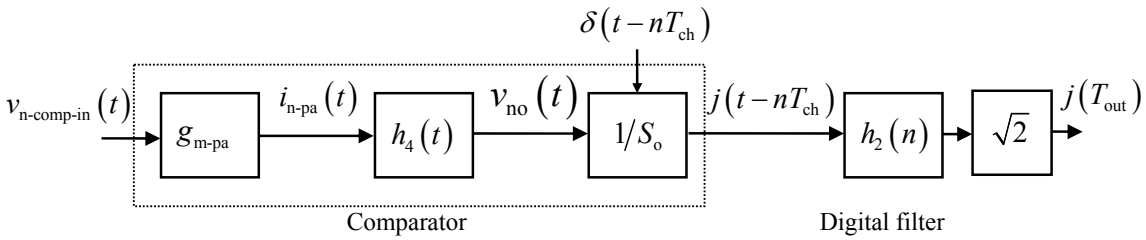

Fig. 4-27: Calculation of jitter caused by the effective noise at the input of the comparator in phase 2 over the full output period T_{out}.

If the noise voltage $v_{n\text{-comp-in}}$ at the input of the system (Fig. 4-27) is white, then due to the filter $h_4(t)$, the noise at the input of the sampler is no longer white. However, considering the effect of noise folding, the noise at the input of the digital filter with transfer function $h_2(n)$ is almost white, as will be explained now:

To understand this let us calculate the ratio of T_{ch}/t_d. We know that according to equation 4-12, $t_d < T_1/2$, and that T_2 can vary from T_1 for zero input to 4 T_1 for maximum signal input (see section 4-3). Therefore t_d is at least 4 times shorter than $T_{ch}=T_1+T_2$. The top curve in figure 4-28 shows the effect of folding the normalized sinc-type-spectrum for $t_d= T_{ch}/4$. In this figure, 21 normalized sinc-functions are added together. The result is almost frequency-independent and very close to 4. Mathematically it can be proven that if we add an infinite number of normalized sinc-functions the result will be equal to T_{ch}/t_d, which in this case is 4.

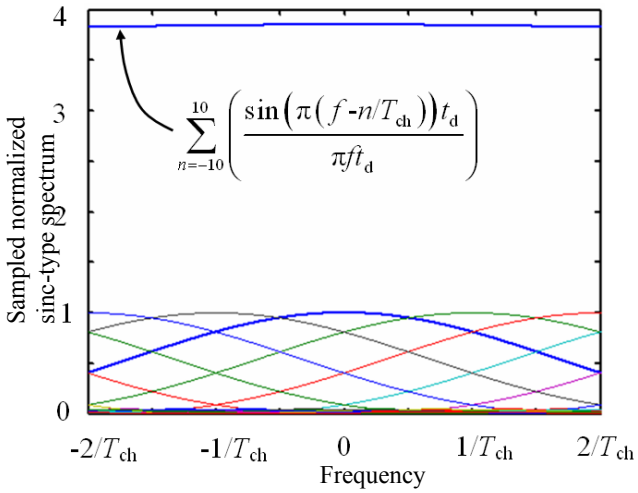

Fig. 4-28: Summing 21 normalized sinc-functions with their first notch at $t_d = T_{ch}/4$.

Knowing the noise energy and taking into account that the spectrum after sampling is white, the noise spectral density of jitter at the input of digital filter can simply be calculated as:

$$S_j(f) = g_{m\text{-pa}}^2 S_{vn\text{-comp-in}} \frac{t_d^2}{C_{o\text{-pa}}^2} \frac{1}{2t_d} \frac{1}{S_{o\text{-pa}}^2} \frac{2}{f_{ch}}, \tag{4-96}$$

so that:

$$J_{vn\text{-comp-in}}(T_{out}) = \sqrt{2} \int_{f=0}^{f_{ch}/2} S_j(f) H_2^2(f)\,df\,. \tag{4-97}$$

When the noise at the input of the system (Fig. 4-27) has flicker noise or has an arbitrary shape, then instead of calculation of the folded noise, it is easier to add the results of the filtered samples (see Eq. 4-24) for the whole range of the spectrum. Mathematically, this results in the expression:

$$J_{vn\text{-comp-in}}\left(T_{\text{out}}\right)=\sqrt{2}\int_{f=f_{\min}}^{\infty}\frac{g_{\text{m-pa}}^{2}S_{vn\text{-comp-in}}}{S_{\text{o-pa}}^{2}}H_{4}^{2}\left(f\right)H_{2}^{2}\left(f\right)\mathrm{d}f\,. \tag{4-98}$$

With the help of equation 4-98 the jitter caused by any type of noise spectrum at the input of the comparator can be calculated.

The approximate value of this jitter can be found if the comparator bandwidth is larger than the high-frequency pole of $H_{\text{vna}}(f)$ (Eq. 4-88) and $H_{\text{vni}}(f)$ (Eq. 4-89), meaning that the jitter caused by v_{na} and v_{ni} can already be calculated at the input of the comparator. The effect of the comparator noise on the jitter, taking into account the effective comparator bandwidth (see Eq. 4-37), can also be calculated at the comparator input.

Ignoring flicker noise, for a one-pole noise spectral density we have:

$$v_{\text{n}}=\sqrt{S_{\text{vn}}\left(f\right)/4\tau}\,. \tag{4-99}$$

When combining equations 4-87, 4-88, 4-89 and 4-98, and taking the comparator effective bandwidth from equation 4-37, we find for the total noise voltage $v_{\text{vn-comp-in}}$ at the input of the comparator that:

$$v_{\text{n-comp-in}}=\sqrt{\frac{S_{\text{vna}}g_{\text{m-CVC}}\left(C_S/C_{\text{int}}\right)^{2}\left(C_{\text{f}}+C_{\text{in}}\right)^{2}}{4\left(C_{\text{f}}C_{\text{S}}+C_{\text{S}}C_{\text{in}}+C_{\text{f}}C_{\text{in}}\right)C_{\text{f}}}+\frac{S_{\text{vni}}g_{\text{m-int}}\left(C_{\text{int}}+C_{\text{S}}\right)^{2}}{4C_{\text{S}}C_{\text{int}}^{2}}+S_{\text{vnc}}\frac{1}{2}\sqrt{\frac{G\omega_{\text{u}}}{V_{\text{dd}}}}}\,. \tag{4-100}$$

With equation 4-11, for the jitter at one deciding moment T_{ch} it is found that:

$$J_{vn\text{-comp-in}}=\frac{C_{\text{int}}}{I_{\text{int}}}v_{\text{n-comp-in}}\,. \tag{4-101}$$

For the following equation, we ignore the correlation between the jitter at the different deciding moments, for one complete output period $T_{\text{out}} = 4NT_{\text{ch}}$, and consider the fact that among the 4 deciding moments of each measurement cycle T_{msm}, only two of them with doubled effect appears in the final jitter, giving us:

$$J_{vn\text{-comp-in}}=2\sqrt{2N}\,\frac{C_{\text{int}}}{I_{\text{int}}}v_{\text{n-comp-in}}\,. \tag{4-102}$$

Example 4-6: With $g_{\text{m-int}}$ =300 µA/V, $S_{\text{vni}} = S_{\text{vnc}} = 3.24\times10^{-16}\text{V}^2/\text{Hz}$ (18 nV/√Hz), C_{int}=10pF, C_{p}=50pF, 40 MHz unity-gain-bandwidth for comparator preamplifier, and if the other parameters are the same as in example 4-4, the three different terms in equation 4-100 equal 3.1×10^{-8} V, 9.7×10^{-9} V, and 3.63×10^{-10} V for the CVC amp, the integrator amp, and the comparator, respectively. The result is that the jitter caused by the total noise at the comparator input amounts to 32ns.

4-6-3 Quantization noise

The differences between the actual analog value and quantized digital value of the measured time intervals are called quantization errors. The process of time quantization is shown in figure 4-29. Since the clock signal and the signal which is being quantized are not synchronized, there are random errors at the beginning and at the end of the measured time interval T.

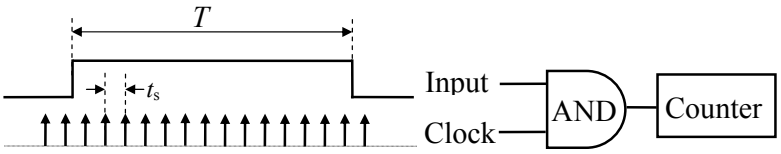

Fig. 4-29: The process of quantization.

This random error has a uniform distribution from $-t_s/2$ to $+t_s/2$. With the errors at the beginning and at the end of a time interval, the standard deviation of the quantized time is [3]:

$$\sigma_T \approx \frac{t_s}{\sqrt{6}}. \tag{4-103}$$

For a 70 MHz clock frequency, this jitter is 6 ns.

The relative jitter ε_q equals:

$$\varepsilon_q \approx \frac{1}{\sqrt{6}} \frac{t_s}{T}. \tag{4-104}$$

For the case that the noise is dominated by quantization noise, the resolution is shown in figure 4-30 for two different clock frequencies.

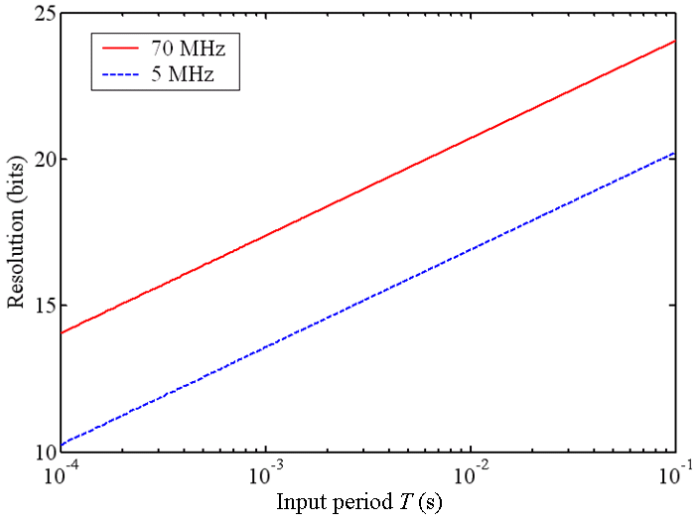

Fig. 4-30: The resolution versus the measurement time for two different clock frequencies for the case that the effect of quantization noise is dominant.

The relative error caused by quantization noise, decreases linearly with increasing measurement time T (see Eq. 4-104). While the jitter caused by the thermal noise of the

interface decreases with the square root of the measurement time T. Therefore, in fast measurements quantisation noise will be dominant.

Example 4-7: With the parameters of examples 4-2 to 4-6 and a 70 MHz clock frequency, (6 ns quantization noise), the total jitter for that conditions amounts to 46 ns. It is clear that our analysis is based on a great deal of approximation, for instance, it ignores all correlation. Moreover we ignored flicker noise. Also we supposed that the filtering effect of the comparator preamplifier on the noise of the previous stage can be ignored. When including all these details, using a more accurate calculation with Matlab, we found that the resolution amounts to 52 ns.

4-6-4 Translation of jitter to the resolution

For C_{ref1} = 0pF and $C_{ref2} = C_{ref}$, and with $T_{ref1} = T_{off}$ and $T_{ref2} = T_{ref}$, equation 3-11 can be rewritten as:

$$C_x = \left(\frac{T_x - T_{off}}{T_{ref} - T_{off}} \right) C_{ref} = MC_{ref} . \tag{4-105}$$

Ignoring the correlation between different periods we have:

$$\sigma_{Cx}^2 = \left(\frac{\partial M}{\partial T_x} \right)^2 \sigma_{Tx}^2 + \left(\frac{\partial M}{\partial T_{off}} \right)^2 \sigma_{Toff}^2 + \left(\frac{\partial M}{\partial T_{ref}} \right)^2 \sigma_{Tref}^2 . \tag{4-106}$$

Considering the different sources of jitter, we can find that only the jitter caused by the current source is different for the different periods T_x, T_{off} and T_{ref}. If we suppose the jitter caused by the current source is not dominant, which is the case for the series of examples in this chapter, the jitter in the different output periods is almost the same. So it holds that: $\sigma_{Tx} \approx \sigma_{Toff} \approx \sigma_{Tref} = \sigma_T$. With this approximation and with the value of M from equation 4-105, equation 4-106 can be rewritten as:

$$\sigma_{Cx}^2 = \frac{\left(T_{ref} - T_{off}\right)^2 + \left(T_x - T_{off}\right)^2 + \left(T_{ref} - T_x\right)^2}{\left(T_{ref} - T_{off}\right)^4} \sigma_T^2 C_{ref}^2 . \tag{4-107}$$

Example 4-8: For the same condition as in the previous examples it holds that: T_{off}=1.28 ms, T_{ref}=3.2 ms and T_x=2.24 ms. If we take σ_T = 46 ns from example 4-7, than according to equation 4-107, a standard deviation of 29.3 aF is found for the capacitance measurement. This value is quite close to the measured standard deviation of 33 aF which is presented in the next chapter.

From equation 4-107 it can be concluded that the resolution for C_x depends on the value of T_x and therefore depends on the value of C_x. Figure 4-31 shows the resolution for the conditions of example 4-8, when C_x changes from 0 pF to C_{ref}=1pF. From equation 4-107, mathematically it can easily be proven that the noise at C_x = 0 pF and $C_x = C_{ref}$ is 15% higher than $C_x = C_{ref}/2$.

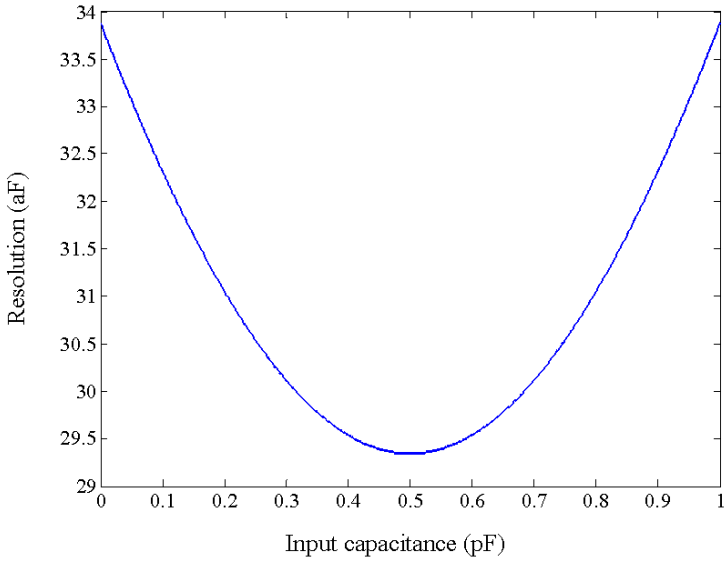

Fig. 4-31: The resolution in aF versus the input capacitance in pF for 1 pF range.

4-7 The effect of PCB parasitics

In chapter 3, section 3-3-2 we showed how the effect of sensor and/or cable parasitic capacitance can significantly be reduced by applying the two-port measurement technique. However, in this section we will discuss the effect of parasitic capacitors that are in parallel to our sensor and reference capacitors. These parasitic capacitances, which are partly due to the wiring on the PCB and the chip, can create significant errors. Figure 4-32 shows the capacitance-to-voltage converter for a floating capacitor, where in addition to C_x the reference capacitors C_{ref1} and C_{ref2} are also shown.

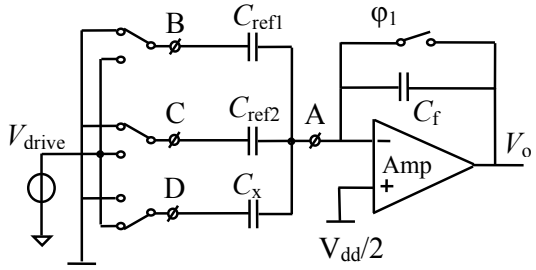

Fig. 4-32: A Capacitor-to-voltage converter.

Although equations 3-8 to 3-11 are valid, the effects of parasitic capacitance are not included in those equations. Parasitic capacitances are found between any pair of conductors. Figure 4-33(a) shows these parasitic capacitances for the circuit of the figure 4-33.

Since drive pins B, C and D are always connected to a voltage source, the parasitic capacitances C_{pBD}, C_{pBC} and C_{pCD} can be ignored. Figure 4-33(b) shows the simplified circuit.

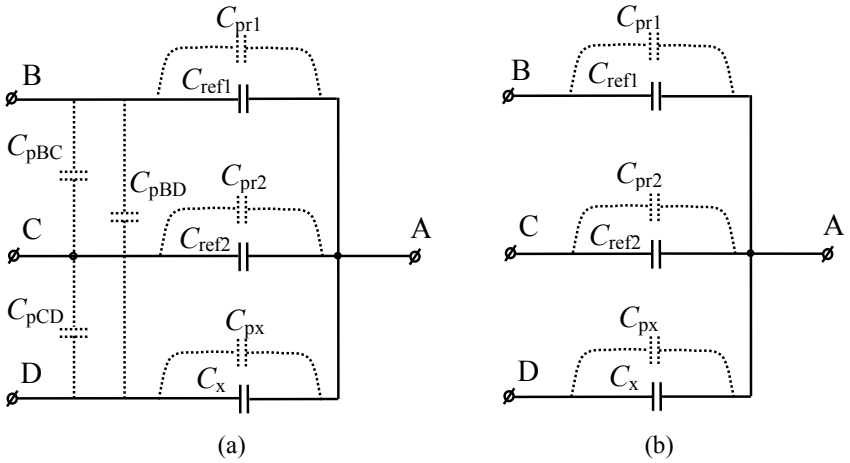

Fig. 4-33: The parasitic capacitance between different pins in the interface.

With the PCB parasitic capacitances between pin A and one of the three pins B, C, D, equations 3-8 to 3-11 can be rewritten as:

$$T_{ref1} = A\left(C_{ref1} + C_{pr1}\right) + B, \tag{4-108}$$

$$T_{ref2} = A\left(C_{ref2} + C_{pr2}\right) + B, \tag{4-109}$$

$$T_x = A\left(C_x + C_{px}\right) + B\,, \tag{4-110}$$

$$C_x = \left(\frac{T_x - T_{ref1}}{T_{ref2} - T_{ref1}}\right)\left(\left(C_{ref2} - C_{ref1}\right) + \left(C_{pr2} - C_{pr1}\right)\right) + C_{ref1} + \left(C_{pr1} - C_{px}\right). \tag{4-111}$$

The shielding of pin A would be the best solution to reduce the effect of these parasitic capacitances. However, complete shielding is not possible, at neither the chip level nor the PCB level. Further decrease of these parasitics can be achieved by maximizing the distance of pin A and its related conductors with respect to the pins B, C and D and their conductors at both the chip and PCB level. Moreover, since only the differential capacitances (C_{pr1} - C_{px}) and (C_{pr2} - C_{pr1}) affect the measurement result, a symmetrical design of the terminal (pin) configurations at both chip level and PCB level will considerably decrease the influence of these parasitic capacitors.

Comparing equation 4-111 with equation 3-12 shows that these parasitic capacitances can create an offset error as well as a gain error. However, both of these errors can be removed during system-level calibration. For instance, when measuring displacement with a capacitive sensor (chapter 2), the system can be calibrated at two reference points. In that case the remaining error in the displacement measurement is due to a nonlinearity error, a resolution error (i.e. noise), and the calibration error, but not the error due to these parasitics. Yet a higher accuracy can be obtained using initial calibration with offset capacitors, with two additional measurements: First we measure $T_{ref1,0}$, $T_{ref2,0}$ and $T_{x,0}$ in the absence of the three input capacitances, C_{ref1}, C_{ref2} and C_x. Next we measure $T_{x,C1}$ by applying a well-known, non-zero capacitor as C_x ($C_x = C_1$). The gain factor of the capacitance-to-period converter and the differential parasitic capacitances can be calculated from the equations:

$$A = \frac{T_{x,C_1} - T_{x,0}}{C_1}, \tag{4-112}$$

$$\left(C_{\text{pr2}} - C_{\text{pr1}}\right) = \frac{T_{\text{ref2,0}} - T_{\text{ref1,0}}}{A}, \tag{4-113}$$

$$\left(C_{\text{pr1}} - C_{\text{px}}\right) = \frac{T_{\text{ref1,0}} - T_{\text{x,0}}}{A}. \tag{4-114}$$

Combining equations 4-111 to 4-114, the value of C_x can be extracted independent from the value of parasitic capacitances C_{pr1}, C_{pr2} and C_{px}.

This is one of the challenges of precision capacitance measurements. Since these parasitic capacitances strongly depend on the PCB board, the PCB designer should have enough knowledge about these details. However, if instead of an interface chip we provide the complete capacitive sensor measurement system, then even users with less expertise can use it.

4-8 The nonlinearity error

There are two major sources of nonlinearity in our interface: the nonlinearity of the capacitance-to-voltage converter and the voltage dependency of the integrated capacitors. Depending on the quality of the feedback and the reference capacitors C_f and C_{ref}, dielectric absorption can also be a source on nonlinearity. In this section, the effects of these sources of nonlinearities are discussed as well.

4-8-1 The nonlinearity of capacitance-to-voltage converter

For two reasons the capacitance-to-voltage converter shows nonlinear behavior: Firstly because of the limited open-loop gain of the amplifier, and secondly because this gain itself is nonlinear.

4-8-1-1 The nonlinearity due to limited open-loop gain of the CVC

In this section, we suppose that the open-loop gain of the CVC (Fig. 4-34) in its active region is constant. The capacitor C_{in} is one of the three input capacitors C_x, C_{ref1} or C_{ref2}.

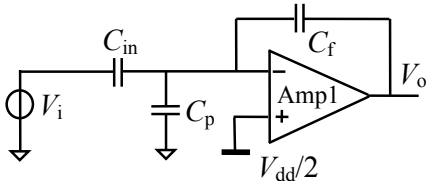

Fig. 4-34: The capacitance-to-voltage converter.

If we suppose that the amplifier is ideal, then it holds that:

$$V_{\text{o}}\big|_{\text{Ideal}} = \frac{V_{\text{dd}}}{2} - \frac{V_{\text{i}} C_{\text{in}}}{C_{\text{f}}}. \tag{4-115}$$

However, in case of limited gain A of the amplifier, the output voltage V_o is:

$$V_{\text{o}} = \frac{V_{\text{dd}}}{2} - \frac{A V_{\text{i}} C_{\text{in}}}{C_{\text{in}} + C_{\text{p}} + \left(1 + A\right) C_{\text{f}}}, \tag{4-116}$$

The input voltage V_i can have transitions from V_{dd} to 0V, or vise versa. In that case, the peak-to-peak output voltage $V_{o\text{-}pp}$ (Fig. 4-2(b)) amounts to:

$$V_{o\text{-}pp} = \frac{2AV_{dd}C_{in}}{C_{in} + C_p + (1+A)C_f}. \qquad (4\text{-}117)$$

From equation 4-117 it can be concluded that in the case of a limited open-loop gain, the transfer function $V_{o\text{-}pp}/C_{in}$ depends on the input capacitance C_{in} and is thus nonlinear.

The nonlinearity can be defined in many different ways (see Appendix A, section A-4). However, in line with the use of three-signal auto-calibration, we have chosen to define the nonlinearity error to be zero at the two reference points $C_x = C_{ref1}$ and $C_x = C_{ref2}$. In this way, the nonlinearity error is the nonlinearity error after a two-point calibration. When the two reference capacitors are selected to be equal to 0 pF and the maximum value of C_x, then the nonlinearity error is the same as the nonlinearity error that is calculated based on the end-point method. Figure 4-35 shows the nonlinearity error for $C_{x,min}= C_{ref1}= 0$pF, $C_{x,max}= C_{ref2}= 0.3C_f$, $C_p =0$pF, and $A =10^4$. The value of parasitic capacitance C_p can hardly make any difference in nonlinearity due to limited gain because $C_p << (1+A)C_f$. Therefore $C_p = 0$pF is used for figure 4-35.

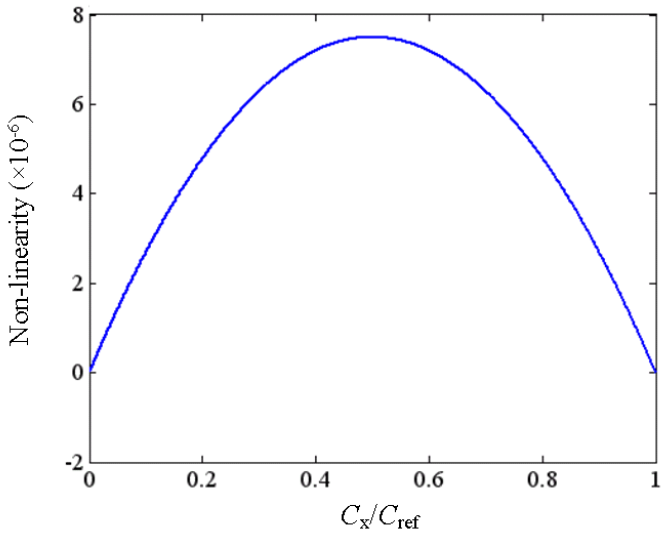

Fig. 4-35: The nonlinearity error caused by the limited gain of CVC amplifier.

It is clear that even with $A =10^4$, which is quite easy to implement, the maximum nonlinearity error is less than 8 ppm. However as we will see in next section, most of the nonlinearity is caused by the fact that this gain is not linear.

4-8-1-2 The nonlinearity of the CVC due to the nonlinearity of the open-loop gain

Due to the nonlinear properties of the amplifier component, the overall gain is nonlinear as well. The main source of this nonlinearity is due to the output resistances of the MOS transistors, which are a nonlinear function of the drain-source voltage V_{ds} [15]. Figure 4-36 shows the low-frequency small-signal gain a of a one-stage OTA with a cascoded output stage versus its DC output voltage while its input DC voltage is kept constant.

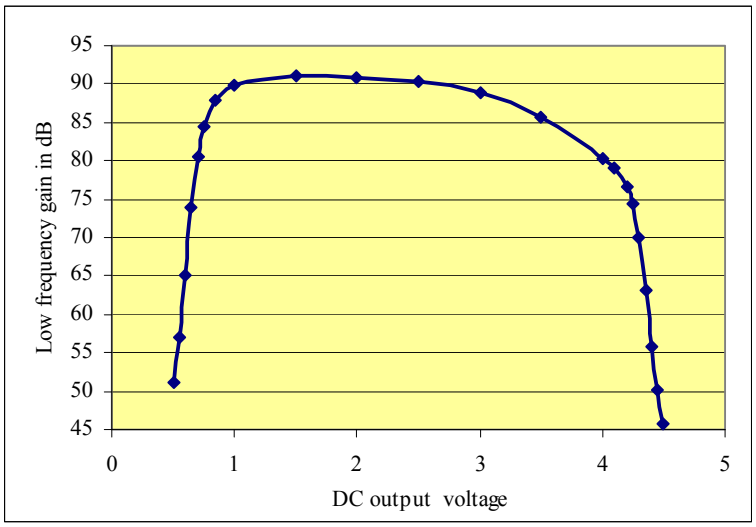

Fig. 4-36: A typical gain of an amplifier versus its output DC voltage.

The gain a is defined as:

$$a = \frac{\partial V_o}{\partial V_i}. \tag{4-118}$$

The sharp decline below 1V and above 4V is because of the approach of the saturation region of the amplifier; however, as we expect, the gain even in middle part is not constant.

However, the gain factor A in equation 4-117 is the large-signal gain defined by equation 4-119:

$$A = \frac{V_o - V_{o,Q}}{V_i - V_{i,Q}}, \tag{4-119}$$

where $V_{o,Q}$ is the quiescent point voltage at the output, which is V_{dd} /2; $V_{i,Q}$ is the quiescent point voltage, which is equal to the input offset voltage v_{io} plus V_{dd} /2. In simulation v_{io} is the systematic offset. To find the large-signal gain of the amplifier by simulation, we used the circuit depicted in figure 4-37.

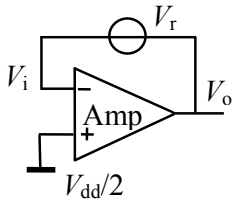

Fig. 4-37: The circuit used to find static and dynamic gain by simulation.

Voltage source V_r is a ramp voltage and its voltage value is selected in such a way that the output voltage V_o remains in the range of the output swing of the amplifier. Figure 4-38 shows the simulated small-signal and large-signal gain of the CVC amplifier.

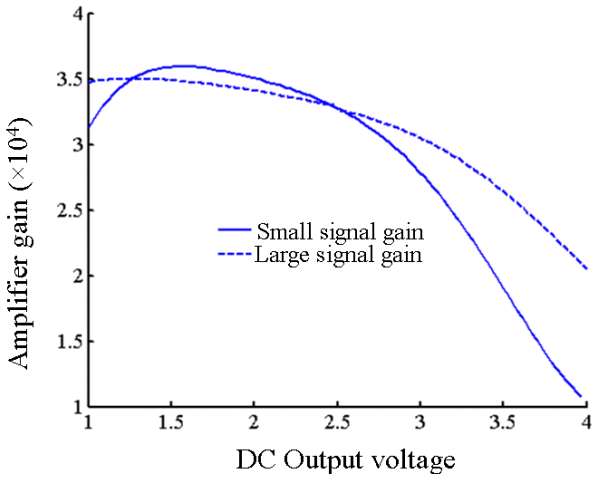

Fig. 4-38: The simulated large-signal and small-signal gain of the CVC amplifier versus DC output voltage.

The effect of this nonlinearity is reduced in two ways: a) by negative feedback, and b) by auto-calibration. From equation 4-117 it is clear that the nonlinearity in the open-loop gain causes more nonlinearity in the CVC for larger parasitic capacitance C_p.

Example 4-9: Suppose an amplifier with the characteristics of figure 4-38 is used as the CVC amplifier. Moreover, we suppose that $C_{x,min} = C_{ref1} = 0$pF, $V_i = 5$V and $C_{x,max} = C_{ref2} = 0.3C_f$. Figure 4-39 shows the nonlinearity caused by both the limited open-loop gain and its nonlinearity for two values of the parasitic capacitance C_p.

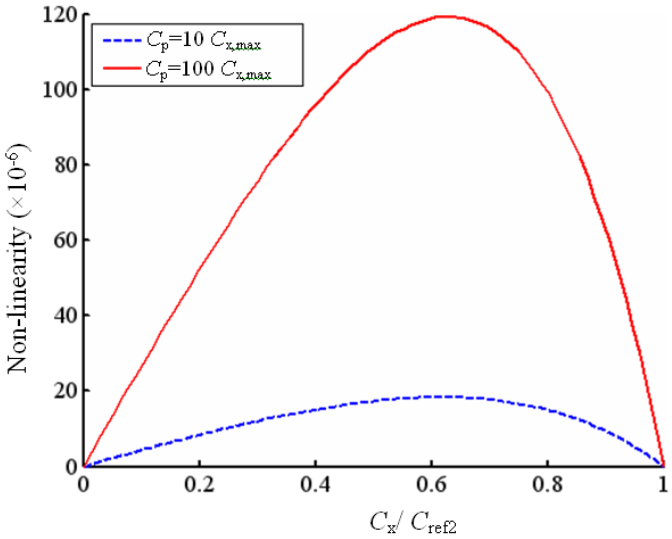

Fig. 4-39: The nonlinearity error caused by the limited and nonlinear open-loop gain of the amplifier in CVC.

The main part of this nonlinearity is caused by the gain nonlinearity rather than its limited value. Yet, increasing the gain will decrease this nonlinearity. In example 4-9 by selecting $C_{x,max} = C_{ref2} = 0.3C_f$, the maximum voltage at CVC output voltage is 1.5V around 2.5V. Therefore, the CVC output voltage can reach from 1V up to 4V. However, if we use a smaller part of the CVC amplifier output-swing, then the nonlinearity will be less. This result is also

supported by our measurement data, which will be presented in chapter 5. Moreover, modification of the CVC amplifier to have more flat gain in its active region will decrease the nonlinearity of the interface.

4-8-2 Nonlinearity of the interface caused by the voltage dependency of the integrated capacitor

As mentioned in section 4-3, one of the disadvantages of implementing C_f in the CVC with an external capacitor is that it can affect the nonlinearity of the interface. When both the feedback capacitor C_f and the sampling capacitor C_S are implemented on-chip, then their voltage dependencies will fully compensate each other.

However, when using an external capacitor for C_f, the differences in the voltage dependencies cause nonlinearity, as will be shown in this section: The on-chip capacitor C_S is a precision analog capacitor with highly-doped poly-silicon as one electrode, and highly-doped n-type on p-type substrate as the other electrode. Moreover, the dielectric material consists of 45 nm of thermal oxide.

The voltage dependency of a capacitor can be modeled as:

$$C(V) = C_0\left(1 + c_1 V + c_2 V^2 + \cdots\right). \tag{4-120}$$

For a precision analog capacitor in the applied technology (0.7 μm CMOS technology), typical values of the voltage-dependency parameters are: $c_1 = 25$ ppm/V, and $c_2 = 5$ ppm/V^2.

According to figure 3-9, the applied voltage ($V_{o\text{-}CVC} - V_{DD}/2$) over C_S is a symmetrical voltage around 0V. This means that the effect of the first-order voltage dependency is removed by the kind of chopper we have applied in our system. However, the second-order voltage dependency will cause nonlinearity.

Example 4-10 If the CVC output voltage for C_{ref1}, C_{ref2} and C_x is 0V, 1.5V and 0.5V, and that the voltage dependency of the external capacitor is zero, then the nonlinearity caused by the second-order voltage dependency of sampling capacitor amounts to 10 ppm.

It should be noted that the voltage dependency of the integrator capacitor cannot create nonlinearity because at the deciding moment the voltage across it is always almost zero.

4-8-3 Nonlinearity of the interface caused by dielectric absorption of the capacitor.

Dielectric absorption is a physical effect occurring in the dielectric of a capacitor and can be modeled as in figure 4-40, where C_x represents the ideal part of the capacitor, and the other components form *RC* branches which model the dielectric absorption [8]. The physical explanation of such an effect is that the polarization and depolarization of dipoles in dielectric material takes time.

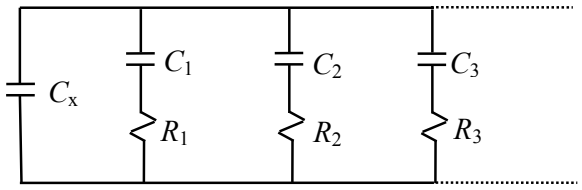

Fig. 4-40: Model of dielectric absorption.

To see how good or bad a capacitor is in terms of dielectric absorption, we can charge a capacitor to a voltage V_{ch} for very long time and then short-circuit it for a short amount of time. The recovered voltage across the capacitor after re-opening the switch is an indication of dielectric absorption [8]. The reason is clear: during the charging process $t_{ch} > R_i C_{i(max)}$, all capacitors with different time constants will be charged. However during discharge over a short time interval $t_{dis.ch} < R_i C_{i(min)}$, the main capacitor C_x is discharged, but the other capacitive components still have some charge, which after charge redistribution yields a final voltage V_f (Fig. 4-41), which amounts to:

$$V_f = V_{ch} \sum_{i=1}^{n} C_i \Big/ \left(\sum_{i=1}^{n} C_i + C_x \right). \tag{4-121}$$

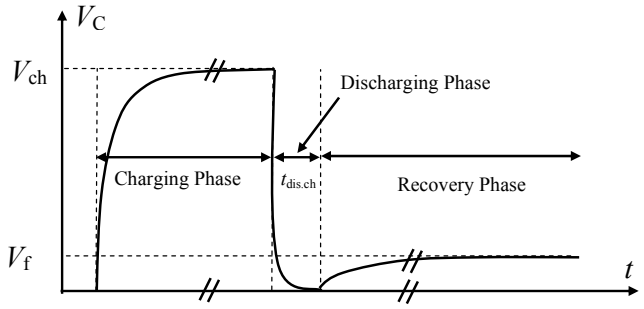

Fig. 4-41: Voltage across the capacitor in different time intervals, charging phase, discharge phase, and recovery phase.

In the experiment mentioned above, the ratio of $(\sum C_i)/C_x$ can be extracted; however, by repeating the experiment for different discharge times, more information about the individual time constant can be produced.

In this section we find the effect of dielectric absorption on the nonlinearity of the relaxation oscillator. It is quite clear that the effective capacitance value in figure 4-40 is frequency-dependent. This effective capacitance value changes from C_x for very high frequencies to $C_x + \sum C_i$ for very low-frequencies. To analyze the effect of dielectric absorption on nonlinearity of relaxation oscillator, let us suppose that all the capacitors in our system are ideal and only the feedback capacitor in the CVC shows a significant amount of dielectric absorption. Then, if for all capacitor branches, the oscillator frequency is much lower or much larger than $1/2\pi C_i R_i$, the effective capacitance value will remain almost constant when the frequency is being modulated by the input signal. In this condition dielectric absorption will not create nonlinearity. However, when the oscillator frequency is close to $1/2\pi C_i R_i$, for any of the branches, the input signal will modulate the effective value of this capacitor by modulating the frequency of the relaxation oscillator, which causes nonlinearity.

In our setup, using a ceramic NP0 type capacitor we found that the nonlinearity caused by dielectric absorption is not a dominant source of nonlinearity, and therefore we did not investigate it in more depth.

4-9 A method for measurement of the nonlinearity

The measurement of the nonlinearity requires some care. In a straightforward way, one could expect it to be possible to measure first the values of three or more reference capacitors with a

(very) precise impedance analyzer and afterwards insert these reference capacitors one-by-one into the test setup. In practice, this method does not work well. In the first place, the nonlinearity of the interface circuit is so small that it is difficult to find impedance analyzers with sufficient accuracy. Moreover, when moving the reference capacitors to another position, the magnitude of the parasitic capacitances changes as well. Therefore, this method cannot be used to measure the nonlinearity of a high-performance system.

In [3] a method is presented in which the interface nonlinearity is derived from the measurement of two stable capacitances: C_{ref1} and C_{ref2} and $C_{\text{ref1}} + C_{\text{ref2}}$.

In that method, the nonlinearity is found using the equation [3]:

$$\lambda = \frac{T_{C_{\text{ref1}}+C_{\text{ref2}}} - T_{\text{off}}}{T_{C_{\text{ref1}}} + T_{T_{C_{\text{ref2}}}} - 2T_{\text{off}}} - 1, \tag{4-122}$$

where T_{Cref1}, T_{Cref2}, $T_{\text{Cref1+Cref2}}$ and T_{off} are the output periods corresponding to the selected capacitances C_{ref1}, C_{ref2}, $C_{\text{ref1}} + C_{\text{ref2}}$, and 0 pF, respectively. If a linear relation exists between the period time T_{i} and the capacitance ($T_{\text{i}} = AC_{\text{i}} + B$), λ in equation 4-122 equals zero. However, the presence of PCB parasitic capacitances limit the accuracy of this method.

The effects of PCB parasitic capacitances on the measurement accuracy were discussed in section 4-7. Here we will discuss the effect of these parasitic capacitances on the non-linearity measurement when using equation 4-122. Figure 4-42 shows a model of these parasitic capacitances.

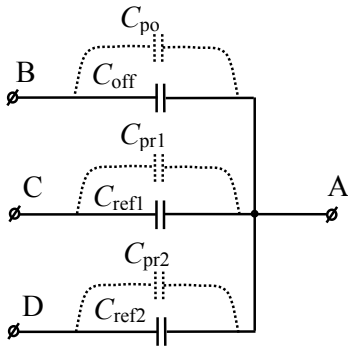

Fig. 4-42: The capacitors with related parasitic capacitances during the non-linearity measurement presented in [3].

If a linear relation exists between the period and the capacitance, at the presence of these parasitic capacitances, λ would equal:

$$\lambda = \frac{C_{\text{ref1}} + C_{\text{ref2}} + C_{\text{pr1}} + C_{\text{pr2}} - C_{\text{po}}}{C_{\text{ref1}} + C_{\text{ref2}} + C_{\text{pr1}} + C_{\text{pr2}} - 2C_{\text{po}}} - 1. \tag{4-123}$$

Therefore, according to equation 4-123, even for a 100% linear system, the value of λ does not equal zero. For instance for $C_{\text{ref1}} = C_{\text{ref2}} = 1\text{pF}$ and $C_{\text{pr1}} = C_{\text{pr2}} = C_{\text{p0}} = 1\text{fF}$, λ equals to 5×10^{-4}.

In order to be less sensitive to the effects of parasitic capacitances, a modified method is presented in [19]. For this purpose, instead of three capacitance values: C_{ref1}, C_{ref2} and $C_{\text{ref1}} + C_{\text{ref2}}$, four capacitance values: C_{ref1}, C_{ref2}, $C_{\text{ref1}}+C_{\text{ref3}}$, and $C_{\text{ref2}}+C_{\text{ref3}}$ are measured (Fig. 4-43).

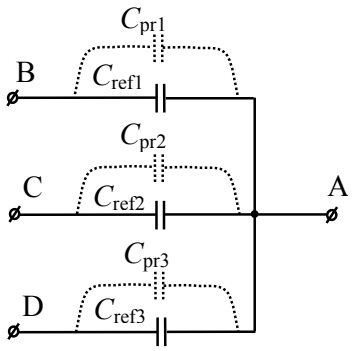

Fig. 4-43: The capacitors with related parasitic capacitances for non-linearity measurement presented in [19].

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The nonlinearity λ_m is calculated according to the equation [19]:

$$\lambda_m = 1 - \frac{T_{C_{ref2}+C_{ref3}} - T_{C_{ref1}+C_{ref3}}}{T_{C_{ref2}} - T_{T_{C_{ref1}}}}. \qquad (4\text{-}124)$$

The measurement should be arranged in such a way that no parasitic capacitances (parasitic capacitances of PCB) are changed during the measurement. This means that not only the wiring of the setup, but also the position of any of the conductors should be invariable [20]. Therefore, the measurement can be performed by just changing the amplitudes of the various excitation voltages.

It can easily be proven that in equation (4-124) the presence of PCB parasitic capacitances will not affect the measured linearity.

For the measurement of very small nonlinearities, a drawback of the method presented in [19] is that it is sensitive to drift caused by changes of the interface temperature. The drift problems can be solved by using auto-calibration [4]. In this case, instead of measuring periods, we measure the *M*–values using 3-signal measurements, which is a special type of auto-calibration [4]. The M-values are calculated using the equation:

$$M = \frac{T_x - T_{off}}{T_{ref} - T_{off}}. \qquad (4\text{-}125)$$

To apply this method, we measured four values of the capacitance C_x. As mentioned above, when measuring small nonlinearities we cannot rely on absolute accuracy. However, by selecting the four C_x-capacitors values ($C_1 = C_{x1}$, $C_2 = C_{x2}$, $C_3 = C_{x1} + C_{x3}$ and $C_4 = C_{x2} + C_{x3}$) with the help of an external multiplexer (Fig. 4-44) –independent of the absolute accuracy of these four capacitors values and with high immunity for the related parasitic capacitances– a modified nonlinearity parameter λ_{mod} can be defined as:

$$\lambda_{mod} = 1 - \frac{M_{Cx2+Cx3} - M_{Cx1+Cx3}}{M_{Cx2} - M_{Cx1}}. \qquad (4\text{-}126)$$

The value of λ_{mod} depends on the selected capacitors. Although the value of λ_{mod} defined by equation 4-126 is a good indicator of for nonlinearity and can be used to compare two different interfaces or two different conditions of a single interface, it would be better to translate the results of equation 4-126 into, for instance, a maximum nonlinearity error when we use end-point fitting (Appendix A). The effect of this can be graphically demonstrated with figure 4-45.

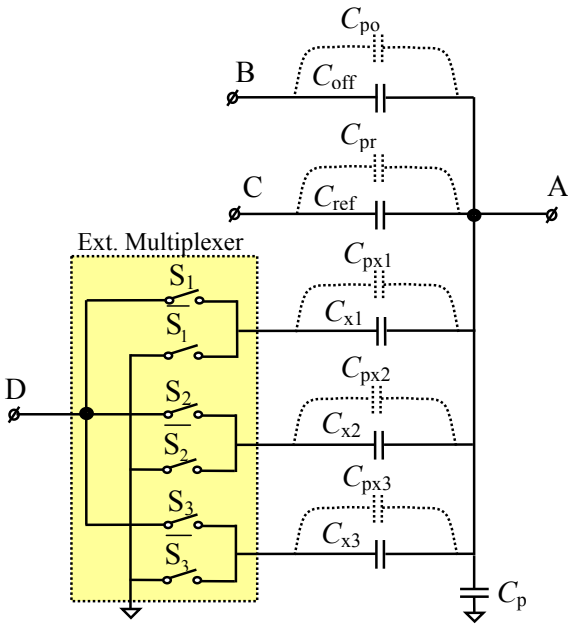

Fig. 4-44: The capacitors with related parasitic capacitances for non-linearity measurement presented in this work.

We first assume that the nonlinearity is parabolic (as predicted by the theoretical analysis in section 4-8). Next, we select the capacitor C_{x1} in the vicinity of 0 pF, the capacitors C_{x2} and C_{x3} in the vicinity of $C_{x,max}/2$, and the capacitor C_{x4} in the vicinity of $C_{x,max}$, and then indicate the related values of λ_{mod} as $\lambda_{mod(0,0.5,0.5,1)}$. Using figure 4-45 and equation 4-126, with some approximation it can be shown that:

$$\lambda_{\mathrm{mod}(0,0.5,0.5,1)} = 1 - \frac{\left(M_{\mathrm{Cx2+Cx3}} - M_{\mathrm{Cx1+Cx3}}\right)/\left(C_{\mathrm{x2}} - C_{\mathrm{x2}}\right)}{\left(M_{\mathrm{Cx2}} - M_{\mathrm{Cx1}}\right)/\left(C_{\mathrm{x2}} - C_{\mathrm{x2}}\right)} = 1 - \frac{1-\gamma}{1+\gamma} \approx 2\gamma. \qquad (4\text{-}127)$$

Therefore, the maximum nonlinearity error ε_m in full-scale span (FSS) with end-point fitting amounts to:

$$\varepsilon = \frac{\lambda_{\mathrm{mod}(0,0.5,0.5,1)}}{4} \approx \frac{\gamma}{2}. \qquad (4\text{-}128)$$

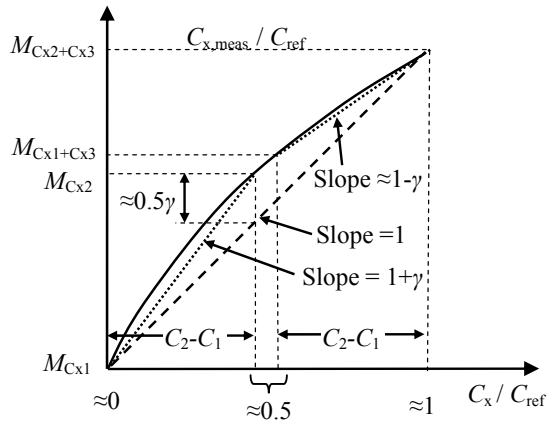

Fig. 4-45: Translation of the measured non-linearity defined by equation 4-126 to maximum nonlinearity error in FSS with end-point fitting.

4-10 Conclusions

In this chapter, the structure and basic properties of the universal interface for capacitive sensors was presented. By analyzing the charge-transfer time constant, we found that the integrator current needs to be programmable. The oscillator frequency, which is inversely proportional to this current, can be set by the user to optimize the interface performance for user-specific applications. In addition to this, a programmable digital divider is available to match the data acquisition rate with the bandwidth of the physical sensor signal. Finally, with an off-chip capacitor, the user can set a desired capacitor range.

It was shown that the effect of delay caused by the comparator is compensated for by the applied auto-calibration. Therefore, there is no need for a fast comparator. This is very important for the noise performance of the interface because a significant part of noise can be removed by filtering with the (slow) input stage of the comparator. An extended noise analysis was presented. For each noise source we categorized the noise in three spectral categories. Then, after calculating and analyzing the transfer functions of the chopper, the averaging filter, the integration filter, the comparator, and also the auto-calibration process, we showed how to calculate the effect of each noise source on the final jitter.

The effect of PCB parasitic capacitances on measurement accuracy was discussed. We showed how to minimize the effect of these parasitic capacitors. It has been advised that for more accurate measurements an extra calibration process are necessary.

For our interface, different sources of nonlinearity were identified. We showed that the nonlinearity measurement needs special care in order not to be sensitive to PCB parasitic capacitances. A new, more adequate method to measure and to characterize nonlinearity was presented. It was shown that this method is immune to the effects of parasitic capacitances.

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CHAPTER 5

A flexible high-resolution interface for floating capacitor

5-1 Introduction

As mentioned in chapter 3, one of the main challenges for capacitive-sensor interfaces is to achieve a high resolution for sensors with large signal bandwidth. This combination of features is required for mechanical sensors applied in control systems, such as dynamic displacement sensors in a servo system. Especially when the power budget is limited, it is not easy to meet the target specifications for such a system [1]. For such applications we tried to extend the limits of resolution and speed. To do so, we designed an interface with optimized noise performance, while using the results of the noise analysis presented in chapter 4. In addition to this design, in chapter 6, 7 and 8 we will present three other designs, but in none of these the noise is a main issue and therefore they have almost the same noise performance as the UTI [2, 3].

To obtain the best noise performance, in the design presented in this chapter we applied several modifications, which are: 1) using a band-limited comparator instead of a fast comparator (chapter 4, section 4-5); 2) designing the integrator current to have a flicker-noise corner frequency that is lower than the data-acquisition rate $1/T_{3\text{-sig.}}$ (chapter 4, section 4-6-2-1); and 3) achieving the highest noise performance while keeping the systematic error below the limit by selecting the interface frequency in relation to the sensor conditions.

The interface with optimized noise performance is designed and implemented in 0.7 μm standard CMOS technology. The measurement results, which are in close agreement with our theoretical analysis, show that with a measurement time of 1s a resolution of 20 bits is achievable while consuming only 5 mW. This resolution corresponds to 1 aF for a 1 pF range. Moreover we will show how easily the user can modify the interface for the best noise performance under specific conditions while keeping the systematic error within the error budget.

5-2 Design considerations for the interface

Figure 5-1(a) shows the block diagram of the interface which is the same as the block diagram shown in figure 4-1 with $C_{ref1} = 0$pF, $C_{ref2} = C_{ref}$, and the defined control signals which are based on our analysis in chapter 4. Its output signal is shown in Fig. 5-1(b). The MUX is a selector which selects one of three possible input capacitors. The following signal-processing component is a capacitance-to-voltage converter CVC (Fig. 3-7(a)). The next signal-processing stage is a voltage-to-period converter (VPC), which is implemented with a relaxation oscillator (Fig. 3-9(a)), and which converts the CVC output voltage into a period time. To eliminate the undesired effects of transfer-parameter drift, auto-calibration is used (see chapter 3). To do so, in addition to input capacitance C_x, an offset capacitor $C_{off} \approx 0$pF and a reference capacitor C_{ref} are also measured in the same way as the measurand capacitor C_x. To implement this method, a multiplexer (MUX) is used to connect the selected capacitor to the capacitance-to-voltage converter (CVC). Pin B (Fig. 5-1), which is intended for the offset measurement, can also be used to connect a capacitor $C_{off} > 0$pF as a second reference capacitor. This could be a good option for application in which the minimum value of the

measurand capacitor C_x is much larger than 0 pF. For instance, when 10 pF < C_x < 12 pF, it might be better to use reference capacitors with values close to the minimum and maximum values. In order not to saturate the CVC amplifier, for the capacitance C_f it should hold that $C_f > 3.3\ C_{x,max}$. However, as will be explained in section 5-5-8, a larger C_f value of $4.7C_{x,max}$ is recommended for higher linearity.

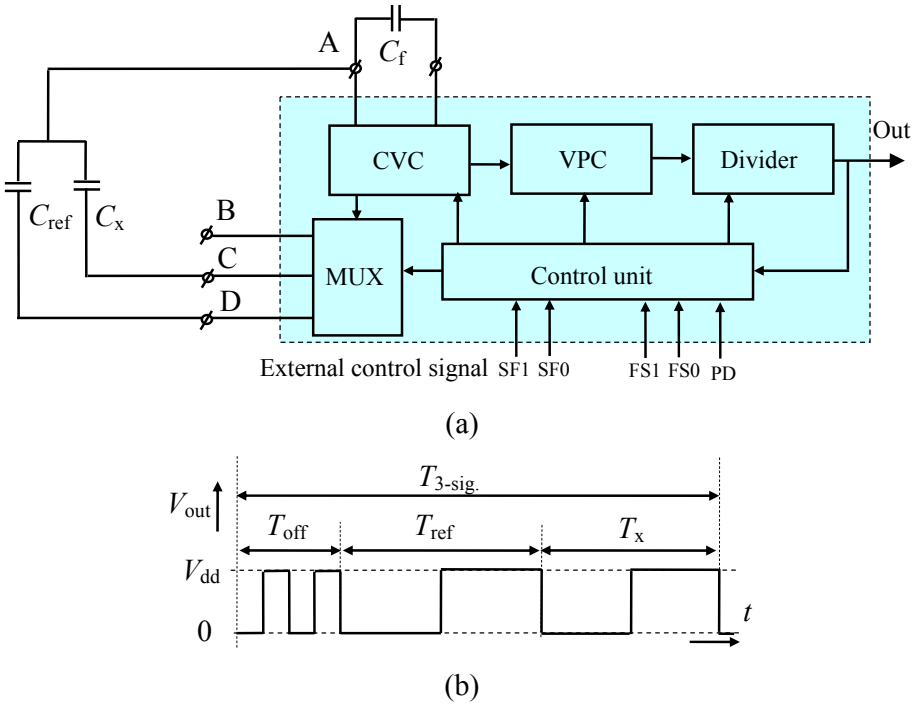


Fig. 5-1: (a) Block diagram of the interface and (b) the output signal.

The external control signals FS0 and FS1 are two digital inputs used to set the integrator current (see chapter 4, section 4-4). With these two inputs, four different integrator currents $2^n I_{ref}$ (n = 0, 1, 2, 3) can be set. In sections 5-3 and 5-4 it is shown how the user can set these inputs to achieve the highest performance with respect to noise and accuracy. The external control signal SF0 and SF1 are two digital inputs used to select the divider number (chapter 4, section 4-2). With this signal, four different measurement times $4^n t_{fast}$ (n = 0, 1, 2, 3) can be set, where t_{fast} is the shortest measurement time (in the very-high-speed mode). The measurement time setting will not have any effect on the systematic accuracy of the interface. However, as explained in chapter 4 section 4-6-3, the effect of thermal noise decreases by almost one bit per factor of 4 in measurement time.

Table 5-1 shows the calculated measurement times for $C_{x,min}$ = 0 pF, $C_{x,max} = C_{ref} = 0.3C_f$, $C_{o1} = C_{o2}$ = 1pF, $C_S = C_{int}$ = 10pF, a drive voltage with a peak-to-peak value of V_{dd} = 5V (chapter 3, Fig. 3-7(b)), and different combinations of the external control signals. For convenience of the reader, the integrator output voltage depicted in chapter 3, figure 3-9(b), is shown again in figure 5-2.

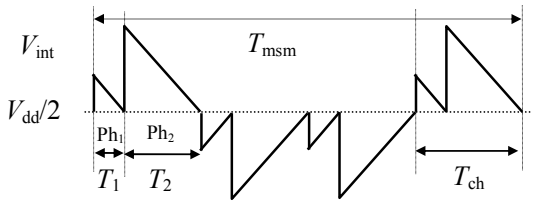


Fig. 5-2: The integrator output voltage.

The time interval $T_1 + T_2$ is equal to the chopper period T_{ch} (chapter 3, section 3-4-3) and equals:

$$T_{ch} = \frac{V_{dd}\left(C_{o1} + C_{o2}\right) + V_x C_S}{I_{int}}, \tag{5-1}$$

where V_x is the amplitude of the CVC output voltage, which is 0V and 1.5V for $C_x = C_{x,min} = 0$pF and $C_x = C_{x,max} = 0.3C_f$, respectively.

The measurement time $T_{3\text{-sig.}}$, including three-signal auto-calibration, amounts to:

$$T_{3\text{-sig.}} = 4N\left(T_{ch,min} + T_{ch,max} + T_{ch}\right), \tag{5-2}$$

where $T_{ch,min}$ and $T_{ch,max}$ are the minimum and maximum values of the chopper periods for $C_{x,min}$ and $C_{x,max}$, respectively.

Table 1: Chopper period and measurement times for different external control signals.

SF1	SF0	FS1	FS0	$N=T_{out}/T_{msm}$	I_{int}(µA)	$T_{ch,min}$(µs)	$T_{ch,max}$(µs)	$T_{3\text{-sig.,min}}$ (ms)	$T_{3\text{-sig.,max}}$ (ms)
0	0	0	0	2	0.5	20	50	0.72	0.96
0	0	0	1	2	1	10	25	0.36	0.48
0	0	1	0	2	2	5	12.5	0.18	0.24
0	0	1	1	2	4	2.5	6.25	0.09	0.12
0	1	0	0	8	0.5	20	50	2.88	3.84
0	1	0	1	8	1	10	25	1.44	1.92
0	1	1	0	8	2	5	12.5	0.72	0.96
0	1	1	1	8	4	2.5	6.25	0.36	0.48
1	0	0	0	32	0.5	20	50	11.52	15.36
1	0	0	1	32	1	10	25	5.76	7.68
1	0	1	0	32	2	5	12.5	2.88	3.84
1	0	1	1	32	4	2.5	6.25	1.44	1.92
1	1	0	0	128	0.5	20	50	46.08	61.44
1	1	0	1	128	1	10	25	23.04	30.72
1	1	1	0	128	2	5	12.5	11.52	15.36
1	1	1	1	128	4	2.5	6.25	5.76	7.68

5-3 Sources of errors

There are different sources of error, which pose different limits on the possible ranges of the input capacitance and parasitic input capacitance, which is explained in this section. At the end of this section, the user will be able to judge whether or not this interface is suitable for his/her application, and which mode would yield the highest performance for that application. Experimental results are presented in section 5-5.

5-3-1 Settling error

In chapter 4, sections 4-4 we showed that for a small capacitance range, it is better to use of an OTA instead of an op-amp for the implementation of the CVC amplifier, while for large capacitance ranges it is better to use an op-amp. In the design presented in this chapter, we use an OTA with a transconductance of 1 mA/V. For convenience of the reader, the CVC configuration is repeated in figure 5-3.

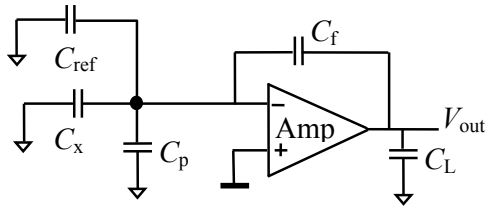


Fig. 5-3: The capacitance-to-voltage converter (CVC).

The charge transfer time constant τ_{CT} amounts to:

$$\tau_{CT} = \frac{C_f C_{in,T} + C_f C_L + C_{in,T} C_L}{g_{m,CVC} C_f}, \tag{5-3}$$

where:

$$C_{in,T} = C_{ref} + C_x + C_p. \tag{5-4}$$

Figure 5-4(a) shows the circuit diagram of the applied CVC amplifier. Figure 5-4(b) shows the simulation results of its low-frequency gain versus the output DC voltage.

The transconductance $g_{m,CVC}$ of this amplifier is about 1 mA/V. The tail current of the input stage equals 200 µA. Because of the applied 1:1 current mirrors, the maximum available output current $I_{o,max}$ is 200 µA.

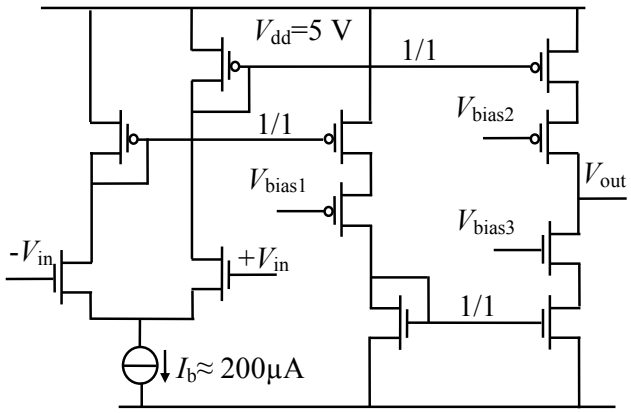
Figure 5-5 depicts the calculated charge-transfer time constant τ_{CT} for different input-capacitance ranges C_{ref} versus the parasitic capacitance C_p, for $C_x = C_{ref}/2$, $C_f = 4.7C_{ref}$, and $C_L = 10$ pF.

As mentioned in chapter 4, section 4-4, a settling accuracy of m bits requires that:

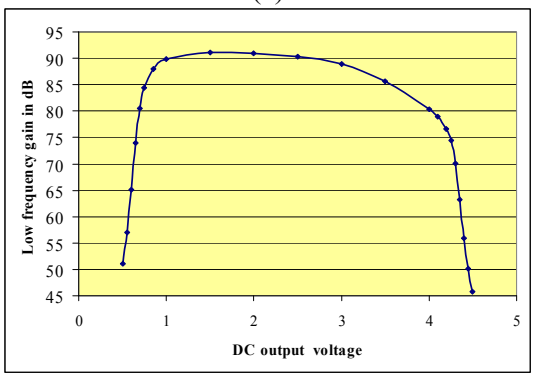
$$T_1 \geq (m+1)\tau_{CT} \ln 2, \tag{5-5}$$

where T_1 is the shortest time interval in the signal V_{int} (Fig. 5-2). To be more precise, because $T_2 \geq T_1$, satisfying condition 5-5 will yield a settling accuracy of > m bits. From equation 5-5 it can be found that for a 14-bit settling accuracy, it is necessary that:

$$T_1 \geq 10\tau_{CT}. \tag{5-6}$$



(a)



(b)

Fig. 5-4: (a) The circuit diagram of the amplifier used for capacitance-to-voltage converter (CVC); (b) simulation of the low-frequency gain versus the output DC voltage.

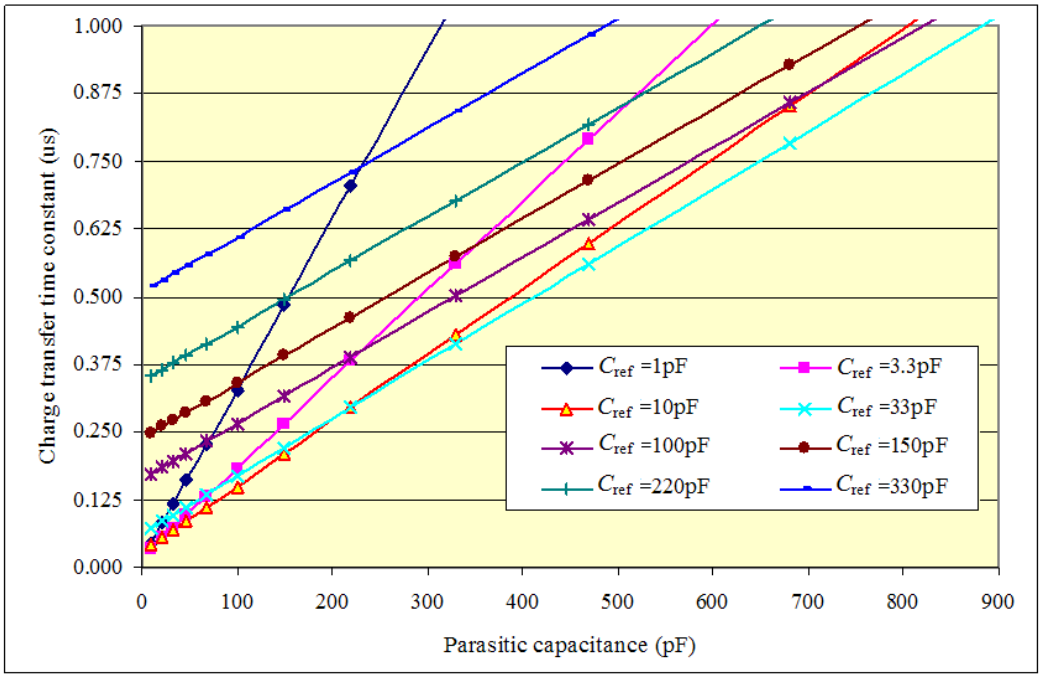


Fig. 5-5: The charge transfer time constant τ_{CT} versus C_p for different reference capacitors which correspond to different ranges.

In the design presented in this chapter, T_1 amounts to 10 µs, 5 µs, 2.5 µs or 1.25 µs, for I_{int} = 0.5 µA, 1 µA, 2 µA and 4 µA, respectively. Therefore, for the four values of the integrator current and the corresponding four different values of T_1, the charge transfer time constant τ_{CT} should be smaller than 1 µs, 0.5 µs, 0.25 µs and 0.125 µs, respectively.

Example 5-1: Suppose that we want to find the maximum parasitic capacitance C_p for a settling accuracy higher than 14 bits for, for instance, the 1 pF and the 10 pF range, respectively ($C_x \leq C_{ref}$ = 1 pF and $C_x \leq C_{ref}$ = 10 pF, respectively). From figure 5-5 it can be found that for C_{ref} = 1 pF, the maximum allowable parasitic capacitances are about 300 pF, 150 pF, 68 pF, and 33 pF, respectively. For C_{ref} = 10 pF, these values amount to 800 pF, 350 pF, 180 pF, and 68 pF. For instance if we want to measure a capacitance up to 1 pF (the 1 pF range) with a parasitic capacitance of up to 50 pF, then the 4 µA option is not suitable. However, among the other three, the best value of the integrator current is 2 µA, because then the measurement can be performed faster, or yield a higher resolution (see section 5-4).

Example 5-2: Let us suppose that $C_x \leq C_{ref}$ = 100 pF, and C_p = 300 pF, and that we want to know which current or currents can guarantee a settling accuracy > 14 bits. From figure 5-5 it can be found that for these conditions the charge-transfer time constant is about 0.45 µs. Therefore, integrator currents of 0.5 µA and 1 µA are suitable. However, 1 µA is the best option.

These two examples show how the user can select the integrator current for optimum performance. However, there is an easier and more general way to find the optimum current. We know that by increasing available time by a factor of two, the settling error is reduced by the power of two. For instance, when the settling error for I_{int} = 2µA is 10^{-3} (corresponding to 10-bit accuracy), then the settling error for I_{int} = 1µA is 10^{-6} (corresponding to 20-bit accuracy). Therefore, the difference in the measured results for two different currents is due to the error of the higher current. If this error is below the error budget, then both currents are suitable. However, if this error is higher than the error budget, then the higher current is not suitable. To see whether or not the lower current is suitable we should look at the square of the difference.

5-3-2 Error due to slewing

Figure 5-6 shows the CVC with related signals. The easiest way to analyze the frequency limitations posed by slewing is to consider that regardless of whether or not the reset switch S_r is ON, the charged pumped by input capacitor C_i into C_f, will require sufficient current provided by the amplifier output to remove this charge in the available time. Otherwise, settling of the amplifier will not be completed, which will cause nonlinearity of the amplifier behaviours and a non-zero amplifier input voltage. By looking at the drive voltage (Fig. 5-6(b)) and the control signal of reset switch, it can be observed that charge pumping will occur at the beginning of phases ph_1 and ph_2. Therefore, the minimum time for T_1 can be calculated as:

$$T_1 > \frac{V_{DD} C_{i,max}}{I_{o,max}}, \tag{5-7}$$

where $C_{i,max}$ is the maximum input capacitance and $I_{o,max}$ is the maximum available current at the output of the CVC amplifier. When the slewing ends, the circuit enters its linear region and therefore it needs more time to settle with certain accuracy. As a result, the limit determined by equation 5-7 is a very rough indication of required time.

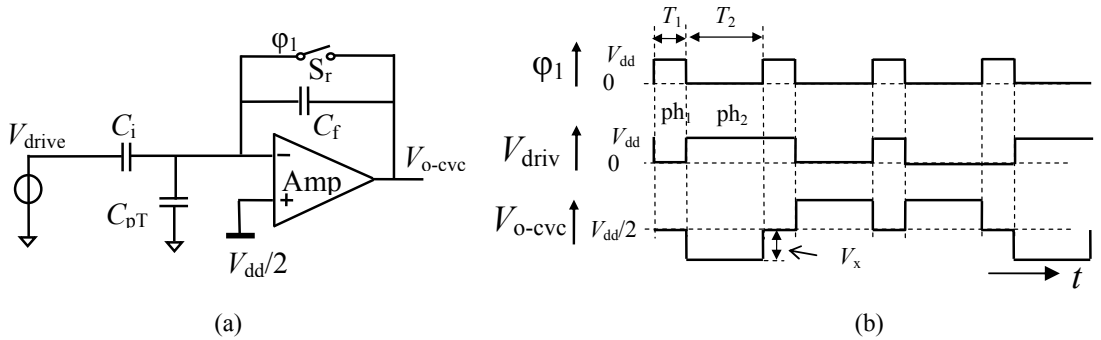


Fig. 5-6: (a) The CVC for a high-quality floating capacitor and (b) the related signals.

As mentioned in section 5-3-1, the maximum available output current $I_{o,max}$ for the applied CVC amplifier is 200 µA. Therefore, for four different values of T_1, 10 µs, 5 µs, 2.5 µs and 1.25 µs, according to equation 5-7, the maximum capacitance $C_{i,max}$ should be smaller than 400 pF, 200 pF, 100 pF, and 50 pF, respectively. Therefore, the maximum capacitance that can be measured amounts to about 400 pF.

5-3-3 Charge-loss error

From figure 5-6, by ignoring the output resistance of the drive-voltage source and considering that the voltage jump of the drive voltage equals V_{DD}, it can be found that the voltage jump V_{jump} at the input of the amplifier amounts to:

$$V_{jump} = \frac{V_{DD} C_i}{C_i + C_{p,T}}. \tag{5-8}$$

From this equation it is clear that for $C_i > C_{p,T}$ the jump at the input of the amplifier can be larger than $V_{DD}/2$. Then with a biasing voltage of $V_{DD}/2$ at the non-inverting input, the instant voltage at the inverting input can exceed the supply voltage in both directions. This will cause forward biasing of a source-to-substrate junction of the reset switch or of the protection diodes in the bonding pads, which will cause charge loss. To prevent this, the condition should be met that:

$$C_{p,T} \geq C_i. \tag{5-9}$$

Some precautions are required to guarantee that this condition is met. For instance, let us suppose that the sensor capacitance can be any value in the range from 1 pF to 100 pF, and that therefore a reference capacitor C_{ref} = 100 pF has been selected. Furthermore, let us suppose that the parasitic capacitance is only 10 pF. Then, when measuring the reference capacitor for a sensor capacitance of, for instance, 2 pF, the total parasitic capacitance $C_{p,T}$ is only 12 pF; therefore condition (5-9) is not met. To improve the circuit, an extra parasitic capacitance $C_{p,\,extra} > C_{ref}$ should be added to the measurement setup.

5-4 Noise performance

With respect to noise, the two main differences between this design and all other designs presented in this thesis concern the design of the integrator-current source and the comparator in the relaxation oscillator. As mentioned in chapter 4, section 4-5, since any delay caused by the comparator is removed by three-signal auto-calibration, the comparator does not need to

be fast. Therefore, we designed a comparator with a limited bandwidth. Moreover, based on our analysis in chapter 4, section 4-6-2, the only low-frequency filtering of the current-source noise is that performed by the three-signal auto-calibration, which suppresses the noise below $1/T_{3\text{-sig}}$. Therefore, in order to have sufficient suppression of flicker noise of the current source, it is necessary that:

$$f_c \leq \frac{1}{T_{3\text{-sig}}}, \tag{5-10}$$

where f_c is the flicker-noise corner frequency of the integrator-current source. In this design, this condition is valid for all different value of $T_{3\text{-sig}}$ (Table 5-1) and therefore the current source flicker-noise is removed by auto-calibration.

Based on the noise analysis presented in chapter 4, section 4-6, we wrote a program in Matlab the input parameters for which are: the sensor parameters, the interface settings I_{int} and N, and the noise spectral densities of the various interface parts. With these parameters, the program calculates the three different periods and their jitter. The final output is the total noise in the simulated value of the measured capacitance C_x. The main sources of jitter are: 1) noise of the integrator current, 2) integrator sampled-noise at the end of phase 2, 3) CVC sampled-noise at the end of phase 1, and 4) continuous noise at the input of the comparator. The first two do not depend on sensor conditions; however, the other two do depend on the sensor conditions. For example, the input-referred noise in the 1 pF range for a capacitance with a value of 0.47 pF was calculated for four different values of the integrator current. For a large parasitic capacitor C_p >20 pF, the sampled noise, which is independent from the integrator current, is dominant. Therefore, for a fixed amount of samples N the total noise for the three currents is almost the same. However, for a proper comparison, we should not fix the amount of samples, but keep the measurement times constant. To do so, we adapted the amount P of measurements so that for all cases the total measurement time $T_{3\text{-sig}}$ = 1 s. Figure 5-7 shows the standard deviation of the simulated capacitance measurement versus the parasitic capacitance for four values of the integrator current. In this simulation, for each current value the parasitic capacitance is pushed up to a maximum value at which the settling accuracy is still higher than 14 bits (see example 5-1). For C_p >20 pF, as expected, increasing the current by the factor of 4 yields a decrease in the noise by about a factor of two. However, for very small parasitic capacitances (C_p < 10 pF) this is no longer the case, the reason being that for small parasitic capacitances the quantization noise plays an important role and is constant. In this simulation, quantization noise amounts to 6 ns, which value is true for a clock frequency of 70 MHz (chapter 4, section 4-6-3).

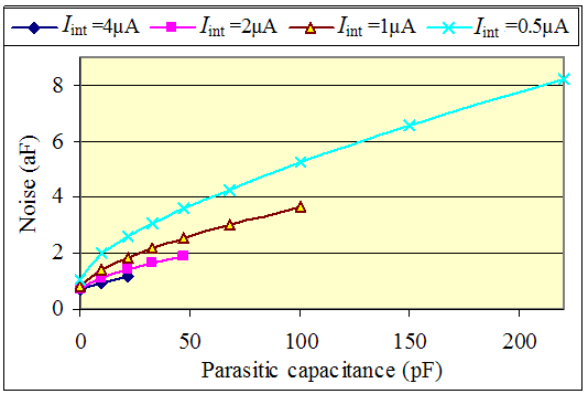


Fig. 5-7: The simulated input-referred noise (standard deviation) for the 1 pF range, measurement time $T_{3\text{-sig}}$=1s, and different values of the integrator current I_{int} versus the parasitic capacitance C_p.

5-5 Implementation and measurement results

5-5-1 Implementation

The interface with optimized noise performance was designed and fabricated in standard 0.7µm CMOS technology. Figure 5-8 shows a photograph of the chip, which measures 1.8 mm× 1.3mm. The supply voltage is 5 V and the measured value for the supply current is about 1 mA.

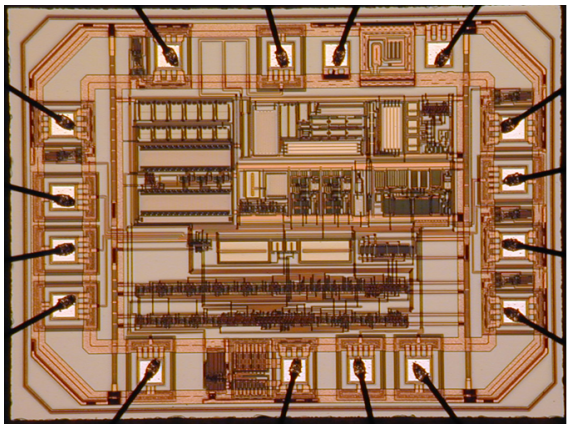


Fig. 5-8: Photograph of the chip, which measures 1.8 mm × 1.3 mm.

The period lengths of the output signals (Fig. 5-1(b)) were measured with a micro-controller. This microcontroller has an internal counter with a sampling frequency of 70 MHz and can measure each period T_{off}, $T_{ref,}$ and T_x by detecting the corresponding rising transients in the interface output signal.

The value of N, which is set by the external control signals SF0 and SF1 (table 5-1), doesn't have a significant effect on the systematic error. Therefore, most of our reported measurement results are performed for $N = 32$. This selection also guarantees that the effect of quantization noise can be ignored. However, to show the speed of our interface, and also the required clock frequency, we also performed measurements at the highest speed. As will be shown, and according to the expectations, increasing the measurement time $T_{3\text{-sig}}$ by a factor of 2 increases the (white) noise by a factor of √2.

5-5-2 Settling error

In the first measurement we tested the effect of the integrator current on the systematic error and the required sensor conditions. Figure 5-9 shows the measured systematic error in the 1pF range for a capacitance of about half the reference capacitor versus the parasitic capacitance for a different integrator current (unfortunately, due to a simple design error, the interface does not work for the 4 µA mode). The selected capacitors are of the type NP0 SMD, and have nominal values of: C_{ref} = 1pF, C_x = 0.47pF, and C_f = 4.7pF. It should be mentioned that due to auto-calibration, independent from settling accuracy, the error from measuring $C_x = C_{ref}$ is zero, which is the reason for measuring the settling error for $C_x = C_{ref}/2$. For our measurement results, the measured values for C_p = 10pF are taken as a reference.

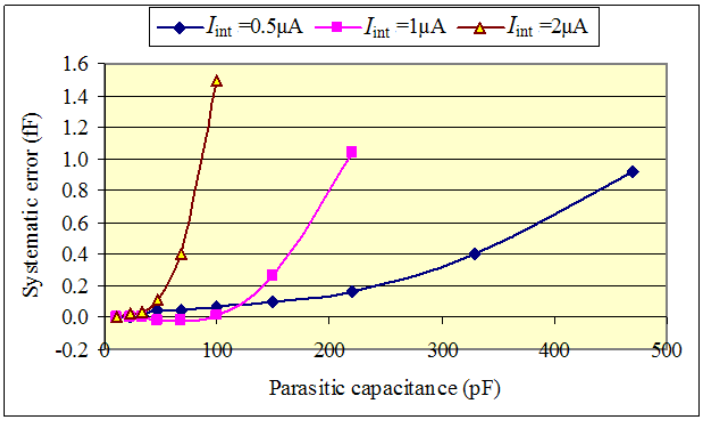
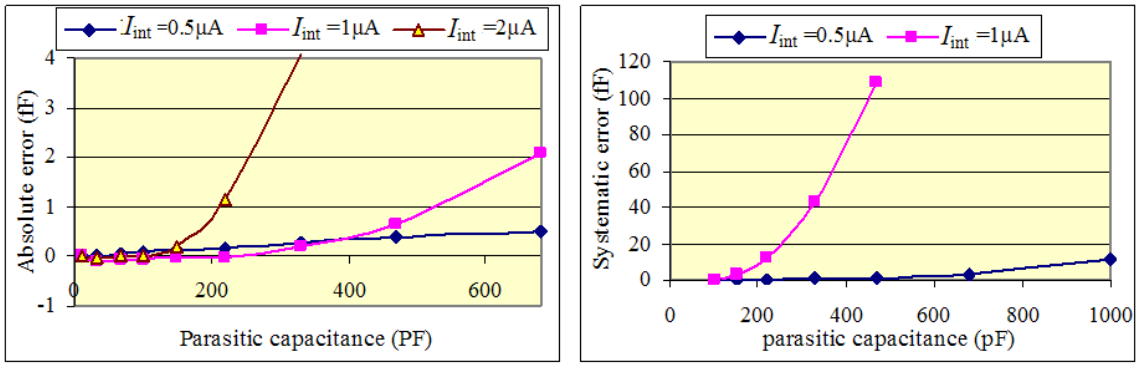


Fig. 5-9: The systematic error versus the parasitic capacitance C_p for $C_x = C_{ref}/2$ for the 1pF range (C_{ref} = 1 pF).

The settling accuracy, which for the 1 pF range is higher than 14 bits, corresponds to a settling error of less than 0.06 fF. Therefore, if we suppose that the error in figure 5-9 is due to unfinished settling, then the maximum affordable parasitic capacitances for three different currents 2 µA, 1µA and 0.5 µA are about 40 pF, 120 pF and 120 pF, respectively. The first two values are close to the theoretical ones from example 5-2,(68 pF and 150 pF), but the third one is far from the theoretical value (300 pF). As we will show in section 5-5-7, increasing the parasitic capacitance will increase the nonlinearity error as well. Therefore, the error in figure 5-9 includes both the nonlinearity error and the settling error. However, distinguishing settling error from nonlinearity error in our system is not difficult. As is mentioned in section 5-3-1, increasing the available time by a factor of two, decreases the settling error by a power of two. Therefore, in the region that the systematic error heavily (much more than inverse-proportionally) depends on the integrator current, settling is most likely the main error source. For instance, for the 1 pF range and I_{int} =1 µA with C_p= 220 pF, the settling error is 1 fF (Fig. 5-9), which corresponds to 10 bits. For the same parasitic capacitance and I_{int} = 0.5 µA, the settling error should be about 20 bits, which corresponds to 1 aF. However, according to figure 5-9, the systematic error is about 160 aF, which should be due to nonlinearity.

The same measurements were performed for the 10 pF and 100 pF ranges (Fig. 5-10). To satisfy the condition 5-9, for each range, the measurement results for a parasitic capacitance $C_p = C_{ref}$ were taken as reference. We can use the results in the following way: Let us suppose that we want to have a settling accuracy of 14 bits. In the 10 pF range this corresponds to 0.6 fF. Then, from figure 5-10(a) it is found that for a settling accuracy of 14 bits, the maximum allowable parasitic capacitances are about 170 pF, 450 pF, and more than 680 pF for the three integrator currents, respectively. These values are quite close to the expected values from example 5-1.



(a) (b)

Fig. 5-10: Systematic error versus parasitic capacitance C_p for $C_x = C_{ref}/2$ for the ranges (a) 10pF and (b) 100 pF.

In the 100 pF range with I_{int} =2 µA (not shown in Fig. 5-10(b)), for $C_x \approx 50$ pF the settling error is about 1 pF (1% of full scale span). In most applications, this type of error is not acceptable. Therefore, in figure 5-10(b) only the measurement results for I_{int} =1 µA and I_{int} =0.5 µA are given.

5-5-3 Slewing error

In this section we focus on the limitations posed by slewing. From figure 5-5 it can be observed that for instance for the 220 pF range with a parasitic capacitance of 220 pF, the charge-transfer time constant is about 0.57 µs. In this case, without the slewing problem, the settling error for T_1 = 5 µs should be about 34 fF. However, the measured error for this condition (Fig. 5-11) is much higher than the settling error. For this measurement, a precision impedance analyzer, Agilent 4294A, was used as a reference, and we calibrated our system for PCB parasitic according to chapter 4 section 4-7.

If we look at our analysis in section 5-3-2, the maximum input capacitance for T_1 = 5 should be lower than 200 pF. Therefore, this error is due to slewing. As we will see in section 5-5-5, this error can be reduced significantly by decreasing the integrator current to 0.5 µA, in order to make T_1 = 10 µs.

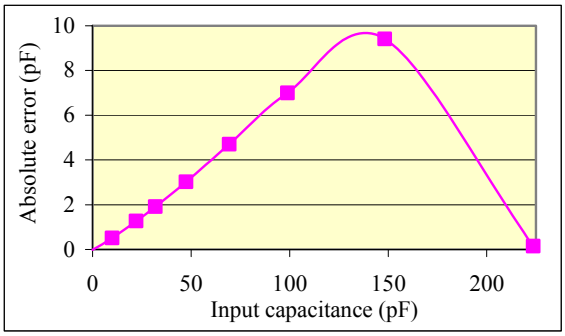


Fig. 5-11: The measured systematic error versus input capacitance in the 220 pF range $C_{x,max} = C_{ref} = C_p = 220$ pF for T_1 = 5 µs.

5-5-4 Charge-loss error

A next series of measurements concern the effect of charge loss at the negative input of the CVC amplifier. As mentioned in section 5-3-3, when the input capacitance is larger than the total parasitic capacitance at the CVC input ($C_i > C_{p,T}$), the voltage jump at the CVC input can exceed the supply voltage and cause charge loss to the substrate. Figure 5-12 shows the absolute measured error in the 100 pF range for C_p = 100 pF and C_p = 0 pF. As can be observed for C_p = 0 pF and for C_i < 33pF, there is a significant error. However, when C_p = 100 pF this error is not visible.

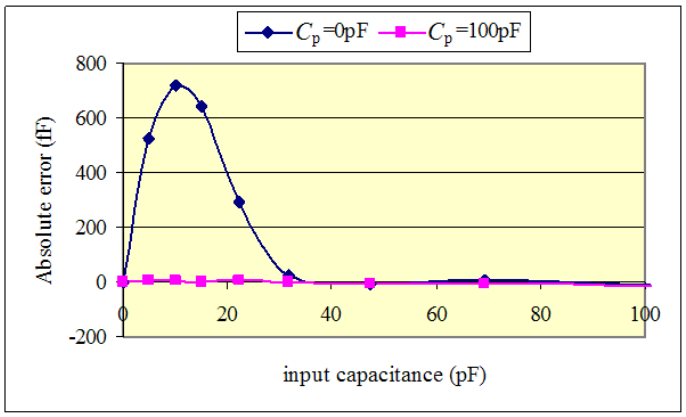


Fig. 5-12: The measured systematic error versus the input capacitance C_i for C_p = 100 pF and C_p = 0 pF, respectively. The integrator current amounts to 0.5µA (T_1 = 10µs).

5-5-5 Maximum capacitance range

Based on our analysis in section 5-3-2, we expect that the maximum capacitance range is smaller than 400 pF. To determine the maximum capacitance range we measured the absolute accuracy while using a precision impedance analyzer, Agilent 4294A, as a reference for different ranges. Figure 5-13 shows the results for the measurement ranges of 33pF, 100 pF, 150 pF, 220 pF, and 330 pF.

For the 33 pF range, an absolute accuracy of about 14 bits is achieved (Fig. 5-13(a)). It should be mentioned that there is at least 1 fF error contributed by the setup. Therefore, the real accuracy of the chip can be even greater than 14 bits. For the higher ranges (up to 220 pF), an absolute accuracy of about 13 bit is measured. However, for the 330 pF range, an error of about 2 pF was measured, which corresponds to an accuracy of less than 8 bits. The reason for such a large error is due to slewing.

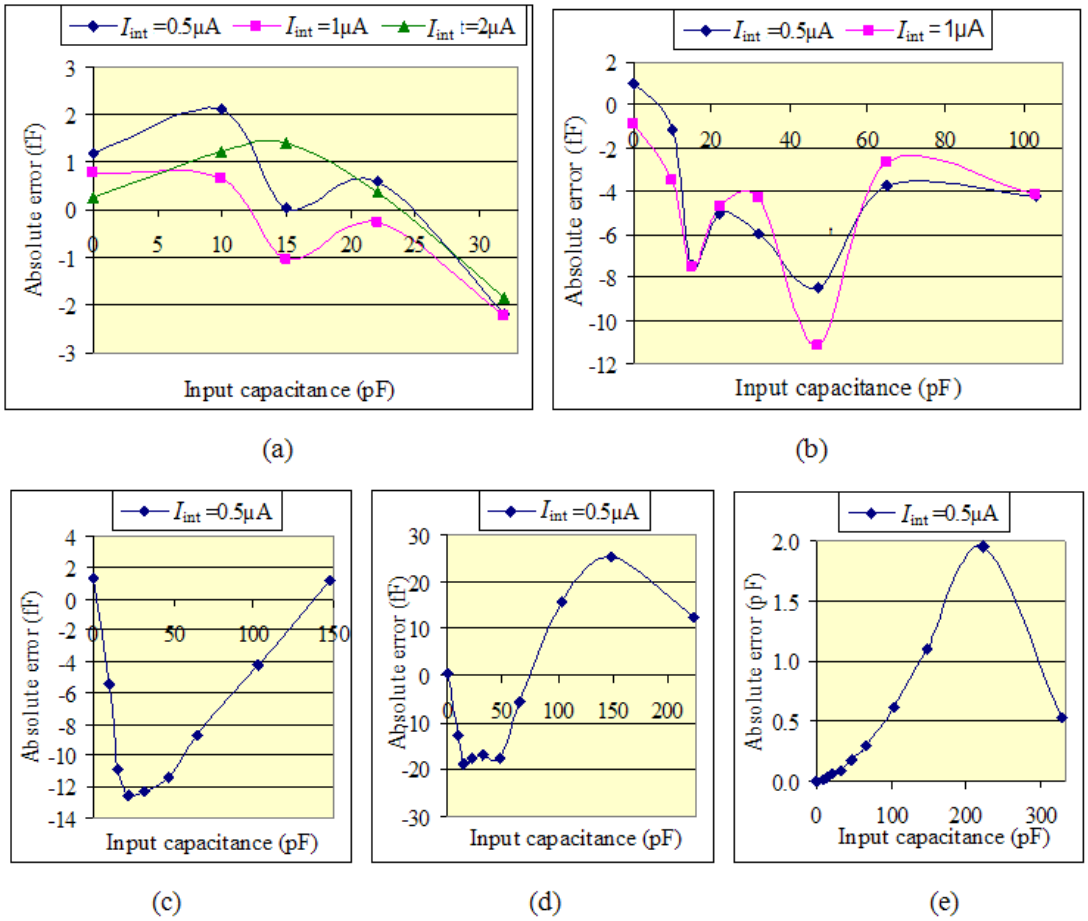


Fig. 5-13: The absolute error versus the input capacitance C_x for (a) the 33 pF range, (b) the 100 pF range, (c) the 150 pF range, (d) the 220 pF range, and (e) the 330 pF range.

5-5-6 Noise error

For the noise performance of the interface, we found that the resolution in bits remains almost constant for the capacitance ranges ≥ 1 pF. According to our experimental results, decreasing the capacitance range to less than 1 pF will not decrease the noise as expressed in F[1]. Consequently, the resolution in bits will decrease (for a definition of "resolution in bits", see Appendix A, Eq. A-1). Figure 5-14 shows the measured and simulated resolution in bits for the 1 pF range and a measurement time of 1 s. For a clock frequency of 70 MHz, both measurement and simulation (see chapter 4, section 4-6-3) show that the quantization noise amounts to 6ns. For all noise experiments, simulations, and the feedback capacitor, it holds that $C_f = 3.3$ $C_{x,max} = 3.3$ pF.

[1] When decreasing the input capacitance range $C_{x,max}$, the input parasitic capacitance $C_{p,T}$ and feedback capacitor C_f, have to be decreased by the same ratio (Fig. 5-5-a). Therefore, the noise gain of the CVC amplifier is almost independent from the input capacitance range. However, for very small input capacitances, the parasitic pin capacitance at the chip and PCB level, which is constant, can dominate the total parasitic capacitance of this node. In that case, when decreasing the input capacitance range and therefore the feedback capacitor, the CVC noise gain will increase.

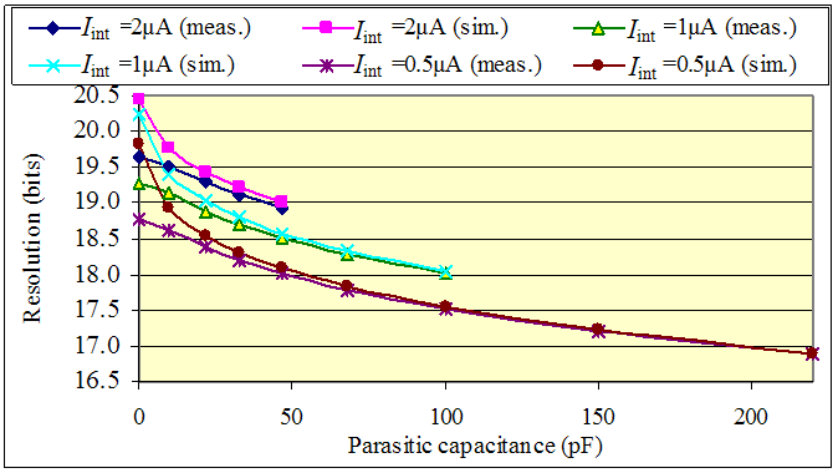


Fig. 5-14: The measured and simulated resolution for the 1 pF range, a measurement time of 1s, and three values of the integrator current.

Note that for C_p > 10 pF, the measured and simulated resolution correspond well with each other. However, for smaller parasitic capacitances the difference is significant. It should be mentioned that in figure 5-14, a parasitic capacitance of 0 pF means that there is no external capacitor as a parasitic capacitance; therefore, $C_{p,ext.}$ = 0 pF. However, due to the effects of the bonding pads and PCB parasitic capacitance C_{p0}, the starting point of the measurement is equivalent to the point of C_p= C_{p0}. From this explanation, part of the difference between the simulation and measurement in figure 5-14 can be explained. Since in real applications, the connection cable always introduces a significant parasitic capacitance, for the region C_p < 10 pF, we did not investigate the details of these differences.

Similar measurements were performed for the 10 pF range. Figure 5-15 shows both the measurements and the simulation results.

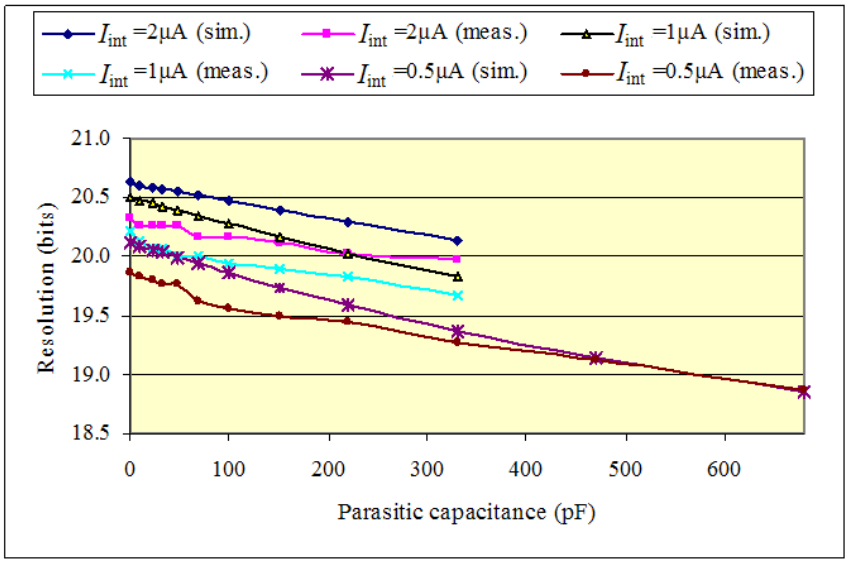


Fig. 5-15: The measured and simulated resolutions for the 10 pF range with a measurement time of 1s, and for three values of the integrator current.

5-5-7 Maximum measurement speed and required sampling frequency

As already mentioned in section 5-5-2, due to a simple design error, the interface does not work for the 4 µA mode. Therefore, the fastest mode is I_{int} = 2 µA and N = 2 (Table 5-1). Table 5-2 shows the resolution for the 10 pF range with I_{int} = 2 µA for different values of N.

Table 5-2: The measurements for time and noise (standard deviation) for I_{int} = 2 µA, C_x = 5 pF, C_{ref} = C_p = 10 pF, and C_f = 33 pF.

N	2	8	32	128
Measurement time(ms)	0.23	0.95	3.79	15.16
Standard deviation of the measured noise (aF)	1400	400	160	85

For thermal noise, a decrease of N by a factor of 4 decreases the measurement time by the same factor, while the standard deviation of the measured values should increase by a factor of 2. For the measurement results shown in table 5-2, the above mentioned explanation is almost valid for the last two columns. However, for the first two columns there is extra noise, which can be attributed to the effect of quantization noise. Figure 5-16 shows the measured result for a capacitance with a nominal value of 5 pF C_x = 5 pF in the 10 pF range, where C_{ref} = C_p = 10 pF and C_f = 33pF. The sampling frequency which is used for digitizing the output periods was 70 MHz. In this figure, the effect of quantization noise can clearly be observed.

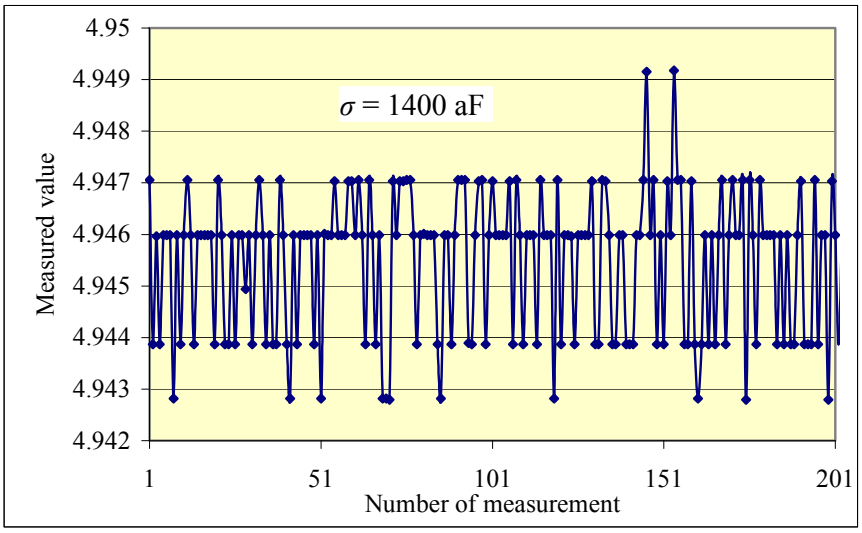


Fig. 5-16: The measured results for a capacitance with nominal value of 5 pF with the measurement time of 230 µs and a sampling frequency of 70 MHz.

In order to find the required sampling frequency, we performed the following tests: Initially, we took a low-cost microcontroller, type LPC2103, which has a timer with a 70 MHz sampling frequency. The measured jitter (standard deviation) of T_x for different N, I_{int} = 2 µA, C_{ref} = C_p = 10 pF, C_x = 5 pF and C_f = 33pF, is shown in the second row of Table 5-3. Part of this jitter $j_{q.n}$ is caused by quantization noise, which according to equation 4-103 is independent from N and amounts to 6 ns. We can simply calculate the jitter excluding quantization noise $j_{excl\text{-}q.n}$, as:

$$j_{\text{excl-q-n}} = \sqrt{j^2_{\text{incl-q-n}} - j^2_{\text{q-n}}} \ . \qquad (5\text{-}11)$$

Substituting the measured jitter and the value of $j_{\text{q.n}} = 6$ ns in this equation yields the values of the jitter on T_x, excluding quantization noise shown in the third row of Table 5-3. As we can see, the related result for $N = 2$ cannot be calculated with equation 5-11. However, for the jitter we can make an estimation in the following way: Assuming that the jitter excluding q.n. is due to thermal noise, this value can be calculated from the fact that the jitter $j_{\text{excl-q.n}}$ will decrease with $\sqrt{N}$, after which we can make an estimation from the value found by for instance $N = 32$ and divide that value by $\sqrt{N}$, which yields 12.7ns/4=3.2ns.

Table 5-3: Measured jitter on T_x for $I_{\text{int}} = 2$ µ, $C_x = 5$ pF, $C_{\text{ref}} = C_p = 10$ pF, and $C_f = 33$ pF.

N ($T_{\text{out}}=N\,T_{\text{msm}}$)	2	8	32	128
Measurement jitter on T_x (ns)	6	9	14	25
Measured jitter on T_x excluding quantization noise (ns)	(3.2) see text	6.7	12.7	24.3

The related values for the other two periods, T_{off} and T_{ref}, were found to be very close to the values presented in table 5-3.

For a further evaluation of the assumptions, we repeated the measurement for $N = 2$ with a more expensive setup using a sampling frequency of 200 MHz. In this case, the quantization noise should be about 2.1 ns. Figure 5-17 shows the measured T_x for the same condition as table 5-3 for $N = 2$ and for the 201 measurement. In this experiment, the measured jitter (standard deviation) amounts to 3.9 ns. When substituting this value in equation 5-11 with $j_{\text{q.n}} = 2.1$ ns, we find jitter $j_{\text{excl-q.n}} = 3.3$ ns, which is very close to the expected value from table 5-3.

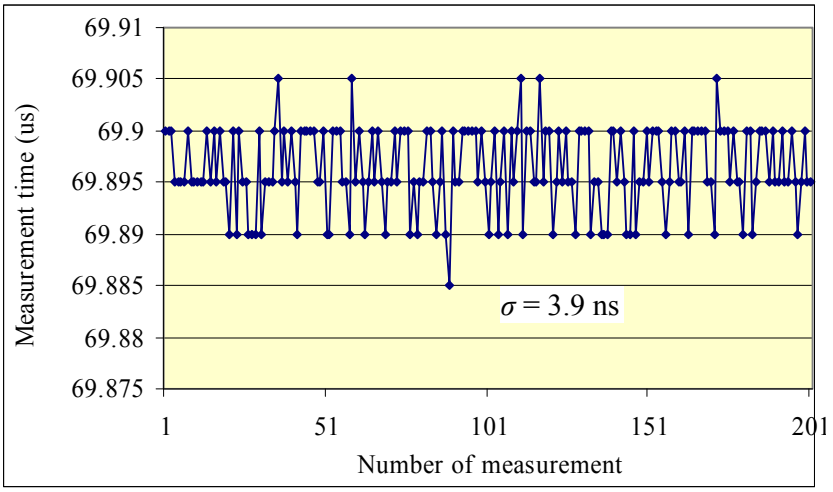


Fig. 5-17: The measured results of T_x for $N = 2$, $I_{\text{int}} = 2$ µA, $C_{\text{ref}} = C_p = 10$ pF, $C_x = 5$ pF, and $C_f = 33$pF with a sampling frequency of 200 MHz.

The same setup with a 200 MHz sampling frequency was used to repeat the measurements referred to in table 5-2, which yielded the results shown table 5-4.

Table 5-4: The measured noise (standard deviation) for I_{int} = 2 µA, C_x = 5 pF, C_{ref} = C_p = 10 pF and C_f = 33 pF with the sampling frequency of 200 MHz.

N	2	8	32	128
Measured noise (aF)	880	380	170	90

Figure 5-18 shows the measured value for C_x in this condition. Unlike figure 5-16, the effect of quantization noise is not significant.

The standard deviation of 880 aF in the 10 pF range corresponds to a resolution of more than 13 bits for a measurement time of only 0.23 ms.

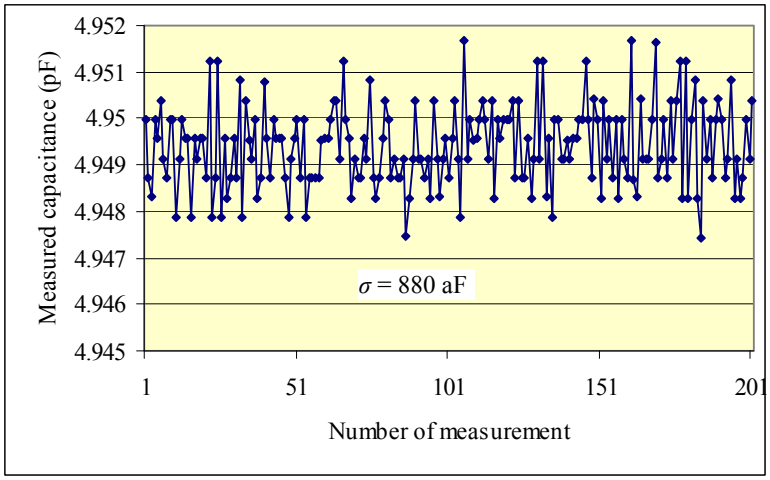


Fig. 5-18: The measured results for a capacitance with a nominal value of 5 pF with a measurement time of 230 µs while using a sampling frequency of 200 MHz.

5-5-8 Nonlinearity

When measuring small nonlinearities, we cannot rely on absolute accuracy. However, by selecting the four C_x-capacitors as C_1= C_{x1}, C_2= C_{x2}, C_3= C_{x1}+ C_{x3} and C_4= C_{x2}+ C_{x3}, and with the help of an external multiplexer (Fig. 5-19), independent from the absolute accuracy of these four capacitors and with high immunity for the related parasitic capacitances, the (modified) nonlinearity parameter λ_{mod} can be defined as (chapter 4, section 4-9):

$$\lambda_{mod} = 1 - \frac{M_{Cx2+Cx3} - M_{Cx1+Cx3}}{M_{Cx2} - M_{Cx1}}. \qquad (5\text{-}12)$$

The value of λ_{mod} depends on the selected capacitors. Figure 5-20 shows the measured nonlinearity λ_{mod} versus the parasitic capacitance C_p, for C_{off} ≈ 0pF, C_{ref} ≈ 10pF, C_1= C_{x1} ≈ 0pF, C_2= C_{x2} ≈ 5pF, C_3= C_{x1}+ C_{x3} ≈ 5pF, and C_4= C_{x2}+ C_{x3} ≈ 10pF. Comparing the nonlinearities measured for C_f = 33 pF and C_f = 47 pF, respectively, shows that a much stronger nonlinearity is found with the smaller capacitance. For C_f = 33 pF, when selecting C_{ref} or C_4, the output of the CVC amplifier changes from 1V to 4V. Then the CVC amplifier almost reaches its saturation region (Fig. 5-4(b)). This supports the conclusion of chapter 4, section 4-8 that the main nonlinearity is caused by the nonlinear open-loop gain of the CVC amplifier.

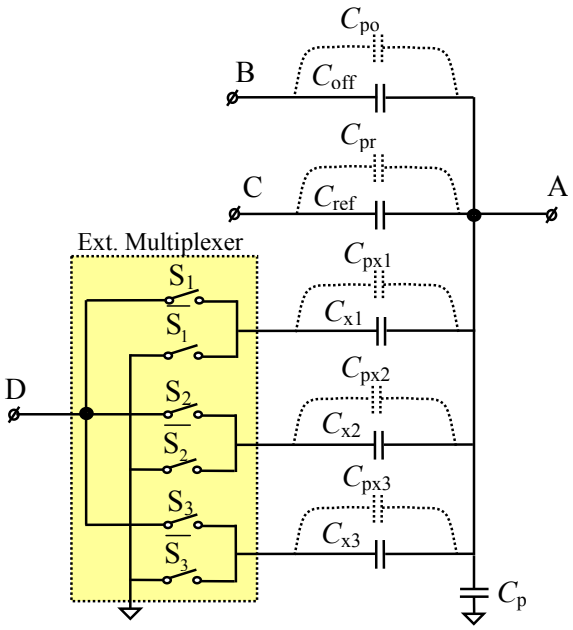


Fig. 5-19: The capacitors with related parasitic for non-linearity measurements presented in this work.

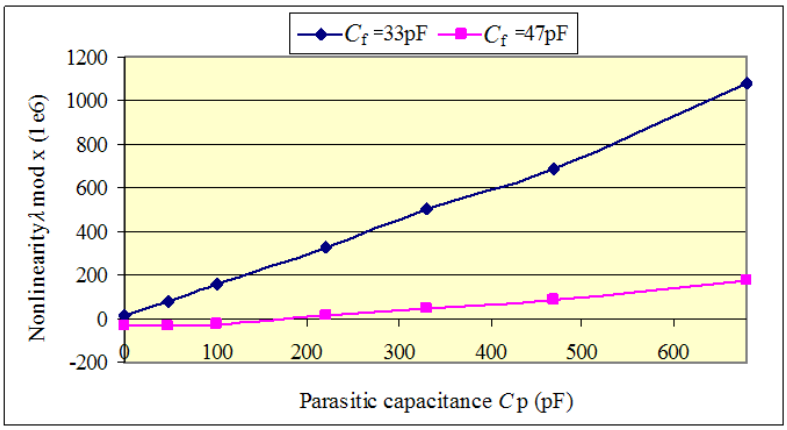


Fig. 5-20: The measured non-linearity defined by Eq. 5-11 versus the parasitic capacitance in the 10 pF range for two different feedback capacitors.

Based on our analysis in chapter 4 section 4-9, the measured maximum nonlinearity error ε_m versus the parasitic capacitance for two different feedback capacitor in the 10 pF range is calculated, which results in equation 5-12.

$$\varepsilon = \frac{\lambda_{\mathrm{mod}(0,0.5,0.5,1)}}{4}. \qquad (5\text{-}12)$$

With this equation the results of figure 5-20 have been converted to those of figure 5-21.

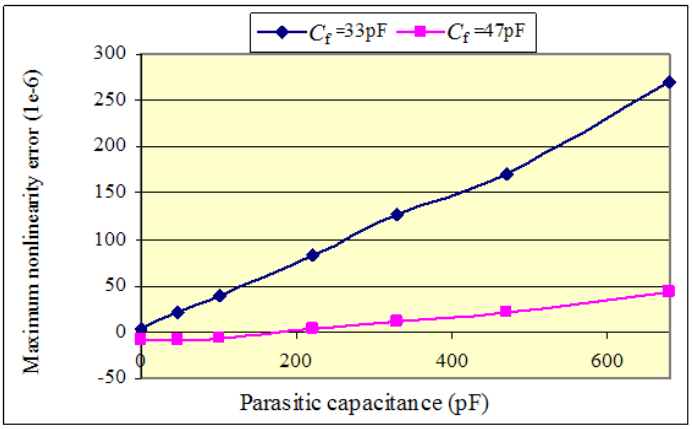


Fig. 5-21: The measured maximum non-linearity error versus parasitic capacitance in the 10 pF range for two different feedback capacitors.

Note that there is a nonlinearity error $\varepsilon_m << 5 \times 10^{-5}$ for a parasitic capacitance as large as 680 pF. However, a nonlinearity error of less than 2.5×10^{-5} can be achieved when the parasitic capacitance is limited to 470 pF, which corresponds to more than 15 bits.

5-6 Users' guide

One of the main characteristics of the designed interface concerns flexibility. This flexibility allows the user to achieve the best performance for a particular application. To assist the user, we briefly summarize the main choices that should be made and the order in which they should be carried out.

First the following question should be answered:

1. Is the maximum range of sensor capacitance value below 220 pF?
2. Are both the required data acquisition rate and the sensor bandwidth below 4 kHz?
3. Is the required resolution below 20 bits/Hz?
4. Is the required linearity less than 15 bits?

When one or more answers to these questions is "No", then this interface is not suitable for that application. Even when all answers are "Yes", we still cannot be sure that this interface is suitable for that application. For instance, suppose the capacitance range is 220 pF and that the required data acquisition rate is 2 kHz: due to the settling error, the only suitable integrator current is 0.5 µA (see sections 5-5-4 and 5-5-5). Consequently, the maximum data acquisition only reaches about 1kHz (table 5-1).

For sensors with a small capacitance value, the parasitic capacitance plays an important role (Fig. 5-5). For instance, for a sensor with capacitance values up to 33 pF, the number of options of the integrator current that can be used (sections 5-3-1 and 5-3-2) depends on the value of parasitic capacitance (Fig. 5-5). For example, for the 10 pF range with a parasitic capacitance of up to 180 pF, all three working integrator current can be selected. However, for this range, for the case that C_p = 500 pF, only for I_{int} = 0.5 µA can a settling accuracy of 14 bits be guaranteed.

When the user concludes that the presented interface can be used for a specific application, the best settings should be found. These settings include:

1. Selection of the offset and reference capacitors C_{off} and C_{ref}.
2. Selection of the feedback capacitor C_f.
3. Selection of the measurement speed.
4. Selection of the most suitable value for the integrator current I_{int} out of 4 available options.

For a good resolution, the values of the capacitors C_{off} and C_{ref} should be not too far from the minimum and maximum values of the sensor capacitances. For convenience, the offset capacitor is often omitted (C_{off} = 0pF). The feedback capacitor C_f should be at least 3.3 times the maximum input capacitance, which can be $C_{x,max}$ or C_{ref}. Therefore it should hold that $C_f > 3.3\times$ max (C_{ref}, $C_{x,max}$). With a larger feedback capacitor of up to 5 ×max (C_{ref}, $C_{x,max}$), a higher linearity can be obtained (Fig. 5-21).

The selection of the measurement speed is quite straightforward. Of course, the measurement speed should be selected to be equal or faster than the required data acquisition rate. However, if the sensor requirement does allow it, it is advisable to set the measurement speed to a minimum, since in that case we can digitize the output period with a lower sampling frequency.

The integrator current I_{int} needs to be selected based on: a) the capacitance range of the sensor, b) the parasitic capacitance value, and c) either the required settling accuracy or the maximum-acceptable systematic error. For instance for the 1 pF range together with a parasitic capacitance of 100 pF, the charge-transfer time constant amounts to about 0.35 µs. Therefore, for settling accuracy >14 bits, the time period T_1 (Fig. 5-2) should be larger than 3.5 µs. This means that only the options I_{int} = 0.5 µA and I_{int} = 1 µA, which correspond to T_1 = 10 µs and T_1 = 5 µs, can be used.

Finally, in the case that the sensor and/or cable parasitic capacitances are smaller than the maximum input capacitance $C_{x,max}$ or C_{ref}, a parasitic capacitance should be added to satisfy equation 5-9.

5-7 Conclusions

A flexible high-resolution-integrated interface for capacitive sensors has been designed and implemented in standard 0.7µm CMOS technology. The relations demonstrated between the different interface parameters/modes and the sensor conditions enable the user to optimize the interface performance with respect to noise and systematic errors. A user guide has been provided which can help inexperienced users to make an optimal choice among the various options. The measurement results, which are in close agreement with our simulation results, show that for a measurement time of 1s, resolution > 20 bits can be achieved. The data-acquisition rate can be as high as 4 kS/s. Even for the highest speed, the interface can still provide a resolution of > 13 bits. The nonlinearity measurement shows that for the 10 pF range, even with parasitic capacitances as large as 680 pF, the maximum nonlinearity error is smaller than 50×10^{-6}. By limiting the parasitic capacitance to 470 pF, the nonlinearity error is less than 25×10^{-6}, which corresponds to the linearity of 15 bits.

References

[1] S. Nihtianov, "High performance capacitive sensor electronic interfaces for displacement measurement in industrial applications", Sensor and Test, Nuremburg, Germany, 26-28 May 2009.

[2] F. van der Goes, Low-cost smart sensor interfacing, PhD thesis, Delft University of Technology, The Netherlands, 1996.

[3] F. van der Goes and G. C. M. Meijer, "A universal transducer interface for capacitive and resistive sensor element", Analog Integrated Circuit and Signal Processing, vol. 14, pp. 249-260, 1997.

CHAPTER 6

A novel interface with very high linearity

6-1 Introduction

As mentioned in section 4-8, in our interface the main source of non-linearity is found in the capacitance-to-voltage converter (CVC). In principle, the voltage-to-period converter and the integrator cannot cause any non-linearity. Therefore, by removing the CVC and using the voltage-to-period converter (VPC) as the capacitance-to-period converter (CPC) we can achieve a much higher linearity. Moreover, in a low-power design, decreasing one op-amp can be beneficial.

When using the VPC as the CPC, as explained in the section 4-3, in order to change the dynamic range of the interface, the values of C_{off1}, C_{off2}, C_{int} and $\hat{I}_{int}$ (Fig. 3-11(a)) should be changed accordingly. Consequently, the implementation becomes very complicated. Moreover, in the case of a large sensor capacitance, the values of the capacitors C_{off1}, C_{off2} and C_{int} become too large to enable integration on the chip. Solution to this problem has been presented by Meijer and Iordanov [1].

In [1] it is shown that for larger capacitive signals the range is limited by possible overload of the input integrator and that this range can be extended with a switched-capacitor interface with negative feedback. The circuit described in [1] was implemented with discrete components. However, in that work, no analysis is presented on noise, linearity and operating limitation of the interface.

In this chapter, it is shown that in addition to a better linearity, the application of negative feedback can also yield a higher noise performance. On the other hand, it will be shown that, due to the occurrence of a specific parasitic capacitor, in many practical applications the circuit with negative feedback cannot work properly unless specific measures are taken. The details of these problems and their solutions are presented in section 6-3.

6-2 The interface with negative feedback

Figure 6-1 shows the basic principle of the interface with negative feedback [2]. In this circuit it holds that $I_b = m\hat{I}_{int}$. The voltages V_1 and V_2 are block-shaped and have the amplitude of $V_{dd}/2$. The basic idea of the circuit is similar to that of the circuit presented in [1]. However, to enable implementation as a CMOS-integrated circuit, the circuit was modified and redesigned. To remove offset effects, we added a chopper, following the (+ - - +) principle, as described in chapter 4, section 4-6-1-1. Some important signals of this circuit are shown in figure 6-2.

To understand the basic principle of this circuit, we ignore the two feedback loops that are indicated with dashed lines, and assume that C_x and C_{o2} are identically driven. During the time interval T_1, φ_1 starts with a transient to the HIGH state, which causes the charge $Q_1 = V_{dd}C_{o1}$ of C_{o1} to be pumped into integrator capacitor C_{int}. Next, this charge is removed by integrating $\hat{I}_{int}$. During time interval T_1, capacitor C_x is charged by the supply-voltage source V_{DD}.

At the beginning of time interval T_2, φ_2 changes from low to high, the drive-side of C_x is

grounded, and the charge $Q_2 = V_{dd}\ (C_{o2} + C_x)$ is pumped into C_{int}. Also, this charge is removed by the integration of $\hat{I}_{int}$. Since the entire charge of C_x is pumped into C_{int} all at once, in the case of a large C_x, this will cause the integrator to overload.

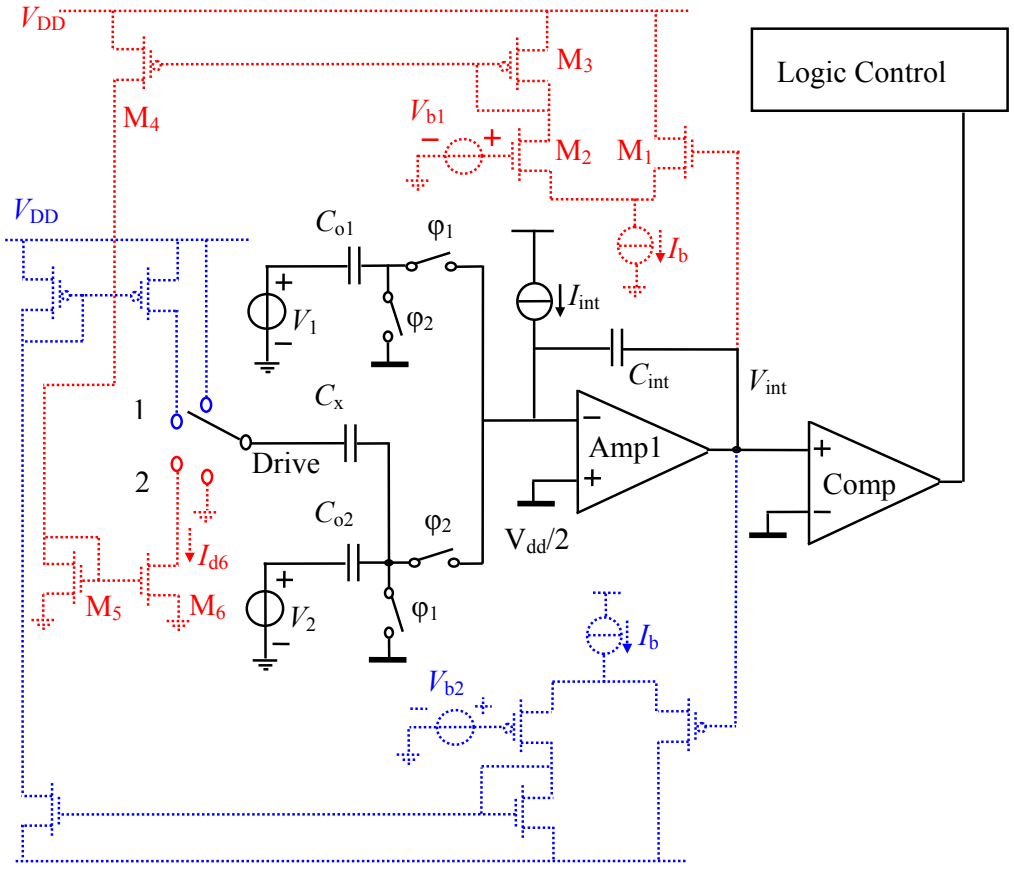


Fig. 6-1: The interface with negative feedback.

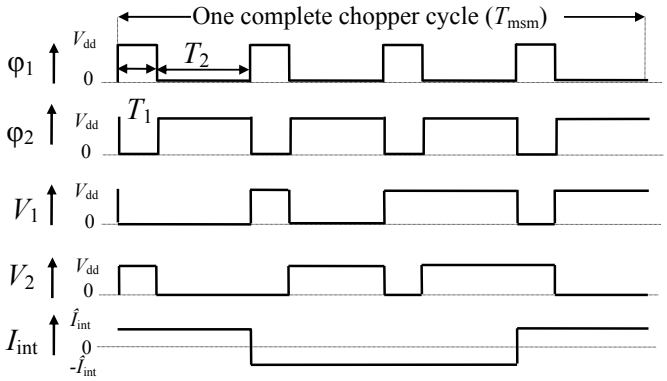


Fig. 6-2: Voltage signals related to the interface of Fig. 6-1.

However, in the circuit in figure 6-1, negative feedback controls the charge transfer speed in such a way that the integrator output voltage always remains in between the two values V_{b1} and V_{b2}. These values, which represent the input-bias voltages of the CMOS differential amplifiers, can easily be set by the designer. Figure 6-3 shows the asymptotic values of the integrator output voltage V_{int} for the circuit in figure 6-1 in the case of $I_b = 2\hat{I}_{int}$.

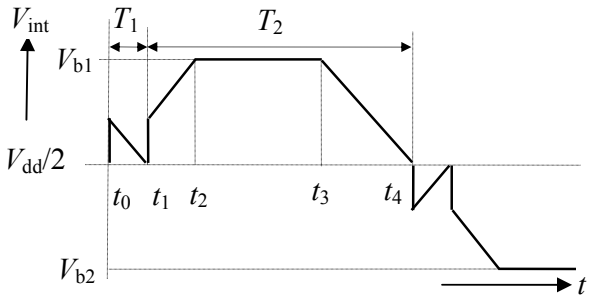


Fig. 6-3: The integrator output voltage V_{int} versus time.

From t_0 to t_1 the circuit integrates the current $\hat{I}_{int}$, which removes the charge pumped from C_{o1}. In this time interval, C_x is connected to V_{dd}. At t_1, C_x is connected to node 2 of the selector while C_{o2} pumps its charge into C_{int}. In the design, care has been taken to meet the condition $C_{int}/C_{o2} > V_{DD}/(V_{b1} - V_{DD}/2)$. In this case, immediately after t_1, the voltage V_{int} is still less than V_{b1}, and almost all bias current I_b of the differential amplifier travels to the left-hand branch so that C_x begins to discharge by I_b. Consequently, C_{int} is charged by I_b - $\hat{I}_{int}$. At t_2, V_{int} equals V_{b1}, at which point the negative feedback forces the integrator output voltage to remain constant, which occurs when the charge current through C_{int} is zero. In this case, the magnitude of the discharge current I_{Cx} of C_x equals $\hat{I}_{int}$. At t_3, the discharging of C_x is almost completed when the drain-source voltage across M_6 drops to almost zero. Then, the drain current of M_6 also drops so that the charge current through C_{in} approximately equals $\hat{I}_{int}$.

It can be shown that the inaccuracy of the bias currents I_b of the differential-amplifier stages does not have a significant effect on the accuracy of the total time intervals representing the capacitive signals. When all four chopper phases are taken into account in the +,-,-,+ order, one complete chopper cycle (Fig. 6-2) equals:

$$T_{msm} = \frac{4V_{dd}(C_{o1} + C_{o2} + C_x)}{\hat{I}_{int}}. \qquad (6\text{-}1)$$

6-3 Condition to be met for proper operation

In order to guarantee stability of the negative-feedback loop, certain conditions should be met. For instance, if we assume that the parasitic capacitances of sensor capacitance C_x (Fig. 6-1) are zero, then for a phase margin of 45 degree, it should hold that:

$$\omega_u \geq \frac{g_{m,D.A.}}{C_{int}}, \qquad (6\text{-}2)$$

where ω_u is the unity-gain bandwidth of the operational amplifier (Amp1 in Fig. 6-1), and $g_{m,D.A.} = \delta I_{d6}/\delta V_{int}$ is the trans-conductance of feedback path transistors M_1 to M_6. A similar condition should hold for the other side of the signal.

So far, the description of the negative feedback mechanism corresponds to that presented in [1]. However, in [1], some details of the discharging C_x in the triode region of M_6 during the time interval t_3 - t_4, along with the effect of any parasitic capacitance at the drive side of C_x, were overlooked. For optimal design, a good understanding of these details is crucial.

For the sake of convenience, the electrical model of a capacitive sensor with related parasitic capacitances C_{p1} and C_{p2} and the concept of the two-port measurement technique [3] are shown in figure 6-4.

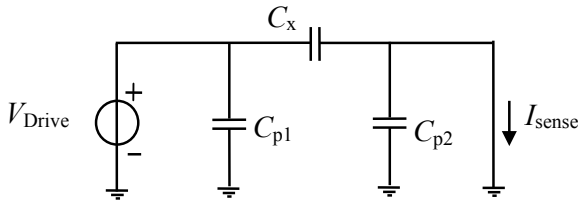


Fig. 6-4: The sensor capacitor C_x with parasitic interconnection capacitances in a setup for a two-port measurement.

According to the concept of the two-port measurement technique, the sensor is driven by a low-impedance voltage source, which eliminates the effect of C_{p1}, while the current I_{sense} is measured with a low-impedance current meter, which eliminates the effect of C_{p2}. However, in the circuit in figure 6.1, the driving source is a combination of voltage source and a current source. As will be shown later in this section, care is taken to guarantee that the initial and the final voltage is determined by the voltage source.

Let us first assume that $I_b = m\hat{I}_{int}$ and $C_{p1} = 0$ pF. During time interval t_2 to t_3 (Fig. 6-3), C_x can easily be discharged to V_{on} by the current $\hat{I}_{int}$. After that, M_6 enters the triode region, so that its drain current decreases. As long as I_{d6} is greater than I_{d5}/m, negative feedback forces the sensor discharge-current to be $\hat{I}_{int}$. However, after that, C_x is discharged exponentially. The drain-source voltage $V_{ds(exp)}$ of M_6 where this happens can easily be derived from the equation [4]:

$$\frac{\mu C_{ox} W}{L}((V_{gs} - V_T)V_{ds(exp.)} - V_{ds(exp.)}^2/2) = \\ = \frac{1}{m}\frac{\mu C_{ox} W}{2L}(V_{gs} - V_T)^2, \qquad (6\text{-}3)$$

where μ is the majority-carrier mobility in the channel, C_{ox} is the oxide capacitance for the active area, and W and L are the width and length of transistor M_6, respectively. The result is:

$$V_{ds(exp.)} = (1 - \sqrt{(1 - 1/m)})V_{on}, \qquad (6\text{-}4)$$

where $V_{on} = (V_{gs} - V_T)$ is the so-called over-drive voltage of M_6 for $I_{d6} = m\,\hat{I}_{int}$. For $m = 2$, these result in:

$$V_{ds(exp.)} = 0.3V_{on}. \qquad (6\text{-}5)$$

To find the condition that should be met in order to discharge C_x with the required accuracy, we assume that $V_{dd} = 5$V and $V_{on} = 0.33$V. Moreover, we assume that C_x discharges with a resolution of 15 bits, which corresponds to 1.5×10^{-4} V. From t_1 to t_3 (Fig. 6-3), C_x is discharged from 5V to 0.1V. Then from t_3 to t_4 it is discharged to 1.5×10^{-4} V. To achieve this, the following condition should be met:

$$\frac{(V_b - V_{dd}/2)C_{int} + 0.3C_x V_{on}}{\hat{I}_{int}} \geq 6.5R_{ds}C_x. \qquad (6\text{-}6)$$

The left-hand side of this equation represents the time available to discharge capacitor C_x, which is the time interval t_3 to t_4 in figure 6-3. The right-hand side represents the time needed

to discharge the capacitor C_x from 0.1 V to 1.5×10^{-4} V.

So far it has been assumed that $C_{p1} = 0$ pF (Fig. 6-4). If we assume that $C_{p1} \neq 0$ pF and that the maximal drain current of M_6 is equal to $I_{d6,max} = n\,\hat{I}_{int}$, and if we take into account the current loss via the parasitic capacitance C_{p1}, we find for the maximum available current $I_{Cx,max}$ for discharging C_x that:

$$I_{Cx,max} = \frac{n\hat{I}_{int}C_x}{C_x + C_{p1}}. \qquad (6\text{-}7)$$

First of all, the current $I_{Cx,max}$ should be at least larger than the integrator current $\hat{I}_{int}$, otherwise there will not be enough current to discharge the capacitor C_x. Figure 6-5 shows the integrator output voltage for three different cases of $C_{p1,}$ and therefore also for $I_{Cx,max}$. This figure can be drawn in the same way as figure 6-3. It is quite clear that in the case of large parasitic capacitance C_{p1}, where cause $I_{cx,max} < I_{int}$, the time period T_2 is affected by this parasitic, which creates a systematic error.

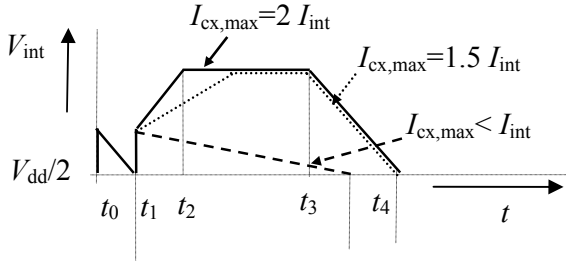


Fig. 6-5: The integrator output voltage V_{int} versus the time for different $I_{Cx,max}$.

For n=2, which is the case in design presented in [1], it is necessary that:

$$C_{p1} \leq C_x. \qquad (6\text{-}8)$$

In most applications, this condition cannot be satisfied. This problem is solved by increasing the maximum available current $I_{Cx,max}$. This can be accomplished in various ways, such as:

- by increasing the differential-amplifier bias current,
- by increasing the aspect ratio of M_6 with respect to M_5,
- by adding a resistor in the source of $M_{5,}$
- by any combination of these.

The last two ways are more power-efficient, because then –only when necessary– the current has a larger value. Assuming that $I_{d6,max} = n\,\hat{I}_{int}$, for the parasitic capacitor C_{p1} the condition to be met is:

$$C_{p1} \leq (n\text{-}1)C_x. \qquad (6\text{-}9)$$

For excessive values of the parameter n, the loop stability will decrease. For instance, when we need to measure a 1 pF capacitor in the presence of a 1-nF parasitic capacitor, then according to equation 6-9 it is necessary that $n \geq 1000$, which for practical reasons is too high. In our design, without increasing the amplifier bandwidth, the maximum value for n is about 40, which means that in the above-mentioned example, the maximum parasitic capacitance should be less than about 40 pF. This value can be increased at the cost of using more power

by increasing the amplifier bandwidth. This example shows that care must be taken to avoid circuit malfunction. In many applications, the condition of equation 6-9 can be met. In other cases, we have to use a conventional drive interface without negative feedback.

In this case, where $I_{d6,max} = n\hat{I}_{int}$, $V_{ds(exp.)}$ can easily be found from equation 6-4 by substituting $m = nC_x/(C_x+C_{p1})$. For instance, for $C_x/(C_x+C_{p1}) = 1/10$ and $n = 40$, we find that $V_{ds(exp.)} = 0.13V_{on}$. Note that V_{on} is the overdrive voltage of M_6 for $I_{d6} = 4\hat{I}_{int}$. The condition that should be met in order to discharge C_x with the required accuracy can be calculated in a similar way as shown in equation 6-6. For the same accuracy of 15 bits and the same V_{on}, this yields:

$$\frac{(V_{b1} - V_{dd}/2)C_{int} + 0.13C_xV_{on}}{\hat{I}_{int}} \geq 5.6R_{ds}(C_x + C_{p1}). \qquad (6\text{-}10)$$

Comparing conditions (6-10) and (6-6) shows that for a large parasitic capacitance C_{p1}, we need a much smaller R_{ds} to achieve the same level of accuracy.

In addition to equation 6-9, $(C_x + C_{p1})$ will have an upper-limit, which can be found in equation 6-10. For instance, in our design, where $V_{b1} = 4.5$ V, $V_{DD} = 5$ V, $C_{int} = 2.5$ pF, $\hat{I}_{int} = 0.7$ μA, $V_{on} \approx 0.3$ V and $R_{ds} = 2.5$ kΩ, it holds that:

$$(C_x + C_{p1}) \leq 550 \text{ pF}. \qquad (6\text{-}11)$$

6-4 Noise performance of the interface with negative feedback

The main part of the noise analysis presented in the chapter 4 is still valid. However, in this design we do not have a capacitance-to-voltage converter. It should be mentioned that during the design phase, many details about noise, which are explained in chapter 4, were not clear. For instance, despite the fact that there is no need for a fast comparator in our relaxation oscillator (based on our discussion in chapter 4), we used a fast comparator. With a fast comparator, the comparator noise can even dominate the noise performance of the interface [5]. Our discussion in this section is based on a fast comparator. It can be argued that after the analysis in chapter 4 about comparator requirements, we might not need this analysis anymore. However, it is possible to use a similar system without auto-calibration for faster operation. In that case, in order to minimize the comparator-delay related error, the user has to use a fast comparator. Therefore, it is still worthwhile to share our experience with the reader.

Another difference between this design and an optimized design in terms of noise, as presented in chapter 4, is the flicker-noise corner frequency of integrator current source. This flicker-noise corner frequency was designed to be lower than chopper frequency $f_{ch} = 1/T_{ch}$ (based on analysis in [6]). Fortunately due to the large transistor used for the required matching, this flicker-noise corner frequency was about 500 Hz, which is much lower than the chopper frequency f_{ch}, yet it is still much higher than required value ($f_c < 1/4NT_{ch}$) calculated in chapter 4.

Figure 6-6 shows the part of the interface that is important for the noise analysis.

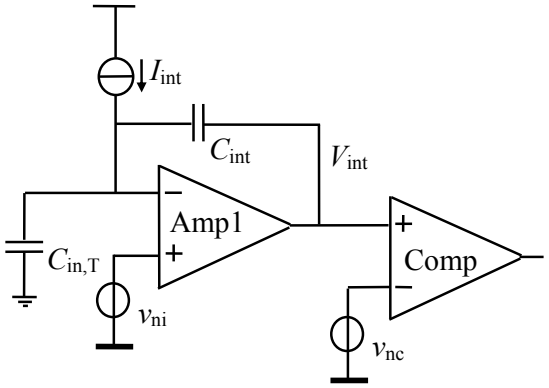


Fig. 6-6: Part of the interface for the noise analysis.

Amplifier Amp1 is an OTA, and therefore the total noise at the input of the comparator caused by this amplifier can be calculated based on equations 4-89 and 4-99, which amounts to:

$$v_{vni\text{-}comp\text{-}in} = \frac{\left(C_{int} + C_{in,T}\right)}{C_{int}} \sqrt{\frac{S_{vni} g_m}{4C_{in,T}}}, \tag{6-12}$$

where S_{vni} is the input noise voltage spectral density and g_m is the transconductance of the amplifier Amp1. It is clear that the voltage noise calculated by equation 6-12 is independent from the biasing current and that the biasing current is set based on the required bandwidth. In this calculation we suppose that the flicker noise can be removed by the applied chopper. During time interval T_1 (Fig. 6-2), the capacitance $C_{in,T} = C_{o1}$; however, during time interval T_2 this capacitance is:

$$C_{in,T} = C_x + C_{p2} + C_{o2} + C_{ref} + C_{off}, \tag{6-13}$$

where C_{ref} and C_{off} consist of two extra capacitors that are connected to the interface to perform auto-calibration. According to this equation, in the case of a large parasitic capacitor C_{p2}, the noise of the integrator amplifier can be dominant. However, in the case of small parasitic capacitor C_{p2}, the noise is probably dominated by the noise of the comparator [2, 5]. The jitter caused by the comparator in each decision time is calculated, as presented in equation 4-11. For convenience, this equation is repeated here:

$$J_{vnc} = \frac{v_{nc}}{\partial V_{int}/\partial t} = \frac{v_{nc} C_{int}}{I_{int}}, \tag{6-14}$$

where v_{nc} is the equivalent input voltage noise of the comparator.

To evaluate the effect of negative feedback on the noise performance of the interface, we assume for the conventional interface, with V_{dd} = 5 V, that at the beginning of time interval T_1 (Fig. 6-7(a)), the voltage step in V_{int} is 0.5 V. Furthermore, for the maximum input capacitance $C_{x,max}$ and at the beginning of time interval T_2, we assume that this step is 2 V.

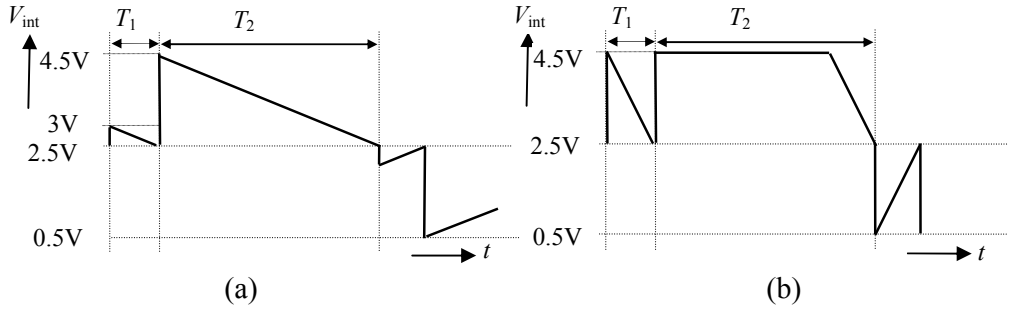


Fig. 6-7: The integrator output voltage: (a) without negative feedback and (b) with negative feedback when the integrator capacitor has been decreased by a factor of 4.

With these voltage steps, overload of the integrator is avoided so that the linearity and dynamic range are guaranteed. With the circuit in figure 6-1, thanks to the negative feedback we are able to decrease the integrator capacitor by a factor of 4, which results in a step of 2 V in V_{int} during both T_1 and T_2 (Fig. 6-7(b)). Due to the steeper voltage slope G, the noise contribution of the comparator is decreased by a factor of 4. To obtain the voltage swing mentioned above, it is essential that $V_{b1} \geq 4.5$ V and $V_{b2} \leq 0.5$ V. The accuracy of these voltages does not affect the accuracy of the interface. The only restriction for them is that their values are within the output-swing range of the integrator amplifier. Therefore, implementation of these voltages is simple. Figure 6-7(b) shows the integrator output voltage V_{int} for $V_{b1} = 4.5$ V and $V_{b2} = 0.5$ V.

6-5 Implementation and measurement results

The interface with negative feedback was designed and implemented in standard 0.7µm CMOS technology. Figure 6-8 shows a photograph of the chip. The supply voltage is 5 V and the measured value for the supply current is about 1.4 mA. As mentioned in chapter 3 section 3-5-6, the effects of the channel-charge injection and clock feedthrough of the chopper switches in our system are negligible. Therefore, the size of switches is optimized based on the required settling and chip area.

Because of the three-signal auto-calibration technique used [7], each measurement cycle consists of three phases: one to measure the offset capacitor C_{off}, one for the reference capacitor C_{ref}, and a third one for the sensor capacitor C_x. The data is read via a serial port (RS232) and analyzed using a Labview program.

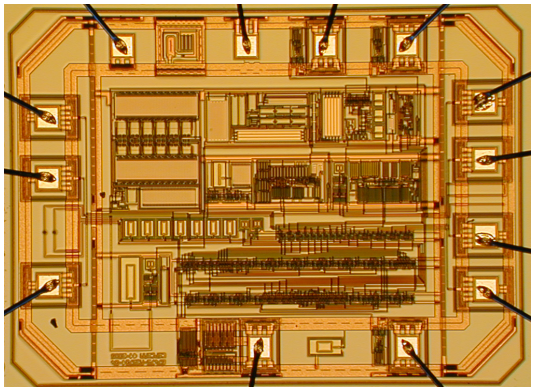


Fig. 6-8: Photograph of the chip, which measures 1.4 mm × 1.9 mm.

According to the principles described above, the selected capacitor in phase T_2 is first driven by a current source and afterwards by a voltage source. The non-selected capacitors are connected to ground, since it is necessary to keep the systematic error to a minimum. Figure 6-9(a) shows an overview of the interface system with its external capacitors. We measured the different periods of the output signal (Fig. 6-9(b)) with a micro-controller. The microcontroller has an internal counter with a sampling frequency of 5 MHz, which can measure each period T_{off}, T_{ref}, and T_x by detecting the corresponding increases in the interface output signal. When necessary, the user of the interface can reduce the quantization noise by using a microcontroller with a faster counter. In this way, the level of quantization noise can be decreased to less than that of thermal and shot noise.

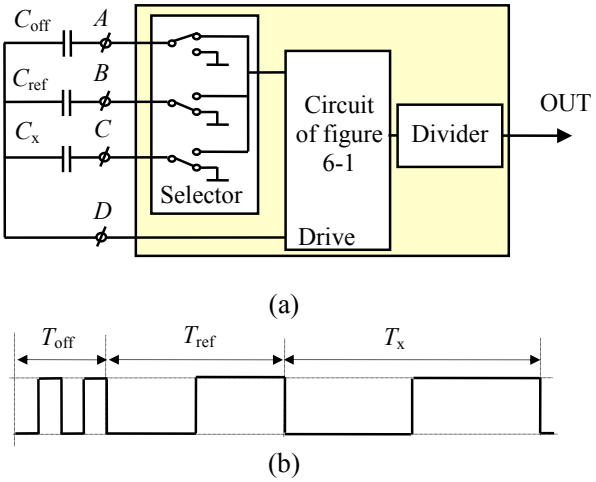


Fig. 6-9: (a) Block diagram of the interface system and (b) its output signal.

In order to verify the results of the analysis of section 6-4 and to demonstrate the effect of negative feedback for the noise, the chip design includes the option to decrease C_{int} by a factor of 4 by laser-cutting a part of it off. Capacitors C_{o1} and C_{o2} are equal and their values are selected in such a way that, before laser-cutting, the step in the integrator output voltage is 0.5 V, as is mentioned in section 6-4. Next, after decreasing C_{int}, this step is 2 V. Figure 6-10 shows the measurement results for the measurement time of 100 ms before and after laser-cutting.

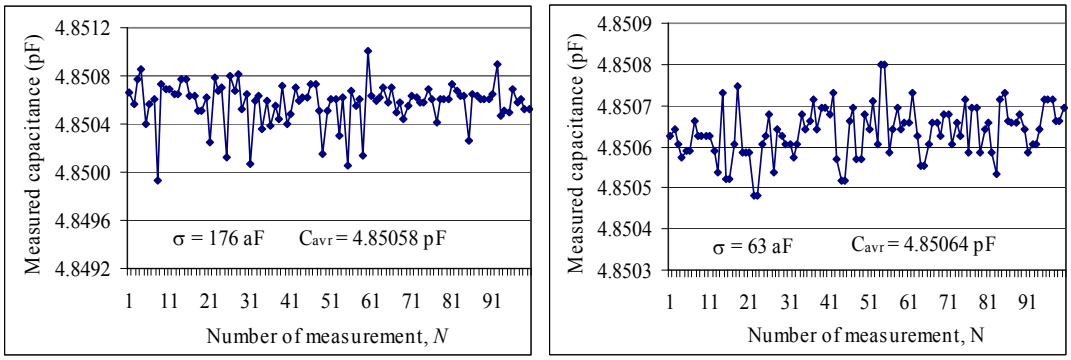


Fig. 6-10: Measurement results for C_x with a nominal value of 4.7 pF while the measurement time is 100 ms for each plotted point: (a) for an integrator capacitor C_{int}= 10 pF, and (b) for C_{int}= 2.5 pF.

It can be concluded that increasing the slope of the integrator output voltage by a factor of 4 results in 2.8 times less noise. The measurement was performed for C_p = 0 pF. Also the comparator on this design is a fast comparator. Based on the provided design parameters, the noise of the interface should be dominated by that of the comparator. According to our discussion in section 6-4 we should expect the improvement in the noise performance of the interface by a factor of 4. In that discussion we assumed that the input referred noise of the comparator is independent from its input signal. Moreover we supposed that the noise of integrator amplifier is much less than that of the comparator.

However, in chapter 4 section 4-6-1-3 we showed that the effective noise-bandwidth of a comparator is increased by increasing the slope of its input signal (Eq. 4-37). Therefore, we can expect to have higher input-referred noise when the slope is increased. This can partly explain the difference between the measurement result and the theory. Moreover, the noise of integrator amplifier contributes somewhat to the output jitter, which cannot be decreased by decreasing the integrator capacitor C_{int}. The achieved noise level corresponds to a resolution of 16.2 bits, which is more than one bit better than the resolution reported in [6] for the UTI.

Figure 6-11 shows the effect of the cable parasitic capacitor C_{p2} on the noise performance of the interface. In this case, laser cutting is applied so that the noise contribution of the comparator is decreased. In addition to a decrease in resolution, capacitor C_{p2} also causes a systematic error, which is shown in figure 6-12. The figure shows that for a parasitic capacitance up to 470 pF, the relative error is less than 0.1%. However, for C_{p2} = 1nF, this error increases to 0.5%.

As discussed in section 6-3, the effect of the parasitic capacitor C_{p1} (Fig. 6-4) depends heavily on the value of capacitor C_x. Care should be taken that condition (6-5) is met (in our design $n \cong 40$). In our measurement we found that for C_x = 10 pF, a parasitic capacitor C_{p1} < 330 pF does not cause a significant error. However, for a parasitic capacitance with a value higher than the capacitance calculated using equation 6-5, the performance of the interface is seriously degraded. For instance, for C_{p1} = 470 pF, the measured result for C_x is about 5 pF instead of 10 pF, which is in agreement with the calculations in section 6-3.

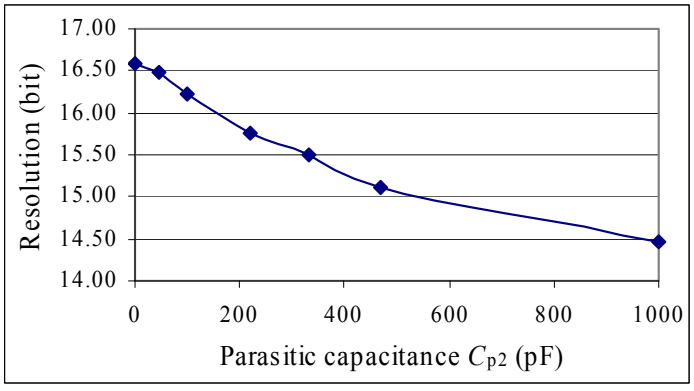


Fig. 6-11: The effect of parasitic capacitor C_{p2} on the resolution for C_{ref} =15 pF, C_x =10 pF, and measurement time of 100 ms.

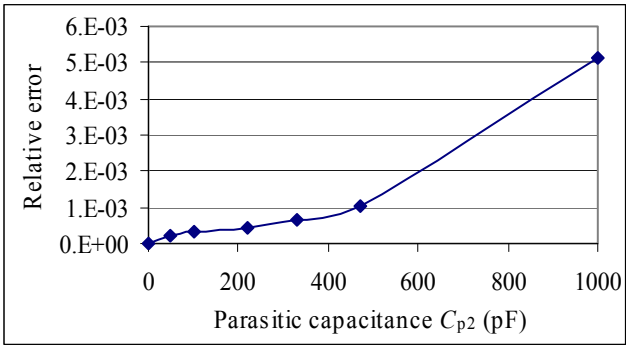


Fig. 6-12: Measured relative error caused by the parasitic capacitor C_{p2} for C_{ref} = 15 pF and C_x = 10 pF.

As is mentioned in chapter 4 section 4-9, the measurement of the nonlinearity requires some care. In order to remain unaffected by the PCB parasitic capacitances while lacking absolute accuracy, the nonlinearity λ has been calculated according to the following equation [2]:

$$\lambda = \frac{T_{C_{ref2}+C_{ref3}} - T_{C_{ref1}+C_{ref3}}}{T_{C_{ref2}} - T_{T_{C_{ref1}}}} - 1. \qquad (6\text{-}15)$$

The measurement should be arranged in such a way that during the measurement no parasitic capacitances (parasitic capacitances of PCB) are changed. Therefore, not only the wiring of the setup, but also the position of any of the conductors should be invariable [3].

In our nonlinearity tests, we selected different combinations of C_{ref1}, C_{ref2} and C_{ref3} in such a way that C_{ref1}, C_{ref2}, C_{ref1}+C_{ref3}, and C_{ref2}+C_{ref3} always stayed within the range of 1 pF to 300pF. Our experimental results show that the nonlinearity is less than 50×10^{-6} over the full range, which is five times better than that reported in [6]. Note that the dynamic range of the interface presented in this paper is much wider than that presented in [6]. Therefore, a straightforward comparison of the mutual results of the different interfaces is not possible and should be evaluated using practical setups.

In addition, we measured the effect of the interface temperature on the overall measurement results. During this experiment, we kept C_x at a constant temperature; however, C_{ref} was kept at the same temperature as the interface. Figure 6-13 shows the measurement results for different interface temperatures, where C_{ref} = 15 pF and C_x = 10 pF (nominal values), both of which are type NP0. The offset capacitor C_{off} was about 0 pF. If the reference capacitor has a temperature coefficient of about 50 ppm, then by changing temperature from -55ºC to 125ºC the reference capacitor can change up to 127 fF on average. This reference capacitor variation by temperature can cause the error of 85fF in the input capacitance measurement. This error is quite close to the measured error. Therefore, it can be concluded that the measured temperature effects are mainly due to those of the reference capacitor C_{ref}, where its temperature varies together with the rest of the interface circuit. To check this we performed another measurement with the reference capacitor at a fixed temperature with only the interface being located in the oven. In this measurement we could not see any significant error in the measured capacitor for the above-mentioned temperature range.

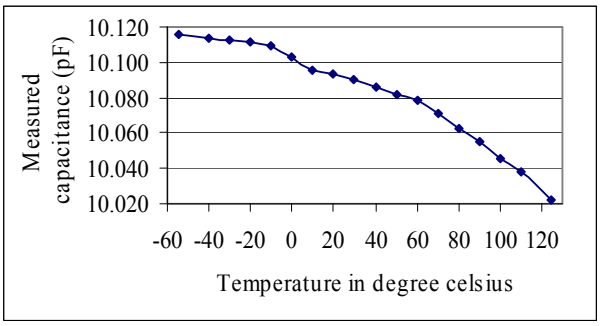


Fig. 6-13. Measurement results for a capacitance with a nominal value of 10 pF at different temperatures.

6-6 Conclusion

An integrated interface for capacitive sensors has been designed and implemented in 0.7μm CMOS technology. It was shown that, due to the occurrence of sensor parasitic capacitor, in many practical applications the circuit with negative feedback cannot work properly unless specific measures are taken. Also it was shown that by applying negative feedback, a higher resolution of at least one additional bit can be achieved. The achieved noise level corresponds to a resolution of 16.2 bits for a measurement time of about 100 ms. Moreover, the introduced interface has very negligible nonlinearity behaviour. However, due to presence of PCB parasitic capacitance, measuring this small nonlinearity is not possible with the existing method. Therefore, a novel method for measuring the nonlinearity which is insensitive to PCB parasitic capacitance is presented. Our experimental results show that the nonlinearity is less than 50×10^{-6} over the full range.

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CHAPTER 7

An integrated interface for leaky capacitive sensors

7-1 Introduction

Depending on the properties of the dielectric materials, the leakage of capacitive sensors can be an issue, for instance, with humidity sensors, level measurement or other applications.

The immunity of the measurements to leakage can be improved using the method reported in [1]. In this method the sensor capacitance is discharged with various time intervals. After read-out and calculation, the capacitive components of the sensor capacitance are found. This method has two drawbacks: (a) a significant increase of the measurement time, and (b) when the leakage conductance exceeds a certain value, due to the DC voltage across the sensor, the interface does not work properly. Yet, for a capacitance of 1.2 pF, the relative error caused by a leakage conductance of less than 0.4 μS is reduced to a value of less than 1.5×10^{-3} [1].

The first drawback is eliminated with an alternative design in which the leaky capacitive sensor is charged with a low-ohmic voltage source. Afterwards, this charge is transferred to a high-quality capacitor as fast as possible [2].

In [2] an analysis of the errors is missing as related to the main design parameters. Moreover, experimental results are limited to rather small capacitive values of up to the level of a few pF, which is rather small for, for instance, humidity sensors and level measurement. Moreover, the experimental interface circuit was implemented with discrete components only.

In this chapter an integrated version of the circuit is presented. A prototype of this interface was designed, and is implemented using 0.7μm standard CMOS technology. This circuit is optimized for sensor capacitances in the range of 30 pF to 500 pF. Experimental results are analyzed. A discussion of design opportunities and constraints is also presented.

7-2 Circuit principles

The applied front-end circuit for leaky capacitive sensors consists of a capacitance-to-voltage converter which is similar to the front-end of high-quality capacitors (chapter 3, section 3-4-2). The main differences are found in the details of the design and in the applied sensor-drive signal. The front-end is designed in such a way that after charging the sensor capacitor with a well-known voltage, the sampled charge is transferred to a high-quality capacitor as fast as possible. To minimize charge loss during the charge-transfer phase, the DC voltage across the sensor is kept at zero. Yet, due to transients, some charge is lost, which can be minimized by maximizing the speed of charge transfer.

Figure 7-1 shows the novel CVC with the most important signals. The capacitors C_{off} and C_{ref} are external capacitors, the resistor R_x represents the leakage resistance of a leaky capacitive sensor C_x. The other components are implemented inside the chip. The pins of the chip are named A, B, C and D.

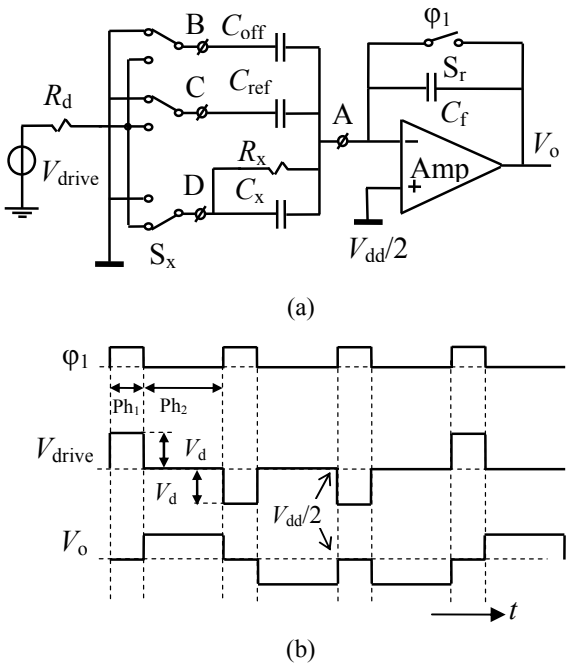


Fig.7-1. (a) A capacitor-to-voltage converter (CVC) for leaky capacitive sensor; (b) the most important related signals.

In phase 1, when φ_1 is high (Fig. 7-1(b)), the selected capacitor C_{in} (i.e. C_x, C_{ref} or C_{off}) is charged to $V_{drive} - V_A \approx V_d$. In phase 2 the charge $C_{in}V_d$ is pumped into the capacitor C_f and causes the output voltage V_o to jump to a value of $C_{in}V_d/C_f$. It is clear that in the ideal case (ideal switches, op-amp and driving-voltage source), R_x cannot affect the output voltage. The effects of non-zero ON resistance R_{on} of the applied switches, non-zero output resistance R_d of the driving voltage source, and limitations of real amplifiers, will be discussed in section 7-3.

7-3 Error analysis

The effects of different sources of error, such as offset, nonlinearity error, and the limited resolution of our interface, have already been analyzed in chapter 4. Therefore, in this section we will only consider the error caused by leakage. This error can be divided into two parts: the charging phase error and the charge-transfer phase error. In this section, we will investigate these errors in more details.

7-3-1 Error caused by leakage during the charging phase

As mentioned in the previous section, in phase 1, the selected capacitor is supposed to be charged to $V_{drive} - V_A \approx V_d$. Although this is correct for C_{off} and C_{ref}, the situation is more complex for C_x. Figure 7-2 shows the CVC for the charging phase when sensor capacitance C_x is selected, where $R_{on,x}$ is the ON resistance of switch S_x (Fig. 7-1(a)) and R_d is the output resistance of the signal source. The resistance $R_{on,r}$ is the ON resistance of the reset switches S_r.

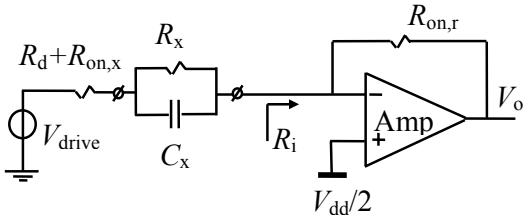


Fig.7-2. The capacitance-to-voltage converter (CVC) in the sampling phase when the sensor capacitance is selected.

With the help of Fig. 7-2, ignoring the settling error, the final voltage of the sensor capacitance is found to be:

$$V_{C_{x,final}} = (V_{drive} - \frac{V_{dd}}{2}) \frac{R_x}{R_d + R_{on,x} + R_x + R_i}, \tag{7-1}$$

where R_i is the input resistance of the amplifier, as indicated in figure 7-2.

Therefore, the relative charging error equals:

$$\varepsilon_{r,ch} \approx \frac{R_d + R_{on,x} + R_i}{R_x}. \tag{7-2}$$

When the amplifier in figure 7-2 is a one-stage OTA with transconductance g_m, the input resistance R_i amounts to $1/g_m$. Then, for instance, to obtain $R_i = 100\Omega$, even with very large input transistors biased in weak inversion, a biasing current of several mA would be required. However, in the case of a buffered amplifier, with parameters corresponding to those in figure 7-3, for the buffered amplifier with feedback resistor $R_{on,r,}$ we have:

$$R_i = \left(R_{on,r} + R_{out}\right) \Big/ \left(1 + g_m R_o\right) \ . \tag{7-3}$$

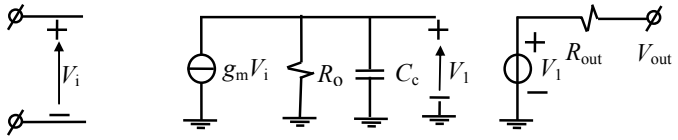


Fig. 7-3: A simple small-signal model of a buffered amplifier using an OTA followed by a voltage follower.

It is clear that in this case, R_i can be ignored. Then the main sources of charging error is due to the ON resistance $R_{on,x}$ of switch S_x, and the output resistance R_d of the driving source. In that case the error amounts to:

$$\varepsilon_{r,ch} \approx \frac{R_d + R_{on,x}}{R_x} \ . \tag{7-4}$$

For instance, for $R_1 = 100\Omega$ with a charging error < 0.1%, the leakage resistor R_x should be larger than 100 kΩ.

7-3-2 Errors caused by leakage during charge-transfer phase

During the charge-transfer phase, there are two types of error due to leakage: a) error due to small DC-voltage differences across the sensor, and b) error due to voltage differences across the sensor at the transient moment. In this section, these errors will be analyzed.

7-3-2-1 Error caused by a DC-voltage difference across the sensor

The drive voltage during charge-transfer phase is $V_{dd}/2$ (Fig. 7-1(b)); however, the other side of the sensor is connected to $V_{dd}/2 + v_{io}$, where v_{io} is the input offset voltage of the CVC amplifier (Fig. 7-4).

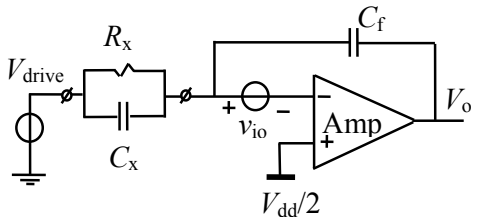


Fig. 7-4: CVC during the charge-transfer phase.

During the charge-transfer phase a DC current of v_{io}/R_x passes through the sensor. The CVC output voltage at the presence of the offset and is shown in figure 7-5. The slope during the time intervals T_2 and T_4 are caused by the DC currents through R_x.

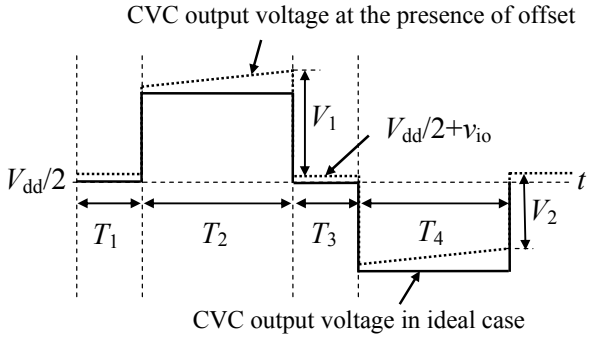


Fig. 7-5: The CVC output voltage at the presence of the offset.

The output of the next stage, which is a voltage-to-period converter (chapter 3, section 3-4-3), is proportional to $|V_1| + |V_2|$ (Fig 7-5). In the ideal case, $T_2=T_4$ and V_1+V_2, so that $|V_1| + |V_2|$, rendering the output period independent from the offset voltage of the CVC amplifier and also independent from the leakage caused by this offset. However, in practice, T_2 and T_4 only differ slightly (chapter 4, section 4-5) and therefore leakage will cause some residual error. Because the leakage exists even during the offset and the reference measurements, part of this error is removed by auto-calibration [chapter 3, section 3-3-1].

7-3-2-2 Error caused by a voltage difference across the sensor at transient moments

Due to the finite charge-transfer speed and the finite fall-time and rise-time of the drive signal, a transient voltage will appear across the sensor. To calculate this transient voltage and the resulting error, figure 7-6 depicts a section of the front-end during the charge-transfer

phase. This figure is an extension of figure 7.2, where the capacitor C_1 is the total capacitance of the non-selected capacitors to ground, including C_{off}, C_{ref}, and the parasitic capacitance of the sensor C_p.

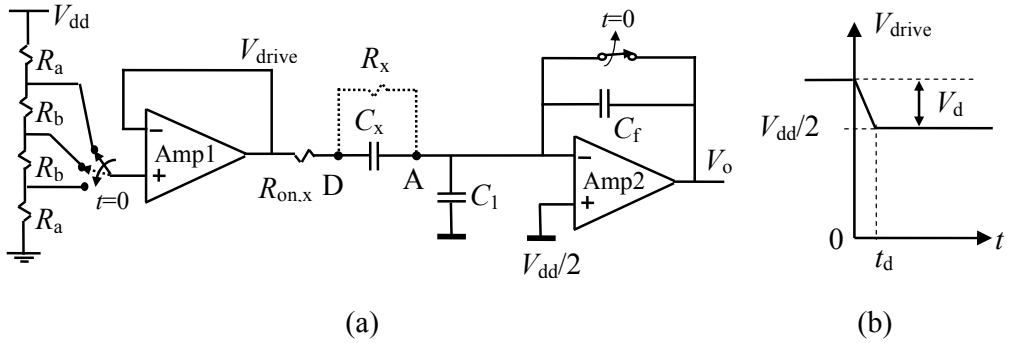


Fig. 7-6. (a) Section of the front-end for calculation of transient voltage across the sensor capacitance and (b) the simplified drive voltage.

The resistor divider at the left hand side of the figure creates $V_{dd}/2$ and $V_{dd}/2 \pm V_d$. This figure shows the case that the sensor capacitor C_x is charged to $V_{dd}/2 + V_d$ and then, at the time $t = 0$ s, the charge $C_xV_d/2$ is transferred to C_f. This is correct if the charge transfer takes place infinitely fast. However, due to not only the finite fall time of drive signal, but also the presence of the resistance $R_d + R_{on,x}$ and the limited bandwidth of the op-amp, there is a transient voltage across the sensor capacitor and therefore some charge is lost through the leakage resistor. To calculate this charge loss we first calculate the effect of each of these three non-idealities separately. In all cases the effect of leakage resistor on the voltage across the sensor can be ignored.

7-3-2-2-1 Error caused by finite fall-time

The finite fall-time of the drive voltage is mainly caused by the limited slew-rate of the drive amplifier Amp1 (Fig. 7-6). This amplifier is a one-stage OTA followed by a buffer stage. Therefore, its slew-rate is almost independent from its load and therefore it is determined by the compensation capacitor at the output node of the OTA and the available current at this node. If $R_d+R_{on,x} = 0$ and the op-amp has an infinite bandwidth $\omega_T \rightarrow \infty$, then the op-amp can keep its input node A (Fig. 7-6) at the biasing level $V_{dd}/2$; only due to the transient at node D is some charge lost. This charge loss can simply be calculated as follows:

$$V_{DA}(t) = V_d\left(1 - t/t_d\right) \quad \text{for} \quad 0 \le t \le t_d . \tag{7-5}$$

The leakage current equals:

$$I_{leakage,SR}(t) = \frac{V_{DA}(t)}{R_x} . \tag{7-6}$$

In this case, the total charge loss amounts to:

$$Q_{loss,SR} = \int_{t=0}^{t_d} I_{leakage,SR}(t)dt = \frac{V_d t_d}{2R_x} . \tag{7-7}$$

7-3-2-2-2 Error caused by $R_1 = R_d + R_{on,x}$.

In this part we suppose that $t_d = 0$, $R_1 << R_x$ and the op-amp has an infinite bandwidth of $\omega_T \rightarrow \infty$. Then the charge loss can be calculated as:

$$V_{DA}(t) = V_d e^{-t/R_1 C_x} \tag{7-8}$$

$$I_{leakage,R_1}(t) = \frac{V_d}{R_x} e^{-t/R_1 C_x} \tag{7-9}$$

$$Q_{loss,R_1} = \int_{t=0}^{t=\infty} I_{leakage,R_1}(t)dt = \frac{V_d R_1 C_x}{R_x}. \tag{7-10}$$

7-3-2-2-3 Error caused by finite bandwidth of the op-amp

When calculating the error due to the finite op-amp bandwidth, we suppose that $t_d = 0$ s and $R_1 = 0$ Ω. Furthermore, we assume that the transient response of CVC amplifier Amp2 (Fig.7-6(a)) is not limited by its slew rate (which is the case in our system). In that case, the transient voltage at node A can be calculated as follows: Immediately after switching, the charge of $C_x V_d$ is redistributed among C_x, C_f and C_1, while the amplifier output V_o remains constant. Therefore, the initial value of node A equals:

$$V_A(0^+) = \frac{V_{dd}}{2} - \frac{V_d C_x}{C_x + C_f + C_1}. \tag{7-11}$$

By ignoring the effect of limited op-amp gain, the final voltage at this node is $V_{dd}/2$. With the help of figure 7-7, the corresponding time constant is calculated as:

$$\tau_{op\text{-}amp} = \frac{C_c(C_x + C_f + C_1)}{g_m C_f}. \tag{7-12}$$

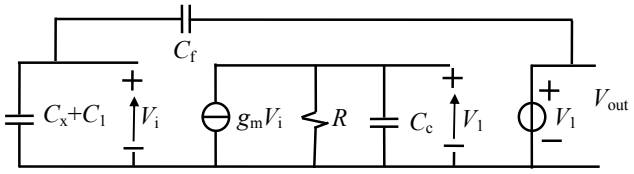


Fig. 7-7: Section of the front-end for calculating the time constant created by op-amp.

The transient voltage across the sensor caused by transient at node A can be written as:

$$V_{DA}(t) = \frac{V_d C_x}{C_x + C_f + C_1} e^{-t/\tau_{op\text{-}amp}}. \tag{7-13}$$

Similar to Eq. (7-10), the charge loss is calculated and is found to be:

$$Q_{loss,\omega_T} = \frac{V_d C_x}{\omega_T R_x C_f}, \tag{7-14}$$

where $\omega_T = g_m/C_c$ is the cut-off frequency of the op-amp.

7-3-3 Total error before auto-calibration

With all the charge loss from equations (7-7), (7-10) and (7-14), the total charge loss $Q_{\text{loss,ch.t}}$ can be calculated. The result is:

$$Q_{\text{loss,ch.t}} = \frac{V_{\text{d}} C_{\text{x}}}{R_{\text{x}}} \left(\frac{t_{\text{d}}}{2C_{\text{x}}} + R_{\text{l}} + \frac{1}{\omega_{\text{T}} C_{\text{f}}} \right). \tag{7-15}$$

The error caused by this charge loss cannot be removed by chopping. This is because, independent from direction of drive voltage, some charge is always lost.

Therefore, taking into account the actual charge $V_{\text{d}}C_{\text{x}}$ to be transferred, the relative error in charge-transfer phase is equal to:

$$\varepsilon_{\text{r,ch.t}} = \frac{-1}{R_{\text{x}}} \left(\frac{t_{\text{d}}}{2C_{\text{x}}} + R_{\text{l}} + \frac{1}{\omega_{\text{T}} C_{\text{f}}} \right). \tag{7-16}$$

The total relative error $\varepsilon_{\text{r-Cx}}$ of the capacitance-to-voltage conversion including the error for the charging phase (Eq. (7-4)) is:

$$\varepsilon_{\text{r,C}_{\text{x}}} = \frac{-1}{R_{\text{x}}} \left(\frac{t_{\text{d}}}{2C_{\text{x}}} + 2R_{\text{l}} + \frac{1}{\omega_{\text{T}} C_{\text{f}}} \right). \tag{7-17}$$

Example 7-1: Suppose that the interface is designed for capacitances up to 500 pF, (see section 7-4) and that the on-chip feedback capacitor C_{f} =100 pF and the drive voltage step V_{d}=0.25 V. The drive voltage can be simplified as shown in figure 7-6(b). Let us suppose that t_{d}=70 ns and that the output resistance R_{d} can be ignored. Moreover, suppose that the CVC amplifier is a one-pole system with ω_{T}=24 Mrad/s (actually it is two-pole system with a unity-gain phase margin of 50 degrees), and that the ON resistance of the switches R_{on}=120 Ω and that R_{x} =100 kΩ. For this case, for different sensor capacitances we have calculated the relative error of the capacitance-to-voltage conversion in two ways: (a) using equation (7-17), which is based on our simple analysis, and (b) with a more accurate simulation with Cadence software. The results are shown in figure 7-8.

The small difference between our simple calculation and the more accurate Cadence simulation is mainly due to the difference in the drive signals, which are more complex than those modeled in figure 7-6(b). From equation (7-17) we can conclude that for a smaller capacitance C_{x} the differences between the two calculations is greater, which agrees with the result depicted in figure 7-8.

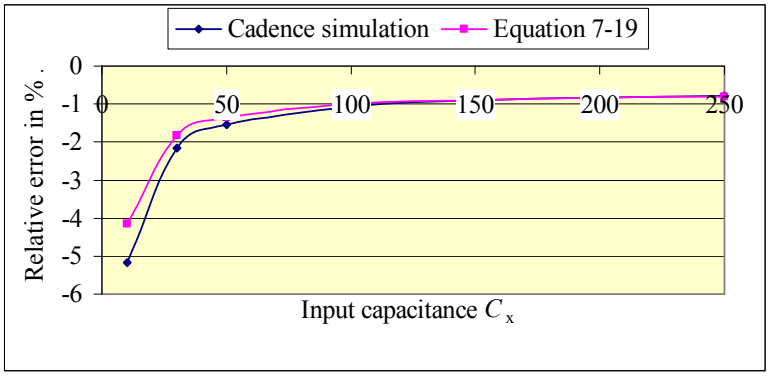


Fig. 7-8. The comparison of the calculated relative error of the capacitance-to-voltage converter for R_x =100 kΩ; (a) using the simple equation (7-17), and (b) using a more accurate Cadence simulation.

7-3-4 Total error after auto-calibration

Figure 7-1 shows that in all three measurement phases (offset, reference and sensor capacitance) the leaky capacitor is connected to node A. Therefore, in all three phases the transient voltage at node A causes some charge loss. Equation (7-12) shows that the time constant of this transient voltage is independent from the selected capacitor. However, as shown by equation (7-13), the magnitude of the transient and the corresponding charge loss are proportional to the value of the selected capacitor. Based on equation (7-14), the relative error in the C_{ref}-to-voltage conversion $\varepsilon_{r,Cref}$ is equal to:

$$\varepsilon_{r,Cref} = \frac{1}{R_x \omega_T C_f}. \tag{7-18}$$

After auto-calibration and when C_{off} = 0pF, for the error in the ratio V_x/V_{ref} it can be found that:

$$\frac{V_x}{V_{ref}} = \frac{V_{x,Ideal}\left(1-\frac{t_d}{2C_xR_x}-2\frac{R_l}{R_x}-\frac{1}{\omega_T C_f R_x}\right)}{V_{ref,ideal}\left(1-\frac{1}{\omega_T C_f R_x}\right)}, \tag{7-19}$$

where, V_x and V_{ref}, $V_{x,Ideal}$ and $V_{ref,Ideal}$ are the output voltages of CVC during the selection of C_x and C_{ref}, respectively. The index "ideal" refers to the case that $R_x \to \infty$.

If:

$$\frac{1}{\omega_T C_f R_x} \ll 1, \tag{7-20}$$

then

$$\frac{V_x}{V_{ref}} = \frac{V_{x,Ideal}}{V_{ref,ideal}}\left(1-\frac{t_d}{2C_xR_x}-2\frac{R_l}{R_x}\right). \tag{7-21}$$

Therefore, the relative error $\varepsilon_{r,Cx,autocal}$ after auto-calibration equals:

$$\varepsilon_{r,Cx,auto\text{-}cal.} = \frac{-1}{R_x}\left(\frac{t_d}{2C_x}+2R_l\right). \tag{7-22}$$

The result of this simple analysis is checked with a Cadence simulation of the complete interface, as shown is in figure 7-9. For this verification analysis, the conditions were identical to those mentioned in example 1.

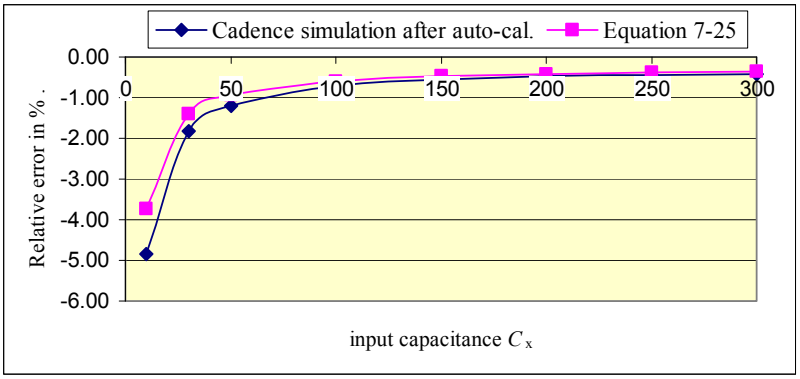
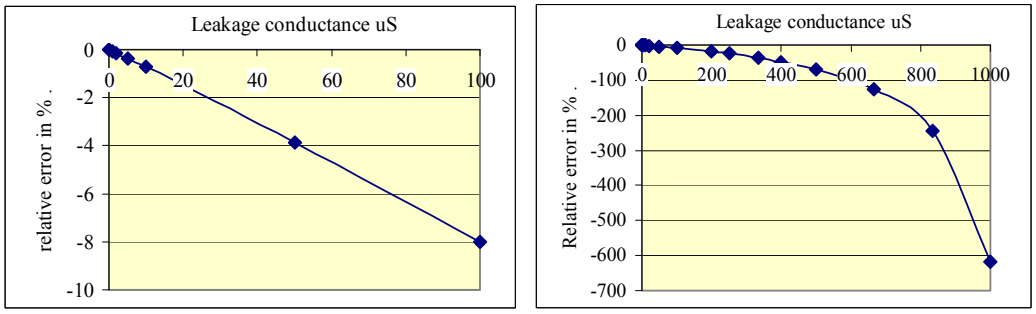


Fig. 7-9. Comparison of the calculated relative errors of the converter with auto-calibration for R_x =100 kΩ (a) using equation (7-25), which is based on a simple analysis, and (b) using a Cadence simulation of the complete interface circuit.

7-3-5 Effect of leakage resistance on the transient voltage

Although it is easy to understand that a small leakage will not have a large effect on transient voltage at node A and D (Fig. 7-6(a)). Yet, for larger leakage this assumption is no longer valid. Consequently, for a given condition, the error up to a certain leakage will be proportional to the leakage conductance; for larger leakage the error is larger than the predicted value in equation (7-22). To show this, we simulated the interface error with Cadence with the parameters of example 1 for a capacitance C_x of 100 pF with leakage conductance ranging from 0.1µS up to 1mS. As is shown in figure 7-10, for leakage conductance higher than about 500 µS, the simple equation (7-22) is no longer valid.



(a) (b)

Fig. 7-10. The results of a Cadence simulation including the relative error after auto-calibration of the converter for an input capacitance of 100 pF and leakage conductance of (a) up to 100µS and (b) up to 1mS.

7-4 Implementation and measurement results

Figure 7-11(a) shows a simplified block diagram of the complete interface, including three-signal auto-calibration. The interface output signal is shown in figure 7-11(b). With three-signal auto-calibration, a single measurement cycle consists of three phases: one to measure the offset capacitor C_{off}, one for the reference capacitor C_{ref}, and a third one for the sensor

capacitor C_x. The different time intervals T_{ref}, T_{off} and T_x represent the periods of the square-wave output signal during the measurements of C_{off}, C_{ref} and C_x, respectively.

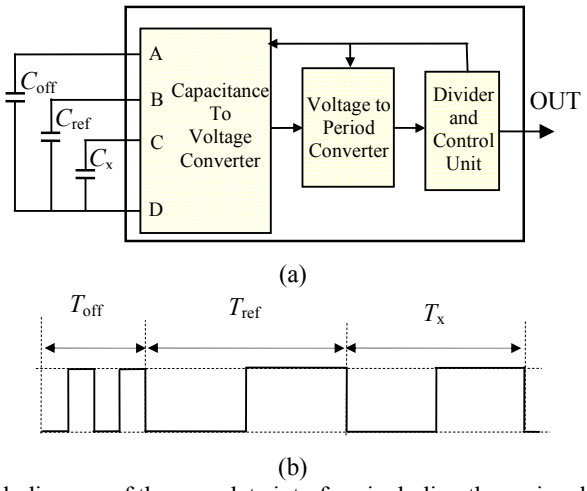


Fig. 7-11. (a) A simple block diagram of the complete interface including three-signal auto-calibration; (b) the interface output signal.

The interface was designed and implemented in 0.7 μm standard CMOS technology. Figure 7-12 shows the chip photograph.

The different periods of the output signal can be read with a micro-controller. For identification purposes, the time interval T_{off} is split into two short periods [4]. Data can be read via a serial port (RS232) and analyzed, for instance, with a Labview program.

The interface consumes 0.7 mA up to 1.4 mA for a power supply voltage that can vary from 3.5 V to 5.5 V. The change of the supply voltage from 3.5 V to 5.5 V causes a relative error that is less than 10^{-4}.

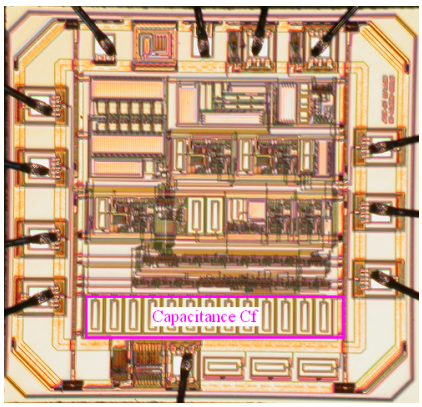


Fig. 7-12. A photograph of the chip, which measures 1.7 mm × 1.7 mm.

As an example, figure 7-13 shows the measurement result for C_x=220 pF, C_{off} =0 pF and C_{ref} =330 pF (the default reference value). The total measurement time is about 30 ms. The standard deviation of the measured capacitor C_x is σ = 11 fF, which corresponds to a more than 14-bit resolution. Since we optimized the interface for a capacitive sensor up to 500 pF, while using a value that was not too large for the integrated capacitor C_f (Fig. 7-1(a)), our driving voltage was limited to 0.25 V. A higher resolution can be achieved by increasing the

driving voltage; however, in this case we also need the larger feedback capacitor C_f (Fig. 7-1(a)). Moreover we should emphasize that this interface is not optimized for noise.

With the method presented in [5 and 6], the nonlinearity of the interface was measured for the 100 pF to 400 pF range. The measured non-linearity appeared to be less than 2×10^{-4}.

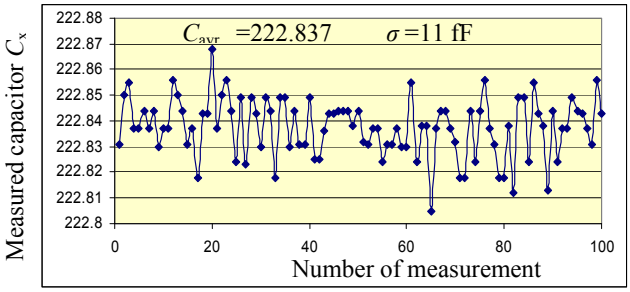
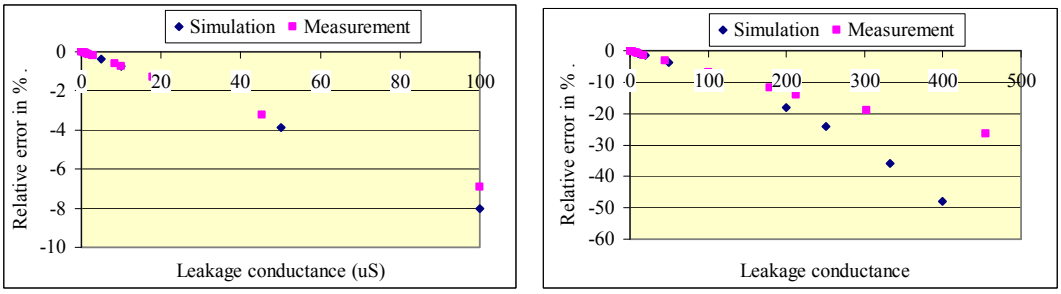


Fig.7-13. Measurement result for a capacitor with a nominal value of 220 pF and a measurement time of 30 ms.

Figure 7-14 shows the simulated and measured result of the relative error $(C_x - C_{x0})/C_{x0}$ versus the leakage conductance, for C_x=100 pF. In principle, C_{x0} should be the measured capacitor for $R_x = \infty$. However, for practical reasons, we made another choice: In our tests the leakage was hardware-simulated with an external resistor. It appears that these resistors have a parasitic capacitor in the order of 0.15 pF. This value is almost independent of the resistor value. Therefore, to mimic this capacitor, during the measurement of C_{x0}, instead of $R_x \rightarrow \infty$, a physical resistance R_x= 10 MΩ was used.



(a) (b)

Fig.7-14. The relative error for C_x=100 pF versus the shunting conductance; (a) up to 100μS and (b) up to 500μS.

As we can see from Figure 7-14, up to 100 μS the simulated and measured errors correspond closely to each other.

The measured result shows that for a capacitance of 100 pF, the presence of a leakage conductance of 100 μS causes a relative error of about 7%. For a leakage conductance larger than 200 μS, the simulation shows an error which is much larger than the measured error. Up to now, we have not found an explanation for the disagreement. However, researching the interfaces for sensors with such a large leakage is beyond the scope of this thesis.

In many applications, the electronic circuitry is connected to the sensor via a long shielded cable. Therefore, it is important that the interface can measure sensor capacitance with enough immunity for the effects of the large parasitic capacitance C_p. Figure 7-15 shows the absolute error ΔC_x in measuring a capacitance with a nominal value of 220 pF versus the parasitic capacitance C_p. Note that with a parasitic capacitance up to 470 pF the error is negligible.

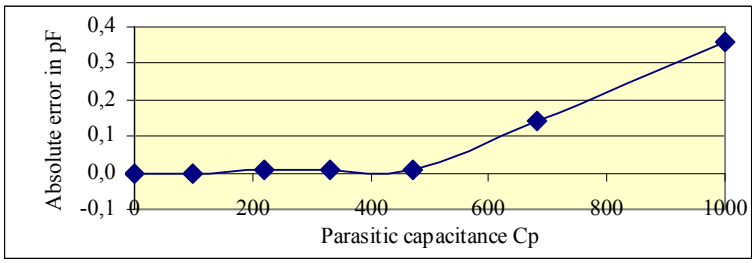


Fig.7-15. The absolute error ΔC_x of a measured capacitance with a nominal value of 220 pF versus the parasitic capacitances C_p.

Additionally, in two different experiments we measured the effect of the interface temperature. In the first experiment, we kept C_x at a constant temperature, while the temperature of the interface including the reference capacitor C_{ref} was varied in the range of -20 ºC to 130ºC. Figure 7-16 shows the measurement results for C_{ref} = 330 pF and C_x = 220 pF (nominal values). Both capacitors are of the type NP0. The offset capacitor C_{off} was about 0 pF. The measurement results for this first experiment are labelled "NP0 type C_{ref}".

In the second experiment, only the interface temperature was changed, while the temperature of the reference capacitor was kept at a constant value. The results of this experiment are labelled as "Ideal C_{ref}". As compared to the first experiment, the error in the second experiment is significantly reduced. Obviously, the drift of about 38 ppm/K measured in the first experiment is due to the temperature drift of the reference capacitor C_{ref}. According to the specifications, the drift of NPO capacitors should be smaller than 50 ppm/K.

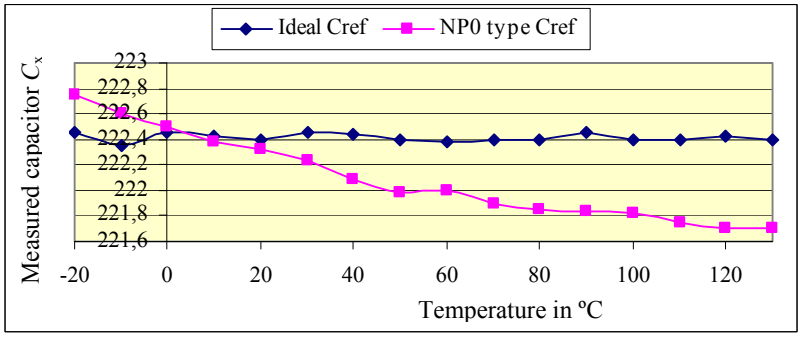


Fig.7-16. The absolute error ΔC_x of a measured capacitance with a nominal value of 220 pF versus the interface temperature for two conditions for the reference capacitor; (a) the temperature of the reference capacitor and the interface are equal and (b) the reference temperature is constant.

7-5 Conclusion

An integrated interface for leaky capacitive sensors has been presented. The major non-idealities of the front-end have been identified and discussed. A complete interface circuit has been designed and implemented in 0.7 µm standard CMOS technology. Even with a drive signal of only 0.25 V, a resolution of 14 bits is achieved for a measurement time of 30 ms. The measured non-linearity is less than 2×10^{-4} for the range of 0pF to 330pF. Measurement results, which are in close agreement with simulation results, show that for a capacitance of 100 pF, a shunt conductance as large as 100 µS will cause a relative error of less than 7%. The interface temperature hardly affects the measurement results.

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CHAPTER 8

An Integrated Interface for Grounded Capacitive Sensors

8-1 Introduction

Often, capacitive sensor elements are connected to the electronic interface circuitry with long wires consisting of cables. To reduce the effects of interference, these connecting wires or cables are shielded. Provisions have to be taken to prevent the parasitic capacitances of these cables from forming direct shunting components for the sensing elements, because without such provisions any changes in these parasitic capacitances would seriously degrade the sensor-system performance.

When the capacitive sensor elements are floating, i.e. when none of the terminals have been connected to ground, then they can be read by interface circuits that are intrinsically immune to stray capacitances [1]. Also it is possible to perform two-step measurements in order to extract the value of a floating capacitance separately from the parasitic capacitance [2]. However, safety reasons and/or operating limitations might require one of the electrodes of the sensing elements to be grounded. This is the case, for instance, with:

1. Level measurements of a conductive liquid in a grounded metallic container with a capacitive sensor [3, 4], where either the grounded tank wall or the conductive liquid is the second electrode.
2. Displacement measurements with single-electrode capacitive sensors (chapter 2, section 2-2-1). The second electrode is the chassis of the machine which is grounded.

For grounded capacitive sensors a typical way of reducing the effects of shunting parasitic capacitances is to apply active shielding (Fig. 8-1) [1]. In figure 8-1, C_{p1} and C_{p2} represent the capacitance between the core conductors of the coaxial cable with its shield and the capacitance of the shield to the ground, respectively.

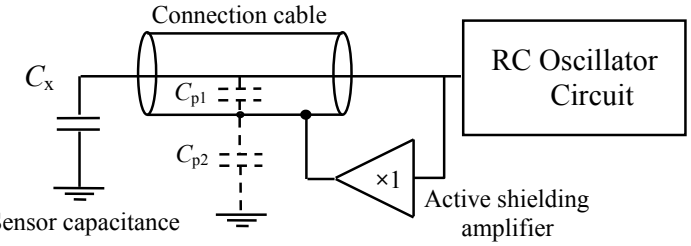


Fig. 8-1. Typical read-out interface for a grounded capacitive sensor.

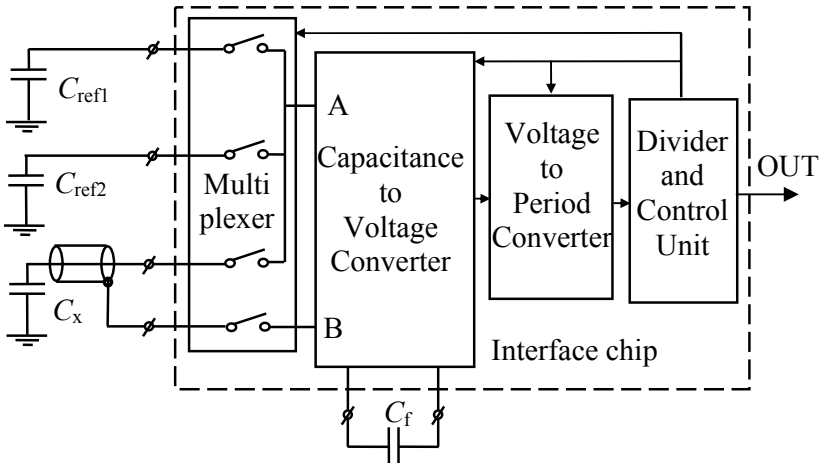
There is a trade off between the accuracy and the stability of this system. Especially if the values of parasitic capacitances are not known or if they vary over a wide range, it is difficult to optimize the system performance [5]. To solve this problem, in a recent publication [6], a novel interface is introduced in which active shields are connected to a buffer voltage while using *feedforward* instead of *feedback*. It has been shown that there are no instability problems with this technique and there is more design freedom to increase the accuracy.

However, the circuit described in [6] is implemented with discrete components, and the capacitive sensing elements are directly connected to a capacitance-to-time converter. In this

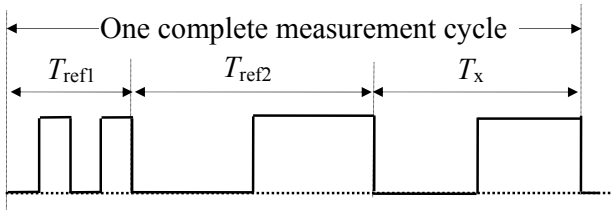
work, we show that the use of a capacitance-to-voltage converter as a front-end significantly improves the system performance. In addition to this thesis, the results of this work have also been published in [7]. The main non-idealities of the interface system are discussed together with methods to reduce their influence. An integrated version of the improved interface for grounded capacitive sensors with feed-forward-based active shielding is presented. In order to reduce the effect of any low-frequency disturbing signals, including flicker noise, interference from the mains, and offset, the interface is equipped with a special kind of chopper, according to the (+ - - +) principle described in [8, 9] and also chapter 4. Moreover, to remove any additive and multiplicative errors, which are mainly caused by uncertainty in design parameters and thermal drift, a three-signal auto-calibration technique (chapter 3) is used. The interface was designed and implemented in 0.7 μm standard CMOS technology. The experimental results are presented in section 8-4. As compared to previous work [6], these results demonstrate both a significant improvement in the immunity for parasitic capacitances, and a higher flexibility in adapting the front-end to the maximum value of the sensor capacitances.

8-2 System setup and front-end circuit

Figure 8-2(a) shows an overview of the complete setup, which consists of a multiplexer, the new capacitance-to-voltage converter, a voltage-to-period converter [6, 7, 8, 9], and a control unit. The output signal is shown in figure 8-2(b). Each measurement cycle consists of three phases, in which a first reference capacitor $C_{ref1,}$ a second reference capacitor C_{ref2}, and the sensor capacitor C_x are measured, respectively. Their values are linearly converted to the time domain and result in corresponding time periods T_{ref1}, T_{ref2} and T_x of the output signal.



(a)



(b)

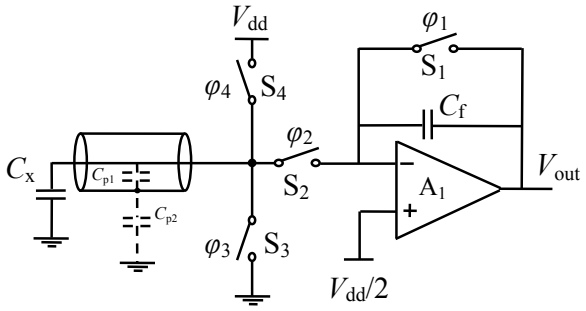
Fig. 8-2. (a) The complete interface including three-signal auto-calibration, and (b) the interface output signal.

To obtain good resolution, the difference (C_{ref2} - C_{ref1}) between the values of the reference capacitors should be large enough. On the other hand, as will be explained in section 8-3-3, the values of C_{ref1} and C_{ref2} should be chosen in such a way that the interface circuit will work in its linear region.

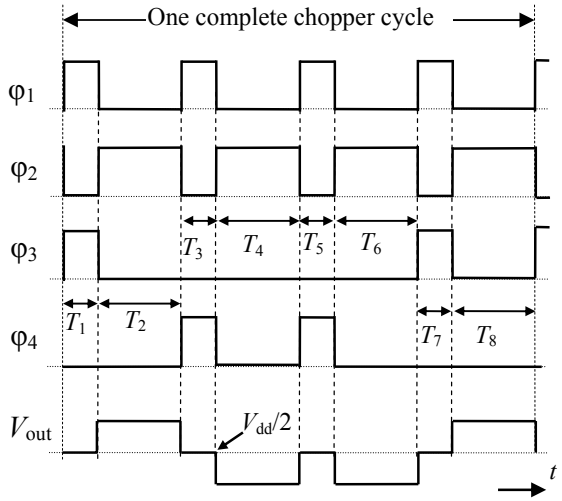
Figure 8-3(a) shows the capacitor-to-voltage converter for the case that the sensor capacitor C_x is selected. The related signals are shown in figure 8-3(b). The switch pairs, (S_1, S_2), (S_2, S_4) and (S_2, S_3) all work in a break-before-make mode. This guarantees that no charge is lost at the negative input of the amplifier. To understand how this SC-circuit works, we first suppose that cable capacitances C_{p1} and C_{p2} are zero and that the amplifier A_1 and the switches are ideal.

During time interval T_1 (Fig. 8-3(b)), S_2 is OFF and S_1 is ON. Therefore V_{out} is set to V_{dd} /2. At the same time, the top electrode of the sensor capacitance C_x is connected to ground via S_3. During time interval T_2, C_x is connected to the negative input of the amplifier. As a consequence, a charge $C_xV_{dd}/2$ will be pumped into C_f, which results in a jump $C_xV_{dd}/(2C_f)$ of the output voltage V_{out}. Similarly, the value of V_{out} can be found for the other time intervals, as depicted in figure 8-3(b).

In the setup in figure 8-3(a), the excitation voltage for the capacitor C_x has one of three well-known values: 0 V, V_{dd}, and $V_{dd}/2$. By knowing this in advance, without using feedback, we can apply the same voltage to the shielding conductor. In this way, the effect of cable parasitic capacitances can be eliminated without any instability problems.



(a)



(b)

Fig. 8-3. (a) The new front-end for a grounded capacitive sensor, and (b) the switch-control signals and the output voltage.

In our design, we need to cover sensor capacitances up to 330 pF. In such a case C_f is too large to be integrated. Therefore, for capacitor C_f we use an off-chip component. The value of this capacitor can be optimized to obtain the maximum output swing of the amplifier for the maximum value of C_x. Next, in the following stage, the voltage-to-period converter can be optimized separately from the sensor-capacitance range. This also allows the end-user to optimize the system performance for a specific application.

8-3 Effects of component imperfections

The major non-idealities to be considered are amplifier offset, switch-charge injection, and switch ON resistances. In this section the influence of these non-idealities will be discussed.

8-3-1 The Offset

Figure 8-4(a) shows the front-end circuit for the case that the sensor-cable shield (point B) is driven with the same voltage as the cable core (point A). When we suppose that the switches and the voltage source are ideal, then C_{p2} does not play a role.

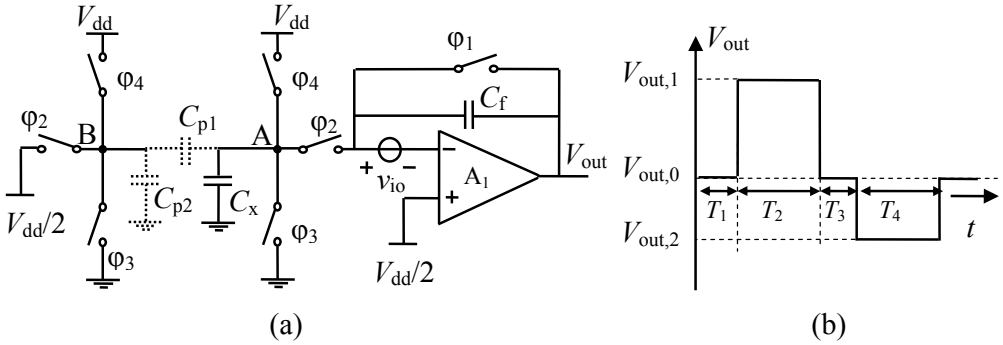


Fig. 8-4. (a) New front-end with shield driver and (b) output voltage in the presence of offset.

The main objective of active shielding is to keep the voltage across C_{p1} at zero, but if φ_2 is high, the voltage across C_{p1} equals the input offset voltage v_{io} of the amplifier. The effect of this offset voltage is eliminated by the applied chopper, as will be shown now:

During time interval T_1 (Fig. 8-4(b)), V_{out} is set to $V_{out,0} = V_{dd}/2 + v_{io}$. At the same time, the top electrode of the sensor and the shield are connected to ground. During time interval T_2, a charge q_1, which equals:

$$q_1 = C_x V_{dd}/2 + \left(C_x + C_{p1}\right) v_{io}, \tag{8-1}$$

is pumped into C_f. This results in an output voltage $V_{out,1}$ which equals:

$$V_{out,1} = V_{out,0} + \frac{C_x V_{dd}/2 + \left(C_x + C_{p1}\right) v_{io}}{C_f}. \tag{8-2}$$

In a similar way we will have:

$$V_{out,2} = V_{out,0} + \frac{-C_x V_{dd}/2 + \left(C_x + C_{p1}\right) v_{io}}{C_f}. \tag{8-3}$$

As we can see, due to the offset, the output voltage is not symmetrical with respect to the level of $V_{out,0}$. However, the next stage, which is a voltage-to-period converter [8, 9], is designed to be sensitive to the peak-to-peak voltage $V_{p\text{-}p}$ only, where it holds that:

$$V_{p\text{-}p} = (V_{out,1} - V_{out,2}) = \frac{C_x V_{dd}}{C_f}. \tag{8-4}$$

This voltage is independent of offset.

8-3-2 Switch ON resistance R_{on}

Figure 8-5 shows the circuit of figure 8-4 at the beginning of time interval T_4. At the beginning of time interval T_4 the capacitor C_x, which at the time interval T_3 , is charged to V_{dd}, while $t = 0^+$ is going to transfer its charge into C_f. After settling, points A and B have almost the same potential (for the moment the offset voltage and the input voltage of the amplifier are considered to be zero), so that the final charge of the parasitic capacitance C_{p1} will be zero. Thus, after the transient time, all the extra charge $C_x V_{dd}/2$ of C_x, is transferred to C_f.

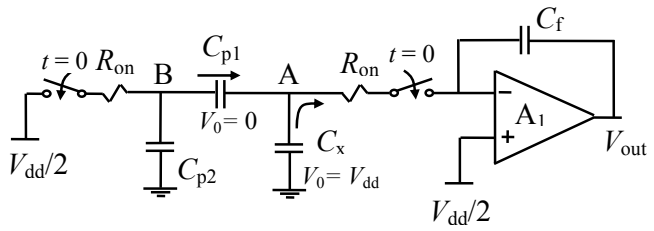


Fig. 8-5. The relevant part of the interface to analyze the charge-transfer process.

The range of the different capacitors in this circuit and the switch size determine the charge-transfer speed, while also determining the accuracy of this transfer in combination with the available time. When we use shielded cable, the safety ground could be used as a return path. However, in that case the current loop is too large and undefined, and therefore susceptible to interference. It is better to use an additional wire to connect the ground of the capacitive sensor to the interface circuit. This is implemented with a special ground electrode near the sensor electrode and connecting this electrode via wire to the interface ground. The best option is to use triaxial cable instead of simple shielded cable. In that case, C_{p2} can be in the same range as C_{p1} (100 pF/m) or even larger. Usually in a low-cost system, a single wire twisted to the shielded cable can be used for the ground connection. In this case, C_{p2} is not well defined.

In our setup, using a coaxial cable with a surrounding twisted wire as ground, the measured value for C_{p2} is found to be about 35pF/m. To understand the influence of the parasitic capacitances, we assume that the cable length l = 40 m, so that C_{p1} = 4 nF and $C_{p2} \approx$ 1.4 nF. Furthermore, we suppose that the sensor capacitance C_x ranges from 10 pF to 330 pF and that the switches are identical. In this case, the voltage transition at node B occurs at a slower pace than that at node A. This means that C_{p1} initially pumps some charge into C_f in the same direction as C_x. Next, this undesired charge is removed with a time constant of about $\tau \approx 2R_{on}C_{p1}$. Figure 8-6 shows the simulation result for the case that C_{p1} = 4 nF, C_{p2} = 1.4 nF, C_f = 1 nF, and C_x = 100 pF. If we suppose that this undesired charge is k times larger than the desired charge $V_{dd}\, C_x$ / 2, then the output voltage during time interval T_4 can be written as:

$$V_{\text{out}}(t) = \frac{V_{\text{DD}}}{2}\left(1 - \frac{C_{\text{x}}}{C_{\text{f}}}\left(1 + k\text{e}^{-t/\tau}\right)\right). \tag{8-5}$$

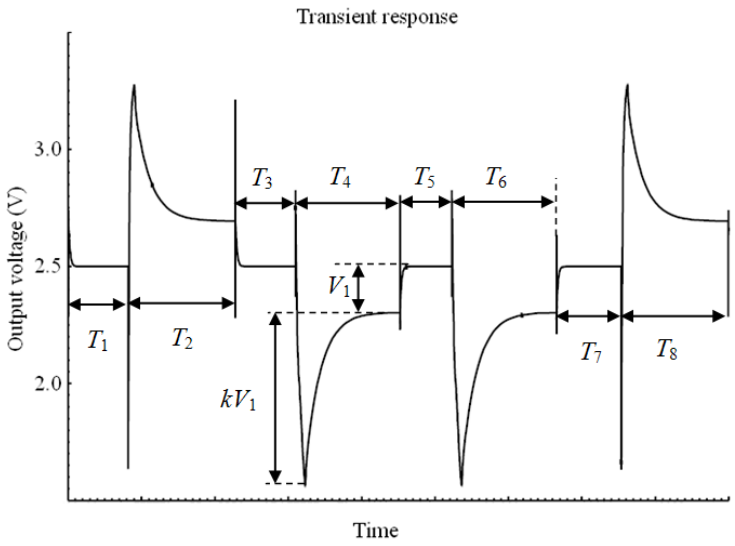


Fig. 8-6. The transient simulation of the front-end circuit of Fig. 8-5 for C_{p1} = 4 nF, C_{p2} = 1.4 nF, C_{f} = 1 nF and C_{x} = 100 pF.

Therefore, the absolute error ΔV_{out} at the end of a time interval T_{a} amounts to:

$$\Delta V_{\text{out}} = k\frac{V_{\text{DD}}C_{\text{x}}}{2C_{\text{f}}}\text{e}^{-T_a/\tau}, \tag{8-6}$$

where $T_{\text{a}} = T_2 = T_4 = T_6 = T_8$ is the available time for charge transfer (Fig. 8-6).

Translating this error to capacitance read-out error results in:

$$\varepsilon_{\text{C.T.}} = kC_{\text{x}}\text{e}^{-T_a/\tau} \tag{8-7}$$

At first look, it might seem that by increasing the sensor capacitance C_{x}, this error will increase also. However, in the assumed range of C_{x} the amount of undesired charge is almost independent from C_{x} from 10 pF to 330 pF. As a consequence, the value of k is almost proportional to $1/C_{\text{x}}$. For instance, for C_{p1} = 4 nF, C_{p2} = 1.4 nF and C_{x} =10 pF, 50 pF and 100 pF, it is found (by simulation) that k = 47, 10 and 4.3, respectively. Therefore, the product of kC_{x} for the three capacitors are 470 pF, 500 pF and 430 pF, respectively. Therefore, in equation 8-7, the sensitivities for the parameters k and C_{x} are compensating each other for the most part. Finally, since T_{a} increases with increasing C_{x} [8], this error should decrease with increasing C_{x}. This appears to be in agreement with the measurement result presented in section 8-4.

In the interface circuit, we added the option of increasing T_{a} by a factor of 2 by decreasing the integrator current I_{int} in the voltage-to-period converter (chapter 3, section 3-4-3). This option can be set with a digital input pin. For the same error, when increasing the available time by a factor of 2, the chip can handle a cable twice the length. As an alternative, instead of increasing the available time T_{a}, we can also decrease the time constant τ by increasing the switch size by the same factor.

8-3-3 Switch-charge injection

In order to drive a parasitic cable capacitance of, for instance, 4 nF with a short settling time, we need quite large switches. Consequently, the switch-charge injection, which includes channel-charge injection and clock feed-through, [10], can be significant. Figure 8-7 shows the relevant part of the interface for analysing this effect.

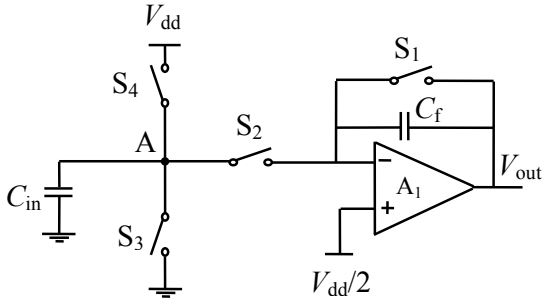


Fig. 8-7. The relevant part of the CVC to analyze the charge injection effect.

The charge injection of S_2 will not induce any error in the output voltage, because after it turns off, S_1 turns on and C_{in} is connected to a well-defined potential. The error induced by the charge injection of S_1 in the output voltage is always in one direction and is similar to that of the offset voltage. This effect is removed by the applied chopper. However, the charge-induced errors caused by S_3 and S_4 add up and are significant. For the three time periods T_{ref1}, T_{ref2} and T_x of the output signal, these errors are almost equal. Therefore, for the main part, these errors will be removed by applying the three-signal auto-calibration technique. However, since the C_{in}-values (Fig. 8-7) are different for the three different phases of the measurements, the injected charges show slight differences [10] so that after three-signal auto-calibration some residual error remains. The largest error is found for the smallest value of C_{in}.

We simulated the effect of switch-charge injection for the complete interface with C_{ref2} = 330 pF and 20 pF ≤ C_x ≤ 330 pF for two values of C_{ref1}, of 0 pF and 10 pF, respectively. In order to analyse this effect separately from the error related to incomplete charge transfer, we used $C_{p1} = C_{p2} = 0$ pF. It can be proven, that the parasitic capacitances C_{p1} and C_{p2} do not affect the switch-charge injection. Figure 8-8 shows the absolute error ($C_{x,cal.} - C_x$) caused by charge-injection versus C_x. In this figure, $C_{x,cal.}$ represents the calculated value of $C_{x,cal}$, which is found from the equation [9]:

$$C_{x,cal} = \left(\frac{T_x - T_{ref1}}{T_{ref2} - T_{ref1}} \right) \left(C_{ref2} - C_{ref1} \right) + C_{ref1} \ . \qquad (8\text{-}8)$$

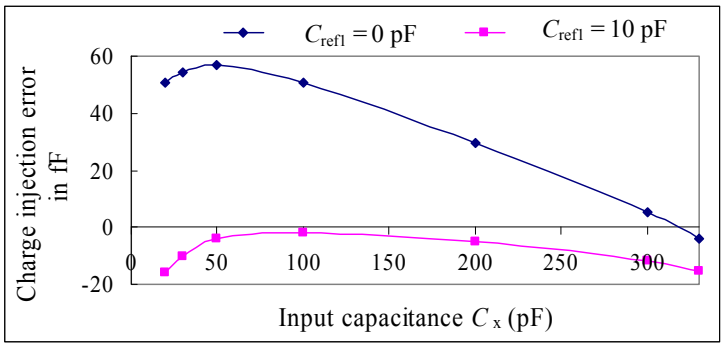


Fig. 8-8. Simulated charge-injection-related error, ($C_{x,cal.}$- C_x) versus C_x, for C_{ref2} =330 pF, C_{ref1} = 0 pF, and 10 pF, respectively.

From this figure it can be seen that the residual error due to switch-charge injection can be reduced significantly by increasing C_{ref1} to, for instance, 10 pF. In the next section it will be shown that for a long cable, even with C_{ref1} = 0 pF, the error due to incomplete settling of the circuit is much larger than that caused by switch-charge injection. Therefore, for a long cable, we can simply select C_{ref1} = 0 pF without introducing a significant error. However, for a short cable, depending on the target accuracy, it is advisable to select C_{ref1} = 10 pF.

8-4 Implementation and measurement results

The interface was designed and realised in 0.7 µm standard CMOS technology. Figure 8-9 shows a photograph of the chip. The supply voltage is 5 V and the measured value for the supply current is about 0.7 mA. This current depends slightly on C_{p2} and will increase to 0.8 mA for C_{p2} = 3.3 nF. Similar to UTI [11], this interface also has two different measurement speeds: slow and fast mode, which differ by a factor of 8. This can be implemented simply by a programmable divider. Also as explained in section 8-3-2, the chip has the option to select two different frequencies which differ by a factor of two. Altogether the interface can have 4 different measurement times, which including auto-calibration are about 5 ms, 10 ms, 40 ms and 80 ms.

In order to see the effect of incomplete settling, we measured different capacitors from 10 pF to 330 pF for a higher oscillator frequency. These measurements were performed for two cases: a) with the emulation of 30 m of coaxial cable with twisted ground wire by using equivalent discrete capacitors C_{p1} = 3 nF and C_{p2} =1 nF, and b) with a real cable 30 m in length with twisted ground wire. The absolute error of these measurements along with the simulation results for C_{p1} = 3 nF and C_{p2} =1 nF are shown in figure 8-10. It can be concluded that the simulation results and the experimental emulation results are in close agreement. For a real cable, the error is slightly larger. Our investigations showed that this increased error was caused by leakage from the cable shield to the grounded conductor.

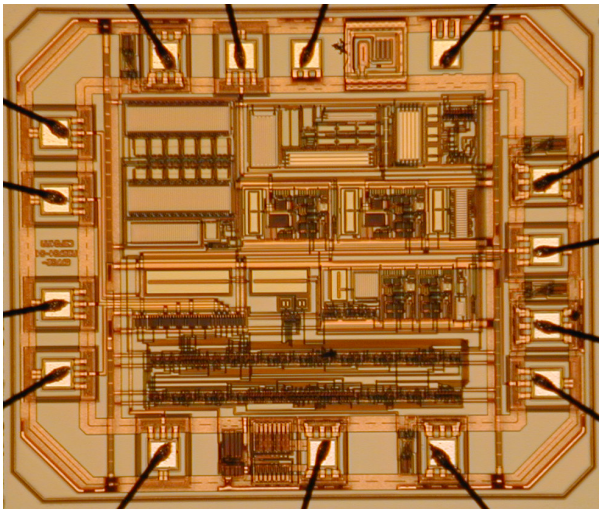


Fig. 8-9. Photograph of the chip, which measures 1.4 mm × 1.7 mm.

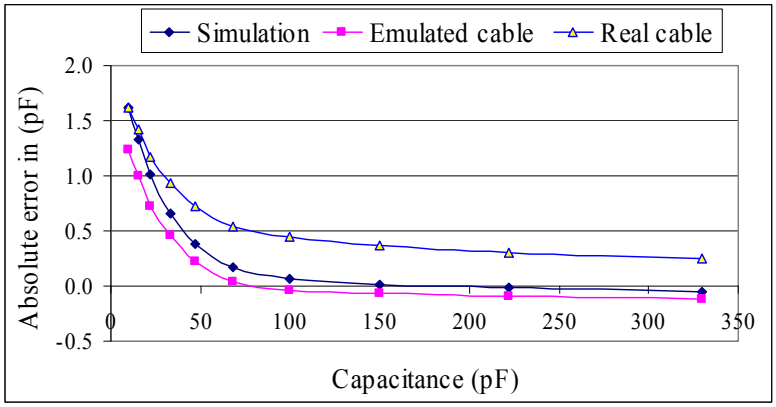


Fig. 8-10. Simulated and measured absolute errors versus the input capacitance for 30 m of cable. The easurement results were obtained with real cable, or with emulation using the equivalent capacitances C_{p1} = 3 nF and C_{p2} =1 nF, respectively.

Figure 8-11 shows a comparison of the measured errors versus the input capacitance for the two frequencies (section 8-3-2) and for a real cable 30 m in length. In the higher frequency mode, the main source of error is due to incomplete charge transfer.

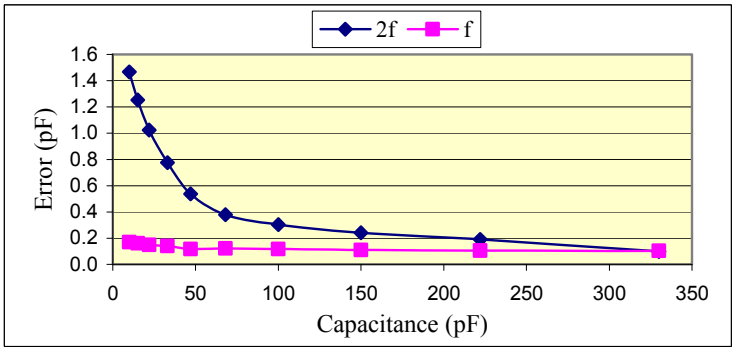


Fig. 8-11. Comparison of the measured absolute error versus C_x in two frequencies for 30 m of cable with a twisted ground wire.

Figure 8-12 shows the measured absolute error versus the input capacitance C_x in the lower frequency mode for four different lengths of cable up to 40 m. From figure 8-12 it is easy to compare the results of the interface system presented in this work with those of previous work [6]. According to this figure, for a sensor capacitance of 27 pF and a cable length of 30 m, the absolute error is about 0.25 pF. With comparable parameters, the system presented in [6] shows an error of more than 26 pF.

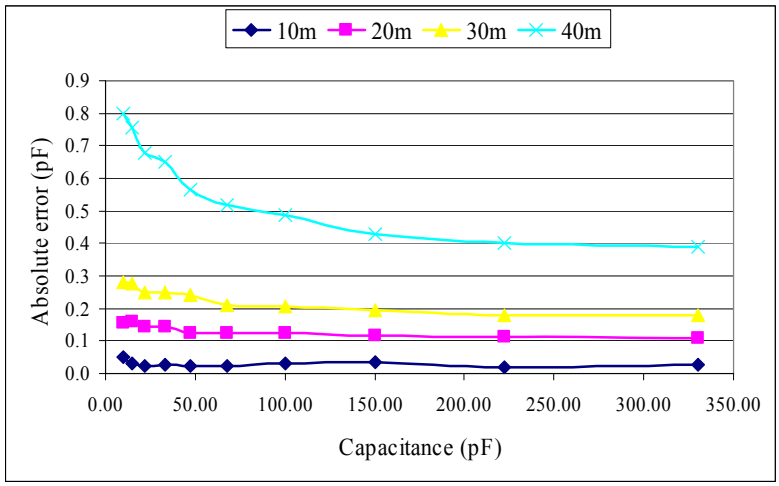


Fig. 8-12. Measured absolute error versus C_x for different lengths of cable with twisted ground wire for lower frequency mode.

Regarding the noise performance, the experimental results show that even for large values of the parasitic capacitances C_{p1} and C_{p2} (Fig. 8-4) these capacitances hardly affect the standard deviation. Therefore the noise performance is dominated by that of the voltage-to-period converter (Fig. 8-2), because otherwise, with increasing C_{p1}, the output noise should increase due to the increased noise gain of amplifier A_1 (Fig. 8-4(a)) [12]. As it is explained in chapter 4 section 4-6-2-1, the flicker noise corner frequency of integrator current source f_c should be smaller than $1/T_{3\text{-sig}}$ for all different conditions. As mentioned, the interface can have 4 different measurement times which including auto-calibration are about 5 ms, 10 ms, 40 ms and 80 ms. It means that flicker noise corner frequency of integrator current source should be lower than 12 Hz. However, the flicker noise corner frequency of the integrator current source in this design is about 500 Hz. Based on the analysis on chapter 4 section 4-6-2-1, we found that the noise of interface is dominated by noise in the integrator current source. This problem was solved, the results of which were already presented in chapter 5.

Figure 8-13 shows the experimental results for 100 measurements for a capacitance with a nominal value of 330 pF and a measurement time of 40 ms, including three-signal auto-calibration. The measured standard deviation amounts to 6.2 fF, which corresponds to about 16 bits of resolution. The result is about one bit better than that reported in [6] for comparable conditions.

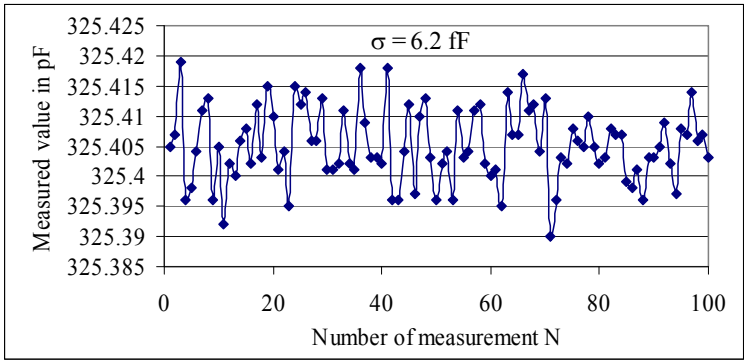


Fig. 8-13. Measured value for a capacitor with a nominal value of 330 pF for a measurement time of 40 ms.

We also measured the nonlinearity according to the method presented in [13]. In order to be independent from the absolute-component accuracy, four different measurements were performed for C_{ref1}, C_{ref2}, $C_{ref1}+C_{ref3}$, and $C_{ref2}+C_{ref3}$, respectively. Supposing linear capacitance-to-time conversion ($T_i = aC_i + b$), independent from the capacitance value, the value of the nonlinearity λ is found with the equation:

$$\lambda = \frac{T_{Cref2+Cref3} - T_{Cref1+Cref3}}{T_{Cref2} - T_{Cref1}} - 1. \qquad (8\text{-}9)$$

The measurement of this nonlinearity should be performed in such a way that the parasitic capacitance (parasitic capacitances of the PCB) during the four measurements remain constant. This means that not only the wiring of the setup, but also its surrounding, should not be changed [14]. In order to implement this, one common side of all three capacitors is connected to the interface, while the other side of these capacitors is connected to ground or to the guard-drive voltage source.

In our nonlinearity tests, we selected different combinations of C_{ref1}, C_{ref2} and C_{ref3} in such a way that, C_{ref1}, C_{ref2}, $C_{ref1}+C_{ref3}$ and $C_{ref2}+C_{ref3}$ are within the range of 10 pF to 330pF, which resulted in a maximum measured nonlinearity of 3×10^{-4}.

8-5 Conclusion

An integrated version of a switched-capacitor interface for grounded capacitive sensors with feed-forward-based active shielding has been analyzed. The main non-idealities of the interface were discussed. A complete interface design was implemented in 0.7 μm standard CMOS technology. The experimental results show good agreement with simulation results. It was shown that if we give the circuit enough time to settle, long connection cable lengths can be afforded. Our measurements show that even with 30 m of connection cable, a capacitance as small as 10 pF can be measured with an error of less than 0.3 pF. For this length of cable, the measured nonlinearity is less than 3×10^{-4} for the range of C_x-values from 10 pF to 330 pF. With a measurement time of 40 ms, a resolution of almost 16 bits was achieved.

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ORIGINAL CONTRIBUTION

The main original contribution of this work can be found in chapters 4 to 8 and concern the following items:

Chapters 4 to 5:

1. A proposal for a universal interface chip that can be used for a wide range op applications without significant sacrificing of performance. The described design has the following unique options:
    a) In a flexible way the ranges of the input capacitance can be set with a single off-chip capacitor.
    b) The oscillator frequency can be adjusted to maximize the speed for a specified settling error.
    c) The measurement speed can be selected out of four modes ranging from about 100 μs up to about 50 ms.
2. In Chapter 4 an improved and complete noise analysis of the system has been presented. Based on the results of this analysis the interface system has been redesigned for optimum noise and speed performance. As compared to systems with the same power consumption and the same overall structure, this yielded an increase of the system resolution with three bits and the possibility to implement very fast measurements.
3. A thorough analysis of the nonlinearity of the interface. Application of the results of this analysis enabled the design of an interface system with two bits higher linearity, as described in chapter 5 and 6.
4. Development of a method for measuring small nonlinearities, in the range of some tens of ppm.
5. The design of an integrated version of the interface circuit.

Chapter 6

In the design presented in chapter 6 we use negative feedback to control the charge-transfer speed. The original contributions in this design concern:

6. An analysis of the effect of this approach for the system nonlinearity.
7. Discovery of specific conditions to be satisfied for proper operation.
8. Analysis of the effect of negative feedback on the noise performance of the interface.
9. The design of an integrated version of the interface circuit

Chapter 7

In chapter 7 we introduce an interface for leaky capacitive sensor. The main original contribution concerns:

10. A thorough analysis of leakage-related errors

11. The design of an integrated version of the interface circuit

Chapter 8

In chapter 8 an interface for grounded capacitive sensors with an active guarding is presented, the original contributions are:

12. A complete analysis of errors caused by parasitic cable capacitances.
13. The design of an integrated version of the interface circuit

APPENDIX A

Terminology

A-1 Error and uncertainty

No matter what precautions are taken, there will always be a difference between the result of a measurement and the true value of a quantity. The difference is called the *measurement error*. If we knew the true value, there would be no reason to make the measurement! A measurement is useless without a quantitative indication of the magnitude of that error [1].

In fact, the reduction—not necessarily the elimination—of uncertainty is central to the concept of measurements. Measurement errors are often assumed to be normally distributed around the true value of the measured quantity. Under this assumption, every measurement has three components: the estimate, the error bound, and the probability that the actual magnitude lies within the error bound of the estimate.

A-2 Error sources

Errors can be divided into two categories, systematic errors and random errors, which are both explained in more detail in this section.

A-2-1 Systematic errors

A systematic error can be caused by a biasing effect in the environment, the method of observation, or the instrument used which introduces error into an experiment such that it always affects the results of an experiment in the same direction. Such errors cannot be removed by repeating measurements or averaging large numbers of results. A common means to remove systematic errors is the observation of a known process, i.e. through calibration. Another means to remove systematic error is by a subsequent measurement with more sophisticated equipment. Some sources of the systematic error are listed below.

A-2-1-1 Loading errors

A loading error occurs when the interaction between the physical process and the sensor is not compensated. A well-known example is the measurement of the potential difference over a resistor by means of a voltmeter.

A-2-1-2 Calibration errors[1]

Calibration errors are induced by:

- The uncertainty of reference values.

[1] Calibration is the act of checking or adjusting (by comparison with a standard) the accuracy of a measuring instrument. By calibration we try to compensate the measurement system for systematic errors.

- Random errors that occur during calibration.
- Erroneous calibration curve.

Errors in the two-point calibration procedure, lead to both a multiplicative and an additive error. The wrong calibration curve occurs when a two-point calibration procedure is used that is based on a linear model of the sensor, whereas in reality the sensor is non-linear. Under certain conditions, this error can be reduced by using a nonlinear calibration curve, and to fit that curve using multiple-point calibration.

A-2-1-3 Dynamic errors

Dynamic errors occur when the measurement instrument is two slow to be able to track a (fast-changing) measurand. Another dynamic error occurs when the bandwidth of the instrument is not sufficient. The measuring device should have an amplitude transfer that is constant over the bandwidth of the measurand.

A-2-2 Random errors

A random error is an error that can be reduced by averaging the results of repeated measurements. The sources of random error are:

A-2-2-1 Environmental errors

External influences, such as the occurrence of Electro-Magnetic Interference (EMI), may cause errors that are often random.

A-2-2-2 Quantization error

The difference between the actual analog value and the quantized digital value is called quantization error. Quantization error occurs in analog-to-digital conversion. It is also called quantization noise.

A-2-2-3 Drift

The generic name for slowly-varying, random error is *drift* [1]. Possible causes for drift are: changes of temperature and humidity, unstable power supply, flicker noise, etc.

A-2-2-4 Noise

The generic name for more or less rapidly changing random error is *noise* [1]. The *thermal noise* of a resistor is caused by the random thermal motion of free electrons in conductors. The *shot noise* arises from the discrete nature of electrical charge. The *flicker noise* of surface semiconductor devices is caused by random trapping and releasing of the electric charge carrier.

Figure A-1 shows the difference between systematic and random errors.

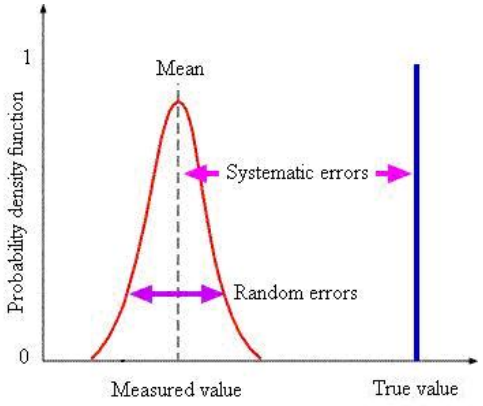

Fig. A-1. Random and systematic errors.

A-3 Specifications of measurement systems

Some of the most important specification of capacitive sensor systems are listed here.

Accuracy: The *accuracy* of a measurement is how closely the measurement result corresponds to the true value. Hence, the accuracy relates to random errors and systematic errors [1].

Precision or repeatability: *Precision* is how closely the measurement results of the same values of the same measurands correspond to each other, and which are obtained under the same conditions. Hence, precision relates to random errors and not to systematic errors [1].

Reproducibility: The *reproducibility* is how close the correspondence is between the measurement results of the same value of the same measurand that is obtained under different conditions (e.g. different instruments, different location, possibly different measurement principle, etc.) [1].

Sensitivity: The *sensitivity S* of a sensor or a measurement system is the ratio of output to input [1]. If $z = f(x)$, then the sensitivity is the differential coefficient $S = \partial f / \partial x$ evaluated at a given set point.

Dynamic range: The range of a measurement system is the interval $[x_{min}, x_{max}]$ at which it can measure the measurand within a given uncertainty σ_e. The *dynamic range D* is the ratio $D = (x_{max} - x_{min}) / \sigma_e$ [1].

Resolution: The *resolution R* expresses the ability of the measurement system to detect small increments of measurand. The resolution is defined as $R = x/\Delta x$, where Δx is the smallest increment that can be detected. Often the specification is given in term of maximum resolution $R_{max} = x_{max} / \Delta x$ [1] or in bits as $R_{max,bits}$, according to the equation:

$$R_{max,bits} = {}^2\log R_{max} = \frac{\ln R_{max}}{\ln 2}. \qquad \text{(A-1)}$$

Non-linearity error: If $z = g(x)$ (where z is the measurement result and x is the measurand), then the non-linearity error is $g(x) - (A + Bx)$, where A and B are two constants that can be defined in various ways [1]. The simplest definition is the end-point method. Here A and B are selected such that $g(x_{min}) = A + B\,x_{min}$ and $g(x_{max}) = A + B\,x_{max}$. The end point method is a special case of two-point calibration. In general, these two points can be selected anywhere. However, it is better to select them neither far beyond the range of input signal nor too close together.

Another (better) approach is to use a best-fit method. The parameters A and B are selected such that $A + Bx$ fits $g(x)$ according to a closeness criterion (e.g. a least-square-error (LSE) fitting). The nonlinearity L is the maximum non-linearity error observed over the specific range that is expressed as a percentage of the range, which is found with the equation:

$$L = \frac{\max\left|(g(x) - (A + Bx)\right|}{x_{\max} - x_{\min}}. \qquad \text{(A-2)}$$

This concept is illustrated in figure A-3. To decrease the non-linearity error, one can use a polynomial as the calibration curve, and a multiple-point calibration to fit that curve.

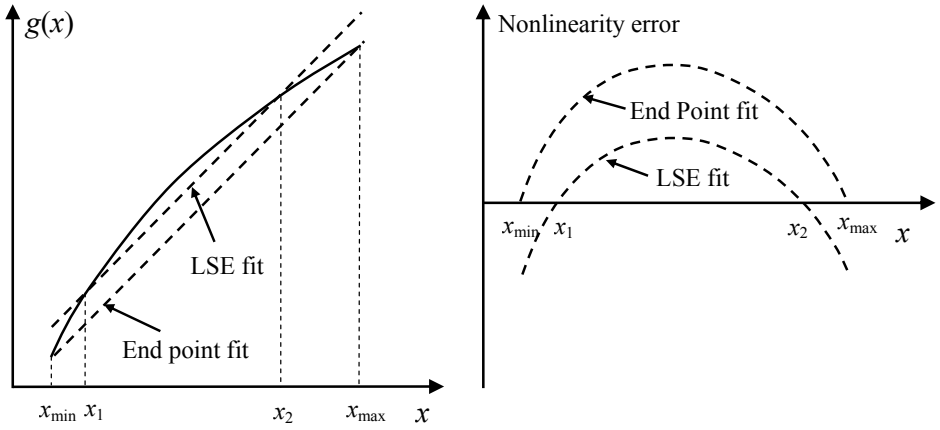

Fig. A-3. The concept of nonlinearity for two different definitions and the corresponding error.

Offset and gain error

In measurement system, $z = A + Bx$, $A = 0$ and $B = 1$ lead to an accurate result. In reality, $A \neq 0$ is called the offset error and $B - 1$ is called the gain error. The offset error is an additive error, whereas the gain error is a multiplicative error.

References

[1] P. P. L. Regtien, F. van der Heiden M. J. Korsten, and W. Olthuis, Measurement science for engineering, University of Twente, The Netherlands, Second Edition.

SUMMARY

This thesis reports the results of research on features, options and limitations of low-cost, high-performance, universal integrated interface for capacitive sensors. It concerns development-driven research, where the objectives of the research focus upon possible realization and application of the interface with optimum results at the level of multi-disciplinary systems. Moreover, the objectives of this research include maximization of the performance in relation to the cost. The interface supports different groups of capacitive sensors such as floating high-quality capacitive sensors, floating leaky capacitive sensors, and grounded capacitive sensors. The interface can be adjusted for both: different ranges of capacitances and different signal bandwidths. To check the validity of the proposed ideas and the results of the analysis, three different types of integrated circuits have been designed, fabricated and tested. These designs and test results are presented in chapter 5, 7 and 8. The material found in the various chapters can be summarized as follows:

Chapter 2 gives an introduction of capacitive sensors. The three main categories of capacitive sensor –*A* type, *D* type and ε type– are explained. In this chapter, some important existing concepts, such as those for two or three-terminal capacitors, guarding and shielding, are summarized. The concept of segmented and differential capacitive sensors and their benefit have also been discussed.

In chapter 3, two types of suited A/D converters are compared: the sigma-delta converter and the oscillator-based converter. The arguments for selecting the oscillator-based converter, such as simplicity, spread of power consumption, and compatibility with Smartec's UTI, have been discussed. Three important measurement techniques necessary to achieve a high measurement performance are briefly described in this chapter. These techniques are: auto-calibration, two-port measurement and chopping. Some important characteristics of the interface are explained as well.

In chapter 4 we first show how an interface as introduced in chapter 3 can be made flexible, so that it can be used in a wide variety of applications. Then, a detailed analysis of important interface features, such as noise, linearity, and immunity for the effects of parasitic capacitances are presented. At the end of this chapter, the challenges of characterizing and measuring very small nonlinearities are presented, together with a practical method to solve the identified problems.

Chapter 5 presents a very flexible, high-performance, universal interface design for which full advantage has been taken of the knowledge and techniques presented in the previous chapters. This interface is suitable for measuring high-quality floating capacitive sensor in various ranges up to 220 pF. The measurement time can be set from about 100 μs up to 50 ms, which corresponds to a data acquisition rate of 20 samples/s up to 10^4 samples/s. With a measurement time of 1 s, the measured resolution is as high as 20 bits, which corresponds to 1 aF in a 1 pF range. This resolution can easily compete with that of other state-of-the art designs and is at least three bit higher than the resolution of Smartec's UTI, which is available in the. Moreover, our novel interface circuit has much more flexibility with respect to the selection of the input capacitance range, parasitic-input-capacitance range, and the measurement time. Furthermore, the nonlinearity of this interface is about two bits better than Smartec's UTI. To help the user in making proper choices when optimizing the interface system for particular applications, a users guide has been included.

Chapter 6 introduces a novel interface in which the principle of negative feedback for the front-end circuit has been applied. Another difference with the design presented in chapter 5 is that the input capacitance-to-voltage converter (CVC) has been removed, so that the relaxation oscillator works as a capacitance-to-period (CPC) converter. The resulting structure is more power-efficient. In addition, since the main source of nonlinearity is found to be in the CVC, removing this converter yields a higher linearity. Furthermore, we showed that applying negative feedback can also increase the resolution. The conditions to be met for proper operation are explained and measurement results have been presented.

Chapter 7 introduces an interface with a modified CVC, which in first order is immune to the leakage of the capacitive sensing elements. Measurement results show that the error in measuring a capacitor with the value of 100 pF caused by a shunting resistor of 100 kΩ is less than 0.6 pF.

Finally, chapter 8 presents an interface for grounded capacitive sensors that are equipped with active guarding, using feedforward instead of feedback. Since there is no possibility of instability in this method, there is more freedom to optimize the immunity of interface for of the effects of parasitic cable capacitances. The measurement results show that when a connection cable with a length of 30 m is used to measure a capacitor in the range of 10 pF to 330 pF, the cable capacitance of 3 nF causes an error of less than 0.3 pF.

SAMENVATTING

Dit proefschrift beschrijft de resultaten van onderzoek naar de karakteristieke eigenschappen, opties en beperkingen van goedkope, hoog kwalitatieve, universele geïntegreerde interfaces voor capacitieve sensoren. Het betreft ontwikkelingsgestuurd onderzoek, waarbij de doelstellingen zijn gespitst op mogelijke realisatie en toepassingen van de interface met optimale eigenschappen op het niveau van multidisciplinaire systemen.

Daarnaast omvat de doelstellingen van het onderzoek een maximalisering van de prestaties in relatie tot de kosten. De interface ondersteunt verschillende groepen capacitieve sensoren, zoals "zwevende" (niet-geaarde) capacitieve precisiesensoren, zwevende capacitieve sensoren met enige resistieve lekkage, en geaarde capacitieve sensoren. Een van de doelstellingen van de interface is dat de schakeling kan worden aangepast voor zowel verschillende capaciteitsbereiken als verschillende signaalbandbreedten. Om de geldigheid van voorgestelde ideeën en gemaakte analysen te toetsen zijn er drie verschillende typen geïntegreerde schakelingen ontworpen, gefabriceerd en getest. Deze ontwerpen en de testresultaten worden besproken in de hoofdstukken 5, 7 en 8.

De inhoud van de verschillende hoofdstukken kan als volgt worden samengevat: Hoofdstuk 2 geeft een inleiding op het gebied van capacitieve sensoren. Er worden drie categorieën sensoren onderscheiden: het *A* type, het *D* type and het ε type. Tevens worden in dit hoofdstuk een aantal belangrijke bestaande concepten voor elektrodeconstructies behandeld, zoals guarding en afscherming, en het gebruik en de voordelen van gesegmenteerde en differentiële sensoren.

In hoofdstuk 3 worden twee geschikte typen A/D omzetters met elkaar vergeleken: het betreft de sigma-delta omzetter and een omzetter die gebaseerd is op het gebruik van een relaxatieoscillator. De argumenten om te kiezen voor een omzetter die gebaseerd is op een period-gemouleerde oscillator worden bespoken. Deze argumenten betreffen: eenvoud, spreiding van vermogensdissipatie en compatibiliteit met Smartec's UTI . Drie belangrijke meettechnieken die nodig zijn om een hoge nauwkeurigheid te kunnen bereiken worden in het kort beschreven. Het betreft: auto-calibratie, 2-poortmeting en chopping. Verder worden sommige belangrijke interfacekarakteristieken behandeld.

In hoofdstuk 4 wordt getoond hoe een interface conform de concepten besproken in hoofdstuk 3 flexibel kan worden gemaakt, zodat hij bruikbaar wordt voor een breed scala aan toepassingen. Vervolgens wordt een gedetailleerde analyse gegeven van de interface kenmerken, zoals ruis, lineariteit, en immuniteit voor de effecten van parasitaire capaciteiten. Aan het einde van hoofdstuk 4 wordt de moeilijkheid van het karakteriseren en meten van zeer kleine niet-lineariteiten behandeld. Praktische oplossingen voor de gevonden problemen worden besproken.

Als praktisch resultaat van wat in vorige hoofdstukken is gevonden, presenteert hoofdstuk 5 een ontwerp voor een zeer flexibele, hoog kwalitatieve, universele interface. Met deze interface kunnen zwevende precisiesensoren worden gemeten met capaciteitswaarden tot 220 pF. De meettijd kan worden ingesteld op een waarde tussen de 100 µs en 50 ms, hetgeen correspondeert met een data-acquisition rate tussen de 10^4 samples/s en 20 samples/s. Met een meettijd van 1 s, bedraagt de gemeten resolutie maar liefst 20 bits, wat correspondeert met 1 aF in een 1 pF bereik. Deze resolutie kan gemakkelijk wedijveren met die van de beste andere ontwerpen van dit moment en is tenminste 3 bits hoger dan die van Smartec's UTI.

Daarenboven heeft onze nieuwe interface een veel grotere flexibiliteit met betrekking tot de selektie van de bereiken van ingangscapaciteiten, parasitaire ingangscapaciteiten, en meettijden.

Verder is de niet-lineariteit van de interface ongeveer twee keer zo goed als die van Smartec's UTI. Teneinde de gebruiker te helpen om de geboden flexibiliteit goed te hanteren, en daarbij de juiste keuzen te maken voor een specifieke toepassing, is een gebruikershandleiding toegevoegd.

Hoofstuk 6 introduceert een nieuwe interface waarin het principe van negatieve terugkoppeling van het ingangscircuit wordt toegepast. In vergelijking met het ontwerp uit hoofdstuk 5 is er nog een tweede verschil: De ingangsomzetter (CVC), die capaciteitswaarden omzet in spanning, is verwijderd zodat de relaxatieoscillator werkt als een omzetter van capaciteit naar periode (CPC).

De hieruit voortkomende structuur valt op door zijn vermogensefficiëntie. Bovendien blijkt dat het verwijderen van de CVC een gunstig effect te hebben op de lineariteit. Tot slot laten we zien dat het toepassen van negatieve terugkoppeling de resolutie kan verhogen. Om het interfacecircuit goed te laten werken moet aan bepaalde voorwaarden worden voldaan. Deze voorwaarden worden toegelicht aan de hand van een analyse en bijbehorende meetresultaten.

Hoofdstuk 7 introduceert een interface met een gewijzigde CVC, die tot op zekere hoogte immuun is voor stroomlekkage van capacitieve sensorelementen. Meetresultaten laten zien dat een lekweerstand van 100 kΩ bij het meten van een capaciteit met een waarde van 100 pF een meetfout veroorzaakt van slechts 0.6 pF.

Het laatste hoofdstuk, hoofdstuk 8, presenteert een interface voor geaarde capacitieve sensorelementen. Deze interface is uitgerust met de mogelijkheid tot active guarding met gebruikmaking van voorwaartse koppeling in plaats van terugkoppeling. Aangezien er hierdoor geen gevaar is voor instabiliteit, is er meer ruimte om de immuniteit van de interface voor het effect van parasitaire kabelcapaciteiten te verhogen. Meetresultaten laten zien dat, zelfs bij een kabellengte van 30 m met een parasitaire capaciteit van 3 nF, capaciteiten kunnen worden gemeten in het bereik van 10 pF tot 330 pF, met een meetfout kleiner dan 0.3 pF.

LIST OF PUBLICATION

Journal Paper

1- A. Heidary and G.C.M. Meijer "Features and design constrains for an optimised SC front-end circuit for capacitive sensors with a wide dynamic range", Journal of Solid State Circuit, vol, 43. no. 7, pp. 1609-1616, July 2008.

2- A. Heidary and G.C.M. Meijer, "An integrated interface circuit with a front-end amplifier for grounded capacitive sensors", Meas. Sci. Tech., vol. 20, No 1, January 2009.

Conference proceedings

1- A. Heidary and G.C.M. Meijer "A Flexible Low-Power High Resolution Integrated Interface for Capacitive Sensors" IEEE International Symposium on Industrial Electronic, Bari, Italy, 4-7 July 2010.

2- A. Heidary and G.C.M. Meijer "Analysis and Design of an Integrated Universal Capacitive Sensor Interface" The 9th International Symposium on Measurement Technology and Intelligent Instruments, St. Petersburg, Russia, June 29-July 2, 2009.

3- A. Heidary and G.C.M. Meijer "A Time-Based Capacitance to Digital Converter with Fast Data Accusation and High Resolution" Sensor and Test, Nuremburg, Germany, May 12-15, 2009

4- A. Heidary and G.C.M. Meijer "An Integrated Interface for Leaky Capacitive Sensor with Emphasize on Humidity Sensor" I^2MTC, Vancouver, British Columbia, Canada, may 26-28, 2008.

5- A. Heidary and G.C.M. Meijer "A Low-Noise Switched-Capacitor Front-End for Capacitive Sensor" IEEE Sensor, Atlanta, Georgia, USA, October 28-31, 2007.

6- A. Heidary and G.C.M. Meijer "An Integrated Switched-Capacitor Front-End for Capacitive Sensors with a Wide Dynamic Range" ESSCIRC, Munich, Germany, September 11-13 2007.

About the author

Ali Heidary was born in Langroud, Iran in 1971. He received his B.S. degree and M.S. degree in electrical engineering from Iran University of Science and Technology and Tehran University in 1992 and 1995, respectively.

From 1995 to 2004, he was a lecturer in the department of electrical engineering, Guilan University, Rasht, Iran. In November 2004, he joined the electronic instrumentation laboratory of Delft University of Technical, The Netherlands, where he is pursuing toward PhD degree in electrical engineering. The subject of his research was to design a low-cost universal integrated interface for capacitive sensors, which resulted in this thesis.

His professional interest includes analog and mixed signal design.

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