5μW-10mW Input Power Range Inductive Boost Converter for Indoor Photovoltaic Energy Harvesting with Integrated Maximum Power Point Tracking Algorithm

Yifeng Qiu[1], Chris van Liempd[1], Bert Op het Veld[2], Peter Blanken[2] and Chris Van Hoof[3,4]

[1] imec – Holst Centre, Eindhoven, the Netherlands

[2] Philips Research Laboratories, Eindhoven, the Netherlands

[3] imec, Leuven, Belgium

[4] K.U.Leuven, ESAT-INSYS, Leuven, Belgium

Abstract – A fully autonomous inductive boost converter for indoor photovoltaic harvesting with maximum power point tracking circuit is implemented in a commercial 0.25μm CMOS process. The converter can handle input power from 5μW up to 10mW and charge a battery or a super-capacitor up to 5V. Its control circuit consumes between 0.8μA and 2.1μA depending on the input power level, resulting in a peak end-to-end efficiency of 70% when tracking a maximum input power of 17μW.

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Energy harvesting provides a means to supply wireless sensor networks in building environment with autonomous and sustainable power [1], [2]. The indoor light can be converted into electricity with a solar cell and stored in a rechargeable battery or super-capacitor [3]. Depending on the indoor illumination level and the installed location as well as the orientation of the solar cell, the output power of an amorphous silicon solar cell can vary from less than a few μW/cm² up to hundreds of μW/cm² [3]. To manage both the illumination variation and a variation in panel size, a power management circuit that is able to efficiently handle a wide range of input power is necessary.

The solar cell can be modeled as a light-controlled current source in parallel with a diode. Its output current is determined by the output voltage in an exponential relation. At one point, the solar cell reaches its maximum power point (MPP). This MPP can be tracked by tuning either the output voltage or the load impedance [4].

We developed an inductive boost converter targeting at solar cells under indoor conditions. The converter would bridge a solar cell array and an energy storage system

(ESS) which can be either a Li-ion battery or a super-capacitor. As shown in Figure 1, the converter consists of two major functional blocks, the power train and the control circuit. The power train consists of an inductor and two power switches (NMOS and PMOS). An on-chip linear regulator directly supplied by V_{BAT}, provides a voltage domain of 1V for the control circuits. The linear regulator takes its reference voltage from a nano-power reference circuit operating under this 1 V domain, as shown in Figure 1. A relaxation oscillator based on charging and discharging a capacitor, generates a clock of 100 kHz for the whole system.

The converter operates in discontinuous conduction mode (DCM) and uses pulse-skipping modulation (PSM), as illustrated in Figure 2. When operating in DCM, the inductor current I_L always decreases to zero at the end of T_{PMOS}. PSM means the converter skips an N_{skip} number of clock cycles before the next T_{NMOS} is generated. By controlling N_{skip} the average input current of the converter is changed and this influences the operation point of the solar cell, as illustrated in Figure 2. The N_{skip} is tunable as integer numbers from 1 to 511, which determines the input power range that the converter can handle. It is possible to reach the maximum power point of the source by controlling N_{skip}, which is handled by a maximum power point tracking (MPPT) algorithm, shown in Figure 1.

The MPPT algorithm is based on the classic Hill-climbing method [5]. A simplified flow chart of the algorithm is given in Figure 3. This method uses an iterative feedback process. While it does not require the characteristics of the solar cell to be known in advance, it needs to monitor a feedback parameter. We chose to monitor the output current of the converter, which is the current through the PMOS. The reason is V_{BAT}

hardly changes during one group measurement (Figure 3) and therefore the output current represents the power converted. Maximizing this current is equivalent to maximizing the input power. The algorithm has two sessions, *Search* and *Long-wait*. In the *Search* session, the algorithm carries out a series of group measurements. Each group measurement consists of three measurements of the converter output current using three N_{skip} values (Nskip, NskipLess and NskipMore). The three values correspond to three different operation points on the power curve, as illustrated in Figure 3 (upper-right). NskipLess and NskipMore are calculated from Nskip based on the selected step size and there are three step sizes. During each measurement, a high-side current sensor (Figure 1) outputs a scaled copy of the current through the PMOS switch and charges one of the three algorithm capacitors (Figure 1), which are associated with the three N_{skip} values.

At the end of each group measurement, the voltages accumulated on the algorithm capacitors are compared with each other by the evaluation comparators shown in Figure 1. The one with the highest voltage wins and the N_{skip} value associated with it becomes the Nskip of the next group measurement, from which a new NskipLess and a new NskipMore will be calculated. Each time the first N_{skip} value of a group measurement (Nskip) in two consecutive group measurements wins, the algorithm switches to a finer step size. If this happens when the current step size is the finest, the algorithm declares the MPP state is reached and this Nskip is the optimal N_{skip} value at this moment. The *Search* session is then ended and the algorithm enters the *Long-wait* session, during which the algorithm does not change the N_{skip} value and the converter operates with the optimal N_{skip} value. The *Search* session is started again after the *Long-wait* session.

A wide input power range results in a huge variation of the algorithm capacitor voltages, as illustrated in Figure 3 (lower-right). To address this issue, the scaling factor of the current sensor is adapted during the Hill-climbing procedure by monitoring the voltages accumulated on the capacitors in order to expand the dynamic range of the algorithm.

The efficiency of the converter without MPPT was measured under various conditions, as shown in Figure 4. The converter is able to convert input power from 5μW up to 10mW. The measured peak efficiency is around 87%. The whole control circuit consumes a static current of 0.65μA from the battery when not converting power. While converting minimal power (5μW) and maximum power (10mW), the current consumption is 0.8μA and 2.1μA, respectively. The measured performance of the converter with MPPT is shown in Figure 5. For the convenience of measurement without losing generality, we simulated a solar cell array with a current source in parallel with three diodes in series, which gives MPP voltages (around 70% of open-circuit voltage) well within the input voltage range when the current is adjusted from 10μA to 1.2mA. The algorithm succeeded in tracking MPP with a relatively flat end-to-end efficiency curve, peaking at 70%. Since the algorithm was implemented as a demonstration of feasibility, Figure 5 also shows some mismatch loss due to the algorithm timing, which was not optimized yet.

When V_{BAT} is below 1V, the converter first charges the ESS through the body diode of the PMOS switch while a startup circuit (Figure 1) ensures that the NMOS switch remains turned off and the PMOS switch subsequently is turned on so that the solar cell can continue to charge the ESS until V_{BAT} reaches 1V, after which the startup circuit is

disabled. This feature is useful when a super-capacitor is left in a dark area for an extended period.

In conclusion, this self-contained and fully autonomous converter features an input power range spanning from 5µW up to 10mW while consuming very little power. A comparison with state-of-the-art publications is shown in Figure 6. The method used for MPPT is generic for energy source with one global maximum on their power curves. It is thus possible to use it with TEG and RF harvesters provided their output voltages fall within the input range. The presented circuit was fabricated in a commercial TSMC 0.25µm CMOS process with 5 metal layers and uses one compact SMD inductor of 1mH. A die photo is shown in Figure 7.

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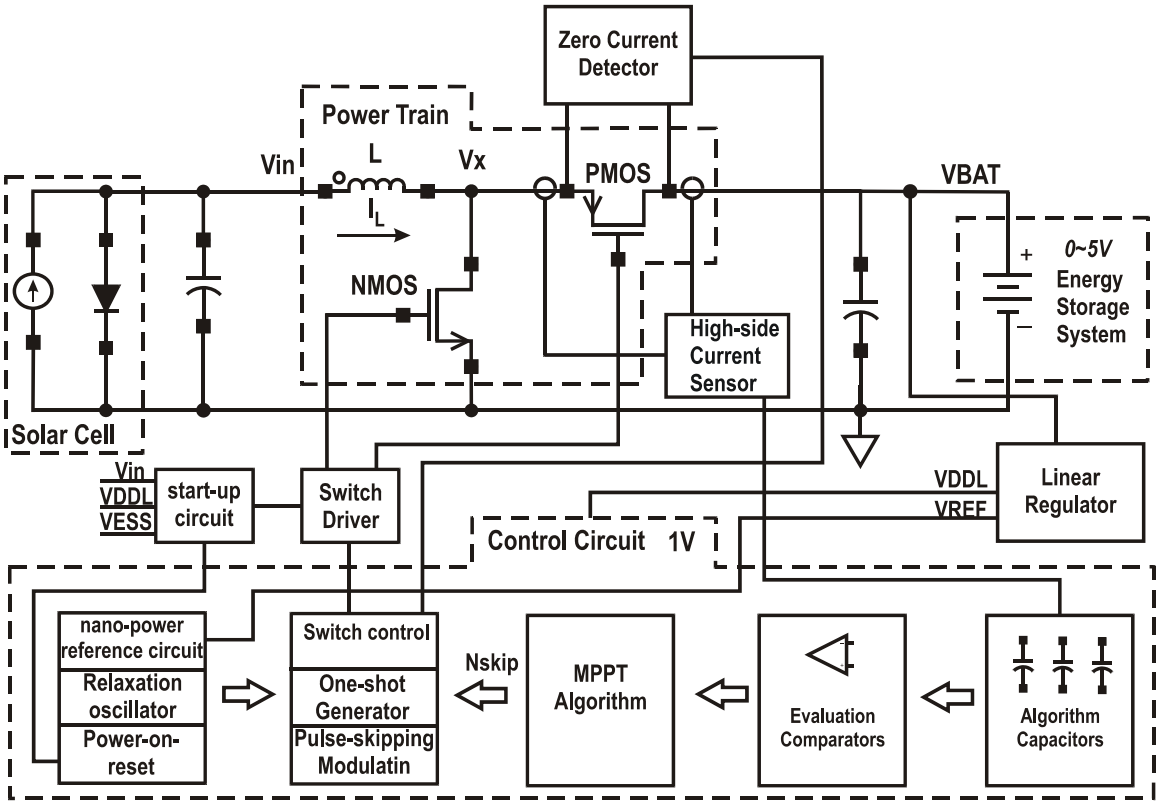
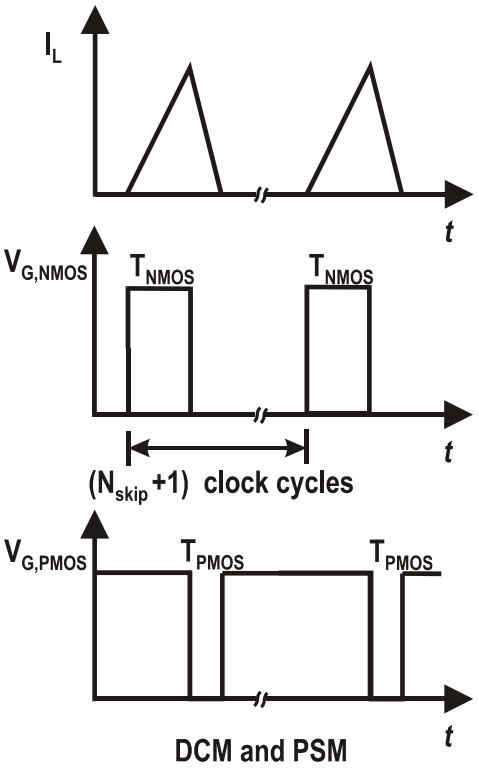


Figure 1 Block diagram of the system.



$$I_{in,avg} = \frac{V_{in} D_1^{\,2} T_s}{2L} \cdot \frac{V_{out}}{V_{out} - V_{in}}$$

$$D_1 = \frac{D_1 T_S}{(1 + N_{skip}) T_{CLK}}$$

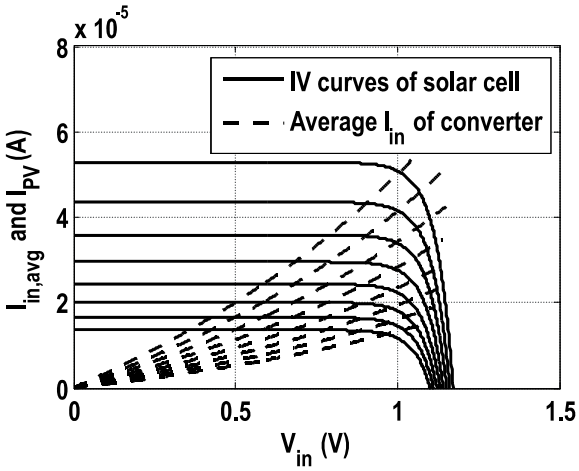


Figure 2 An illustration of DCM and PSM influencing the operation point of the solar cell. The dashed curves are sweep of N_{skip} (using a fixed D_1T_S) and the solid curves are sweep of solar cell power.

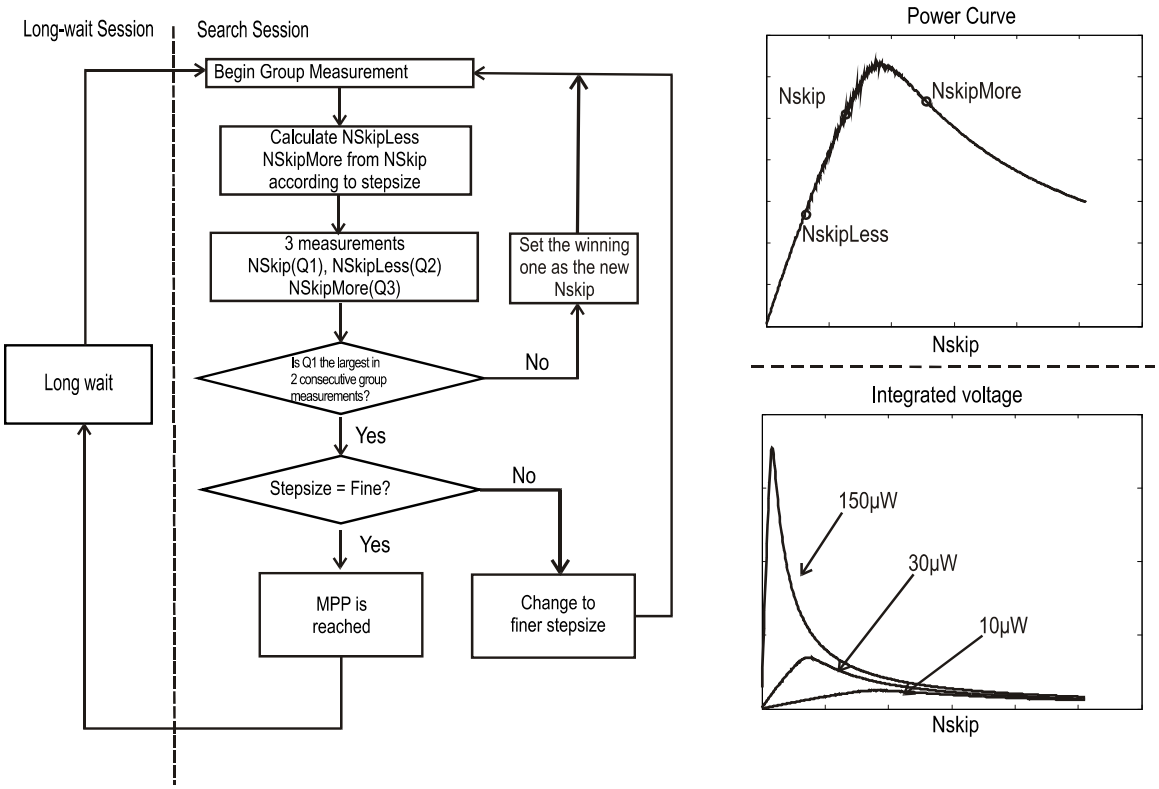


Figure 3 Simplified diagram of the maximum power point tracking algorithm

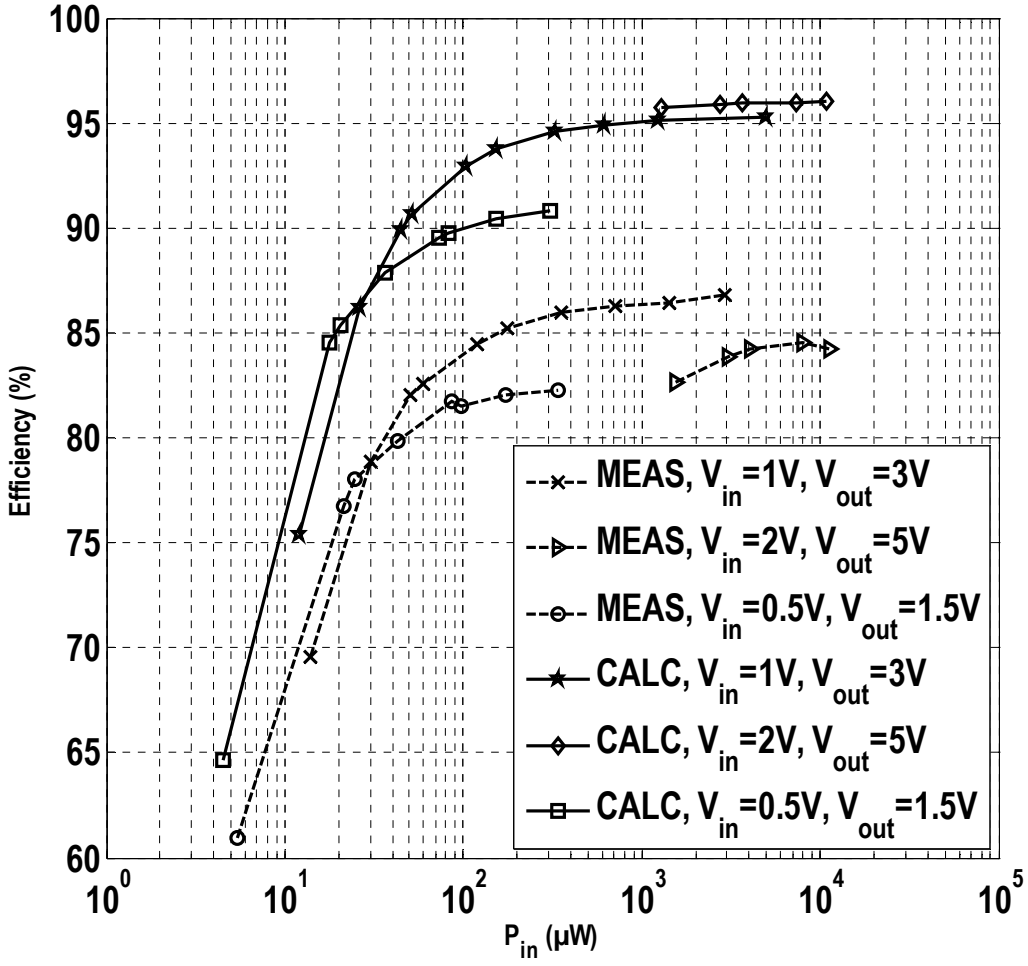


Figure 4 Measured (dashed) and calculated (solid) converter efficiency with respect to input power. The calculated efficiency includes an estimate of the control circuit power consumption but excludes other non-idealities.

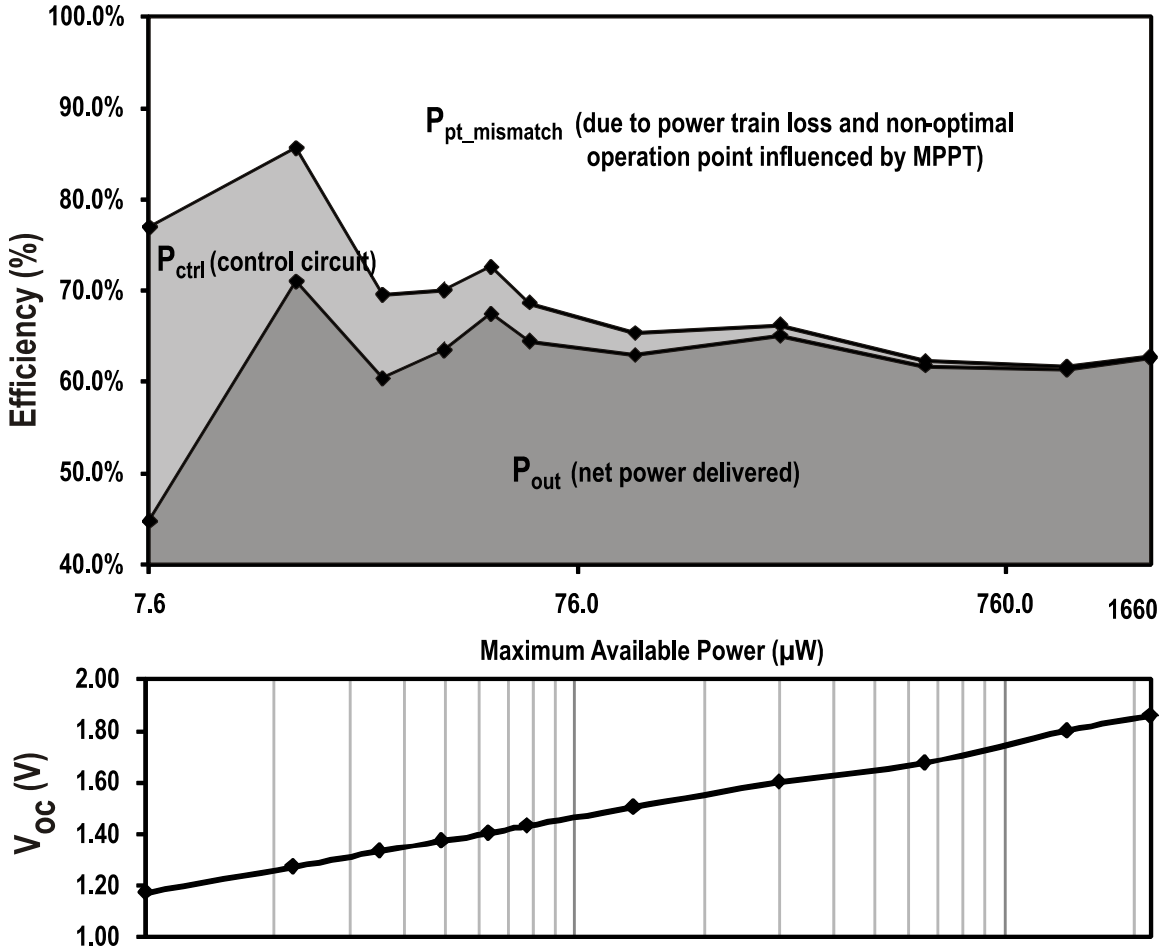


Figure 5 Experimental end-to-end efficiency using a discrete equivalent circuit as a solar cell simulator (V_{BAT}=3V) to cover the broad input power range. Also shown is the corresponding open-circuit voltage.

	[6] (ISSCC,09)	Carlson (JSSC,10)	This work
Input voltage range	>0.6V	20mV to 250mV	0.5~2V
Output voltage	0~3.3V	1V	0 ~ 5V
Power throughput	Pin=10μW ~ 1mW	Pout=1μW ~ 100μW	Pin=5μW ~ 10mW
Power consumption of control circuit	2μW @ P_{in}=100μW 7μW @ P_{in}=1mW	1.6μW @ P_{in}=54μW 1.1μW @ P_{in}=233μW	2.4μW @ P_{in}=8μW 3.5μW @ P_{in}=1.66mW
	(V_{BAT} = 2V)	(V_{BAT}=1V)	(V_{BAT} = 3V)
Function	Harvester interface +MPPT	Harvester interface + voltage regulator	Harvester interface + MPPT
Architecture	Reconfigurable capacitive charge-pump	Inductive boost converter	Inductive boost converter
Maximum efficiency converter: $\eta=P_{out}/P_{in}$	82%	78%	87%
Maximum efficiency end to end: $\eta=P_{out}/P_{mp}$	70%	N/A	70%
Startup voltage	V_{in}>0.6V and V_{BAT}>2V	V_{BAT} > 0.6V	V_{in} or V_{BAT} > 1V

Figure 6 Comparison with state-of-the-art publications.

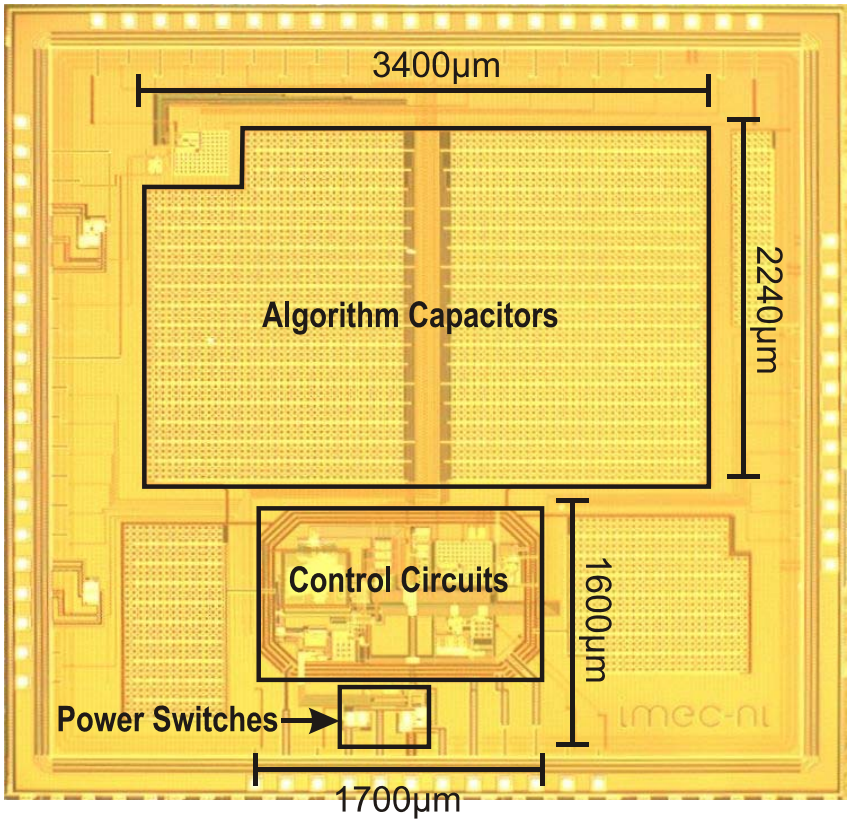


Figure 7 Die photo.