Ultra-Low Energy Time-Mode ADC with Background Calibration for Biomedical Sensing Applications

MSc Thesis

by

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ABSTRACT

Biomedical engineering focuses in advancing health care by taking advantage of the technological improvement. An important part of biomedical engineering is biomedical sensing, that focuses in the acquisition of biopotential signals. Through time, a lot of research has been done on the acquisition of biopotential signals and a variety of methods has been presented. The main goal of the front-end circuits of the biomedical sensing devices is to convert the analog value obtained by a sensor to its digital equivalent. In order to achieve an accurate conversion, the analog-to-digital converters used, need to achieve a medium resolution and a sampling frequency at the kilohertz range. Another important aspect in biomedical sensing devices is to achieve minimum power and area consumption.

The properties of the biopotential signals and the requirements set by the biomedical applications, make the design of ADCs based on classical mixed architectures increasingly difficult, as technology scaling deteriorates the performance of the analog part of the devices. In the presented thesis, time-domain signal processing techniques have been used in order to develop a programmable resolution, low-voltage, low-power and small-area time-mode ADC for biomedical applications.

The proposed time-mode ADC is a novel architecture and it is composed of a voltage-controlled ring oscillator based analog-to-time converter, followed by an asynchronous, unfolded SAR, coarse TDC and an asynchronous, enhanced range. fine flash TDC, As the input is sensed, the analog-to-time converter, embeds the analog information within the time period between a rising and a falling edge of the output signal. Following, the output time pulse is fed to the TDC that quantizes the pulse and produces the digital equivalent representation of the sensed value. The resolution of the ADC can be programmed from 8 to 10 bits. The delay elements of the coarse TDC are based on a novel modified version of Dynamic Leakage Suppresion delay elements. Moreover, a novel background calibration mechanism is introduced to correct the errors due to process variation. The calibration removes the offset and gain error of the ADC and achieves DNL and INL reduction.

The integrated circuit has been implemented in a 65nm TSMC process and its performance has been evaluated through Cadence and Synopsys tools. The ADC uses a 0.5V supply voltage and consumes 771 nW for 10-bit resolution. The total area of the ADC is 0.01342 mm^2. The maximum sampling rate is 2.2 KS/s. The DNL and INL of the 10 bit converter are +0.86/-0.83 and +0.88/-1.79 respectively. The simulation results indicate an SNDR of 61.3 dB and an ENOB of 9.8 bit for a 10mV peak-to-peak 1kHz input frequency.

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INTRODUCTION

1.1. IMPORTANCE OF BIOMEDICAL SENSING AND BIO-SIGNAL PROPERTIES

The population of the world has doubled within the last half century. Trying to understand this increase, various factors can be identified. The most important one is considered the improvement of the medical care, and thus the increased life expectancy of the population [1] . This is one of the main reasons behind the expansion of the healthcare industry in the last fifty years. Apart from the expansion of the healthcare industry, technology has been improving dramatically as well. As it is natural, these two industries have joined together to form what is called biomedical engineering. The main goal of biomedical engineering is to advance health care in the best possible way, from diagnosis to monitoring and therapy, by taking advantage of the technological improvement.

The understanding of biopotential signals is of high importance for the design of sensors and front-end circuitry of biomedical devices. Biopotentials are generated by collections of electrogenic cells through the generated volume conduction of currents [2]. This results in different biological systems to have different but specific electrical mechanisms. For example, electrocardiogram (ECG) is the result of action potentials of cardiac muscle cells [3], electroencephalogram (EEG) is the result of voltage fluctuation due to ionic current within neurons of the brain [4], Electrooculogram (EOG) is the result of biopotential induced by eye movement [5] and electromyogram (EMG) is the result of electrical currents generated during neuromuscular activities [6]. The mechanisms that have been described previously, lead to well characterized electrical properties. In Figure 1.1 the frequency ranges and amplitudes of different biopotential signals are depicted. As it can be summarized from the Figure, biopotential signals are usually characterized to have low frequency ranges in the order of a few kHz and small voltage amplitudes at the order of few mV [7].

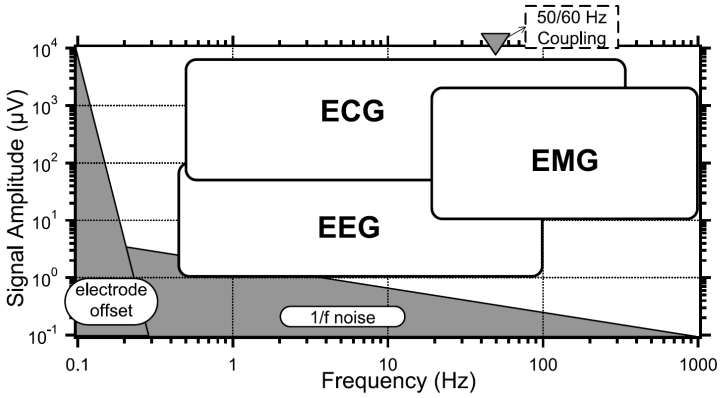


Figure 1.1: Electrical properties of biopotential signals [8]

1.2. ANALOG TO DIGITAL CONVERTERS IN BIOMEDICAL SENSING

In order to read the biopotential signals, and take advantage of the performance of digital circuitry, an acquisition system is needed. The most common readout front-end architecture of biopotential signals is depicted in Figure 1.2 and it is composed by a low noise amplifier (LNA), a low-pass filter (LP filter) and an analog to digital converter (ADC). From the above blocks, the LNA and the ADC are the most critical regarding their SNR performance and their optimization has been proposed through various methods. In modern clinical practice, the reduction of the size of the traditionally bulky and expensive instruments is of vital importance. Such a reduction is not only attractive in order to increase the comfort of the patients, but also to increase the mobility of the patients and eventually achieve autonomous biomedical devices for long term usage from the patient. Autonomous biomedical devices impose another important specification for the acquisition system apart from the size. The power consumption and thus the operation time of the devices needs to be maximized [9]. To summarize, the requirements for ADCs of biomedical sensing devices, they need to achieve a medium resolution, sampling frequency at the kilohertz range with the lowest possible area and power consumption.

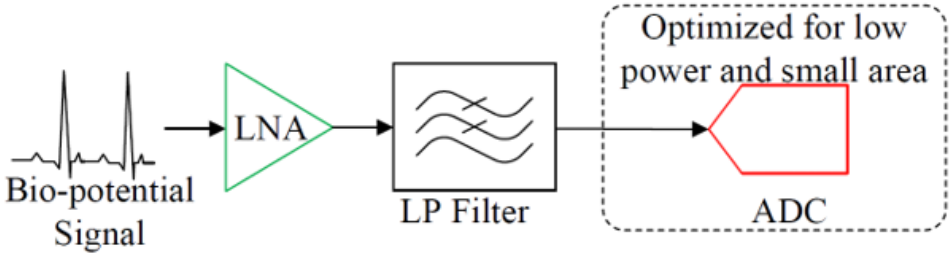


Figure 1.2: Front-end architecture of readout for biopotential signals [8]

The design of ADCs based on classical mixed signal architectures becomes increasingly difficult for biomedical sensing applications. This leads to the creation of two different trends. The first trend is the move of the accuracy and precision burden from the analog to the digital domain. This is achieved by the minimization of the mixed-signal part at the modern signal processing systems and the creation of more and more digitally assisted analog designs, as in [10] [11].

The second trend is using time-domain signal processing (TDSP) techniques and focuses at the representation and quantization of the signals in the time domain. In TDSP, a time interval is specified between either the rising edges of two signals or the time interval between a rising and a falling edge of a signal. The signals that are used for the time interval representation are digital and digital gates are used to process them. The main reasons of this choice, are the advantages that arise by technology scaling at the time domain, as the gate delays and thus the resolution is improved [12]. Moreover, due to their mostly digital architecture, they can tolerate higher noise margins under reduced supply voltages, and thus lower power consumption. In order to take advantage of TDSP techniques in data converters, three main blocks are required in order to communicate with the environment, the analog to time (ATC), the time to digital (TDC) and digital-to-time (DTC) converters.

1.3. RESEARCH GOAL AND SUGGESTED APPROACH

The main goal of the research progress presented here is to contribute to the area of the front-end electronics of biomedical devices through developing a novel programmable resolution, low-voltage, low-power and small-area time-mode ADC for biomedical applications. The proposed time-mode ADC (TM-ADC) is composed of a voltage-controlled ring oscillator (VCRO), followed by an asynchronous unfolded SAR coarse TDC and an asynchronous, enhanced range fine flash TDC, as depicted in Figure 1.3. As the analog voltage is sensed, the ATC converts it to a time pulse, embedding the analog information to a time period between a rising and a falling edge. The ATC outputs also the MSB of the digital output. The time pulse output of the ATC is then fed to the SAR-TDC that operates as a coarse-quantizer. The delay elements of the coarse TDC are based on a novel modified version of Dynamic Leakage Suppresion delay elements. The coarse TDC outputs not only the 6-bit digital conversion of the original time pulse, but also a time residue. The time residue is converted by the fine TDC to obtain the remaining 3 digital bits. Then, a simple digital block combines the three digital outputs to form the final 10-bit equivalent of the analog sensed value. A novel background calibration mechanism is introduced to correct the errors due to process variation. The calibration removes the offset and gain error of the ADC and achieves DNL and INL reduction.

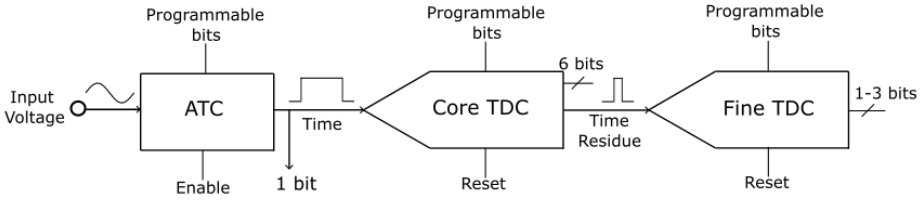


Figure 1.3: Suggested time-mode ADC simplified block diagram

1.4. THESIS DISSERTATION OUTLINE

The thesis report is composed of six chapters and the outline is as follows. In chapter 2, the current approaches used in the design of ADCs, time-mode ADCs and their components are discussed, along with their performance suitability for biomedical sensing applications. Moreover, in chapter 2 a brief presentation of the ADC performance metrics is included. In chapter 3, the system level design is introduced and explained, as well as the reasoning behind the selection of each block of the system. In chapter 4, the circuit implementation down to transistor level is presented along with the various challenges, trade-offs and performance evaluation. Furthermore, in chapter 4 the layout implementation of the system level blocks and their performance are presented. The simulation results and the performance of the ADC are evaluated and compared with state-of-the-art biomedical ADCs in chapter 5. Conclusions and further recommendations are discussed in chapter 6.

2

ADCs, ATCs, TDC AND THEIR PERFORMANCE FIGURES

Analog to Digital Converters are key-components in most electronic systems and applications, as they are the blocks that convert the information from an analog representation to a digital one. When a sensor operates, it translates natural phenomena to an electrical representation and specifically an analog signal by modulating a current or voltage value. When such a signal is available, it is needed to be converted and represented in its digital counterpart, which is suitable for further processing

Given the importance of such a block for so many different applications, a lot of research has been done in the field, resulting in various architectures and implementations, as different ADCs are suitable for different applications. The criteria based on the selection of an architecture are mostly the type of the input signal, conversion speed, resolution, power consumption, size and latency. Biomedical applications form their own requirements for the data converters and they are shown in Table 2.1. Bio signals are usually of low amplitude, typically less than 10mV. The resolution of ADCs needs to be in the medium range, typically from 7-to-12 bit. The bandwidth of the converters is usually smaller than 10kHz and can vary depending on the application. For most biomedical signals, a bandwidth of 1kHz is sufficient. The conversion speed in the majority of the applications is also not an issue and it can tolerate slow converters. The size of the converters is important as the smaller the devices are, the easier it is to be integrated into implementable or wearable devices. The power consumption is one of the most crucial performance metrics, as it directly translates to the operating time, allowing severe reduction at the batteries and thus the size of the devices.

Input Amplitude	10 mV
Resolution	Medium (6-12 bits)
Bandwidth	10Hz-1kHz
Power	Minimum
Area	Minimum

Table 2.1: Requirements of Biomedical ADCs

2.1. ANALOG-TO-DIGITAL CONVERTERS ADCS

Depending on the chosen criterion, different subdivisions of ADCs can be made. Such a criterion can be the selected sampling frequency in comparison with the signal bandwidth, resulting in two main classes of ADCs, the Nyquist rate converters and the oversampled converters. In the first category, the signal is sampled at the Nyquist rate or above it, resulting in a sampling frequency of at least twice the bandwidth of the signal [13]. In the second category, the sampling rate is much higher than the Nyquist rate and results in slower converters with higher resolution.

Another useful criterion is the conversion speed or the time needed for conversion. Based on the conversion speed the converters are categorized as:

- The first category in this classification is the parallel search converters. Here, the information from the input signal is converted to a single step in time, by comparing its value with all the required reference levels at one time moment.
- In the second category belong the sequential search algorithm converters. In this class, the total conversion is split in different phases. In each phase, a new set of references is used to quantize the information based on the information acquired from the previous phases.
- The third category is composed of the linear search algorithm converters. In this case, the input signal is compared in each phase to a linearly increasing reference until the value is quantized.
- The last category is the oversampled converters, where the signal in each phase is compared to fewer reference levels than required for the desired accuracy, but through the repetition of the conversation and the averaging of the output, a higher accuracy is achieved.

Under the parallel converters classification, there are two main architectures, the flash and the folding ADCs. A typical flash architecture is depicted in Figure 2.1. Through a reference voltage and a ladder structure all the $2^N - 1$ intermediate reference voltages for quantization are created and they are compared with the input voltage. Through a set of $2^N - 1$ comparators, a simultaneous comparison between the input and the reference voltages occurs and a thermometer code is obtained. Then a decoder is used for an N-bit digital representation. This architecture is used in many designs as it is the fastest ADC with low latency. Moreover, a sample and hold circuit is not always needed, due to the fact that the input value is necessary only during the activation of the comparators and the latches of the comparators can operate as one [14]. However, problems appear

when such an architecture is used for high accuracy as the area, the design complexity and power consumption increase with a 2^N fashion. The above-mentioned benefits and drawbacks make flash converters great candidates for applications that require very high conversion speed and low resolution, typically around 6 bits [15]. Flash converters are also used in hybrid architectures where they are combined with other architectures to result in high resolution and fast conversion.

The second main architecture of parallel converters is the folding ADC. Here a pre-processing stage is used in order to fold the input within a much smaller range and then convert the input value with quantization levels around the input value in the same way as a flash converter. In this architecture, the area and the power consumption are greatly reduced, while the latency and complexity are increased due the folding, the need for a coarse ADC and a digital block to combine the two digital outputs. Biomedical applications do not require the inherent advantages of the parallel converter architectures, high speed and bandwidth, while at the same time, low resolution, high power consumption and large area, make them unsuitable for such applications.

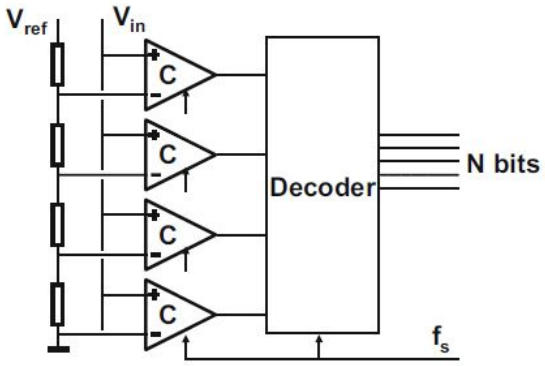


Figure 2.1: Flash ADC architecture [14]

In the sequential search algorithm converter classification, there are two main architectures, the Successive Approximation Register (SAR) and the Pipeline converters [16]. In the first architecture, the input value is estimated during N cycles, in which the input is compared to a different reference voltage which is based on the information acquired from the previous phases. For a conversion range of V_{con}, the input value is initially compared to $V_{con}/2$ and the MSB is obtained. Based on the MSB, $V_{con}/4$ is added or subtracted to the reference voltage, resulting to a new reference with a value of $3V_{con}/4$ or $V_{con}/4$. In this second phase, the input is compared with the new reference and the MSB-1 bit is obtained. Through the succession of this procedure, the final N-bit digital value is obtained. A typical SAR architecture is depicted in Figure 2.2. Initially the register has the MSB bit in logical high and the DAC converts it to an analog value $V_{con}/2$. The DAC output is compared with the input value and if the comparator gives an output of 1, the MSB remains 1 otherwise it becomes 0. In a similar way, during N phases

the N-bits are obtained. SAR ADCs are widely used in various applications as they are able to achieve a medium to high resolution with relatively medium speed and latency. However, despite the relatively simple architecture, there is a need for a good sample and hold for the input value as it needs to remain constant through the whole conversion period. Moreover, the DAC implementation is critical, as it imposes the accuracy achieved [14]. The complexity, size and power increase linearly with the resolution. SAR ADCs make a great candidate for biomedical applications as they not only offer the required resolution and bandwidth, but they are also able to achieve low power and area performance [17].

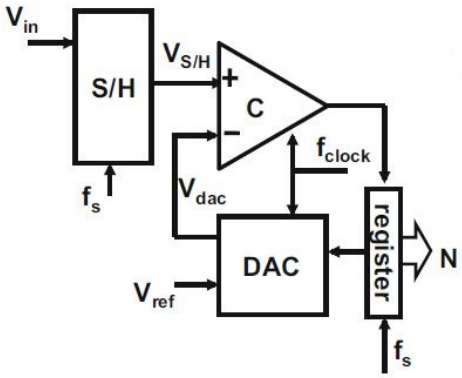


Figure 2.2: Successive Approximation Register (SAR) ADC architecture [14]

In pipeline architectures the input value is calculated through M repetitions, where M is the number of stages. In Figure 2.3 a stage of a pipeline ADC is depicted where the input is sampled and hold steady and a flash ADC is used to quantize the input value to 3 bits. Then, these 3bits are fed to a DAC and the analog output is subtracted from the initial input value. The analog residue is multiplied with a factor of 8 and fed to the next stage. A common technique used to allow digital correction is to add 1 bit overlap at the ADC and DAC and thus, the output of the stage occupies half of the range of the next stage ADC allowing correction. Given that each stage samples and holds its input and determines its output at different moments, registers can be used to save the output values. By doing so, each stage can resolve a different input value and thus achieve pipelining. Given the pipelining, high conversion speed can be achieved but with a medium latency as there are multiple stages and digital operations that are needed [15]. The complexity, size and power increase linearly with the resolution. Pipeline ADCs make a good candidate for biomedical applications as they are able to achieve the desired performance while obtaining low power consumption[18].

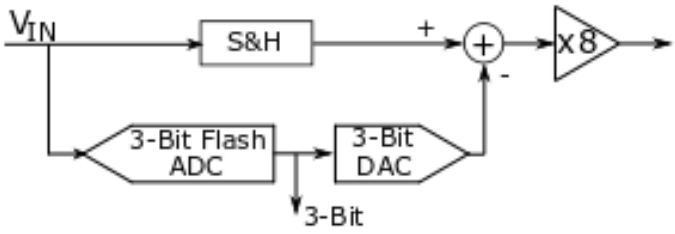


Figure 2.3: Pipeline ADC architecture [14]

In the linear algorithm converter classification,the most common architectures are actually two, the slope and the dual slope ADCs. In Figure 2.4 a simple slope architecture is depicted. When an input is sampled and held, the counter starts to increase from zero by count of 1. The counter values are fed to the DAC and they are compared to the input signal. As soon as the DAC output reaches the Vsignal, the comparator outputs 1 and the value of the counter is copied to the register. In a dual slope ADC, the operating principle is similar. However, the counter does not start from zero every time a new value is sampled but it is increasing or decreasing from the previous output. Such an architecture needs a super-fast internal clock compared to the sampling frequency as it needs to be $2^N * F_s$. The linear slope architectures are very simple, small and robust and find usage in many applications. However, they are very slow as they need at least 2^N periods and have a high latency as pipelining is not an option [14]. The power is doubled for every additional bit needed, while the area is not affected by the resolution.

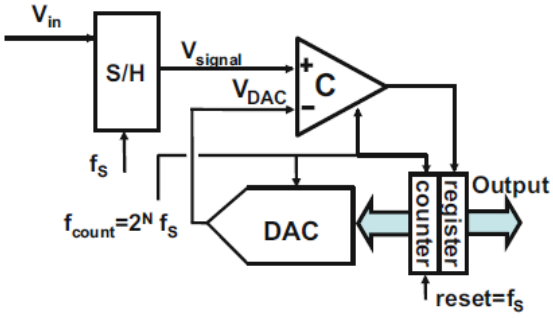


Figure 2.4: Slope ADC architecture [14]

The last category, oversampled converters, vary vastly from the above Nyquist rate architectures. This is due to the fact that the main goal of such converters is not to quantize wide-band signals but signals whose bandwidth is limited. The most popular architecture is sigma-delta converters and a typical architecture is depicted in Figure 2.5. Here the output of the DAC is subtracted from the input signal and then fed to an integrator. The output of the integrator is fed to an ADC (or a comparator as it may be an 1-bit ADC) and a digital value is obtained. This digital value is then fed to the DAC and the opera-

tion is repeated. Through the repetition of this process a bitstream is created which is then digitally filtered and decimated to the digital binary output. Sigma-delta converters are able to achieve high resolution for a low-to-medium conversion speed. Another advantage of sigma-delta ADCs is that the area and design complexity are not affected by the increase of the resolution for a specific implementation. Sigma/delta converters are inherently suitable for applications demanding high resolution, making them not an obvious choice for biomedical purposes. However, implementations able to meet the performance requirements of other architectures have been presented through time as in [19].

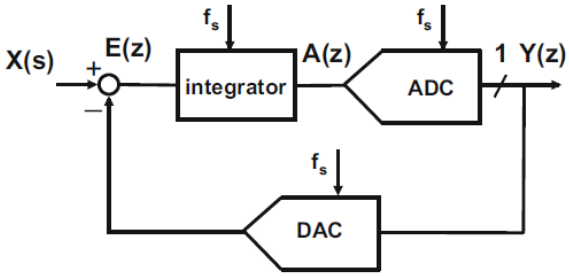


Figure 2.5: Oversampled ADC architecture [14]

Table 2.2 summarizes the performance of the analog to digital converters presented. Comparing the performance of the different architectures with the requirements for biomedical ADCs presented in Table 2.1, it is evident that SAR and pipeline architectures are the most suitable candidates. They are able to meet the requirements for speed and bandwidth while their power and area consumption is low and increases linearly with the increase in resolution [14]. Flash converters are not the most popular choice in the biomedical field as their high-speed performance does not justify the increase in power and area, however some implementations with modified architectures exist as in [20]. Despite the low speed and area of slope converters, they are not popular in the field of biomedical devices, due to their speed and bandwidth limitations. Sigma-Delta converters are not extensively used in biomedical applications as their high-resolution performance is not of interest, but there are applications taking advantage of their oversampling and noise shaping properties[21].

Architecture	Flash	SAR	Pipeline	Slope	Sigma Delta
Accuracy	<8bits	6-15 bits	8-16 bits	6-16 bits	16-24 bits
Speed	Highest	Moderate	High	Slowest	Slow
Bandwidth	High	Moderate	High	Lowest	Low
Power	High	Low	Low	Low	Moderate
Area	High	Small	Small	Small	Small

Table 2.2: Performance comparison of ADC architectures

2.2. TIME-MODE ANALOG-TO-DIGITAL CONVERTERS

While the technology scaling in the ultra-deep sub-micron regime is beneficial for the performance of the digital systems, it imposes stringent constraints on the analog signal processing and the front-end of ADCs, making the previously described generic structures less attractive. One of the main reasons is that the intrinsic gain of the transistor decreases while following Moore's law, due to the parasitic short channel effects and the physics of the transistors themselves **abraham2010moores**. Research on the topic has resulted in many countermeasures that cope with the problem of the reduced transistor gain. However, there are still other difficulties rising due to the reduced supply voltages, signal swing, voltage headroom, signal to noise ratio and increased noise coupling. Altogether, classical mixed signal architectures tend to become increasingly difficult to implement [22] [23] [24]. A promising solution for many applications seems to be the representation and processing of the signals in the time domain by using properties as the delay, frequency and phase of the signals. The main reason for this choice is that time-mode signal processing is mostly implemented in digital domain. This not only allows us to take advantage of all the typical digital design advantages, but also with technology scaling, time mode designs' performance improves while achieving reduced power consumption and area. In order to take advantage of time-domain signal processing techniques in analog to digital converters, two main blocks are required in order to communicate with the environment, the analog to time (ATC) or voltage to time (VTC) and the time to digital (TDC) converters. An analog to digital converter, that employs time-mode processing, operates based on the principle that an analog input value is first converted to a time quantity in the form of delay, frequency or phase through an ATC and then the time quantity is quantized to a digital value through a TDC.

2.2.1. ANALOG-TO-TIME CONVERTER

An analog to time converter is a fundamental block for all the time-domain signal processing systems as it is the block that converts an analog quantity to its time mode representation and its performance is vital for the accuracy of the whole system. Through time, many different topologies have been reported, some are more digitally assisted and some more analog. The main conversion principle though, for most of them, is the charging/discharging of a capacitance by using a current source.

The current starved inverter depicted in Figure 2.6 is the core in many ATC topologies. The basic principle is that a clock signal propagates through the inverter core (M2-M3 transistors) and the input transistor M1 is used to control the discharging current of the CL capacitance and thus the falling edge of the clock. Typically, such a topology does not achieve high linearity and is used when medium conversion accuracy is needed. Based on this simple principle, many different implementations have been proposed aiming at achieving higher performance, such as increased input range [25] , linearizing the transfer curve [26] [27] and lowering the power consumption [28].

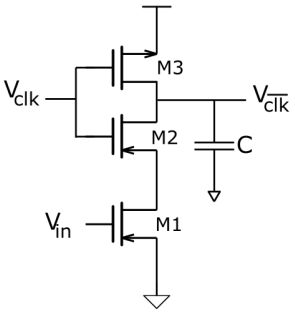


Figure 2.6: basic current starved inverter topology [29]

Voltage controlled oscillator ATCs are typically based on the cascaded current starved inverter topology. A cascade of current starved inverters are used in order to increase the performance of the VTC through an amplification and feedback design that results in a square waveform with varying frequency. A typical single ended N-stage ring VCO is depicted in Figure 2.7. The number of stages determines the nominal oscillation frequency and it can vary vastly between implementations [30] [31]. VCO based ATCs are able to achieve high gain, high frequency, low power, high linearity and small implementations through different trade-off mechanisms [32].

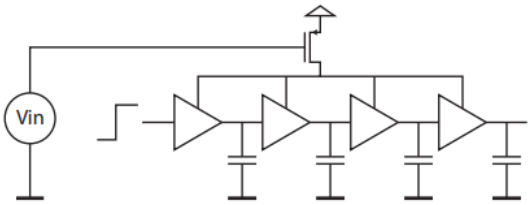


Figure 2.7: basic Voltage controlled oscillator ATC topology [29]

2.2.2. TIME-TO-DIGITAL CONVERTER

The time to digital converter is the second building block in time-mode analog to digital conversion as it is the block responsible for the quantization of the time signal. A time-mode signal can be defined either as the time between the edges of a signal, or the time difference of two separate signals, usually called the start and stop signal. Most TDC implementations are heavily composed of digital circuitry, performing better with technology scaling. Technology scaling is beneficial as the gate delays are reduced and thus higher resolution can be achieved. Moreover, higher conversion speeds, lower power consumption and reduced die area are benefits that come with technology scaling [33]. Through time, many TDC topologies have been implemented and presented in literature having different benefits depending on the application aimed.

One of the first and simplest implementations of time to digital conversion is the counter-based TDC. The basic principle is that a counter counts the number of a reference clock's periods within the input time interval. Given that the reference clock edges

and the time interval edges do not occur simultaneously, quantization errors are introduced. This topology is simple and has a low area consumption. However, its resolution is tied to the speed of the external clock, and thus a high frequency clock is needed, resulting in increased power consumption.

Flash TDC is a widely used topology as its core is the basic delay line as shown in Figure 2.8. The operation principle is based on the fact that the start signal propagates along the delay line and when the stop signal arrives the intermediate nodes are sampled simultaneously. When the simultaneous sampling occurs, the start signal propagates through a part of the chain and a thermometer code is created. The result of the thermometer code is given by $D_{therm} = DT/T_{LSB}$, where DT is the time interval for conversion and T_{LSB} is the delay of a single delay element. As it can be seen from the above equation, the resolution of the TDC is limited to the delay of a delay element. The use of inverters as delay elements rises some challenges as different rise and fall times of the elements can create mismatch. In order to circumvent this challenge a differential design has been presented and is depicted in Figure 2.9. In this topology, both the start and $\overline{start}$ signal propagate through the differential delay lines and the outputs of the inverters are swapped in each stage. The mismatch of the delay elements has been fixed, but the area and power of the converter is doubled. Based on this topology, many implementations have been proposed in the literature optimized for aspects such as area, power consumption, linearity and dynamic range [34].

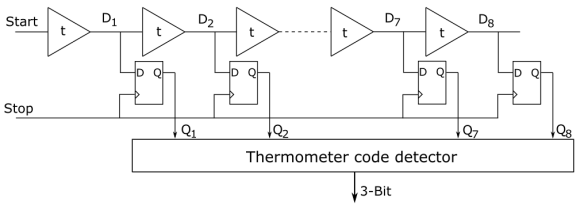


Figure 2.8: Basic flash TDC topology [35]

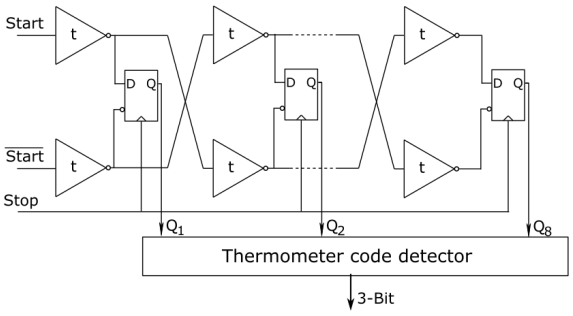


Figure 2.9: Basic differential line flash TDC topology [35]

Looped TDC is a topology based on the flash TDC, with the aim to enhance the range and measure longer time intervals with reduced area consumption. The operation prin-

ciple of the looped TDC is depicted in Figure 2.10. The basic idea is to create a loop around the original flash TDC and count the number of times the start signal has propagated through the chain when the stop signal goes high. This process results in a coarse quantization by the counter and a fine quantization by the delay line. The final digital value is obtained by $D_{therm} = N_{inv} * M_{loop} + N_{therm}$, where N_{inv} is the number of inverters in the delay chain, M_{loop} is the value of the counter and N_{therm} is the thermometer code obtained by the core TDC. Apart from the area reduction, looped TDCs, given the usage of the same elements multiple times, achieve better performance under local process variations [14]. The loop structure creates also some non-linearity issues due to the asymmetrical layout and the feedback multiplexer. Based on the idea of the looped flash TDC, different implementations have used this idea with a different TDC core as in [36] that a SAR ADC is used.

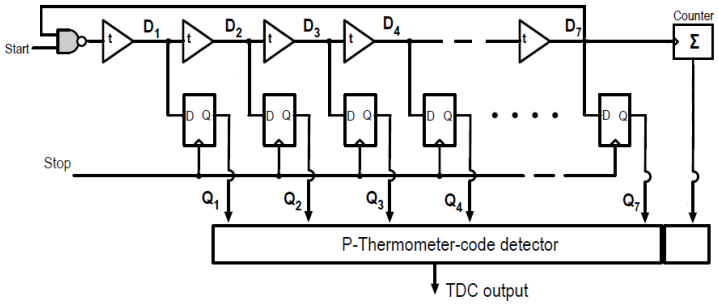


Figure 2.10: Basic looped-flash TDC topology [37]

The so far analyzed TDCs share a common characteristic. Their resolution is defined by the technology as it is limited to the delay of an inverter or a delay element. In order to cope with this problem a second generation of TDCs has been created that targeted sub-gate delay resolution in order to achieve higher resolution, linearity, smaller offsets, area and power consumption [38]. The ratio between the technology defined resolution over the resolution of the architecture is called the interpolation factor (IF). Local passive interpolation (LPI) TDC is such an approach that aims at sub-gate delay resolution utilizing a differential delay line where both start, $\overline{start}$ and stop signals are used. The basic topology of LPI TDC is depicted in Figure 2.11. The operation principle is similar to the flash TDC but by adding resistors between the inputs and outputs of the delay elements, voltage division is achieved between two same logical values with skew of one delay. The number of resistors defines the interpolation factor. Cross-coupled inverters are used in order to increase the speed of the delay elements. This is important in order to achieve proper interpolation, as the high-to-low and low-to-high propagation delays need to be smaller enough than the delay of the delay cells [39]. In order to achieve linear interpolation only the ratio of the resistors is important. The absolute value of the resistors is a trade-off between linearity and the power consumption. Low resistance values lead to more linear interpolation. The cross-currents of the resistors lead to an increase in the power consumption, and thus higher total resistance is desired to reduce the cross-currents and the power consumption. This approach shows good interpolation results

under global process variations due to the fact that only the ratio of the resistors is important.

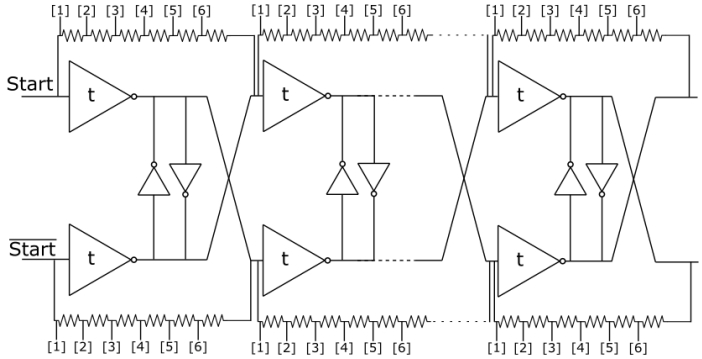


Figure 2.11: Basic Local Passive Interpolation TDC topology [40]

Vernier TDC is one of the architectures that aim at achieving sub-gate delay resolution. The architecture of Vernier TDC is shown in Figure 2.12. The time interval to be quantized is denoted by the start and stop signals, which are fed to two delay lines with different delay elements. The delay elements of the start signal chain have a larger delay than the ones of the stop signal chain. This results in a slower propagation of the start signal, allowing the stop signal to catch up with the start signal. The resolution of the TDC is not defined by the delay of the inverters but by the difference between the two delay cells, resulting in a theoretically infinite resolution. However, the propagation of the signals through two different chains, gives rise to some disadvantages like the matching between the elements and the performance under local process variations.

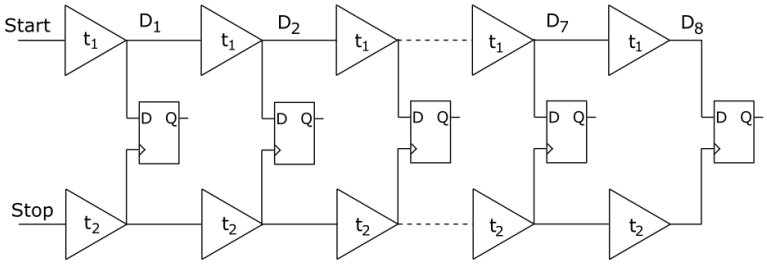


Figure 2.12: Basic Vernier TDC topology [41]

Pulse-shrinking TDCs aim at achieving sub-gate delay resolution by employing a delay chain with intentional asymmetries [42]. The architecture of a pulse shrinking TDC is depicted in Figure 2.13. The time interval for quantization is captured between the rise and fall time of a pulse. Each delay element in this architecture is composed of two inverters with different delays. When the time pulse arrives at the delay chain, the rising edge is inverted by the first delay with a delay of t_{d1}^{fall} and by the second delay with a delay of t_{d2}^{rise}. When the falling edge of the pulse arrives, the first delay inverts it with a delay of t_{d1}^{rise} and the second with a delay of t_{d2}^{fall}. The pulse shrinking is based on the different delays the rising edge and the falling edge of the pulse propagate, and it defines the resolution of the TDC. The need for two inverters leads directly to an increased area and power consumption at the cost of higher resolution.

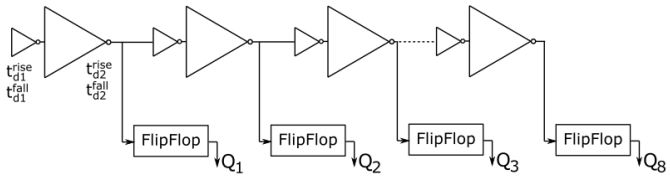


Figure 2.13: Basic Pulse-shrinking TDC topology [37]

Time amplification TDCs aim at higher resolution without the need for sub-gate delay resolution structures. Higher resolution is achieved by stretching the time interval along the time axis with a constant gain. Due to the small linear region of time amplifiers, this architecture is usually composed of a coarse and a fine TDC. The residue of the coarse TDC is fed to the time amplifier resulting in a bigger time interval for the fine TDC. Time amplification TDC designs usually face more challenges as time amplifiers are not linear and are susceptible to noise.

Parallel scaled delay elements TDCs achieve sub-gate delay resolution but their main goal is the improvement of the latency and conversion time of TDCs. The basic block diagram is depicted in Figure 2.14. In this architecture the delay elements are placed in parallel with different load capacitances at each branch. The different load capacitances between the inverter outputs and the flip-flops leads to different delays for the delay cells. The operation is pretty simple as the start signal is fed simultaneously to all the branches and the outputs are sampled simultaneously. Depending on the duration of the time pulse, the signal will manage to propagate through a part of the branches resulting in a thermometer code. The resolution of this architecture is not defined by the technology but by the difference of the delays of the consecutive branches.

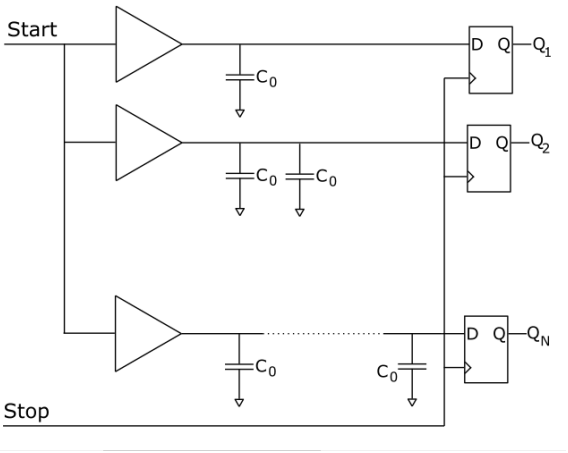


Figure 2.14: Basic parallel scaled delay elements TDC topology [33]

Gated Ring Oscillator TDCs is an approach that aims at the increase of the resolution by means of oversampling and noise shaping. The architecture is based on the ring oscillator and it is depicted in Figure 2.15. The basic principle is that a time interval is quantized based on the number of delay elements the pulse propagates. The difference between a GRO oscillator and a traditional oscillator-based structure is that the oscillator only operates for the time interval needed for the measurement. Between consecutive measurements, the switches to the supply and ground open and the state of the oscillator freezes. First order noise shaping is achieved due to the fact that by freezing the state of the oscillator, the residue of a measurement is transferred to the next measurement. The implementation of such a TDC is not trivial and effort needs to be put to reduce the injection of current during the switching of the delay elements to the supply and ground.

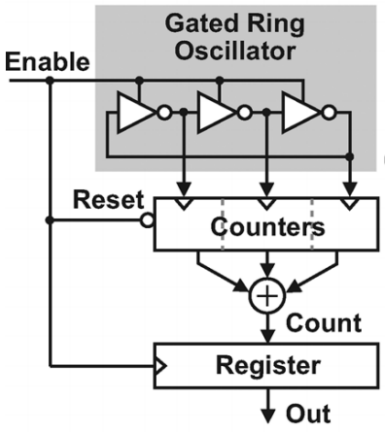


Figure 2.15: Basic Gated Ring Oscillator TDC topology [43]

Sigma-Delta TDCs is another approach to achieve fine resolution. A conceptual diagram of the TDC is depicted in Figure 2.16. The operation principle is the same with voltage domain sigma-delta converters but instead of an analog input, the input is in phase domain. A phase detector is used in the summation node of the input with the feedback loop signal. In the feedback loop, a digital to phase converter is used in order to generate the phase-domain reference signals. The loop filter function is not easily understood in time mode and for this reason it usually happens in voltage domain. After the filter, the comparator operates in voltage domain as well. Different approaches have been taken through time in order to tackle with the challenges of time mode sigma delta architectures as in [44] [45] [46]

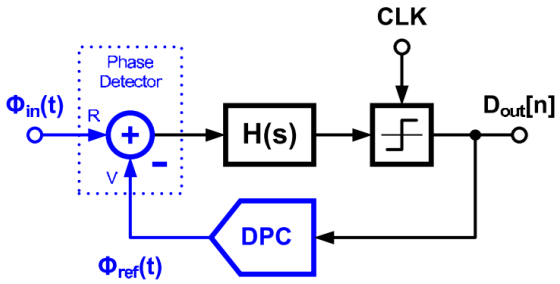


Figure 2.16: Basic Sigma-Delta TDC topology [47]

2.3. ADC CHARACTERIZATION

Designing or selecting the proper ADC for an application is directly related to understanding the characteristics and performance Figures of the converter and the origins of their limits. A common differentiation of the characteristics can be made based on wether their values are time dependent or not.

2.3.1. STATIC CHARACTERIZATION

Static characteristics aim at quantifying into metrics the static performance of an ADC. The static performance of a time-mode ADC is affected both by the analog to time and the time to digital conversions.

The transfer function of an ADC depicts the mapping of the analog values to their digital counterparts. The transfer function of an ideal ADC is a straight line, but given the finite number of digital codes in a real ADC, the ideal transfer function is a uniform staircase plot as depicted in Figure 2.17. The number of digital codes defines the resolution of the ADC. Analog values in the x-axis are continuous while digital codes in the y-axis are discrete. This results in the fact that a digital code represents not a single analog value but a fraction of the analog range. The input fraction that corresponds to one code is the LSB of the converter and it is $LSB = FSR/(2^N - 1)$, where FSR is the full-scale range of the converter and the N is the resolution of the converter. Due to non-idealities in the performance of a converter, a real transfer curve deviates from the ideal. These imperfections are divided into the linear and non-linear imperfections.

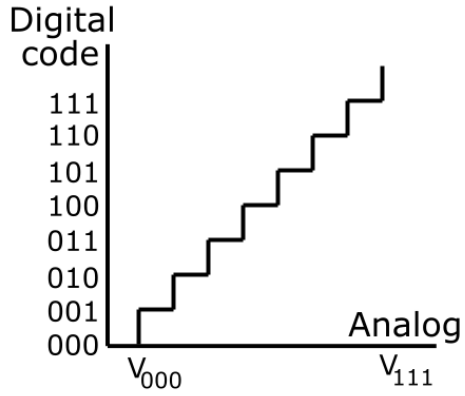


Figure 2.17: Transfer curve of ADC

The gain and offset errors are the linear imperfections and are visible directly from the transfer curve as shown in Figure 2.18. The offset error of an ADC is defined as $E_{offset} = (V_{00\ldots01} - V_{LSB})/V_{LSB}$ where, $V_{00\ldots01}$ is the input voltage equal to the first digital code. The offset error is a measure that quantifies the difference between the first ideal and actual code transition.

The gain of an ADC is defined as $k_{ADC} = DB/DV$ and it represents the slope of the transfer function. In a time mode ADC the gain is defined by the product of the gains of the ATC and TDC. The gain of the ATC and TDC are defined as $k_{ATC} = DT/DA$ and $k_{TDC} = DB/DT$. The gain error of an ADC is defined as $E_{gain} = (V_{11\ldots11} - V_{00\ldots01})/V_{LSB} - (2^N - 1)$. The gain error represents the deviation of the slope of the converter from its ideal slope and it can be noticed from the difference of the last step of the ideal and actual code transition.

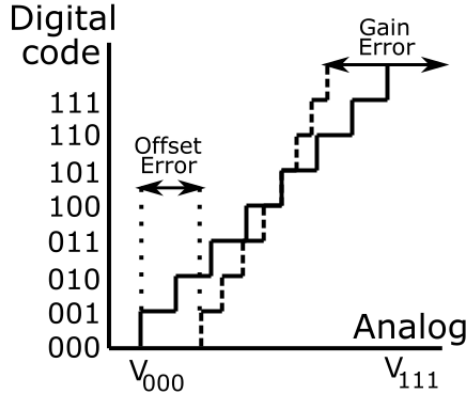


Figure 2.18: Offset and gain error in the transfer curve of ADC

The deviation of the ideal transfer function with a real transfer function leads to non-

linear imperfections in the conversion. The metrics describing the non-linear distortion are the differential non-linearity (DNL) and the integral non-linearity(INL) [14]. The first is a microscopic metric that describes for each step, its deviation from its ideal value. The DNL metric is depicted in Figure 2.19. The offset and gain errors described earlier contribute to the differential non-linearity as they affect the size of each step, and thus they should be removed before the calculation of the metric. Typically, DNL is presented either in a graph presenting the DNL values of all the codes, or as a single value that is the maximum value of the DNL of all the codes. The DNL for a time-to-digital transfer curve is calculated as:

$$DNL[k] = \frac{(t_{k+1} - t_k - T_{LSB})}{T_{LSB}} = \frac{t_{k+1} - t_k}{T_{LSB}} - 1 \tag{2.1}$$

Where t_k is the time moment the transition to the value k occurs and t_{k+1} is the time moment of the next transition.

The DNL metric is also used in order to describe the missing codes in the transfer curve of an ADC or TDC. A missing code is a translated to the overlapping of t_k and t_{k+1}. From formula 2.1 it is easily seen that this occasion is translated to a DNL value of -1. Thus, in order to guarantee the presence of all the codes, a DNL>-1 should be achieved.

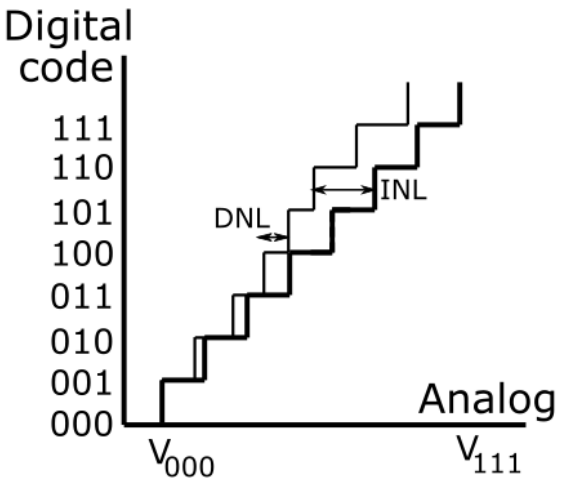


Figure 2.19: Differential Non-Linearity (DNL) and Integral Non-Linearity(INL)in the transfer curve of ADC

The second metric is the integral non-linearity(INL) which describes the distortion in a macroscopic way as it describes the error in the position of a code from its ideal value. The INL metric is depicted in Figure 2.19. The offset and gain errors described earlier contribute in the INL as they affect both the slope and the position of first code, and thus they should be removed before the calculation of the metric. Typically, INL is presented either in a graph presenting the INL values of all the codes, or as a single value that is the maximum value of the INL of all the codes. The INL for a time-to-digital transfer curve is calculated as 2.2. As it should be clear so far, the two metrics are strongly correlated

as the INL is the summation of the DNL of all the previous codes. This is depicted in the formula 2.3.

$$INL[k] = \frac{\left(t_k - t_{k,\,\text{ideal}}\right)}{T_{LSB}} = \frac{\left(t_k - t_{1,\,\text{ideal}}\right)}{T_{LSB}} - (k-1) \tag{2.2}$$

$$INL[k] = \sum_{k=1}^{n-1} DNL[k], k > 1 \tag{2.3}$$

2.3.2. DYNAMIC CHARACTERIZATION

So far, the described performance characteristics are not time depended. However, the performances of ADCs and TDCs are affected by dynamic, time dependent errors and limitations. For the evaluation of the devices under these errors, a number of dynamic characteristics has been established.

At this point, it is considered important to briefly describe how the noise in voltage domain is translated to noise in time domain and how it affects time-to-digital converters. Time domain signals are robust against voltage noise, as they have high noise margins, as digital circuits. However, voltage noise affects time domain signals when they are transitioning from a logical 0 to a 1 and vice versa. This is due to the fact that noise voltage around the switching threshold of the inverter is translated to time uncertainty. This time uncertainty has the form of jitter and it can affect highly the performance of the converter [48]. The most effective way to reduce the translation of voltage noise to jitter in time-domain circuits, is to have fast transitions at the signals. This can be simply explained, if one realizes that around the switching threshold, the voltage to time conversion gain can be linearly approximated as $V = (dV/dt) * t$. Thus, a gaussian distributed noise with a sigma of σ_u is translated to a gaussian distributed time-noise through

$$\frac{\sigma_v}{\sigma_t} = \frac{dV}{dt} \tag{2.4}$$

The signal to noise (SNR) ratio of a data converer is defined as the ratio between the maximum sinusoidal signal power that the analog-to-digital converter can handle, excluding the contribution of the harmonics at the multiples of the fundamental frequency. The SNR is given by:

$$SNR = 10\log_{10}\left(\frac{P_{\text{signal}}}{P_{\text{noise}}}\right) = 20\log_{10}\left(\frac{S_{rms}}{N_{rss}}\right) \tag{2.5}$$

where P_{signal} is the power of the fundamental, $P_{noise}$is the power of the noise, S_{rms} the rms value of the fundamental and N_{rss} is the mean value of the root-sum-square of the noise.

The power of the noise in data converters is the contribution of random noise and quantization noise. The quantization noise affects the SNR in a similar way as the random noise and is given by:

$$\text{SN}_Q\text{R} = 10\log_{10}\left(\frac{\text{Signal power}}{\text{Quantization error power}}\right) = 20\log_{10}\left(\frac{V_{\text{signal},rms}}{V_{Q,rms}}\right) \tag{2.6}$$

The SN_QR for an N-bit converter, that is used to quantize a signal at the Nyquist frequency is approximated by

$$\mathrm{SN_QR} = 1.76 + N \times 6.02 \text{ dB} \tag{2.7}$$

2

The Signal-to-Noise and Distortion Ratio (SNDR) is another useful metric in data converters as it quantifies the ratio between the power of the fundamental signal and the noise and harmonics power. The SNDR is given by

$$\mathrm{SNDR} = 10\log_{10}\left(\frac{\mathrm{P_{signal}}}{\mathrm{P_{noise}} + \mathrm{P_{harmonics}}}\right) = 20\log_{10}\left(\frac{\mathrm{S_{rms}}}{\mathrm{N_{rss}} + \mathrm{H_{rss}}}\right) \tag{2.8}$$

where P_{signal} is the power of the fundamental, P_{noise} is the power of the noise, $P_{harmonics}$ is the power of the harmonics, S_{rms} the rms value of the fundamental, N_{rss} the mean value of the root-sum-square of the noise and H_{rss} the mean value of the root-sum-square of the harmonic components.

Another common metric is the Total Harmonic Distortion (THD, that describes the ratio between the power of the fundamental signal over the power of the harmonics. The THD is given by

$$\mathrm{THD} = 10\log_{10}\left(\frac{P_{\mathrm{distortion}}}{P_{\mathrm{fundamental}}}\right) = 20\log_{10}\left(\frac{V_{\mathrm{distortion_{rms}}}}{V_{\mathrm{fundamental_{rms}}}}\right) \tag{2.9}$$

So far, the metrics shown, present the performance of the converter regarding the noise and distortion. The Effective Number of Bits (ENOB) uses the above metrics to characterize the real performance of the converter. The ENOB is given by:

$$\mathrm{ENoB} = \frac{\mathrm{SNDR} - 1.76}{6.02} \tag{2.10}$$

Different Figures of merit have been used that characterize the real performance of the data converter under different constraints. The Walden F.o.M. measures the performance of a converter regarding its power consumption as a combination of bandwidth BW and ENOB and is given by:

$$\text{F.o.M. } W = \frac{\text{Power}}{2^{ENOB} \times \text{ Minimum } \left(2BW, f_s\right)} \tag{2.11}$$

In a similar way the performance of a converter regarding its area consumption as a combination of bandwidth BW and ENOB and is given by:

$$FOM_P = \frac{\langle p \rangle}{f \times 2^{ENOB}} \tag{2.12}$$

3

ADC Architecture and System Level Design

So far, an analysis of the most typical ADC as well as the most typical TDC architectures, has been presented. It has also been highlighted that different architectures have benefits for a range of applications and through different implementations the resulting converters can become more and more suitable for specific applications. As it was explained in chapter 2, biomedical sensing applications have strict requirements regarding power and area consumption while the performance in terms of resolution needs to be medium and the sampling frequency at the kilohertz range. Taking into consideration the different drawbacks of the various architectures and the benefits of time domain signal processing, a different architecture is presented with main goal to achieve programmable resolution performance, varying from 8 up to 10 bits for the desired signal bandwidth, with the lowest power and area consumption.

3.1. Proposed Architecture

The proposed time-mode ADC architecture is composed of three main blocks and they are a voltage-controlled ring oscillator based ATC, followed by an asynchronous unfolded SAR core TDC and an asynchronous, enhanced range fine flash TDC, as depicted in figure 1.3. The proposed implementation employs also programmable conversion resolution. Moreover, a background calibration mechanism has been developed to reduce the effect of non-idealities.

The first block in the chain is the ATC. The ATC implementation is based on a VCRO, due to its controllability, low power and simplicity. The ATC is used in order to achieve the desired programmable oversampling ratio. The second one is the TDC, composed of a coarse unfolded SAR with time-domain subtraction and a fine enhanced range flash TDC. The first one is chosen for both low power consumption and small area properties while having moderate conversion speed [49] and the second one for its simple and robust architecture, small area and high conversion range. The last part of this section is

the calibration algorithm of the coarse TDC. The whole implementation is asynchronous due to its advantages over synchronous implementations. Namely the lower power operation due to the lack of a clocking signal and a better interface to TDSP system as the signal processing is mostly event based [50].

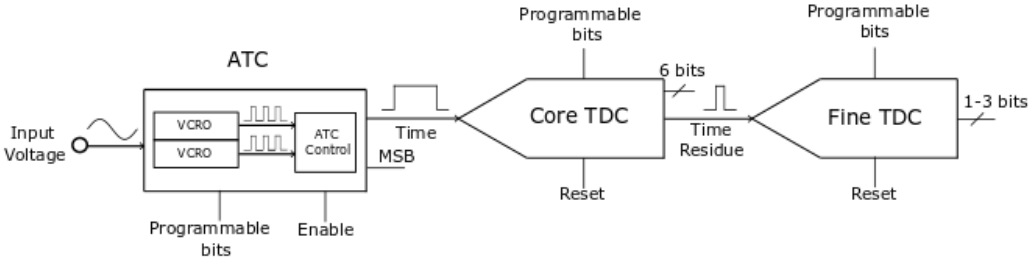


Figure 3.1: Proposed time-mode ADC architecture

The operation of the proposed architecture is rather simple. As the analog voltage is sensed, the ATC is converts it to a time pulse, embedding the analog information to a time period between a rising and a falling edge. The time pulse output of the ATC, is fed to the unfolded-SAR TDC that operates as a coarse-quantizer. The ATC creates also the MSB of the conversion. The core TDC outputs not only a part of the digital conversion of the original time pulse, but also a time residue, that is converted by the fine TDC to obtain the rest digital part. Then, a simple digital block combines the three digital outputs to form the final 10-bit equivalent of the analog sensed value. The calibration mechanism is composed of two steps. First, at the beginning of the TDC operation, the errors coming from the coarse TDC are quantified. The second step takes place in every conversion, as it takes the previously calculated errors into account, in order to create the digital equivalent of the input.

The ADC architecture implemented in this dissertation is shown in figure 3.1. The analog signal 'Vin,p' and its differential signal 'Vin,n' (180 degrees degrees phase shifted) are fed to two VCROs, the pVCRO and the nVCRO respectively. As soon as the oscillation frequency has stabilized, the pVCRO asserts the $nVCRO_{enable}$ signal in order to start the nVCRO as well. The output signals of the two VCROs are time pulses that depend on the input signal amplitude and thus they encapsulate in time domain the analog information.

In order to achieve the desired performance, in terms of signal to noise and distortion ratio, a control block has been implemented that combines the VCRO outputs and creates a single time pulse that represents the analog input signal by the duration of the pulse width. The control block does not only combine the two VCRO outputs to achieve the desired performance, but it also averages a programmable number of samples, achieving the desired oversample ratio. Moreover, the control block outputs the MSB of the digital word by detecting which VCRO has a positive and which has a negative input value.

The final time pulse of the control block is fed to the TDC. The TDC is implemented as a two-stage approach employing an unfolded SAR as the coarse stage and an en-

hanced range flash TDC as the fine stage. The coarse TDC is responsible for quantizing the time information in 6 digital bits. The selected resolution affects the delay values of the coarse TDC and it is selectable through its programmable input signal. The coarse TDC outputs also a time residue which encapsulates the remaining time information to be quantized. This residue signal is fed to the fine TDC which outputs from 1 to 3 digital bits, depending on the desired resolution. The fine TDC is also responsible for the measurements needed for the calibration of the coarse TDC. Finally, the MSB from the VCRO control block, the 6 bits from the coarse and the 1-3 digital bits from the fine TDC are combined to obtain an 8-10 digital bit representation of the analog input.

3.1.1. ANALOG-TO-TIME CONVERTER

The analog-to-time converter (ATC) is an utmost important element for time-mode analog-to-digital converters as it is used for the conversion of the input voltage to a pulse delay time interval, similar to pulse width modulation. The time interval for this architecture is encoded by the rising and falling edges of a signal with on-state equivalent to the time interval of the measurement. The linearity of the ATC limits the overall resolution of the ADC. Due to this, there are many different architectures of ATCs aiming to achieve linear behavior, from simple implementations based on a simple integrator [51] to complex implementations employing differential structures [52], or by employing several parallel current starving devices [53]. The basic building blocks of the ATC are depicted in figure 3.2, the voltage control oscillators and the control logic block.

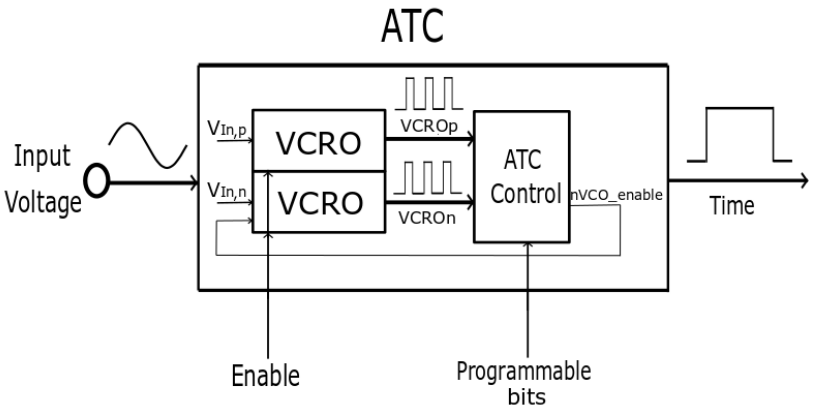


Figure 3.2: Proposed Analog-to-Time Converter architecture

3.1.2. VOLTAGE CONTROLLED OSCILLATOR

The voltage-controlled oscillator is implemented as a resettable 11-stage current starved VCRO and is shown in figure 3.3. Initially, a VCRO implementation has been selected as its performance characteristics fit the demands of biomedical sensing applications. VCROs when compared with relaxation oscillator implementations, are able to achieve relatively higher spectral purity while their size is small due to the lack of on-chip inductors as LC tank implementations [54]. Monostable multivibrator circuits were also

taken under consideration, however their performance in terms of power and spectral purity was considered inferior to VCROs. As VCROs are able to achieve oscillation frequencies much higher than the application desires, current starving is applied in order to limit the current and thus the charge and discharge speed of each stage's capacitive load. The current starving implementation gave rise to another important benefit in biosensing applications, the reduced power consumption [29]. In order to increase the gain of the VCRO, the current of the input transistor was mirrored, to modulate the turn-on resistance of both the pull-up and pull-down transistors of the intermediate nodes. To control the oscillation and achieve stable oscillation frequencies and also be able to power down the ATC when not needed, a reset signal was implemented by the addition of the AND logical function. The implemented VCRO achieves a constant gain over the input range, with a reset signal to control its operation.

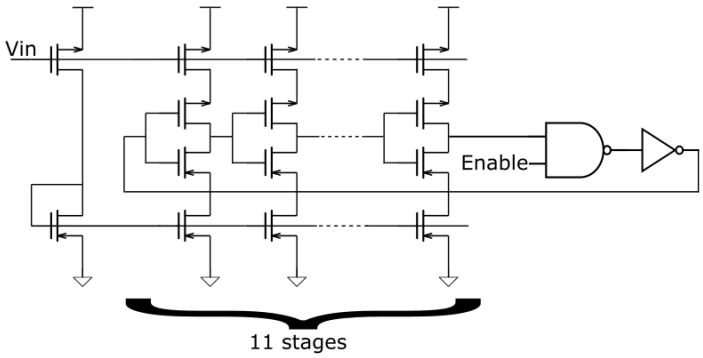


Figure 3.3: Implementation of the proposed Voltage Controlled Ring Oscillator

3.1.3. VCRO CONTROL BLOCK

The VCRO control block has manifold tasks in the operation of the ATC. The main duty of the control block is to control the operation of the two VCROs and create the final time pulse output of the converter and the MSB of the conversion. In order to achieve this, four modules are used and are depicted in figure 3.4 along with their input and output ports and their connections.

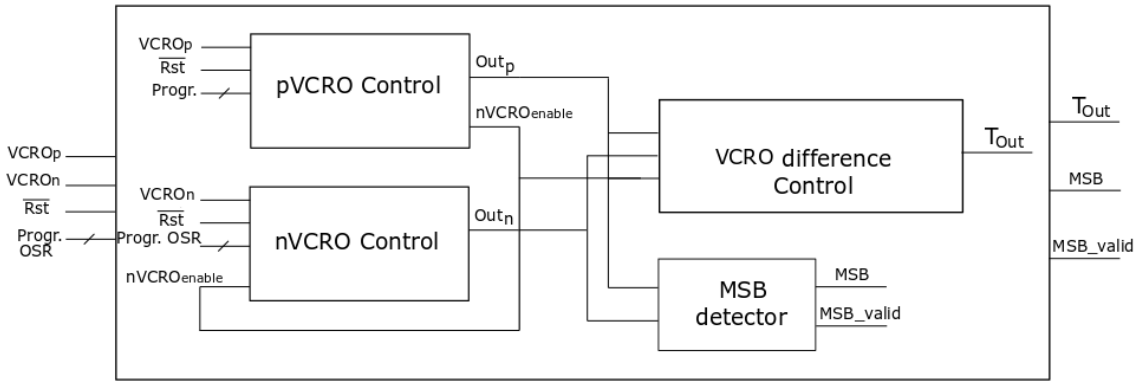


Figure 3.4: Analog to time converter Control Block diagram

The ATC control block receives the two high frequency square wave signals of the two VCROs, the active-low reset of the ADC and the programmable oversampling ratio. The ATC control block produces the MSB and the time pulse representation of the analog input, encoded by the rising and falling edges of the output signal T_{Out}. The pVCRO control is responsible for summing the output pulses of the VCRO and thus achieving the desired oversampling ratio, as well as synchronising the operation of the two VCROs by controling the starting moment of the nVCRO. Internally it is composed of three four modules. The pVCRO and nVCRO Control blocks, the VCRO difference Control andthe MSB detector.

The main goal of the two VCRO control blocks is to create the oversampled outputs of the VCROs. The pVCRO control block gets as input the square wave output of the pVCRO, the active-low reset of the ADC and the programmable oversampling ratio. It is responsible for the creation of the Out_p signal that encapsulates in its on-state the oversampled pVCRO output. Moreover it creates the $nVCRO_{enable}$ signal, that is used in order to activate the nVCRO. The nVCRO control is responsible for summing the output pulses of the nVCRO and thus achieving the desired oversample ratio. It gets as input the square wave signal of the nVCRO, the active-low reset of the ADC, the programmable oversampling ratio and the $nVCRO_{enable}$ signal. It outputs the Out_n signal that encapsulates in its on-state the oversampled nVCRO output.

The VCRO difference Control produces the final output signal of the ATC that encapsulates the oversampled differential VCRO time equivalent of the input signal. In order to achieve this, it gets as inputs the Out_p and Out_n signals from the pVCRO and nVCRO control blocks respectively, and the $nVCRO_{enable}$ from the pVCRO control block. As the input voltage modulates the oscillation frequency of the VCROs, the time pulse created from the VCROs is devided to the DC time component and the AC time component. The first one is equal to the oscillation frequency of the VCO when no input signal is applied. The AC time component, is the amount of time that is equivalent to the analog sensed voltage. The VCRO difference block is reset through the $nVCRO_{enable}$ signal.

The MSB detector block gets as inputs the Out_p and Out_n signals from the pVCRO and nVCRO control blocks respectively and the active-low reset of the ADC. The MSB

detector block creates two outputs, the most significant bit of the total ADC resolution and the MSBvalid signal, that is used to show that a valid MSB is obtained. The MSBvalid signal is needed for the case that a tiny signal falsely does not trigger the detector.

In order to explain the operation principle, it is considered beneficial to use the timing diagram illustrated in figure 3.5. As soon as the active-low reset signal goes high, the pVCRO starts oscillating and produces the pVCRO signal at its output. Then, the next 10 cycles are omitted in order to have a stable oscillation frequency. As soon as the 10 cycles occur, the pVCRO control block asserts its $Out-p$ signal and the $nVCRO_{enable}$ signal, in order to power-up the nVCRO. The nVCRO starts oscillating as well, causing the Out_n signal to be asserted. From this moment, the two oscillator control blocks start counting the periods of oscillation and are in a state ready to deassert their outputs as soon as the desired OSR is achieved. In the timing diagram example, the nVCRO reaches first the OSR limit and thus it is deasserted. This, is the moment that the VCRO difference control block asserts its output and the MSB detector is deciding for the value of the MSB. When the pVCRO reaches the OSR limit, the Out_p signal and thus the output of the ATC are deasserted. The two VCROs keep oscillating for 5 more periods, in order to eliminate any effects of the power-down of the circuit to the converted time pulse.

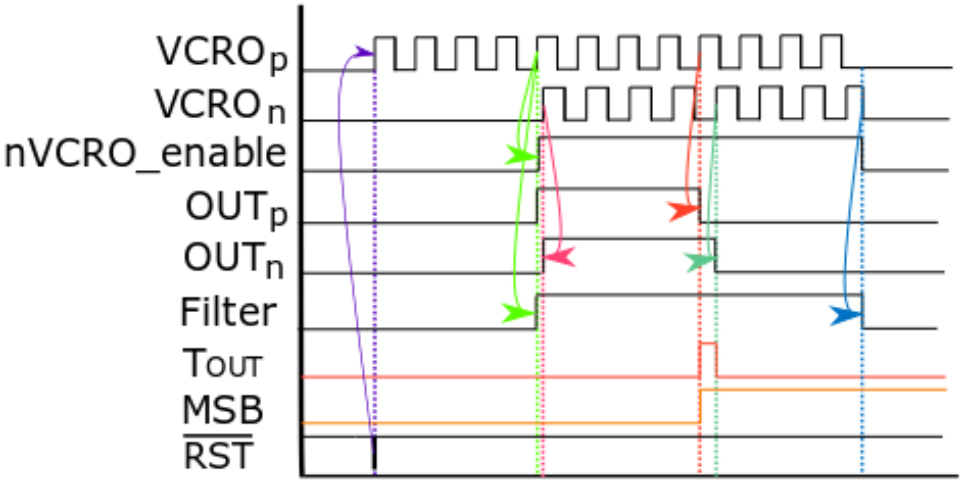


Figure 3.5: ATC Control Block timing diagram

3.1.4. TIME-TO-DIGITAL CONVERTER

The time-to-digital conversion is implemented in two stages. First, the time pulse is fed to an asynchronous, unfolded SAR , coarse TDC employing time-domain subtraction [55] that outputs 6 digital bits and a residue time pulse. Then, the enhanced range fine flash TDC quantizes the time residue to a 2-to-8 bit thermometer code. Both TDCs have been implemented asynchronously, due to the event-based operation of time-domain pulse signals. The choice of a two-stage implementation was due to two reasons. Firstly, to relax the resolution requirements of the coarse TDC and secondly, to be able to take the measurements needed for the calibration of the TDC.

COARSE TDC

The coarse TDC is implemented as an asynchronous unfolded SAR coarse TDC employing time subtraction similar to [55]. The selection of such an architecture was due to its reduced power and area consumption, while achieving sufficient resolution and conversion speed for biomedical sensing applications [55]. Moreover, the lack of a clock signal is not only beneficial due to lower power consumption, but it also makes a great fit with time domain signal processing systems as it follows the common event-based interface used.

In order to fully understand the operation principle of such an architecture, the time subtraction mechanism needs to be described first. Time subtraction is achieved by delaying the input pulse (Tin) by the desired subtraction value (Tsub) and XNORing the input signal with the delayed version of itself within a time window. The time window is defined by the rising edge of the original signal and the falling edge of its delayed version. This operation results at the absolute outcome of the subtraction: $Tout = Tin - Tsub$. In order to get the sign of the resulting time pulse, the observation that the positive result is generated by the AND logical operation of the XNOR gate and that the negative is generated by the NOR logical operation of the XNOR gate, needs to be made. For the case that the result of the subtraction is 0, no output pulse is detected. The AND and NOR logical operations can be easier understood through the example given in Figure **??**.

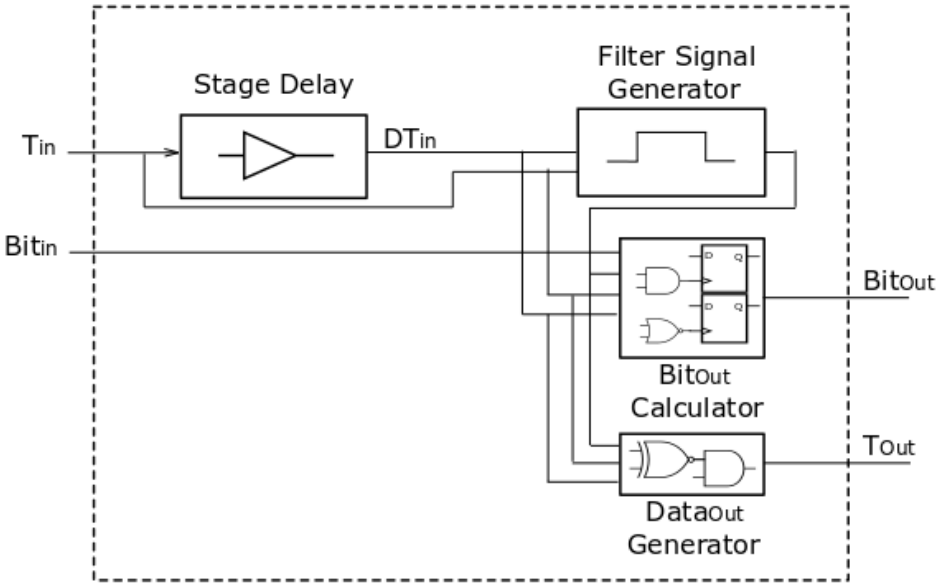


Figure 3.6: Block diagram of a stage of the suggested coarse TDC [55]

The unfolded-SAR TDC is composed of 6 cascaded stages without employing time amplification between them, as typically is done in the analog domain. Each of the stages, gets two inputs, the pulse to be converted T_{in} and the bit of the previous stage Bit_{in}. The outputs of each stage are the digital bit Bit_{out} and the time residue T_{out} that

will be processed by the following stages. Each stage is composed of its stage delay, a filter generator, a Bit_{out} calculation block and the $Data_{out}$ generator block. The delay ration of each stage, is equal to 2^{N-k}, where N is the conversion resolution and k is the stage number (with k=1 being the first stage). The filter signal generator is responsible for constraining the operation time of the rest of the circuit only for the period of interest, in order to avoid undesired outputs. The period of interest is defined from the rising edge of T_{in} signal and the falling edge of its delayed version DT_{in}. The Bit_{out} calculator block is responsible for the decision and generation of the output bit. The $Data_{out}$ generator block outputs the time residue that is the absolute outcome of the subtraction: $Tout = Tin - DT_{in}$ and needs to be converted from the following stage.

The operation principle of each stage is illustrated in figure 3.6. The T_{in} pulse is fed to the stage delay and together with its delayed version to the rest of the blocks. The filter signal generator produces an active high output (Filter) that is fed to the Bit_{out} calculation and T_{out} generator blocks. The $Data_{out}$ generator by XNORing the two versions of the input signal and ANDing its result with the filter signal create the T_{out} residue signal. The Bit_{out} calculator block employs an AND and an NOR gate that detect if the two signals are overlapping or not. Depending on the Bit_{in} signal and which one of the two gates fires, the decision on the output bit is made as depicted in Table 3.1.

	$Bit_{in} = 1$	$Bit_{in} = 0$
AND output goes high	$Bit_{out} = 1$	$Bit_{out} = 0$
NOR output goes high	$Bit_{out} = 0$	$Bit_{out} = 1$

Table 3.1: Decision table for Bit_{out} creation

The operation principle of the unfolded-SAR can be explained in an easier way through an example. For simplicity, lets assume that a 4-bit unfolded SAR is used with a T_{LSB} of 10ns and the input pulse has a value of 91ns. Lets also assume that the delays of the stages are 80ns, 40ns, 20ns and 10ns respectively starting from stage one to four. In figure 3.7 the timing diagram is presented in order to visualize the example. Initially the two versions of the input signal overlap and given that the Bit_{in} of the first stage is always 1, the decision is Bit_{out}=1 and the resulting time pulse is T_{out}=11ns. The next stage has a delay of 40ns that results in a "negative" 29ns T_{out} pulse and given that the $Bit_{in} = 1$, the Bit_{out}=0. The third stage has a delay of 20ns. Thus, the two versions of the 29ns input signal are overlapping. Given that the $Bit_{in} = 0$, this means that the result is a "negative" 9ns and the results in a "negative" 29ns T_{out} pulse and given that the $Bit_{in} = 1$, the Bit_{out}=0. The last stage has a delay of 10ns and thus the two signals do not overlap. The result is a T_{out}=+1ns and results in a "negative" 29ns T_{out} pulse and given that the $Bit_{in} = 1$, the Bit_{out}=1 as the $Bit_{in} = 0$.

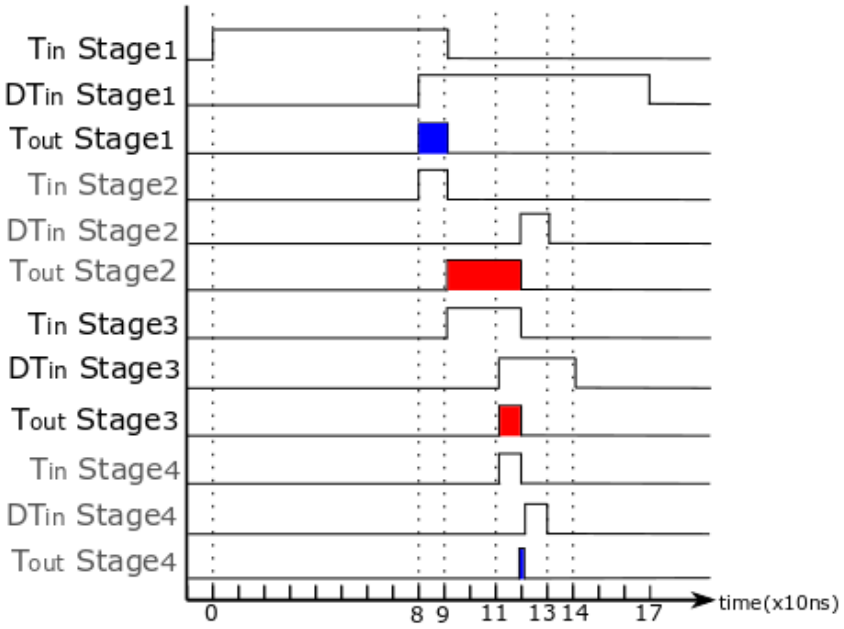


Figure 3.7: Timing diagram of 91ns quantization example of a 4-bit TDC with 10ns T_{LSB}, employing the suggested coarse TDC architecture

FINE TDC

The fine TDC is implemented as an asynchronous, enhanced-range flash TDC. The category of flash TDCs may not seem as the best candidate for biomedical sensing applications due to its high speed and power consumption, however there are many reasons that in this specific time-mode ADC implementation, the enhanced-range flash TDC is a great candidate. First, the asynchronous implementation of the flash TDC reduces drastically its power consumption, as energy is used only during the conversion period. Moreover, the usage of current starved inverters allows to achieve the desired delays with reduced power consumption. Another advantage of the flash TDC comes from the inherit nature of the converter, as it has a monotonic transfer curve. The thermometer code produced, together with a thermometer-to-binary bubble tolerant converter can guarantee monotonicity. Flash TDC implementations, due to their simple operation principle are suitable to convert them to looped-TDC architectures, and thus adding great advantages to the whole implementation. A benefit is the enhanced conversion range allowing the converter to exceed its previous limits through the addition of a counter with a slight increase in the area consumption. The simple and robust architecture, together with the enhanced range, make this implementation able to operate not only as the fine TDC but also as the calibration TDC. During the background calibration phase, the multiple usage of the same delay elements in the looped TDC, will allow better performance under local process variations. As it will be explained later in the chapter, during the background calibration phase, the fine TDC can produce bits with half T_{LSB}, making the calibration procedure twice more accurate.

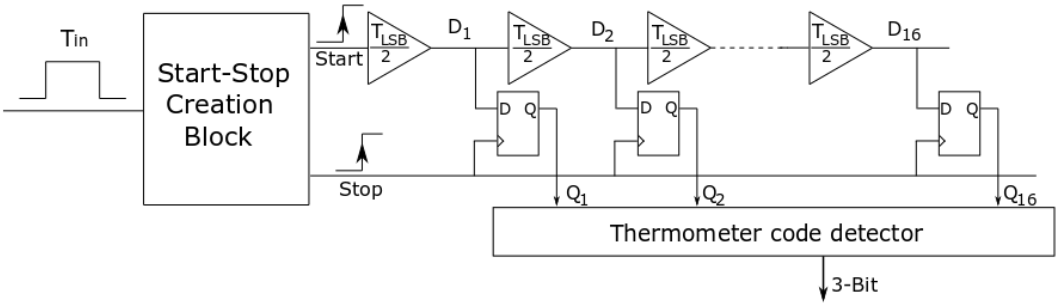


Figure 3.8: Fine TDC architecture

The input of the fine TDC is the time delay between the rising and falling edges of the residue pulse created by the last stage of the coarse TDC. However, the flash TDC implementation requires the time information to be encoded in the difference between two rising edges of two pulses. For this reason, a start-stop creation block has been implemented, to proceed with the creation of the appropriate signals. The flash TDC operation is based on the basic delay line. The start signal propagates through the delay line and when the stop signal arrives, the intermediate nodes and the counter value, are sampled simultaneously. When the simultaneous sampling occurs, the start signal has propagated through a part of the chain and a thermometer code has been created. The result of the thermometer code is given by $D_{therm} = DT/T_{LSB}$, where $DT = T_{fine} - D_{counter} * \frac{N_{del,cel}}{2} * T_{LSB}$. T_{fine} is the time interval for conversion for the fine TDC, $D_{counter}$ is the value of the counter, $N_{del,cel}$ is the number of delay cells in the delay chain. This process results in a coarse quantization by the counter and a fine quantization by the delay line. The final digital value is obtained by $D_{fine} = \frac{N_{del,cel}}{2} * D_{counter} + \frac{D_{therm}}{2}$, where $N_{del,cel}$ is the number of delay cells in the delay chain, $D_{counter}$ is the value of the counter and D_{therm} is the thermometer code obtained by the core TDC. In order to achieve the large delays needed and deal with the mismatches created by the different rise and fall times of the propagated signals, the delay cells are composed of four current-starved inverters instead of just one, as is commonly done in high resolution TDCs. Current starved inverters have been used as they achieve increased delay values and thus allow to achieve big delays with low power consumption.

3.2. PROGRAMMABLE RESOLUTION

Biosignal sensing applications require devices with the lowest possible area and power consumption, while the resolution of the converter is not needed to be high. Typically, in order to combine the low area and power consumption with the resolution demands, devices with resolutions from 6 to 12 bits have been implemented [49] [56] [57]. Devices used for different applications or different modes of operation in an application, through programmable resolution, can decrease their power consumption by sacrificing the achieved resolution. The programmable resolution in this architecture is implemented in order to allow the trade off between the achieved resolution and the power consumption.

A programmable resolution ADC can be implemented by omitting a part of the digital output code, however such an approach would not have an effect in the power consumption. Some reduction in the power consumption could be achieved by powering down the least significant parts of the ADC. However, in time mode ADCs, such an approach would be translated into omitting the part with the smallest delay cells and thus powering down a part of the converter does not reduce power consumption significantly.

An example could be used to explain better the not-high significance of the power consumption reduction in such an approach. Let's assume that a converter achieves a resolution of 8 bits and its delay cells are composed of cascaded versions of the T_{LSB} delay unit in a binary way. Thus, the MSB-delay cell is composed of 2^7 cascaded delay units and the LSB-delay is composed of only 1 delay unit. The total power consumption of the delay cells of such an implementation would be equal to

$$\text{Power}_{\text{total}} = \sum_{i=0}^{i=7} 2^i * P_{\text{unit}} = \left(2^8 - 1\right) * P_{\text{unit}} = 255 * P_{\text{unit}} \tag{3.1}$$

Where P_{unit} is the power consumption of the delay cell, with delay equal to the T_{LSB}. If the resolution of the converter is decreased to 6 bits by omitting the two least significant bits, the new T'_{LSB} is equal to $4 * T_{LSB}$ and the new power consumption would be given by

$$\text{Power}'_{\text{total}} = \sum_{i=2}^{i=7} 2^i * P_{\text{unit}} - (2^1 + 2^0) * P_{\text{unit}} = \left(\left(2^8 - 1\right) - 2^1 - 2^0\right) * P_{\text{unit}} = 252 * P_{\text{unit}} \tag{3.2}$$

Where P_{unit} is the same as before. As can be seen from the above example, indeed employing such a technique does not allow a significant power consumption.

In order to achieve a power consumption reduction that is proportional to the resolution reduction, another approach needs to be taken. The main idea of the approach taken in this ADC, is to keep the LSB delay the same and by the reduction of the oversampling ratio and the delay of the most significant delay cells, manage to achieve a proportional to resolution TDC power reduction. First, through the reduced oversampling ratio, the ATC power consumption decreases linearly with the reduction of the resolution (1 bit reduction is translated to half the power consumed by the ATC). Second, by reducing the delay of the delay cells responsible for the most-significant bits, a significant power consumption reduction can be achieved (1 bit reduction is translated to quarter the power consumed by the TDC). At this point, it is important to mention that in the above explanation, the power consumed by the pure digital control circuitry is not included in the calculations, as it is not dominating the conversion power.

The block diagram used for the explanation of the operating principle of the proposed programmable resolution for the ADC was given in figure 3.1. The nominal resolution of the device is selected to be 10 bits and the performance of the device when operating with the 10-bit resolution is considered for the rest of the analysis to be the nominal one. When the resolution of the device is decreased to 9-bits, the SNDR requirement of the ADC is reduced by 6dB. A 6dB reduction for the time-mode signal is translated to an OSR reduction to OSR/4 for the ATC. However, due to design choices made at an earlier moment,an OSR reduction to OSR/4 was not possible and an OSR/2

is implemented. The reduction of the OSR by 4 times was not possible due to the implementation of the delay elements with much higher delays. This made the reduction of the delays impossible, by tapping between the delay cells, as there were not enough elements. The advantages though of the delay cells regarding power consumption justified this decision, as their power consumption was minimal. This OSR reduction by two, is directly translated to time pulses with half their duration. For this reason, the delay cells of the coarse TDC are implemented to have programmable delays that can be controlled through the "programmable bits" signal. As the time pulses are reduced to half, and the coarse delay elements are reduced in half, it allows us to keep the T_{LSB} of the fine TDC the same. The operation of the fine TDC is affected as well, as it produces half the number of thermometer bits.

In order to better understand the operating principle of the proposed programmable resolution the following example can be given. Let's assume that a converter achieves a resolution of 7 bits, with 4bits from the coarse TDC and 3 bits from the fine TDC. Let's also assume that the OSR needed for the ATC is equal to 2, the T_{LSB} is equal to 20ns and the delays as shown in Table 3.2 . If the reduction to 6 bits resolution is desired, this would be translated to a reduction of the OSR to 1, the T_{LSB} to remain equal to 20ns and the delays as depicted in Table 3.2. Let's assume now that the analog equivalent of 106*V_{LSB} is given to the ATC. In the 7-bit resolution a time pulse with width equal to 2120ns is created by the ATC. The stage delays, the input and output delays, as well as the code created for the 7-bit resolution case are listed in Table 3.3. In Table 3.4 the same analysis is done for the 6-bit reduced resolution where the time pulse with width equal to 1060ns is created by the ATC with OSR of 1.

	7bit Resolution	6bit Resolution
ATC OSR	2	1
Maximum Delay	2550 ns	1270 ns
1^{st} stage delay of coarse TDC	1280 ns	640 ns
2^{nd} stage delay of coarse TDC	640 ns	320 ns
3^{rd} stage delay of coarse TDC	320 ns	160 ns
4^{th} stage delay of coarse TDC	160 ns	80 ns
Number of fine TDC delay elements	8	4
Delay of fine TDC delay elements	20 ns	20ns

Table 3.2: Example of 1 bit reduction with the suggested programmable resolution implementation

	Stage Delay	Tin	Tout	Dout
1^{st} stage delay of coarse TDC	1280 ns	2120 ns	+840 ns	1
2^{nd} stage delay of coarse TDC	640 ns	840 ns	+200 ns	1
3^{rd} stage delay of coarse TDC	320 ns	200 ns	-120 ns	0
4^{th} stage delay of coarse TDC	160 ns	-120 ns	+40 ns	1
Fine Flash TDC stage delay	20 ns	40 ns	0	010

Table 3.3: Example of 7bit operation of suggested TDC with 4 stages coarse and 3 stages fine resolution

	Stage Delay	Tin	Tout	Dout
1^{st} stage delay of coarse TDC	640 ns	1060 ns	+420 ns	1
2^{nd} stage delay of coarse TDC	320 ns	420 ns	+100 ns	1
3^{rd} stage delay of coarse TDC	160 ns	100 ns	-60 ns	0
4^{th} stage delay of coarse TDC	80 ns	-60 ns	+20 ns	1
Fine Flash TDC stage delay	20 ns	20 ns	0	01

Table 3.4: Example of 6bit operation of suggested TDC with 4 stages coarse and 2 stages fine resolution

The power reduction, in such an approach, is much higher than the previously analyzed cases 3.1, 3.2 and making the same comparison as earlier for a 2 bit reduction in resolution the new total power is equal to:

$$\text{Power"}_{\text{ total}} = \sum_{i=2}^{i=7} 2^{i-2} * P_{\text{unit}} - (2^1 + 2^0) * P_{\text{unit}} = \left((2^6 - 1) - 2^1 - 2^0\right) * P_{\text{unit}} = 60 * P_{\text{unit}} \tag{3.3}$$

3.3. CALIBRATION

Process variations greatly affect the performance of time-mode ADCs and it is a common technique to employ a secondary TDC for calibration purposes in order to get rid of the errors as in [58] [59]. In the architecture proposed in this dissertation, the fine TDC is used as the calibration TDC as well. This takes place due to the fact that its delay elements have sufficiently good performance under process variations. As it has already been mentioned and will be analyzed in the next chapter, the delay elements used for the coarse TDC are able to achieve the high delays needed, while having a small power consumption. However, this makes the coarse delay cells to have poor driving capabilities making them highly susceptible to process variations, as a relatively small increase or decrease at the load capacitance of a stage will make the delay much higher or lower respectively. In order to cope with such a problem, a novel calibration algorithm has been implemented based on measuring the errors of the coarse TDC delay cells, and use them in order to obtain the correct measurement.

The calibration procedure starts by applying 6 different time pulses so that the 6 delays can be quantified. For each time interval fed to the coarse TDC, 6 digital bits and a time residue is produced. Thus 6 equations with the following form can be produced.

$$T_{in,k} = \sum_{i=1}^{6} \text{bit}_{\,k}(i) * X(i) + T_{\text{residue,k}} \tag{3.4}$$

Where $Bit_k(i)$ is the digital output of the i^{th} stage for the kth input (either 1 or 0), X(i) the delay of each stage and $T_{residue,k}$ the time residue of the coarse TDC for the kth input. By solving the linear system of the 6 equations, the 6 delays can be calculated.

The coarse TDC architecture is based on time subtraction operation. When a time delay greater than the nominal one is subtracted from the input time pulse, the information is lost and there is no possibility for the information to be recovered. For this reason, the summation of the delay of the coarse TDC elements needs to be smaller than

the nominal delay. In order to guarantee this demand, the delay cells have been implemented with programmable delays.

The next step is the recalculation of the error for the new delays. For this step, the same procedure is followed as previously in the first step. As soon as the error is calculated, it needs to be quantized, so that it can be included in the calculation.

As explained in the operation of the coarse TDC architecture, the bit of the previous stage Bit_{in} determines the "sign" of the time pulse fed to the stage. Thus, the output bit of the last stage of the coarse TDC ($D_{coarse6}$) determines the sign of the residue and needs to be taken into consideration in the calibration operation as well. The formulas for the obtainment of the final correct measurement are:

$$D_{final} = 2^{N_2} * D_{\text{coarse}} + D_{\text{fine}} + D_{\text{correction}}\,, \text{ for } \mathrm{D_{coarse\,6}} = 1 \tag{3.5}$$

and

$$D_{final} = 2^{N_2} * D_{\text{coarse}} + \left(2^{N_2} - D_{\text{fine}}\right) + D_{\text{correction}}\,, \text{ for } \mathrm{D_{coarse\,6}} = 0 \tag{3.6}$$

Where D_{coarse} is the coarse TDC output, D_{fine} the fine TDC output and $D_{correction}$ the signed sum of the errors. For the $D_{correction}$ calculation, the Bit_{in} of the stage is taken into consideration. When the Bit_{in} is 1 the error is added keeping its sign, while for the case that the Bit_{in} is 0, the error is added with the opposite sign.

In order to understand the principle of the above operation, two examples are given. Let's assume that the same unfolded SAR is used as in the example in section 3.1.4, which is a 4-bit unfolded SAR with a T_{LSB} of 10ns and the delays of the stages nominally are 80ns, 40ns, 20ns and 10ns. Due to some error though, the delays of the stages are 71ns,38ns, 16ns and 7ns, as shown in Table 3.5. Through the set of the 6 3.4 equations, the errors are measured to -9ns,-2ns, -4ns and -3ns. The minus sign is used to show that the delays are smaller than their nominal values. In figure 3.9, the conversion of an input of 134ns is depicted. The methodology is the same as explained in section 3.1.4 to obtain the digital equivalent of the input which is $D_{coarse} = 1111$ and the time residue is $T_{residue} = 2ns$. As the Bit_{in} of all the stages is 1, the $T_{correction}$ is just the summation of the errors and it is $T_{correction} = -18ns$. As the last bit of the conversion is 1, equation 3.5 is used. So we have,

$$T_{input,calculated} = D_{\text{coarse}} * T_{LSB,coarse} + T_{\text{residue}} + T_{\text{correction}} \tag{3.7}$$

$$T_{input,calculated} = (15 * 10ns) + 2ns + (-18ns) = 150ns + 2ns - 18ns = 134ns \tag{3.8}$$

As it can easily be observed from the result of the above equation, the original input has been successfully recreated through the calibration procedure.

Stage	1st	2nd	3rd	4th
Nominal Delays	80 ns	40 ns	20 ns	10 ns
Implemented Delays	71 ns	38 ns	16 ns	7 ns
Delay Error	-9 ns	-2 ns	-4 ns	-3 ns
T_{in}	134 ns	63 ns	25 ns	9 ns
Bit in	1	1	1	1
T out	63 ns	25 ns	9 ns	2 ns
Bit out	1	1	1	1
Tin	36 ns	35 ns	3 ns	13 ns
Bit in	1	0	1	0
Tout	35 ns	3 ns	13 ns	6 ns
Bit out	0	1	0	0

Table 3.5: Example of calibration mechanism using a 4-bit unfolded SAR , for a 134ns input (blue) and a 36ns input (green)

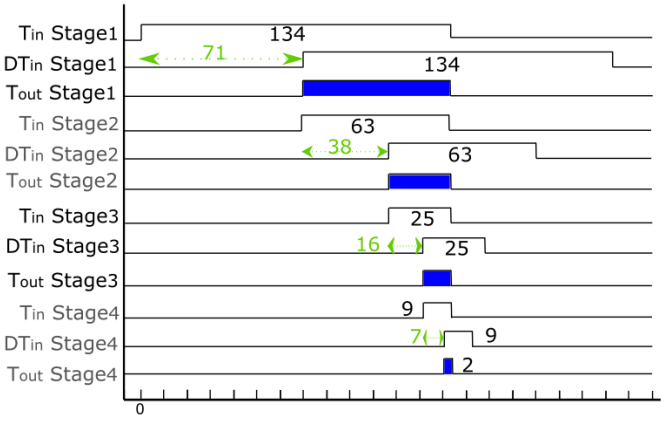


Figure 3.9: Timing diagram of 134ns conversion example of a 4-bit unfolded SAR with 10ns nominal T_{LSB} and delay errors as described in Table 3.5

As the basic idea has now been explained also through a simple example, a more complicated example may be given, in order to explain the importance of the Bit_{in} for the calculation of the correction. The operation procedure of the conversion of an input of 36ns is illustrated in figure 3.10, and Table 3.5. As the delay errors of the stages have already been calculated, the first step of the calibration procedure is not needed. The digital equivalent of the input is $D_{coarse} = 0100$ and the time residue is $T_{residue} = 6ns$. The correction time value is calculated taking into consideration the Bit_{in} of each stage that now is not always 1 (as the previous example) and the values are depicted in Table 3.5. The $T_{correction}$ is given by:

$$T_{correction} = (+1) * (-9ns) + (-1) * (-2ns) + (+1) * (-4ns) + (-1) * (-3ns) \tag{3.9}$$

$$T_{correction} = -9ns + 2ns - 4ns + 3ns = -8ns \tag{3.10}$$

As the Bit_{out} of the last stage is 0, equation 3.6 is used. So we have,

$$Input_{calculated} = D_{\text{coarse}} * T_{LSB,coarse} + \left(T_{LSB,coarse} - T_{\text{residue}}\right) + T_{\text{correction}} \tag{3.11}$$

$$Input_{calculated} = (4 * 10ns) + (10 - 6ns) + (-8ns) = 40ns + 4ns - 8ns = 36ns \tag{3.12}$$

As it can easily be observed from the result of equation 3.12, the original input has been successfully recreated through the calibration procedure.

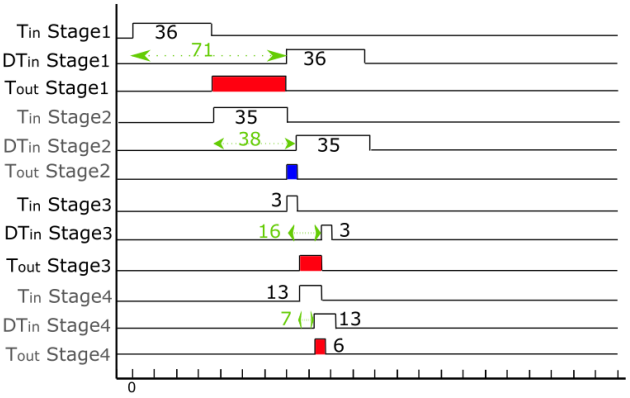


Figure 3.10: Timing diagram of 36ns conversion example of a 4-bit unfolded SAR with 10ns nominal T_{LSB} and delay errors as described in table 3.5

In the above examples, the values used for the residue and correction have not been quantized, as this would introduce a quantization error and it would complicate the explanation of the calibration mechanism. When quantized versions of the time residue and the correction time are used, the reconstructed analog input is not exactly the same as the original input but a quantization error is included.

4

CIRCUIT IMPLEMENTATION

In the previous chapter the system-level design choices were discussed together with the operating principles and challenges introduced by each block. Following this, the transistor level implementation of each block is going to be presented in this chapter. Apart from the circuit description and their operating principles, the performance of the blocks will be also discussed, in order to present the main challenges and considerations regarding each block.

4.1. ANALOG-TO-TIME CONVERTER

The analog to digital converter is one of the most critical components of the implemented ADC as it directly affects the performance of the converter. Firstly, the operating principle of the voltage controlled oscillator and its control block will be presented. The sub-threshold operation of its transistors will be presented and its gain will be derived. The effects of the noise, mismatch, supply voltage on the operation of the ATC, as well as the need for oversampling will be additionally analyzed.

4.1.1. CIRCUIT DESCRIPTION OF RING OSCILLATOR

The ring oscillator is composed of an odd number of cascaded inverters in a feedback topology as the output of the last stage is fed back to the first stage's input. The circuit has no stable operation point as each inverter stage triggers the next inverter stage causing a logical inversion of its output [60]. Due to the odd number of the stages, there is an odd number of inversions causing the circuit to oscillate. The frequency of oscillation is determined by two factors. First, as the signal needs to propagate through the whole chain, the number of inverters (N), inversely affects the oscillation frequency. In the same way, the oscillation frequency is affected by the low-to-high (t_{plh}) and high-to-low (t_{phl}) propagation delays of the inverter stages. This relationship is described by the following formula:

$$f_0 = \frac{1}{T} = \frac{1}{N(t_{phl} + t_{plh})} = \frac{1}{2Nt_d} \tag{4.1}$$

Where t_d is the propagation delay and is given by $t_d = (t_{phl} + t_{plh})/2$. The above equation stands only for the case that the rise and fall times of the delay cells are much smaller than the propagation delays.

In order to convert a ring oscillator to a voltage-controlled oscillator, the oscillation frequency need to be controlled. As it was described by equation 4.1, the way to achieve this, is by controlling the propagation delay of the inverters. The propagation delay of each stage is dependent on the charging and discharging of the intermediate nodes. Assuming all the stages are identical, and thus have the same load capacitance, and the switching threshold of the inverters is $V_{TH,inv}$ the propagation delays are given by:

$$t_{plh} = C_{\text{node}} \frac{V_{TH,inv}}{I_{charge}} \tag{4.2}$$

$$t_{phl} = C_{\text{node}} \frac{V_{DD} - V_{TH,inv}}{I_{discharge}} \tag{4.3}$$

For the case that the switching threshold $V_{TH,inv}$ is equal to VDD/2 and that the two currents are the same and equal to I_D, the propagation time is given by:

$$\mathrm{t}_{plh} + \mathrm{t}_{phl} = \frac{V_{DD} C_{node}}{I_D} \tag{4.4}$$

Thus, the oscillation frequency is given by:

$$f_{\text{osc}} = \frac{1}{N\left(t_{plh} + t_{phl}\right)} = \frac{\mathrm{I_D}}{N \mathrm{C_{ta}} \mathrm{V_{DD}}} \tag{4.5}$$

As depicted in Figure 4.1, each stage is composed of the inverter core (M1 and M2 transistors) and the current starving transistors (M3 and M4).The goal of introducing the top (M4) and bottom (M3) transistors, is to use them as a current source and a current sink respectively. By doing so,the charge and discharge current of the capacitive load can be controlled and thus the oscillation frequency is controlled. The control voltage could be imposed directly on the starving devices, but that would be translated into either the control of only one of the two transitions, or the need for two different control voltages, or different low-to-high and high-to-low transitions for the case both M3 and M4 are controlled by the same voltage. The first case would be translated into half the possible VCRO gain, as only the charging or the discharging current would be controlled. The second case is not practical as it would dictate the need for an extra source. The third one, would be translated into sub-optimal performance as the gain of the input devices would not be maximum for both M3 and M4. A great way to make both the charging and discharging currents the same, without the need for a second source and maximum gain, is the usage of the bias stage composed by transistors M5 and M6 and mirror their current to the current starving devices. By mirroring the current to M3 and M4 transistors, their turn-on resistances are controlled and so are the charging and discharging currents of the nodes.

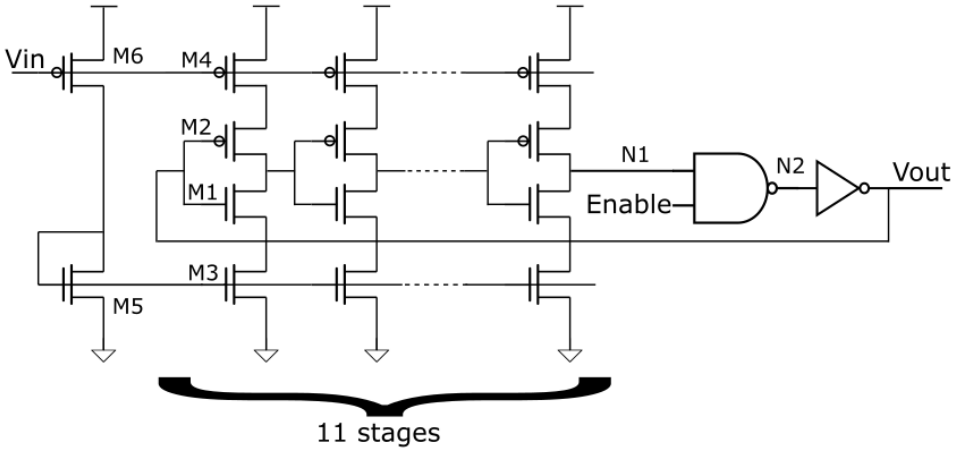


Figure 4.1: Voltage Controlled Ring Oscillator circuit

As it was explained in section 3.1.1, there is the need to be able to stop the oscillator and turn it back on at specific moments. In order to achieve this, the NAND and the extra inverter were introduced and the control voltage "ENABLE" is used. The control sequence is described in Table 4.1. When the enable signal is deasserted, the NAND outputs always a logic high and thus the other input of the NAND (node N1) has no effect and the oscillation signal cannot propagate. This situation results in a broken loop and thus there is no oscillation. However, when the Enable signal is high, the NAND output (node N2) operates as an inverter. The NAND output is always the inverse of the input of the NAND resulting to $\overline{N1}$ and the circuit is free to oscillate.

Enable	Node N2	State
Low	High/Low	Off
High	$\overline{N1}$	free to oscillate

Table 4.1: State control of VCRO

The extra circuit to control the state of the oscillator could have been added to any point of the circuit. However, it was selected to be the last stage due to its increased driving capability and thus faster high-to-low and low-to-high transitions.

4.1.2. ATC GAIN

In order to analyze the gain of the ATC, it is needed to introduce first the basic equations of subthreshold MOS transistor equations. The input transistor operates in weak inversion and its drain to source current is expressed as:

$$I_{DS} = I_S \exp\frac{V_{GS}-V_T}{nU_T}\left[1-\exp\frac{-V_{DS}}{U_T}\right] \tag{4.6}$$

where n > 1 is the slope factor (practically always below 1.6), V_{GS} the gate to source voltage and V_{DS} drain to source voltage, V_T the gate to source threshold voltage and I_S the

specific current given by

$$I_S = 2n\mu C_{ox} U_T^2 W/L \tag{4.7}$$

where μ is the carrier mobility, C_{ox}, the gate oxide capacitance per unit area, $U_T = kT/q$ and W/L the width-to-length ratio of the channel.

From the equation 4.1 it has been clear that the oscillation frequency is linearly dependent on the charging and discharging currents. The two currents in this implementation are equal and described by equation 4.6. The I_{DS} is exponentially dependent on the voltage applied at the gate of the input transistor. This can be also seen at Figure 4.2 that the DC component of the input voltage is swept over the supply voltage range.

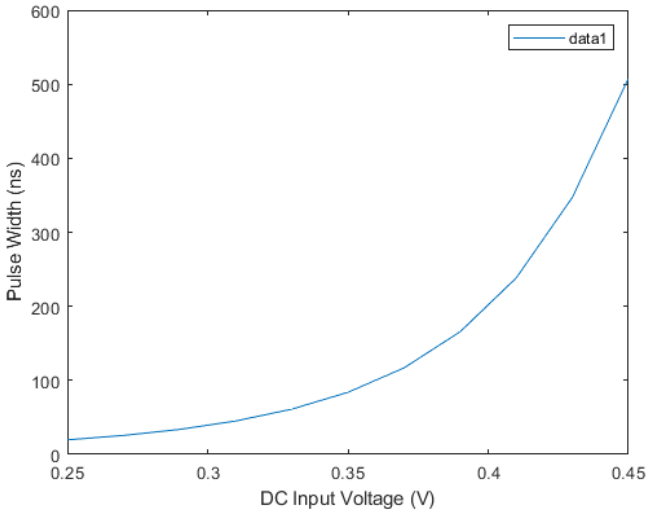


Figure 4.2: Voltage Controlled Ring Oscillator DC input voltage sweep

However, in applications as the one presented in this thesis, that the input voltage range is in the order of mVs, the gain of the ATC can be considered linear and through rearranging the equation and taking the Taylor expansion of the non-constant exponential component, the current equation becomes:

$$I_{DS} = I_S * \exp\left(\frac{V_{DC} + V_{in} - V_T}{nU_T}\right)\left[1 - \exp\left(-\frac{V_{DS}}{U_T}\right)\right] \tag{4.8}$$

$$I_{DS} = I_S * \exp\left(\frac{V_{DC} - V_T}{nU_T}\right)\left[1 - \exp\left(-\frac{V_{DS}}{U_T}\right)\right] * \exp\left(\frac{V_{in}}{nU_T}\right) \tag{4.9}$$

Where the applied input voltage is composed of the V_{DC} and the V_{in} terms. Taking the Taylor series expansion of the above equation:

$$I_{DS} = I_S * \exp\left(\frac{V_{DC} - V_T}{nU_T}\right)\left[1 - \exp\left(-\frac{V_{DS}}{U_T}\right)\right] * \left[1 + \frac{V_{in}}{nU_T} + \frac{1}{2}\left(\frac{V_{in}}{nU_T}\right)^2 + \frac{1}{6}\left(\frac{V_{in}}{nU_T}\right)^3 + \cdots\right] \tag{4.10}$$

As described in section 3.1.2 a differential ATC has been implemented by using two VCROs. This is done in order to get rid of the DC time component as explained earlier and to suppress the even order harmonics that affect the output spectrum. Through re-writing the equation 4.9 in a form that all the non-input dependent terms are included in term "A", we have:

$$I_{DS} = A * \exp\left(\frac{V_{in}}{nU_T}\right) \tag{4.11}$$

For the two inputs $V_{in,p}$ and $V_{in,n}$, we have:

$$I_{DS,p} = A * \exp\left(\frac{V_{in,p}}{nU_T}\right) = A * \left[1 + \frac{V_{in,p}}{nU_T} + \frac{1}{2}\left(\frac{V_{in,p}}{nU_T}\right)^2 + \frac{1}{6}\left(\frac{V_{in,p}}{nU_T}\right)^3 + \cdots\right] \tag{4.12}$$

And

$$I_{DS,n} = A * \exp\left(\frac{V_{in,n}}{nU_T}\right) = A * \left[1 + \frac{V_{in,n}}{nU_T} + \frac{1}{2}\left(\frac{V_{in,n}}{nU_T}\right)^2 + \frac{1}{6}\left(\frac{V_{in,n}}{nU_T}\right)^3 + \cdots\right] \tag{4.13}$$

The resulting time pulse width for the ATC is the absolute result of the subtraction of the two time pulses of the ATCs and it is described by:

$$T_{\text{out}} = \left|T_{\text{out},p} - T_{\text{out},n}\right| = \left|\frac{N * C_{\text{tot}} * V_{DD}}{I_{DS,p}} - \frac{N * C_{\text{tot}} * V_{DD}}{I_{DS,n}}\right| \tag{4.14}$$

By using equations 4.12 and 4.13 the output pulse is given by:

$$T_{\text{out}} = \frac{(N * C_{\text{tot}} * V_{DD})}{A} * \left|\frac{1}{1 + \frac{V_{\text{in},p}}{nU_T} + \frac{1}{2}\left(\frac{V_{\text{in},p}}{nU_T}\right)^2 + \frac{1}{6}\left(\frac{V_{\text{in},p}}{nU_T}\right)^3} - \frac{1}{1 + \frac{V_{\text{in},n}}{nU_T} + \frac{1}{2}\left(\frac{V_{\text{in},n}}{nU_T}\right)^2 + \frac{1}{6}\left(\frac{V_{\text{in},n}}{nU_T}\right)^3}\right| \tag{4.15}$$

Where $V_{in,p} = -V_{in,n}$. As the DC bias voltage is included in the "A" term, we get:

$$T_{\text{out}} = \frac{(N * C_{\text{tot}} * V_{DD})}{A} * \left|\frac{\frac{2V_{\text{in}}}{nU_T} + \frac{2V_{in}^3}{6(nU_T)^3}}{1 - \frac{1}{12}\left(\frac{V_{\text{in}}}{nU_T}\right)^4 - \frac{1}{36}\left(\frac{V_{\text{in}}}{nU_T}\right)^6}\right| \tag{4.16}$$

Thus, the resulting output pulse, after eliminating the higher order terms is given by:

$$T_{\text{out}} = \frac{(N * C_{\text{tot}} * V_{DD})}{I_S * \exp\left(\frac{V_{DC} - V_T}{nU_T}\right)\left[1 - \exp\left(-\frac{V_{DS}}{U_T}\right)\right]} * \frac{2V_{\text{in}}}{nU_T} \tag{4.17}$$

By combining the above equation with equation 4.1, the result is that the oscillation frequency, and thus the resulted output time pulse is linearly dependent to the input voltage for the desired input range. For the presented implementation, the simulation results that support the above analysis are presented in Figure 4.3.

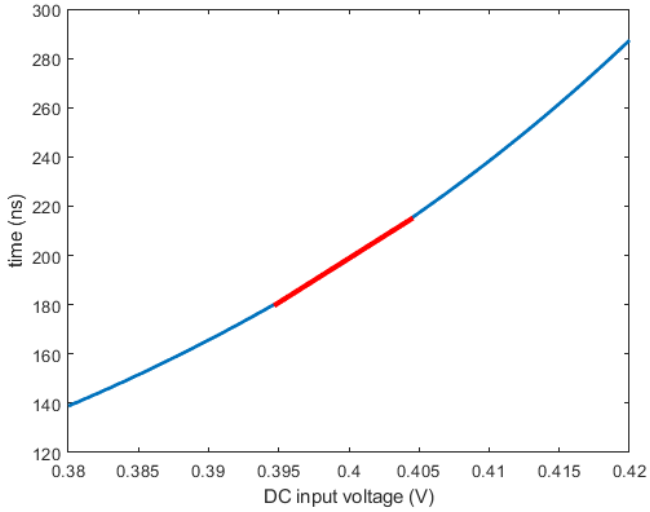


Figure 4.3: Voltage Controlled Ring Oscillator DC input voltage sweep around the selected DC operation point

In order to implement a VCRO that operates as an analog-to-time converter for a time-mode ADC, it is of vital importance to take into consideration the noise contribution of the circuit, as it can limit the resolution of the whole converter. In this analysis, two main noise components are taken into consideration, the white noise and the flicker noise. The basic principle is that the voltage variations due to noise result into timing uncertainty at the edges of the resulted time pulses. This occurs as the intermediate capacitance in each inverter stage, integrates the noise over the propagation delay period of the inverter, and so the instant of the threshold crossing of the next stage varies.

For the following white-noise analysis if was assumed that a positive input is supplied to a single inverter stage, there are two main noise contributions, firstly the white noise of the on-device (NMOs) and the channel noise due to the off-transition (PMOS).

$$\sigma^2_{t_{dN}} = \frac{4kT\gamma_N t_{dN}}{I_N (V_{\mathrm{DD}} - V_{tN})} + \frac{k\,\mathrm{TC}}{I_N^2} \tag{4.18}$$

The first component is due to the thermal noise at the channel of the on-device and the second term due to the dump of the charge of the channel of the off-device.

As the VCRO is composed of N cascaded inverters, the total period has a jitter affected both by the pullup stages and the pulldown stages resulting in:

$$\sigma^2_\tau = N\left(\sigma^2_{t_{dN}} + \sigma^2_{t_{dP}}\right) = \frac{\mathrm{kT}}{I f_0}\left(\frac{2}{V_{\mathrm{DD}} - V_t}\left(\gamma_N + \gamma_P\right) + \frac{2}{V_{\mathrm{DD}}}\right) \tag{4.19}$$

From the above equation, useful conclusions can be made for the design of the VCRO's noise performance. Firstly, the higher the supply voltage, the better it is, as the noise is inversely proportional to VDD. Secondly, the higher the current and thus the power consumption, the lower the noise is. Finally, the number of stages does not affect directly the

noise, but the oscillation frequency and thus the noise. In other words, the noise performance of two VCROs that have the same oscillation frequency but different number of stages is the same [61].

Another important form of noise that has been taken into consideration while designing the VCRO is the flicker noise. Flicker noise is qualitatively different, as the pull-up and pull-down currents contain flicker noise that does not fluctuate over a single transition, but slowly over many. The flicker noise contributes to jitter and is given by:

$$\sigma_\tau^2 = \frac{C_{ox}}{8NIf_0}\left(\frac{\mu_N K_{fN}}{L_N^2} + \frac{\mu_P K_{fP}}{L_P^2}\right) \tag{4.20}$$

From the above equation, useful conclusions can be made for the design of the VCRO's noise performance. Firstly, the higher the current and thus, the power consumption, the lower the noise is. Moreover, increasing the length of the channel reduces the flicker noise. Finally, increasing the number of stages affects, for a constant current, reduces the effect of flicker noise to jitter [61].

Taking the above design conclusions into consideration, an ATC with noise behavior sufficient for the demands of the application has been designed. The noise behaviour of the implemented ATC, when no input is applied, is shown in Figure 4.4. The ATC has a jitter of 0.57ns and an SNR of 27.1dB. The 2048 points Fast Fourier Transform (fft) of the output pulse of the ATC for an input signal of 1 kHz is depicted in Figure 4.5.

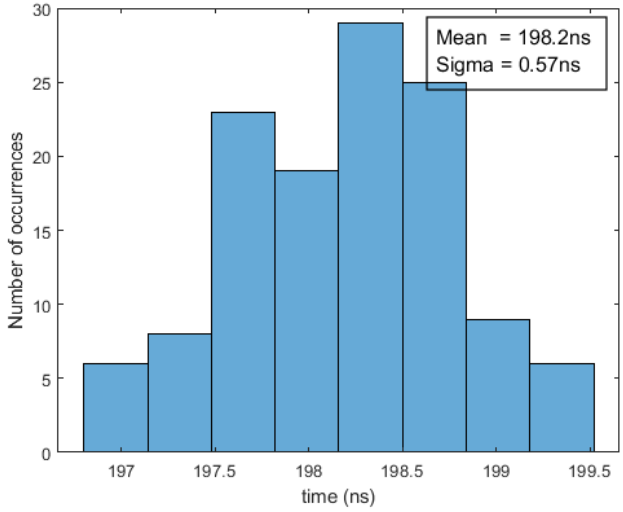


Figure 4.4: Noise simulation of Analog-to-Time Converter

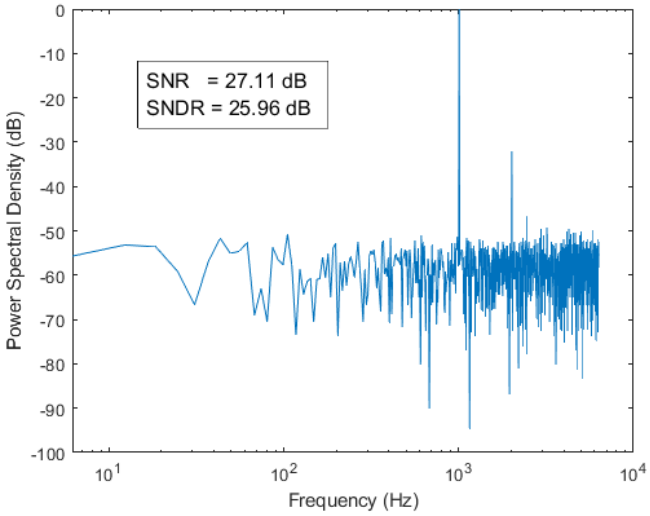


Figure 4.5: Fast Fourier Transform (fft) of the output pulse of the ATC

4.1.3. OVERSAMPLING

Achieving the desired resolution for a 10-bit analog-to-digital conversion, creates performance demands from each individual block of the implemented converter. In the case of the analog-to-time converter, the desired resolution performance, creates a demand for a 10-bit accurate conversion. As analyzed in section 3.1.1, the performance of the ATC could be improved by increasing the supply voltage and the charging and discharging currents. However, in a biomedical application, where energy efficiency is vital, such an approach is not ideal. The best approach would be to take advantage of the properties of the bio signals that need to be converted and find an alternative solution. The low amplitude and frequency of the application targeted signals, together with the time-mode implementation, allow to employ oversampling in a simple and energy efficient way.

Oversampling is the technique where the performance of a converter is improved through averaging the converter output over several samples. As explained in [62], when sources of errors or nonlinearities that follow a gaussian distribution are averaged, the performance is improved by 3dB for every doubling of the number of samples that are averaged. The number of samples taken to create the averaged conversion result, is called oversampling ratio (OSR). This is due to the fact that the output pulse is given by equation 4.21, as it is the adition of OSR times the initial time pulse, and the noise is given by 4.22, due to the addition of the power of the noises sources. The technique of oversampling brings another added benefit. As an OSR number of samples are taken to convert one value, the bandwidth of the converter decreases by the OSR factor as described in equation 4.23. Given the low frequency components that are of interest in biopotential signals, and the high bandwidth of the implemented ATC, the bandwidth reduction due to oversampling, not only does not limit its performance but it also operates as a

filter for higher frequency components. The oversampling mechanism is implemented in the ATC control block as explained in section 3.1.2 by encoding an OSR number of converted pulses within the rising and falling edges of the final output pulse. The OSR of the ATC has been designed to be programmable, in order to allow the achievement of the desired resolution under process variations. Moreover, the OSR can be increased further, if there is the need for a longer output pulse that fits the TDC delays under process variations as it is explained in section 4.5.

$$T'_{\text{out}} = OSR * T_{\text{out}} = OSR * \frac{(N * C_{\text{tot}} * V_{DD})}{I_S * \exp\left(\frac{V_{DC}-V_T}{nU_T}\right)\left[1-\exp\left(-\frac{V_{DS}}{U_T}\right)\right]} * \frac{2V_{\text{in}}}{nU_T} \tag{4.21}$$

$$N'_{ATC} = OSR * N_{ATC} \tag{4.22}$$

$$BW'_{ATC} = \frac{BW_{ATC}}{OSR} \tag{4.23}$$

As the MSB of the ADC conversion is obtained from the phase detector, the desired resolution for the converter is reduced to 9 bit in order to obtain a 10-bit accurate result, meaning that a 56dB accurate conversion is needed. The effect of the applied oversampling for a single ATC is depicted in Table 4.2, where the SNR and SNDR of the converter for different OSR values are presented. As it can be easily observed in the table, the oversampling technique is reducing the noise with almost 3dB for every doubling of the OSR but the harmonic distortion of the VCRO dominates the accuracy of the conversion, limiting it to 32 dB. This can also be observed in Figure 4.6, where the fft plot of the single ATC for an input signal of 10mV peak-to-peak at 1kHz and an OSR of 512 is presented.

OSR	SNR (dB)	SNDR (dB)
1	27.11	25.96
2	30.01	27.76
4	33.21	29.66
8	35.87	30.46
16	38.57	30.98
32	41.49	31.41
64	44.14	31.59
128	46.57	31.67
256	48.35	31.70
512	50.64	31.73

Table 4.2: Effect of oversampling ratio on the conversion performance of the single ended ATC

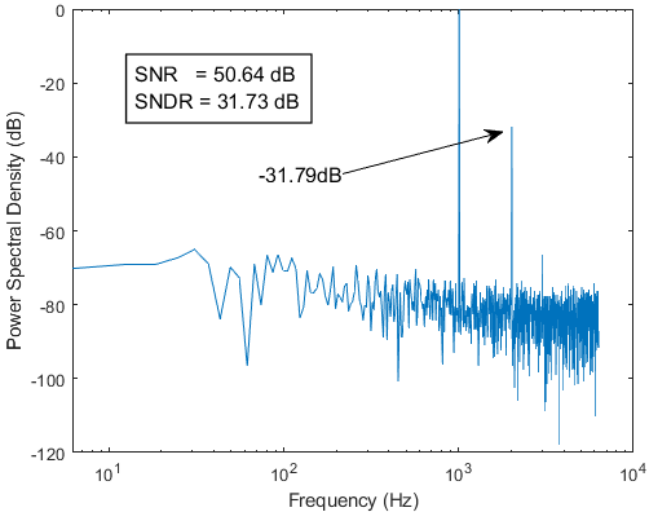


Figure 4.6: Fast Fourier Transform of the output pulse of the VCRO for an 1kHz input signal and an OSR of 512.

As it can be seen in Figure 4.6, the second harmonic is not suppressed by the oversampling and it limits the resolution of the whole converter. In order to circumvent this limitation, the differential ATC has been implemented so that the even order harmonics are suppressed. In Table 4.3, the effect of the applied oversampling for the differential ATC is depicted, where the SNR and SNDR of the converter are shown for different OSR values. As it is easily observed both from Table 4.3 and Figure 4.7, the performance of the converter is not limited anymore from the harmonic distortion of the VCRO. In Figure 4.7 the fft plot of the differential implemented ATC for an input signal of 10mV peak-to-peak at 1kHz and an OSR of 128 is depicted.

OSR	SNR (dB)	SNDR (dB)
1	30.30	30.25
2	33.36	33.32
4	36.32	36.27
8	39.60	39.53
16	42.88	42.83
32	45.79	45.69
64	48.59	48.47
128	51.31	51.11

Table 4.3: Effect of oversampling ratio on the conversion performance of the differential ATC

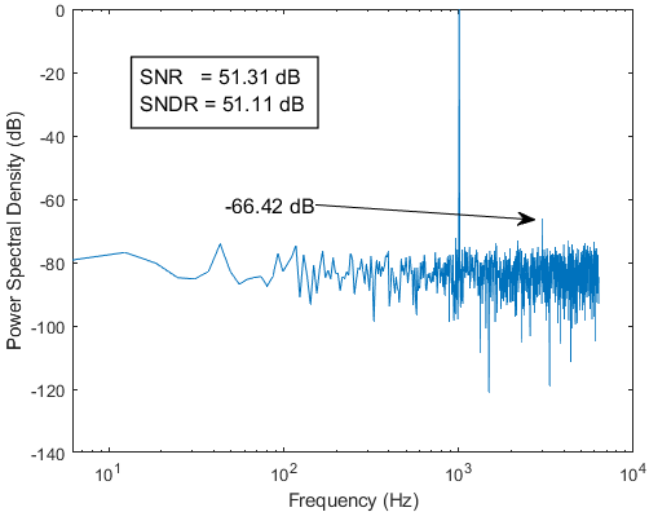


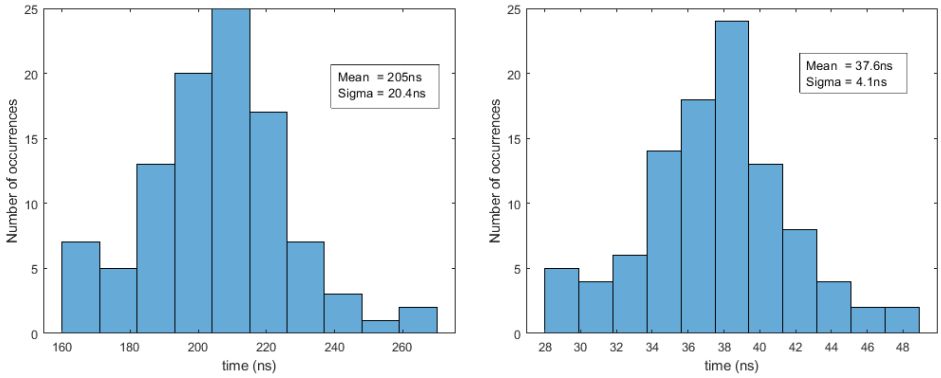
Figure 4.7: Fast Fourier Transform of the output pulse of the differential ATC for an 1kHz input signal and an OSR of 128.

4.1.4. MISMATCH

As the implemented ATC is composed of two VCROs that employ pMOS transistors to modulate the charging and discharging currents of the internal inverters and thus the voltage-controlled modulation, the circuit is affected by mismatch due to process variation effects. The mismatch will cause a threshold voltage variation at the input devices and thus it will cause a gain error. The error introduced by mismatch is inversely proportional to the area of the input devices as described in [63] and it is described by:

$$\sigma^2(V_T) \propto \frac{1}{WL} \tag{4.24}$$

In order to reduce the effect of mismatch, large input devices should be used together with increasing the number of stages and thus the effective area of the input transistor.As described by 4.24 the effect of mismatch is reduced proportionally. However, the number of the stages of the VCROs cannot be increased freely, as the oscillation frequency and the gain of the ATC are affected as well, as described in equations 4.1 and 4.17. Moreover, the number of stages is proportional to the power and area consumption. The effects of mismatch in the output pulse of the ATC, when no input is applied, are presented in Figure 4.8a. The mismatch of the ATC is not going to affect only the DC component of the time output, but also the gain of the ATC and thus its output range. The effects of the mismatch in the output range are depicted in Figure 4.8b.



(a) DC time component

(b) Output time range

Figure 4.8: Mismatch effects on ATC

4.1.5. LAYOUT IMPLEMENTATION

The ATC is composed of the two VCROs and the ATC control block as illustrated in Figure 3.2. Ideally, all the implemented layout cells should have dimensions fitting the dimmensions set by the standard cell library provided from the foundry, in order to be easily placed and routed in a digital design flow. However, as the designed ATC, employs current starved inverters with both high threshold and low threshold transistors, the restrictions regarding the height of the cells could not be met. The resulting VCRO layout is depicted in Figure 4.9. The dimensions of the implemented VCRO are 7.1um*12um.The sizes of the transistors are listed in Table 4.4, where the names of the transistors are shown in Figure 4.1.

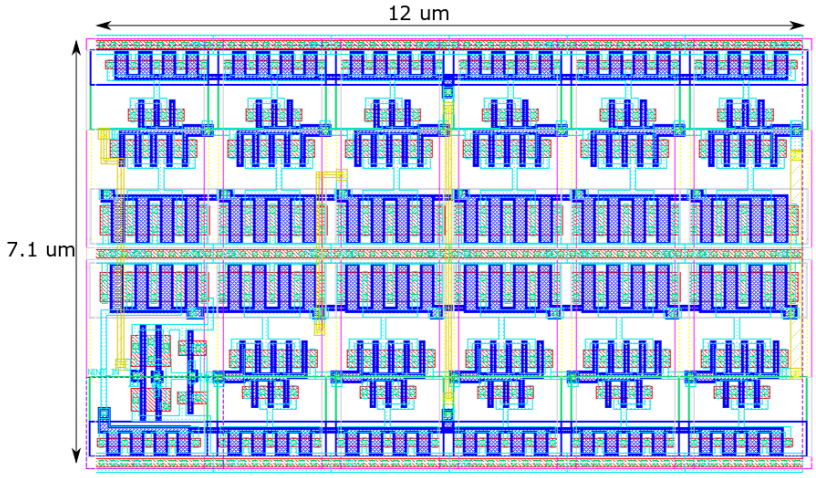


Figure 4.9: Layout of VCRO with enable circuitry

Transistor Name	Type	Width (nm)	Length (nm)
M1	nch_hvt	600	65
M2	pch_hvt	1500	65
M3	nch_lvt	600	200
M4	pch_lvt	2000	200
M5	nch_lvt	600	200
M6	pch_lvt	2000	200

Table 4.4: Voltage Control Ring Oscillator transistor properties

The ATC layout with its extracted parasitic capacitances has been simulated in order to compare its performance with the pre-layout. In Table 4.5, the comparison of the two is found. As can be easily observed, the two results deviate greatly.

	pre-layout	post-layout
DC time component	200ns	752ns
Output time range	36ns	203ns

Table 4.5: CD time component and output pulse time range pre-layout and post-layout comparison.

This increase in both the DC time component and the time range of the converted output pulse occurs mainly due to two reasons. Firstly, due to the well proximity effect, the input transistors experience an increase in their threshold voltages and they are pushed further into the subthreshold region. The result of this is a reduction in the charging and discharging currents of the inverters. As it can be seen from equation 4.1 such a decrease inversely affects the output time pulse. The second reason behind the observed time increase, is the increase of the capacitance in the intermediate nodes due to the extracted parasitic capacitances. As can be seen from equation 4.1, an increase of the capacitance leads to a proportional increase in the converted time pulse. As the operating currents of the ATC are small, make the above-described changes in the ATC circuit to have a dominant effect in the behavior of the circuit. A way to overcome the increase in the output pulse DC component and time range are described in section 4.5.

The ATC control block has been implemented using the digital design flow and its layout implementation is depicted in Figure 4.10. The dimensions of the ATC control block are 19.8um*50um. As the operation of the control block is purely digital, differences between the pre-layout and post-layout simulations are negligible.

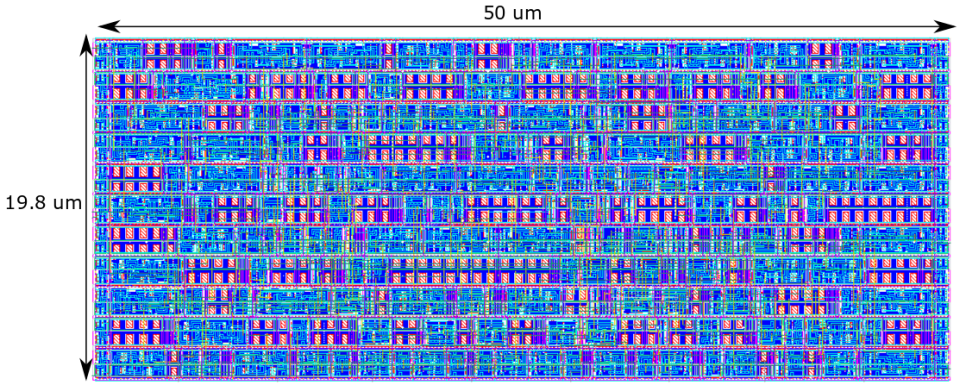


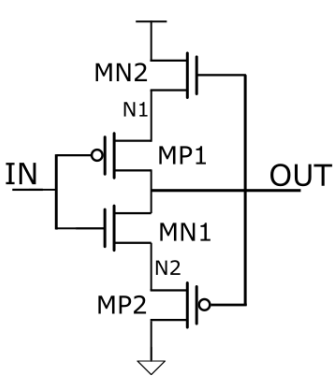
Figure 4.10: Layout of ATC control block

4.2. COARSE TDC

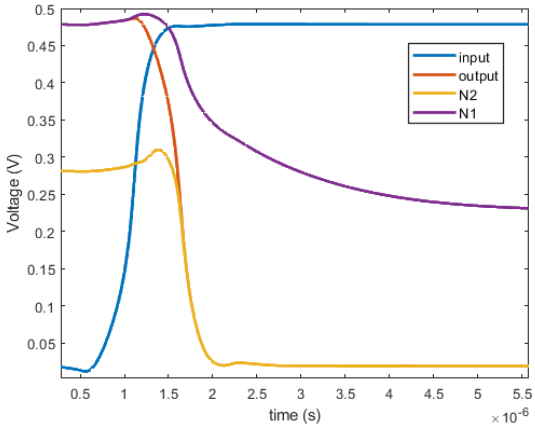
The operation principle of the coarse TDC was analyzed in section 3.1.4. The implementation details of the delay elements is of interest, as they need to be able to create delays at the range of 10^{-6} seconds while their power consumption needs to remain minimal and their performance suitable for the desired accuracy. In order to satisfy the above criteria Dynamic Leakage Suppression (DLS) delay cells have been considered. In [64], [65] DLS logic cells have been used as a way to reduce the standby power consumption to two to three orders of magnitude, at the cost of substantially degrading the speed of the circuit. In [66] DLS logic has been used to implement a wake-up oscillator due to its low standby power consumption and the lack of need for high oscillation frequency. The same reasons led to the selection of such an implementation for the delay cells, as the needed delays are big and the minimizing of power consumption is desired.

4.2.1. CIRCUIT DESCRIPTION

One of the advantages of the DLS logic implementations is the drastic reduction of the stand-by current. In order to proceed with the analysis of the DLS delay cells, Figure 4.11b shows the steady-state voltages when a logic low input is given to the inverter. As the input is low, the output of the inverter is at logic high and the pull-down path should is responsible for any leakage current. By introducing the feedback PMOS device (MP2), whose gate is at a logic high, the node n2 is forced to settle to roughly VDD/2. As the node n2 has settled at VDD/2, both MN2 and MP2 are placed in the super-cutoff region, reducing drastically their leakage currents. The same steady state analysis stands for the case that the input is a logic high, as the feedback NMOS (MN2), forces the node N1 to settle at VDD/2 and puts MN1 and MP1 in the super-cutoff region.



(a) DLS inverter schematic



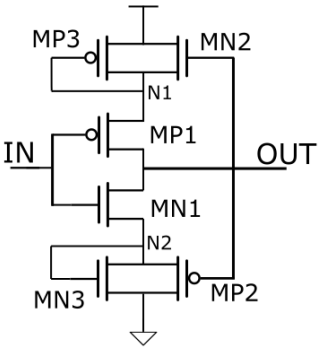
(b) DLS inverter operation

Figure 4.11: Dynamic Leakage Suppression (DLS) inverter schematic and nodes voltages

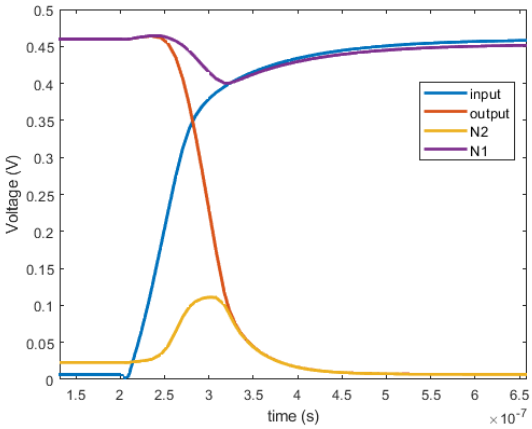
The dynamic operation of the DLS logic is based on the leakage currents of the feedback transistors. Figure 4.11b is used in order to visualize the behavior of the internal nodes and the operation of the transistors. Let's assume that the inverter is at the previously described steady-state with a logic low input, and the input transitions from 0 to VDD. As the gate voltage of MN1 increases, the transistor turns on it is put in weak inversion, driving node N2 to follow the output node voltage. The change at the voltage of node N2, puts MP2 in the cut-off region (previously it was in super cut-off) and the output node and N1 are discharged to some degree as they provide the necessary charge. As N1 and 'OUT' are discharged, MP1 and MN2 are placed in the super-cutoff region. At the same time, the leakage current of the PMOS feedback transistor, continue to discharge node N2 and thus the output node, resulting in faster discharge of the output and bigger reduction of the leakage currents of the pull-up transistors. In the above description, the importance of the MP2 and MN2 should be noted, as their leakage currents are the ones that define the performance of the circuit. For this reason, their sizing is of great importance, as it will define not only the speed of the gate but also, to a certain extend, the rising and falling transition times of the gate. The internal transistors are sized so that the loading of each stage is small and the pull-up and pull-down properties of the internal inverter are similar.

The performance in terms of the power needed for achieving a delay has been outstanding, achieving delays of a few micro second for energy consumption of a few femto Joule. However, there have been drawbacks regarding the process variation effects and the noise performance of the devices. The first one is due to the fact that the inverters operate based on the leakage currents, and thus they are sensitive to threshold voltage shifts, that are caused from process variation. The second one is due to the fact that the delays achieved from the cells are in the order of 10^{-6} seconds, and the rising and falling edges are long. The long edges are translated to a large dt/dV and thus a small voltage noise is translated to a big-time uncertainty and thus jitter.

In order to circumvent these drawbacks, a modification has been made in the presented DLS inverter. Two diode-connected devices have been added in parallel with the feedback transistors. The proposed delay cell is shown in Figure 4.12a. By adding the diode connected transistors, the main changes in the operation of the modified DLS inverter are two. Firstly, the internal nodes N1 and N2 do not settle around VDD/2 but around VDD and VSS respectively, as the parallel connected devices (MN3 and MP3) are not in the cut-off region but they are in weak inversion, pulling the internal nodes almost to the rails. The second difference is due to the fact that there is a path from the intermediate nodes to the supplies, the charging and discharging of the output node does not depend only on the leakage currents of the big feedback devices, but also on the current of the small diode connected transistors. The benefits of adding the MP3 and MN3 transistors comes from faster rising and falling edges, resulting in less jitter. However, the drawback is that the devices consume more power and they have bigger leakage currents. Moreover, because they are much faster, more devices are needed to achieve the desired delay for each stage.



(a) Modified DLS inverter schematic



(b) Modified DLS inverter operation

Figure 4.12: Modified Dynamic Leakage Suppression (DLS) inverter schematic and nodes voltages

For the creation of the delay elements, a series of cascaded modified DLS inverter cells have been used. The values of the achieved delays are listed in Table 4.6. In the same Table the number of modified DLS inverters used to implement the needed delays is includes. Moreover, in this table, the energy dissipation along with the static energy consumption of the delay stages can be found.

Stage	Delay (us)	No. of elements	Energy during delay (pJ)	Static Energy for 1us (fJ)
1st	18.536	370	5.16	270
2nd	9.241	185	1.34	130
3rd	4.627	93	0.359	68
4th	2.318	47	0.1	35
5th	1.174	24	0.031	18
6th	0.572	12	0.011	9

Table 4.6: Coarse TDC stage delay characteristics

In [66] the performance of the DLS inverter over a wide range of supply voltage, is described to be stable with small differentiations on the propagation delay. However, due to the addition of the parallel connected devices, the performance of the modified DLS inverter under a range of supply voltages is affected greatly. As observed in Figure 4.13 there is an exponential decrease, that can be explained with the exponential increase of the current of the parallel connected devices.

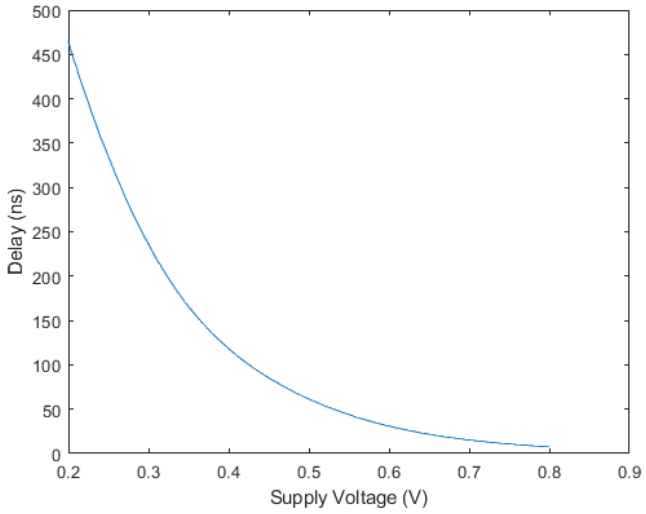


Figure 4.13: Delay of Modified DLS inverter over a variety of supply voltage.

The effect of mismatch due to process variation effects has been highly pronounced in the DLS inverters. The mismatch causes a threshold voltage variation at the feedback devices and thus it affects the performance of the delay elements greatly. The addition of the parallel devices MP3 and MN3 reduces the effects of the mismatch in the delays. The standard deviation of the delay elements under process variations are listed in Table 4.7.

Stage	Sigma (ns)
1st	357
2nd	309
3rd	189
4th	148
5th	97
6th	56

Table 4.7: Mismatch of coarse TDC delay elements.

As the implemented delay elements aim at creating slow transitions and thus big delays, they are affected by noise. This is due to the fact that the rms noise voltage is translated to jitter though the charging/discharging slope of the inverters as described in equation 4.25.

$$\frac{\sigma_V}{\sigma_t} = \frac{dV}{dt} \tag{4.25}$$

The standard deviation of the rms jitter of the six delay elements used in the coarse TDC are listed in Table 4.8.

Stage	Jitter (ns)
1st	9.8
2nd	6.8
3rd	4.7
4th	3.1
5th	2
6th	1.68

Table 4.8: Jitter of the coarse TDC delay elements.

4.2.2. INTERFACE BETWEEN DLS AND STANDARD LOGIC

As the delay elements do not have inherently a rail-to-rail operation and their rise and fall times are big, measures need to be taken to reduce both the static and dynamic power consumption of the following standard cells. In order to achieve this, two main actions have taken place. Firstly, the size of the feedback devices was increased so that the output node settles closer to the rails, causing at the same time faster delay elements. Secondly, an interface between the DLS logic cells and the rest standard logic is introduced in order to minimize the power consumption. The interface is composed of four cascaded high V_T devices, that sharpen the rising and falling edges of the delay cell output, while they achieve rail-to-rail operation. The DLS-interface is shown in Figure 4.14.

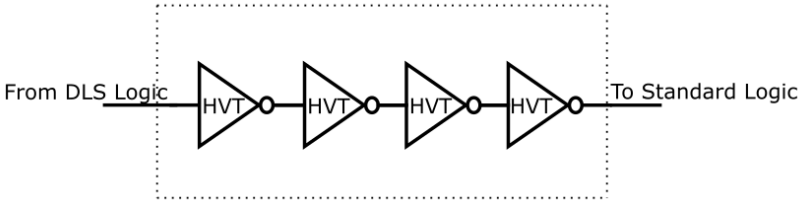


Figure 4.14: Interface between the DLS delay cells and the standard digital cells

4.2.3. GATE NOT FIRING PROBLEM

As analyzed in [55] the coarse TDC resolution limitation is imposed by its dead zone. The dead zone is the time period in which the converter does not have the ability, through the residue generator (XNOR gate), to create an output pulse for small time difference between the falling edge of the input signal (Tin) and the rising edge of its delayed version (DTin). The dead zone of the implemented TDC control logic is from 150ps for non-overlapping Tin and DTin, to 1.45ns for overlapping Tin and DTin. The simulated dead zone range is not a limitation for the implemented TDC, as the TLSB of the whole TDC is an order of magnitude larger, and thus the lack of an output pulse would have the same digital output as the creation of a small pulse. Another possible limitation for the coarse TDC is the error between the expected output time pulse and the time pulse that is measured. The error was simulated and it is +1.9ns for the case of non-overlapping Tin and DTin, and -2.1ns for the case of overlapping Tin and DTin. As the values of this error are much smaller than the T_{LSB} of the whole TDC, they don't impose a limitation. The above values are summarized in Table 4.9.

	Dead Zone	Output Data Error
Overlapping Tin and DTin	1.45ns	-2.1ns
Non-ovelrapping Tin and DTin	0.15ns	+1.9ns

Table 4.9: Dead zone and output data error of implemented coarse TDC

4.2.4. LAYOUT IMPLEMENTATION

The layout of each stage of the coarse TDC is composed of two main blocks, the delay element of the stage and its control block. The layout implementation of the coarse TDC is composed of the cells of the six delay elements and their control blocks. As the control blocks are the same for the 5 first stages, the same cell has been used. The control block of the last stage is slightly different as described in 3.1.4 and for this reason, its layout implementation is slightly different. Ideally, all the implemented layout cells should have dimensions fitting the standards of the library provided by the foundry, in order to be easily placed and routed together. As the designed DLS inverters that are used in the delay cells, employs both high voltage threshold and low voltage threshold transistors, fitting the cell in the standard cell dimensions is not a simple task. The resulting DLS inverter layout is depicted in Figure 4.15 and its dimensions are 1.8um*7.8um. The sizes of the transistors are listed in Table 4.10, where the names of the transistors follow Figure 4.12a.

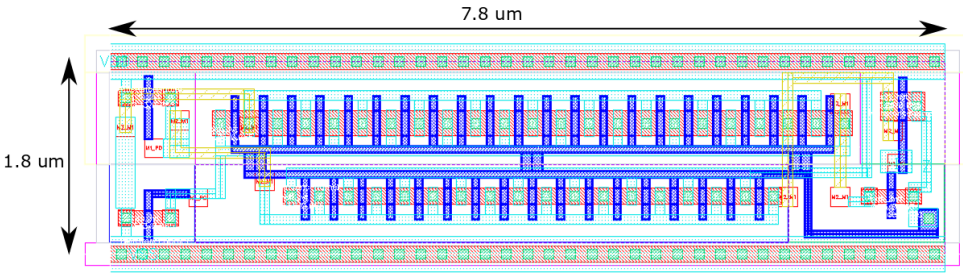


Figure 4.15: Layout of modified DLS inverter

Transistor Name	Type	Width (nm)	Length (nm)
MN1	nch_hvt	130	65
MN2	nch_lvt	2550	65
MN3	nch_lvt	130	65
MP1	pch_hvt	260	65
MP2	pch_lvt	5000	65
MP3	pch_lvt	130	65

Table 4.10: Modified DLS inverter transistor properties

The layout implementation of the delay cells of each stage is similar to each other. The delay cells are composed of the DLS inverters, the DLS-standard logic interface for the four outputs and the multiplexer used to select one of the four elements. The multiplexer selection input depends on the desired resolution. The smallest delay element, the one of the last coarse TDC stage is shown in Figure 4.16. The rest of the delay elements differ only in the amount of the DLS inverter cells used, and they are not presented here.

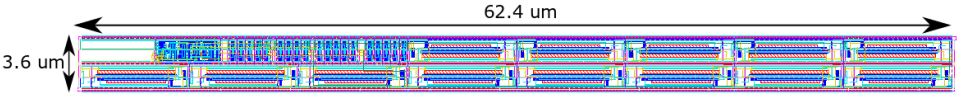


Figure 4.16: Layout of last coarse TDC stage delay

In Table 4.11 the layout dimensions of the eight cells are listed. The delay elements have the biggest dimensions in the whole TDC and they are expected to occupy the biggest area of the layout implementation. In order to have a compact layout, the width of all the delay elements has been kept the same as it will be further explained in section 4.5.

Cell	Height (um)	Width (um)
1st stage delay	84.6	62.4
2nd stage delay	43.2	62.4
3rd stage delay	21.6	62.4
4th stage delay	12.6	62.4
5th stage delay	7.2	62.4
6th stage delay	3.6	62.4
1st-5th stage control	3.6	50
last stage control	3.6	50

Table 4.11: Dimension of coarse TDC cells.

The layout implementation of the coarse TDC delay elements with their extracted parasitic capacitances have been simulated in order to compare their performance with the schematic level simulation results of the delay elements. In Table 4.12, the comparison of the two is made.

Delay Element	Pre-layout Delay (us)	Post-layout Delay (us)
1st stage	18.536	60.885
2nd stage	9.241	30.376
3rd stage	4.627	15.192
4th stage	2.318	7.561
5th stage	1.174	3.722
6th stage	0.572	2.132

Table 4.12: Delay elements of coarse TDC, pre-layout and post-layout comparison.

As can be easily observed from the comparison table, the delays of the post-layout simulation deviate greatly from the designed ones. This increase is mainly due to two reasons. Firstly, due to the well proximity effect, the current limiting transistors experience an increase in their threshold voltages and they are pushed further into the subthreshold region. The result of this is a reduction in the charging and discharging currents of the inverters, resulting in increased propagation delays. The second reason behind the delay increase is the increased capacitance in the intermediate nodes due to the parasitic capacitances. As the delay elements‘ operation is based on the leakage current of the devices and the driving ability of the inverters is low, such an increase in their load capacitance inevitably leads to increased delay times. As it will be described in section 4.5, only the last stage delay needs to be redesigned while the dimensions remain the same.

The implementation of the control block for each stage is shown in Figure 4.17. The layout of the control blocks has been implemented using the standard digital flow. As the control logic of the stages are purely digital, and there are not strict timing restrictions in their operation, their performance difference is negligible as they are able to provide the correct digital output within the desired conversion period.

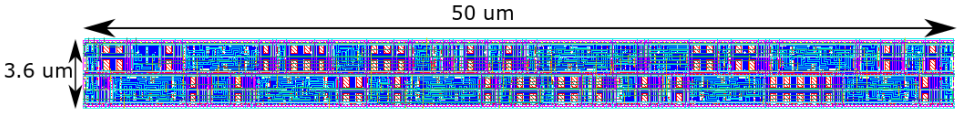


Figure 4.17: Layout of last coarse TDC stage control block

4.3. FINE TDC

For the implementation of the delay cells of the fine TDC, the selection of DLS inverters was not a feasible option, as much smaller delays are needed and the power consumption of the interfaces between the DLS delays and the thermometer coded bit-decision circuit is high. Moreover, the usage of the fine-TDC as the calibration TDC for the coarse TDC, dictates the need for a more robust solution. Apart from the above constraints, there is still the need for low power consumption and relatively high delays, making standard cell delay blocks unattractive. The best candidate to satisfy the above criteria is the current starved inverter. The implemented current starved inverter to act as a delay element is depicted in Figure 4.18. The basic operation principle of the implemented delay cell is that by controlling the available charging and discharging currents of the stage load capacitance, the delay of the inverter can be controlled. The mechanism that controls the delay of the inverter, is that through the control voltage applied to the current limiting devices, the turn-on resistance of the pull-up and pull-down transistors are modulated and so does their delay. In detail, the core inverter transistors (M1 and M2) implement the inverting function of the cell, while the transistors M3 and M4 are operating as a current sink and a current source respectively.

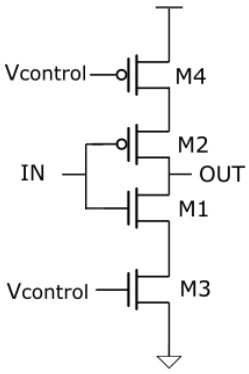


Figure 4.18: Current starved inverter used in the delay element for the fine TDC

One control voltage has been used in order to control the limiting factor of the delay for two main reasons. First, it simplifies the design, as only one source is needed. Second, though the correct sizing of the rest of the circuitry, the effect of fluctuations of the control voltage on the stage delay can be reduced. This is due to the fact that with a higher control voltage the NMOS limiting device sinks more current, leading to smaller high to low propagation delays. On the other hand, the PMOS limiting device sources

more current, leading to smaller low to high propagation delay. As a delay cell is composed of four inverters, the four propagation delays are averaged, leading to a delay value with reduced variation. The above is shown in Figure 4.19.

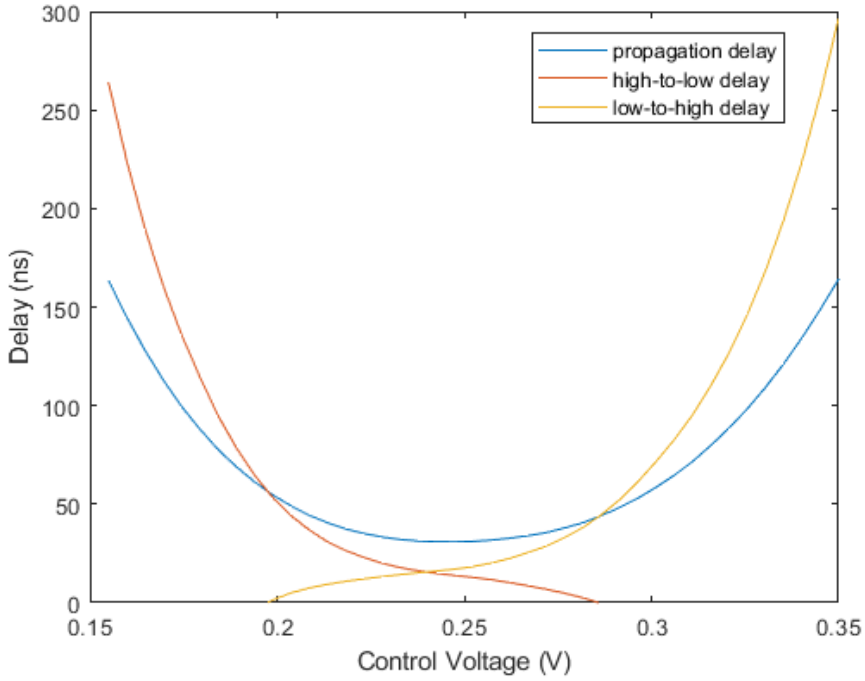


Figure 4.19: Current starved inverter of fine TDC control voltage sweep

The fine TDC does not have limitations regarding its control logic, as the flipflops that generate the start and stop signals can produce a correct output for input time pulses much smaller than the T_{LSB}. However, an offset at the order of a few nano second is added that does not affect the resolution of the TDC as the T_{LSB} is 2 orders of magnitude larger. In the case that the control circuit does not create a start and stop signal, the result of the fine TDC is expected to be 0, and thus no error is introduced.

The performance of the delay element used for the fine TDC delay cells for a wide supply range needs to be characterized. As described by 4.6, the charging and discharging currents show an exponential dependency to the supply voltage, as observed in Figure 4.20 as well.

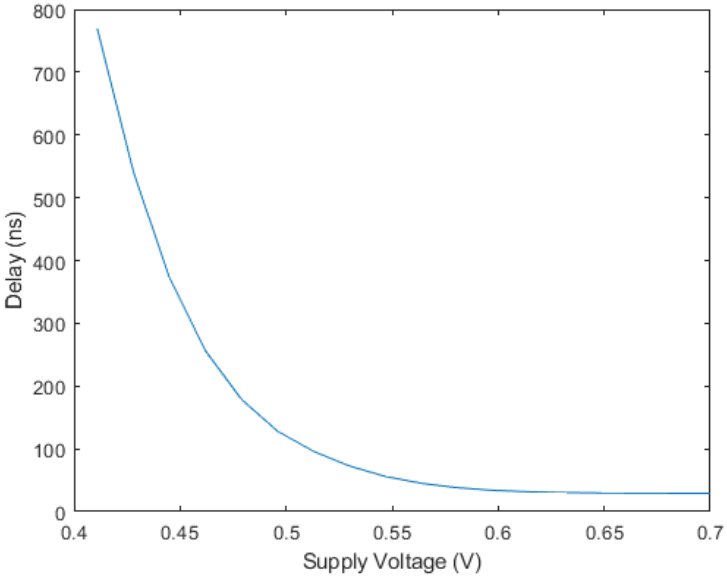


Figure 4.20: Fine TDC stage delay dependency with supply voltage range

The effect of mismatch due to process variation effects needs to be examined for the fine TDC delay elements, as it can affect the performance of the total ADC. The mismatch in the current starved inverters causes a threshold voltage variation not only at the switching threshold of the inverter, but also at the current limiting devices and thus it affects the performance of the delay elements. The standard deviation of the delay elements under process variations is 8.46ns and the histogram of the stage delay is presented in Figure 4.21.

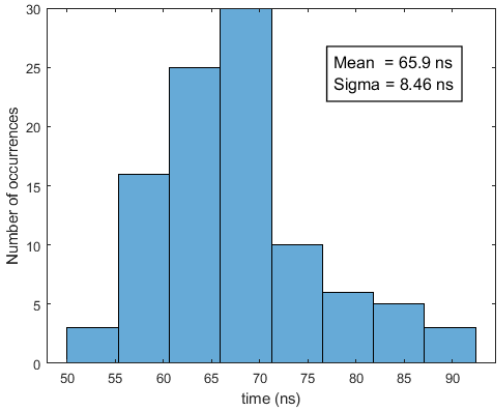


Figure 4.21: Mismatch of fine TDC stage delay

As the implemented delay elements for the fine TDC aim at creating much smaller delays than the modified DLS elements of the coarse TDC, they are affected much less by noise. This is due to the fact that the rms noise voltage is translated to jitter through the charging/discharging slope of the inverters as described in equation 4.25. The histogram of the jitter of the delay element in the fine TDC is depicted in Figure 4.22, where a jitter of 0.56ns is reported.

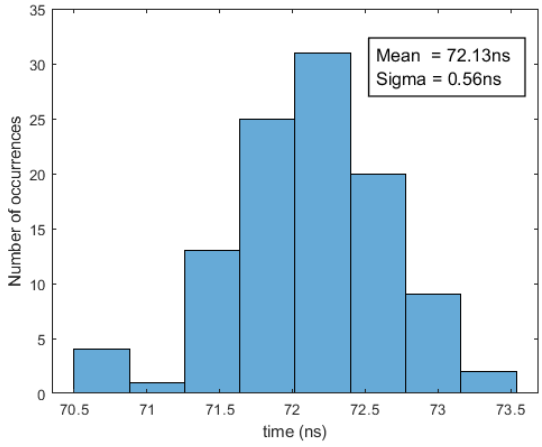


Figure 4.22: fine TDC stage delay jitter

4.3.1. LAYOUT IMPLEMENTATION

The fine TDC is composed of three main blocks. The input stage, the loop counter, the TDC delay elements and their flipflops. The input stage as analyzed in section 3.1.4 is responsible for the creation of the start and stop signal as well as the creation of the new start signal when the signal starts a new loop. The layout of the fine TDC input stage has been implemented using the standard cells provided from the manufacturer library. Its dimensions are 1.8um*13.4um, and it is shown in Figure 4.23.

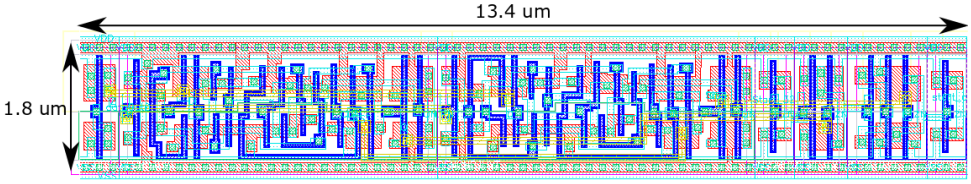


Figure 4.23: Layout of the fine TDC input stage

The counter block, responsible for the enhanced range operation of the TDC, has been implemented using the standard digital flow. Its dimensions are 3.6um*50um, and it is depicted in Figure 4.24. The performance of the input stage and loop counter block post-layout circuit, did not deviate substantially from the pre-layout simulated one.

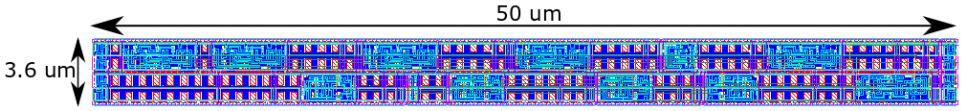


Figure 4.24: Layout of the fine TDC loop counter

The layout implementation of the current starved inverter that is used as the fine TDC delay inverter is presented in Figure 4.25. The dimensions of the cell are 1.8um*1.2um following the standard cell library sizing restrictions. The whole fine TDC employs 32 current starved inverters used as delay elements and four extra current starved inverters that operate as dummy load in order to achieve the desired behavior when the signal is looped. The layout implementation of the flash TDC that is a part of the fine TDC is depicted in Figure 4.26. The size of the implemented cell is 3.6um*60um, following the standard cell layout rules. The sizes of the transistors are listed in Table 4.13, where the names of the transistors follow Figure 4.18.

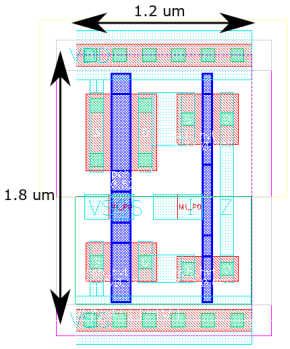


Figure 4.25: Layout of the starved inverter used in the fine TDC delay cells

Transistor Name	Type	Width (nm)	Length (nm)
M1	nch_hvt	170	65
M2	pch_hvt	340	65
M3	nch_hvt	260	130
M4	pch_hvt	520	130

Table 4.13: Transistor properties of the current starved inverter used in the fine TDC delay cells

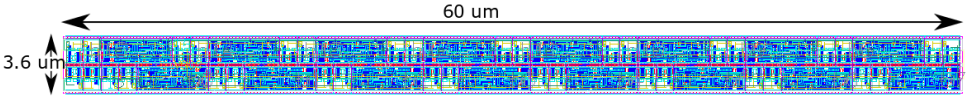


Figure 4.26: Layout of the fine TDC

The layout implementation of the fine TDC with the extracted parasitic capacitances has been simulated in order to compare its performance with the so far simulated results of the pre-layout implementation. In Table 4.14, the comparison of the two is made.

	Pre-layout Delay	Post-layout Delay (us)
Chain Delay	578 ns	1.771 us
T_{LSB}	72.29 ns	221.5 ns

Table 4.14: Delays of fine TDC, pre-layout and post-layout comparison.

As can be easily observed in the comparison table, the delays of the post-layout simulation deviate greatly from the designed ones. The reasons of the simulation result deviation is similar to the reasons that cause the performance change of the DLS inverter. As it is described in section 4.5, changes in the delay elements is not needed for the final operation of the implemented ADC.

4.4. PROGRAMMABLE RESOLUTION

As explained in section 3.2 the resolution of the TDC can be programmed from 8 to 10 bits. In order to achieve this, the OSR of the ATC is modified through the programmable control bits, and the fine TDC delay cells are not affected. However, the coarse TDC delay cells need to have a programmable delay in order to implement the suggested programmable resolution scheme. The structure used to implement the programmable delay is illustrated in Figure 4.27. The basic idea is that the chain of inverters is tapped every $N_{elements}/4$, and the four nodes at $N_{elements}/4$, $2*N_{elements}/4$, $3*N_{elements}/4$, $N_{elements}$ are fed to the DLS-to-standard-cell interface. The outputs of the interface are fed to a multiplexer and through the select bits, the desired delay is achieved. Table 4.15 lists the simulated delay values for the different resolutions.

In Table 4.16 the post-layout delay values for the different resolutions are depicted. The post-layout delays follow the expected $Delay_{stage}/4$, $2*Delay_{stage}/4$, $3*Delay_{stage}/4$, $Delay_{stage}$ ratios.

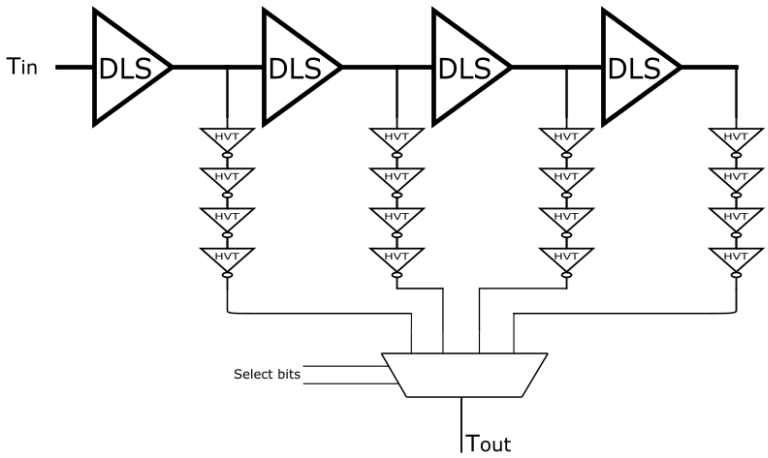


Figure 4.27: Schematic of programmable delay

Stage	Delays for Select=00 (us)	Delays for Select=01 (us)	Delays for Select=10 (us)	Delays for Select=11 (us)
1st	4.635	9.265	13.894	18.522
2n	2.324	4.642	6.963	9.245
3rd	1.180	2.313	3.511	4.624
4th	0.578	1.157	1.745	2.317
5th	0.278	0.578	0.902	1.153
6th	0.120	0.289	0.440	0.560

Table 4.15: Pre-layout coarse TDC delays for programmable resolution

Stage	Delays for Select=00 (us)	Delays for Select=01 (us)	Delays for Select=10 (us)	Delays for Select=11 (us)
1st	15.241	30.480	45.705	60.885
2nd	7.634	15.259	22.886	30.376
3rd	3.882	7.688	11.566	15.192
4th	1.893	3.921	5.739	7.561
5th	0.879	1.902	2.918	3.722
6th	0.545	1.102	1.611	2.132

Table 4.16: Post-layout coarse TDC delays for programmable resolution

4.5. POST-LAYOUT CHANGES

As it has been made clear in this chapter so far, the performance of the converter has been affected in the layout step by the parasitic capacitances. All the blocks of the converter has been designed so that errors like this can be corrected with minimum effort.

First of all, the ATC through the programmable OSR allows the increase of the gain of the converter and achieve higher delays than the nominal, simply by increasing the OSR. An increase in the OSR leads to bigger delays and thus the increase of the T_{LSB} of the TDC. As defined by equation 4.23, with an increased OSR, the bandwidth is reduced. Thus, the limitation is that the new bandwidth of the ATC needs to be bigger than the desired converter bandwidth. The OSR cannot be reduced from its nominal value to achieve smaller delays freely either, as this would be directly translated to a reduction in the performance of the ATC. As the designed ATC achieves a slightly higher SNDR than the required, a small reduction in the OSR is still possible. A second way to change the gain of the converter, is by changing the DC component of the input signal. By doing so, the gain of the input devices is affected in the way observed in Figure 4.2. The alteration of the DC input voltage may seem a straight forward procedure, however such a change affects the noise performance of the VCRO and thus the OSR may need to be modified as well in order to achieve the desired resolution.

The delay elements of the coarse TDC are implemented with programmable delays. The programmable delays as explained in section 3.2 are used in order to implement a programmable resolution feature. However, the option of the delay cells with values of $3 * T_{stagedelay}/4$ has been implemented so that a smaller delay can be achieved. This was done as explained in section 3.3 in order to guarantee the correct operation of the converter under process variations through the calibration mechanism. The selection of one of the above options of the programmable delays could be used in order to achieve a smaller delay and solve the problem of the increased delays.

As the fine TDC is implemented as a flash TDC that uses 2 delay elements to create a T_{LSB} delay, by using the flip-flop in the intermediate node, the resolution of the converter can be altered to $T_{LSB}/2$. Such an approach would allow us to reduce the delay of the stage in half. Moreover, the implementation of the delay elements with current starved inverters, allows to control the achieved delay by modifying the control voltage. The effect of the control voltage at the stage delay is presented in Figure 4.19.

4.5.1. IMPLEMENTED POST-LAYOUT CHANGES

As the redesign of all the above elements used in the time-mode ADC, in order to achieve the already specified performance would be time-consuming, the usage of the above described implemented techniques is desired. As someone can easily notice by observing the delay values of the coarse TDC stages in Table 4.12, all the delays have been almost tripled, due to the increase at the load capacitance of the modified DLS inverters in the same way. Moreover, as can be easily noticed in Table 4.14, the fine TDC delays have also increased in a similar way, as the delays have tripled. This observation can be very useful, as it means that **the TDC delay elements have still the correct ratio, but their absolute value has increased**.

Based on this observation, the new T_{LSB} and the new ideal delays of the stages can be recalculated based on the delay of the first stage of the coarse TDC. The new ideal stage

delays together with the delay error, of the post layout implemented delays are listed in Table 4.17. In the table, it is clear that all the delay elements are within specifications apart from the last stage of the coarse TDC. Thus, a redesign of this delay element is required. The redesign of such an element is not complicated as it only requires the removal of two modified DLS inverters. The new post-layout stage delays are listed in Table 4.18, where it is made clear that all the delay elements are within specifications.

Delay Element	Post-layout Delay (us)	New Ideal Delay (us)	Delay Error (ns)	Delay Error LSB percentage
1st stage coarse	60.885	60.885	0	0
2nd stage coarse	30.376	30.442	66	0.28
3rd stage coarse	15.192	15.221	29	0.12
4th stage coarse	7.561	7.610	49	0.20
5th stage coarse	3.722	3.805	83	0.34
6th stage coarse	2.132	1.902	230	0.97
stage fine	0.2215	0.238	16	0.07

Table 4.17: Post-layout delays, delay errors, new post-layout delays

Delay Element	New Post-layout Delay (us)	New Delay Error (ns)	New Delay Error LSB percentage
1st stage coarse	60.885	0	0
2nd stage coarse	30.376	66	0.28
3rd stage coarse	15.192	29	0.12
4th stage coarse	7.561	49	0.20
5th stage coarse	3.722	83	0.34
6th stage coarse	1.825	77	0.32
stage fine	0.2215	16	0.07

Table 4.18: Re-designed post-layout delays and their errors

So far, the TDC has been modified so that there are not systematic errors in the conversion and all the delay stages are within the specifications. However, as the T_{LSB} of the TDC has tripled, the conversion range of the ATC needs to be modified as well. As explained in section 4.5 one of the options is the increase of the OSR as long as the new bandwidth is sufficient and the power budget allows it. By increasing the OSR from 512 to 600, the new ATC conversion range becomes 600*203ns= 121.8us. For such a conversion range, a TDC with $T_{LSB} = 237ns$ is desired, and from Table 4.17 it can be seen that both the conversion range and the T_{LSB} of the ATC and TDC fit. Thus, the implemented TDC has a T_{LSB} of 238ns.

4.6. CALIBRATION

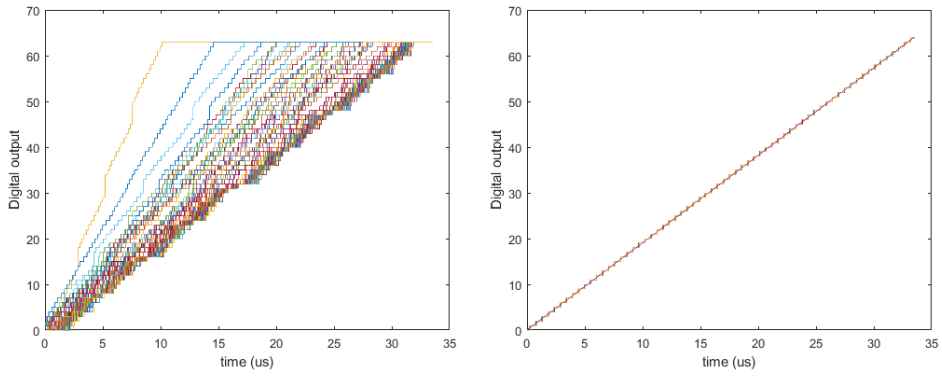
The calibration mechanism was explained and examples showing the operation were given in section 3.3. At this point it is considered useful to show the effects of the calibra-

tion mechanism in the transfer curve of the coarse TDC. As explained in section 4.2 the DLS delay elements are highly affected by the mismatch due to process variation effects and it has been one of the reasons that the circuit has been modified with the addition of the two diode connected transistors. The mean values and standard deviation of the DLS delay elements for 100 samples are listed in Table 4.19. In order to highlight the effect of the calibration mechanism on the linearity of the converter, the data from the original DLS delay elements have been used for the following plots.

Stage	Mean (us)	Sigma (us)
1st	17.346	5.234
2nd	8.673	2.659
3rd	4.310	1.281
4th	2.384	0.714
5th	1.147	0.340
6th	0.523	0.155

Table 4.19: Effects of mismatch on the original DLS delay elements (without the diode connected transistors)

In Figure 4.28a, the transfer curves of 100 samples of the TDC converter are depicted. As can be clearly noticed from the figure, the majority of the transfer curves suffers from offset, gain error, large DNL and INL errors. In Figure 4.28b, the same data-set has been used to plot the transfer curves of the 100 samples after the application of the calibration mechanism. Through the comparison of the two figures, the effects of the calibration mechanism are obvious. Offset and the gain error are removed and there is a drastic improvement in the DNL and INL of the converters.



(a) Before calibration

(b) After calibration

Figure 4.28: Effects of the calibration mechanism on the transfer curve of the coarse TDC under process variation

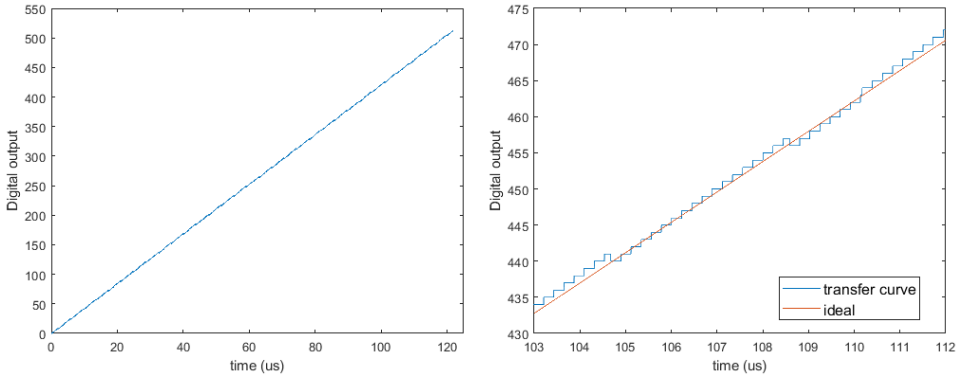
5

SIMULATION RESULTS AND PERFORMANCE EVALUATION

In this chapter, the performance of the implemented ADC is characterized through a variety of performance figures. As analyzed in chapter 2.3, the performance figures are important to understand the characteristics, advantages and imperfections of the implemented ADC. Moreover in this chapter, a comparison between the suggested time-mode ADC for biomedical sensing applications with state of the art ADCs is made.

5.1. TRANSFER FUNCTION

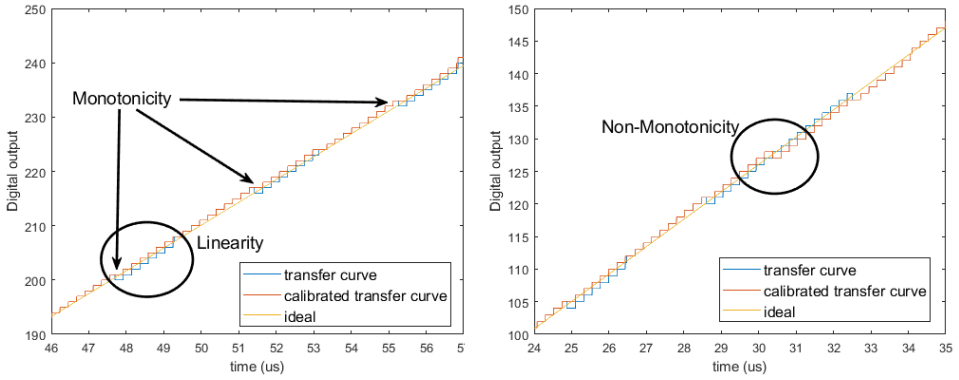
The transfer function of the TDC is useful to understand and characterize the linear imperfections of the static performance of the ADC. The transfer curve of the implemented TDC is shown in Figure 5.1a. As it can be seen in Figure 5.1b that is a sections of the transfer curve plotted in Figure 5.1a, the converter may follow closely the ideal transfer plot but is non-monotonic. The calibration mechanism has been used in order to correct the errors in the transfer curve. As can be seen in Figure 5.2a, the calibration improves the linearity of the converter and reduces the occurrences of non-monotonous behaviour. However, as the calibration is done using quantized information by the T_{LSB} of the fine TDC, the correction cannot be perfect and still occurrences of non-monotonicity exist as depicted in Figure 5.2b.



(a) TDC transfer curve

(b) section of 5.1a highlighting the imperfections

Figure 5.1: Transfer curve of Time-to-Digital Converter



(a)

(b)

Figure 5.2: Effects of calibration mechanism on the TDC transfer curve

5.2. DIFFERENTIAL AND INTEGRAL NON-LINEARITY

As introduced in 2.3, the Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) are two metrics that aim to describe the static performance of a converter and specifically its non-linear distortion. The static performance and linearity of the converter is affected both by the ATC and the TDC. The implemented differential ATC has a linear behavior with a third order component at -66.42dB and for this reason its not expected to affect the linearity of the ADC. This claim ideally should be verified with simulation plots but due to the time duration of the simulations, this is not possible. The DNL and INL of the post-layout TDC are depicted in Figure 5.3 and 5.4. The maximum and minimum values of DNL and INL are +0.86/-0.83 and +0.88/-1.79 respectively.

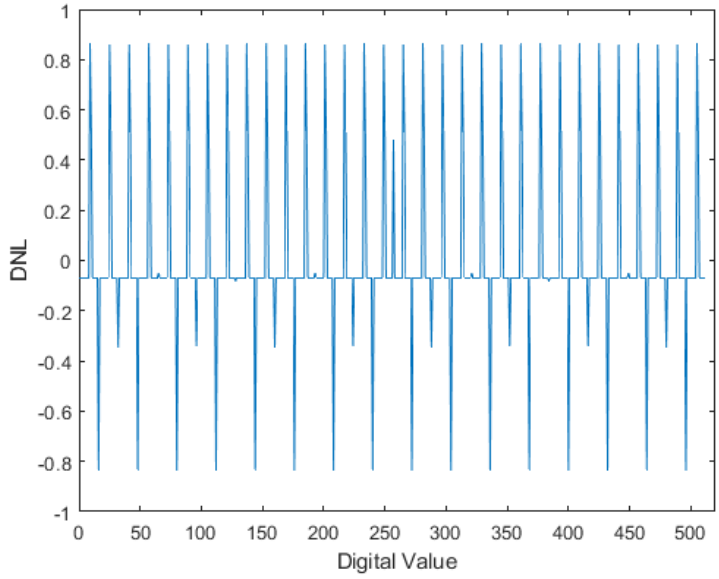


Figure 5.3: Differential Non-Linearity (DNL) of TDC

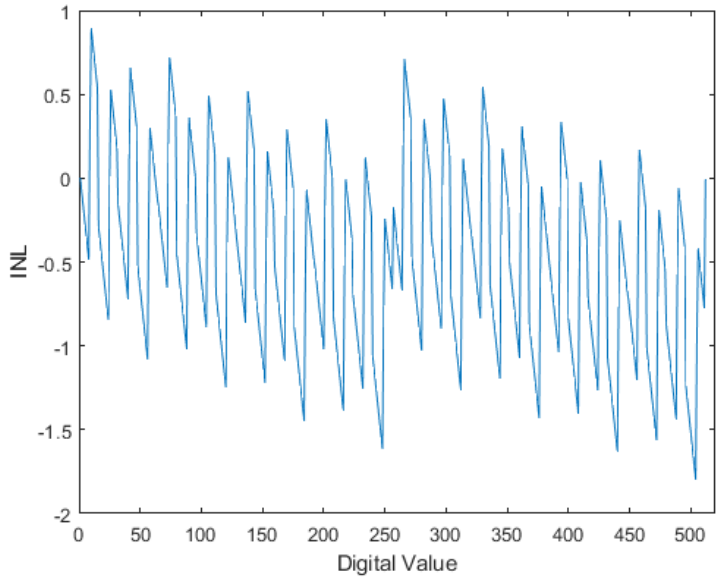


Figure 5.4: Integral Non-Linearity (INL) of TDC

As analyzed in section 3.3, the developed calibration mechanism aims to correct linearity errors due to process variations. However, it is of interest to see the effects of the calibration mechanism on the DNL and INL of the post-layout TDC. The DNL and INL are presented in figures 5.5 and 5.6 respectively. The accuracy of the calibration mechanism is equal to the $T_{LSB}/2$ of the fine TDC as explained in 3.3. Thus, the transfer curve is not perfectly corrected, and it has non-linear distortion.The maximum and minimum values of DNL and INL are +0.86/-0.83 and +0.51/-1.81 respectively. From the comparison of 5.3 and 5.5 the effects of the calibration mechanism become visible. The number of digital codes that experience a big DNL error are reduced, but they are still present due to the quantized value applied to the signal for correction.

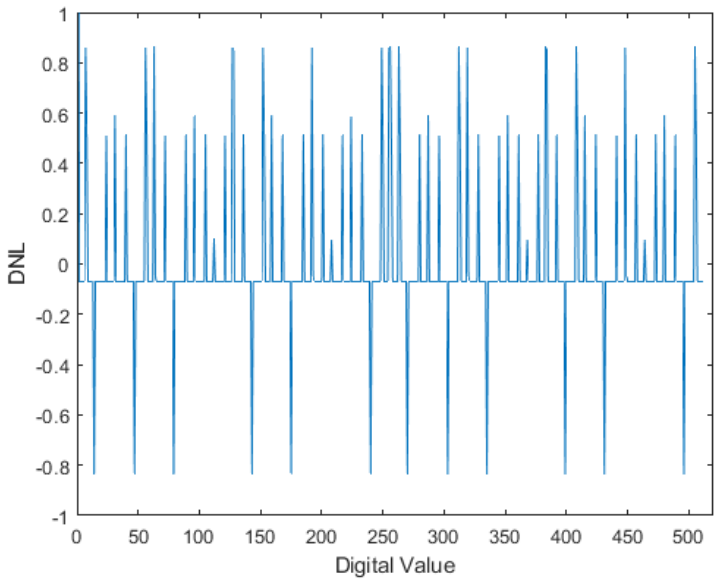


Figure 5.5: Differential Non-Linearity (DNL) of calibrated TDC

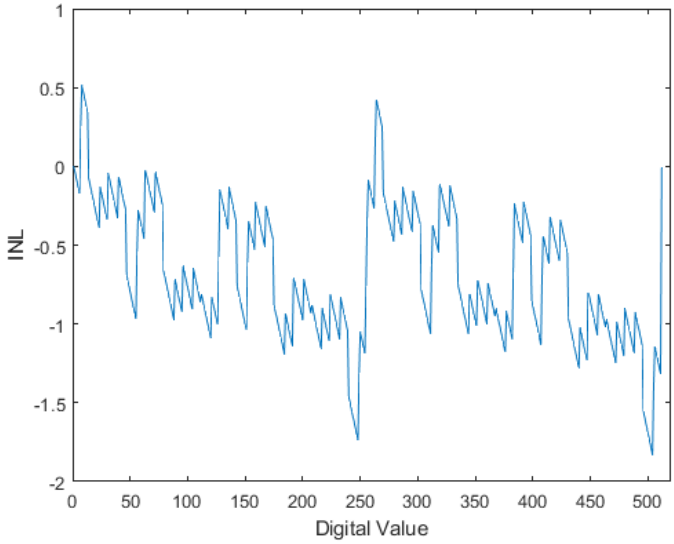


Figure 5.6: Integral Non-Linearity (INL) of calibrated TDC

5.3. DYNAMIC PERFORMANCE AND EFFECTIVE RESOLUTION

In order to characterize the dynamic performance of the converter, a Fast Fourier Transform (FFT) on the output of the analog-to-digital converter is needed. However, an FFT on the output of the analog-to-time converter has been performed. As the noise of the time-to-digital converter is minimal and listed in Table 5.1, its contribution is not substantial. The same stands for the MSB signal obtained from the ATC control block, as its rms jitter is 0.5ns. However, the quantization noise of the TDC and its DNL errors are going to affect the noise floor of the ADC, as described in 5.2 from [14] and set it to $SN_{Q+DNL}R = 61.3dB$. Ideally, this statement should be proven and presented through simulation results. In order to do so and present the FFT of the ADC, a transient noise simulation of the post-layout circuit for 0.98 seconds is needed. Such a simulation was impossible to perform due to the computer run time required.

Stage	Standard deviation (ns)
1st	28.7
2nd	20.3
3rd	12.9
4th	9.1
5th	6.76
6th	4.55
fine	1.41

Table 5.1: Standard deviation of the rms jitter of the post-layout delay elements.

$$\mathrm{SN}_{Q+DNL}\mathrm{R} = 10^{10}\log 2^{(2N-3)} - 10^{10}\log\left(\frac{1}{12} + \frac{\sigma_A^2}{V_{LSB}^2}\right) \tag{5.1}$$

$$\mathrm{SN}_{Q+DNL}\mathrm{R} = 6.02N - 9.03 - 10^{10}\log\left(\frac{1}{12} + \frac{\mathrm{DNL}^2}{2\lambda^2}\right) \tag{5.2}$$

Figure 5.7 shows the 2048 points FFT plot of a 1kHz, 10mV peak-to-peak input signal is shown. The reported SNR is 31.36dB and the SNDR is 31.3 dB, while the higher order harmonics are invisible. In Figure 5.8 the blue plot depicts the FFT of the pre-layout simulated converter and the orange plot depicts the FFT of the post-layout simulated converter. As can be easily observed from the comparison of the two plots, the performance of the ATC has not deviated vastly. A small increase (1dB) in the SNDR of the converter is noticed and is probably due to the increased capacitance in the intermediate nodes due to the parasitic capacitances. The effect of the oversampling ratio is shown in Table 5.2 and it follows the theoretical 3dB improvement for every doubling of the OSR. For the selected OSR of 600, the SNDR of the ATC has been calculated to be 58.18 when a theoretical 55.94 dB is needed.

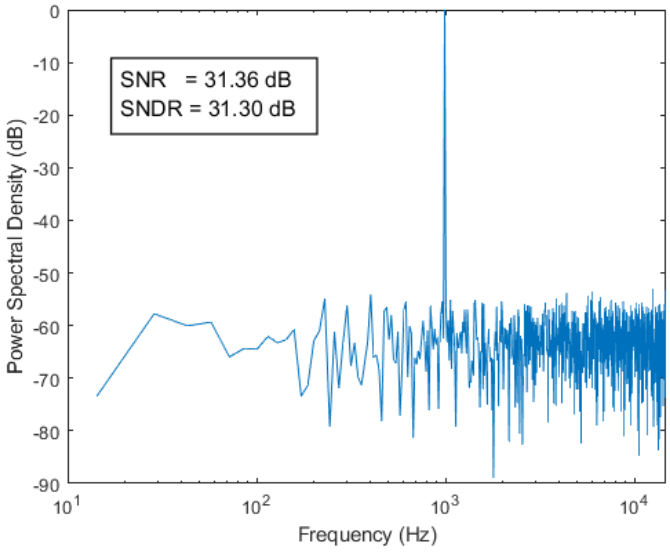


Figure 5.7: Fast Fourier Transform of the output pulse of the post-layout differential ATC for an 1kHz input signal and an OSR of 1

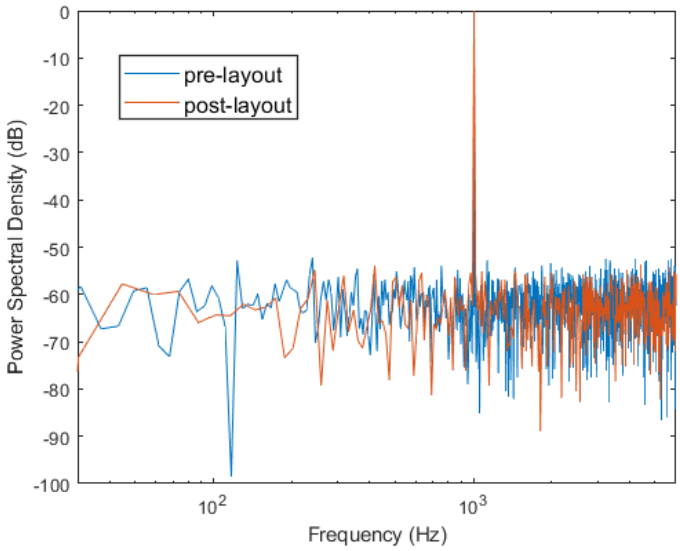


Figure 5.8: Fast Fourier Transform of the output pulse of the differential ATC for an 1kHz input signal and an OSR of 1, for the pre-layout (blue) and the post-layout (orange) circuit

OSR	SNR (dB)	SNDR (dB)
1	31.36	31.30
2	34.31	34.28
4	37.22	36.14
8	40.26	40.09
16	43.13	42.98

Table 5.2: Effect of oversampling ratio on the conversion performance of the post-layout ATC

5.4. POWER

In biomedical sensing applications, the power consumption needs to remain as low as possible. The power consumption of the converter has been an important factor since the beginning of the design and it is 771nW. In Table 5.3 and in the pie chart of Figure 5.9 the power consumption of the various blocks of the converter are illustrated. As can be easily observed, the majority of the power is consumed in the delay elements. It should be noted that the energy consumed during the creation of the delayed input signal 'DTin' is smaller than the leakage energy, as for the majority of the conversion period, the delay elements remain idle. The fact that the leakage energy is dominating the energy needed for a conversion, does not allow to observe the energy reduction due to the reduced resolution.

Resolution	Power (nW)
ATC	89
Coarse TDC	674
Fine TDC	8
Total	771

Table 5.3: Power consumption of the post-layout ADC blocks and total power consumption

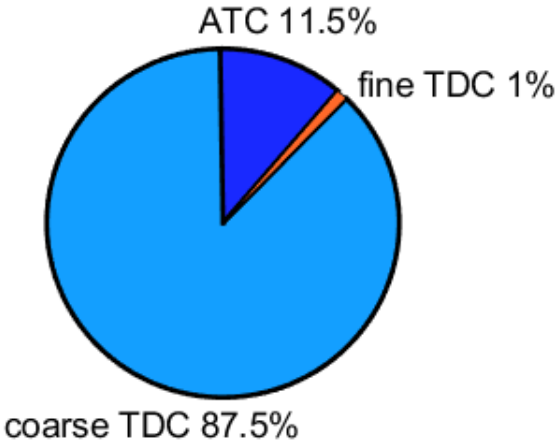


Figure 5.9: Power consumption of the post-layout ADC blocks

5.5. AREA

The area of the ADC components are listed in Table 5.4, along with the total ADC area. In Figure 5.10 the area is illustrated in a pie chart. It is easily observed that the coarse TDC delay elements occupy the biggest part of the ADC area. The total ADC area is $0.01342 mm^2$.

	Area (um^2)	Area (%)
ATC	1160	8.7
Coarse TDC delays	10780	80.3
Coarse TDC control	1080	8
Coarse TDC total	11860	88.3
Fine TDC	396	3
Total ADC	13420	100

Table 5.4: ADC building block and total layout area

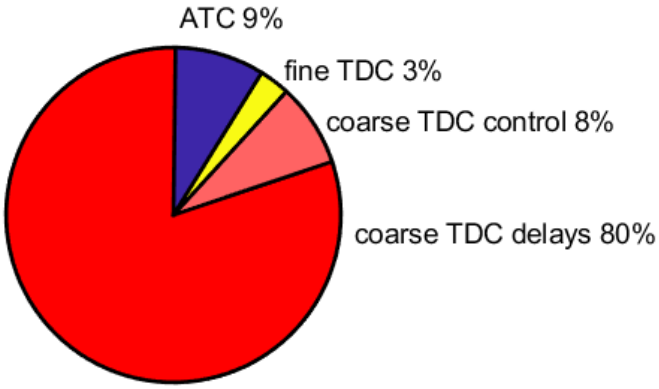


Figure 5.10: ADC layout area pie chart

5.6. COMPARISON

The performance of the ADC is summarized in Table 5.5. In the same table, the designed ADC is compared with state-of-the-art ADCs for biomedical sensing applications. It is important at this point to mention, that this comparison is not entirely accurate, since post-layout simulation results are compared with measurement results. The comparison is made though, as it gives a direction of the possibly achieved specifications.

	[67]	[68]	[69]	[70]	[71]	This Work
Technology (nm)	180	130	65	180	65	65
Resolution (bits)	8	10	6	8	9	10
Supply Voltage (V)	0.5	1	0.5	0.8	0.55	0.5
Input Range (Vpp)	0.25	1	0.25	2.25	NA	0.01
Input Bandwidth (kHz)	2.05	0.5	500	5.1	10	1.1
ENOB (bits)	6.9	9.1	NA	7.9	8.21	9.8
Power (nW)	850	53	650	840	159	771
Area (mm2)	0.11	0.16	NA	0.05	0.191	0.013

Table 5.5: Performance comparison

6

Conclusion and Recommendations

6.1. Conclusion

This master thesis has explored the advantages, limitations and trade-offs in the design of ultra-low energy time-mode ADCs for biomedical sensing applications. A novel ADC architecture has been presented and it is composed of a VCRO based ATC, followed by an asynchronous unfolded SAR coarse TDC and an asynchronous, enhanced range fine flash TDC. As the input is sensed, the ATC embeds the analog information within the time pulse of the output signal. Following, the output time pulse is fed to the TDC that quantizes the pulse and produces the digital equivalent representation of the sensed value. The resolution of the ADC can be programmed from 8 to 10 bits. The delay elements of the coarse TDC are based on a novel modified version of DLS delay elements. Moreover, a novel background calibration mechanism was introduced to correct the errors due to process variation. The calibration removes the offset and gain error of the ADC and achieves DNL and INL reduction.

The VCRO based ATC was selected due to its ability to achieve the desired spectral purity, small size and easy oversampling. The SAR-TDC was chosen due to its small power consumption, sufficient resolution and conversion speed, the fine TDC due to its small size, simplicity, robust design, monotonicity and small power consumption. The selection of the separate parts were made based not only in the individual performance of each part, but taking also into consideration benefits that can arise from their combination. The programmable OSR, implemented in the ATC, allows to fine-tune the generated time pulses to fit T_{LSB} of the TDC. The programmable delays of the coarse-TDC allow the designer to achieve a reduced power consumption by sacrificing the resolution. The fine-TDC, due to its enhanced range, is suitable for calibration and correcting the delays of the coarse TDC.

The integrated circuit has been implemented in a 65nm TSMC process and its per-

formance has been evaluated through Cadence and Synopsys tools. The ADC uses a 0.5V supply voltage and consumes 771 nW for 10-bit resolution. The total area of the ADC is 0.01342 nm^2. The maximum sampling rate is 2.2 KS/s. The DNL and INL of the converter are +0.86/-0.83 and +0.88/-1.79 respectively. The simulation results indicate an ENOB of 9.8 bit for a 10mV peak-to-peak 1kHz input frequency.

6.2. RECOMMENDATIONS

The implemented ADC has shown the low-power capabilities that can be achieved by the combination of time domain signal processing and the selected ATC and TDC architectures. On the same tie, the conclusion imply that more research can be done on this subject and the performance of the system can be further improved. Thus, the list bellow provides the main points of improvement:

- As explained in section 4.5 the ATC discards the DC time component of the VCROs. The DC time component is 4 times the maximum pulse width generated from the ATC as shown in Table 4.5. As only the AC time component is fed to the TDC, the TDC remains iddle for the majority of time. As explained in section 5.4 the static power dominates the conversion power. Thus, by introducing 3 more ATCs, it would be possible to use time interleaving techniques and utilize the TDC during the whole conversion period. Such an approach would increase the bandwidth of the ADC by 4 times and it would give a rise of of 35 percent at the total power consumption.
- The static power consumption of the delay elements dominates the total power of the ADC. The reduction of the leakage currents of the modified DLS inverters would have an impact on the total power consumption. Thus, the introduction of the HVT transistor MN4, as shown in Figure 6.1, is a possible way to reduce the static power consumption. The leakage current reduction is achieved by asserting the $Activate_{Delay}$ signal only during the stage conversion period. The rest of the time, MN4 transistor would be off and it would contribute in the leakage current reduction.

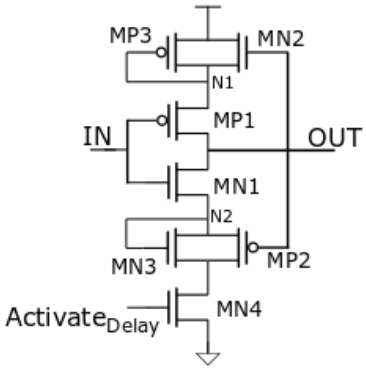


Figure 6.1: Modified DLS inverter to reduce leakage current

- The monotonicity of the coarse TDC and the fine TDC have been achieved and presented in the dissertation. However, as presented in Figure 5.1, when the outputs of the two TDCs is combined, non-monotinicity was observed. The calibration mechanism was applied, and a drastic reduction to the non-monotonicity occurrences has been achieved, as depicted in Figure 5.2. The creation of an additional digital correction circuit that could prevent the non-monotonicity would be of interest.

- The current ADC uses an external signal to obtain the digital outputs of the TDCs. The creation of a completion detection circuit, would be beneficial, as it would be able to create the signal needed for the obtainment of the digital outputs and it would eliminate the need for this external signal. Moreover, a completion detection circuit would allow to achieve lower power consumption if it is combined with the $Activate_{Delay}$ signal of the suggested modified delay element in Figure 6.1.

- The simulations required for the performance evaluation of the ADC make the optimization process of the ADC slow. Highly accurate transient noise simulations for a long simulation time with small time steps are needed. The possibility to evaluate the performance of the ADC through a different methodology would be of interest, as it would allow the speed-up of the process and further optimization.

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