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***Abstract*—The paper proposes an Asymmetrical Modular Multilevel Converter (AMMC) suitable for low/medium-voltage dc-ac conversions with very high output quality. The modules' dc-links of the AMMC are charged to a binary exponential sequence to produce a large number of output levels using only a few modules.**

The concept of using asymmetrical dc-links for high-quality output is not entirely new. However, the practicality of existing approaches is relatively low and challenged by the difficulties in maintaining the required dc-link voltages as well as suppressing their interaction with the output, which often requires multiple isolated dc/dc converters. We solve this problem by aligning the modules in the Marquardt MMC inverter module configuration that offers more control freedom, hence the term AMMC. Furthermore, we introduce a highly effective switched-inductor charge transfer and balancing mode between modules and even across arms. We accordingly modify the underlying conventional chopper modules so that the dc-link voltage control can be completely sensorless. The proposed AMMC is tested in a lab setup with four modules per arm reaching 32 output levels. In contrast to the low benefit of an additional module in MMC due to only linear improvement of the output granularity, each further module halves the finest voltage step. The components to maintain the graded voltage sequence and the underlying inductive charge transfer only a fraction (< 10%) of the load current so that relatively low-power devices can be used.

Keywords—DC/AC applications; high-definition; binary asymmetrical CHBs, modular multilevel converters.

I. Introduction

Modular multilevel converters (MMCs) and similar cascaded converters are in wide use for high-voltage applications, such as high-voltage dc transmission (HVDC) as well as back-to-back links and power quality systems such as static synchronous compensators (STATCOM) [1]–[9]. For various further applications, such as battery storage systems, large photovoltaic systems, and motor drives [10]–[18].

Conventional cascaded and modular multilevel converter often employ a larger number of modules to achieve a high output voltage range beyond the reach of power transistors [19], [20]. As a byproduct, the output quality can be very high. However, modular multilevel converters with a larger number of modules are rarely a practical option for low/medium-voltage applications due to the exorbitant cost, control, and maintenance effort, despite the output quality being a primary concern [21]–[24].

Particularly motor drives and power-quality facilities for harmonics elimination have a strong interest in improving both the temporal resolution, which provides control over a wider spectral bandwidth, and amplitude resolution. Whereas the need to increase the output quality appears obvious for compensation systems to deal with high-order harmonics and inter-harmonics as well as flicker and transients [25], [26], motor drives can particularly suffer from distortion of conventional inverters. The distortion of conventional motor inverters, particularly switching distortion, is responsible for a wide range of adverse effects, such as unnecessary heating, e.g., of magnets in permanent magnet drives and of the lami-

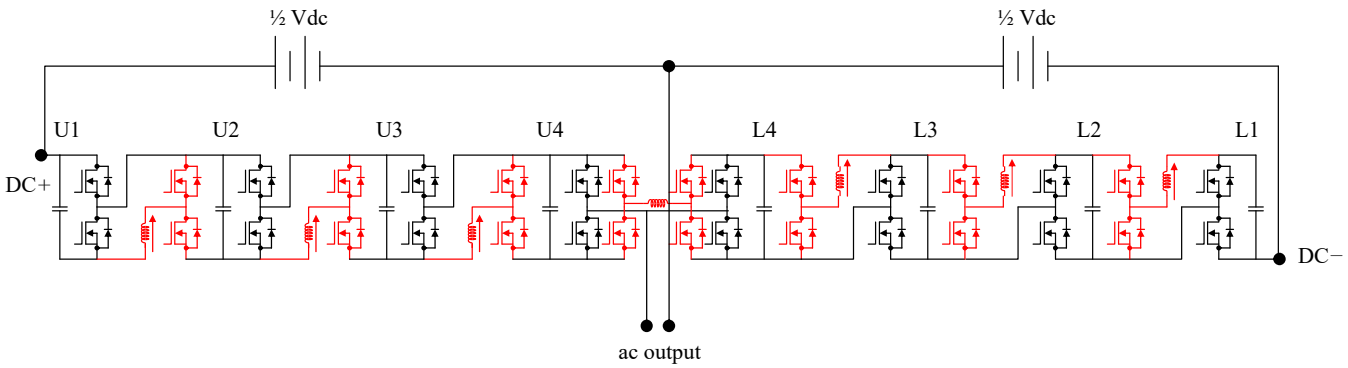

Fig. 1. The proposed single-phase AMMC with autonomous dc-link voltage maintenance. The upper branch is denoted by *U*, and the lower branch by *L*. Black: main current path for output. Red: auxiliary components for trimming the modules' dc-link voltages.

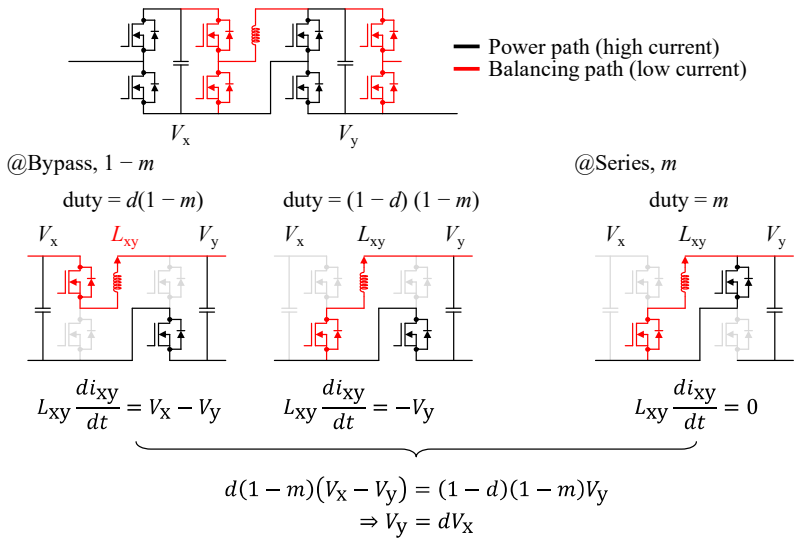

Fig. 2. (a) An ACHB with self-balancing ability. The converter includes auxiliary dc/dc circuits (red) to ensure a voltage step of 2:1. (b1, b2) Two dc/dc switching states contribute to the voltage ratio of 2:1.

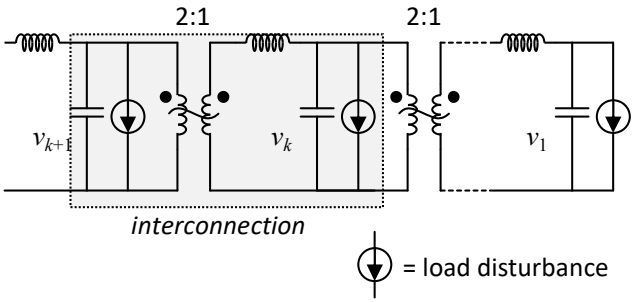

Fig. 3. Equivalent circuit for predicting the dynamics of the voltage conversion.

nation, copper losses and current displacement due to high-frequency effects, and, most unpleasantly, degradation [27], [28]. Such degradation includes accelerated insulation ageing due to displacement currents and finally partial discharge driven by voltage transients but also bearing potentials and bearing currents [29]–[32]. Wide-bandgap devices in conventional converters can aggravate loss and degradation further [33]. Although MMCs bring about higher output quality, their quality improvement only scaled between linear (amplitude granularity only) and squared (additional switching rate gain with additional modules) and therefore need notably too many modules for the required levels [23].

One approach to significantly lower the number of modules and associated cost charges the modules to voltages following an exponential sequence, termed *asymmetrical modular multilevel converter* (AMMC). Whereas modules with larger voltage provide the coarse output, modules with smaller voltages refine this first approximation and compensate the remaining differences, accordingly. Such work with different step sizes reminds of analog-digital converters and is a highly attractive configuration since a large number of output levels are obtained from just a few modules [34]–[43]. However, such asymmetrical dc-link voltages in the modules limit the freedom of synthesizing the output voltage to a certain degree so that various load conditions are sometimes not possible [36], [44]–[46].

An apparently straightforward solution implements either multiple dc supplies or galvanically-isolated dc/dc converters to the AMMCs [39]–[42]. The extra magnetic and semiconductor components need to process significant portions of the output power and therefore add large cost, weight, and extra loss [47]. A different approach refrains from adding components and power supplies, but differentially charges and discharges each module to the exact level using the load current. The resulting control is fairly complicated as it needs to carefully navigate through the set of valid operating states to avoid overcharging any modules and can lead to large interaction between real instant module voltages, charging, and output [34], [36], [45], [46], [48]. Furthermore, the use of the load current, including circulating currents, the time scale for balancing is half of the period length of the output frequency, rendering the maintenance of the proper module voltages below this duration complicated, can and introduce a second harmonic into the module voltages as well as strong interaction between output voltage and the module voltage ratio. Although, this issue also exists in conventional MMCs, it tends to be secondary there as it involves only a fraction of the module voltage; the high resolution of the AMMCs smallest voltage step, however, is easily smaller than the voltage fluctuations on the module with the highest voltage. Thus, despite the effort (or rather due to the selected balancing solution through the load), the waveform type is restricted, and the required information about the load angle implies higher input-to-output delay and less robustness against

rapid, unforeseen load changes.

This paper seeks a hybrid solution where only one power supply is used, yet minor circuit modifications are involved to significantly simplify the maintenance of the dc-link voltages. Indeed, the dc-link voltages autonomously stay at the designed power series, and neither require voltage/current monitoring nor interfere with the output voltage formation.

II. Asymmetrical MMC

Fig. 1 shows the proposed single-phase AMMC circuit for bidirectional dc/ac voltage-source conversion. The dc power source is connected in the same style as conventional MMCs, and the ac output is tapped from the center of the branch. In contrast to conventional MMCs, the AMMC's module voltages are charged to as power series. Here, we use a binary series that follows

$$V_{U1} : V_{U2} : V_{U3} : V_{U4} : V_{L1} : V_{L2} : V_{L3} : V_{L4} = 1 : 2 : 4 : 8 : 8 : 4 : 2 : 1.$$

Henceforth the term *binary* is dropped without causing ambiguities. Notice that the modules' dc-link voltages are symmetric, practically "mirrored" between the upper and lower branches to allow a smoother and consistent voltage ratio across the modules.

The AMMC also differs from MMCs with respect to module topologies. Here, additional auxiliary transistors and inductors are added to each chopper cell (denoted in red in Fig. 1). These auxiliary components help transferring excessive charges across the modules and maintain the voltage gradient of 2:1. With the voltage ratio locked at 2:1, the absolute module voltages are uniquely determined by the input dc supply (i.e., between DC+ and DC−) and the inserted modules. As such, the module voltages are controllable without the need for any sensors. The auxiliary components as well as the dc-link maintenance will be discussed in more detail later.

The instantaneous output voltage of AMMCs resembles that of the conventional MMCs and follows

$$v_{\mathrm{ac}} = \frac{1}{2} \sum_{k=1\ldots N} s_{Lk} V_{Lk} - s_{Uk} V_{Uk}, \tag{1}$$

where $s_k \in \{0, 1\}$ denotes either the bypass state (=0) or series state (=1). Meanwhile, the external dc link poses the following constraint:

$$\mathrm{avg}\left(v_{\mathrm{dc}}\right) = \mathrm{avg}\left(\sum_{k=1\ldots N} s_{Lk} V_{Lk} + s_{Uk} V_{Uk} \right). \tag{2}$$

As such, the time-average value of the total voltage inserted between DC+ and DC− determines the cumulative module voltage. For simplicity, we use a complementary control scheme and set

$$s_{Uk} + s_{Lk} = 1 \left(\forall k\right), \tag{3}$$

i.e., modules of the same dc-link voltage are paired together, at any time, there is exactly one module (either from the upper or the lower arm) out of each pair activated, and another one being bypassed. As such,

$$V_{dc} =_{(1)} s_{U1} + s_{U2} + \cdots + s_{UN} =_{(2)} 2^{N-1} s_{U1} =_{(3)} s_{L1} + s_{L2} + \cdots + s_{LN} =_{(4)} 2^{N-1} s_{L1}$$

where equalities $=_{(1)}$ and $=_{(3)}$ follow directly from Eq. (2)–(3); the second and fourth equalities assumed binary voltage distribution which is addressed in the next section.

With the mutually exclusivity feature of Eq. (3), we define $s_k' = s_{Lk} - s_{Uk} \in \{-1, +1\}$, so that Eq. (2) is reduced to

$$v_{\mathrm{ac}} = \frac{1}{2} \sum_{k=1\ldots N} s_k' V_{Lk} \tag{4}$$

As such, the switching combination can be determined in a manner similar to exchanging coins, where the reference output level is recursively approached, working from the largest module (s_N') towards the smallest one (s_1'). The binary power series permits ample redundancies to synthesize most of the levels, which hints a systematic exploitation to clear individual module's charge, and thus alleviating the effort to trim the excessive module energy. For simplicity, this paper randomizes the choice among the redundant state combinations.

III. Autonomous Module Voltage Regulation

The sensorless voltage control method implements auxiliary components in the modules. These auxiliary components form various load current paths together with the main switches (see Fig. 2). Alternating between these various paths allows operating the interconnection between two modules concurrently as modular multilevel converter and as dc/dc converter between the module dc-link capacitors of adjacent modules.

We want to take module x and y as an example (see Fig. 3). When module y is in bypass mode ($s_y = 0$), two dc/dc states exist, and the corresponding dynamics are shown in Fig. 3 (left). We can find that, regardless of the duration of $s_y = 0$, the voltage ratio at equilibrium equals $V_x : V_y = d : 1$, where d denotes the duty ratio between the two dc/dc states. Setting the duty cycle $d = ½$ achieves exactly our desired dc-link ratio. To keep things simple, we do not leverage the cases for $s_y = 1$, where the auxiliary circuit is simply set to follow the main switch, and makes no change over the inductor's current, i.e., *memorizing* the state i_{xy} until the circuit returns to $s_y = 0$ again.

The operation of the auxiliary circuits follows a very simple logic and does not require any information regarding the load current or the capacitor voltages. The voltage gradient is enforced at 1: d by circuit laws. It should be emphasized that all switching states of the auxiliary components only exchanges charge across the floating capacitors and do not alter the AMMC's output voltage, screened by the inductors. Setting d = ½ implies equal duration between the two dc/dc states under $s_y = 0$, which is easily achievable in digital controllers by means of digital counters. Most importantly, the dc/dc mode of the module interconnections run concurrently with the module multilevel mode can rapidly distribute charge and maintain the required voltage ratios according to a power series. Other MMC concepts with intentionally unequal and graded module voltages, in contrast, need large circulating currents and typically follow the period length of the output frequency—more accurately half of it—thus introducing a second harmonic on the module voltage and complicating maintenance of the voltage ratio within this duration.

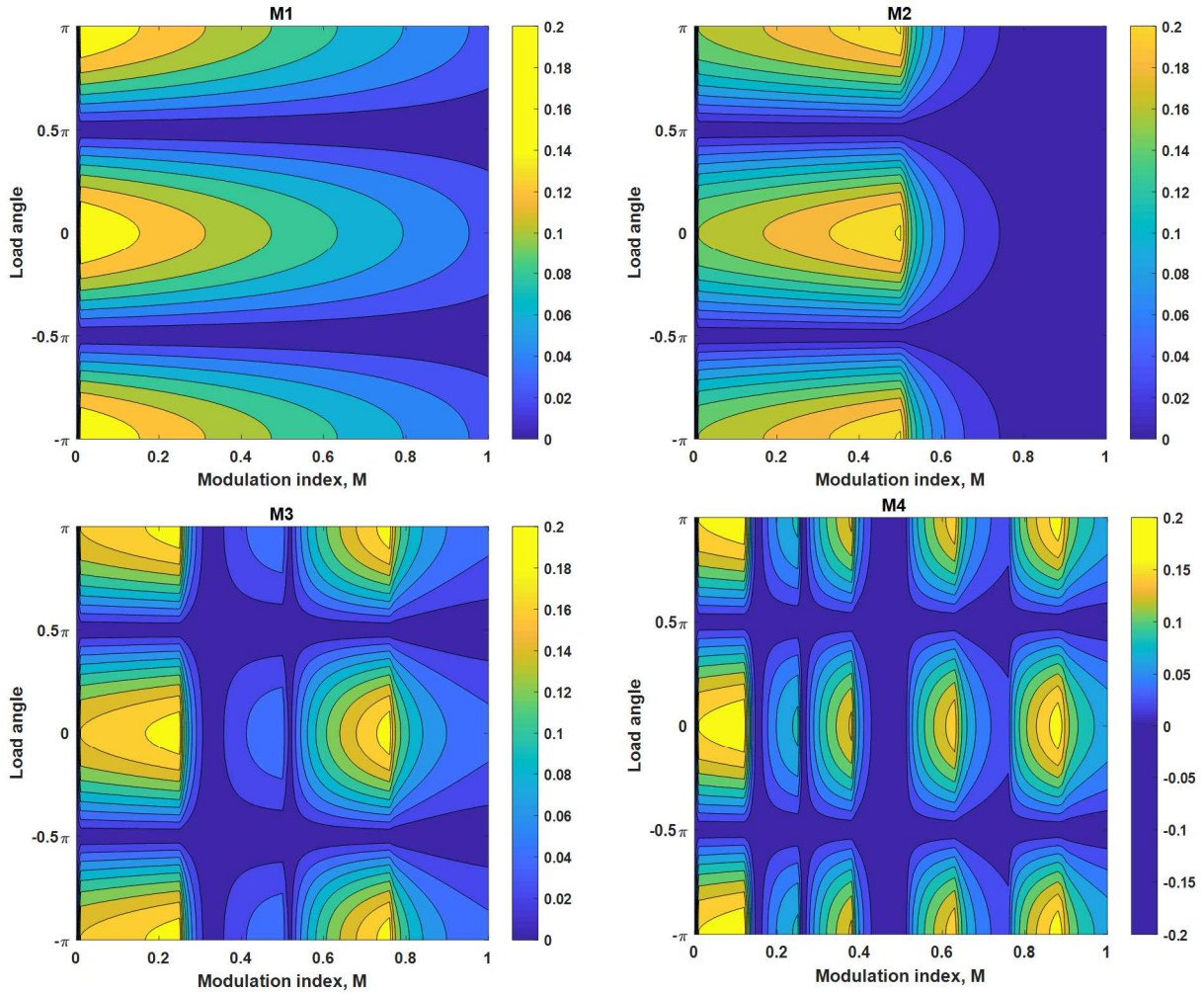

Fig. 4. Simulated charge-accumulating rate per module under different combinations of load angle and modulation index.

The equivalent circuit for predicting the energy conversion dynamics can be obtained from averaging out the switching states (Fig. 3) [49]. The model in Fig. 3 shows three factors that limit the regulation speed: *1)* the share of time when $1 - m$ when $s_y = 0$, *2)* the inductance of the dc/dc circuit, *3)* the portion of time that the module is exposed to the load current.

IV. Simulation and Experimental Results

A. Simulation results

In summary, the proposed control scheme of the AMMC comprises three parts: *1)* set the sum of the module voltages according to Eq. (2), which lead to a constraint on the main switches' state per Eq. (3), *2)* finalize the main switches' state to synthesize the output voltage per Eq. (4), and *3)* control the auxiliary circuits to trim and re-distribute the surplus energy of each module.

Such control scheme decouples the output-voltage control from the module-voltage regulation and imposes no restriction on the output waveform or the load condition. However, it is still important to evaluate if any module is systematically over/under-charged by the load current—if certain modules absorb net charge throughout the operation, the auxiliary circuits have to work unnecessarily harder to transfer the net charge in/out of these modules and therefore generate additional loss. Such systematic long-term imbalance can be compensated through known module scheduling, for instance, as follows below.

To isolate and evaluate such effect, we set up a numerical model of AMMC with each module having infinite capacitance. The influence from the module's voltage ripple is therefore eliminated. We recorded the charge-accumulation rate per module and swept the load condition across modulation depth m-times the load angle. The results are visualized in a 2D chart in Fig. 4, where brighter color (yellow) indicates higher charge-accumulation rate, or higher workload for the auxiliary circuits; conversely, darker color (blue) indicates lower charge-accumulation rate. Dark color represents the desired case where the stress on the auxiliary circuit is minimal. We can find that *1)* up to 20% the load current unavoidably disturbs the module dc links, which must be counteracted by the auxiliary circuit; *2)* pure reactive load is the ideal condition for AMMC due to the minimal excessive charge, while pure active load entails the highest power transfer via the auxiliary circuits.

B. Experimental results

We test the control method on an experimental AMMC setup with eight modules (4 + 4). Each module implements low-voltage field effect transistors (IPT015N10N5, Infineon) and ceramic capacitors with approximately 400μF. A 1-Ω power resistor serves as load. The control algorithm as well as the switching signals are implemented on an FPGA

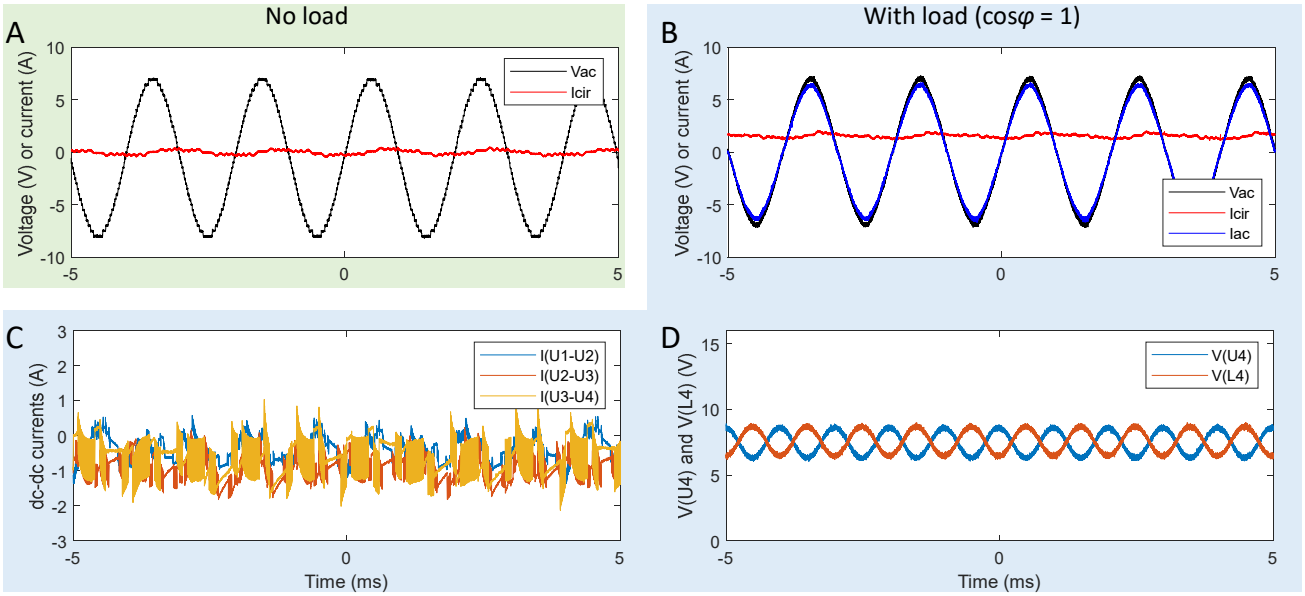

Fig. 5. Experimental waveforms. (A) Output voltage waveforms under no load condition. (B–D) with load.

clocked at 40 MHz (Xilinx Zynq-7020, sbRIO 9627, National Instruments).

Fig. 5A shows the output voltage under no load condition. Since the voltage steps are $^1/_{32}$ of the maximum voltage (compared to $^1/_5$ if the MMC were operated with symmetric module voltages), they are barely visible in the figure and the voltage trace is almost smooth. Each additional module would further reduce the granularity by a factor of 2 (compared to only (n + 1) / n for conventional MMCs). When the load is applied, the modules' dc links exhibit certain ripple (

Fig. 5D) that modulates the quantized output steps, resulting in a smoother output waveform with small distortion (

Fig. 5B).

Fig. 5C shows the charge-transferring current through the auxiliary dc/dc circuits. These currents are much smaller than the output current and estimated to constitute only 10% of the conduction loss.

V. Conclusion

Modular multilevel converters with asymmetric dc links, i.e., modules with different voltages, are an ideal configuration to generate a large number of output levels from only a few modules. The challenge, however, lies in controlling and maintaining the dc-link voltages. The proposed AMMC modifies the module interconnections so that they can concurrently operate as modular multilevel converters and as switched-inductor dc/dc converters to accurately maintain practically any fixed voltage ratio between adjacent modules. Thus, the presented AMMC circuit can operate the modules, for example, in a binary power series so that the second module has half the voltage of the first, the third half of the second, and so on, to enable very fine granularity of the output voltage.

Our experimental data demonstrate an AMMC with eight modules, four per arm, and binary sequence of the module voltages. The system could tightly maintain a stable voltage ratio between neighbors in a module arm. Furthermore, the measurements underline that the balancing current is small compared to the load current (less than a tenth) so that the additional components, both transistors and inductors, can have relatively low current ratings.

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