# Scaling spin qubits in quantum dots more - distant - industrial

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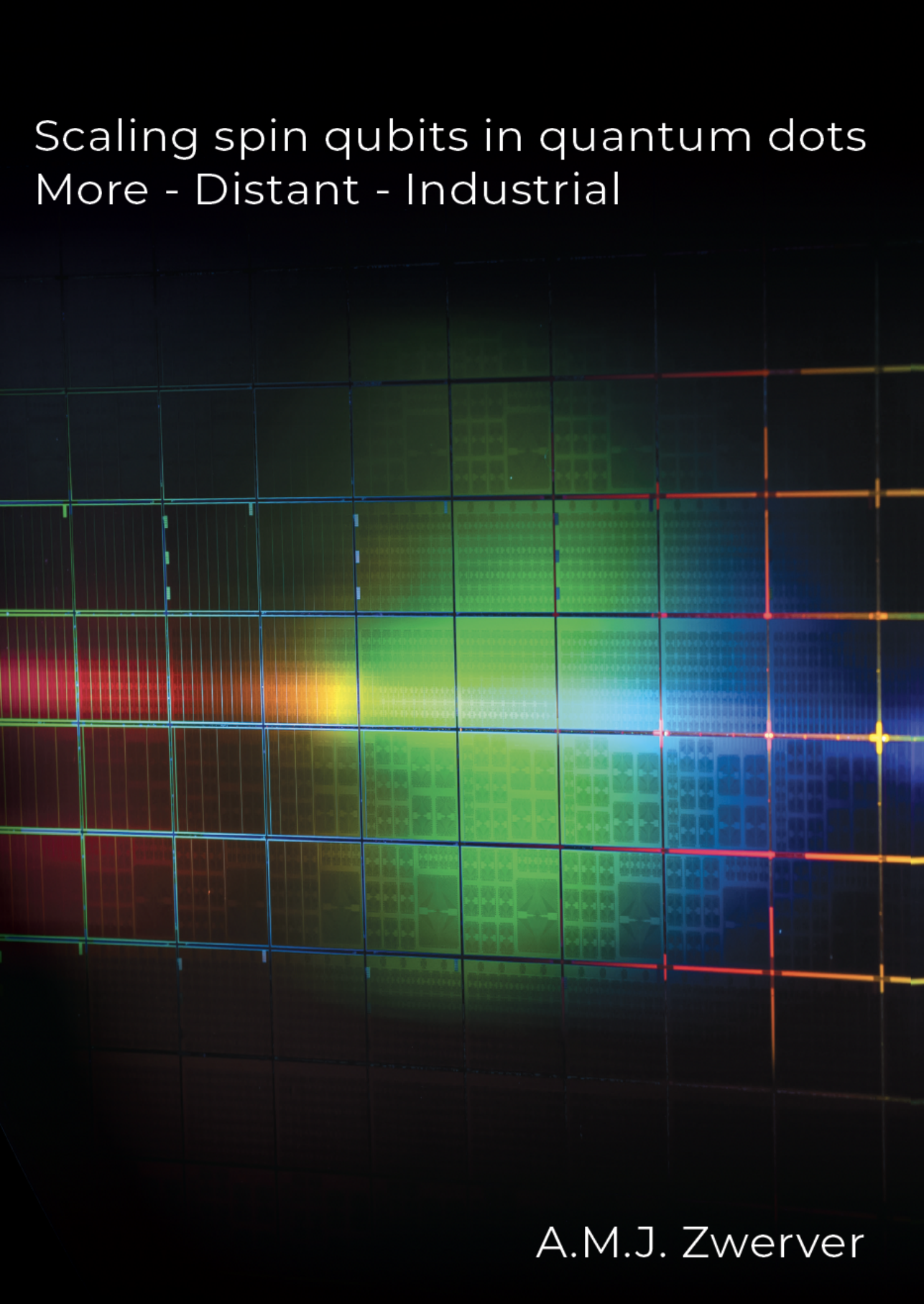

A.M.J. Zwerver

# SCALING SPIN QUBITS IN QUANTUM DOTS
# MORE - DISTANT - INDUSTRIAL

# SCALING SPIN QUBITS IN QUANTUM DOTS
# MORE - DISTANT - INDUSTRIAL

**Proefschrift**

ter verkrijging van de graad van doctor
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in het openbaar te verdedigen op
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door

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*Come with me and you'll be,*
*In a world of pure imagination,*
*Take a look and you'll see,*
*Into your imagination.*

*We'll begin with a spin,*
*Travelling in the world of my creation,*
*What we'll see will defy,*
*Explanation.*

[Willy Wonka]

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# SUMMARY

The discovery of the counter-intuitive laws of quantum mechanics at the beginning of the 20th century revolutionized physics. Quantum-mechanical properties, such as superposition and entanglement, can be harnessed to create quantum technology that opens a computing power far beyond the computing power that we know today. A quantum computer would enable efficient simulations of chemical reactions and material properties, which is expected to greatly impact healthcare and the energy transition.

Practical quantum computation requires millions of qubits, either with neighbour-to-neighbour connectivity, or connected via quantum links. Spin qubits in electrically-defined silicon quantum dots are promising qubit candidates due to their small footprint and relatively long coherence time. The last decade meant a leap for the understanding and control of spin qubit systems with devices up to three quantum dots. Yet building systems capable of performing useful quantum calculations has proven difficult due to low sample yield, as well as challenges in controlling and scaling these systems. In this thesis, we explore quantum-dot-based spin qubits and their suitability for scaling to larger systems. This quest was threefold and can be summarized as: More, Distant, Industrial.

**More:** Increasing the number of quantum dots and thus qubits to numbers greater than three was proven challenging, among others due to the the cross-capacitance that was posed upon quantum dots by the metallic gate electrodes of their neighbours. Here, we develop a material platform-independent method to individually control the chemical potential of each quantum dot and the number of electrons in it without affecting the quantum dots in their vicinity. We demonstrate the method by tuning up a linear array of eight GaAs quantum dots, containing exactly one electron each.

**Distant:** Thereafter, we shift our focus to creating quantum links between distant quantum dots by shuttling electron spins across a chip. Given the superior spin coherence times, we moved to silicon quantum dots, which were not as far developed at the time. To improve our understanding of the material and allow for the fabrication of silicon arrays beyond two quantum dots, we formulate metrics that allow for sample comparison across material platforms and gate geometries, which allows us to examine samples and detect disorder and flaws to improve (uniform) sample fabrication. This enables the fabrication of a sample that can host an array of up to five quantum dots and tune it with the method described above. To mimic a quantum link, we shuttle an electron forth and back through four quantum dots of the array up to 1000 times, corresponding to a total distance travelled of approximately 80 $\mu$m. We

observe that the spin orientation was preserved, forming a promising base for a quantum link.

**Industrial:** Thirdly, in collaboration with Intel, we harness the experience of the semiconductor industry by industrially manufacturing quantum chips and controlling a qubit on these chips. By means of the metrics that we defined, we demonstrate that industrial manufacturing on 300-mm wafers allows for high yield and reasonable cross-wafer uniformity of the samples, while allowing for well-defined quantum dots and qubits with a performance that is comparable to state-of-the-art spin-qubit results. This high-yield fabrication without compromising qubit properties is crucial for scaling to the thousands of qubits that we need for practical quantum computation.

The results in this dissertation provide perspective for scaling up silicon quantum dots and position the silicon spin qubit as a primary candidate for achieving quantum advantage with large-scale devices with millions of qubits.

A.M.J.

# SAMENVATTING

De ontdekking van de kwantummechanica in het begin van de 20ste eeuw betekende een revolutie voor de natuurkunde. Niet alleen werden de tegenintuïtieve fundamenten van de natuur onthuld, maar het begrip van de kwantummechanica bracht ook baanbrekende ontwikkelingen op technologisch gebied met zich mee. Tegenintuïtieve kwantummechanische eigenschappen, zoals superpositie en verstrengeling, kunnen worden gebruikt om kwantumtechnologie met ongekende rekenkracht te genereren. Zo zou een kwantumcomputer efficiënte simulaties van chemische reacties en materiaaleigenschappen mogelijk maken, hetgeen naar verwachting van grote invloed zal zijn op de gezondheidszorg en de energietransitie.
Voor het uitvoeren van praktische kwantumberekeningen zijn miljoenen kwantumbits (qubits) nodig, ofwel direct verbonden met hun buren, ofwel verbonden via kwantumlinks. Qubits gebaseerd op de spin van een elektron, gevangen in elektrisch gevormde, silicium kwantumdots, zijn veelbelovende qubitkandidaten vanwege hun kleine voetafdruk en relatief lange coherentietijd. In het laatste decennium hebben zowel het begrip van als de controle over spinqubitsystemen in chips met maximaal drie kwantumdots een grote sprong voorwaarts gemaakt. Toch is het niet evident gebleken om systemen te bouwen die bruikbare kwantumberekeningen kunnen uitvoeren vanwege enerzijds het lage aantal werkende kwantumchips en anderzijds de uitdagingen die komen kijken bij het manipuleren en opschalen van deze systemen. In dit proefschrift onderzoeken we de potentie van op kwantumdots gebaseerde spin qubits om op te schalen naar grotere systemen. Deze zoektocht was drieledig en kan worden samengevat als: Meer, Veraf, Industrieel.

**Meer**: Het opschalen tot meer dan drie kwantumdots en dus meer dan drie qubits bleek uitdagend, ondermeer vanwege de overspraak die op de kwantumdots werd uitgeoefend door de metalen elektroden van nabijgelegen kwantumdots. In dit proefschrift ontwikkelen we een methode om de chemische potentiaal van en het aantal elektronen in elke kwantumdot individueel in te stellen zonder de kwantumdots in de omgeving te beïnvloeden, onafhankelijk van het materiaal dat als basis voor de kwantumchip wordt gebruikt. We demonstreren de methode door een lineaire rij van acht GaAs kwantumdots te vormen en aan te sturen, elk met precies één elektron.

**Veraf:** Daarna verleggen we onze focus naar het maken van verbindingen tussen kwantumdots op afstand door elektronenspins over een kwantumchip heen en weer te pendelen. Vanwege de betere coherentietijden van op spin gebaseerde qubits in silicium, hebben we de overstap gemaakt naar de destijds minder ontwikkelde siliciumkwantumdots. Om ons begrip van kwantumdots in silicium te versterken en de fabricage van meer dan twee siliciumkwan-

tumdots mogelijk te maken, formuleren we metrieken die, onafhankelijk van het materiaal, vergelijkingingen tussen verschillende kwantumdots en kwantumchips mogelijk maken. Op deze manier kunnen wanorde en gebreken op de kwantumchips worden gedetecteerd en kan de fabricage van (uniforme) kwantumchips worden verbeterd. Aan de hand van de door de metrieken opgedane kennis was het mogelijk een kwantumchip te fabriceren waarop een rij van maximaal vijf kwantumdots kan worden gevormd met behulp van de hierboven beschreven methode. Om de effecten van een kwantumverbinding beter te begrijpen, pendelen we een elektron tot 1000 keer heen en weer door de kwantumdots, wat overeenkomt met een afstand van ongeveer 80 $\mu$m. We zien dat de oriëntatie van de spin tijdens dit pendelen behouden blijft, wat een veelbelovende eerste stap is op weg naar een coherente kwantumlink.

**Industrieel:** Tot slot benutten we, in samenwerking met Intel, de ervaring van de halfgeleiderindustrie door op industriële schaal kwantumchips te fabriceren en een qubit op deze chips te besturen. Met behulp van de eerder gedefinieerde metrieken tonen we aan dat het industrieel produceren van kwantumchips op 300 mm-wafers een hoog aantal werkende kwantumdots oplevert en dat de de kwantumchips gemaakt op verschillende wafers redelijk uniform blijken te zijn. Tegelijkertijd kunnen er op de chips zowel goed gedefinieerde kwantumdots worden gevormd, als qubits waarvan de kwaliteit vergelijkbaar is met de beste qubits uit het veld. Dergelijke kwantumchipfabricage, waarbij een hoog rendement behaald kan worden zonder afbreuk te doen aan de kwaliteit van de qubit, is cruciaal met het oog op het opschalen naar de duizenden qubits die nodig zijn voor praktische kwantumberekeningen.

De resultaten in dit proefschrift bieden perspectief voor het opschalen van siliciumkwantumdots en positioneren de siliciumspinqubit als een belangrijke kandidaat voor het behalen van kwantumvoordeel met kwantumcomputers met miljoenen qubits.

Anne-Marije

# 1 INTRODUCTION

*For all is just a woven web of guesses*

Xenophanes

1

## 1.1 THE QUANTUM REVOLUTION

In his work *Republic* [1], Plato describes a conversation between his brother Glaucon and Socrates. In this conversation, they deliberate the nature of reality and ponder over our perception of the world. Our physical world is absolute, nor timeless, they state, and everything in it is just a reflection of an 'ideal Form', or 'Idea'. This Form captures the essence of an object. Appearances change and no entity of an object is similar, yet the Form is what discerns them as that particular object: no chair is alike, yet we recognize them as chairs, because they are imprints of the Form chair. A Form is essentially a blueprint for the perfect object and it is aspatial, timeless and absolute. The Forms are at the core of everything we know, were it qualities, objects, or living creatures, but we can merely aspire to catch a glimpse of it.

Plato visualizes this idea with the allegory of the cave. We are all caught in a cave, chained, forced to sit away from the entrance and to face the back wall. The cave would be dark, but behind us, there would be a fierce fire. And in front of the fire are people carrying objects, animals and trees. As we could only see the wall, the mere things we perceived were shadows. Obscure reflections of the actual world outside: the true Forms. And we would interpret the shadows as reality, as they were all we saw. Only those curious and brave enough to pursue the effort of breaking free and turning around, were able to truly see and understand nature.

We could argue that each scientific law is a Form. Through observations we experience imprints of the law in our world, yet only those who pursue to profoundly comprehend their observations, might be able to grasp the actual Form and unravel nature more and more.

### 1.1.1 The discovery of the quantum

With the turn of the 20th century, the course of physics turned upside down. At the time, most physicists were of the idea that all theoretical Forms were uncovered and just a handful of paltry puzzles remained to be solved[1]. One of these puzzles was the ultraviolet catastrophe: theory predicted that a perfect emitter, such as a black body, should emit infinite energy at high frequencies. Yet as black bodies do not have endless energy, reality shows that the energy in the high-frequency spectrum actually approaches zero. It was in the autumn of 1900 when Max Planck, pondering upon this problem, solved the paradox by proposing that energy could only be absorbed or emitted in discrete packages of their frequency, or *quanta*: $E = hf$ [2]. Thus, energy states with their excitation energy much higher than the temperature ($hf > kT$) could not exist. Although Planck himself mainly referred to his solution as *'an act of despair'* [3] and the story goes that, to illustrate this, he even called his quantum constant '$h$' for 'help variable' [4], his ideas marked the start of a new chapter in physics.

Planck's ideas gained traction when, in 1905, Albert Einstein proved that quanta could explain the photoelectric effect [5]. He demonstrated that light, which was believed to be inherently wavelike ever since Christian Huygens wrote his *Traité de la lumière* [6], could behave like a particle. Additionally, the opposite was demonstrated in 1924 by Louis de

[1] One of these puzzles led, as we will see, to the birth of quantum mechanics. The other puzzle was the nature of light propagating through vacuum, which opened the field of relativity.

Broglie: particles of matter, such as electrons and protons, have wavelike properties. With the discovery of this so-called wave-particle duality, quantum mechanics was officially born and in the years that followed, the principles of quantum mechanics were laid out by physicists like Niels Bohr, Werner Heisenberg and Erwin Schrödinger.

### 1.1.2 The interpretation of quantum mechanics

Although the laws of quantum mechanics were precisely established in the first quarter of the twentieth century, it was merely the mathematical structure that physicists agreed on. As much agreement there was on the mathematical foundation, so much debate was there on the interpretation of quantum mechanics. Quantum theory predicts some counter-intuitive phenomena that are often said to be rooted in three fundamental principles of quantum mechanics: superposition, measurement and entanglement. These phenomena are illustrated in two of the postulates with which John von Neumann laid the mathematical foundations of quantum mechanics [7]:

- **Schrödinger postulate:** As long as the system is not subject to measurements, the state of the quantum system in time will be described by a wave $|\psi\rangle$ that follows the Schrödinger wave equation:

$$\frac{-\hbar^2}{2m}\nabla^2\Psi + V\Psi = i\hbar\frac{\partial\Psi}{\partial t} \tag{1.1}$$

- **Projection postulate:** If the system is in state $|\phi\rangle$ when a measurement of the physical quantity $A$ is performed on the system and the measurement result is the eigenvalue $a_i$, then the system will remain in the eigenstate corresponding to $a_i$ after this measurement.

The Schrödinger postulate captures the evolution of the system, stating that the system cannot be located with certainty. The particle can have any position in a two-dimensional Hilbert space and it is often said that a particle is in 'multiple states at the same time', which is called superposition. However, the projection postulate states that, upon measurement, the system's state will be projected onto one of its eigenstates along the measurement axis, with probabilities of the various outcomes, $|\psi|^2$, given by the Born rule [8]. Hence the system will be reduced to a classical state. In that respect, quantum mechanics resembles Plato's cave: the quantum mechanical wave function describes the rich outside world, yet, when we try and observe a state, it reduces to a mere shadow.

The third quantum phenomenon that governs quantum mechanics is entanglement. Entanglement describes an inseparability between multiple quantum elements that share a superposition. The states of the elements are correlated, independent of the distance between them. The inextricable link of the elements makes that their states can be defined nor measured without instantaneous knowledge, or determination of the other element.

The ostensible incompatibility of the wavelike evolution of a quantum state, as described by Schrödinger's equation and the definite state that a system is in after it has been subject

to a measurement, was subject to much debate among physicists. The big question that is agonizing many scientists still today, is what it means for an element to be in a superposition and how, by means of a measurement, the transition from a probability distribution to a defined value is made. Moreover, it was the classically-unknown phenomenon of entanglement that gave physicists a headache. Did entanglement deny *locality*[2]?

As a response to the measurement problem, Heisenberg and Bohr developed the Copenhagen interpretation of quantum mechanics in which they proclaim that quantum mechanical behaviour is completely indeterministic. Before measurement, a particle can be anywhere, nowhere, or in multiple places at once, i.e. before measurement, the particle does not have *reality*. Measurement of the quantum system causes the wave function to 'collapse' in exactly one of the possibilities that the wave function allows the particle to be in, consistent with the probabilities that are assigned to each possible state by the Born rule.

The idea of indeterminism, the denial of reality and the possibility of non-locality gave rise to countless questions and criticism. The probably most famous response came from Einstein, nota bene one of the founding fathers of quantum mechanics, in collaboration with Podolsky and Rosen. In a paper titled '*Can quantum-mechanical description of physical reality be considered complete?*' [9] they argued that, given local reality, quantum mechanics was either wrong, or incomplete, imposing that additional, 'hidden', variables are necessary to properly interpret quantum mechanical observations. Einstein emphasized his views on indeterminism with the famous words: '*God does not play dice*'[3] [10]. Niels Bohr was a firm proponent of the Copenhagen interpretation and responded in a paper with the exact same title that the assumption of local reality was wrong and that we should revise our perception of reality [11]. The debate went on for years and was never settled.

It was John Bell who, in 1964, introduced the Bell inequalities, with which he theoretically demonstrated that a local realistic nature cannot hold in quantum mechanics [12]. Any interpretation of quantum mechanics should therefore at least renounce either reality, or locality. Over time, his theory has been experimentally verified various times [13, 14]. eventually even without loopholes [15–17], finally confirming the fascinating nature of quantum mechanics. It is important to mention, though, that although a quantum system may be non-local, the superluminal transfer of meaningful information is prohibited.

In the meantime, the counter-intuitive mysteries were not solved and some people considered the Copenhagen interpretation unsatisfactory. In 1952, David Bohm developed his own interpretation of quantum mechanics[4], in his words '*mainly to show that an alternative to the Copenhagen interpretation is at least logically possible*' [18]. Bohmian mechanics is a non-local hidden variable theory, stating that the wave function describes a 'hidden' quantum field, that governs the particle trajectories over deterministic paths [19, 20]. Bohm's interpretation

[2] Locality is short for local causality

[3] It is not surprising that Einstein had difficulty accepting the implications of quantum mechanics. Especially entanglement seemed to imply a superluminal connection between elements. And it was Einstein who, a few years prior, based his successful theory of relativity on the claim that information transfer could not exceed the speed of light. A claim that, even given entanglement, still holds to this day.

[4] Actually, Louis de Broglie already proposed a similar theory, the Pilot-wave theory, in 1927, yet was met with severe criticism.

marked the starting point for the development of a whole range of interpretations. Among these, are the relative state interpretation (or Many Worlds interpretation), which negates the wave-function collapse by alleging that the observer becomes part of the system and all possible outcomes happen in a superposition of parallel universes [21], and the transactional interpretation, which explains superposition by having an element travelling forward and backwards in time to its eigenstates until a measurement locates it [22]. It is definitely insightful to delve further in the foundations of quantum mechanics. Some good starting points would be [23, 24]. Still today, more than 100 years after its development, the conceptions on how to interpret quantum mechanics still vary widely. Or, as Richard Feynman puts it: *'I think I can safely say that nobody understands quantum mechanics'*.

### 1.1.3 Grasping quantum mechanics with quantum mechanics

It was the same Richard Feynman who once suggested in a speech that, in order to get a better grasp of the quantum mechanical world, we need to make use of quantum mechanics itself [25]. As classical computers as we know it are, in fact, classical, they are incompetent to simulate quantum mechanical systems, which have features beyond local reality. Moreover, the complexity of quantum problems scales exponentially with the number of elements rather than polynomially, implying that for a single element to be added, the computing power needs to be doubled to execute a calculation. He ended his speech with the famous words: '*Nature isn't classical, dammit, and if you want to make a simulation of Nature, you'd better make it quantum mechanical, and by golly it's a wonderful problem because it doesn't look so easy*'.

## 1.2 THE SECOND QUANTUM REVOLUTION

Feynman's ideas launched an era that can be referred to as the second quantum revolution. Where the first quantum revolution was all about discovering the dazzling laws of quantum mechanics and building its mathematical foundations, the second quantum revolution focuses on harnessing the potential of quantum mechanics as a technological resource. No longer are we "passive observers of the quantum world" [26], merely using quantum mechanics in applications such as lasers, GPS and transistors. But we are able to actively create and manipulate quantum states, operating them at the boundaries of our knowledge and thereby opening a whole range of technologies, among which quantum communication, quantum sensing and quantum computation.

### 1.2.1 Quantum calculations

By embracing the concepts of quantum mechanics, quantum computers offer a fundamentally new method of calculation that promises to solve problems that would take billions of years on all current supercomputers combined [27]. It is expected that this will open currently intractable applications in factorization problems, drug design and material modelling.

The difference between a classical computer and a quantum computer is rooted in the fundamental building blocks. Classical computers store and process information by means

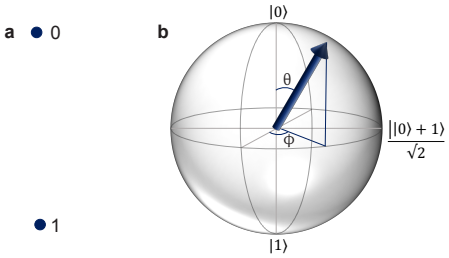


Figure 1.1.: **Classical bits and quantum bits. a.** Representation of binary, classical bits. **b.** An arbitrary qubit state can be visualized on the Bloch sphere by describing the qubit as $\cos(\theta/2)\,|0\rangle + \exp(i\phi)\sin(\theta/2)\,|1\rangle$ with $\theta \in [0,\pi]$ and $\phi \in [0,2\pi]$. The basis states $|0\rangle$ and $|1\rangle$ are featured on the north and the south pole of the sphere respectively and the maximal superposition states $(|0\rangle + \exp(i\phi)\,|1\rangle)/\sqrt{2}$ are at the equator. Points inside the sphere represent the qubit being in a statistical mixture of different quantum states and hence it lost its pure quantum state.

of bits. Bits are binary and can take the values 0, or 1. Quantum computers are built up of quantum mechanical bits, qubits in short. Also qubits can be in the states $|0\rangle$, or $|1\rangle$, yet by employing the laws of quantum mechanics, qubits can also be in every possible superposition of $|0\rangle$ and $|1\rangle$. In our Plato analogy, we could argue that classical computers compute with mere shadows, whereas quantum computers make use of the full potential of the 'Forms of the outside world'. A quantum bit can be in every superposition of its basis states:

$$|\psi\rangle = \alpha\,|0\rangle + \beta\,|1\rangle\,, \tag{1.2}$$

with probability amplitudes $\alpha, \beta \in \mathbb{C}$ and $|\alpha|^2 + |\beta|^2 = 1$ for normalization. To visualize its richness, we can parametrize the qubit state as $\cos(\theta/2)\,|0\rangle + \exp(i\phi)\sin(\theta/2)\,|1\rangle$ with $\theta$ the qubit amplitude and $\phi$ the phase. This captures the qubit's two-dimensional Hilbert space on a sphere, called the Bloch sphere, see Fig. 1.1. The surface of the Bloch sphere represents all possible superposition states of the qubit, with the basis states $|0\rangle$ and $|1\rangle$ featured on the poles. Qubit operations are rotations over the surface of the Bloch sphere.

The power of a qubit compared to a classical bit is clearly illustrated when we perform a computation $f(x)$. A classical computer will have to calculate $f(0)$ and $f(1)$ sequentially, whereas the superposition of the quantum state allows for simultaneous evaluation: $f(|\psi\rangle) = \alpha f(|0\rangle) + \beta f(|1\rangle)$ [28]. The calculating power of a quantum computer can be spectacularly enhanced by increasing the number of qubits. Generally, $N$ qubits can compute on $2^N$ states simultaneously. This means that, while a classical computer has to double the number of classical bits to double its computing power, for a quantum computer the computing power is doubled by the addition of a single qubit. This generates an exponential speed up and it is usually said that, in theory, a quantum computer with a mere 50 qubits is able to do calculations that are intractable with the best classical computer to date [29]. This effect is called quantum advantage.

Thus, the the quantum computer seems to bring dazzling opportunities, yet there is a catch. Upon measurement, the qubit superpositions collapse to one of their eigenstates and

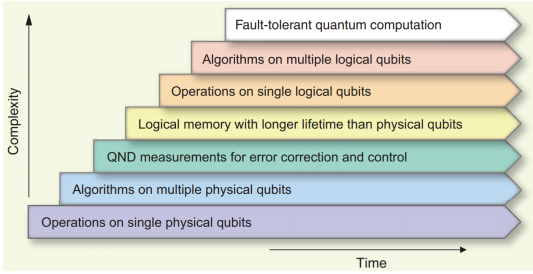


Figure 1.2.: **Complexity steps towards building a fault-tolerant quantum computer.** [38] formulated seven stages for the development of quantum computers, where more complexity is added per stage. As each step is built upon the previous stage, full expertise of a stage is required before moving to the next stage. Current quantum computing efforts hover around the third stage.

merely become shadows of the rich Forms they were before observation. So, even though we calculate in the world of Forms, we can only observe the classical shadows and we seem not able to break free[5] [30]. For long, scientists thought that this made quantum calculations useless, until Peter Shor proposed the first quantum algorithm that exponentially expedited large-number factorization [31]. Finding quantum algorithms that work within these limitations and ensure a quantum speed up is an ongoing challenge in the field of quantum computation.

The realization of quantum technology starts with the formation of high-quality qubits. Yet, just as there are many ways to manufacture a classical bit, ranging from transistors to reflective trails in a cd, there is currently a wide variety of quantum hardware platforms studied, each having its own advantages and disadvantages. Examples are optical qubits [32], superconducting transmon qubits [33], spins around a NV-centre in diamond [34], ion traps [35] and qubits made in semiconductor quantum dots [36]. In order to be able to evaluate and compare the suitability of a potential qubit system, David DiVincenzo proposed a list of five criteria that each promising qubit system needs to adhere to [37]:

1. A qubit has to be a well-defined, scalable, two-level system.

2. The ability to initialize the qubit in a well-defined state.

3. The system should have a universal set of quantum gates, that can bring a qubit (and qubit combinations) in every possible (combined) state. For a single qubit this means the qubit can be brought anywhere on the Bloch sphere.

4. The ability to read out the qubit(s) individually and with high fidelity.

5. The time during which a qubit state is preserved needs to be much longer than the time of single- and multiple-qubit gates.

[5] This is called Holevo's bound: for a quantum computation, we can just get out a single classical bit of information when measuring a single qubit.

1

### 1.2.2 The sprouting of the quantum era

The first experimental demonstration of quantum algorithms, performing the Deutsch-Josza [39] and Shor algorithm [40] on an NMR system, meant a leap for the realization of quantum computation. Since then, many more promising qubit systems popped up. Yet, scaling to systems that allow for the reliable computation of quantum algorithms is the most daunting challenge that quantum computers face today. This is caused by the inherent fragility of the qubit. Firstly, qubits cannot be shielded from their environment completely. Inevitable interactions with the environment cause the qubit to lose its quantum state. This is called decoherence. Moreover, as the wide spectrum of possible qubit states needs to be reduced to binary states upon measurement, the smallest calibration errors can have considerable consequences. And inevitably, if the number of qubits increases, the probability of an error occurring in the calculation grows, making the performance of reliable quantum computation challenging.

The road towards fault-tolerant quantum computation was paved by the formulation of error-correction codes [41, 42]. These codes allow for reliable quantum computation with imperfect qubits by encoding a single qubit state onto multiple qubits. This ensemble of physical qubits, together called a logical qubit, will be used to perform calculations. Due to the added degrees of freedom, individual errors in physical qubits can be localized and corrected faster than they occur by means of majority voting or other schemes, provided at least the error probability per elementary operation is below a threshold value. We usually consider an error-correction threshold of 1% to perform the so-called surface code [43], yet, in principle, we could say that the lower the error rate of the qubits, the fewer qubits are required per physical qubit. Still, fault-tolerant quantum computing is envisioned to require millions of qubits. The steps towards fault-tolerance are drawn up by Schoelkopf and Devoret, see Fig. 1.2 [38].

On our way towards fault-tolerant quantum computing, we are entering an era where qubit coherence and fidelities increase and, although the error rates are high, there are enough qubits to perform tasks that are beyond the capability of classical super computers. Hence, although the devices are noisy and prone to errors, it opens a previously inaccessible computational regime. These first meaningful quantum computations and analog quantum simulations are expected to be very insightful and informative. This era, usually called the Noisy Intermediate-Scale Quantum (NISQ) era [29], was ushered in by the first demonstration of quantum advantage on a 53-qubit chip[6] [44] and is now starting to bloom [45–47].

In the meantime, quantum information has gained traction and many institutes and companies are getting involved. Large companies invested and joined, like IBM, Google and Alibaba (superconducting qubits), Intel, CEA Leti and IMEC (semiconductor spin qubits), Fujitsu (diamond-based quantum internet) and many more. Meanwhile, a whole bunch of start up companies is sprouting, varying from companies building quantum computers to companies that are dedicated to making part of the control stack. The exciting new community that is rapidly built, will most likely cause the development of quantum technology to skyrocket.

[6] Although this demonstration was highly impressive, the calculation was noisy and not meaningful

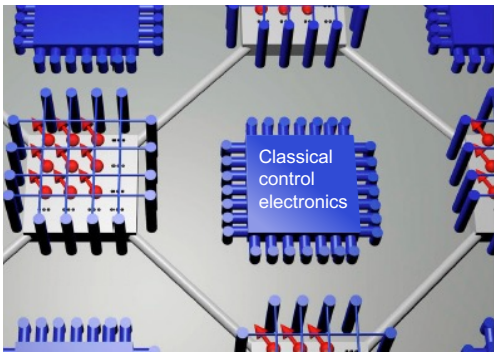


Figure 1.3.: **Sparse qubit architecture.** Proposal for a scalable spin-qubit architecture with qubit registers and on-chip control electronics. Figure adapted from [54].

## 1.3 INDUSTRY-MANUFACTURED SPIN QUBITS

One of the promising qubit nominees is the electron spin captured in a quantum dot [48]. Spin qubits stand out because of their small size, which allows for a high qubit density on-chip and makes them particularly suitable for scaling [36]. Moreover, spin qubits are only weakly perturbed by their solid-state environment, which makes for robust, long-lived qubits.

Pioneering work on spin qubits has been performed in III-V materials, in particular GaAs. However, the abundance of non-zero nuclear spins in the environment of the qubit limited the coherence time strongly. Recently, the field has steered away from GaAs and focused on Si as the host material, which offers a more quiet qubit environment. This transition really put spin qubits on the map as promising qubit candidate. Since then, long-lived qubits [49], as well as high-fidelity qubit operations [50–52] and qubit readout [53] have been demonstrated.

Now spin qubits amply satisfy the DiVincenzo criteria and fidelities hover around the error-correction threshold, research focus shifts towards exploring spin qubits as a scalable platform. Several qubit architectures have been proposed for this challenging task. One of these designs proposes the formation of a sparse array containing dense, $N$x$M$ qubit registers, interconnected with quantum links, see Fig. 1.3 [54]. The qubits in the registers have nearest-neighbour control and could be arranged in a crossbar structure to share gate electrodes [55], or be individually addressed [56]. The space created by the quantum links allows for the implementation of classical control electronics on-chip. The current challenge towards building such architectures is making the constituent parts: dense quantum-dot registers, coherent links and uniform, high-yield and high-quality samples.

Out of all qubit candidates, the quantum dot based spin qubit resembles the classical transistor the most. It is often argued that spin qubits, especially those made in silicon, form a compelling qubit platform because of their compatibility with current semiconductor manufacturing. This would be a great advantage for the scalability of high-yield, uniform qubit systems. Nevertheless, the methods used in industry fabrication lines, although highly reliable and uniform, are intrusive and little flexible. It is therefore an outstanding question whether these techniques actually allow for the fabrication of quantum dot structures and whether

the industrial processing conditions that ensure high-yield transistor fabrication do not compromise qubit quality and coherence. In this thesis, we collaborate with Intel to explore the compatibility of spin qubits in electrically-defined quantum dots with advanced semiconductor manufacturing.

## 1.4 THESIS OUTLINE

In this thesis, we will explore quantum-dot-based spin qubits and their ability to scale to larger systems. This quest was threefold. 1) Can we scale up the number of quantum dots in a linear array such that they each hold a single electron simultaneously and can we tune them with a scalable method. 2) Can we establish quantum links that connect distant qubits, while making space for on-chip electronics? 3) Can we harness the years of experience in the semiconductor industry to fabricate silicon-based devices that allow for quantum dots to be formed and host a spin qubit, such that we can readily build high-yield, uniform quantum devices. With other words: scaling quantum-dot-based spin qubits: more, distant, industrial. The outline of the thesis is as follows:

- In **Chapter 2** we will introduce the physics of electrically-defined quantum dots. We build up the quantum dot step-by-step; starting from the material stacks that form the base for our quantum dots, to the physics of single and multiple coupled quantum dots. Moreover, we will introduce the interaction of the electron spin with its environment.
- **Chapter 3** explores the assets and weaknesses of the quantum dot based electron spin as a qubit by following the DiVincenzo criteria.
- The setup used for the research conducted in this thesis, is described in **Chapter 4**. Moreover, the most common measurement techniques are introduced, as are the metrics that qualify the suitability of a device.
- In **Chapter 5**, we explore the ability to scale the number of quantum dots.
- **Chapter 7** focuses on electron shuttling as the base for a quantum link, where we study the preservation of spin polarization during the shuttling process.
- In collaboration with Intel, in **Chapter 6** we harness the experience of the current semiconductor industry by manufacturing a quantum chip and controlling a qubit on this chip.
- Finally, in **Chapter 8**, we provide conclusions from this thesis. Moreover, we look ahead to what the future can bring us and which experiments may bring spin qubits in electrically-defined quantum dots a step further towards stepping away from the shadows and making the future quantum.

# 2 ELECTRICALLY-DEFINED QUANTUM DOTS IN SOLID-STATE MATERIALS

*Quantum David overpowers Classical Goliath*

John Preskill

*This chapter describes the physics of electrons captured in electrically-defined semiconductor quantum dots relevant for the work in this thesis. We will start with an overview of the main substrates that are used as quantum dot hosts. Then, we will dive further into the physics of quantum dots and we will end this chapter by studying the limitations that the environment poses on the electron spin.*

## 2.1 FROM TRANSISTORS TO QUANTUM DOTS

People have been using computers to expedite calculations for thousands of years. First, in the primitive form of a tally stick, or an abacus and later, rooms filled with people, mainly women[1], were used for comprehensive calculations [57]. Yet, the invention of the transistor in 1947 marked a breakthrough for computation as it was known [58]. After the on-chip integration of many transistors, the development of the computer accelerated and followed Moore's law ever since its formulation [59], reducing the footprint of the transistors, while expanding the computer's capacity, marked by the development from digital pocket calculators to current-day smart phones and super computers.

Still today, classical computer bits are based on field-effect transistors (FETs). A FET is an electrical structure made in a semiconductor material, typically silicon. The structure contains three connections: a metallic topgate, separated from the silicon by an insulating layer and a source and drain contact. By controlling the bias on the topgate, a two-dimensional electron gas (2DEG) can be accumulated at the silicon-insulator interface of the substrate, forming a current channel between the source and drain contacts. A source-drain current can be either induced, or blocked by controlling the voltage of the metal gate residing above the channel. A positive bias on the gate electrode allows for electrons to flow between the source and the drain (bit state '1'), whereas a negative bias will deplete the electrons, blocking the current (bit state '0').

Out of the various flavours of qubits that exist, the electron spin hosted in a semiconductor quantum dot is the quantum mirror of the classical transistor. By leveraging the current-day technology that is used to manufacture transistors, we can fabricate nano-scale structures in which single electrons can be trapped and used as a qubit [60]. A quantum dot is an artificial system that can capture electrons down to precisely one electron. Islands of electrons are formed by confining electrons of an electron sea in three dimensions. Similar to a FET, a quantum dot sample contains source and drain contacts and confines the electrons in one dimension in the form of a 2DEG. Yet, instead of a single top gate controlling the channel, the potential landscape is shaped further into potential minima, or quantum dots by capacitively coupling the electrons to three metallic top gates. Two of the gates control the tunnel barriers of the quantum dot, through which the electrons are coupled to the source and the drain reservoirs, whereas the third gate controls the electrostatic potential of the quantum dots and hence regulates the number of electrons that reside in the quantum dot. As the dimensions of the quantum dot are small, typically $10 - 100$ nm, the Coulomb repulsion of the electrons needs to be overcome for an extra electron to be added. Once the thermal energy subceeds the coulomb repulsion, usually around 4 K, the number of electrons that can reside in the potential minimum is discrete. Moreover, as the island is about the same size as the de Broglie wavelength of the electrons inside the host material, $\lambda = \frac{h}{2m^* E_K}$, the electrons are confined tightly enough that the orbital levels are quantized [61]. These orbitals can be filled

[1] Women were considered to be better with 'language' and cheaper in payment.

with electron spins sequentially, which is why this system is often called an artificial atom.

This chapter provides an introduction to the quantum dot physics that is relevant for this thesis. We will discuss the main substrates that are typically used as quantum dot hosts. Then, the relevant physics of electrons in quantum dots will be described. We will end this chapter by discussing the limitations that the nature of the substrate poses on the spin. For a more thorough understanding of spins in electrically-defined quantum dots, we recommend you to study [36, 62–64] and [65].



## 2.2 QUANTUM-DOT STACKS

The basis for lateral quantum dots is the semiconductor material stack that hosts the quantum dots and provides confinement of the electrons in a 2DEG. There are four stacks that are highly promising for quantum-dot-based quantum computation: gallium-arsenide/aluminium-gallium-arsenide (GaAS/AlGaAs), silicon/silicon-germanium (Si/SiGe), silicon metal-oxide- semiconductor (SiMOS) and germanium/silicon-germanium (Ge/SiGe). A schematic of the material stacks and energy diagrams is provided in Fig. 2.1. Work on other semiconductor substrates, such as InAs or InSb and work on hutwires and nanowires falls outside the scope of this thesis.

Initially, quantum dot research was based on group III-V materials, with the main focus on GaAs-AlGaAs heterostructures. These heterostructures, grown by molecular beam epitaxy, consist of respectively a layer of GaAs, an $Al_xGa_{1-x}As$ layer, where $x$ is usually $0.3$, and a layer of AlGaAs, n-doped with Si dopants. The dopants facilitate the creation of the 2DEG; the electrons provided by the Si dopants diffuse into the GaAs. However, since the band gap difference between GaAs and AlGaAs will prevent recombination with the now positively-charged donor atoms, a thin sheet of electrons will be formed at the GaAs/AlGaAs interface. Consequently, the conduction band will fall below the Fermi energy and at low temperatures, only the lowest energy modes will be energetically accessible, confining the electrons along the z-direction, see Fig. 2.1. Confinement in the second and third dimensions is achieved via Schottky-type top gates.

Both GaAs and AlGaAs crystals have a Zinc-blende structure with almost matching lattice constant, which results in an exceptional structural quality of the heterostructure, leaving very few defects that could give rise to electron scattering. This allows for mobilities as high as $10^7$ cm$^2$/Vs [74], in combination with a relatively low percolation density, smaller than $10^{10}$ cm$^{-2}$ [74]. Moreover, the relatively low effective mass ($m^* = 0.067m_e$) causes the electrons in the 2DEG to have large energy spacings. In combination with the clean substrates, these features allow for large ($> 100$ nm-pitch) quantum dots and excellent control of the potential landscape, making GaAs a suitable material for pioneering quantum-dot and spin-qubit research. Spin qubits in GaAs quantum dots can be manipulated by making use of the natural and sizeable spin-orbit coupling [64] and attaining the single-electron regime, initialising, reading out and controlling spins in single quantum dots [36,

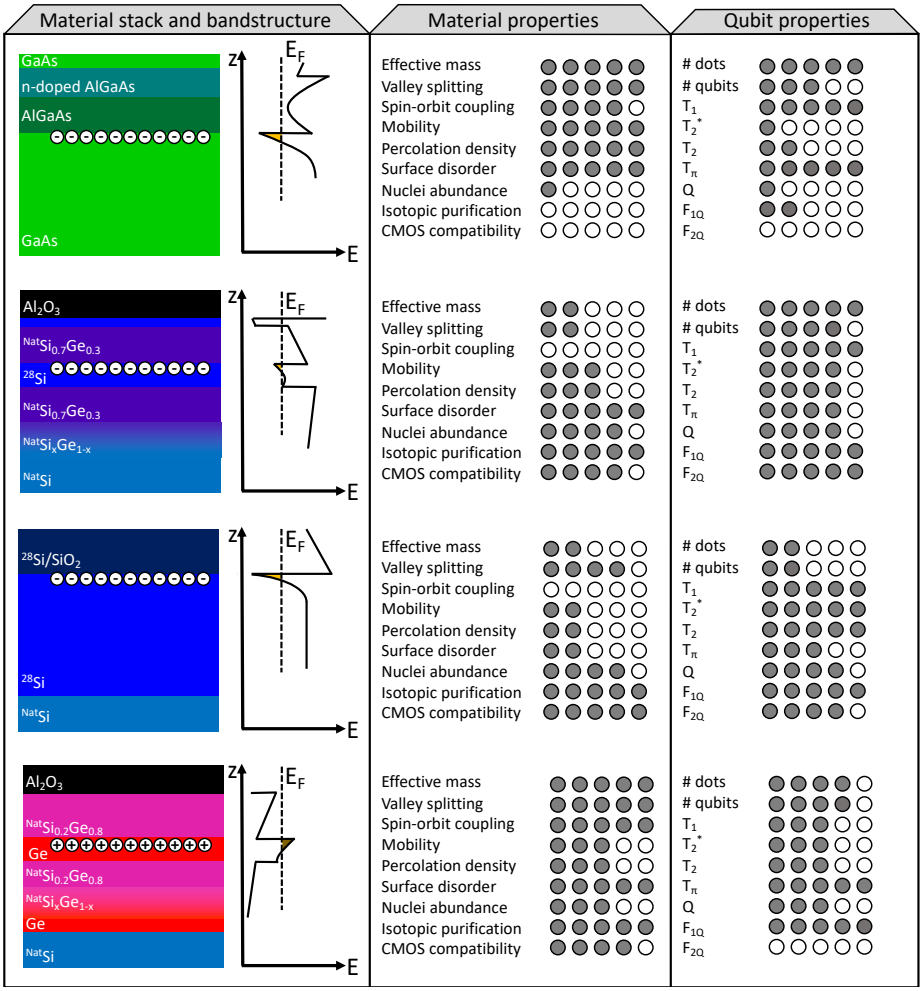


Figure 2.1.: **Material stacks and properties.** Material stacks for semiconductors typically used for quantum dot-based spin qubits: GaAs, Si/SiGe, SiMOS and Ge/SiGe. Schematics of the material stacks with their energy diagrams, indicating the conduction band minimum, are depicted on the left. For each material, the material properties are characterized. These material properties mainly rise from the band structure of, disorder in and nuclear isotopes in the material. Moreover, the quantum dot and qubit properties of each material are qualitatively defined. The table is inspired on [64] and [66] and based on values from [49–51, 67–73]

75] and performing two-qubit gates [76–80] were all first demonstrated in GaAs samples. Moreover, control and transportation of electrons and spin states in larger-dot arrays has been demonstrated [81–88], as we will see in chapter 5 of this thesis, as well as the control over two-dimensional quantum dot arrays [89, 90] and quantum simulation [91–93]. Nevertheless, qubit coherence times are severely limited by the hyperfine interaction between the qubit and the abundance of local nuclear spins in the substrate.

In the quest to diminish the nuclear spin bath and hence increase the qubit's coherence time, group IV material silicon (Si) emerged as a promising candidate to host spin qubits. Natural silicon has 95 % zero-spin nuclei ($^{28}$Si and $^{30}$Si) and can be purified to make the abundance of nuclear spin isotopes ($^{29}$Si) below a few hundred ppm [94]. This drastically reduces the hyperfine interaction of the qubit with the host material and therefore coherence times can be increased by orders of magnitude compared to GaAs samples [49, 95]. An additional advantage of silicon substrates is its compatibility with the contemporary industrial chip manufacturing. It is expected that industry processes can be readily adapted for both Si/SiGe and SiMOS wafers. Leveraging such industrial knowledge will undoubtedly boost substrate properties, such as mobility, percolation density and disorder [64] and will allow for large-scale sample fabrication with high yield and reproducibility, on which we will elaborate in chapter 7 of this thesis. Yet also silicon substrates come with a challenge: the indirect band gap and six-fold degeneracy of the conduction band minimum induce an extra degree of freedom, the valley [96]. Small valley splittings lead to quasi-degenerate spin and valley states that can hinder (multiple-) qubit control and the extra degree of freedom may lift Pauli spin blockade, which is why a high valley splitting is essential for high-performance quantum computation [97, 98]. There are two widely used flavours of silicon samples: the silicon/silicon germanium (SiGe) heterostructure and the silicon metal-oxide-semiconductor (MOS) stack.

The Si/SiGe heterostructure consists of a tensile strained, thin ($\sim 10$ nm) silicon quantum well [64], wrapped between two layers of $Si_xGe_{1-x}$, where $x$ is gradually decreased down to $x = 0.7$ to adjust for the lattice mismatch of $4.2\%$ between Si and Ge atoms [99]. To ensure a smooth substrate surface, the top of the structure contains a thin ($< 4$ nm) silicon cap. An insulating layer separates the substrate from the metallic gates. Although silicon samples can be used in depletion mode by adding modulation dopants, these dopants are usually omitted and by biasing accumulation gates on top of the sample, electrons from the ohmic contacts accumulate in the quantum well at the Si/SiGe interface [100]. Additional (overlapping) metallic gates allow for the confinement of the potential landscape in the second and third dimension. The epitaxial interface in Si/SiGe heterostructures results in mobilities beyond $10^5$ cm$^2$/Vs and percolation densities as low as $\approx 10^{10}$ cm$^{-2}$ [101, 102] allowing for low disorder and high control. Yet the effective electron mass in silicon is relatively large, $m^* = 0.19m_e$. This requires smaller quantum dots than in GaAs stacks and therefore puts stricter conditions on the metallic gates, that need to be need to be fabricated closer together, or overlapping [103]. Steady progress in the field resulted in coherence times of several milliseconds [50], single-qubit-gate fidelities exceeding $99.9\%$ [50] and two-qubit gate fidelities higher than $99\%$ [51, 52] and enabled the implementation of quantum algorithms, such as the Deutsch-Josza algorithm [104, 105] and three-qubit entanglement [106]. Moreover, single-electron transportation has been demonstrated [107, 108], as well as strong coupling of two distant spin states to a photon in the microwave regime [109, 110] and strong spin-spin coupling in the dispersive regime [110]. Currently the main challenge for qubits in SiGe heterostructures is the relatively small valley splitting. Although valley splittings up to 260 $\mu$eV have been measured [111], typical valley splittings are below 150 $\mu$eV [112, 113]. Research

to increase the valley splitting is ongoing [114, 115].

As in FETs, the 2DEG in SiMOS quantum dot samples is formed at the silicon-oxide interface [54, 116]. Due to strong confinement at the interface, the valley splitting in SiMOS can be in the order of $0.2 - 1$ meV [117, 118]. Metallic top gates allow for the accumulation and the confinement of the potential landscape. As the combination of the high effective electron mass in silicon and the proximity of the 2DEG to the metallic gates results in relatively small quantum dots, SiMOS samples typically require an overlapping gate structure [119]. Moreover, due to disorder in the oxide, proximity to the oxide results in high charge noise and relatively low electron mobilities and high percolation densities of respectively $10^4$ cm$^2$/Vs [120–122] and $10^{11}$ cm^-2 [122]. This complicates quantum dot tuning and spin control. Especially when the quantum dots approach the few-electron regime, multiple quantum dots are formed beneath adjacent gates. On the other hand, the high valley splittings allow for qubit operation at relatively high temperatures, such as 1 K [123, 124]. The higher cooling power at those temperatures in combination with the application of cryogenic control electronics [105] allows for the integration and operation of classical control electronics on the chip, which is a very appealing feature for scaling. Additionally, single-qubit gate fidelities of 99.98 % [67] and two-qubit gate fidelities of $98\%$ [125] have been reached and the longest quantum dot based spin qubit coherence time to date is measured in SiMOS [49].

Recently, Ge/SiGe heterostructuctures have rapidly claimed their place as a promising qubit platform [126, 127]. Ge samples consist of a strained Ge quantum well grown between two SiGe spacer layers. The stack is topped with a Si cap and an oxide layer to isolate the metallic gates [119, 128]. The current Ge effort is hole-based; the 2DHG is formed on the Ge/SiGe interface by means of hole accumulation. Germanium provides a compelling heterostructure; the holes combine mobilities exceeding $10^6$ cm$^2$/Vs, percolation densities below $2 \times 10^{10}$cm$^{-2}$ [128] and a low effective mass ($m^* = 0.05m_e$), allowing for high quantum-dot control and tunability [64]. Due to the strain on the quantum well, the valley degeneracy is eliminated. Moreover, Ge has a direct band gap and a strong intrinsic spin-orbit coupling, which allows for fast qubit driving without the inconvenience of low-laying valley states, or the need for external driving mechanisms. However, spin-orbit coupling also poses limitations to the qubit. Charge noise from the substrate causes fluctuations in the electric field around the spin. As a result, the electron starts to wiggle. The changing spin-orbit coupling that the spin feels, causes g-factor fluctuations over time, which is currently the main contribution to qubit decoherence.

Natural Ge contains $7.7\%$ non-zero spin isotopes ($^{73}$Ge) which allows for coherence times of around $100$ $\mu$s, times that may improve further in purified Ge [129]. Moreover, single-qubit gate fidelities approaching $99.99\%$ have been demonstrated [71] and the number of qubits has, to date, been doubled every year, demonstrating two-qubit gates [130] and even four-qubit gates [72]. Germanium is compatible with semiconductor manufacturing technologies, which can improve mobilities and percolation densities and provides considerable possibilities for scaling.

## 2.3 ELECTRICALLY-DEFINED QUANTUM DOTS

Metallic top gates confine the electrons in the 2DEG further to form quantum dots. One of the advantages of gate-defined quantum dots is that adjusting the bias on the gates allows to adjust some quantum dot properties. We can measure the quantum dot properties by opening a bias window between the source and the drain and measuring the current through the quantum dot.



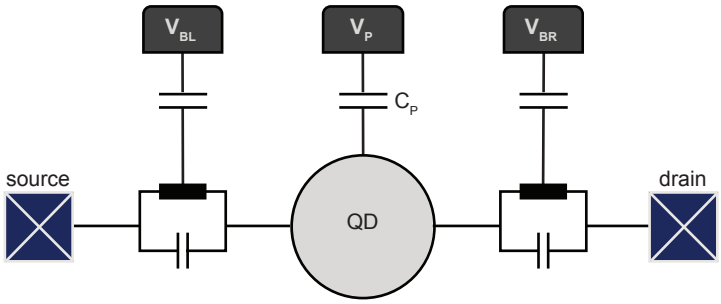


Figure 2.2.: **Electrical model of a quantum dot.** The quantum dot is capacitively coupled to its plunger gate and connected to the source and the drain reservoir via tunnel barriers, represented by parallel capacitors and resistors, tunable by a barrier gate. Electrons can flow from the source, through the tunnel barrier onto the quantum dot and on to the drain, inducing a current through the quantum dot.

### 2.3.1 Single quantum dots

An effective starting point for the description of quantum-dot physics is by means of electron transport through a single quantum dot that is tunnel coupled to a source and a drain reservoir. These measurements are conveniently described by the constant interaction model, which is based on two assumptions. Firstly, the classical interaction between the electron and the environment can be described by a constant capacitance $C$. As depicted in the electrical circuit in Fig. 2.2, $C = C_S + C_D + C_g$, with $C_D$, $C_S$ and $C_g$ the capacitive coupling of the quantum dot to the source, drain and gate respectively (neglecting self-capacitance and capacitances to other gates and parts of the 2DEG). Secondly, the discrete single-particle energy spectrum is not altered by the interaction between the electrons in the quantum dot.

A convenient way to describe the quantum dot is by the energy required to add the $N_{\text{th}}$ electron to a quantum dot in its ground state, called the electrochemical potential, $\mu(N)$:

$$\mu(N) \equiv U(N) - U(N-1) = (N - N_0 - \frac{1}{2})E_C - \frac{E_C}{|e|}\sum_i C_i V_i + E_N. \qquad (2.1)$$

Here, $E_C = |e|^2/C$ is the charging energy. Due to the small system dimensions, the charging energy needs to be paid when an extra electron is added to the quantum dot to overcome the Coulomb repulsion between the electrons. This is a purely classical energy. Moreover, the small dimensions of the quantum dot add a quantum effect, represented by

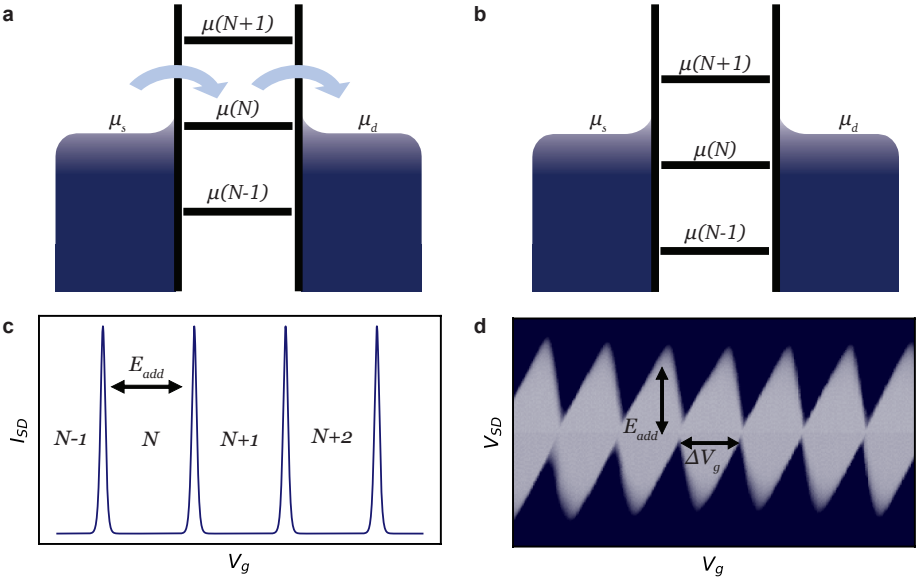


Figure 2.3.: **Coulomb interactions in a single quantum dot. a.** Electron transport through the quantum dot can occur when the electrochemical potential of the quantum dot aligns with the bias window. **b.** When the electrochemical potential of the quantum dots falls outside the bias window, the current is blocked and the quantum is is said to be in Coulomb blockade. In **b.**, the quantum dot contains exactly $N$ electrons. **c.** Schematic figure where the source drain current is plotted as a function of the gate voltage. The Coulomb peaks represent the configurations where $\mu_S \leq \mu_{dot} \leq \mu_D$ and hence a source-drain current is induced, as in **a**. In the other regions, the quantum dot is in Coulomb blockade, as in **b**. **d.** Figure of the current through the quantum dot as a function of the gate voltage and the bias window. Within the diamond-shaped regions, the system is in Coulomb blockade and the number of electrons on the quantum dot is in equilibrium.

the third term of the electrochemical potential. The orbitals are quantized and filled according to Hund's rule, with orbital energy $E_{orb} \sim \frac{\hbar^2}{m^* l^2}$, where $m^*$ is the effective mass of the electron and $l$ is the quantum-dot dimension. To both the charging energy and the orbital energy applies: the smaller the quantum dot, the larger the energy. The sum of the charging energy and the orbital energy is the addition energy:

$$E_{add} = \mu(N+1) - \mu(N) = E_C + E_{orb}. \tag{2.2}$$

The addition energy is mainly governed by the charging energy, as the orbital energy can be zero, when electrons are added to spin-degenerate energy levels. Once the charging energy exceeds $kT$, the number of electrons on the quantum dot is discrete.

Because the electrochemical potential depends linearly on the gate voltage, $V_G$, electrons are added to the quantum dot linearly with gate voltage. We can therefore conveniently visualize the quantum dot system as a ladder of electrochemical potentials that moves up and down as we change $V_G$, see Fig. 2.3. Whenever the electrochemical potential for the

$N_{\text{th}}$ electron, $\mu(N)$ is tuned below the Fermi energy of the source ($\mu_S$) and drain ($\mu_S$) reservoir, the $N_{\text{th}}$ electron is added and exactly $N$ electrons reside in the quantum dot. Electron transport measurements can be executed by opening a bias window, i.e. applying a voltage ($\sim 200\ \mu$eV) to the source: $\mu_S - \mu_D = -|e|V_{SD}$. By adjusting the gate voltage, the chemical potential moves down and an electron can tunnel from the source, through the dot onto the drain whenever $\mu_S \leq \mu(N) \leq \mu_D$, inducing a current peak, called Coulomb peaks, see Fig. 2.3a,c. If the chemical potential falls outside the bias window, the number of electrons on the quantum dot is static, current is impeded and the quantum dot is said to be in Coulomb blockade, see Figs. 2.3(b-c). Coulomb blockade can be lifted in two ways: by opening the bias window further until it encloses an addition line, which effectively broadens the coulomb peak, or by changing the electrochemical potential by means of $V_g$. This effect is visualized in Fig. 2.3d, where the gate voltage is swept versus the bias-window. The figure features Coulomb diamonds: grey diamond-shaped, Coulomb-blockaded regions. By opening the bias window, or scanning the gate voltage, Coulomb blockade can be lifted. The addition energy is represented both in the distance between the Coulomb peaks and when the bias window covers the distance between the Coulomb peaks. As the former is in volts and the latter in energy, we can use the Coulomb diamonds to extract the lever arm; a measure to convert the gate voltage to energy: $\alpha = C_P/C = \Delta E_{SD}/\Delta V_G$. When $kT < E_{add}$, a Coulomb peak can be normalized as: $G_{norm} = \cosh^{-1}[\mu_{dot}(N) + C]/2k_bT$ [131]. By fitting this expression to a Coulomb peak, the electron temperature can be extracted.



### 2.3.2 Double quantum dots

Multiple quantum dots can be connected via tunnel coupling in a linear, or two-dimensional array to form a multi-dot system. The smallest multi-dot system is a double quantum dot arrangement. A double-dot system is conveniently mapped in a charge stability diagram, see Fig. 2.5. In a charge stability diagram, the plunger gates of the two respective quantum dots are swept, while the current-response is monitored. As we increase the plunger gate for one quantum dot, we clearly see lines, often called addition lines, that represent the coulomb peaks, indicative of an electron from the reservoir being added to the specific quantum dot. In the regions between the lines, the system is in a Coulomb-blockaded regime. These equilibrium regimes are usually referred to by their charge state, ($N_1$,$N_2$), where $N_1$ ($N_2$) is the electron number on dot 1 (dot 2). If the two quantum dots are completely decoupled and they do not experience cross-capacitance from their respective plunger gates, we would merely see horizontal and vertical lines crossing in a rectangular pattern. However, for neighbouring dots, the electrochemical potential in one dot is capacitively coupled to the charge state of the other quantum dot. Moreover, the quantum dots experience capacitive coupling to the gates of neighbouring quantum dots. Consequently, the electron number on a quantum dot can alter, due to adjustment of neighbouring gates, or changes in the neighbouring quantum dot. The former is reflected in the tilted addition lines of the charge stability diagram, where the slope depends on the the capacitive coupling of the quantum dot to the two gates that are swept. The latter results in a charge step in the addition lines at each cross point, splitting the

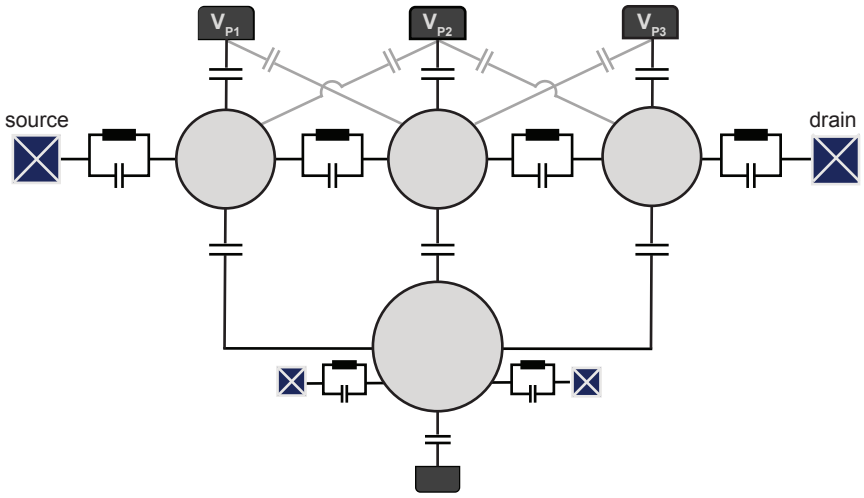


Figure 2.4.: **Electrical model of multiple quantum dots.** This diagram depicts the interactions of a multiple dot system, capacitively coupled to a sensing dot. The three quantum dots are capacitively coupled to their respective gates. Moreover, due to cross-capacitance, they are to a certain extend also coupled to adjacent gates. Electrons can tunnel between the source, the drain and the quantum dots and in between the quantum dots. The tunnel barriers are represented by tunable system of a parallel capacitor and resistor. The tunnel barrier can be adjusted by means of barriers gates, which are omitted for clarity. The sensing dot is connected to a separate source and drain, through which the current through the sensing dot can be monitored. Changes in the charge on the three quantum dots can be capacitively sensed by the charge sensor.

cross point in two so-called triple points. This gives rise to the so-called honeycomb pattern that is typical for a charge stability diagram.

The line in between the triple points indicates a charge transition between the two quantum dots. On the line, the quantum dot states are degenerate. By crossing the line, the electron configuration is changed by making it favourable for an electron to move to the other quantum dot. The alignment of the electrochemical potentials in both dots is indicated by the detuning $\epsilon$, which is for one electron in a double-dot configuration determined as $\epsilon = \mu(0,1) - \mu(1,0)$, or, more generally as $\epsilon = \mu(M-1,N) - \mu(M,N-1)$, with $\mu$ the electrochemical potential of the ground state.

The hybridization of an electron wave function over the two dots (charge states) is determined by the tunnel coupling and the detuning between the dots. When the tunnel coupling is sufficiently high and the detuning is sufficiently low, the electron wave functions are not entirely localized on a single quantum dot. Rather, the two possible charge configurations form superpositions in a bonding and antibonding orbital, where the energy of the bonding (antibonding) orbital is $|t_c|$ lower (higher) than the orbitals of the separate dots [62]. The tunnel coupling can be measured by determining the charge distribution as a function of detuning of the two dots [132], or via photon-assistant tunnelling measurements [133, 134]

and can be adapted by changing the bias on the corresponding tunnel barrier.

A double-dot system containing two electrons can be in the $(2,0)$, the $(0,2)$, or in the $(1,1)$ charge configuration, where the two spins can form four possible states: the singlet state, or one of the three triplet states. The degeneracy between the three triplet states can be lifted by the application of an external magnetic field [36]. As the singlet state has an anti-symmetric wave function and the wave function of the triplet states is symmetric, in a single quantum dot electrons in the singlet state can reside in the same orbital, whereas electrons that form a triplet have to overcome the orbital splitting. Hence, the singlet state is separated from the triplet states by the singlet-triplet splitting, $E_{ST}$. The four possible two-electron states are:

$$S = \frac{|\uparrow_i\downarrow_j\rangle - |\downarrow_i\uparrow_j\rangle}{2} \tag{2.3}$$

$$T_- = |\downarrow_i\downarrow_j\rangle \tag{2.4}$$

$$T_0 = \frac{|\uparrow_i\downarrow_j\rangle + |\downarrow_i\uparrow_j\rangle}{2} \tag{2.5}$$

$$T_+ = |\uparrow_i\uparrow_j\rangle\,, \tag{2.6}$$

where $i$, $j$ are the specific dots that the electrons are in, which can be both the same quantum dot, or two different quantum dots. The coupling of the charge states $(1,1)$ and $(0,2)$ is determined by the tunnel coupling: $\sqrt{2}t_c$. Apart from hyperfine and spin-orbit coupling effects, the tunnel coupling is spin-preserving. This means that the singlet (triplet) $(2,0)$-state merely hybridizes with the singlet (triplet) $(1,1)$-state, inducing an avoided crossing: $2\sqrt{2}t_c$.

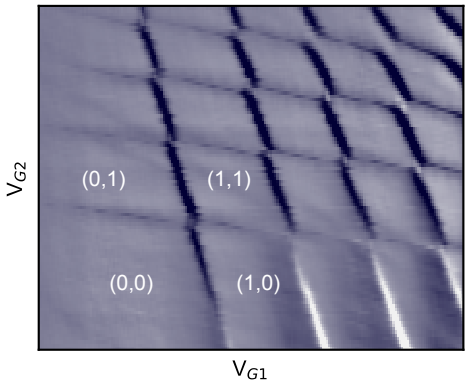


Figure 2.5.: **Charge stability diagram.** Charge stability diagram of a double quantum dot as a function of the voltage on the plunger gates of the respective quantum dots. The vertically and horizontally tilted lines represent the addition lines of electrons to quantum dot 1 and quantum dot 2 respectively. The regions in between represent the equilibrium charge states, indicated by the electron number $(N_1, N_2)$ in dot 1 and dot 2.

### 2.3.3 Multiple quantum dots

Scaling the number of qubits implies the use of multi-quantum-dot systems. Also multi-dot arrays are conveniently visualized in charge stability diagrams; as quantum dots capacitively couple to the gates of neighbouring quantum dots, multi-dot systems were initially mapped in a single charge stability diagram. The two plunger gates of the outer-most dots were swept and each quantum dot was recognized by their specific coupling to the swept gates, thus by the specific slopes of its addition lines. However, a charge stability diagram is merely a two-dimensional cut-out of a multi-dimensional system. Moreover, due to the cross-capacitance, the increase of the bias on one gate results in a change in the electrochemical potential of all adjacent quantum dots and the tunnel coupling between them. Consequently, tuning a multi-quantum-dot system became increasingly intricate. To minimize the influence from adjacent gates on electrochemical potentials and tunnel couplings and expedite quantum-dot tuning, it is convenient to make use of so-called virtual gates. By orthogonalising the cross-capacitance, virtual gates allow the adjustment of the electrochemical potential of a specific quantum dot [79, 91], or the tunnel coupling between two quantum dots [135, 136] while keeping the electrochemical potential of the other dots unchanged. Chapter 5 of this thesis uses such virtual gates to implement an efficient tuning strategy and rapidly tune a linear array of eight quantum dots.

### 2.3.4 Charge sensing

Up to now, we particularly discussed electron-transport measurements through a quantum dot; measurements where a bias is applied across one or more quantum dots and the source-drain current is monitored. These transport measurements are particularly practical for the initial characterization of quantum-dot properties, such as the measurement of coulomb peaks, coulomb diamonds and double quantum dots. However, for the confinement and control of a single electron and the performance of single-shot qubit readout, this method may be insufficient. Typically, when a quantum dot is emptied, the tunnel barrier between the quantum dot and the reservoir increases. This results in faint, or even invisible coulomb peaks, see Fig. 2.6a. Moreover, as transport measurements are based on current detection, individual electrons cannot be perceived and hence this method does not allow for single-shot readout.

An alternative and more meticulous measurement method is electron detection by means of a nearby charge sensor. For charge sensing of the electrons, an electrometer is placed in the vicinity of the quantum dot, see Fig. 2.4. Changes in the electrostatic potential of the quantum dot are capacitively sensed by the charge sensor and hence detected (Fig. 2.6b). There are several examples of charge sensors, but most commonly used are a quantum point contact (QPC) [137] and a separate quantum dot [138], often called a sensing dot, or single-electron transistor. The concept of these types of charge sensors is the same; the sensor is biased to a steep flank, for QPCs usually the flank to the first conductance plateau, for sensing dots the flank of a coulomb peak, while the conductance through the sensor is monitored. As the flank is steep, the conductance is very sensitive to changes in the electron occupation of the quantum dot. Typically, a sensing dot is preferred over a sensing QPC, as

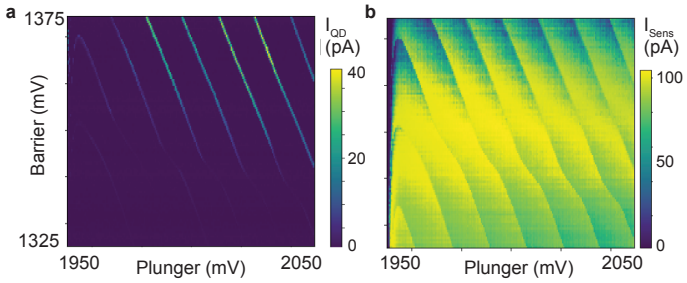


Figure 2.6.: **Transport measurement vs charge sensing measurements. a** Coulomb peaks of a single quantum dot measured in transport and **b** by means of a nearby charge sensor. Whereas the sensitivity of the transport measurements is low at lower electron numbers, the charge sensor is able to detect the charge transitions in that regime.

both the coulomb peaks are sharper and hence more sensitive and there is a higher degree of control over sensing dots than over QPCs [138].

The performance of the charge sensor is dependent on the signal-to-noise ratio (SNR) of the system. The noise in the system can be reduced by means of low-pass filters, yet these filters limit the bandwidth and therefore pose restrictions on the tunnelling rate of the electrons. A high charge-sensing signal hinges on the following points:

- The capacitive coupling between the quantum dot and the sensor. This is reflected in the shift of the chemical potential of the sensing dot when a charge $q$ is added to the quantum dot: $\Delta\mu_{sensor}/q$
- The sensitivity of the charge sensor, indicating the change in the electrometer's conductance $G$ as a result of the shift of its chemical potential. This emphasizes the advantages of a steep sensor slope, as a steeper slope will cause a larger conductance step: $\Delta G/\Delta\mu_{sensor}$.
- The quality of the readout setup. This is determined by the bias over the sensing dot, as a higher bias will induce a higher current through the sensing dot - although the bias should not exceed the relevant energy scales, such as charging energy, valley splitting and orbital energy. Moreover, the measurement equipment should detect the signal, while not degrading the SNR: $V_{signal}/\Delta G$.

Some of these parameters are opposing each other as, for example, a higher bias window over the sensor will generate a higher current response, yet it will also broaden the coulomb peak, which will reduce the sensor response. Thus for optimization of these parameters, we have to look for sweet spots.

Recently, high-fidelity electron and qubit readout has also been achieved by means of dispersive sensing. Here, a high-frequency signal is applied to a gate or resonator in the vicinity of the quantum dot. The ability of the charges on the quantum dot to respond to the

applied excitation, will translate into a frequency shift of the monitored frequency signal. This method has been successfully demonstrated in several studies [53, 139–141] and achieved readout fidelities above 98%, with a prospect to reach fidelities over 99.9% [53]. Because this method mainly uses existing quantum dot structures such as metallic gates for charge sensing, dispersive readout techniques have the advantage that they do not require the overhead that sensing dots bring.



## 2.4 INTERACTION WITH THE ENVIRONMENT

As the quantum dot is hosted in a solid-state material, the electron charge and spin state cannot be entirely decoupled from the environment. The interaction between the charge of the electron and the environment entails exchange with reservoir electrons and charge noise. The former effect can be suppressed by sufficient tunnel coupling tuning. Although the spin state of the electron barely couples to the magnetic environment, as the magnetic moment of the spin state is small, $\mu_B = 9.27x10^{-24}$ J/T [36] and is only affected by the electric environment indirectly, spins can couple to the environment via spin-orbit interaction, hyperfine interaction with the nuclear spin bath, or by charge noise.

### 2.4.1 Spin-orbit coupling

The spin-orbit interaction (SOI) couples the electron spin with its orbital motion. A moving electron spin in a spatially-varying electric field $\mathbf{E}$ will effectively experience a varying electric field over time. This translates to a relative magnetic field, $\mathbf{B_{SO}}$, which couples to the electron's spin and is proportional to $\mathbf{E} \times \mathbf{p}$, with $\mathbf{p}$ the electron's momentum.

In solid-state materials, the local electric field can have two causes, both originating from the absence of symmetries in the crystal. First, electric fields can be induced by a strong asymmetry in the confinement potential (structural inversion asymmetry): the Rashba contribution to the SOI [142]. As the Rashba term depends on the confinement potential, the strength of the Rashba SOI, $\alpha$, is material dependent [36]. Moreover, there is the Dresselhaus term in the SOI. This is caused by bulk-inversion asymmetry and is therefore only applicable to crystals with an asymmetric lattice structure, such as the Zincblende lattice [143]. The strength of the Dresselhaus SOI, $\beta$, depends on the material properties of the crystal and on $< p_z^2 >$ [36], indicating that alterations in the electron confinement caused by a different top-gate composition can change the Dresselhaus effect of the SOI [144]. For a crystal grown in the $[0, 0, 1]$-direction, the two-dimensional spin-orbit Hamiltonian is given as:

$$H_{SO}^{2D} = \alpha(-p_y\sigma_x + p_x\sigma_y) + \beta(-p_x\sigma_x + p_y\sigma_y) \tag{2.7}$$

with $p_i$ the spin's momentum due to motion in the $i$-direction, $\boldsymbol{\sigma}$ the Pauli spin matrices and $x$ and $y$ pointing along the crystallographic directions $[1, 0, 0]$ and $[0, 1, 0]$ respectively. Equation 2.7 illustrates that, depending on the direction of motion, the Rashba and Dresselhaus terms of the SOI will add, cancel, or are perpendicular, see Fig. 2.7a [145]. Therefore, the total SOI that an electron spin experiences is anisotropic. The SOI is expressed in the spin-orbit length, $l_{SO}$, the distance after which the spin rotated by an angle $\pi$.

Spin-orbit interaction contributes to electron spin relaxation mediated by electric field fluctuations. Although the electric field does not couple to the spin states directly, spin-orbit interaction couples the spin and orbital degrees of freedom [146], such that the eigenstates of the system are admixtures of the spin and orbital states which do couple to the electric field [147, 148].

Electric field fluctuations can either have an external (e.g. gate potential), or an internal origin (e.g. nearby quantum point contact [149], or background charge fluctuations [150]) and are dominated by the phonon bath [36]. Through so-called deformation potential phonons, the crystal lattice will be inhomogeneously contorted. This changes the bandgap of the host material, which gives rise to fluctuating electric fields [36]. In GaAs heterostructures, an additional contribution arises, where the piezo-electric effects causes homogeneous strain, leading to electric fields. Thus via SOI, the spin can couple to electric field fluctuations, giving rise to spin relaxation, see section 3.1.5.

The spin-orbit interaction differs per material. GaAs substrates give rise to both Dresselhaus and Rashba spin-orbit coupling. As silicon has a diamond lattice, there is bulk inversion symmetry. Therefore, silicon substrates do not exhibit Dresselhaus spin-orbit coupling and are only effected by the Rashba term [63].

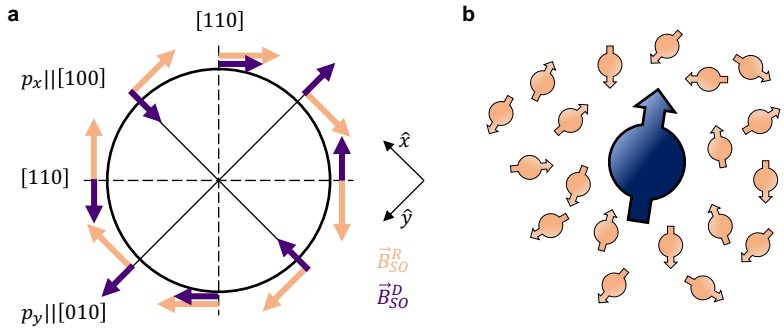


Figure 2.7.: **Interactions of the spin with the environment. a.** Representation of the effective magnetic field working on the spin as a result of the Rashba (orange) and Dresselhaus (purple) contributions to the spin-orbit interaction for a spin moving through an electric field with momentum **p**. In this figure $\alpha < 0$, $\beta > 0$, $\alpha \neq \beta$. Figure adapted from [151]. **b.** A spin in a semiconductor material will have hyperfine interaction with all non-zero spins in its surroundings.

### 2.4.2 Hyperfine interaction

The nuclei in the host material may contain non-zero spin isoptopes that can interact with the electron spin trapped in the quantum dot. The dominant effect is the hyperfine interaction. The strength of the hyperfine interaction between the electron and the $k_{\text{th}}$ nucleus in its surroundings is proportional to the overlap of the electron wavefunction and the wavefunction of the nucleus squared and is given by the Fermi contact hyperfine constant, $A_k$. The Hamiltonian for the total hyperfine interaction sums over all nuclear spins in the electron's surroundings:

$$H = \sum_k A_k \mathbf{I}_k \cdot \mathbf{S}, \tag{2.8}$$

with $\mathbf{I}_k$ and $\mathbf{S}$ the spin operators for the $k_{\text{th}}$ nucleus and the electron respectively [152]. It is convenient to interpret the effect of the nuclear spin ensemble as an extra magnetic field acting on the electron spin. This magnetic field, $B_N$, is called the Overhauser field [36]:

$$H = g\mu_B \mathbf{B}_N \mathbf{S}. \tag{2.9}$$

If the Overhauser field would be polarized or static, its effect on the electron spin could be calibrated and treated as an additional magnetic field. Yet both the orientation and the magnitude of the Overhauser field fluctuate and, in the presence of an external magnetic field, will follow a Gaussian distribution with width: $\sigma_N = \mathbf{B}_{N,max}/\sqrt{N}$ [153]. The random Overhauser field leads to phase randomization of the electron spin evolution and hence to decoherence [153–155].

Changes in the Overhauser field over time are caused by changes in $\sum_k A_k \mathbf{I}_k$. This can either be caused by a change in nuclear polarization ($\mathbf{I}_k$), as the result of a flip of a nuclear spin. Or this change can be induced by a flip-flop event. In this case, the net polarization stays the same, yet there is a flip-flop process between two nuclear spins that have a different overlap ($A_k$) with the electron spin. Usually, the Overhauser field fluctuates on a timescale slower than the electron spin, so the Overhauser field assumes a quasi-static random value. In GaAs devices, all atoms in the the host material have a nucleus with non-zero spin, thus the Overhauser field is high. The polarized Overhauser field can be as high as 5 T [156] and the randomized field is typically around 5 mT [153]. In natural silicon, there is an abundance of zero-spin nuclei, resulting in weaker Overhauser fields and longer coherence times. Additionally, silicon substrates can be purified such that the number of non-zero nuclear spins is just a few hundred ppm [94, 122], which reduces the Overhauser field to several $\mu$T [157].

Although hyperfine interaction limits spin coherence and is aimed to be suppressed as much as possible, it is demonstrated that in substrates with few nuclear spins, the hyperfine interaction can also be harnessed to employ nuclear spins as donor qubits [158].

### 2.4.3 Charge noise

As hyperfine interaction is suppressed, charge noise emerges as the dominant limitation of qubit coherence and gate fidelity [50, 159]. The main contributor to charge noise is the electric field noise caused by changes in the electrode potential, or by two-level fluctuators that reside in the stack, such as in the gate oxide [160]. Because each quantum dot couples to a different ensemble of specific two-level systems, the charge noise can vary per dot [161]. By the same token, different values of the gate electrode, or electron occupations may trigger specific two-level fluctuators, such that the charge noise in a quantum dot can even change per Coulomb peak, as demonstrated in chapter 7 of this thesis. Moreover, the screening effect that electrons provide, makes the charge noise decrease with quantum dot filling. Typically,

the noise is described with a power law that governs the entire relevant frequency bandwidth for the qubit ($\sim 10^{-3}$-$10^{6}$ Hz) [50, 160, 162]:

$$S(f) = \frac{A}{f^{\alpha}}, \tag{2.10}$$

where $A$ is the noise level at 1 Hz and $\alpha$ is between 0.5 and 2 [50, 118, 157, 160–163]. Generally, $\alpha = 1$, giving a $1/f$ noise spectrum. There are various physical mechanisms that result in the $1/f$ charge noise spectrum. A simple description simulates the two-level systems as two coupled potential minima. If the tunnel barrier height between the minima has a uniform distribution over the ensemble, the hopping rate between the two levels follows an exponential distribution, which accounts for a $1/f$ noise spectrum [164]. An $\alpha$-value larger than 1 suggests the domination of a single two-level system, for example caused by the fluctuators being in the vicinity of the quantum dot. As the two-level fluctuators are thermally activated, the charge noise behaviour over temperature is of interest for operating qubits at higher temperatures. Yet, to date, no clear temperature dependence of the noise has been found, varying from a linear [163], or quadratic [118] increasing noise power with temperature, to a nonmonotonic temperature dependence [161]. These different characters of the noise may be due to the variety in the number and the activation energy of relevant two-level fluctuators [165]. Charge noise can be measured either by measuring the noise on a Coulomb peak flank in a transport measurement, or by analysing the dynamical decoupling curves of a qubit.

## 2.5 VALLEY SPLITTING

The conduction band minimum for Si samples is located at 85% of the Brillouin zone[2], whereas the valence band maximum is located at the center of the Brillouin zone. Thus Si has an indirect band gap. As silicon has cubic bulk symmetry, this conduction band minimum is six-fold degenerate; it consists of four $\Delta$-valleys ($\hat{k}$=$\pm\hat{x}$, $\pm\hat{y}$) and two $\Gamma$-valleys ($\hat{k} = \pm\hat{z}$). The valley degeneracy can be lifted either by strain, by confinement of the wave function, or by electric fields.

Due to confinement and, in the case of Si/SiGe, biaxial tensile strain[3], the four in-plane $\Delta$ valleys are lifted by tens of meV [166]. The degeneracy of the two lower-lying $\Gamma$ valleys can be split by confinement in the 2DEG against a sharp and flat interface and by additional electric fields in the $\hat{z}$-direction [63], see Fig. 2.8a. The splitting of the $\Gamma$-valley degeneracy, often called valley splitting, is typically in the order of $0 - 800$ $\mu$eV. As this is smaller than the orbital splitting of the quantum dot, the valley splitting is a crucial metric in silicon quantum information processing. A small valley splitting may break the promise of a well-defined two-level system. First of all, for small valley splitting, valley states may be thermally accessible. This causes leakage of the qubit information and hinders not only the qubit's initialization, manipulation and readout fidelity [167], but this valley hopping also limits the coherence time of the qubit. Moreover, the extra degree of freedom that the valley splitting brings may lift Pauli

[2] $k \approx \pm 0.85 \times \frac{2\pi}{a}$, with $a$ the lattice constant of silicon

[3] Due to the 4% lattice mismatch between Si and Ge this strain is inherently induced.

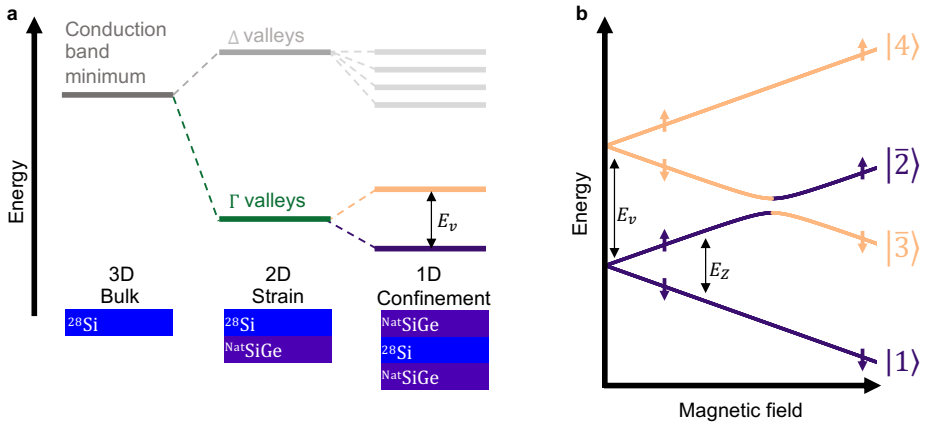


Figure 2.8.: **Valley splitting. a.** The splitting of the six degenerate valley states in silicon as a result of strain and confinement. **b.** Energies of spin up and spin down electrons in the two lowest valley states as a function of magnetic field. As the magnetic field increases, the Zeeman splitting increases. Spin-orbit coupling and valley-orbit coupling may induce spin-valley coupling, which peaks when $E_z = E_v$.

spin blockade. This both impedes PSB readout, as well as two-qubit control that is based on the exchange interaction between two qubits [97, 98, 168].

Via spin-orbit coupling and valley-orbit coupling, the second-order process of spin-valley coupling may occur. When $E_{orb} > E_v$, the system can be described by the Zeeman levels of the first valley ($|1\rangle$ , $|2\rangle$) and the Zeeman levels of the second valley ($|3\rangle$ , $|4\rangle$) [117, 118]:

$$H = \sum_i \frac{E_i}{2} |i\rangle \langle i| + \Delta_{23} |v_1 \uparrow\rangle \langle v_2 \downarrow| , \tag{2.11}$$

where the first term describes the four separate valley states and the latter term the SOI-mediated spin-valley mixing with $\Delta$ the coupling strength [4]. Due to the spin-valley coupling, the eigenstates of the system will be admixtures of $|2\rangle$ and $|3\rangle$ (Fig. 2.8b):

$$|\bar{u}\rangle = \left( \sqrt{\frac{1-a}{2}} |u\rangle - \sqrt{\frac{1+a}{2}} |w\rangle \right), \tag{2.12}$$

with $u, w = 2, 3$ and $a = -(E_v - E_Z)/\sqrt{(E_v - E_Z)^2 + \Delta^2}$. In the presence of an electric field, such as phonons or Johnson noise from the 2DEG, the spin-valley mixing contributes to spin flip processes. The relaxation rate depends on both the relaxation rate of the valley and the relaxation due to spin-valley mixing and is maximal when $E_Z = E_v$, where the spin relaxation is completely determined by the fast inter-valley relaxation [117].

As a large valley splitting implies operation at higher temperatures, better qubit control and longer coherence times, the field would benefit from large valley splitting. Yet, valley splitting is a complex parameter to control. It is mainly determined by disorder on the atomic

[4] Officially, there is also a mixing term for states $|1\rangle$ and $|4\rangle$, yet as these states are well-separated, this term can be neglected

interface, a scale much smaller than the few nm-scale that is controlled in sample fabrication. One of the main contributions of disorder are the atomic interface steps, where the thickness of the quantum well changes on the length-scale of the quantum dot diameter. As a consequence, the wave function confinement changes per step and valley-orbit coupling is induced [169]. Valley splitting is linearly dependent on electric fields and has been controlled by adjusting the bias on the gate electrodes both in SiMOS [117] and in SiGe [170].

# 3 SPIN QUBITS IN LATERAL QUANTUM DOTS

*We begin with a spin,*
*Travelling in the world of our creation*

Willy Wonka

*This chapter explores the spin confined in an electrically-defined quantum dot as a qubit. By means of the DiVincenzo criteria, we analyse the most common techniques for spin qubit initialization, manipulation and readout and hold these techniques against the light of scaling. Moreover, we discuss what determines the relevant timescales for spin qubits and how the quality of the qubit can be analysed.*

## 3.1 SPIN QUBITS

The translation from quantum computing theory to the physical implementation of a quantum computer requires the underlying qubit system to adhere the DiVincenzo criteria [37] (see section 1.2.1). There are several ways to leverage the spin of an electron captured in quantum dots as a quantum hardware platform that meet the DiVincenzo critera. First, there is the singlet-triplet qubit, that encodes the qubit in the singlet and triplet state of two electron spins residing in two quantum dots [77, 171]. Secondly, the exchange-only qubit encodes the qubit in certain spin configurations of three electrons in three quantum dots [172, 173]. Moreover, there are the quantum dot hybrid qubit, where three electrons are divided over two quantum dots [174, 175], and the quadrupolar-exchange-only qubit where the computational basis consists of certain states of four electrons over three quantum dots [176]. The advantage of multi-dot qubits, is that these larger systems usually simplify the experimental requirements (e.g. merely electrical operation, thus no magnetic field required). Moreover, each system offers protection against a different types of decoherence. The price for this is a higher qubit leakage to non-computational states. Moreover, multi-dot qubit systems require more resources per qubit, both on the chip and for qubit control.

In this thesis, we use the spin degree of freedom of a single electron as compuational basis. As this qubit was first proposed by Loss and DiVincenzo [48], it is sometimes referred to as Loss-DiVincenzo qubit, but it is often simply called a spin qubit. Advantages of spin-qubits are their relative simplicity and weak coupling to electric and magnetic field-fluctuations. Over the last two decades, spin qubits have been convincingly proven to fulfill to the five DiVincenzo criteria [37]: high-fidelity readout, initialization and single- and two-qubit gates above the error-correction theshold have been demonstrated, while the qubit coherence time is relatively long. In this section, we will discuss these five critera for spin qubits.

### 3.1.1 Electron spins: a well-defined two-level system

A functional qubit requires a well-defined two-level system in which the orthogonal computational basis states, for example $|0\rangle$ and $|1\rangle$, can be encoded. The spin degree of freedom of an electron naturally satisfies this specification. The electron spin state is a minuscule intrinsic magnetic moment [177, 178], of which the eigenvalues are either $-\frac{1}{2}\hbar$, or $\frac{1}{2}\hbar$, more commonly known as 'spin down' ($|\downarrow\rangle$) and 'spin up' ($|\uparrow\rangle$) respectively. As spin has a quantum-mechanical nature, the spin can also be in any arbitrary superposition of $|\uparrow\rangle$ and $|\downarrow\rangle$: $\alpha|\uparrow\rangle + \beta|\downarrow\rangle$. The electron spin states are degenerate, but, as the spin up and spin down state have opposite magnetic orientation, this degeneracy can be lifted by the application of a magnetic field, separating the spin states by the Zeeman energy splitting:

$$\Delta E_Z = g\mu_B B. \tag{3.1}$$

Here, $\mu_B$ is the Bohr magneton, $B$ the applied magnetic field and $g$ is the Landé g-factor. The latter is material dependent, resulting in $|\uparrow\rangle$ being the ground state in GaAs heterostructures, because the Landé g-factor is negative ($g = -0.44$) whereas $|\downarrow\rangle$ is the ground state in silicon-based samples ($g \approx 2$). The $|\uparrow\rangle$ and $|\downarrow\rangle$ states are orthogonal and hence form

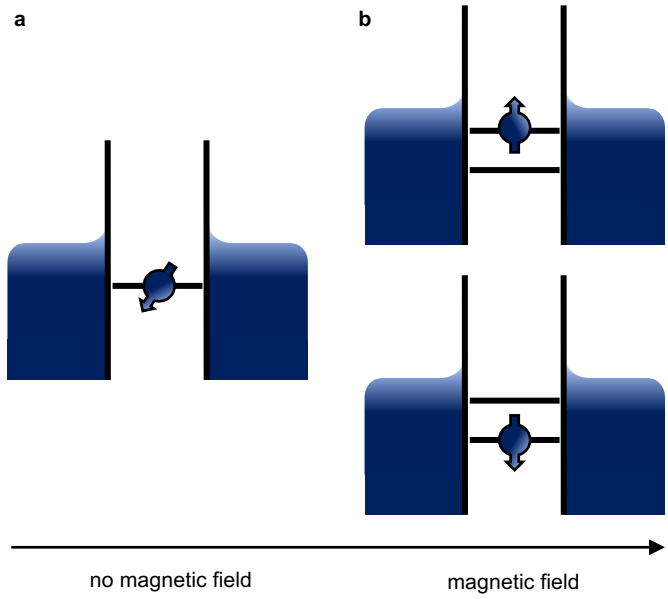


Figure 3.1.: **Zeeman splitting. a.** In the absence of a magnetic field, the spin up and spin down states of the electron are degenerate. **b.** Due to the application of a magnetic field, the spin up and spin down states have an energy splitting proportional to the strength of the magnetic field.

a computational basis for the qubit, where we assign the ground state as $|0\rangle$ and the first excited state as $|1\rangle$, see Fig. 3.1.

### 3.1.2 Spin-qubit readout

Fast, reliable and scalable measurement of the spin state is crucial for both scientific purposes, as for quantum computation. Since the qubit is encoded in a single spin, the measurement has to be single-shot and, consequently, high-fidelity [73]. Especially when scaling up and quantum error-correction codes come into play, minimum fidelities of 99% are required for readout in timescales shorter than the spin coherence time, to allow for repetitive measurements. A challenge is posed by the tiny magnetic moment of the spin, which makes direct readout of the spin state difficult. Instead, we map the spin states onto different charge states in the quantum dot and subsequently read out the charge state [48]. Such spin-to-charge conversion has been the conventional spin-qubit readout approach for years and several readout protocols have been developed. Here, we discuss two types of single-shot readout, most commonly used for spins in quantum dots: spin-selective tunnelling and Pauli spin blockade readout.

*Spin-selective tunnelling*

Spin-selective tunnelling, first proposed by [179] and first demonstrated by [75], exploits the difference in energy between the spin up and the spin down state for spin-to-charge con-

version. For spin-selective tunnelling, the spin-up and spin-down levels are separated by a magnetic field and aligned around the Fermi level such that the Fermi level falls within the two spin levels. Consequently, a spin-up electron can tunnel out of the quantum dot into the reservoir, whereas for a spin-down electron, this is highly implausible[1], see Fig. 3.2 for the readout sequence for spin up (top) and spin down (bottom). Thus, the charge occupation of the quantum dot will depend on the spin state of the electron. For a spin-down electron, the charge occupation is constant, meaning the charge-sensing signal remains unaltered. After a spin-up electron tunnels out of the quantum dot, Coulomb blockade is lifted and a spin-down electron can tunnel into the dot. Therefore, the quantum dot will eventually end up with an electron in the spin-down state. Both tunnelling events, the spin-up electron leaving the dot and the spin-down electron entering, cause a change of charge in the quantum dot. These changes cause in a 'blip' in the charge sensing signal that can be detecting by means of thresholding.

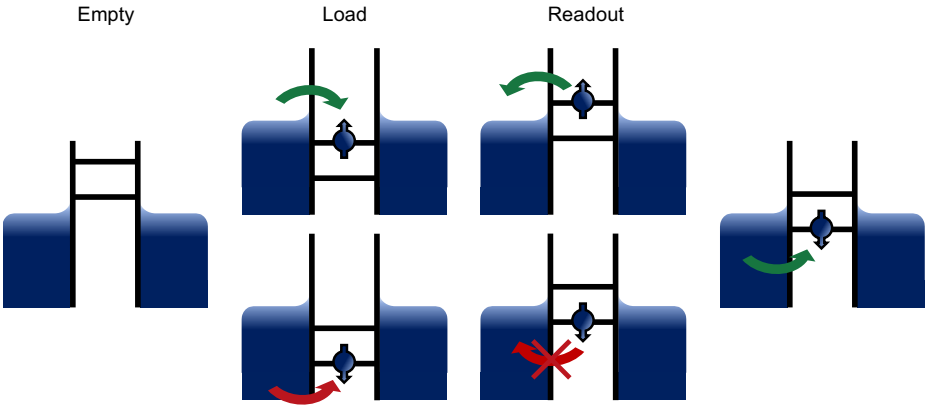


Figure 3.2.: **Spin to charge conversion by means of 'Elzerman readout'.** The spin state of an electron in a quantum dot adjacent to a reservoir can be detected by means of energy-selective tunnelling. The readout position is calibrated such, that a spin-up electron can tunnel out of the quantum dot (top), while for a spin-down electron, tunnelling is prevented (botton). The tunnelling events will induce a charge transition in the quantum dot, which can be detected by a nearby charge sensor. After the tunnelling of a spin-up electron into the reservoir, a spin-down electron can be loaded in the quantum dot. Thus, regardless of the spin state, after the readout, the quantum dot will contain a spin-down electron.

The measurement fidelity, a measure of whether the measured outcome corresponds to the actual spin state, is determined by two types of errors for spin-selective tunnelling; (i) a false-positive, in which a blip is detected, even though the electron was spin down ($\alpha$) and (ii) false negative, when a spin-up state remains undetected ($\beta$). Generally, $\alpha$-errors are caused by thermal excitations of spin-down electrons ($\alpha_1$), or by noise pushing the signal beyond the threshold value ($\alpha_2$), whereas $\beta$-errors can be caused by relaxation of the spin-up state ($\beta_1$), or when the tunnelling of the spin-up electron out of and back into the quantum dot is too fast to detect ($\beta_2$). The total readout fidelities are given as:

[1] Note that for GaAs the Landé g-factor is negative, thus $|\downarrow\rangle$ is the excited state that can tunnel out and $|\uparrow\rangle$ is the ground state that is caught in the quantum dot.

$$F_{\uparrow} = 1 - \beta \approx (1 - \beta_1)(1 - \beta_2) + \alpha_2\beta_1$$
$$F_{\downarrow} = 1 - \alpha \approx (1 - \alpha_1)(1 - \alpha_2) + \alpha_1\beta_2 \tag{3.2}$$

High-fidelity spin-selective tunnelling readout requires careful alignment of the spin levels with respect to the Fermi level. Moreover, it requires a stable system; background fluctuations can either change the calibration of the electrochemical potential, or can cause an $\alpha$-error via photon-assisted tunnelling through high-frequency noise. To prevent $\alpha$-errors, the Zeeman energy needs to exceed the thermal broadening of the electrons in the reservoir ($\Delta E_Z \geq k_b T$); imposing both a high magnetic field and a low electron temperature. To minimize $\beta$-errors, the readout time should exceed the tunnel time of the spin. Moreover, the relevant tunnel times of the spin should be tuned to match the bandwidth of the measurement electronics.



*Pauli spin blockade readout*

Pauli spin bloackade (PSB) readout is based on the Pauli exclusion principle, which states that the fermionic wavefunction is antisymmetric [180]. This means that two electrons with symmetric spin states cannot reside on the same orbital, whereas two electrons with antisymmetric spin states can. PSB readout requires two quantum dots, for which the highest-filled orbital is occupied with a single electron. Usually, the quantum dots are occupied with one electron each, leaving the system in the $(1, 1)$-regime. These two electrons will either form a singlet- or a triplet state. For PSB readout, the system is pulsed from the $(1, 1)$ to the $(2, 0)$-regime. When the electrons form the antisymmetric singlet state, this transition is allowed, inducing a charge transition and hence a step in the charge sensing signal. However, when the electrons form a triplet state, the Pauli exclusion principle states that the electron has to occupy the next orbital, which is energetically inaccessible. Hence, for a triplet, the system will remain in the (1,1)-regime. The state of the system can be determined by thresholding the integrated sensor signal. Figure 3.3 shows a schematic of the PSB readout sequence.

The measurement fidelity for PSB readout is dominated by $\alpha$-errors, caused by singlet-triplet relaxation, which causes a triplet states to relax into a singlet state and to be detected as such. Interestingly, this relaxation can be used as a feature. When singlet-$T_0$ relaxation is sufficiently fast compared to the relaxation of $T_+$ and $T_-$, the PSB protocol can be used for parity readout, distinguishing the parallel states from the antiparallel states [181].

High-fidelity PSB readout requires careful calibration of the readout point; once the detuning exceeds the singlet-triplet splitting ($E_{ST}$), the triplet state is energetically accessible and PSB is lifted. Moreover, PSB can be lifted by the accessibility of low-lying valley states. A large valley splitting is therefore advantageous for high-fidelity PSB readout. In SiGe samples, where the valley splitting is typically lower than in SiMOS samples, this problem is sometimes circumvented by performing PSB readout on the $(3, 1) - (4, 0)$ anticrossing.

Lately, methods have been developed to improve the signal-to-noise ratio of the PSB sensing signal and hence increase the readout fidelity. Both methods are based on the conditional tunnelling of a third electron to a nearby quantum dot. For latched PSB readout,

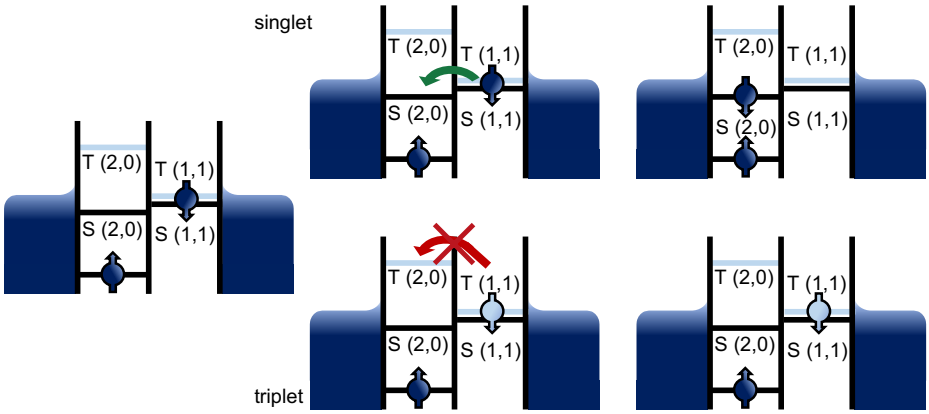


Figure 3.3.: **Spin to charge conversion by means of PSB readout.** Electrons in a singlet configuration can recombine in the first dot (top), whereas two electrons in the triplet configuration need ot occupy different orbitals. As the next orbital is energetically inaccessible, the triplet state is prohibited from recombination in the same dot. The tunnelling event of the singlet state will induce a charge transition that can be detected by the sensing dot.

the readout position is tuned such, that an extra electron will tunnel in from the reservoir if a singlet is being detected; instead of $(1,1)-(0,2)$, the readout will be $(1,1)-(1,2)$ [182]. For cascade readout, the singlet transition causes a nearby electron in a third quantum dot to tunnel to a fourth quantum dot: $(1,1,1,0)-(0,2,0,1)$ [88]. This method can be extended to more spins in even larger quantum dot arrays, giving rise to an electron cascade, analogous to toppling dominoes. Both methods can achieve fidelities over 99%.

For the implementation of larger qubit arrays, PSB readout is often preferred over Elzerman readout. Although Elzerman readout is relatively simple and requires only a single-quantum dot, it might not be suitable for scaling-proof quantum computing protocols. Firstly, high-fidelity readout requires a high magnetic field, which translates to high-frequency operation and limits the measurement to low-temperature operation. Secondly, the readout scheme requires the quantum dot to reside next to a reservoir which may be problematic for the readout of spin states in the center of a long quantum dot array. Although this problem can be circumvented by shuttling electrons spins to quantum dots that border a reservoir [81]. Finally, due to the necessity to detect the charge jump caused by an electron jumping out of the quantum dot, the tunnelling rate to the reservoir should not exceed the measurement bandwidth for Elzerman readout. This may result in relatively slow readout, which is a show-stopper for quantum algorithms that require feedback. Although PSB readout demands two quantum dots, it does not require a reservoir. Consequently, the readout can be performed anywhere within the array and the spins do not suffer from reservoir broadening and the readout can be performed at relatively high temperatures [123, 124]. Moreover, the Zeeman splitting does not need to be large, making that the readout can be performed while operating the qubit using relatively low frequencies. Also, if the singlet-triplet relaxation time exceeds the measurement time, the readout preserves the singlet/triplet spin states.

### 3.1.3 Qubit Initialization

The third requirement for viable quantum computers is the ability to initialize the qubit in a well-defined state. For spin qubits in lateral quantum dots, there are several methods for initialization [73]. Firstly, the qubit can be initialized through relaxation into its ground state. In case of a single qubit in silicon, this would be spin down. However, as relaxation times for spin qubits can be orders of magnitude longer than other relevant qubit timescales, even exceeding a second at typical operating fields of 1 T [69, 70, 170, 183–185], this method is time-consuming. The process can be expedited significantly by finding a relaxation hotspot, for example mediated by the orbital splitting, or the valley splitting, such that initialization can be achieved in microseconds [117, 186]. Secondly, singlet-triplet relaxation can be used for initialization. For two spins in a double quantum dot, the spins can be moved to the same quantum dot. Relaxation to the singlet ground state is usually in the orders a few to hundreths of microseconds for silicon [53]. Also this relaxation involves a spin flip. But since the singlet-triplet energy separation is larger than the Zeeman splitting, relaxation singlet-triplet relaxation rates are higher than single spin relaxation rates. Initialization in either the singlet state, or the antiparallel spin state can be achieved, by respectively ramping the spin back over the anticrossing adiabatically, or non-adiabatically. A third option for initialization is initialization through readout. As described in section 3.1.2, Elzerman readout leaves the quantum dot filled with a spin in the ground state. Whereas PSB readout distinguishes the singlet from the triplet state (3.1.2). Furthermore, one could deterministically load a spin in the ground state by adiabatically pulsing the spin levels through the Fermi level. However, this either requires the quantum dot to border on a reservoir, or the spin to be shuttled to the desired location [81]. As qubit systems grow, quantum non-demolition measurements are getting feasible [187–189]. For non-demolition measurements, the qubit is entangled with an ancilla qubit. When the ancilla qubit is read out, the wavefunction of the entangled qubit is projected in a state that depends on the measurement outcome. Conditional rotations can bring the qubit in the desired initial state [189]. Non-demolition measurements are a fundamental part of quantum error correction codes and as qubit systems grow, this type of initialization will become increasingly attractive.

### 3.1.4 Quantum logic gates

Performing operations to every possible qubit combination is at the heart of quantum information processing. A requisite for every qubit system is therefore to provide a universal set of quantum logic gates; a minimum set of gates that can take a qubit in an arbitrary input state to any state in the system's $2^N$-dimensional Hilbert space[2]. For quantum-dot based spin qubits, transitions between the basis states, such as the Zeeman-split spin up and spin down states, can be driven by applying an ac magnetic field in resonance with, but perpendicular to the external magnetic field. This can be illustrated for a spin $|\downarrow\rangle$, where the Hamiltonian is defined as $H = \hbar\omega(|\uparrow\rangle\langle\uparrow| - |\downarrow\rangle\langle\downarrow|)$, with $\omega$ the Larmor frequency as determined by the Zeeman

[2] A universal set of quantum logic gates usually consists of two rotations along orthoginal axes and a two-qubit gate [28]

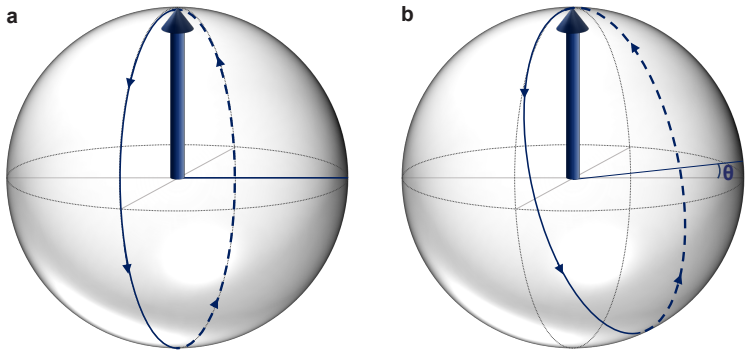


Figure 3.4.: **Qubit rotations in the rotating frame. a.** An on-resonance microwave burst is static with respect to the Larmor precession and it will rotate the qubit about an axis on the equator of the Bloch-sphere; the phase of the microwave burst will determine the axis. **b.** Once the driving frequency is slightly-off-resonant, the drive will have an offset with respect to the Larmor frequency, effectively driving the qubit around a tilted axis. The angle, $\theta$, of the axis depends on the quantity of the frequency offset.

splitting. When we apply a drive with power $A$, frequency $\omega_d$ and phase $\phi$, $A\cos(\omega_d t + \phi)$, the Hamiltonian in the rotating frame is:

$$H = \hbar(\omega - \omega_d)(|\uparrow\rangle\langle\uparrow| - |\downarrow\rangle\langle\downarrow|) + \hbar\Omega e^{i(\omega_d-\omega)t+\phi}|\downarrow\rangle\langle\uparrow| + \hbar\Omega^* e^{i(\omega-\omega_d)t+\phi}|\uparrow\rangle\langle\downarrow|, \tag{3.3}$$

with $\Omega$ the oscillation frequency between $|\downarrow\rangle$ and $|\uparrow\rangle$ and $\Omega \sim A$ [190]. When driving on resonance, $\omega_d = \omega$,

$$H = \hbar\Omega|\downarrow\rangle\langle\uparrow| + \hbar\Omega^*|\uparrow\rangle\langle\downarrow|. \tag{3.4}$$

As an effect, the spin will start rotating about the x-axis at a frequency $\Omega$, also referred as the Rabi frequency [28]. This can most intuitively be understood in the rotating frame. As the driving field is rotating with the Larmor precession, both fields are static with respect to the rotating frame, see Fig. 3.4a. The perpendicular component of the drive resonantly causes the spin to oscillate between the up and down levels. When the drive frequency is tuned away from resonance, the drive will acquire an offset $\delta\omega$ with respect to the Larmor frequency, causing the spin to rotate around a tilted polar axis and the Rabi frequency $\Omega_R$ to increase[3], as depicted in Fig. 3.4b. When the drive frequency is completely off-resonant, the spin will be randomly pushed around in the rotating frame and its motion averages out. The Rabi frequency, $\Omega$ and the angle over which the qubit rotates are determined by the amplitude and duration of the microwave burst. Rotation about a different azimuthal axis, can be achieved by changing the phase of the microwave burst. Transitions between Zeeman-split levels can be accomplished either directly, via Electron Spin Resonance, or indirectly, via Electric Dipole Spin Resonance. Although EDSR usually drives the spin faster, both ESR techniques and EDSR techniques have already demonstrated single-qubit gate fidelities over 99.9% in silicon [50, 67].

[3] $\Omega_R = \sqrt{\Omega^2 + \delta\omega^2}$

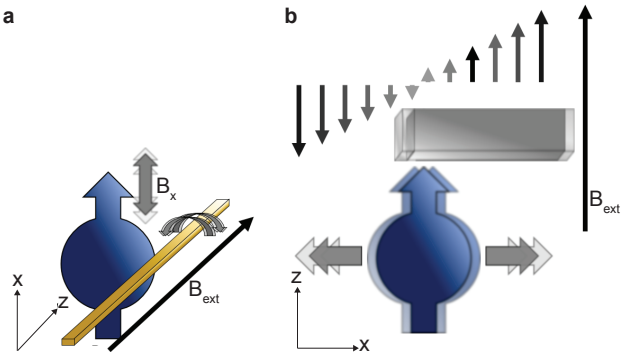


Figure 3.5.: **Qubit driving mechanisms: ESR and EDSR. a.** Driving the qubit with ESR. An oscillating current through a stripline in the vicinity of the quantum dot. This oscillating current will induce an oscillating magnetic field, which rotated the qubit. **b.** Qubit driving by means of EDSR. For EDSR, the environment of the qubit should contain an (artificial) magnetic field gradient. When a drive is applied on a gate electrode that is capacitively coupled to the qubit, the qubit will feel an oscillating magnetic field. This causes the qubit to move in the magnetic field gradient and hence feel an effective oscillating magnetic field.

*Electron Spin Resonance*

Electron Spin Resonance (ESR) drives the qubit directly by means of an oscillating magnetic field [78]. The oscillating magnetic field is generated by sending an oscillating current through a shunted coplanar waveguide, often called stripline [191], such that the oscillating magnetic field is directed perpendicular to the Zeeman splitting (Fig. 3.5a). Striplines are relatively easy to fabricate. Yet, the oscillating magnetic field through the stripline may cause local heating of the qubits, especially if the stripline is not superconducting. This sets limitations to the applied power and hence to the Rabi frequency. Moreover, striplines do not provide local qubit addressability. Once multiple qubits are considered, individual qubit driving may become challenging, as in some systems such as silicon, qubits may have the same g-factor and are exposed to the same external magnetic field. As confining the driving magnetic field to one qubit at a time is unattainable, the solution is found in adjusting the individual qubit frequencies slightly with respect to each other, giving them all a unique Larmor frequency. In GaAs and Ge samples, this addressability is naturally achieved either by the Overhauser field, or by g-factor tuning. As in silicon these effects are minimal, qubit addressability may need to be artificially added.

*Electric Dipole Spin Resonance*

Electric Dipole Spin Resonance, or EDSR, drives the spin indirectly by means of an oscillating electric field, mediated by spin-orbit coupling or by a magnetic field gradient perpendicular to the Zeeman splitting. The electric field, applied to one of the top gates, wiggles the electron wavefunction backwards and forwards. Consequently, the moving electron will effectively sense an oscillating magnetic field (Fig. 3.5). In materials with a strong spin-orbit coupling,

this spin-orbit coupling can be used to rotate the spin [130, 145]. In silicon samples, however, the tiny spin-orbit coupling does not produce a significant effective magnetic field and artificial spin-orbit coupling can be introduced by means of a micromagnet [167, 192–195]. Although micromagnets mimic the spin-orbit coupling and will therefore contribute to spin relaxation (see section 3.1.5) [69], they allow for Rabi frequencies up to tens of MHz. Moreover, when a micromagnet is applied, qubit addressability can be engineered by means of a magnetic field gradient in the direction of the external magnetic field. This gradient makes each qubit experience a slightly different magnetic field, altering its Zeeman splitting up to about 100 MHz. This bandwidth is sufficient for a proper multi-qubit design; qubits that are separated further than the range of a microwave burst, may contain similar Zeeman splittings.



*Two-qubit gates*

Two-qubit gates can be realized by tuning the overlap of the wavefunctions of two electrons, which gives rise to the exchange interaction $J$ acting on the spins. The exchange interaction can be tuned, either by changing the tunnel coupling $t_c$ between the dots, or by adapting the detuning $\epsilon$. The type of two-qubit gate that is performed, depends on the ratio of the exchange interaction with respect to the difference in Zeeman energy between the two dots: $J/\Delta E_Z$ [196]. Three relevant regimes can be distinguished [197]. When the exchange interaction is pulsed from $J = 0$ to $J >> \Delta E_Z$, the eigenstates of the system change from the up-down basis to the singlet-triplet basis. By controlling the timing of the singlet-triplet oscillations and pulsing back to $J = 0$, the SWAP-gate between $|\uparrow\downarrow\rangle$ and $|\downarrow\uparrow\rangle$ and the entangling $\sqrt{\text{SWAP}}$ gate can be performed [77, 79, 197]. The CROT gate can be performed when the eigenbasis is close to the up-down basis and $J > 0$. By turning on the exchange interaction, the wave functions of the spins start to slightly overlap. This makes the energy of the $|\downarrow\uparrow\rangle$ and $|\uparrow\downarrow\rangle$ states decrease, such that the frequencies between each eigenstate is unique. A CROT gate can be performed, by selectively driving single-qubit transistions between these states with an external microwave source [95, 124, 125, 197, 198]. In the same regime, the CPHASE gate can be performed [51, 104, 199]. By adiabatically pulsing the systems such that the exchange is on, where the antiparallel eigenstates will acquire a phase compared to the parallel spin states, the CPHASE gate is performed when their respective phase $\phi_1 + \phi_2 = \pi$. Due to the local magnetic field gradient, CPHASE and CROT gates are naturally implemented in the presence of a micromagnet [196]. Both the CROT gate and the CPHASE gate yield a CNOT gate up to single-qubit rotations. Recently, a conditional four qubit gate has been performed [72].

### 3.1.5 Relevant and relatively-long coherence times

Even when qubits can be initialized, manipulated and read out, meaningful quantum computation only flourishes when the qubit system can preserve its quantum state long enough for a considerable number of operations to be performed. Qubit fragility originates in coupling of the qubit to the environment. Electron spins can couple to the environment via spin-orbit interaction and hyperfine interaction with the nuclear spin bath. A key challenge in quantum

computation is therefore to engineer the environment of the qubit such that the noise is minimal, while not annihilating the interaction with the environment completely, such that the qubit can still interact with the measurement electronics.

Coupling of the spin to the environment causes the spin to lose its quantum information and become a statistical mixture of several states [28]. There are two relaxation mechanisms that the spin is subject to that each have their specific timescales [200]. Firstly, there is relaxation along the polar axis of the Bloch sphere, or longitudinal relaxation, which describes the qubit decay from the excited state ($|1\rangle$) to the ground state ($|0\rangle$), as depicted in Fig. 3.6a. The corresponding timescale, $T_1$, can exceed seconds in quantum dot samples. The second relaxation mechanism is relaxation around the azimuthal axis, also transversal relaxation, or decoherence, which describes the timescale, $T_2$, on which the phase of the qubit randomizes, due to environmental fluctuations (Fig. 3.6b). Theoretically, $T_1$ dictates the upper bound for $T_2$ as $T_2 \leq 2T_1$ [36]. For spin qubits, $T_2$ is typically one to several orders of magnitude smaller than $T_1$, making the coherence time the limiting timescale.

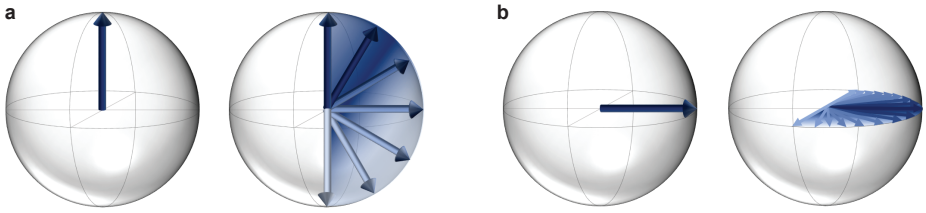


Figure 3.6.: **Qubit relaxation mechanisms. a.** Longitudinal relaxation of the qubit. The qubit state will relax from the excited state $|1\rangle$ to the ground state $|0\rangle$, with the corresponding timescale $T_1$. **b.** Transversal relaxation of the qubit. A qubit in superposition will lose its phase information.

*Relaxation time*

The primary source of spin relaxation is the electric field fluctuations, coupled to the qubit through the spin-orbit interaction (see section 2.4.1) mainly caused by the phonon bath that absorbs the spin energy upon relaxation. Additional, yet less dominant factors that can contribute to spin relaxation, are the hyperfine interaction, which can be almost eliminated in purified Si, and the spin-valley interaction. The hybridization of valley states results in a relaxation hotspot [117]. This causes the electric field fluctuations to couple (indirectly) to the spin, via the electron's valley, and cause relaxation (section 2.5 and chapter 7). This effect is absent in GaAs samples. Finally, virtual tunnel processes to the reservoir can cause relaxation, but this exchange can be sufficiently suppressed by tuning. Since the spin-orbit coupling is indirect and silicon has a large band gap, the spin-orbit interaction in silicon devices is rather weak, which allows for a long $T_1$. Micromagnets provide an artificial spin-orbit coupling and hence influence the relaxation time [69]. Still, especially in silicon, relaxation times can reach the order of seconds [70, 185] (chapter 7).

*Coherence time*

The major source of dephasing for solid-state spin qubits is the hyperfine interaction between the spin and the surrounding nuclear spin bath of the host material (section 2.4.2). The Overhauser field, induced by the nuclear spins, couples to the spin and the time-fluctuations of the Overhauser field randomize the Larmor frequency of the qubit. As a consequence, the pure qubit state evolves into a statistical mixture of multiple states and hence dephases [28]. The decay time during free evolution of the spin is called $T_2^*$. $T_2^*$ can be measured by means of a Ramsey experiment: the spin is pulsed to superposition, where it can evolve freely for time $\tau$. The spin is read out after pulsing it back to one of the poles [36]. Ramsey experiments are sensitive to low-frequency, or quasi-static noise [201] and the coherence time can be extended by means of echo pulses. By using a refocusing $\pi$-pulse at precession time $\tau/2$, the effects of the quasi-static field on the phase of the spin can be partly eliminated [202]. This is called the Hahn echo, characterized by $T_{2,Hahn}$ [203]. Increasingly higher frequencies can be (partially) cancelled out by using an increasing number of $\pi$-pulses within the evolution time $\tau$, leading to increasingly higher coherence times. The most well-known example of such a pulse scheme is the Carr-Purcell-Meiboom-Gill (CPMG) sequence, $T_{2,CPMG}$ [204, 205], where the $\pi$-rotations may be either about the $x$-axis or $y - axis$ of the Bloch sphere, or alternately about both.

In GaAs heterostructures, each Ga and As isotope contains a non-zero nuclear spin. This abundance of nuclear spins limits the coherence time of the qubits significantly. Generally, $T_2^*$ in GaAs reaches tens of nanoseconds [78, 90, 206]. Silicon naturally contains only 5% non-zero-spin isotopes, which allows for significantly higher coherence times of around 1 $\mu$s. In purified silicon, with only 8 ppm nuclear spins, $T_2^*$ is further increased by one to two order of magnitude and the coherence time can be even extended to $T_{2,CPMG} =$ 28 ms [49]. Once the nuclear field fluctuations have been sufficiently suppressed, the main source for decoherence is charge noise [50]. Charge noise is caused by defects and two-level fluctuators in the sample that mainly reside in the gate oxide and at the semiconductor-oxide interface.

*Quality factor*

Although both the relaxation time and coherence time are relevant timescales for quantum computation, it is important to place them into perspective. Coherence times of different qubit platforms can vary by orders of magnitude; transmon qubits, which are $T_1$-limited, usually maintain their coherence in the order of tens of microseconds [207] and silicon spin qubits have a coherence time of milliseconds [49], whereas ion traps can have coherence times exceeding several minutes [208]. Yet all three platforms have the potential to form the basis of large-scale quantum computers. Therefore, not only the coherence time itself, but also two other quantities are meaningful qubit benchmarks. Firstly, the number of operations that can be performed before the qubit decoheres. This ratio of the number of operations and the coherence time gives the quality factor of the qubit, or $Q$. Moreover, the success rate, or Fidelity, of the qubit operations is a crucial qubit metric.

# 4 EXPERIMENTAL SETUP AND METHODS

*A goal without a plan is just a wish*

Le Petit Prince

*This chapter describes the experimental setup that we used for the work in this thesis, as well as the experimental methods.*

## 4.1 SAMPLE DESIGN

Electrically-defined quantum dots can be formed in various host materials, as described in chapter 2. In this thesis, we work with samples on three different heterostructures: GaAs/AlGaAs, Si/SiGe and SiMOS, see Fig. 4.1. The samples on the GaAs/AlGaAs and Si/SiGe heterostrucutres are fabricated in an in-house cleanroom, whereas the sample on the SiMOS stack is fabricated in a 300-mm, industrial cleanroom. All three samples are linear arrays; Fig. 4.1 respectively depicts a GaAs/AlGaAs linear 8-dot device, a SiMOS 3-dot sample and a Si/SiGe 5-dot design. All three devices contain small metallic top gates that are used to shape the potential landscape. The gates serve alternately as barrier gates and plunger gates. Plunger gates control the electrochemical potential in the quantum dot, whereas barrier gates regulate the tunnel coupling between the quantum dot and an adjoining reservoir [62], or between two neighbouring quantum dots. On the sides, metallic contacts, known as ohmic contacts, are implanted in the samples, to allow for transport measurements.



There are several design constraints that one has to consider while fabricating a sample on one the these stacks. First of al, GaAs samples are usually operated in depletion mode, whereas samples on silicon stacks are operated in accumulation mode [64]. The AlGaAs part of the GaAs/AlGaAs heterostructure, as depicted in chapter 2, is n-doped with silicon dopants. The silicon donor electrons can diffuse into the GaAs, but will not be able to return, due to the bandgap difference between AlGaAs and GaAs; the conduction band in GaAs is lower in energy than that of AlGaAs. The electrons will be attracted by the, now positively-charged silicon ions and will hence form a 2DEG at the GaAs/AlGaAs interface. Applying negative voltages on the metallic top gates allows to shape the 2DEG into potential wells [62]. Contrarily, the silicon samples are undoped[1]. The 2DEG is created by means of electron accumulation through extra, positively biased, top gates that attract electrons from the metallic ohmic contacts. By applying positive voltages on the (accumulation) gates, a 2DEG is created and the potential landscape can subsequently be shaped by altering the voltages on the plunger and barrier gates [64]. Both the depletion mode and the accumulation mode have (dis)advantages. Dopants can facilitate tuning, but can also cause disorder in the heterostructure, distorting the potential landscape. The accumulation gates make dopants obsolete and hence provide a cleaner stack, yet including them requires a more complicated gate-architecture.

Another considerable difference between GaAs and silicon substrates, is the difference in effective electron mass in the substrates, $0.067m_e$ for GaAs versus $0.19m_e$ for silicon [63]. The almost three times higher effective mass of the electrons in silicon, makes the wavefunction more confined. Hence, in order to meticulously control and couple neighbouring electrons, while preventing extra electrons to be attracted and spurious quantum dots to be formed inadvertently, silicon samples require a smaller gate pitch than GaAs samples [63]. Such smaller gate pitch, in combination with the extra gates required to accumulate the 2DEG, poses a challenge on device fabrication. Silicon samples often contain an overlapping-gate

[1] Initially, Si/SiGe samples contained dopants, yet these samples were very unstable and ongoing work focuses on silicon samples in accumulation mode

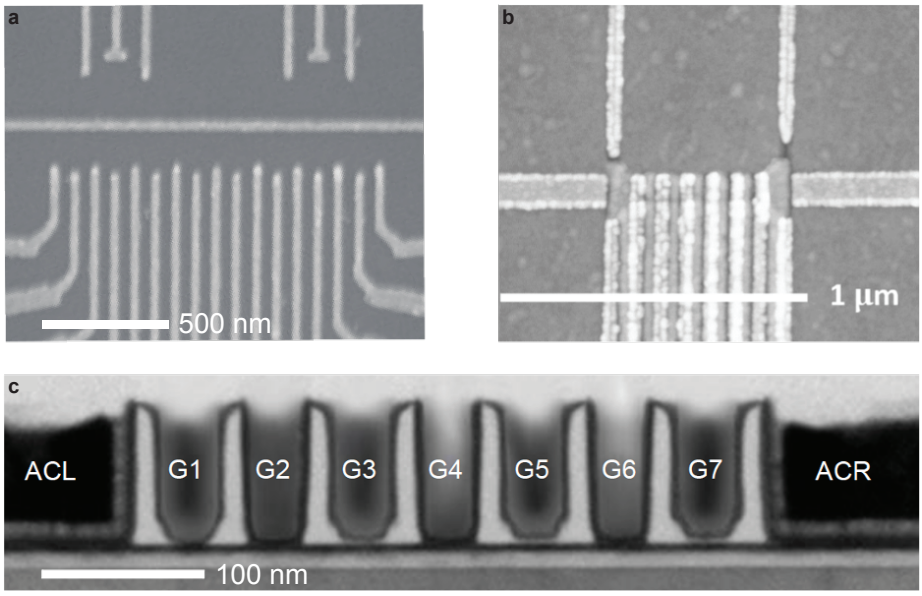


Figure 4.1.: **Quantum dot devices in different materials. a.** Scanning electron microscope image of a GaAs device that can host a linear array of eight quantum dots (bottom) and two sensing dots (top). **b.** Scanning electron microscope image of a SiGe device that can host a linear array of five quantum dots and a sensing dot on either side of the array. The overlapping gate structure of the barrier (white) and plunger gates (grey) is visible. **c.** Tunnelling electron microscope image of a SiMOS device.



design [103, 119], in which several types of gates are fabricated in different layers, separated by a dielectric oxide.

## 4.2 EXPERIMENTAL SETUP

As qubits are fragile, forming, maintaining and controlling them requires care. We do not want the qubits to be disturbed by environmental fluctuations. Moreover, we need to engineer the equipment precisely to ensure we deliver signals to the qubit that are fast enough to form and manipulate the qubits, while, simultaneouly not disrupt the qubit by noise. In this section we subsequently describe the cryogenic setup and the dc and high-frequency electronics setup that we use to form quantum dots and control qubits.

### 4.2.1 Cryogenic setup

Quantum bits are extremely sensitive to environmental disturbance. Defining a good qubit hinges on a clean two-level system, without the qubit to be able to switch between the two levels at will. For Loss-DiVincenzo qubits, the two-level system is defined by the Zeeman energy. A prerequisite for coherent qubit operation is that the Zeeman energy exceeds the thermal energy. Moreover, the thermal energy needs to maintain below other relevant energy

scales, such as the valley splitting and the orbital energy, to prevent thermal energy from inducing random excitations.

$$E_T = k_B T < g\mu_B B = E_Z \tag{4.1}$$

As an example, for a silicon sample ($g \approx 2$) in a magnetic field of $B = 0.5$ T, $T < 0.67$ K. To reach such temperatures, samples are cooled down in a dilution refrigerator. A dilution refrigerator can cool its interior to a sub 10-mK temperature. This cooling is achieved by the use of two separate mechanisms; the first mechanism cools down the refrigerator to approximately 4 K, the second mechanism decreases the refrigerator temperature to base temperature. Cooling the refrigerator down to 4 K used to be accomplished by means of a liquid helium bath[2]. This requires a continuous supply of liquid helium (and nitrogen). More recently, closed-cycle refrigerators, or 'dry refrigerator' have been developed, that use a two-stage pulse tube for the first cooling phase [209–211]. Pulse-tube cooling utilizes the expansion of a working fluid, usually Helium, for cooling. The expanded, cold working fluid passes a heat exchanger to cool down the refrigerator [212]. For a two-stage pulse tube, the cold end of the first cooling stage is the input for the second cooling stage. Dry refrigerators do not need to be filled periodically, but provide a closed cooling cycle and are therefore more simple, more efficient and in the long run less costly than wet-refrigerators [213].

The second cooling mechanism, to cool to sub-Kelvin temperatures, is based on the dilution of $^3$He and $^4$He isotopes [214]. The mixing chamber of the refrigerator contains a mixture of $^3$He and $^4$He. When such a mixture of $^3$He and $^4$He is cooled down below a critical point, the isotopes separate in two phases; a $^3$He-rich phase, or concentrated phase and the dilute phase, which is rich in $^4$He, but still contains about 6.4% of $^3$He. By means of a distiller (or still), the $^3$He is distilled from the $^4$He, based on their vapour pressure. By pumping $^3$He out of the still, an osmotic pressure gradient is created between the mixing chamber and the still which [ulls $^3$He from the dilute phase into the still. This distorts the equilibrium in the dilute phase and to retrieve equilibrium in the mixing chamber, $^3$He will cross the barrier from the concentrated phase into the diluted phase, undergoing a phase transition. As this is an endothermic process, this process requires heat, which is extracted from the walls of the mixing chamber. The $^3$He that is pumped from the still is circulated through the system and ends up in the mixing chamber again, ensuring a closed cooling cycle [212, 213].

For the work in this thesis, we used three different dilution refrigerators: two dry refrigerator (Oxford Triton, Bluefors XLD) and a wet refrigerator (Oxford Kelvinox 300).

*Triton 400*

The Triton 400 refrigerator has a cooling power of $\approx 1$ mW at the PT2 plate and $\approx 400$ $\mu$W at the mixing chamber plate at 100 mK. The refrigerator encloses a superconducting vector magnet at the PT2-plate that can apply a magnetic field of (x, y, z) (1, 1, 6) T. The refrigerator contains 48 dc lines going from room temperature to the mixing chamber plate, which are filtered with pi filters and RC filters at base temperature. These dc lines end in a 51-pin

[2] Because the dilution unit of the refrigerator resides in liquid helium, this type of refrigerator is called a wet refrigerator.

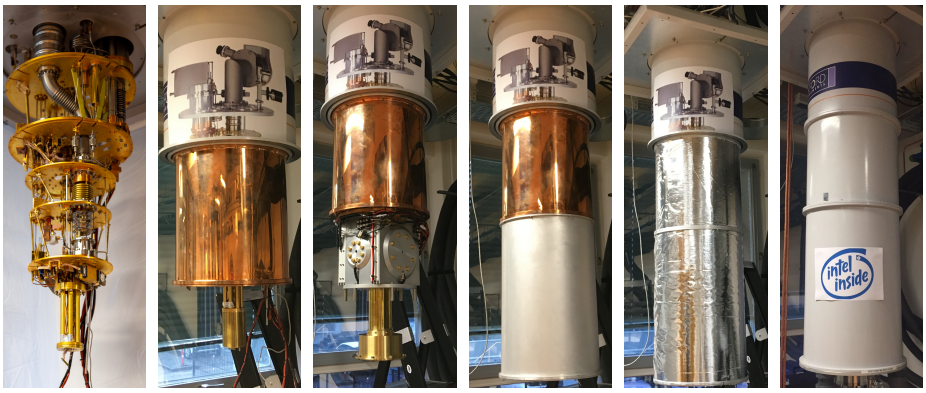


Figure 4.2.: **Oxford Triton dilution refrigerator.** The various cooling shields and plates of the Oxford Triton dilution refrigerator, characterizing the various cooling stages.



nanoD connector. Another 24 lines go into the refrigeratorto the PT2 plate, one of which powers a Weinreb CITLF3 amplifier at 4 K. Moreover, the refrigerator holds fourteen high-frequency lines: eight lines contain attenuators with a total attenuation of 23 dB, two lines are attenuated with 0 dB, one line has an added attenuation of 55 dB, one line provides readout of an on-chip resonator and two lines facilitate the RF reflectometry setup. The latter two lines recombine in a mini-circuits, ZEDC-15-2B directional coupler at the still plate. To facilitate sample exchange, the refrigerator is equipped with a bottom loader. This bottom loader is connected to the refrigerator with a load lock. Via this load lock, a sample-containing puck can be loaded into the refrigerator, while the refrigerator remains cold. The entire sample exchange takes approximately 14 hours. In comparison; an entire thermal cycle for the refrigerator takes at least 78 hours.

*Bluefors XLD*

The Bluefors XLD refrigerator has a cooling power of 570 $\mu$W at the mixing chamber plate at 100 mK and a cooling power of 16 $\mu$W at 20 mK and is equipped with a 3-T superconducting axial magnet. The refrigerator contains 96 dc lines that go from room temperature to the mixing chamber plate and are filtered with RC filters and copper powder filters at base temperature. The dc lines end in two separate 50-pin flex cables and thus allow either one 100-line PCB, or two 50-line PCBs to be connected. Another 24 dc lines are installed and go from room temperature up to the PT2 plate of the refrigerator to power two Weinreb CITLF3 amplifiers at the 4-K plate to facilitate RF readout. The refrigerator contains sixteen SCuNi-CuNi graphite-coated coaxial lines that are either attenuated with 23 dB (eight lines), or with 28 dB (eight lines)[3]. Moreover, the refrigerator has four extra high-frequency lines to accommodate two RF-readout setups. Per RF-readout setup, the incoming and outgoing high-frequency lines are combined in a mini-circuits, ZEDC-15-2B directional coupler at the mixing chamber plate.

[3] After the experiment in chapter 4 of this thesis, the Bluefors XLD was upgraded with another sixteen coaxial lines

*Oxford Kelvinox 300*

The Oxford Kelvinox 300 allows for a base temperature of $\approx$ 20 mK. The refrigerator is equipped with a bi-axial, superconducting magnet with a maximum magnetic field of $(x, z) = (3, 7)$ T. The refrigerator contains 40 manganese dc wires going from the room-temperature equipment to the mixing chamber. In the mixing chamber, these wires can individually be connected to a rerouting PCB in order for them to apply voltages to the appropriate gates. The dc wires are filtered with pi-filters at room temperature. Moreover, they go through copper powder filters and RC filters at base temperature to reduce thermal noise. Additionally, the refrigerator contains six copper wires to accommodate a LED. The refrigerator contains four coax cables. From RT to the 1K plate ULT-05 Keycom wires attenuated with 20 dB. From the 1K-plate to the mixing chamber, the wires are NbTi EF085B KEYCOM, two of which are attenuated with an extra 10 dB and two with 6 dB. The coax cables are connected to the sample via EF085D KEYCOM flex cables. The refrigerator is cooled down to $\sim$ 4 K by filling the OVC with a liquid helium bath about twice per week. The IVC contains the dilution unit, a home-made cold finger and the sample. In the IVC, the device is shielded with a home-made copper can to absorb 4 K radiation from the IVC. This can is attached to the mixing chamber and not in thermal contact with the IVC.



### 4.2.2 Preventing noise by attenuation

Although the dilution refrigerator cools down its interior to sub 10 mK, this does not necessarily cause the electrons in the 2DEG to be cooled down to those temperatures. Electrical control with dc and ac pulses, generated at room temperature can considerably warm up the 2DEG. Filtering of the lines is required to get the 2DEG temperatures as low as possible. To reduce thermal noise from high-frequency electronics to Johnson noise before it reaches the sample, attenuators are mounted at various stages in the refrigerator. Attenuation is chosen such that the noise is reduced sufficiently, while the signal-to-noise ratio of the measurement is optimized and the equipment output range is not reduced too much. We can choose the noise attenuation as follows. The noise, or photon flux, can be described by the Bose-Einstein distribution [215]:

$$n_{BE} = \frac{D(E)}{\exp(hf/k_B T) - 1}, \tag{4.2}$$

with $D(E)$ the density of states in the 1D transmission lines, $f$ the frequency, $T$ the noise temperature, $h$ Planck's constant and $k_B$ the Boltzmann constant. The room-temperature equipment will send noise to the sample at a distribution of $T_{HOT}$. To reduce this noise before it reaches the sample, the required attenuation is given by the noise ratio at the temperature stages that are traversed in decibel:

$$10 \log_{10} \left( \frac{\exp(hf/k_B T_{hot}) - 1}{\exp(hf/k_B T_{cold}) - 1} \right), \tag{4.3}$$

where, by taking the ratio, $D(E)$ cancels out. Thus, we need approximately 10 dB attenuation when the temperature changes with one order of magnitude[4]. Equipment at each temperature stage will induce noise at its own temperature distribution, thus, attenuating the signal even further merely attenuates the signal, while the noise is maintained, which limits the SNR. As such, we need a maximum of 20 dB attenuation in the refrigerator up to the 4-K stage. When attenuating further to milli-kelvin temperatures, the attenuation required to cool down the photon flux further increases rapidly with frequency, meaning the photon flux temperature will rapidly increase with frequency and the photon flux is not in equilibrium with the electron bath. Therefore, the signal is attenuated by an additional 4 dB between the cold plate and the mixing chamber, in the guise of finding a sweet spot where most of the Johnson noise is curtailed, while allowing for a large signal at the sample. Moreover, as the cooling power at the mixing chamber is in the order of a few hundred $\mu$W, we aim to minimize attenuation at the mixing chamber to avoid excessive heating of the mixing chamber.



### 4.2.3 Printed Circuit Boards

The sample is connected to the refrigerator electronics via a printed circuit board (PCB). The PCB is thermally anchored to a metallic cold finger, attached to the mixing chamber of the refrigerator. The sample is glued onto the PCB and connected to the electronic lines via wire bonds. Several PCBs are used for the research in this thesis.

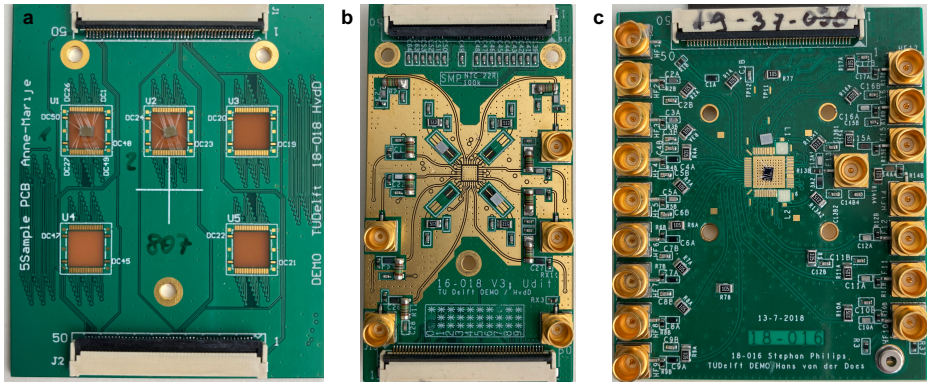


Figure 4.3.: **PCBs. a.** The multiplexed PCB that can host and measure up to five samples simultaneously. **b.** Measurement PCB 1. The sample is glued in the central square and there is room for up to four inductors to facilitate RF readout. DC cables can be connected by means of the flex cable connectors at the top and bottom of the PCB and the PCB has ten SMP connectors to accommodate high-frequency lines. **c.** Measurement PCB 2. The sample is hosted in the center of the PCB and two inductors can be glued on the side of the sample. The PCB has flex-cable connectors on the front and the back to accommodate the connection to DC lines and has 17 SMP connectors to connect high-frequency lines.

[4] This approximation is valid at least down to 4 K and up to 20 GHz

*Multiplexed PCB*

Figure 4.3a depicts the multiplexed PCB[5]. The PCB is designed solely for high-throughput test purposes and allows for the signals from five samples to be multiplexed, hence to be measured and readout simultaneously. The PCB contains 50 dc lines. Each sample has access to two unique lines, meant to connect ohmic contacts[6]. The other 40 lines are five-fold multiplexed and can be used to apply bias on the gates. In theory, five identical samples can be bonded to separate ohmic contacts, while similar gates are connected to the same, multiplexed line. After cool down, the five samples can be measured simultaneously. The PCB was designed as a first-generation multiplexed-PCB, with the risk in mind that if one of the samples has a leaking, multiplexed gate, this leak will prevent voltage from being applied over the same multiplexed gate on the other samples. Due to the abundance of dc-lines, the PCB can also accommodate several smaller samples, all bonded to unique dc-lines, to be cooled-down simultaneously. A more elaborate multiplexed design was already proposed while designing this PCB and is now being developed. As the multiplexed PCB was designed for test purposes only, the PCB does not contain any fast lines.



*Measurement PCB 1*

This PCB[7] is used throughout the majority of this thesis, see Fig. 4.3b. The PCB contains 48 dc lines, 33 of which are filtered to ground with a capacitor of 100 pF and can be connected to the sample, the other 15 lines are directly connected to ground and thus are idling. The PCB contains nine high-frequency (HF) lines, that each are connected to a separate dc-line via a home-made bias-tee, with an RC-time of 470 ms ($R = 10$ M$\Omega$, $C = 47$ nF). This combination allows for the definition of quantum dots (DC voltages) and fast pulses (HF lines). Moreover, the sample accommodates RF-readout via a four-fold frequency-multiplexed high-frequency line. On the PCB, the signal is sent into four LC tank circuits that can can be connected to separate ohmic contacts. This enables high-bandwidth readout of the sensing dot.

*Measurement PCB 2*

The third PCB[8] used in this thesis is shown in Fig. 4.3c. The PCB contains 48 dc lines, filtered to ground via a 100 pF capacitor. 43 of the dc lines can be connected to control electronics. Four dc-lines are connected to ground directly, the last dc-line is connected to a laser light-emitting diode (LED) on the PCB. The LED can be used for a quick sample-reset; shining light using the LED enables charges in the substrate to be freed from traps and as such it resets the charge configuration of the quantum well. The LED on the PCB has a wavelength of 780 nm, with a maximum output capacity of 5 mW at a current of 70 mA.

[5] This PCB has been designed in collaboration with Hans van der Does.

[6] To optimize the number of lines on the PCB, remaining ohmic contacts can be connected to ground. These ohmics can act as the drain of the current path and, as such, a bias window is opened between the biased ohmic and the grounded ohmic

[7] This PCB is designed by Juan Pablo Dehollain, Uditendu Mukhopadhyay and Hans van der Does

[8] This PCB is designed by Stephan Philips and Hans van der Does

As the LED power dissipation causes rapid refrigerator heating, we reset the sample by applying 5 mA-current at 5 V, hence limit the power to 25 mW and we apply this power for a maximum of $\sim$ 10 s. The PCB contains 16 fast lines, that are connected to the control electronics via SMP connectors and are combined with a dc line via a home-made bias-tee with a time constant of of 100 ms ($R = 1$ M$\Omega$, $C = 100$ nF) on the PCB to enable the quantum dot formation in combination with fast control. The RC time constant of this PCB is shorter than the time constant of measurement PCB 1 (470 ms). The RC time constants are a consideration between the ability to apply long pulses and the tuning speed of the sample in DC. RF readout is accommodated via a twofold frequency-multiplexed high frequency line, connected to two LC tank circuits. The tank circuits can be connected to ohmic contacts and such facilitate high-bandwidth measurements.



### 4.2.4 Setup

Control over the metallic gate voltages, as well as fast pulses and microwaves for qubit control and readout are enabled by a room-temperature, electronic setup. The setup contains both dc and ac components. As the quantum dots and qubits are rather susceptible to noise, the dc part and the ac part of the electronic setup are separated. Here, the electronical setup that feeds the Oxford Triton refrigerator is described. The setups for the other refrigerators are comparable.

*dc setup*

The potential landscape in the quantum well is shaped by applying dc voltages to metallic gates. These metallic gates control both the chemical potential of the quantum dots (plunger gates) and the tunnel barriers between quantum dots and between a quantum dot and the reservoir (barrier gates). Moreover, the dc setup can be used to apply a bias over the ohmic contacts of a sample and hence allow for transport measurements.

The specific voltages that we want to apply are set on the computer. The computer sends the signal via an optical cable to digital-to-analog converters (DACs) in an inhouse-built SPI-rack [216]. These DACs allow for a voltage range of 8 V [9] with a sixteen-bit resolution. Via a matrix module, the DACs are connected to a respective gate and the signals are sent into the refrigerator via two shielded 24-pin fisher cables. In the refrigerator, the dc lines are thermally anchored at each temperature stage of the refrigerator. To filter out high-frequency thermal noise and hence reduce the electron temperature, the dc lines are filtered with $\pi$-filters and RC-filters at the mixing chamber plate[10]. The pi-filters reduce the noise up to 5 GHz. Then, the lines either pass a second-order RC-filter with a cut-off frequency of $\approx$ 33 Hz to bias the gates, or a first-order RC-filter with a higher cut-off frequency that allows for slow ($\approx$ 200 kHz) and fast ($\approx$ 1.3 MHz) measurements through the ohmic contacts. The latter lines have an increased measurement bandwidth to facilitate single-shot readout[11]. The dc lines

[9] This range can be set positive (0-8 V), negative, ($-$8-0 V), or bipolar ($-$4-4 V), powered by an isolated power supply. For most of the measurements in this thesis, the range was set to bipolar.

[10] The XLD Bluefors and the Oxford Kelvinox 300 are equipped with copper powder filters instead of pi-filters

[11] These high cut-off frequencies are obsolete when RF readout is installed

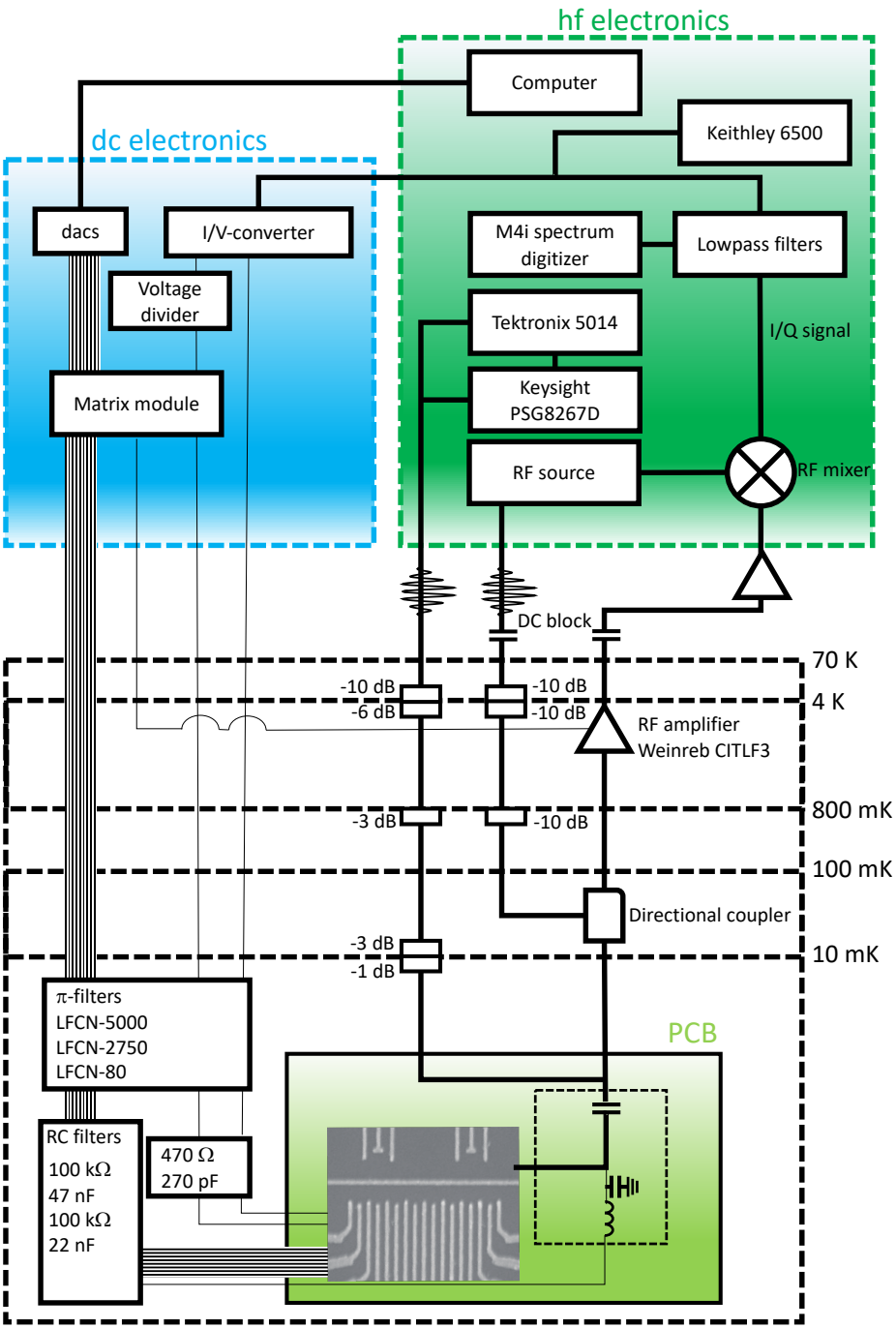


Figure 4.4.: **Schematic overview of the electrical measurement setup.** Schematic of the setup as described in the text.

are connected to the PCB by means of a 50-pin flex cable. Some of the dc lines on the PCB are routed to a bias-T, in order to enable the combination of dc-control and fast control for a specific gate.

To enable transport measurements, charge detection and single-shot spin readout, a bias window is opened between the ohmics by applying a bias on one ohmic. As this bias should be about three orders of magnitude smaller than the voltages that control the gates, a voltages divider in the SPI-rack allows for high-resolution control with a division factor up to $10^4$. The current is read out out via a current-to-voltage (I-V) converter, with a cut-off frequency of 50 kHz and resistance of 183 Ω. The dc readout signal is amplified and sent to a keithley6500 multimeter. For single-shot readout, the signal from the I-V converter is filtered by a low-pass filter with a cut-off frequency of 3 kHz and sent to a M4i spectrum digitizer, with 16 bit resolution and a maximum sampling rate of 250 MS/s.



*HF setup*

The high-frequency setup is used for a threefold purpose. Firstly, to apply fast pulses to the gates. Such pulses allow for nanosecond-control over the quantum dot's chemical potentials and tunnel couplings, i.e. change the electron occupation of a quantum dot, or the exchange coupling between quantum dots. These pulses are used both for qubit experiments and, via millisecond-timescale ramps, for the rapid scanning of charge stability diagrams. Additionally, the setup is used to apply radiofrequency signals with the purpose of qubit manipulation. Depending on the sample, these radiofrequency signals can drive the qubit either electrically (EDSR), or magnetically (ESR). The third purpose of the setup is to enable high-bandwidth measurement via a radio-frequency reflectometry setup.

The fast pulses are generated by a Tektronix 5014 arbitrary waveform generator (AWG)[12]. To filter out high-frequency noise, the signals are filtered at room temperature via ferrite coils and subsequently sent into the refrigerator via stainless steel (RT-4 K) and superconducting (4 K-10 mK) semi-rigid coax cables. The outer conductor of the coax cables is thermally anchored to each plate in the refrigerator. Attenuators that add up to an attenuation of 19 dB are mounted at various stages up to the still plate to reduce the room-temperature thermal noise to Johnson noise before it reaches the sample. Thereafter, the signal is attenuated by an additional 4 dB between the cold plate and the mixing chamber, seeking for a sweet spot where most of the Johnson noise is curtailed, while allowing for a large signal at the sample. At the mixing chamber, the coax cables are connected to the PCB via flexible coax cables with SMP-connectors, where the high-frequency signal is combined with the dc-signal via a home-made bias-tee. The Oxford Triton refrigerator contains 8 coax cables with a total of 23 dB attenuation, two coax cables with 0 dB and one coax cable with 55 dB attenuation[13].

Qubit manipulation is performed by means of radio-frequency signals ( 1-20 GHz), generated by a Keysight PSG8267D vector source. Coax lines connected to the microwave source are filtered with a dc block.

[12] For all three setups we used one (Oxford Triton, Oxford Kelvinox 300) or two coupled (XLD) Tektronix 5014 AWGs

[13] The XLD refrigerator contains sixteen coax cables with a total of either 23 dB (eight lines) or 28 dB (eight lines) attenuation, the Oxford Kelvinox 300 contains 4 lines with either 30 dB, or 26 dB attenuation

Since the attenuator reduces transmitted power by converting photons to heat, you also need enough cooling power on a specific plate to eliminate of that heat again.

To increase the readout bandwidth, a tank circuit can be coupled to one the ohmic contacts to perform radio reflectometry readout, see next section. The readout signal is filtered and then sent to an M4i digitizer card, triggered by the AWG.

## 4.3 METHODS AND METRICS

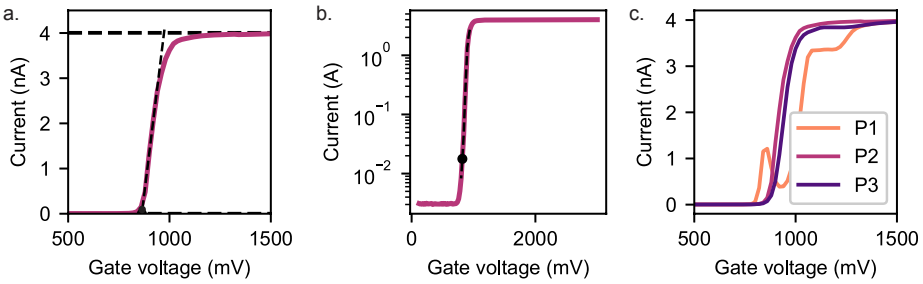


Figure 4.5.: **Sample characterization.a.** Threshold voltage analysis for a pinch-off curve for gate $P2$ of **c**. The gate has a threshold voltage of $V_t = 840$ mV. **b.** Subthreshold slope analysis for gate $P2$. **c.** Pinch-off curves for the three plunger gates of a specific device. The spread in threshold voltages and the shape of the curves can be analysed to define the sample uniformity. The threshold voltages of gate $P1$, $P2$ and $P3$ are respectively811, 840 and 748 mV, or 300, 311 and 276 $\mu$eV. The spread in turn on is 24 $\mu$eV, which is about 2.7 times the charging energy for this sample of 8.9 $\mu$eV.

Both the sample yield and initial indications of sample uniformity can be studied during the characterization of the sample. The yield analysis mainly involves the analysis of the functionality of all the metal gates and ohmic contacts. Typically, when all metal gates and ohmic contacts work, the device is suitable for measurements as described in this thesis. Yet, inhomogeneity in a device hampers the prospects for scaling. Inhomogeneous device behaviour, for example caused by a non-uniform gate stack, or by background impurities and charges in the gate oxide, in the dopant layer (GaAs), or trapped at the dielectric interface [63], prevent uniform quantum dot and qubit behaviour. For devices in this thesis, the effect of these impurities can be overcome by carefully sculpting the potential landscape by means of device tuning. However, for devices with increasing numbers of quantum dots, this will be impractical at the least. Moreover, several scaling architectures assume shared gates for various quantum dots and hence demands sample uniformity [55].

Additional to metrics to determine material quality, such as mobility and percolation density [122], it is useful to define metrics that provide insight in both sample yield and homogeneity of the quantum dots. These metrics are platform-independent and can be used to compare different devices. Initial metrics that indicate device performance are key metrics borrowed from the transistor industry [217]. Firstly, the spread of the threshold voltages of all similar gates within a device gives a measure of the sample uniformity.The threshold voltage indicates the transition between a channel controlled by the voltage on a metallic

gate being 'on', of 'off'. It is defined as $V_t = V_r - V_{SD}/2$, where $V_r$ is the intersection between the tangent line to the steepest point of the pinch-off curve and 0 A and $V_{SD}$ is the bias difference between the source and drain contact, see Fig. 4.5a. Typically, we aim for the threshold voltages to fall within the range of the smallest charging energy of all quantum dots in the device. This would be an indication that quantum dots can be homogeneously filled and controlled when using the same control line for multiple gates. Figure 4.5c shows the pinch-off curve for three plunger gates of a device. For this device, the difference in threshold voltage equals 2.7 times the charging energy. There is a second characteristic that can be studied from the pinch-off curves. The shape of the pinch-off for $P_1$ in Fig. 4.5c deviates from the shapes of the other two curves. The extra bump indicates the presence of impurities or trapped charges underneath the gate. Secondly, the subthreshold slope can be considered. The subthreshold slope is a measure of how quickly a gate turns on. It is defined as the minimum of $(\frac{d}{dV}\log_{10}(I))^{-1}$, with $I$ the current and $V$ the gate voltage. A high subthreshold slope means a slow turn on, which indicate sample disorder, see Fig. 4.5b. Thirdly, a crucial metric for Si/SiGe devices is the working window. As silicon devices are typically operated in accumulation mode, the application of a voltage is required to accumulate the 2DEG. Yet, when the applied voltage crosses a certain threshold, the energy of the silicon cap falls below the Fermi energy and electrons start to collect in the cap. These electrons have a screening effect on the quantum well, with as a result hysteresis and eventually a complete drift of the turn on voltage, see Fig 4.6. This process is merely reversible by a complete reinitialization of the device, either by means of a thermal cycle, or by shining light using an LED. The working window is defined as the difference between $V_t - V_d$, where $V_t$ is the turn on voltage of the channel, while $V_d$ is the voltage where the hysteresis begins.

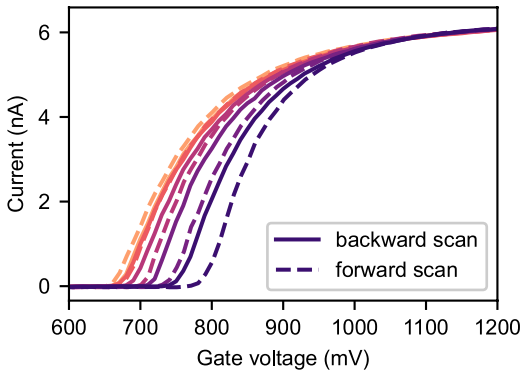


Figure 4.6.: **Hysteresis in a Si/SiGe sample.** Determining the working window for a Si/SiGe sample by doing forward and backward scans to an increasing gate voltage.

Additional metrics to consider for disorder assessment are the channel resistance of the sample, the uniformity of the lever arms and charging energies of the quantum dots [103] and the amount of charge noise in the sample. It would be interesting to take the analysis a step further and compare quantum-dot metrics with metrics for qubit analysis, such as the qubit coherence time and drive frequency.

# 5 LOADING A QUANTUM-DOT BASED "QUBYTE" REGISTER

*Electrostatically defined quantum dot arrays offer a compelling platform for quantum computation and simulation. However, tuning up such arrays with existing techniques becomes impractical when going beyond a handful of quantum dots. Here, we present a method for systematically adding quantum dots to an array one dot at a time, in such a way that the number of electrons on previously formed dots is unaffected. The method allows individual control of the number of electrons on each of the dots, as well as of the interdot tunnel rates. We use this technique to tune up a linear array of eight GaAs quantum dots such that they are occupied by one electron each. This new method overcomes a critical bottleneck in scaling up quantum-dot based qubit registers.*

This chapter has been adapted from C. Volk*, A.M.J. Zwerver*, U. Mukhopadhyay, P.T. Eendebak, C.J. van Diepen, J.P. Dehollain, T. Hensgens, T. Fujita, C. Reichl, W. Wegscheider and L.M.K. Vandersypen,
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## 5.1 INTRODUCTION

Quantum-dot based spin qubit platforms [36, 48, 54] are maturing: important recent landmarks include the realization of 99.9%-fidelity single-qubit gates [50], the implementation of two-qubit gates [79, 80, 95, 125, 198, 199] and two-qubit algorithms [104]. Moreover, due to the small system size and the compatibility with semiconductor manufacturing techniques, these systems have a high potential for scaling. Hoewever, although a high degree of control of the charge and spin degrees of freedom has been shown, research has been mainly limited to single, double and triple dot systems. Recently, control of the charge occupation of four dot systems has been demonstrated [83–85, 89] and a single electron could be controllably placed in a 3x3 array [218]. However, device specific approaches to tuning quantum dots will need to be replaced by a systematic approach, as arrays become larger with the scale-up of quantum-dot based quantum circuits.

The controlled formation and filling of large quantum dot (QD) arrays poses multiple challenges. Individual gate voltages affect not only the parameter they are designed to control, typically the electrochemical potential of a specific QD or the tunnel barrier between two adjacent QDs, but through capacitive cross-talk also affect other electrochemical potentials and tunnel barriers [62]. Furthermore, tuning devices is complicated by a disordered potential landscape arising from charges trapped in randomly located impurities and defects in the substrate and at the surface [219, 220]. Finally, electrons are loaded into QDs from an electron reservoir. When a target dot is separated from the reservoir by one or more other dots, electrons are typically loaded by co-tunnelling, only virtually occupying the intermediate dots. However, for more than three or four dots, the co-tunnel rates become impractically low.

These challenges present themselves when measuring the charge occupation in quantum dot arrays through conventional charge stability diagrams. In such diagrams, the signal from a charge sensor is recorded while sweeping two gate voltages, resulting in a 2D plot that exhibits regions in gate voltage space with a fixed number of electrons on each dot, separated by lines indicating charge additions to the array, or charge transitions between dots [62]. Such a 2D plot corresponds to a plane in a multi-dimensional space spanned by all the gate voltages. As arrays get larger, when sweeping just two gate voltages, cross-talk leads to slopes of charge transition lines that are almost parallel and hard to distinguish. Assignment of charge transition lines to specific dots is further complicated by non-uniform addition energies. Furthermore, the intersections between different charge addition lines can cluster together in a small gate voltage region. Finally, the difficulty of loading electrons to dots far from the reservoir leads to postponed loading of dots (latching) or to missing charge addition lines [221]. Those complications lead to plots that are difficult to interpret [222].

Cross-talk and the background disorder potential have been compensated for in short dot arrays using so called virtual gates, which are linear combinations of multiple gate voltages chosen such that only a single electrochemical potential or tunnel barrier is addressed [91]. Virtual gates also make it possible to strategically choose the measured 2D plane in gate-space, so that multi-dot charge stability diagrams become easy to interpret [91, 173, 218]. The difficulty of loading electrons into large arrays has been circumvented using additional

reservoirs in between groups of three dots [223]. In another approach, an additional access point to a reservoir was created halfway a linear array of five QDs [222]. Instead of loading electrons by co-tunnelling, electrons can also be made to sequentially tunnel through a chain of dots to reach their target location [81], but this approach requires the chain of dots to be already formed in the first place.

We explored several approaches to form long linear arrays in a controlled way, such as forming individual single dots first and stitching them together, stitching together double dots, or starting with a large QD and then splitting it up into an array of separate dots. However, we found it difficult to make these approaches work well.

Here, we show the controlled filling of an array of eight QDs, which we call a Qubyte register, using a method that is both conceptually simple and effective. Starting from a double dot, we introduce the "$n+1$ method", adding dots one by one using virtual gates. Every new dot added adjacent to the existing array is right next to a reservoir so the dot can be filled easily. The use of virtual gates saves the charge occupation in the previously formed dots while adding a new dot, and also keeps the charge stability diagrams simple to interpret. We show that we can locally control the number of electrons on each dot down to the last electron, and that we can set all interdot tunnel couplings to typical values used in spin qubit experiments. Finally, we discuss the limitations and potential pitfalls of the $n+1$ method.



## 5.2 DEVICE AND INITIAL CHARACTERIZATION

Fig. 5.1a shows a scanning electron micrograph of a device nominally identical to the one used in the experiment. The gate layout has been adapted from previous triple and quadruple quantum dot devices [85, 173]. On one side, 17 gates with a pitch of 80 nm are fabricated to control the tunnel barriers and electrochemical potentials of the QDs. The upper part of the sample accommodates two sensing dots (SD) that are capacitively coupled to the linear QD array. The circles indicate the intended positions of the QDs. All measurements are carried out in a dilution refrigerator with a base temperature below 20 mK.

Initially, the device is characterized by DC transport measurements. The pinch-off characteristics of the channel between each of the plunger $P_i$ or barrier $B_i$ gates and the central gate $D$ is measured (see schematics in Fig. 5.1a) and single QDs are formed by sweeping pairs of neighbouring barrier gates. These measurements confirm that all QDs, including the sensing dots, can be formed (if not, the sample is considered unsuitable to host eight QDs). Moreover, the pinch-off values determined for each gate act as starting parameters for further tuning. In all subsequent measurements, we probe the linear QD array via the two sensing dots, which are sensitive to the number of electrons in the array, as well as to their position in the array. The charge sensors are probed using RF reflectometry (see Experimental methods section).

To illustrate the difficulty of traditional tuning strategies, Fig. 5.1b shows a charge stability diagram for a linear six-dot array (sextuple dot) confined between the barrier gates $B_1$ to $B_7$. The charge stability diagram has been recorded sweeping the voltages of gates $P_2$ and $P_7$, i.e. the gates mostly coupled to the outer QDs. In the diagram charge addition lines with

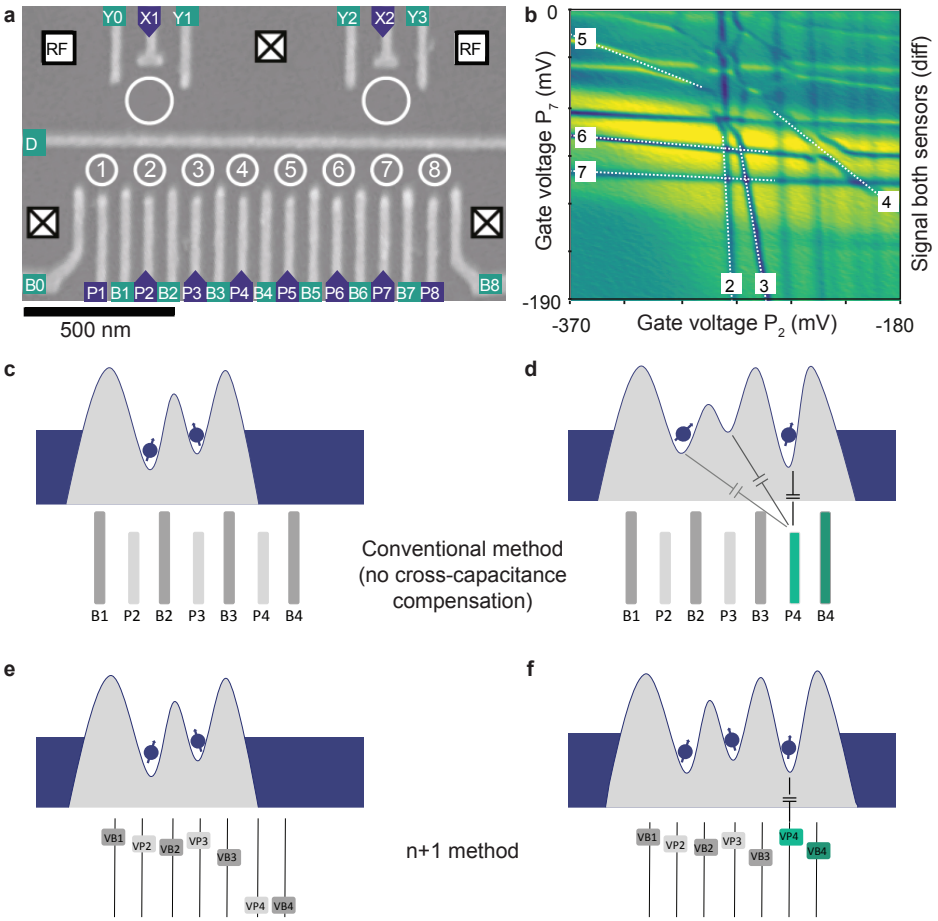


Figure 5.1.: **Device design and tuning principle. a.** Scanning electron micrograph of a device nominally identical to the one used in the experiment. The scale bar measures 500 nm. The circles indicate the intended positions of eight quantum dots (QDs) that define a Qubyte register and of two additional dots that are used for charge sensing. For the linear array, the designed dot-to-dot pitch is 160 nm. The plunger gates connected to high frequency lines are marked with blue triangles. The squares indicate the position of the Fermi reservoirs. Two on-board tank circuits for RF reflectometry readout are connected to each of the sensing dots. **b.** Charge stability diagram of a sextuple dot formed between barrier gates $B_1$ and $B_7$. The sum of the differential demodulated voltages of both sensing dots is plotted. The dashed lines highlight charge transitions of each of the six QDs (the numbers refer to the labels in panel **a**). **c., d.** Illustration of the potential landscape of a double QD. Gates $P_4$ and $B_4$ are used to form a third QD. Capacitive cross-talk, indicated by the capacitor symbols, has not been compensated for. Thus, these gates influence the potential of the other QDs as well (to avoid clutter, we did not draw any other capacitor symbols). **e., f.** A double QD is extended to a triple QD using the virtual plunger $VP_4$ and barrier $VB_4$. Due to cross-capacitance compensation these parameters only act locally on the potential landscape.

different slopes can be identified. However, charge transitions with similar slopes can be only be assigned unambiguously to specific dots, after also stepping other gate voltages (see e.g. the small difference in slope between the transitions for dots 6 and 7). Even then, the complex pattern of transitions in the center of the diagram makes it extremely difficult to determine the charge occupation at every point in this gate space. Moreover, cross-capacitances hinder local tuning of the electrochemical potential and tunnel rates.

## 5.3 $n+1$ TUNING METHOD

To tune up a multi-dot array dot by dot, we make use of virtual gates, which compensate for the cross-talk on the electrochemical potentials that occurs when sweeping actual gate voltages (see Fig. 5.1c-d). The virtual gates as used here do not compensate for cross-talk effects on tunnel barriers. The virtual plunger gate $\mathrm{VP}_i$ directly corresponds to the electrochemical potential of $\mathrm{QD}_i$, up to a lever arm. The compensation is performed to first order, so that we can express the virtual gates as linear combinations of the physical gate voltages, summarized by a cross-capacitance matrix [79, 91].



The tuning procedure consists of the following steps, described in more detail below:

1. Tune up a double quantum dot (DQD) and one sensing dot with the traditional strategy.
2. Measure the cross-capacitance between all gates and the electrochemical potentials of these three QDs and record them in a cross-capacitance matrix. This matrix can now be used to generate virtual gates.
3. Use the virtual plunger and barrier gates adjacent to the existing dots to form the next QD without disturbing the former.
4. Measure the cross-capacitance between all gates and the electrochemical potential of the newly formed QD and place these values in the corresponding row of the matrix.
5. Re-measure the cross-capacitances to the previously formed QDs and update the matrix accordingly.

Steps 3 to 5 are repeated to extend the array, adding one QD at a time.

Before we describe these five steps in more detail, we first explain how the cross-capacitance matrix $A = (\alpha_{ij})$ is used to create virtual gates. For illustration purposes, we do this for the first three dots, leaving out the outer barrier gates and the gates of the sensing dots for simplicity. The following relationship expresses how much each physical gate affects each virtual gate:

$$\begin{pmatrix} \Delta\mathrm{VP}_1 \\ \Delta\mathrm{VB}_1 \\ \Delta\mathrm{VP}_2 \\ \Delta\mathrm{VB}_2 \\ \Delta\mathrm{VP}_3 \end{pmatrix} = \begin{pmatrix} 1 & \alpha_{12} & \alpha_{13} & \alpha_{14} & \alpha_{15} \\ 0 & 1 & 0 & 0 & 0 \\ \alpha_{31} & \alpha_{32} & 1 & \alpha_{34} & \alpha_{35} \\ 0 & 0 & 0 & 1 & 0 \\ \alpha_{51} & \alpha_{52} & \alpha_{53} & \alpha_{54} & 1 \end{pmatrix} \begin{pmatrix} \Delta P_1 \\ \Delta B_1 \\ \Delta P_2 \\ \Delta B_2 \\ \Delta P_3 \end{pmatrix} \tag{5.1}$$

For convenience, we set the diagonal entries to 1 (dimensionless), disregarding the lever arm. This implies we express virtual gates in units of Volt, similar to the physical gates. Furthermore, since we do not include cross-talk effects on tunnel barriers, the off-diagonal

matrix elements relating the physical gate voltages to virtual barrier gates are set to zero. The inverse matrix expresses the linear combination of physical gate voltages that is needed to sweep a virtual gate. We note that the diagonal entries of the inverse matrix do not need to be equal to 1.

We now turn to the five steps in the $n+1$ method. In step 1, we form $QD_2$, $QD_3$ and the left sensing dot using conventional methods. The resulting charge stability diagram is shown in Fig. 5.2a. The matrix $A_1$ at this point is simply the identity matrix (this matrix and the matrices produced in subsequent steps are shown in Appendix A). For step 2, the matrix entries for $QD_2$, $QD_3$ and the left sensing dot are determined by recording how much an addition line for $QD_i$ in a $P_i$ scan is displaced when stepping any of the other plunger (barrier) gates $P_j$ ($B_j$) by an amount $\delta V$ (see Fig. 5.6). The ratio of the shift of the charge transition line of $QD_i$ in the $P_i$ scan and $\delta V$ yields the corresponding entry in the cross-capacitance matrix. We do this for all eight plunger and nine barrier gates of the linear array, as well as for the plunger gates of both sensing dots. The resulting matrix is $A_2$.



The effectiveness of the cross-talk compensation can be seen by recording a charge stability diagram in the virtual gate space, i.e. using $VP_2$ and $VP_3$ as sweep parameters (see Fig. 5.2b). Ideally, addition lines of $QD_2$ and $QD_3$ appear as orthogonal (horizontal and vertical) lines. In practice, the compensation is not always perfect because we extrapolate each cross-capacitance from just two data points (see Fig. 5.6), but it is usually good enough.

To add the next QD (step 3), here $QD_4$, we form a new tunnel barrier using the neighbouring virtual barrier gate, $VB_4$. The pinch-off values determined in DC transport indicate a suitable voltage range to scan with the barrier gate. Optionally, we then monitor the charge stability diagram $VP_2$ - $VP_3$ while stepping $VB_4$. Once the barrier is raised sufficiently to form an additional QD, new addition lines appear in the charge stability diagram (see arrows in Fig. 5.2c). The charge transitions of the previously tuned QDs are only slightly affected, indicating the effectiveness of the virtual gate concept.

We complete the tuning of the newly formed dot to the single-electron regime by measuring a charge stability diagram, here sweeping virtual plunger $VP_4$ versus virtual barrier $VB_4$. A set of diagonal lines indicates charge transitions of the newly formed QD (see Fig. 5.2d). We can identify the last charge transition in the bottom left of the figure. The cross-capacitance matrix is unchanged, $A_3 = A_2$.

Next, we update the cross-capacitance matrix (step 4). First, we fill the row corresponding to $VP_4$ in an otherwise unity matrix, which gives $A'_4$. The effect of all $VP_j$ and $VB_j$ on $VP_4$ is determined, as described for the first double dot, with the distinction that we now start from a set of virtual gates, expressed by matrix $A_2$. We then consolidate the virtual gates for dots 2-4 (and the first sensing dot) into the matrix $A_4 = A'_4 A_3$.

Finally, in step 5, the matrix entries in $A_4$ are updated to account for reduced screening of the gate potentials when the two-dimensional electron gas at the location of $QD_4$ is depleted. To do so, we remeasure the cross-talk from all the virtual plunger and barrier gates to all the virtual plunger gates. This results in the matrix $A'_5$, which represents a correction on $A_4$ and is constructed using the virtual gates expressed by $A_4$. Therefore, the updated

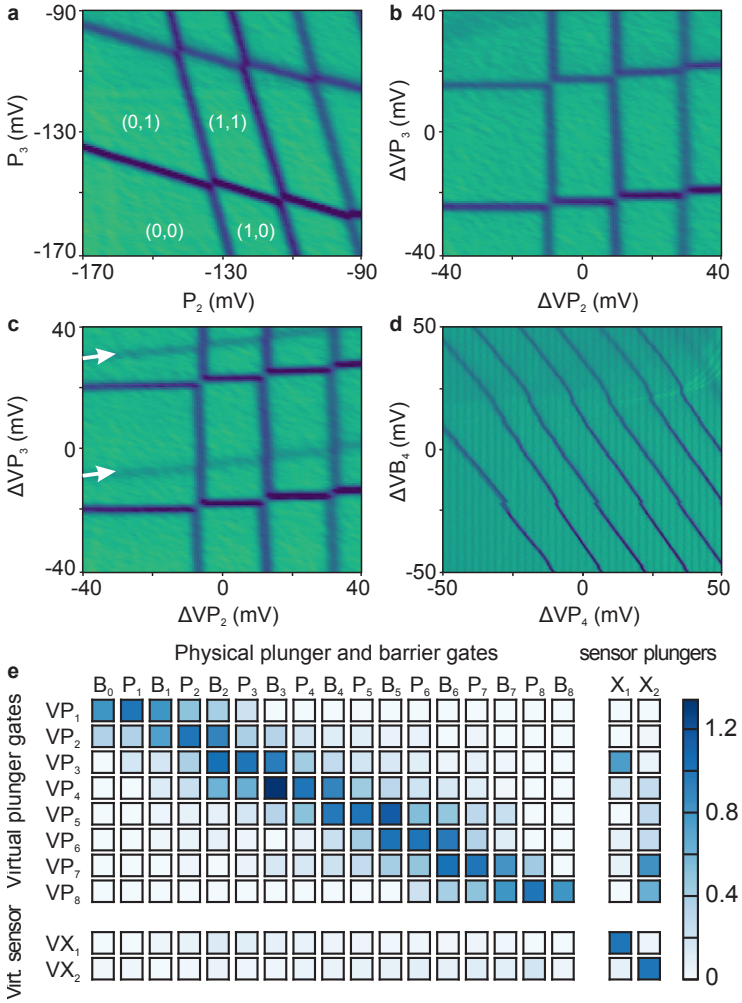


Figure 5.2.: **Tuning method. a.** Charge stability diagram of a DQD in the single-electron regime. The charge sensor response is plotted in color scale (the differential demodulated voltage, in arbitrary units, is plotted here and in similar plots below) as a function of the plunger gate voltages $P_2$ and $P_3$. **b.** Charge stability diagram of the same DQD recorded as a function of the virtual plungers $VP_2$ and $VP_3$. **c.** Charge stability diagram where an additional QD has been formed to the right of the DQD by raising the relevant tunnel barrier. The arrows indicate the position of the addition lines of the newly formed dot. **d.** Differentiated demodulated charge sensor signal as a function of virtual plunger $VP_4$ and virtual barrier $VB_4$. The charge addition lines corresponding to the newly formed QD are clearly visible. No transitions of the pre-existing dots are observed, due to the use of virtual gates. **e.** Visualization of the cross-capacitance matrix of the eight-dot array. The entries of each row show how the virtual plunger value (and hence the electrochemical potential) of a QD is influenced by other gate voltages. The rows for virtual barrier gates are omitted for simplicity. The plungers of both sensing dots are included in the matrix.

cross-capacitance matrix $A_5$ is found by matrix multiplication, $A_5 = A_5' A_4$. Additional dots, including the second sensing dot, are formed by repeating steps 3 to 5.

## 5.4 QUBYTE IN THE SINGLE-ELECTRON REGIME

We apply the $n+1$ method to form a sextuple QD and octuple QD. We start with a DQD confined between the barrier gates $B_1$ and $B_3$ and initially extend the array to the right. The electrochemical potentials and thus the number of electrons residing on all QDs can be independently controlled. The results are verified by charge stability diagrams of neighbouring pairs of virtual plunger gates, see Fig. 5.3b-f, where the sextuple dot has been initialized with one electron in each of the QDs. The gate voltages at the center of all of these plots are identical. All data sets have been acquired by fast voltage sweeps. Each plot can be interpreted as a charge stability diagram of a DQD, independent of the neighbouring QDs. The virtual gates control the electrochemical potential of the DQD and the number of electrons can be determined easily from the measurements. This set of measurements contains the full information of the charge state of the sextuple QD and is much easier to interpret and work with than conventional charge stability diagrams, where multiple charge addition lines as well as interdot transitions are visible in a single plot. In fact, the data of Fig. 5.1b was taken for illustration purposes only, after forming the sextuple dot using measurements such as those in Fig. 5.3.



Following the same $n+1$ method, the sextuple QD is further extended to an octuple QD array by adding another QD on each side. Due to limitations of the experimental setup (see Experimental methods section for details), the plunger gates $P_1$ and $P_8$ are not connected to high-frequency lines necessary to apply fast gate voltage sweeps. Therefore, any measurement using virtual gates involving these gates must rely on slow gate voltage sweeps. For this reason, we first formed a sextuple dot in the center and only then extended it to an octuple dot. Fig. 5.3a and g show charge stability diagrams as a function of $\mathrm{VP}_1$, $\mathrm{VP}_2$ and $\mathrm{VP}_7$, $\mathrm{VP}_8$, respectively, completing the formation of the Qubyte register.

The cross-capacitance matrix for the octuple QD configuration of Fig. 5.3 is shown in Fig. 5.2e. It visualizes the effect of plunger and barrier gates on the electrochemical potential of all QDs. As discussed, each row has been normalized such that the diagonal elements are 1. In these units, the effect of the closest barrier gates on the electrochemical potential of a QD is typically between 0.9 and 1.1. This is in agreement with the device geometry (see Fig. 5.1a) where the barrier gates are 30 nm longer than the plunger gates, bringing them close to the expected QD position. The influence of a neighbouring plunger gate on a dot potential is on the order of 0.4 to 0.5 and the one of the next-nearest neighbour 0.15 to 0.2, so the coupling diminishes with distance, as expected (Fig. 5.7 plots the cross-capacitance versus distance). The cross-capacitance to the sensing dots is small (typically below 0.1), but nevertheless it is relevant to correct for, as the sensing dots are operated at a steep slope of a Coulomb peak to maximize the charge detection sensitivity.

By means of the virtual barrier gates $\mathrm{VB}_i$, we can adjust the interdot tunnel couplings while cross-capacitance correction compensates the influence on the electrochemical po-

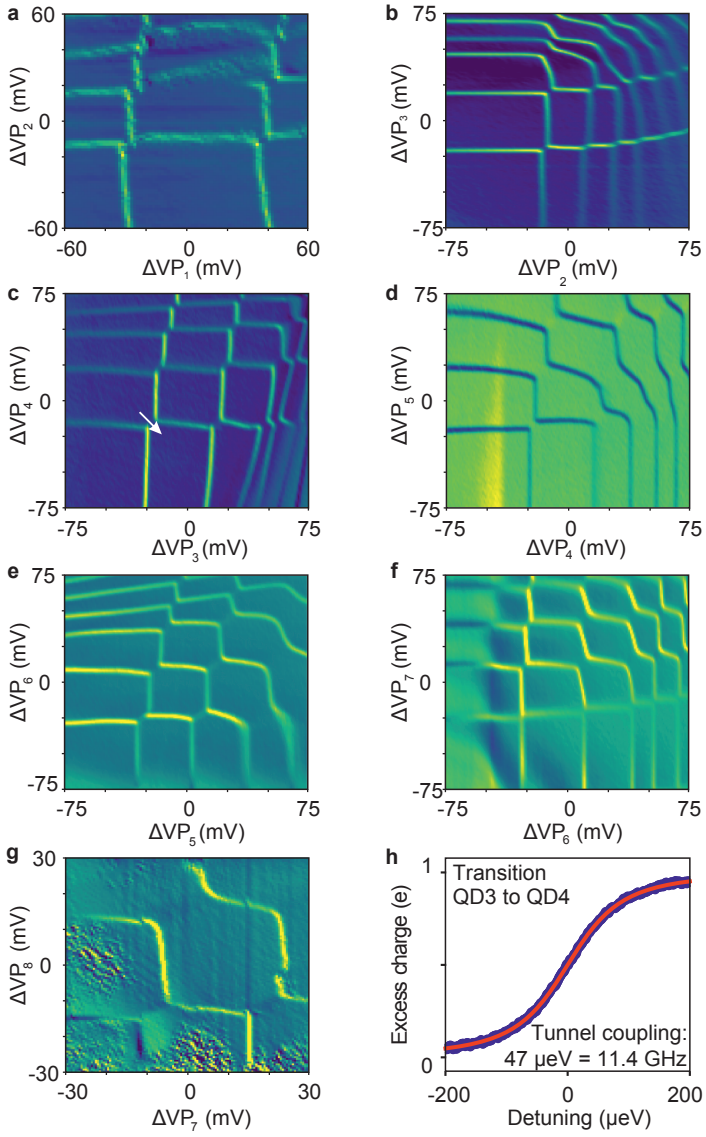


Figure 5.3.: **Qubyte in the single-electron regime. a-g.** Charge stability diagrams of pairs of neighbouring QDs within the array. The differential demodulated voltage is plotted as a function of the virtual plunger gates. For panels **b-f.**, the charge stability diagrams were measured with a sextuple QD defined between barrier gates $B_1$ and $B_7$. The measurements are centered around the single-electron occupation. Panels **a., g.** show charge stability diagrams of the two outermost DQDs of an octuple QD array. These panels took about 2 hours each, compared to 10 s for the other panels, and may thus be more susceptible to background charge rearrangements. **h.** Scan along the interdot detuning axis of $QD_3$ and $QD_4$ with one electron in those two dots (see arrow in **c**). The data has been fit according to the model described in [91, 132].

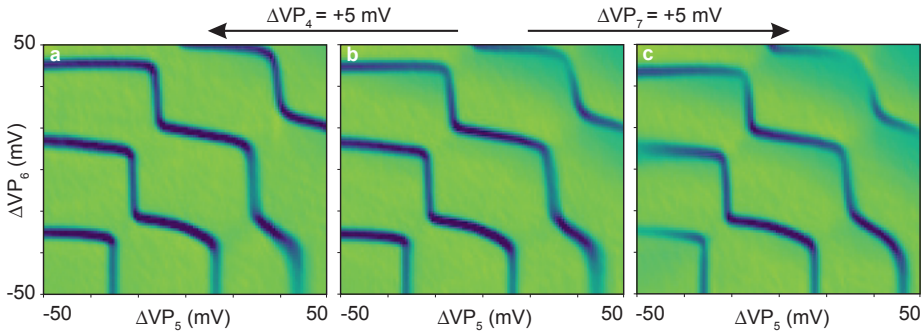


Figure 5.4.: **Verifying independent control of the electrochemical potentials.** Charge stability diagrams of $QD_5$ and $QD_6$ measured as function of the virtual plunger gates with all other QDs near the center of a charge stability region. Panel **b.** is a reference measurement. Panel **a., c.** are taken for identical gate voltages as **b.** except that $VP_4$ ($VP_7$) is increased by 5 mV. We note that stepping $VP_4$ ($VP_7$) has almost no influence on the charge stability diagram of $QD_5$ and $QD_6$. This figure shows a subset of the data shown in Fig. 5.10.

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tentials. To determine the interdot tunnel coupling, we measure the charge sensor response along the detuning axis across a single-electron transition. Fig. 5.3h shows an example for the (1,1,0,1,1,1)-(1,0,1,1,1,1) transition, where the numbers in brackets indicate the number of charges on each of the six dots, from $QD_2$ to $QD_7$. The data is fit according to a simple model considering broadening of the transition due to tunnel coupling and thermal excitation [91, 132], using a measured effective electron temperature of $T_e = 90$ mK. The tunnel coupling for all pairs of neighbouring dots has been tuned to a range of 5 to 15 GHz (see Fig. 5.9).

To further verify the validity of the $n+1$ method implemented via the use of virtual gates, we record the charge stability diagram of two neighbouring dots, while all other dots are kept in Coulomb blockade. One by one we step the virtual plunger gates of the neighbouring dots, which ideally should not affect the measured charge stability diagram. Fig. 5.4 depicts such a test for $QD_5$ and $QD_6$. In panel a, $VP_4$ has been increased compared to panel b and in panel c $VP_7$ has been increased. The charge stability diagram is not affected by small changes in neighbouring electrochemical potentials, which implies that the virtual gates behave as expected and verifies that the charge stability diagram indeed shows addition lines of the expected dots. The 5 mV step size was chosen large enough such that the functioning (or not) of the virtual gates can be properly tested, while remaining well below half the addition energy. A step (positive or negative) of more than half the addition energy would change the electron occupation. The same measurements are repeated for all QDs; charge stability diagrams of neighbouring QDs were measured while the electrochemical potential of all other QDs has been altered. Data sets for all gate combinations are shown in Fig. 5.10, showing similar results as presented in Fig. 5.4.

We note that it is not trivial that this method works flawlessly and care has to be taken to ensure the electron occupation of each dot is as intended. Specifically, it is important that the neighbouring QDs remain sufficiently far from any charge transitions. This requires that the cross-capacitances are measured with a reasonable accuracy, and that the neigh-

bouring QDs be detuned from the Fermi level by more than the interdot capacitive coupling energy. To illustrate this point, a set of charge stability diagrams for $QD_4$ and $QD_5$ is shown in Fig. 5.5a-c, with increasing values for $VP_6$ per panel (a video, available on https://doi.org/10.5281/zenodo.5731421, shows a similar effect in series of charge stability diagrams in steps of 0.5 mV in $VP_6$). Fig. 5.5a shows a reference plot of a clean charge stability diagram. In Fig. 5.5b, the same gate voltages are scanned but $VP_6$ has been changed by 10 mV. Extra lines appear, which disappear again when increasing $VP_6$ further (Fig. 5.5c). The extra lines can be understood if we inspect the charge stability diagram for $QD_5$ and $QD_6$, which is depicted in Fig. 5.5d with arrows indicating the values of $QD_6$ used in panels a-c. We see that arrow b, which corresponds to the case of Fig. 5.5b, passes through an interdot transition of $QD_5$ and $QD_6$, then intersects an addition line for $QD_6$ (since the virtual gates are not perfect, this addition line is slightly tilted) and finally cuts through another interdot transition of $QD_5$ and $QD_6$. These three crossings occur at the positions of the red circles in Fig. 5.5b. By comparison, arrows a and c do not pass through any charge transitions involving $QD_6$. This set of data makes clear how to avoid ambiguity in controlling and verifying the number of electrons on each dot.



We can observe the same effects in classical simulations of the charge stability diagrams. The simulation considers only three QDs and adopts the constant interaction model [62], meaning the charging energies and capacitive interdot coupling energies are assumed to be constant. Imperfections of the cross-capacitance matrix are taken into account in the model. Other effects, e.g. tunnel coupling, non-linearities of the cross-talk and latching effects are neglected. Fig. 5.5e shows a simulated charge stability diagram for $QD_5$ and $QD_6$, with the arrows a, b and c at similar locations as in the measurements of Fig. 5.5d. Fig. 5.5f shows the simulated charge stability diagram for $QD_4$ and $QD_5$, for the case of arrow b. Similar to the data in Fig. 5.5b, we observe extra lines in the simulated charge stability diagram, as arrow b passes through interdot transitions and an addition line for $QD_6$. While details vary, in part because tunnel coupling is not included in the simulation, the simulation results are in good qualitative agreement with the experimental data.

## 5.5 DISCUSSION

We developed a powerful technique to tune an array of QDs one by one and load it in the few electron regime. We apply this method to tune up a linear array of eight quantum dots in GaAs from scratch.

All charge stability diagrams have been acquired by fast voltage sweeps. At low resolution and low averaging, sufficient for tuning purposes, the acquisition time per panel is on the order of a few 100 ms. High-quality data sets such as those shown in Fig. 5.3b-f take approximately 10 s per panel. Based on these time scales, creating a six-dot array following the n+1 method, starting from measurement of the pinch-off characteristics of individual gates, currently takes one to two days for an experienced user and a well behaved sample. This was confirmed on a second sample of the same design. We did observe that not all lithographically similar devices are suitable to host eight QDs. During the initial DC characterization, in some devices

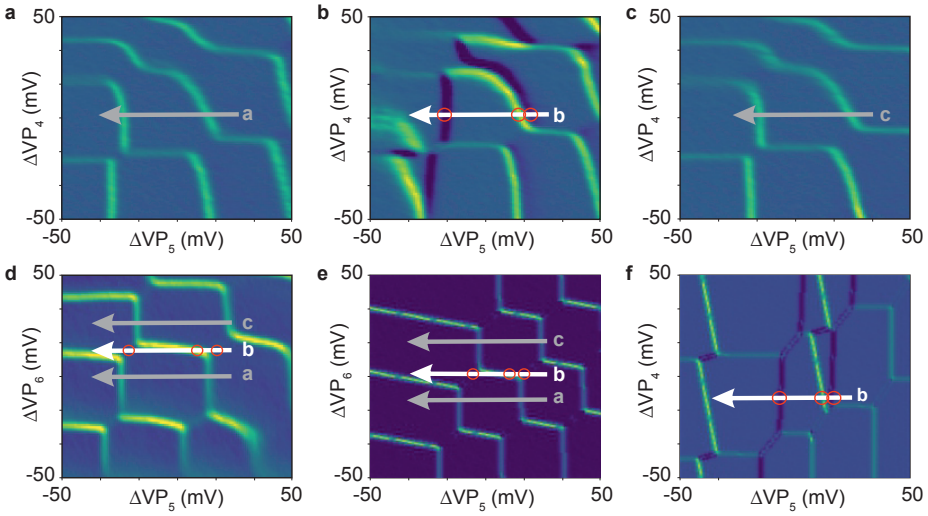


Figure 5.5.: **Possible pitfalls when using virtual gates. a-c.** Charge stability diagrams of $QD_5$ and $QD_4$. The virtual plunger $VP_6$ is stepped by 10 mV from **a** to **b** and by another 15 mV from **b** to **c**. In **b**, additional lines appear, which arise both from interdot and dot-reservoir transitions, as explained in the text. **d.** Charge stability diagram of $QD_6$ and $QD_5$. The arrows indicating cuts along the $VP_5$ axis for three different values of $VP_6$ correspond to the arrows in panels **a-c**. **e.** Simulated double dot charge stability diagram computed for a triple quantum dot system. The simulation assumes the constant interaction model, taking into account the capacitive interdot coupling and using on purpose an imperfect cross-capacitance matrix. The simulation results exhibit similar features as the measurements in panel **d**. The three arrows are drawn at the corresponding locations as in panel **d** as well. **f.** Simulated charge stability diagram computed for the same triple quantum as in **e**, but for the other DQD. Similar to the data in panel (**b**, we observe several additional interdot and dot-reservoir charge transition lines.

not all QDs could be formed individually or some QDs seemed to be positioned under a gate instead of in the channel. We note that this failure mode can be identified at an early stage of measurements prior to running the n+1 method. On the other hand, the method can cope with limited uniformity in a device and a certain amount of disorder, as seen from the variation in the pinch-off voltages in Tables 5.1-5.2. Furthermore, the virtual gates technique facilitates tuning of the tunnel couplings, which we showed could be tuned to a relevant range for qubit operations in this device.

With regards to the scalability of this method, we make the following observations. First, the cross-capacitance quickly drops with distance between the gates and the dots. Therefore, only the entries near the diagonal of the cross-capacitance matrix are relevant and need to be determined. This implies a linear scaling of the number of cross-capacitance elements as a function of the number of dots. Second, as we relied on charge addition lines in charge stability diagrams of neighbouring QDs to determine the number of electrons per dot, each of the QDs must be able to exchange electrons with at least one of the reservoirs. QDs not positioned at the end of the array need to exchange electrons via co-tunnelling, mediated by a virtual occupation of the QDs in between [62]. The co-tunnel rate scales inversely proportional with the number of interdot tunnel barriers between a dot and the nearest reservoir, as well

as with the detuning of the dots in between them [224]. As a result, we found that it was important to sufficiently open the existing interdot tunnel barriers before adding the last few dots, to avoid excessive latching effects. Once latching occurs, it becomes harder to reliable determine virtual gates and open the tunnel barriers. However, this is by no means a fundamental obstacle. When dots are formed one at a time, the newly formed dot is immediately adjacent to a reservoir and can thus be easily loaded. For dots in the interior, the $n+1$ method we introduced in principle takes care of maintaining their occupation through cross-talk compensation. If desired, verifying the dot occupation in the interior of a long array after it is formed can still be done, for instance by emptying the array (while not removing it), followed by sequential tunnelling of electrons to the desired locations [81]. Finally, we believe that the $n+1$ method is not bound to a specific device geometry or material. In particular, we expect that it is directly applicable to linear arrays in silicon based QD devices [107] and can be extended to two-dimensional QD arrays. The $n+1$ method can become a standard method to conveniently tune QD arrays and should lend itself well to automation [225, 226].

The data also shows the limitations of the current approach. We correct for the cross-capacitance of plunger and barrier gates influencing electrochemical potentials but not for the influence on tunnel barriers. As a consequence, altering a virtual plunger gate will affect neighbouring barriers, as can be seen in Fig. 5.3b. Increasing $VP_2$ and $VP_3$ increases the interdot tunnel coupling, which can be deduced from the broadening of the interdot transitions. In principle cross-capacitance effects on barriers can also be taken into account, as was demonstrated recently for a triple dot array [91]. However, this task is not trivial since the dependence of gate voltage to tunnel coupling is typically exponential and thus the linear approximation of the cross-capacitance matrix is only valid over a limited voltage range. As we have shown in this work, adjusting the interdot tunnel couplings individually is not a very difficult task, and this can be implemented using automated tuning algorithms as well [227].



## 5.6 CONCLUSION

Altogether, the $n+1$ method shown here enables future experiments involving increasing numbers of electron spin qubits in semiconductor quantum dot arrays. It addresses an important bottleneck in scaling up quantum dot arrays and highlights the potential of this approach for large-scale quantum computation and simulation.

## 5.7 EXPERIMENTAL METHODS

**Device fabrication**

The sample is fabricated from a silicon-doped GaAs/AlGaAs quantum well grown by molecular beam epitaxy. A two-dimensional electron gas is formed 90 nm below the surface. It shows a mobility of $1.6 \cdot 10^6$ cm$^2$/Vs at an electron density of 1.9x10$^{11}$ cm$^{-2}$. A single layer of metallic gates (Ti/Au), defined by electron-beam lithography, is biased with appropriate voltages to selectively deplete the 2DEG underneath. During cooldown, the gates have been biased individually with positive voltages between +50 and +250 mV to reduce charge noise [219, 220] and to improve the uniformity of the pinch-off characteristics of the gates.

Details on bias cooling and pinch-off voltages are shown in Tables 5.1-5.2.

| Gate names | $D$ | $B_0$ | $B_1$ | $B_2$ | $B_3$ | $B_4$ | $B_5$ | $B_6$ | $B_7$ | $B_8$ |
|---|---|---|---|---|---|---|---|---|---|---|
| Bias cooling | +100 | +50 | +100 | +100 | +200 | +250 | +200 | +250 | +200 | +200 |
| Pinch-off | . | -332 | -330 | -308 | -338 | -392 | -422 | -300 | -300 | -298 |
| 8dot configuration | -340 | -200 | -120 | -25 | -40 | -85 | -260 | -105 | -265 | -230 |

Table 5.1.: Voltages in mV applied to the barrier gates during cooldown, pinch-off voltages measured with -340 mV applied to the central gate D and typical gate voltages applied in the Qubyte configuration (all eight QDs tuned). The voltages applied during cooldown were chosen based on measurements from an earlier cooldown of the same device. On a second device where we successfully applied the $n+1$ method, we used a uniform bias cooldown voltage.

| Gate names | $P_1$ | $P_2$ | $P_3$ | $P_4$ | $P_5$ | $P_6$ | $P_7$ | $P_8$ | $Y_0$ | $X_1$ | $Y_1$ | $Y_2$ | $X_2$ | $Y_3$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bias cooling | +50 | +100 | +100 | +100 | +100 | +100 | +100 | +150 | +50 | +200 | +100 | +50 | +200 | +200 |
| Pinch-off | -640 | -624 | -592 | -524 | -604 | -444 | -494 | -288 | -700 | -750 | -700 | -500 | -1200 | -750 |
| 8dot configuration | -295 | -200 | -385 | -240 | -220 | +10 | -75 | 50 | -420 | 115 | -515 | -370 | 0 | -500 |
| Lever arm | . | 80 | 82 | 63 | 55 | 45 | 60 | . | . | . | . | . | . | . |

5

Table 5.2.: Voltages in mV applied to the plunger and sensing dot gates during cooldown, pinch-off voltages measured with -340 mV applied to the central gate D and typical gate voltages applied in the Qubyte configuration (all eight QDs tuned). The voltages applied during cooldown were chosen based on measurements from an earlier cooldown of the same device. The last row of the table contains the lever arm of the plunger gates in $\mu$eV/mV (measured in a double-dot configuration).

**Experimentel setup**

Plunger gates $P_2$ to $P_8$ of the array and the plunger gates of both sensing dots ($X_1$, $X_2$) are connected to bias-tees on the printed circuit board with a cut-off frequency of $f_C \approx 0.3$ Hz. This allows combining DC voltages and nanosecond gate voltage pulses on the same gate. Due to limitations of the experimental setup only eight gates ($P_2$ - $P_7$, $X_1$, $X_2$) could be connected to high-frequency lines. The bias-tee at $P_8$ limits the bandwidth to 0.3 Hz. Low-pass filtered DC lines are connected to $P_1$ ($f_C \approx 150$ kHz) and all barrier gates ($f_C \approx 5$ kHz).

Except for the initial characterization using DC transport, RF reflectometry is used, enabling fast, simultaneous readout of both charge sensors by frequency multiplexing [138, 228]. As the capacitive coupling and thus the sensitivity decreases with distance from the sensor, we read out both sensors simultaneously to maximize the readout quality. The charge stability diagrams shown in Figs. 5.2-5.5 show the signal from the nearest charge detector. The sum of the derivative along both axis is plotted. In Fig. 5.1b, the signals from the two charge sensors are added. LC tank circuits based on home-built superconducting NbTiN inductors are connected to the ohmic contacts of the sensing dots (see labels RF in Fig. 5.1a). RF tones close to the resonance frequencies of the tank circuits, at 108.5 MHz and 171.9 MHz, are sent to the sample. The reflected signal is amplified at 4K and at room temperature, I/Q demodulated to baseband, filtered with a 1 MHz low-pass filter, and recorded with a fast data acquisition card.

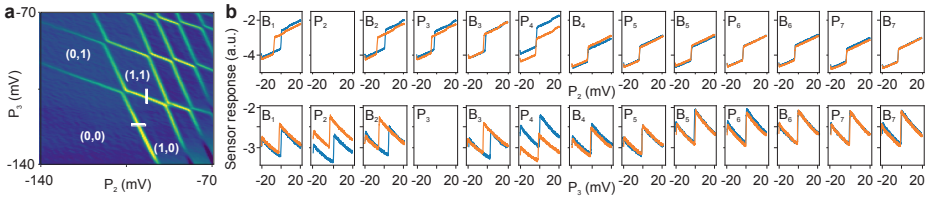


Figure 5.6.: **Measuring cross-capacitances. a.** Charge stability diagram of a DQD ($QD_2$ and $QD_3$) in the single-electron regime. Note that these are the first two dots formed, the 2DEG under the other gates is not depleted. Cross capacitance has not been corrected, i.e. the virtual gates are still equal to the physical gates. **b.** Set of scans to determine the cross-capacitance coupling of each of the gates to the potentials of $QD_2$ and $QD_3$. The scans of $P_2$ (top row) and $P_3$ (bottom row) are taken along the white lines in **a**, for two different values of the gate indicated within each panel. For the orange traces, the corresponding gate voltage has been increased by $\Delta V$ = +10 mV compared to the blue traces. As described above, from this set of measurements the entries of the cross capacitance matrix corresponding to $VP_2$ and $VP_3$ can be determined.

### Cross-capacitance calibration

The cross-capacitance factors are determined by one-dimensional scans. Figure 5.6b shows the cross-capacitance calibration for the first two QDs, $QD_2$ and $QD_3$, taken along the white lines in Fig. 5.1a. The cross capacitance from a gate to a QD is determined by stepping a gate with $\Delta V = 10$ mV and monitoring the shift ($\Delta$QD) in the addition line of the QD. The cross capacitance entry is determined as $\alpha = \Delta\text{QD}/\Delta V$. The resulting matrix is $A_2$ in Appendix A. How the cross-capacitance falls with the number of dots is depicted in Fig. 5.7.

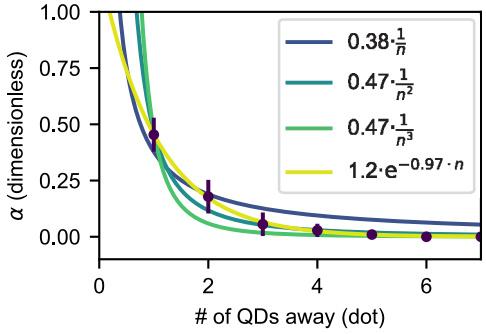


Figure 5.7.: **Cross-talk as a function of distance.** The measured cross-capacitance between plunger gates and QD electrochemical potential as a function of the distance between the gate and the dot. Each data point is the average of the corresponding matrix entries, with the error bar indicating the standard deviation. The data is fitted with several fit functions, as indicated.

### Charge stability traces

Fig. 5.8 shows an alternative visualization of the charge transitions of the sextuple QD. Performing just 1D sweeps of the virtual plunger gates, which are a horizontal or vertical cut through a 2D charge stability diagram, allows measuring all charge transitions with a refresh rate of a few Hz. This allows to control parameters of the sextuple dot and verify the effect on all the charge occupations of all six dots in real-time. While the 1D traces can be recorded

very fast, they lack certain information and are more prone to incorrect interpretation. For instance, in 1D traces, interdot tunnel couplings cannot be extracted and the difference between interdot and dot-reservoir transitions may or may not be easily seen. 2D charge stability diagrams remove such ambiguities or limitations.

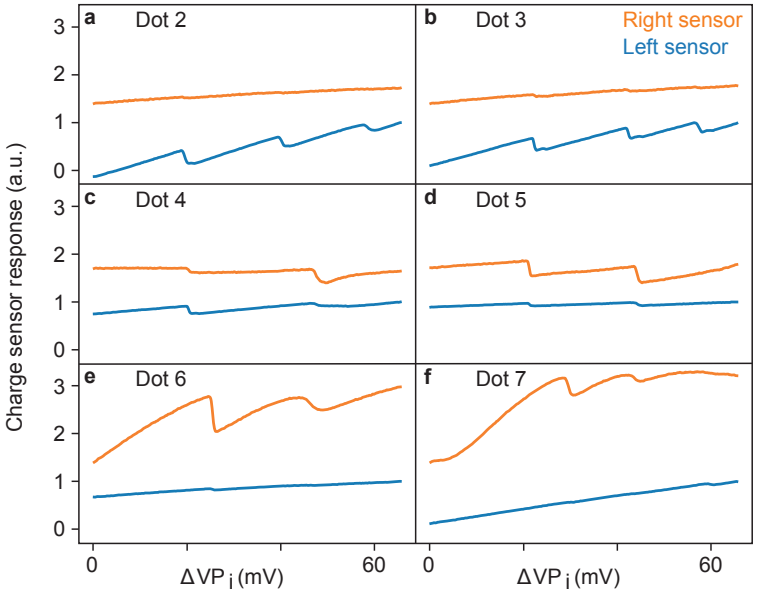


Figure 5.8.: **1D traces. a.-f.** Consecutive fast sweeps of the virtual plunger gates of the sextuple dot. The raw demodulated signal of both sensors is shown. The data shows that the left charge sensor is most sensitive to charge transitions of $QD_2$ and its sensitivity decreases for dots farther away. It is practically insensitive to charge transitions in $QD_6$ and $QD_7$. Both charge sensors are thus necessary to read out the full device.

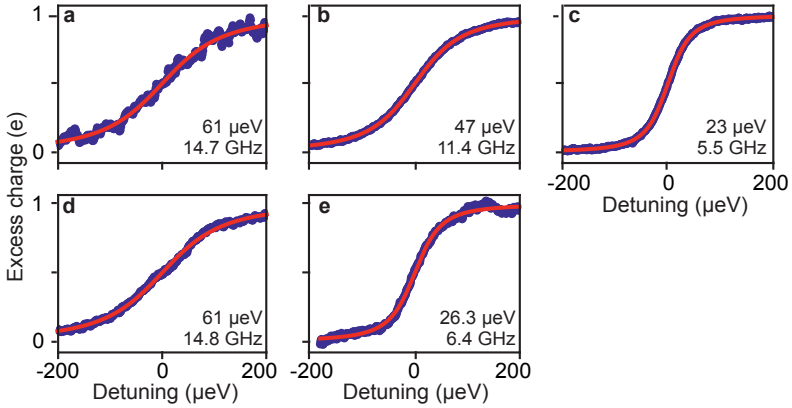


Figure 5.9.: **Tunnel coupling.** Scan along the interdot detuning axis of neighbouring QDs with one electron in these two dots. The data has been fit according to the model described in [91, 132]. In each panel the tunnel coupling extracted from the data is given in $\mu$eV and GHz.

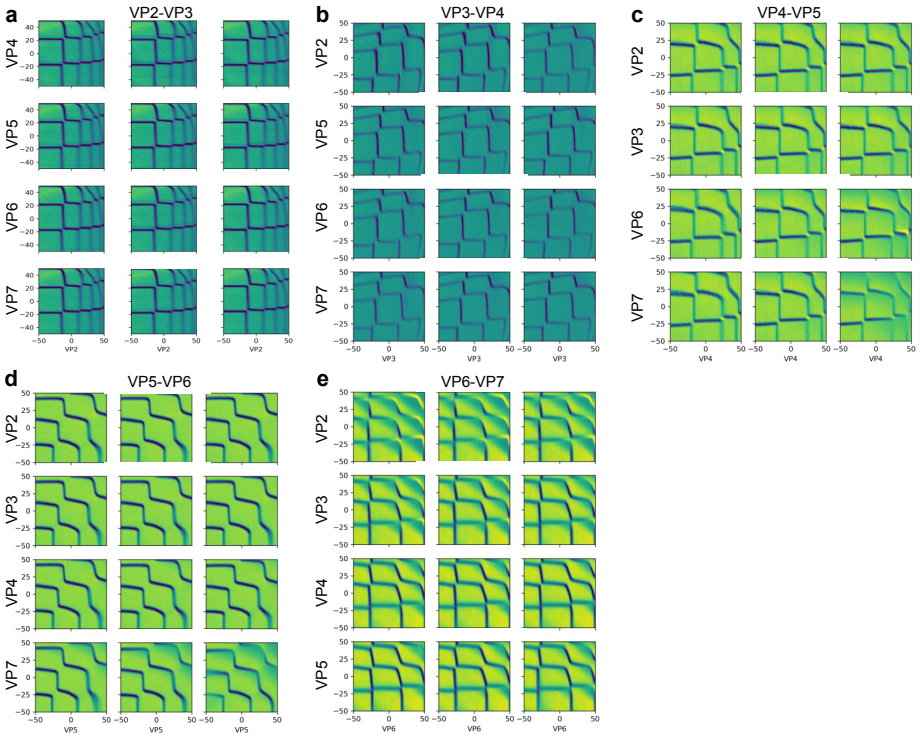


Figure 5.10.: **Verification of charge addition lines.** Charge stability diagrams of **a.** $VP_2$ and $VP_3$, **b.** $VP_3$ and $VP_4$, **c.** $VP_4$ and $VP_5$, **d.** $VP_5$ and $VP_6$ and **e.** $VP_6$ and $VP_7$. In each of the panels the other gate voltages have been stepped by $-5$ mV (left) and $+5$ mV (right) from the center panel. The stepped gate is indicated on the side of the panels.

# 6 SHUTTLING AN ELECTRON SPIN IN A SILICON QUANTUM DOT ARRAY

*Coherent links between qubits separated by tens of micrometers are expected to facilitate scalable quantum computing architectures for spin qubits in electrically-defined quantum dots. These coherent links allow to generate space for classical on-chip control electronics between qubit arrays, which can help to alleviate the so-called wiring bottleneck [54]. An elegant method of achieving coherent links between distant spin qubits is by shuttling the spin through an array of quantum dots. Here, we use a linear array of four tunnel-coupled quantum dots in a Si/SiGe heterostructure to create a short quantum link. We move an electron spin through the quantum dot array by adjusting the electrochemical potential for each quantum dot sequentially. This allows us to shuttle an electron forward and backward through the array up to* 250 *times, which corresponds to a total distance of approximately* 80 *µm, without measurable loss of the spin polarization.*

AM.J. Zwerver, S.V. Amitonov, S.L. de Snoo, M. Russ, M.T. Mądzik and L.M.K. Vandersypen, *In preparation*, 2022.

## 6.1 INTRODUCTION

Practical quantum computation requires millions of high-quality qubits. To scale to these millions of qubits, spin qubits in electrically-defined silicon quantum dots are particularly of interest because they combine a high quality with a small footprint. Recently, long-lived spin qubits have been demonstrated in silicon [49], as well as high-fidelity single [50, 67] and two-qubit gates [51, 52, 229]. Moreover scaling the number of spin qubits while maintaining a high fabrication yield can be advanced by employing semiconductor manufacturing techniques (chapter 7 of this thesis).

Several architectures have been proposed to scale to the large qubit numbers that we need for fault-tolerant quantum computation [41]. It is commonly recognized that for spin qubits, long-range qubit connections are a crucial part in such scaling architectures [37, 54–56, 230]. These quantum links would alleviate the constraints on the overhead that is necessary to form and control the qubits. Moreover, separating qubit registers on the same chip from each other by some distance would allow for the placement of on-chip control electronics, which can significantly reduce the number of input/output lines of the chip.



With regards to scaling architectures, the establishment of long-range spin coupling is therefore an essential research area. Several approaches have been proposed and explored, among which distant qubit connections via coherent SWAP operations [231]. Moreover, quantum information transfer can be achieved by means of flying qubits. Both photon-mediated qubit coupling via a superconducting resonator [109, 110, 232–234] and surface acoustic waves (SAW) [235, 236] have been demonstrated as promising quantum links. Although the superconducting resonator can additionally be used for gate-dispersive readout [53], the footprint of the superconducting resonator makes this approach particularly interesting for qubit coupling beyond the $\mu$m-scale. Also electron transport through SAW requires large overhead. Furthermore, the method makes use of the piezo-electro effect in GaAs, which is absent in Si.

Electron shuttling offers a promising alternative for spin transfer on the sub-mm scale. Bucket-brigade-mode shuttling, where an electron is transported through an array of quantum dots by successively adjusting their electrochemical potentials, has successfully been demonstrated in GaAs devices, both in linear quantum dot arrays [81, 85] and in triangular [237] and two-dimensional arrays [90]. Yet, with the focus of the research field shifting to silicon, it is to be demonstrated whether these results hold: silicon samples inherently exhibit more disorder than samples in GaAs, which can hinder the shuttling success. Moreover, Si has an extra degree of freedom in the form of a valley state that adds an additional loss channel for the shuttling spin [96]. Promising results have been obtained by shuttling a charge through a linear array of multiple SiGe quantum dots with the bucket brigade mode [107] and by the use of a slow-motion travelling potential wave [108]. Moreover, spins have been coherently shuttled back and forth through two neighbouring quantum dots in SiMOS [238] and SiGe [239]. Yet, spin shuttling through long quantum dot arrays remains to be demonstrated. Here, we shuttle a single spin through a five-quantum-dot linear array, occupying three, or four quantum

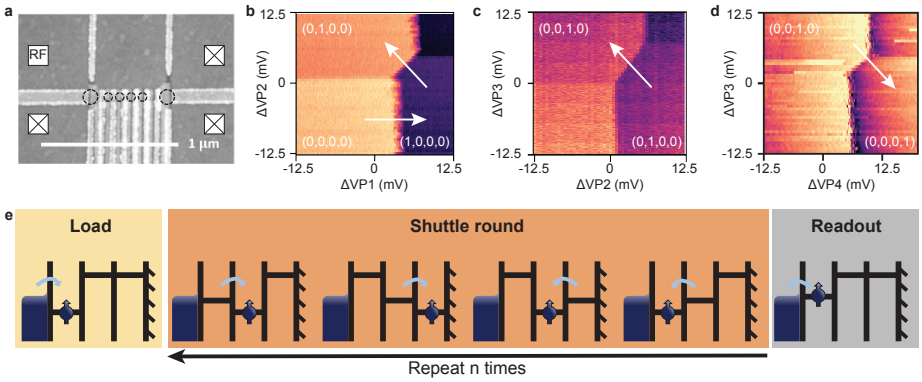


Figure 6.1.: **Shuttling through a Si/SiGe device. a.** Scanning-electron microscope image of a device nominally identical to the device used for this work. The device can contain a linear array of five quantum dots by sufficiently tuning the plunger gates (grey) and barrier gates (white) in the array. The quantum dots used in this work are indicated by the small circles. The sample contains a sensing dot on either side of the array (big circles), of which the left sensor is connected to an RF readout circuit via the ohmic reservoir. **b, c, d** Charge stability diagrams for (**b**) quantum dots 1-2, while quantum dots 3, 4 are empty, (**c**) quantum dots 2-3, while quantum dots 1,4 are empty and (**d**) quantum dots 4-3, while quantum dots 1,2 are empty. The charge stability diagrams are measured by means of virtual gates. The electron occupation per charge region and the shuttling trajectory of the spin are indicated on the figures. **e.** Shuttling procedure through three quantum dots. An electron spin is loaded with random polarization into quantum dot 1. A shuttling round consists of shuttling the electron to quantum dot 2, then to quantum dot 3 and back. The shuttling is repeated for *n* rounds. Eventually, the electron polarization is read out by means of energy-selective tunnelling.



dots. We move the electron forth and back through the array for up to 1000 hops, equal to a distance of 80 $\mu$m, without indication of the loss of its spin polarization.

## 6.2 SHUTTLING PROCEDURE

Figure 6.1a shows a scanning electron micrograph nominally identical to the sample used for this work. The device is fabricated on an undoped Si/SiGe heterostructure, with a strained 10-nm $^{28}$Si quantum well, 32 nm below the surface. The device contains three layers of Ti/Pd gate electrodes, respectively screening gates, plunger and accumulation gates and barrier gates, isolated by $Al_2O_3$ dielectric layers. The sample can host a linear array of up to five quantum dots with an 80-nm pitch by applying a bias to the metallic gate electrodes, where the plunger gates allow for adjustment of the electrochemical potentials of the quantum dots, whereas the barrier gates control the tunnel couplings between the quantum dots. On either side of the array, a sensing dot can be formed, which doubles as electron reservoir. All measurements are performed in a dilution refrigerator with a base temperature below 20 mK and with an applied in-plane magnetic field of 1.3 T. This magnetic field is well above the valley splitting of the quantum dots, which ranges between 80 and 85 $\mu$eV ( [240], Fig. S5a-c).

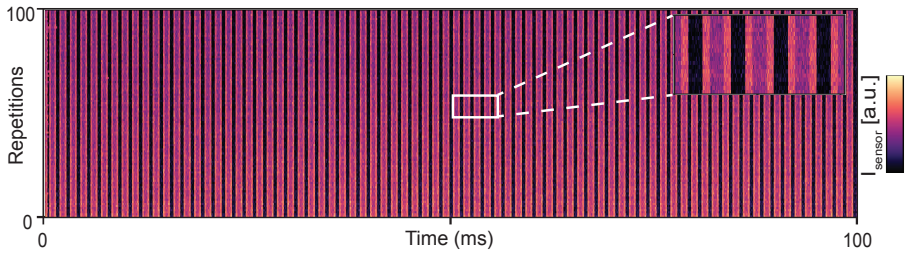


Figure 6.2.: **Shuttling many rounds.** Single-shot sensor response for 100 shuttling traces. The spin is loaded in dot 1 and then shuttled forth and back to dot 3 for 78 rounds. Each single-shot trace has an offset in $VP_1$ of 0.04 mV. We see that for each trace, the electron shuttles back and forth as expected, making the shuttling deterministic at this pace, 300 $\mu$s per hop. Inset: zoom in of a part of the plot to emphasize the sensor response.



By means of virtual gates and the method described in chapter 5, we tune the five-quantum-dot linear array to the single-electron regime, such that the electron occupation of the five dots is (1, 1, 1, 1, 1), with quantum dot 1 on the left and quantum dot 5 on the right side of the array. All quantum dots can be formed simultaneously, yet a defect in one of the high-frequency lines prohibits fast control of the fifth quantum dot. As these fast pulses are essential for shuttling, we will focus on the leftmost four quantum dots for the remainder of this work. Initially, we shuttle over three quantum dots, see Fig. 6.1b-c for the charge stability diagrams. Later, we will also shuttle through quantum dot 4, Fig. 6.1d. The tunnel coupling between the quantum dots is tuned between $\sim 2 - 4$ GHz.

A schematic of the shuttling sequence over three quantum dots is depicted in Fig. 6.1e. The shuttling procedure starts in the (0, 0, 0)-regime, with the three electrochemical potentials of the quantum dots well above the Fermi energy of the reservoir. By lowering the electrochemical potential of quantum dot 1 and pulsing deep into the (1,0,0)-regime, we load an electron with random spin polarization in quantum dot 1. Then, we sequentially shuttle the electron through the 1-2 anticrossing into the (0,1,0)-regime and through the 2-3 anticrossing into (0,0,1). By reversing the sequence, we shuttle the spin back to quantum dot 1. To ensure a well-controlled transition between the quantum dots and prevent shuttling errors in the charge or valley state, the electrons need to be moved through the anticrossing adiabatically with respect to the inter-dot tunnel coupling. We design our pulse scheme to ensure adiabatic transition through the anticrossing; first, we pulse to a point close to the anticrossing and then ramp through the anticrossing before we pulse deep into the new quantum dot. When the spin is in a particular quantum dot, the electrochemical potentials of the other quantum dots are pulsed well-above the Fermi energy of the reservoir, such that the electron is prevented from tunnelling back and no second electron can enter the array. We can repeat the shuttling sequence up to $n$ rounds and eventually determine the spin polarization by means of energy-selective readout [75]. The shuttling procedure through four quantum dots is similar, with the addition of a quantum dot.

## 6.3 SPIN SHUTTLING

First, we measure the spin relaxation time in each quantum dot separately. We do so by following the shuttle procedure to move the spin to the desired quantum dot and varying the wait time in this quantum dot. Thereafter, the electron is shuttled back to quantum dot 1 and its spin polarization is determined. For the measurements in quantum dot 2 and 3, the load time in quantum dot 1 is set to 50 $\mu$s, to ensure both the loading of an electron in the quantum dot array and potential relaxation to the lower valley [69, 104, 117, 241]. To ensure adiabatic spin transfer, the time for passing through the subsequent anticrossings is set to 10 $\mu$s per transition. We determine a relaxation time for quantum dot 1, quantum dot 2 and quantum dot 3 of $T_{1,1} = 124 \pm 29$ ms, $T_{1,2} = 270 \pm 95$ ms and $T_{1,3} = 148 \pm 44$ ms respectively, where the uncertainty is one standard deviation around the mean, see Fig. 6.5. The relatively large error bars are a result of the sparsity of data points for longer waiting times.

Following spin shuttling work in a GaAs device [81], we study the effects of shuttling the electron through the array on the spin polarization. Initially, the electron is shuttled forth and back through the array once, while the total wait time in the array, $t_{array}$ is divided symmetrically and equally over the quantum dots. By varying $t_{array}$, the weighted relaxation time of the spin in the array can be determined. The weighted relaxation time for three dots is plotted in Fig. 6.3a (black circles). Fitting the data to an exponential yields a relaxation time of $T_{1,weighted} = 174 \pm 24$ ms. We expect that the measured weighted $T_1$ is related to the relaxation times of the separate dots as:

$$T_{1,weighted} = 3(\frac{1}{T_{1,1}} + \frac{1}{T_{1,2}} + \frac{1}{T_{1,3}})^{-1}. \tag{6.1}$$

With regards to the $T_1$ values of the separate quantum dots, we expect $T_1 = 162 \pm 45$ ms. The weighted relaxation time falls within the uncertainty range.

Yet, practical quantum links will extend for several micrometers. To verify whether long-range spin shuttling is achievable in Si/SiGe samples, we mimic a quantum link by shuttling the electron forth and back through the array for many shuttling rounds, while monitoring the (virtual) sensor response, see fig. 6.2. Apart from some latching during the spin loading in the array - the tunnel barrier with the reservoir had to be sufficiently closed to allow for the readout protocol - we see that the electron shuttles forth and back through the array as expected. This is a prerequisite for the spin to be shuttled with high fidelity.

To analyse the effect of shuttling on the spin polarization, we vary both the number of shuttling rounds and the total shuttling time; we load an electron with random spin polarization into the array and shuttle it a various number of shuttle rounds through the array for a fixed time, $t_{array}$. Figure 6.3a (b) shows the spin up probability after $n$ shuttling rounds through three (four) dots for $t_{array}$ varying between 25 ms and 300 ms. Note that each shuttle round through three (four) quantum dots contains four (six) subsequent hops between neighbouring quantum dots. For shuttling through three quantum dots, we find that, for each wait time, there is no sign of systematic decay of the spin up probability up to $n = 250$ ($n = 500$, see Fig. 6.7)

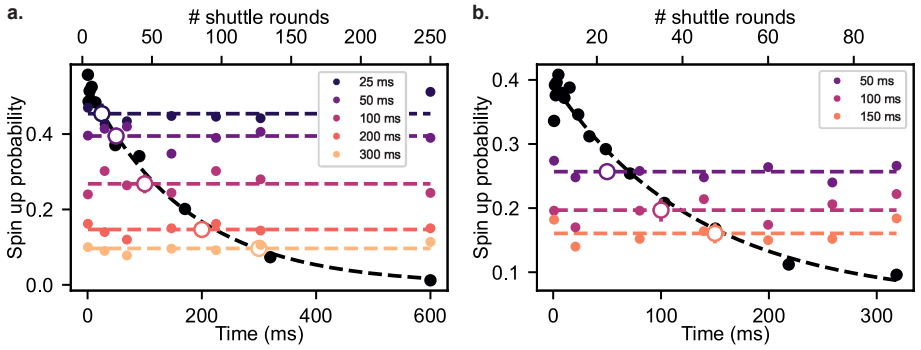


Figure 6.3.: **Spin polarization after multiple rounds of shuttling. a.** Shuttling through three quantum dots. Spin-up probability after shuttling back and forth through the quantum dot array once for varying shuttling times (black circles). Each data point is averaged 750 times. Fitting an exponential to the data yields a $T_1$ of 174 $\pm$ 24 ms. The coloured circles represent the spin-up probability for five different total shuttling times after shuttling the spin back and forth through the array *n* rounds (top axis). Each data point is averaged 500 times. The average spin up probability for all shuttle rounds per wait time is plotted as a function of wait time (open circles). The error bar of 1 standard deviation mainly falls within the open circles. The dashed coloured lines also represent the average of the data points per time and are a guide to the eye. **b.** Shuttling through four quantum dots. Spin up probability after shuttling back and forth through the quantum dot array once for varying shuttling times (black circles). Each data point is averaged 500 times. Fitting an exponential to the data yields a $T_1$ of 136 $\pm$ 30 ms. The coloured circles represent the spin-up probability for a $t_{array}$ of 50 ms, 100 ms and 150 ms respectively after shuttling the spin back and forth through the array *n* rounds (top axis). Each data point is averaged 500 times. The average spin up probability for all shuttle rounds per wait time is plotted as a function of wait time (open circles). The error bar of 1 standard deviation mainly falls within the open circles.

shuttle rounds, which equals 1000 (2000) hops, or 80 (160) $\mu$m. For shuttling through four quantum dots, the results are analogous up to at least 90 rounds (540 hops and 43 $\mu$m).

The average spin up probability for all shuttling rounds per $t_{array}$ falls almost exactly on the weighted $T_1$ plot, which indicates the absence of spontaneous spin flips, other than through relaxation. Still, we analyse the effect of spin flips during the shuttling process. Ref. [81] considers three mechanisms that can cause a spin flip: electron exchange with the reservoirs, hyperfine interaction with the nuclear spins and spin flips induced by spin-orbit interaction. We assume that spin flips caused by the first two mechanisms can be neglected, as the pulses are precisely tuned, the tunnel barriers to the reservoirs are sufficiently closed compared to the inter-dot tunnel barriers and the quantum dot is fabricated on an isotopically-enriched $^{28}$Si quantum well. The spin-orbit interaction is believed to be small in silicon samples [63], although there are measurements in SiMOS indicating a spin-orbit length of only 1 $\mu$m [242]. We therefore analyse the accumulation of errors through transition-induced spin flips by simulating such events and comparing the simulations to the measurement data. Even when the probability for transition-induced spin flips is 0.02% per transition, we should see an increase of spin-up probability as the number of shuttle rounds increases, see Fig. 6.6. When fitting a linear curve to the data, we see a change in spin up probability between $-6 \times 10^{-5}$

and $2.4 \times 10^{-4}$ per hop. This indicates that the probability of spontaneous spin flips to occur is smaller than $0.02\%$ per hop.

The fastest shuttle times used in this experiment amount to about $12.5$ $\mu$s per hop. This shuttle-time hovers around the $T_2^*$-times measured in isotopically enriched silicon [49–51, 125, 157, 243]. For coherent spin shuttling, the shuttling rate should be increased by at least one order of magnitude. Subsequent shuttle efforts should therefore focus on decreasing the shuttle time by increasing the tunnel rate between the quantum dots and increasing the ramp rates through the anticrossings. In this way, the effect on the qubit coherence of shuttling through a longer quantum dot array can be studied. For future experiments, a more elegant way of electron shuttling can be realized by moving the electron in a travelling potential wave [108, 244].

## 6.4 CONCLUSION

In conclusion, we demonstrated the shuttling of an electron through a virtual array of $1000$ quantum dots by means of the bucket-brigade mode, with no signs of degration of its spin polarization. We monitored $100$ shuttling traces and observe that for each trace, the spin moves back and forth through the quantum dot array as expected. The method used in this work can be easily extended to larger quantum dot arrays, which highlights the potential of electron shuttling for long-range qubit coupling. Ongoing research will focus on determining the shuttling feasibility for long-range quantum interconnects by looking for high-fidelity, coherent shuttling.



## 6.5 EXPERIMENTAL METHODS

Experimental methods regarding the data in this chapter.

**Setup**

The measurements were carried out in an Oxford Triton dry dilution refrigerator with a base temperature around $10$ mK. The dc part of the setup consists of two in-house built, battery-powered SPI racks, containing digital-to-analog converters. The voltage pulses applied to the sample are generated by two Tektronix AWG5014 arbitrary waveform generators and sent to the sample via coaxial lines, connected to the sample via a bias tee with a cut-off frequency of $3$ Hz on the printed circuit board. The response of the left charge sensor was monitored with an RF reflectometry setup at a resonance frequency of $f = 214$ MHz, containing an in-house fabricated NbTiN inductor. The signal is amplified at the 4-Kelvin plate and demodulated using an in-house built SPI demodulation rack. The sensor response of the right charge sensor was converted to voltage through a home-built amplifier. This latter signal was not used for single-shot readout.

**Data analysis**

During the measurements, we encountered a timing problem between the AWG and the digitizer, which resulted in a an offset of up to $50$ $\mu$s in the readout traces for different shuttle

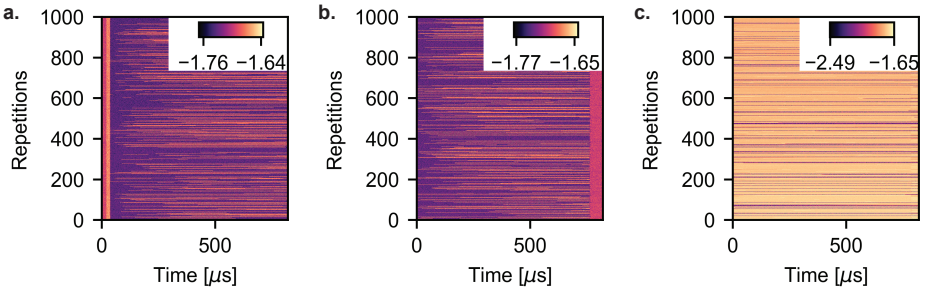


Figure 6.4.: **Single-shot traces for three different data points.** Single-shot traces for shuttling the electron 250, 500 and 8 rounds through the array respectively for $t_{array} = 25$ ms. The sensor reponse is monitored on the digitizer in Volt. **a.** The digitizer timing is slightly offset with respect to the readout pulse; the last two shuttling steps are recorded on the left side of each trace. **b.** The digitizer timing is offset with respect to the readout pulse; the start of the compensation pulse is recorded on the right side of each trace. **c.** Digitizer error, several 'empty' lines are recorded at a digitizer response significantly lower than the single-shot traces. These are the data for the outlier in Fig. 6.7.

rounds, see Fig. 6.4. To ensure a similar readout duration for each data trace, we cut off the start and end of each data trace by the same number of points. Thereafter, we smoothen the data by means of boxcar averaging; we average each data point with the 25 points around it. Subsuquently, we assign each data trace '0', or '1' by means of relative thresholding.

6

### Relaxation times in each quantum dot

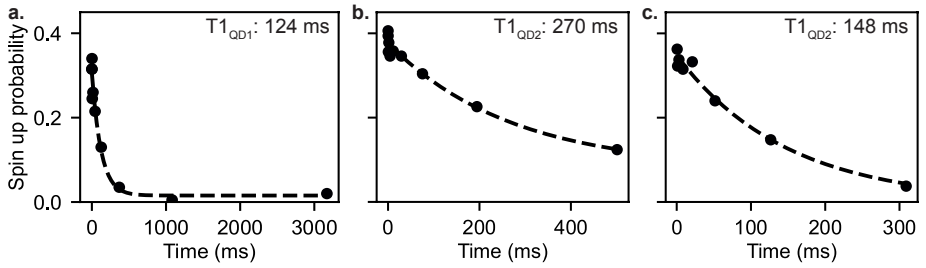


Figure 6.5.: **Relaxation times for the separate quantum dots.**Spin up probability of a randomly loaded spin as a function of waiting time in (**a**) dot 1, (**b**) dot 2 and (**c**) dot 3 at a magnetic field of 1.3 T. Fitting the data to an exponential decay yields relaxation times of $T_{1,1} = 124 \pm 29$ ms, $T_{1,2} = 270 \pm 95$ ms and $T_{1,3} = 148 \pm 44$ ms. Each data point is averaged 300, 500 and 400 times for dot 1, 2 and 3 respectively.

### Simulation of spontaneous errors

In the main text, we comment that three possible spin flip mechanisms have an easier smaller effect than in an earlier shuttling experiment on a GaAs quantum dot array. Here, we try to bound the spin-flip probability by comparing numerical simulations with the experimental data. Fig. 6.6 shows numerical simulation results considering a 0.02% probabiity of a transition-induced spin flip from spin down to spin up when shuttling from left to right and a 0.02%

probability of a transition-induced spin flip from spin up to spin down when shuttling from right to left. Other numerical simulations for the case of a spin flip being higher than 0.02% and the probabilities on a spin flip up/down being unequal, show a still larger effect on the spin-up probability.

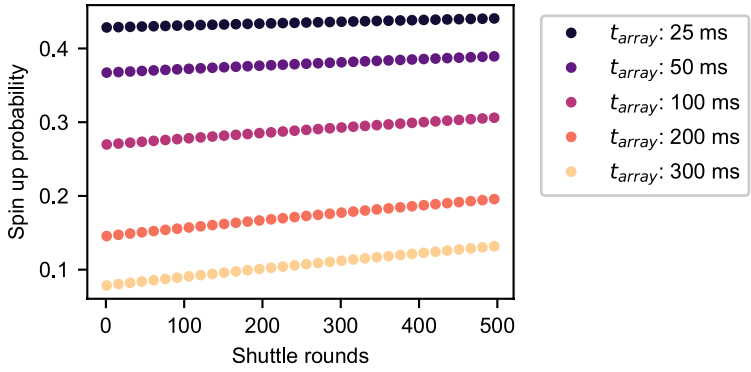


Figure 6.6.: **Simulation of spontaneous errors.** Spin-up probability versus number of shuttle rounds when there is a 0.02% probability of a bit flip during transitions.



### Shuttling 500 rounds

Data for shuttling through three quantum dots up to 500 shuttling rounds.

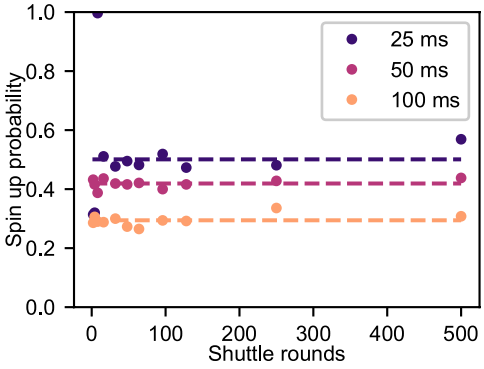


Figure 6.7.: **Shuttling 500 rounds through an array of three quantum dots.** Shuttle data for shuttling an electron up to 500 rounds (2000 hops) through an array of three quantum dots. Each data point is the average of 1000 single-shot traces, taking for three different total times in the quantum dot array: 25, 50 and 100 ms. As there was a shift in the readout position during the data collection, while the total time in the array was 25 ms, the first four data points have a calibration error. These points are plotted, yet are not taken into account for the data analysis.

# 7 QUBITS MADE BY ADVANCED SEMICONDUCTOR MANUFACTURING

*All of our devices can be mass produced so that they are absolutely perfect copies of one another*

Richard Feynman

*Full-scale quantum computers require the integration of millions of qubits and the potential of using industrial semiconductor manufacturing to meet this need has driven the development of quantum computing in silicon quantum dots. However, fabrication has so far relied on electron-beam lithography and, with a few exceptions, conventional lift-off processes that suffer from low yield and poor uniformity. Here, we report quantum dots that are hosted at a* $^{28}Si/^{28}SiO_2$ *interface and fabricated in a* 300 *mm semiconductor manufacturing facility using all-optical lithography and fully industrial processing. With this approach, we achieve nanoscale gate patterns with excellent yield. In the multi-electron regime, the quantum dots allow good tunnel barrier control, a crucial feature for fault tolerant two-qubit gates. Single-spin qubit operation using magnetic resonance in the few-electron regime reveals relaxation times of over* 1 *s at* 1 *T and coherence times of over* 3 *ms.*

This chapter has been adapted from A.M.J. Zwerver, T. Krähenmann, T.F. Watson, L. Lampert, H.C. George, R. Pillarisetty, S.A. Bojarski, P. Amin, S.V. Amitonov[1], J.M. Boter, R. Caudillo, D. Corras-Serrano, J.P. Dehollain, G. Droulers, E.M. Henry, R. Kotlyar, M. Lodari, F. Lüthi, D.J. Michalak, B.K. Mueller, S. Neyens, J. Roberts, N. Samkharadze, G. Zheng, O.K. Zietz, G. Scappucci, M. Veldhorst, L.M.K. Vandersypen, J.S. Clarke,
*Nature Electronics*, **5** (3), 2022.

## 7.1 INTRODUCTION

The idea of exploiting quantum mechanics to build computers with computational powers beyond any classical device has gathered momentum since the 1980s [25]. However, in order for full-fledged quantum computers to become a reality they need to be fault tolerant: that is, errors from unavoidable decoherence must be reversed faster than they occur [245]. The most promising architectures also require a system that is scalable to millions of individually-addressable qubits with a gate fidelity over 99% and tuneable nearest-neighbour couplings [43, 246].

Spin qubits in gate-defined quantum dots (QDs) offer great potential for quantum computation due to their small size and relatively long coherence times [48, 61, 63]. Single-qubit gate fidelities over 99.9% [50, 67] and two-qubit gate fidelities over 99% [51, 52, 247] have already been demonstrated, as well as algorithms [104], conditional teleportation [248], three-qubit entanglement [106] and four-qubit universal control [72]. Moreover, silicon spin qubits have been operated at relatively high temperatures of 1–4 K [123, 124], where the higher cooling power enables scaling strategies with the integration of control electronics [54, 55, 105, 249, 250].

A major advantage of silicon spin qubits is that they could leverage decades of technology development in the semiconductor industry. Today, industrial manufacturing conditions allow the fabrication of uniform transistors with gate lengths of several tens of nanometres and spaced apart by 34 nm (fins) to 54 nm (gates) — feature sizes that are well below the 193 nm wavelength of the light used in the lithography process [251]. This engineering feat, and the high yield that allows integrated circuits containing billions of transistors to function, are enabled by adhering to strict design rules and by using advanced semiconductor manufacturing techniques such as multiple patterning for pitch doubling, subtractive processing, chemically selective plasma etches, and chemical mechanical polishing [252]. These processing conditions are more intrusive than the e-beam lithography [49, 50, 70, 104, 118, 123, 195, 198, 199, 242, 253–257] and metal lift-off [49, 50, 104, 118, 123, 195, 198, 199, 254] processing conditions typically used for quantum dot fabrication, but they will be key to achieving the extremely high yield necessary for the fabrication of thousands or millions of qubits in a functional array.

A quantum dot device is similar to a transistor, taken to the limit where the gate above the channel controls the flow of electrons one at a time [258]. In linear qubit arrays, the transistor gate is replaced by multiple gates, which are used to shape the potential landscape of the channel into multiple potential minima (quantum dots), to control the occupation of each dot down to the last electron, and to precisely tune the wavefunction overlap (tunnel coupling) of the electrons in neighbouring dots [62]. In addition, qubit devices commonly rely on nearby integrated charge sensors to provide single-shot spin readout and high-fidelity initialisation [36, 61].

A key question is then whether the reliable but strict design rules of industrial patterning can produce suitable qubit device layouts. A separate consideration is that qubit coherence is easily affected by microscopic charge fluctuations from interface, surface and bulk defects.

Therefore, another key question is whether the coherence properties of the qubits survive the processing conditions needed to achieve high yield and uniformity. Quantum dots and qubits fabricated on the wafer-scale in industrial foundries have been reported [70, 253, 255–257], but they rely on electron-beam lithography and avoid chemical mechanical polishing for the active device area. Chemical mechanical polishing requires a uniform metal density across the wafer, which introduces its own complexities for quantum dot devices due to the large amount of floating metal and added capacitance. In this chapter, we report fully optically-patterned quantum dots and qubits that are made in a state-of-the-art 300 mm wafer process line, similar to those used for commercial advanced integrated circuits.

## 7.2 DEVICE ARCHITECTURE AND FABRICATION

A dedicated mask set based on 193 nm immersion lithography is created for patterning quantum dot arrays of various lengths, as well as a number of test structures, such as transistors of various sizes and Hall bars. These test structures allow us to directly extract important metrics at both room temperature and low temperature, including mobility, threshold voltage, subthreshold slope and interface trap density. Analysed together, these metrics give us understanding of the gate oxide and contact quality along with the electrostatics to help troubleshoot process targeting [259]. Once the test structure metrics are satisfactory, we then characterise the quantum dot arrays.



As in current complementary metal-oxide-semiconductor (CMOS) transistors, the active region of these quantum dot devices consists of a fin, varying in width between 20 and 70 nm, etched out of the silicon substrate [251]. Nested top-gates with a pitch of 50 nm, separated from the fin by a composite $SiO_2$/high-k dielectric, are used to form and manipulate quantum dots. Figure 7.1a shows a high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image of the active device area. A cross-section transmission electron microscopy (TEM) image along a fin with quantum dot gates is shown in Fig. 1b. Phosphorus ion implants on both ends of the fin, well separated from the active region, serve as ohmic contacts to the fins. We pattern two such linear quantum dot arrays, separated by 120-150 nm (see Fig. 7.1c for a TEM image across both fins). In our experiments, we use a quantum dot in one array as a charge sensor for the qubit dots in the other array. A 3D device schematic is shown in Fig. 7.1d.

The process flow starts from a conventional transistor flow but is adapted to fabricate two sets of gates in successive steps using a combination of 300 mm optical lithography, thin film deposition, plasma etch, and chemical mechanical polish processes. The main steps are illustrated in Fig. 1e. First, the fins are defined in a Si substrate. The space between the fins is filled in with a $SiO_2$ shallow trench isolation (STI) dielectric material and polished. Then, a composite $SiO_2$ and high-k dielectric layer is formed to isolate the gates from the substrate. The first gate layer (with even numbers) is defined using an industry standard replacement metal gate process [260–262] and consist of a workfunction metal with tungsten fill. Ohmic regions are formed by means of phosphorus n+ implantation at the end of both fins.

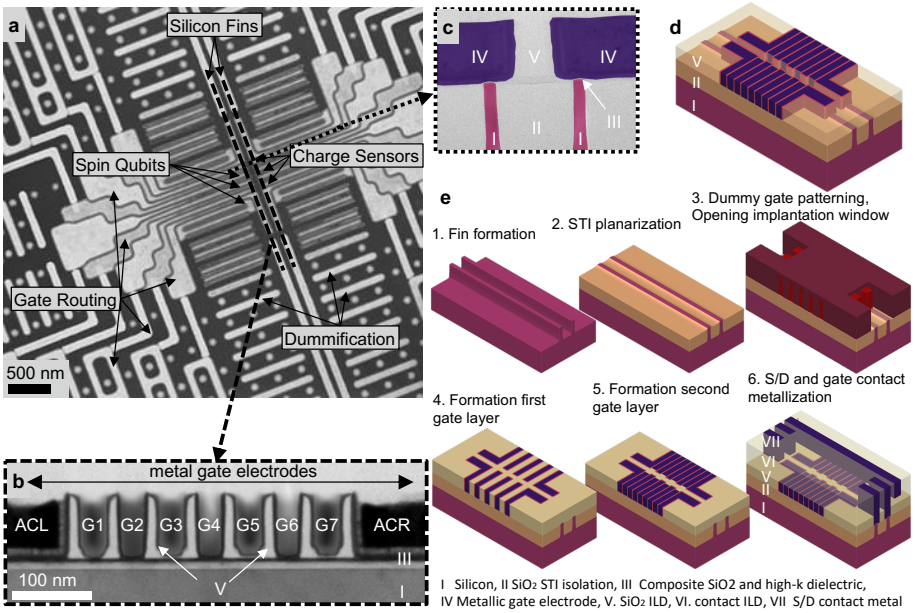


Figure 7.1.: **Industrially fabricated quantum dot devices. a,** HAADF-STEM image of a typical device. The active region consists of two parallel silicon fins; one hosts the qubits and the other hosts the sensing dot. The fan-out of the gates, is clearly visible, as are many additional metallic structures (called dummification) needed to maintain a roughly constant density of metal on the surface, which ensures homogeneous polishing on a wafer scale. **b,** TEM image along a Si fin, showing 7 metallic finger gates to define the quantum dot array and two accumulation gates to induce reservoirs connecting to the phosphorus n-type implants that serve as ohmic contacts (outside the image). The gates are isolated from the fin by a composite $SiO_2$ and high-k dielectric layer. In between the gates is a $SiO_2$ ILD for isolation. **c,** False-coloured TEM image perpendicular to the Si fins, showing the silicon fins and the $SiO_2$ STI fill in between the fins. **d,** Schematic of the active region of the device. **e,** Schematic of the process steps used to fabricate the devices: Si fin formation (1), STI planarization (2), poly silicon dummy gate patterning, n+ implants for S/D formation (3), ILD deposition for gate spacer formation, planarization, dummy gate removal, first gate layer formation (4), ILD etch to open window for second gate layer, second gate layer formation (5), ILD deposition, trench formation and metal fill for contacting gates and implants and ESR line formation (6).

The area between the gates of the first layer is filled with a $SiO_2$ inter-layer dielectric (ILD) and patterned to selectively remove the oxide in the qubit device region and allow for the second gate layer to be formed. The second gate layer (with odd numbers) is then formed adjacent to the first gate layer. Finally, a tungsten or copper contact layer is patterned to enable routing to bond pads, as well as ohmic and gate contacts. For the devices intended for coherent experiments (discussed in Fig. 7.4) alternate masking steps are run to integrate an electron-spin-resonance (ESR) line within the existing contact routing layer. The ESR line consists of a copper wire that shunts a coplanar stripline (connected to an on-chip coplanar waveguide [191]), placed parallel to the fins (Supplementary Fig. 7.5).

The samples used only for quantum dot formation are fabricated on natural silicon substrates, whereas the samples used for qubit readout and manipulation are fabricated on an isotopically enriched $^{28}$Si epilayer with a residual $^{29}$Si concentration of 800 ppm [94, 122]. This reduces the hyperfine interaction of the qubits with nuclear spins in the host material and thus increases qubit coherence [63].

A single 300 mm wafer contains 82 unit cells (die) with in total more than 10, 000 quantum dot arrays of various lengths, with up to 55 finger gates per fin. Figure 7.1b shows a TEM image of a typical device with seven finger gates on top of each fin.

## 7.3 HIGH-VOLUME DEVICE CHARACTERIZATION

To analyse device yield and sample uniformity, both within the wafer and across different wafers, automated probing at room temperature is used to measure one seven-gate device per die and determine the threshold voltage per gate. Devices are considered yielding if the channel in both fins turns on, all individual gates on both fins can switch off current flow through the respective channel and the ohmic contacts and gates are not leaking. Figure 7.2a shows a map that indicates the device yield of wafer 20, containing devices with an ESR line. The device yield is about 98%, with only two devices at the edge of the wafer not fully functioning. Supplementary Fig. 7.6 shows additional yield maps for four almost identical wafers without stripline (wafers 11, 12, 13 and 14) which differ from each other only by etching and polishing parameters, to illustrate how process parameters are targeted. Repeatedly, for optimized process parameters, we find only a few samples at the edge of the wafer to be not fully yielding.



Process uniformity is studied by comparing the room-temperature threshold voltage of individual gates. Figure 7.2b shows a histogram of the threshold voltage for the gates in the second gate layer of all devices over wafers 11-14, with a standard deviation in threshold voltage of 70 mV. The standard deviation in the first gate layer is higher, as we consistently find the samples at the edge of the wafers to have lower threshold voltages (Supplementary Fig. 7.10 and Supplementary Fig. 7.13 for the wafer with the ESR line). Further analysis of the threshold voltages (Supplementary Figs. 7.7 - 7.12) reveals that the variation in threshold voltage within a device is similar to that across a wafer and between wafers. Additionally, we find that the threshold voltage variation for the (wide) accumulation gates is smaller than that for the finger gates made in the same layer. These observations are consistent with known sources of variability in transistor manufacturing [217]. Unlike scaled transistors, our qubit devices are not optimized for short channel effects, and as we go from accumulation gates to gate layer 2 to gate layer 1 this reduction in short channel control causes the threshold voltage to have a very strong dependence on gate dimensions, which augments variability.

Next, we study the relation between threshold voltages measured at room temperature versus those measured at low temperature (5 K and below) for all gates. Figure 7.2c shows the data from wafers 11-14, and Supplementary Fig. 7.14a includes data for over 600 gates on 20 different wafers for which we took low-temperature data. Interestingly, the threshold voltage measured at room temperature shows a linear correlation with that measured at

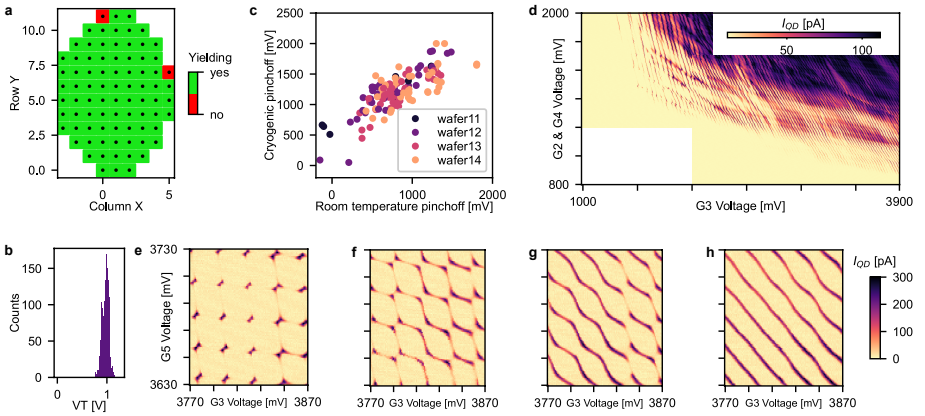


Figure 7.2.: **Tunable single and double quantum dots a,** Room temperature yield map for wafer 20, which contains devices with ESR striplines. Yield is defined in the main text. **b,** Histogram of room temperature threshold voltages for all gates of the second gate layer (G1, G3, G5, G7) from yielding devices of wafers 11-14 (2288 gates from 286 devices in total). The standard deviation of all these gates across the four wafers is 70 mV. **c,** Correlation map for threshold voltages at room-temperature and low-temperature for all gates from all samples from wafers 11-14 which have been cooled down. **d,** Charge stability diagram for a single QD measured via electron transport. **e-h,** Charge stability diagrams of a double quantum dot formed under gates G3 and G5. The gate voltage on G4 is gradually increased (G4 is 1245, 1308, 1353 and 1398 mV from **e** to **h**), showing good control over the interdot tunnel coupling.



low temperature. Due to different processing parameters for the different wafers, both the slope as well as the offset of the linear correlation can shift slightly. When examining the low-temperature threshold voltages, we again find that the spread in gate layer 1 is larger than the spread in gate layer 2, see Supplementary Fig. 7.15.

From the 79 samples that we cooled down across 20 wafers, four samples were not working due to human errors in wire bonding. Out of the other 75 samples, we find only 21 out of the 1050 gates not working, indicating that room temperature measurements can be used to preselect samples to cool down for quantum dot analysis. Published data rarely present device-yield analysis like we are presenting here [72]. However, it is our experience that with conventional electron beam lithography and lift-off processing, only a small percentage of the devices with similar complexity functions fully.

## 7.4 QUANTUM DOT MEASUREMENTS

All quantum dot and qubit measurements are carried out in a dilution refrigerator, operated at base temperature. The measurements have been performed on a plethora of different devices from different process flow generations, measured in three different dilution refrigerators in different laboratories.

We form quantum dots by tuning the gates individually to define a suitable potential landscape (dots can be controllably formed below any of the inner 5 gates). Figure 7.2d shows a typical result, where we measure the current through a QD while sweeping three gate voltages (labeled in Fig. 7.1b), one of which (G3) mostly controls the electrochemical

potential of the quantum dot and the others (G2 and G4) mostly control the tunnel barriers. In the range $1\text{V} < V_{G3} < 3.9\text{V}$, we count more than 80 lines, known as Coulomb peaks, separating regions with a stable number of electrons on the QD. As the voltage on G3 is made more negative, exactly one electron is removed from the QD after crossing each Coulomb peak. While the Coulomb peaks are parallel and evenly spaced at a high G3 voltage ($> 3$ V), they become irregular and also further separated towards the few-electron regime (around 1.5 V on G3). Such irregular behaviour is characteristic of Si-MOS devices, due to their close proximity to the dielectric interface [49, 95, 118, 123, 125, 242, 253, 256]. More importantly, measured samples from anywhere across wafers 11-14, consistently show regular Coulomb oscillations in the many-electron regime (see Supplementary Figs. 7.16-7.20), and allowed to reach a similarly-looking few-electron regime whenever we tried.

Analysing these first-generation dots through so-called Coulomb diamonds [36], gives an average charging energy of $8.9 \pm 0.2$ meV (all error bars are $1\sigma$ from the mean) per dot in the multi-electron regime (see Supplementary Fig. 7.21). Charge noise measurements in the multi-electron regime give a power spectral density with approximately a $1/f$ slope and a charge noise amplitude in the range of $1 - 10$ $\mu\text{eV}/\sqrt{\text{Hz}}$ at 1 Hz (Supplementary Fig. 7.22). These are common charge noise values in Si-MOS QD samples [118]. The variations between the data points are not unexpected, as different gate voltages typically activate different charge fluctuators in the stack.

Figure 7.2e shows the transport through a double QD as a function of the gate voltages that (mostly) control the electrochemical potential of each dot, G3 and G5. Characteristic points of conductance are measured, so-called triple points. At these points, the electrochemical potentials of the reservoirs are aligned with the electrochemical potentials of the left and the right dot, such that electrons can tunnel sequentially through the two dots [62]. Increasing the voltage applied to the intermediate gate G4 is expected to lower the tunnel barrier between the dots, eventually reaching the point where one large dot is formed. This behaviour is seen in Figs. 7.2e-h, as the gradual transition from triple points to single, parallel and evenly spaced Coulomb peaks. This shows the tunability of the interdot tunnel coupling in this double dot, which is advantageous for two-qubit control in such a system [51, 106, 123, 198].

In a next step, we use a QD in one fin as a charge sensor for the charge occupation of the QDs in the other fin. This allows us to unambiguously map the charge states of the qubit dots down to the last electron [36]. A characteristic charge stability diagram showing the last electron transition is shown in Fig. 7.3a. The current through the sensor is measured as a function of the voltage on two gates controlling the qubit dot. In the few-electron regime, we can usually distinguish lines with several different slopes, indicating the formation of additional, spurious dots next to the intended dot. However, we consistently are able to find a clean region in the charge stability diagram with an isolated addition line corresponding to the last electron. In this regime, we observe a 500 pA difference in the sensing dot current between the occupied and unoccupied quantum dot states for a source-drain voltage of 500 $\mu$V.

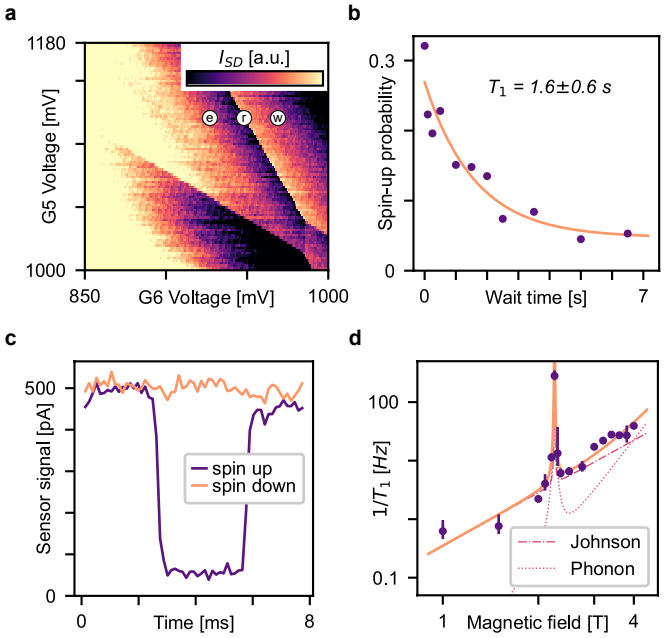


Figure 7.3.: **Charge sensing and single-shot spin readout. a,** Charge stability diagram of the last-electron regime of a QD, measured with a sensing dot in the other fin. The points w, r and e refer to the wait, readout and empty stages of the gate voltage pulse. **b,** Spin-up probability as a function of load time at a magnetic field of 1 T. The exponential fit yields a $T_1$ of 1.6 $\pm$ 0.6 s. **c,** Real-time current through the sensing dot indicating a spin-up (purple line) and spin-down (orange line) electron, recorded with a measurement bandwidth of 3 kHz set by an external low-pass filter. **d,** Relaxation rate ($1/T_1$) as a function of the applied magnetic field (purple dots). The relaxation rate is fitted by a model (orange line) that includes the effect of Johnson noise and phonons coupling to the spin via spin-orbit interaction. From this fit, we extract a valley splitting of $E_v = 260 \pm 2$ $\mu$eV.

## 7.5 INDUSTRIALLY-MANUFACTURED QUBITS

In order to define a qubit via the electron spin states, we apply a magnetic field in the [100]-direction, parallel to the fins, separating the spin-up and spin-down levels in energy. We perform single-shot readout of the spin of a single electron by means of spin-dependent tunnelling and real-time charge detection (Fig. 7.3c). Here and below, we did not optimize the state preparation and measurement conditions. We measure the spin relaxation time, $T_1$ using a three-stage pulse to gate G6 [75] and find $T_1$ exceeding 1 s at a magnetic field of 1 Tesla (Fig. 7.3b). This $T_1$ is among the longest relaxation times reported previously for silicon quantum dots [70, 117, 118, 123] and indicates that the advanced semiconductor processing conditions do not degrade the spin relaxation time. Upon measuring $T_1$ as a function of magnetic field, we find a striking, non-monotonic dependence, which is well described in the literature and the result of the valley structure in the conduction band of silicon. Following [117, 118], we fit the magnetic field dependence of the spin relaxation rate ($1/T_1$) with a model including the effect of Johnson noise and phonons inducing spin transitions mediated

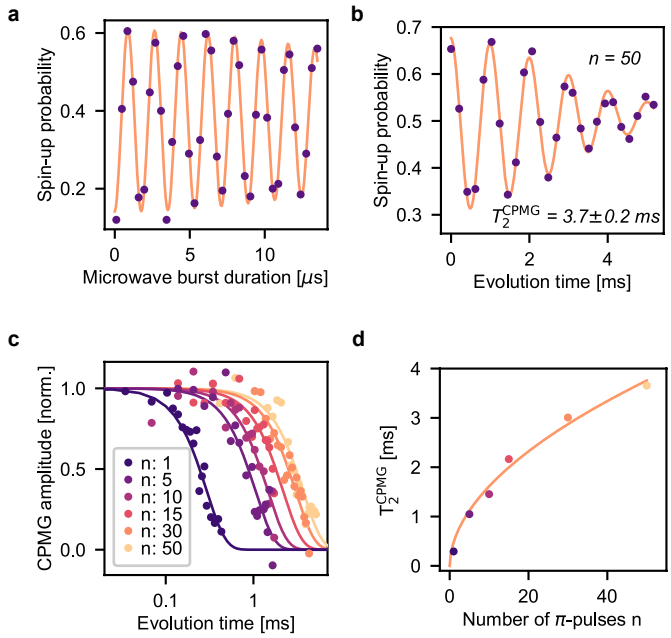


Figure 7.4.: **An industrial silicon spin qubit a,** Rabi oscillations of the measured spin-up probability as a function of microwave burst duration. **b,** CPMG experiment, the measured spin-up probability as a function of the free evolution time separating 50 $\pi$ pulses, with an artificial phase detuning on the last pulse. The data is fitted with $A(\cos(\omega t + \phi) + B)\exp(-(t/T_2^{CPMG})^2) + C$. The fitted CPMG coherence time $T_2^{CPMG}$ is 3.7±0.2 ms. **c,** Demodulated and normalized CPMG amplitude as a function of the total evolution time for different numbers $n$ of $\pi$-pulses. **d,** Measured coherence time $T_2^{CPMG}$ for different numbers of CPMG $\pi$ pulses. The orange line represents a fit through the data (excluding $n = 1$) following $T_2^{CPMG} \propto n^{(\gamma/(\gamma+1))}$. We extract $\gamma = 1.1 \pm 0.2$.

by spin-orbit coupling, and taking into account the lowest four valley states (Fig. 7.3d). The peak in the relaxation rate around 2.25 T corresponds to the situation where the Zeeman energy equals the valley splitting energy, from which we extract a valley splitting of 260 $\pm$ 2 $\mu$eV, well above the thermal energy and qubit splitting in this system.

To coherently control the spin states, we apply an ac current to the stripline in order to generate an oscillating magnetic field at the QD [78]. Electron spin resonance occurs when the driving frequency matches the spin Larmor frequency of $f = 17.1$ GHz, which is set by the static magnetic field at the dot. By selectively pulsing only the spin-down level below the Fermi reservoir, we load the QD with a spin-down electron. We then pulse deep in the Coulomb blockade regime to manipulate the spin with microwave bursts. Finally, we pulse to the readout point. The spin-up probability as a function of microwave burst duration shows clear Rabi oscillations (Fig. 7.4a). We have studied coherent control in three different qubits (this comparably small number does not reflect a decrease in device yield from electrically functional devices to operational qubits, see Experimental methods section). The main figures show data for qubit 1 (Q1) and Supplementary Figs. 7.29- 7.31 show data for qubit 2 (Q2),

formed on the same device (Supplementary Fig. 7.23), and for qubit 3. As expected, the Rabi frequency is linear in the driving amplitude, reaching up to about 900 kHz for Q2.

The spin dephasing time $T_2^*$ is measured through a Ramsey interference measurement (see Supplementary Fig. 7.26). Fitting this Ramsey pattern with a Gaussian-damped oscillation, yields a decay time of $T_2^* = 24 \pm 6\ \mu s$ when averaging data over 100 s (the error bar here refers to the statistical variation between 41 post-selected repetitions of 100 s segments). As we repeat such Ramsey measurements, we observe slow jumps in the qubit frequency. Averaging the free induction decay over 2 hours and 40 minutes still gives a $T_2^*$ of $11 \pm 2\ \mu s$, see Experimental methods section for more details.

To analyse the single-qubit gate fidelity, we employ randomized benchmarking [263] (Supplementary Fig. 7.28). A number, $m$, of random Clifford gates is applied to the qubit, followed by a gate that ideally returns the spin to either the spin-up or spin-down state. In reality, the probability to reach the target state decays with $m$ due to imperfections. The standard analysis gives a single-qubit gate fidelity of 99.0% for Q1 and 99.1% for Q2. With the Rabi decay being dominated by low-frequency noise, the present combination of $T_2^*$ and Rabi frequency should allow an even higher fidelity [95, 123, 124]. We suspect the single-qubit gate fidelity to be limited by improper calibration.

Finally, we study the limits of spin coherence by performing dynamical decoupling by means of Carr-Purcell-Meiboom-Gill (CPMG) sequences (see Fig. 7.4b for the coherence decay using 50 pulses). These sequences eliminate the effect from quasi-static noise sources. Figure 7.4c shows the normalized amplitude of the CPMG decay as a function of evolution time for different numbers of $\pi$-pulses, $n$. By fitting these curves we extract $T_2^{\mathrm{CPMG}}(n)$. We use a Gaussian decay envelope which yields distinctly better agreement than an exponential decay. The $T_2^{\mathrm{CPMG}}$ times are plotted as a function of $n$ in Fig. 7.4d. We obtain a $T_2^{\mathrm{CPMG}}$ of over 3.5 ms for $n = 50$ CPMG pulses, more than 100 times larger than $T_2^*$, with room for further increases through additional decoupling pulses. The CPMG data for Q1 is consistent with charge noise as the limiting mechanism (see Experimental methods section). For Q2, an additional noise mechanism is likely present.



## 7.6 CONCLUSION

In summary, we have shown that samples fabricated using industrial processing conditions show exceptionally good quantum dot yield, along with key performance indicators such as charge noise, the charge sensing signal, $T_1$, $T_2^*$ and $T_2^{\mathrm{CPMG}}$, that are already comparable to commonly observed values (see Supplementary Table 1). The formation of easily tunable double dots bodes well for the implementation of two-qubit gates in this system. Several further improvements are possible. First, the current ESR stripline has a finite resistance of the order of 50 $\Omega$, which causes device heating. This effect can be minimized by making the ESR wire wider and using lower resistivity materials. Finally, spurious dots in the few electron regime and two-level systems can be removed by reducing the presence of material charge defects [264, 265]. While growth conditions for high-quality Si/dielectric interfaces have been identified, we have indications that performance-limiting defects are

formed through downstream processing. Further work is ongoing to optimize the process flow and recipes (temperature budget, plasma conditions, chemical exposure, and annealing conditions) to reduce defects at the end of line. Although there are significant challenges to overcome in order to engineer out these defects and improve qubit performance and scalability, the full 300mm device-integration line we have established will allow us to run a high volume of experiments to accelerate this development over what could be achieved by conventional fabrication methods.

These advanced manufacturing methods can be adapted to allow for 2D quantum dot arrays as well. Moreover, these processing steps are by default integratable with any other CMOS technology, which opens up the potential to integrate classical circuits next to the qubit chip. Eventually, industrial processing has the potential to achieve the very high quantum dot uniformity that would enable cross-bar addressing schemes [55]. The compatibility of silicon spin qubits with fully-industrial processing demonstrated here, highlights their potential for scaling and for realising a fault-tolerant full-stack quantum computer.

## 7.7 EXPERIMENTAL METHODS

**Setup and instrumentation**

The measurements were performed on two different setups, setup 1 (S1, Delft) and setup 2 (S2, Hillsboro). The samples were cooled down in a dilution refrigerator, operated at the base temperature of around 10 mK (S1: Oxford Triton dry dilution refrigerator, S2: Bluefors XLD dry dilution refrigerator). DC voltages were applied via Delft in-house built, battery-powered voltage sources (S1 and S2). The printed circuit board onto which the sample was mounted contained bias tees with a cut-off frequency of 3 Hz to allow for the application of gate voltage pulses (S1 and S2). The pulses were generated by an arbitrary waveform generator (AWG, S1: Tektronix AWG5014, S2: Zurich Instruments HDAWG). The baseband current through the sensing dot was converted to a voltage by means of a home-built amplifier, filtered through a room-temperature low-pass filter (S1: 3 kHz, S2: 1.5 kHz) and sampled by a digitizer (S1: M4i spectrum, S2: Zurich Instruments MFLI). Microwave bursts for driving ESR were generated by a vector source with an internal IQ mixer (S1 and S2: Keysight PSG8267D), with the I and Q channels controlled by two output channels of the AWG.

**Charge noise measurements**

Each charge noise data point in Supplementary Fig. 7.22 is obtained by recording a 140 second time trace (at 28 Hz sampling rate) of the current through the QD with the plunger gate voltage fixed at the steepest point of the Coulomb peak flank. To convert the current signal to energy, we first convert the current to gate voltage by multiplying the data by the slope of the Coulomb peak at the operating point. Then, we multiply with the lever arm to convert from plunger gate voltage to energy. To obtain the power spectral density (PSD), we divide the data in 10 equally long segments, take the single-sided fast Fourier transform of the segments and average these. Fitting the PSD to $A/f^{\alpha}$ we extract the energy fluctuations

at 1 Hz ($\sqrt{A}$) for each Coulomb peak. We extract a mean value of $\alpha = 1.1 \pm 0.3$.

**Spin readout**

In order to read out the spin eigenstate we use energy-selective tunnelling to the electron reservoir [75]. The spin levels are aligned with respect to the Fermi reservoir, such that a spin-up electron can tunnel out of the QD, while for a spin-down electron it is energetically forbidden to leave the QD. Thus, depending on the spin state, the charge occupation in the QD will change. To monitor the charge state, we apply a fixed voltage bias across the sensing dot and measure the baseband current signal through the sensing dot, filtered with a low-pass filter and sampled via the digitizer. In post-analysis we threshold the sensing dot signal and accordingly assign a spin-up or spin-down to every single shot experiment. After readout, we empty the QD to repeat the sequence. As is commonly seen in spin-dependent tunnelling, the readout errors are not symmetric, which is reflected in the range of the oscillations in Figs. 7.4a,b.

**Qubit operations**

When addressing the qubit, we phenomenologically observe that the qubit resonance frequency shifts depending on the burst duration. The precise origin of this resonance shift is so-far unclear, but appears to be caused by heating. Similar observations have been made in recent spin qubit experiments [50, 104, 105] that used electric-dipole spin resonance via micromagnets as the driving mechanism. To ensure a reproducible qubit frequency in the experiments, we apply an off-resonant microwave burst prior to the intended manipulation phase to saturate this frequency shift. We further investigate this frequency shift in Supplementary Figs. 7.24 and 7.25.



**Ramsey oscillation**

We observe that the qubit resonance frequency in the devices exhibits jumps of several 100 s of kHz on a timescale of 5-10 minutes. To extract meaningful results, we monitor this frequency shift throughout the experiments and accordingly discard certain data traces, such that we only take into account data acquired with the qubit in a narrow frequency window. To illustrate the frequency shift, we show the FFT of 100 repetitions of a Ramsey interference measurement of qubit 1 (measurement time $\sim$ 2 hours 40 min) in Supplementary Fig. 7.26a, which tracks the qubit frequency over time. In order to estimate the $T_2^*$ of qubit 1, we fit each of the 100 repetitions of the Ramsey measurement (measurement time per repetition $\sim$ 100 s) and extract a $T_2^*$ value. Evidently, some of the data quality is rather poor due to the previously described frequency jumps in which case the extracted $T_2^*$ value is meaningless. We calculate the mean square error of each fit and disregard all the measurements with a high error. The average $T_2^*$ of the 41 remaining traces is $24 \pm 6$ $\mu$s (Supplementary Fig. 7.26b). Averaging the data traces of all 41 traces and then fitting a decay curve yields a dephasing time of $16 \pm 2$ $\mu$s (Supplementary Fig. 7.26c); averaging the data of all 100 traces still gives a dephasing time of $11 \pm 2$ $\mu$s (Supplementary Fig. 7.26d).

**CPMG coherence measurements and power spectral density**

To ensure robust fitting, the CPMG sequences are applied with a phase detuning on the last pulse. We fit the resulting curves with a Gaussian damped cosine function: $A(\cos(\omega t+\phi)+B)\exp[-(t/T_2^{\mathrm{CPMG}})^2]+C$. If, instead of using a Gaussian decay, we leave the exponent of the decay open as a fitting parameter, we obtain values for the exponent between 2.3 and 2.6, but the use of the additional parameter results in less robust fits. The offset $B$ is included to compensate for the loss of readout visibility for long microwave burst duration. We attribute this to heating generated while driving the spin rotations. The measurement is divided into segments, each consisting of 200 single shots. Each segment includes a simple calibration part, based on which we post-select repetitions for which the spin-up probability after applying a $\pi$-pulse is above 25 percent. In this way, we can exclude repetitions where the qubit resonance frequency has shifted drastically. The remaining repetitions are averaged to obtain the characteristic decay curves for each choice of $n$, one of which is shown in Fig. 7.4b. From fitting the decay curves, we extract the $T_2^{\mathrm{CPMG}}$ times as a function of $n$, shown in Fig. 7.4d. To extract the CPMG amplitude as a function of evolution time from the data, we demodulate the measured values with the parameters extracted from the fit, according to $A_{\mathrm{CPMG}}=(x-C)/(A(\cos(\omega t+\phi)+B))$, with $x$ the measured data. Due to experimental noise, points where the denominator is small, do not yield meaningful results. Hence, we exclude data points for which the absolute value of the expected denominator is smaller than 0.4. The extracted CPMG amplitudes are plotted in Fig. 7.4c. In a commonly used simplified framework [201, 266], we can relate the data of Fig. 7.4d to a noise power spectral density of the form $S(\omega)\propto 1/\omega^{\gamma}$. Specifically, fitting the data to $T_2^{CPMG}(n)\propto n^{\gamma/(\gamma+1)}$ gives $\gamma=1.1\pm0.2$. Alternatively, we can estimate $\gamma$ by fitting the noise power spectral density extracted from the individual data points in the CPMG decays [266] in Supplementary Fig. 7.27(a). This analysis gives $\gamma=1.2\pm0.1$. Either way, the extracted power spectral density is close to the $1/f$ dependence that is characteristic of charge noise. Charge noise can affect spin coherence since the spin resonance frequency is sensitive to the gate voltage, as also reported before for Si-MOS based spin qubits [49]. We next estimate how large charge noise would need to be in order to dominate spin decoherence. To do so, we extrapolate the extracted spectral density in the range between $10^3$ and $10^4$ Hz to an amplitude at 1 Hz, which after conversion to units of charge noise gives $29\pm27$ $\mu$eV/$\sqrt{\mathrm{Hz}}$. With the caveat that this extrapolation is not very precise, we note that this value is only slightly larger than the charge noise amplitude in the multi-electron regime of $2-10$ $\mu$eV/$\sqrt{\mathrm{Hz}}$. Considering that charge noise values are typically higher in the few-electron regime, this suggests that coherence of Q1 may be limited by charge noise [266]. For Q2, which is another qubit in the same sample, the same procedure gives an extrapolated noise at 1 Hz that is an order of magnitude larger. Possibly a two-level fluctuator is active in the vicinity of this qubit in the regime where the qubit data was taken.

**Downselection of qubit samples**

To select devices for coherent measurements, we use an automated probe station for RT tests of quantum dot arrays on wafer 20. Across the 82 die on the wafer, we test turn-on for

both fins of a single device and find that 80/82 samples (162/164 fins) conduct. Furthermore, each of the gates G1 through G7 for these 160 fins is able to control the current. The device yield as far as can be established by room-temperature testing is thus 98%. From this wafer, we selected 7 samples for low-temperature testing, for which the threshold voltages looked clean and the spread in threshold voltages was below 125 mV. For those 7 samples, 13 of the 14 fins conducted at low temperature. The failure mode of the other one is not known. The gate response was hysteretic for one of seven gates on one of the 13 fins, and was fine for the other gates on this fin and all gates on the other fins. With all six samples, we reached the single-electron regime. With three samples, we had confirmed technical issues outside the sample (filter board limitations and human errors) and with a fourth sample, we had a suspected issue with the transmission line outside the sample. These issues could most likely have been resolved but we didn't pursue that since meanwhile, on two other of the 6 samples, we had taken qubit data, realizing 3 different qubits. Evidently, the room-temperature automated prober allows high-volume characterization. By comparison, sequential cooldowns of individual samples to cryogenic temperatures and the subsequent experiments for qubit control and measurement, are much more time-consuming, hence the much lower number of samples for which we characterized qubit performance.

## 7.8 SUPPLEMENTARY FIGURES



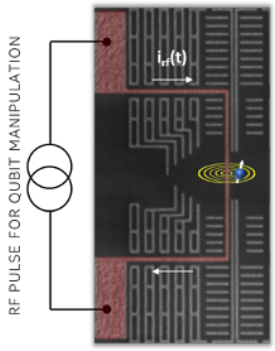


Figure 7.5.: **Sample with ESR line.** A scanning electron microscope image of a sample with an ESR line, nominally identical to the samples measured in this chapter. The ESR line is false-coloured in red. The active area of the sample is indicated by the cartoon of a spin. Metal dummification is clearly visible in the image, the quantum dot gates are not visible as they are covered by dielectric.

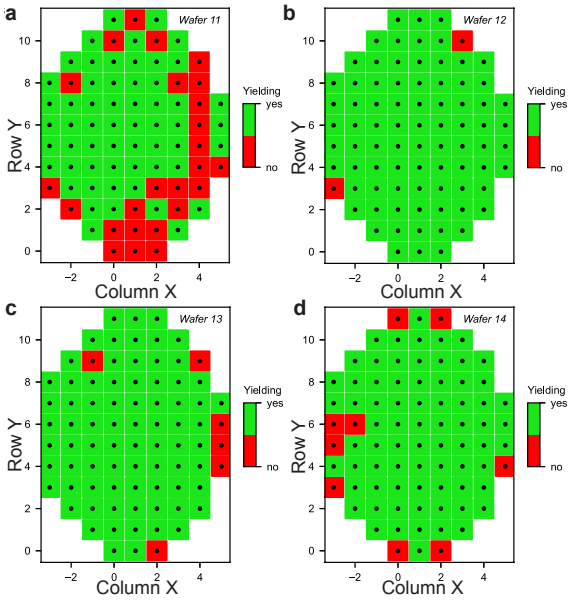


Figure 7.6.: **Yield maps for wafers 11-14.** Each 300-mm wafer consists of 82 die and each die contains quantum dot arrays with various design skews and array sizes (up to 55 gates), as well as transistor and calibration test structures. To analyse cross-wafer sample yield, automated probing at room temperature is used to measure one seven-gate device per die (nominally identical to the devices discussed in the main text). For each device, the turn on voltage (when biasing all gates with the same voltage) and the threshold voltage for each of the seven gates (sweeping down one gate voltage at a time while keeping the other gate voltages above the turn-on voltage) on both fins are analysed. Moreover, the workings of the ion-implanted ohmic contacts are tested. If the device shows turn on, pinch-off for each gate and the ohmic contacts work, the device is labeled 'functioning' (green). In any other case, the device is labeled non-functioning and discarded (red). In total, we studied 20 wafers. All wafers were fabricated with different process parameters. Out of the 20 wafers, the production process of wafers **a,** 11, **b,** 12, **c,** 13 and **d,** 14 was almost identical, apart from the modification of some etching and polishing steps per wafer for process optimization. For wafer 11, the polishing was pushed outside the optimal process window, resulting in a lower yield. For all four wafers, the non-yielding devices are found around the edge of the wafer.

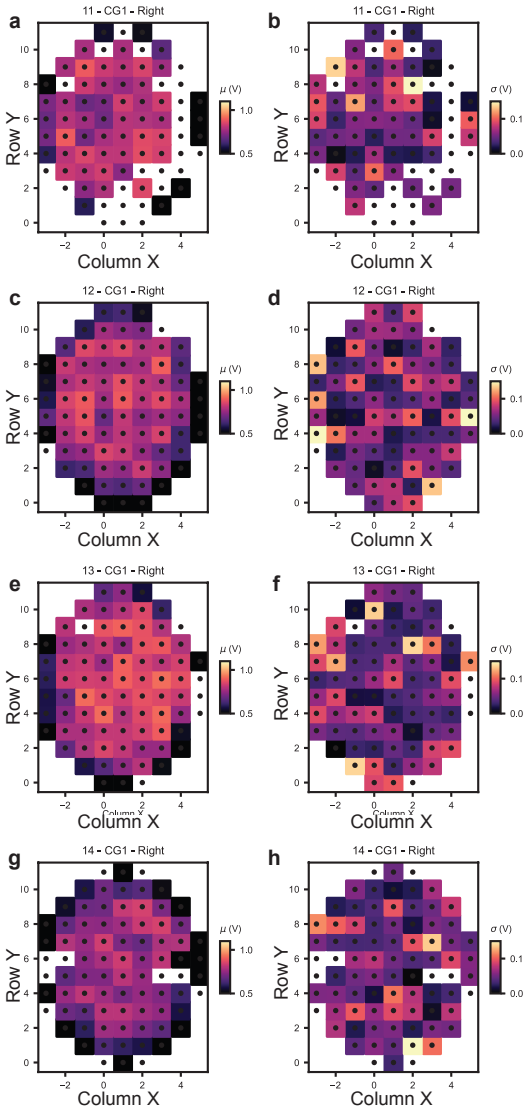


Figure 7.7.: **Cross-wafer variation of threshold voltages of the first gate layer at room temperature.** For each yielding device on the almost identical wafers 11, 12, 13 and 14, the threshold voltage for the seven gates on both fins is analysed. Each device has two gate layers. Gate layer 1 contains gates G2, G4 and G6 and gate layer 2 contains gates G1, G3, G5 and G7. **a, c, e, g,** Mean threshold voltage per device of the three gates of the first gate layer (even-numbered) for the yielding devices on wafer 11 (**a**), 12 (**c**), 13 (**e**) and 14 (**g**). The samples at the edge of the wafer consistently have a lower threshold voltage than the samples at the center of the wafer. **b, d, f, h,** Standard deviation of the threshold voltages per device of the first gate layer for the yielding devices on wafer 11, 12, 13 and 14. Apart from a few outliers, the standard deviation of the threshold voltage per sample is always below 140 mV.

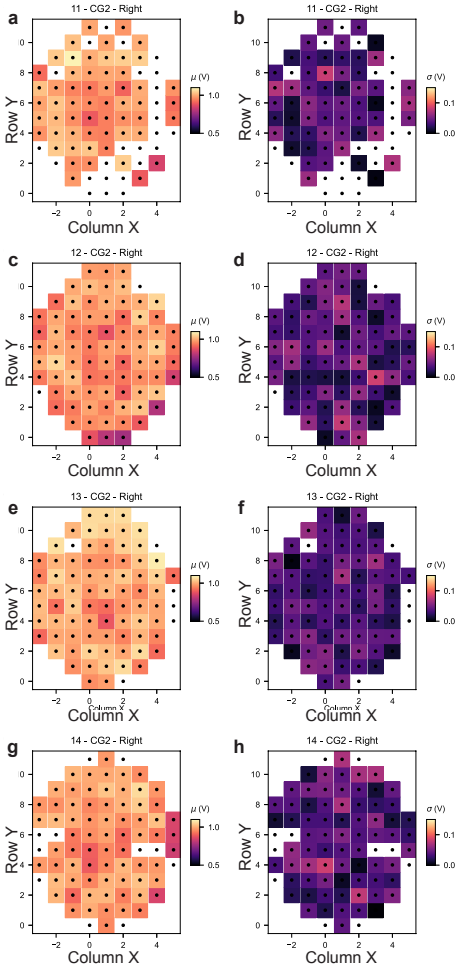


Figure 7.8.: **Cross-wafer variation of threshold voltages of the second gate layer at room temperature.** For each yielding device on the almost identical wafers 11, 12, 13 and 14, the threshold voltage for the seven gates on both fins is analysed. Each device has two gate layers. Gate layer 1 contains gates G2, G4 and G6 and gate layer 2 contains gates G1, G3, G5 and G7. **a, c, e, g,** Mean threshold voltage per device of the four gates of the second gate layer (odd-numbered) for the yielding devices on wafer 11 (**a**), 12 (**c**), 13 (**e**) and 14 (**g**). **b, d, f, h,** Standard deviation of the threshold voltages per device of the second gate layer for the yielding devices on wafer 11, 12, 13 and 14. Apart from a few outliers, the standard deviation of the threshold voltage per sample is always below 70 mV.

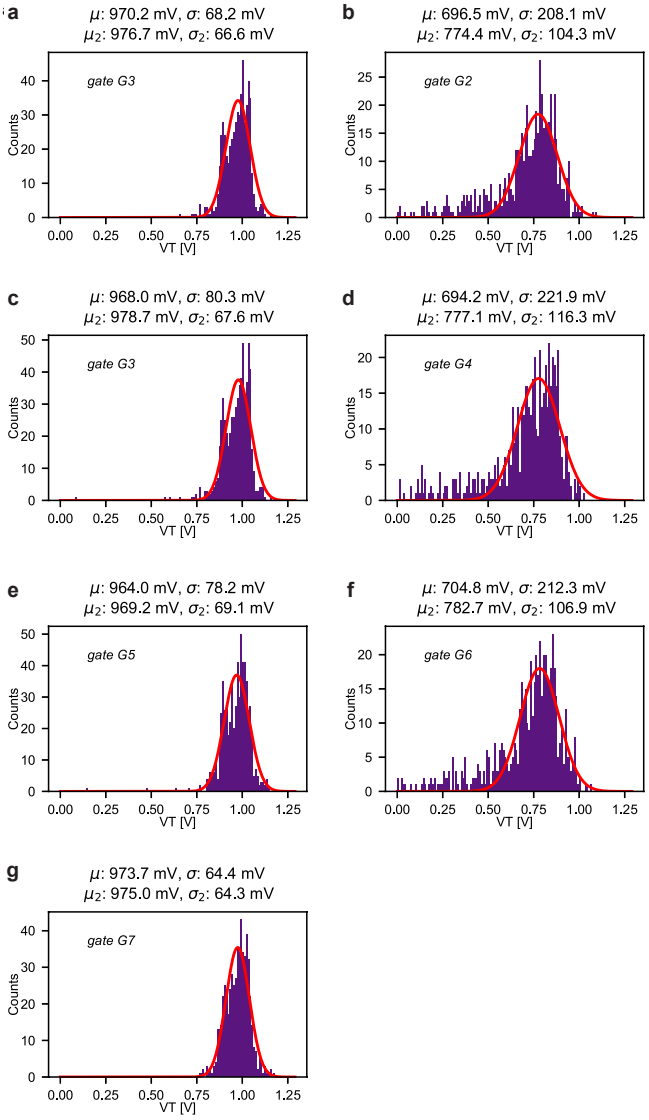


Figure 7.9.: **Histograms of threshold voltage per gate at room temperature.** Histograms for the threshold voltage per gate (G1-G7) for all yielding samples on wafers 11-14. We see that the gates on gate layer 1, G2 (**b**), G4 (**d**) and G6 (**f**) have a wider spread in threshold voltage than the gates from gate layer 2 G1 (**a**), G3 (**c**), G5 (**e**) and G7 (**g**). This is mainly caused by the fact that the samples around the edges of the wafers consistently show significantly lower threshold voltages for the first gate layer than samples in the center of the wafer (see Supplementary Fig. 7.7). When we analyse each gate separately, we observe that the mean value and the standard deviation for all three gates in gate layer one is of similar order per gate, as are the mean and standard deviation for the four gates of gate layer 2. In addition to the mean and standard deviation of the individual threshold voltages, we provide above each panel in the second line the mean and the standard deviation of a Gaussian distribution fitted to the data (red line).

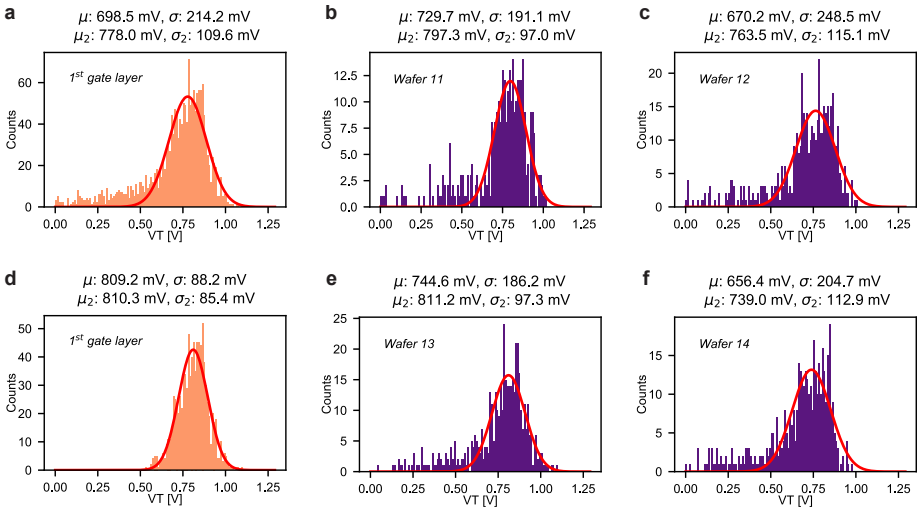


Figure 7.10.: **Histograms of threshold voltage per wafer for the first gate layer at room temperature. a,** Histograms for the threshold voltage for all gates of the first gate layer of both fins for all yielding samples of wafers 11, 12, 13 and 14. **b, c, e, f** Histograms for the threshold voltage for all gates of the first gate layer of both fins for all yielding samples of wafer 11 (**b**), 12 (**c**), 13 (**e,**) and 14 (**f**). **d,** Histograms for the threshold voltage for all gates of the first gate layer of both fins for all yielding samples of wafers 11, 12, 13 and 14, while not taking into account the samples at the edge. We see that when only taking into account the samples at the center of the four wafers, the standard deviation approaches that for the second gate layer (Supplementary Fig 7.11), where this edge-effect is not apparent. The average threshold voltage is a bit lower for the first gate layer than for the second gate layer. This can be explained by the extra oxide layer between the second gate layer and the sample. In addition to the mean and standard deviation determined by the individual threshold voltages, we provide above each panel in the second line the mean and the standard deviation of a Gaussian distribution fitted to the data (red line).

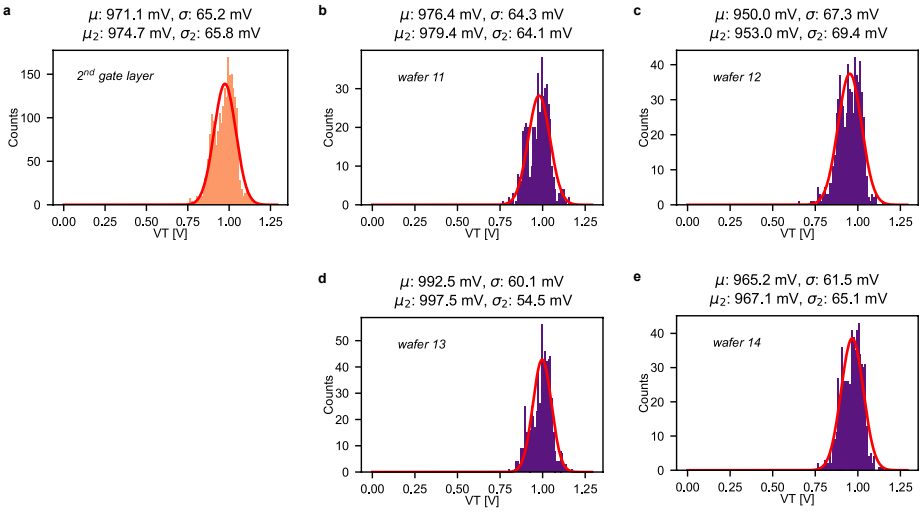


Figure 7.11.: **Histograms of threshold voltage per wafer for the second gate layer at room temperature. a,** Histograms for the threshold voltage for all gates of the second gate layer of both fins for all yielding samples of wafers 11, 12, 13 and 14. **b, c, d, e** Histograms for the threshold voltage for all gates of the second gate layer of both fins for all yielding samples of wafer 11 (**b**), 12 (**c**), 13 (**d**) and 14 (**e**). In addition to the mean and standard deviation of the individual threshold voltages, we provide above each panel in the second line the mean and the standard deviation of a Gaussian distribution fitted to the data (red line).

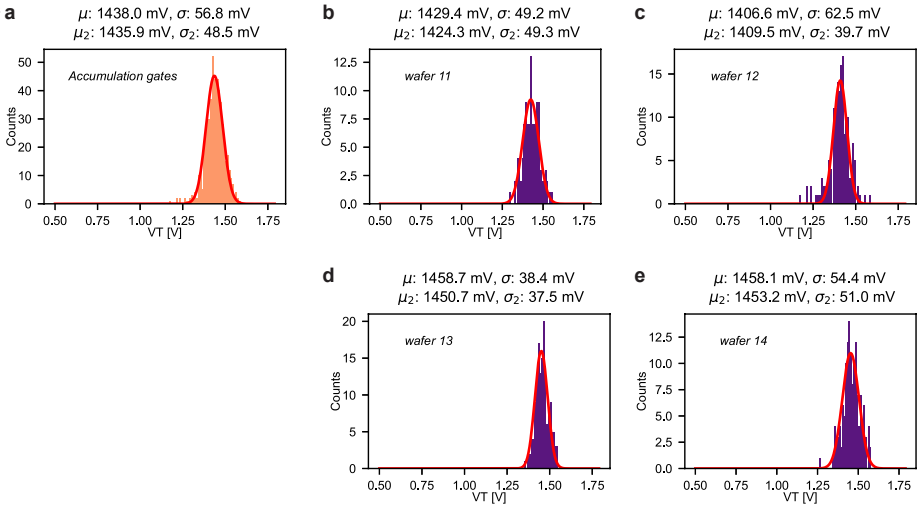


Figure 7.12.: **Histograms of threshold voltage per wafer for the accumulation gates at room temperature. a,** Histograms for the threshold voltage for all accumulation gates of both fins for all yielding samples of wafers 11, 12, 13 and 14. **b, c, d, e,** Histograms for the threshold voltage for all accumulation gates of both fins for all yielding samples of wafer 11 (**b**), 12 (**c**), 13 (**d**) and 14 (**e**). The standard deviation of the accumulation gates per wafer is significantly smaller than the standard deviation of gate layer 1, the gate layer in which also the accumulation gates are fabricated. We expect this to be caused by the larger size of the accumulation gates compared to the finger gates in gate layer 1. The spread in threshold voltages for the accumulation gates is also smaller than the spread in threshold voltages of gate layer 2. In addition to the mean and standard deviation of the individual threshold voltages, we provide above each panel in the second line the mean and the standard deviation of a Gaussian distribution fitted to the data (red line).

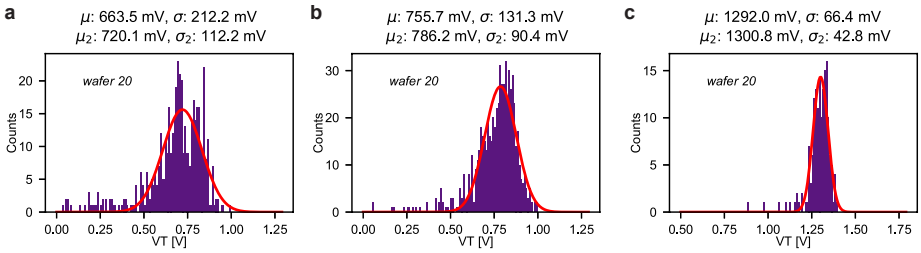


Figure 7.13.: **Histograms of threshold voltage for the gates of wafer 20 at room temperature. a, b, c** Histograms for the threshold voltage for all gates of both fins for all yielding samples of gate layer 1 (**a**), gate layer 2 (**b**) and the accumulation gates (**c**) of wafer 20, the wafer containing the samples with the stripline.

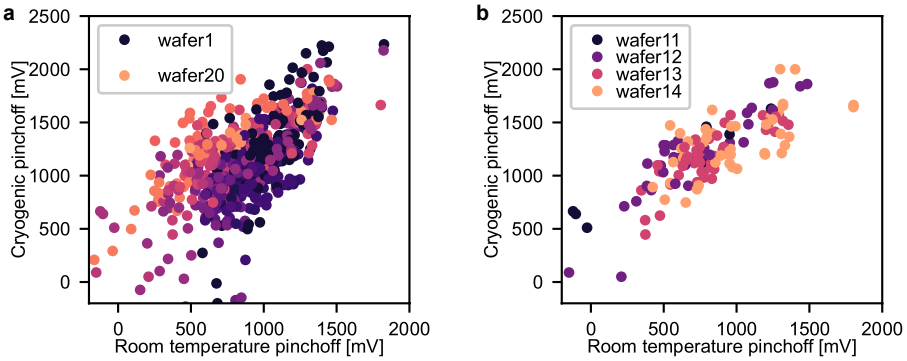


Figure 7.14.: **Correlations of threshold voltages between room temperature and low temperature.** For each gate, we plot the threshold voltage at room temperature versus the threshold voltage at low temperature, **a** for 20 different wafers at different stages of the development and optimization of the process flow and **b** for wafers 11-14.

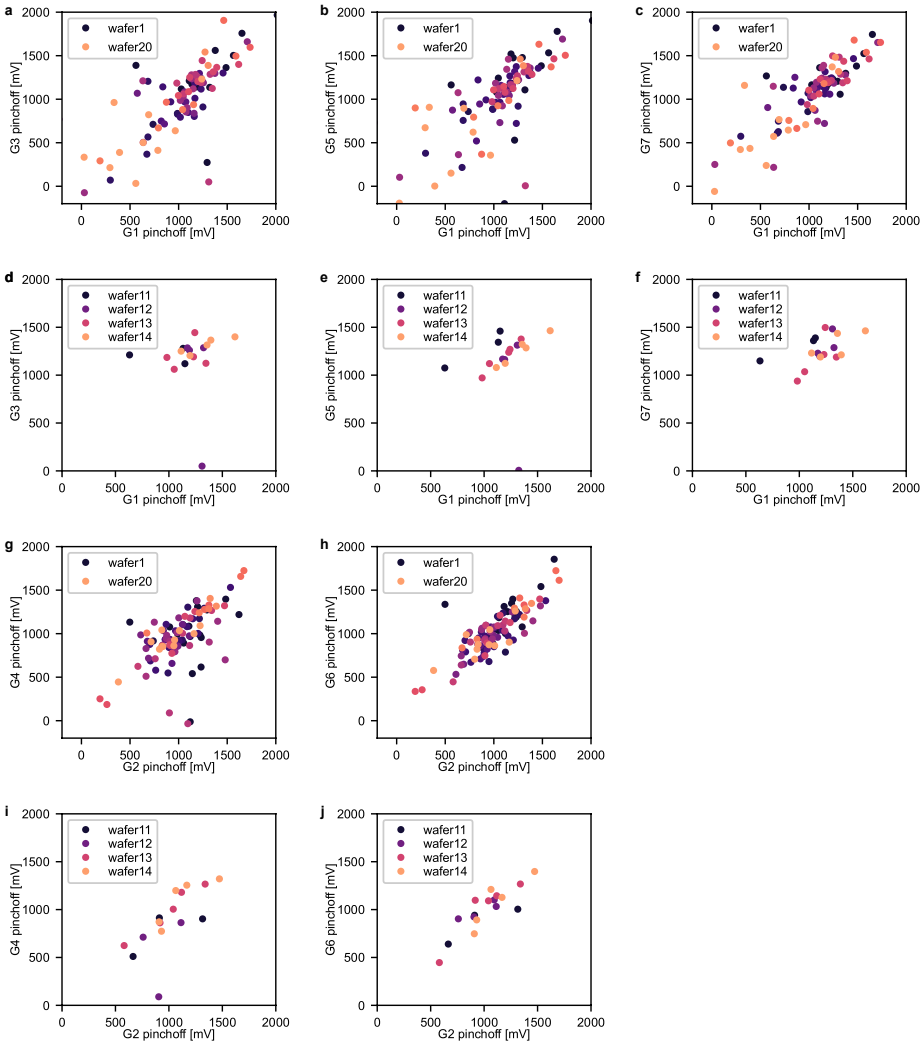


Figure 7.15.: **Correlations of threshold voltages between gates within a quantum dot array made in the same gate layer, measured at low temperature.** Threshold voltage for gates G3, G5 and G7 versus gate G1 (all made in the second gate layer) for wafers 1-20 **a, b, c** and then for wafers 11-14 only **d, e, f**. Threshold voltage for gates G4 and G6 versus gate G2 (all made in the first gate layer) for wafers 1-20 **g, h** and then for wafers 11-14 only **i, j**. Note that for each wafer, as many datapoints are shown as (yielding) devices were characterized at low temperature. If the threshold voltages were all identical, the data points in each panel would all overlap with each other. We see a larger spread when comparing across all 20 different wafers than when comparing only wafers 11-14 to each other, which can be expected since the process parameters are more diverse across all 20 wafers. Furthermore, while the spread in threshold voltages is largest for gate layer 1, there is a clear linear trend between the threshold of different gates made within gate layer 1 on the same device.

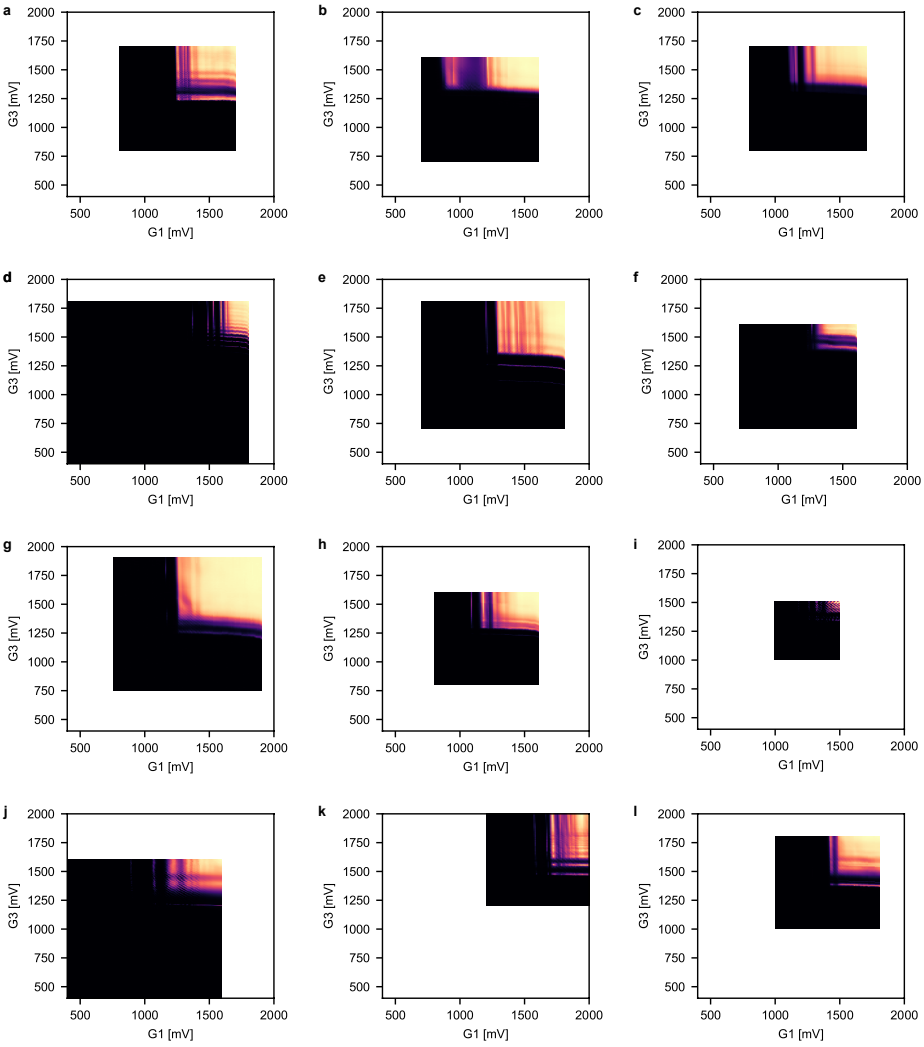


Figure 7.16.: **Barrier-barrier maps for gates** $G1$-$G3$**.** Barrier-barrier maps for a quantum dot under gate $G2$ for 12 different samples, taken from yielding devices across wafers 11 (**a-c**), 12 (**d-f**), 13 (**g-i**) and 14 (**j-l**). For each sample, we are able to form a quantum dot.

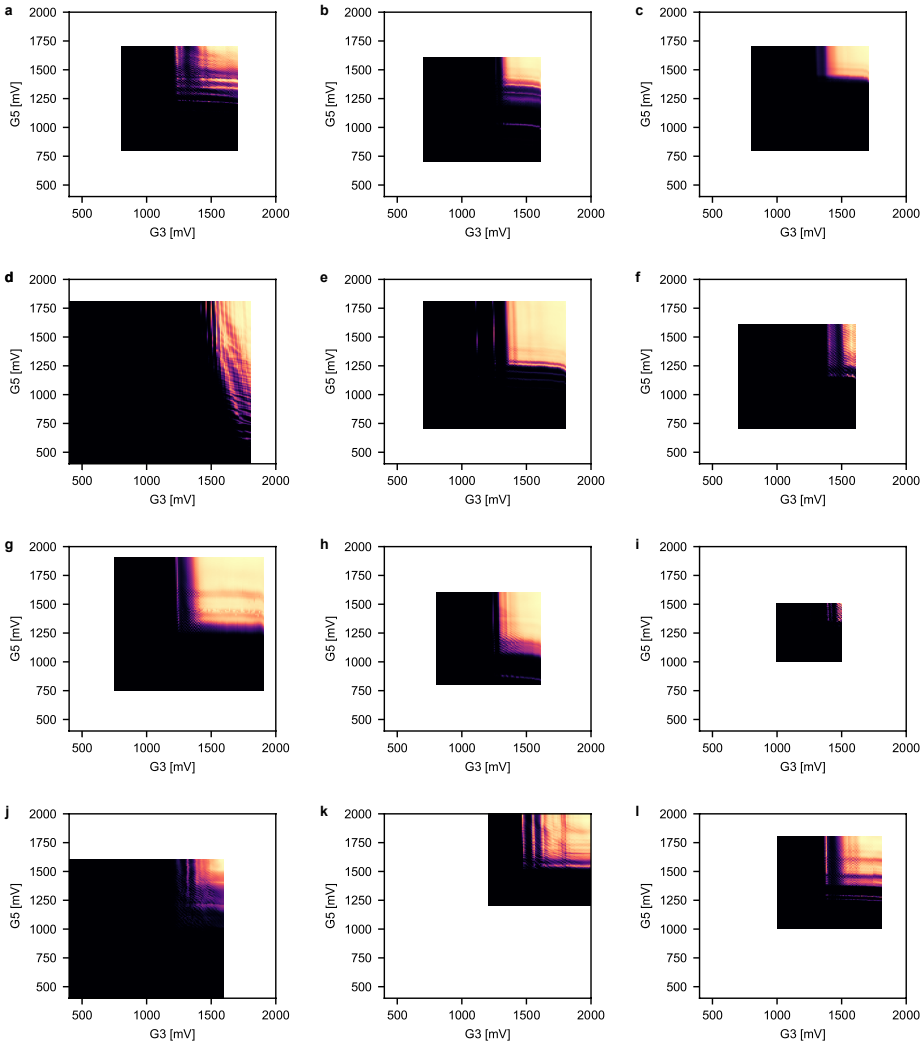


Figure 7.17.: **Barrier-barrier maps for gates** *G*3**-***G*5**.** Barrier-barrier maps for a quantum dot under gate *G*4 for 12 different samples, taken from yielding devices across wafers 11 (**a-c**), 12 (**d-f**), 13 (**g-i**) and 14 (**j-l**). For each sample, we are able to form a quantum dot.

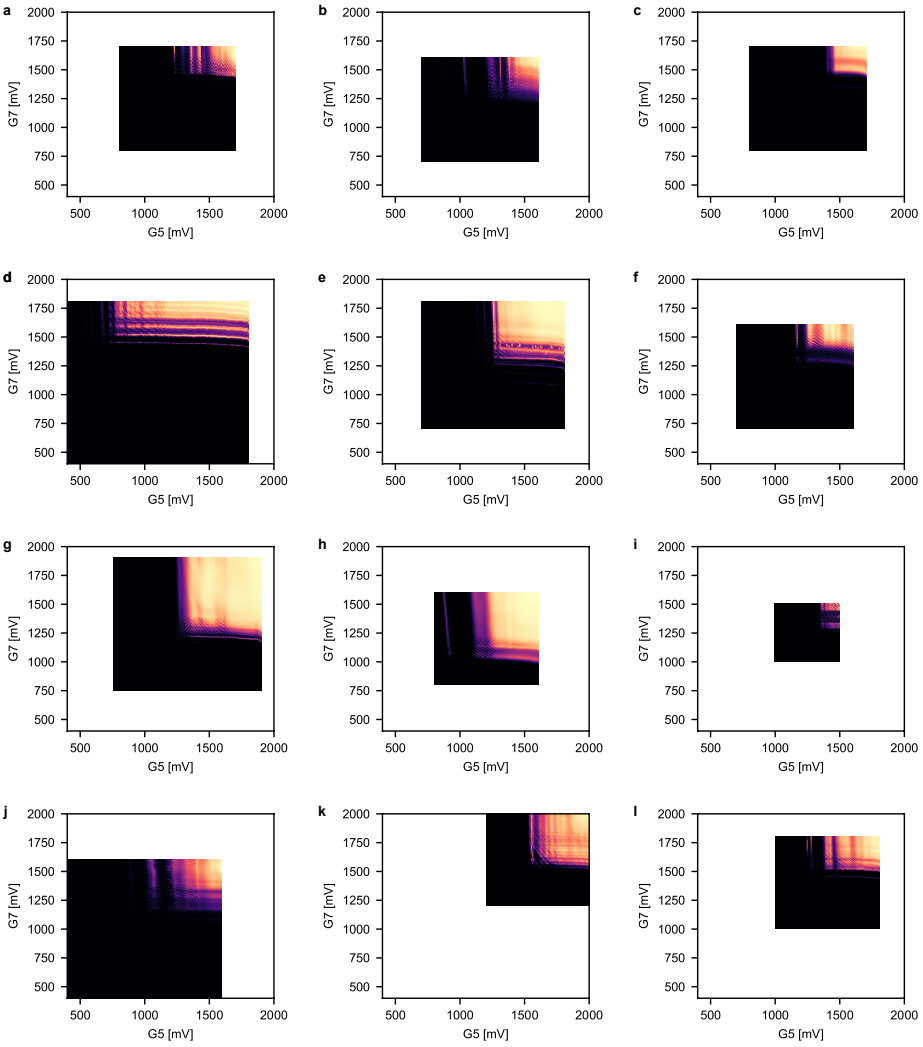


Figure 7.18.: **Barrier-barrier maps for gates** *G*5**-***G*7**.** Barrier-barrier maps for a quantum dot under gate *G*6 for 12 different samples, taken from yielding devices across wafers 11 (**a-c**), 12 (**d-f**), 13 (**g-i**) and 14 (**j-l**). For each sample, we are able to form a quantum dot.

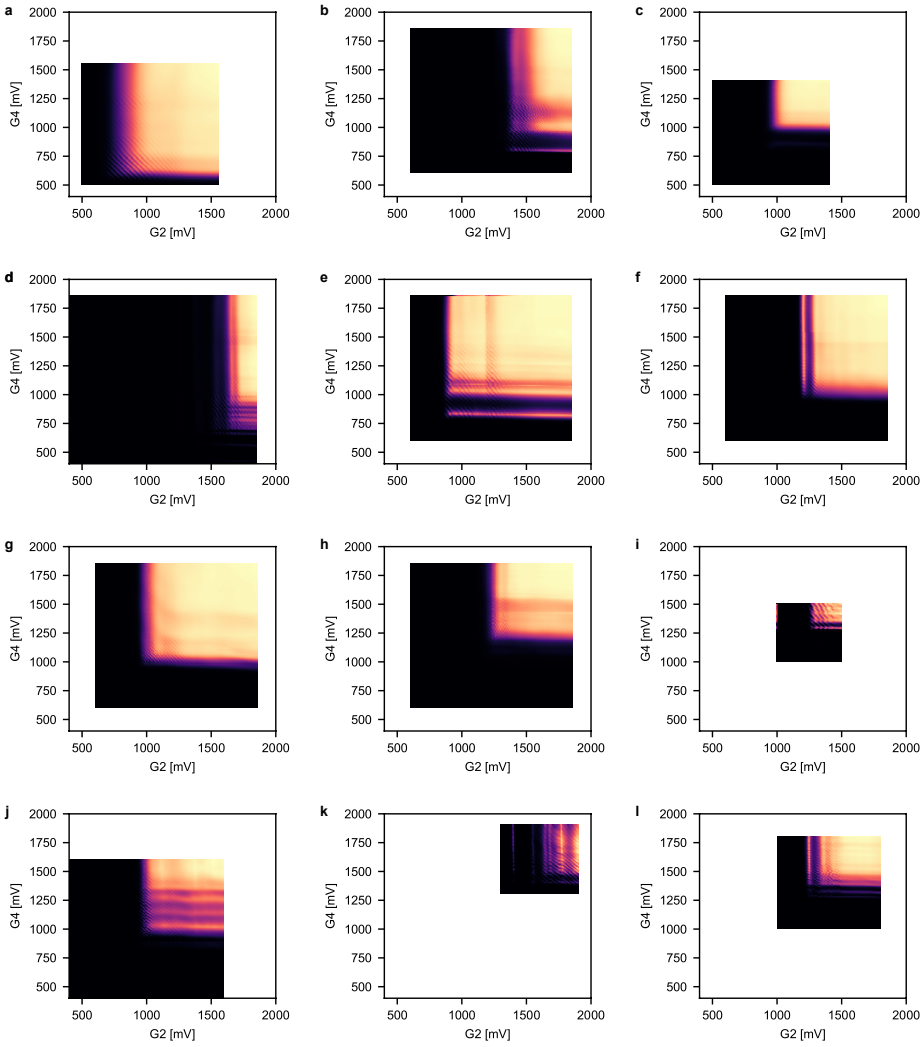


Figure 7.19.: **Barrier-barrier maps for gates** *G2*-*G4*. Barrier-barrier maps for a quantum dot under gate *G3* for 12 different samples, taken from yielding devices across wafers 11 (**a-c**), 12 (**d-f**), 13 (**g-i**) and 14 (**j-l**). For each sample, we are able to form a quantum dot.

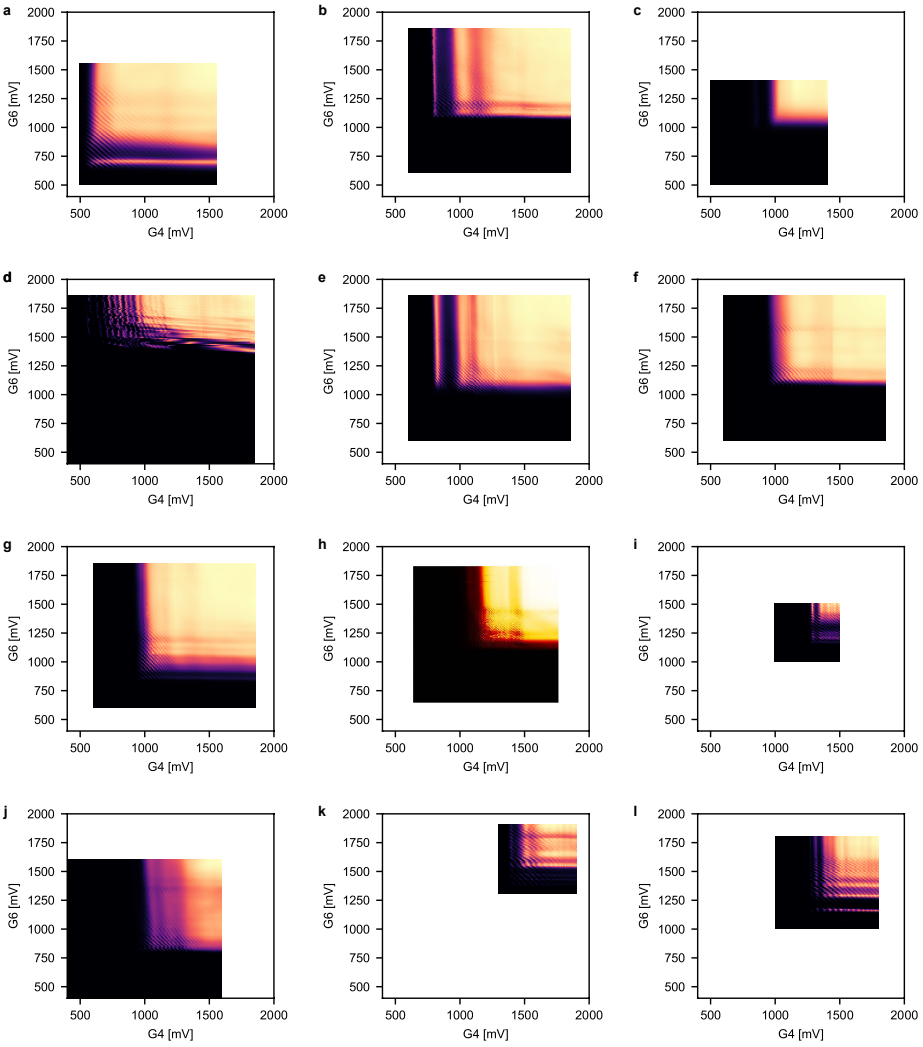


Figure 7.20.: **Barrier-barrier maps for gates** *G*4**-***G*6**.** Barrier-barrier maps for a quantum dot under gate *G*5 for 12 different samples, taken from yielding devices across wafers 11 (**a-c**), 12 (**d-f**), 13 (**g-i**) and 14 (**j-l**). For each sample, we are able to form a quantum dot. For the dot in **h**, the data was not stored properly, so the figure is reproduced from a screenshot.

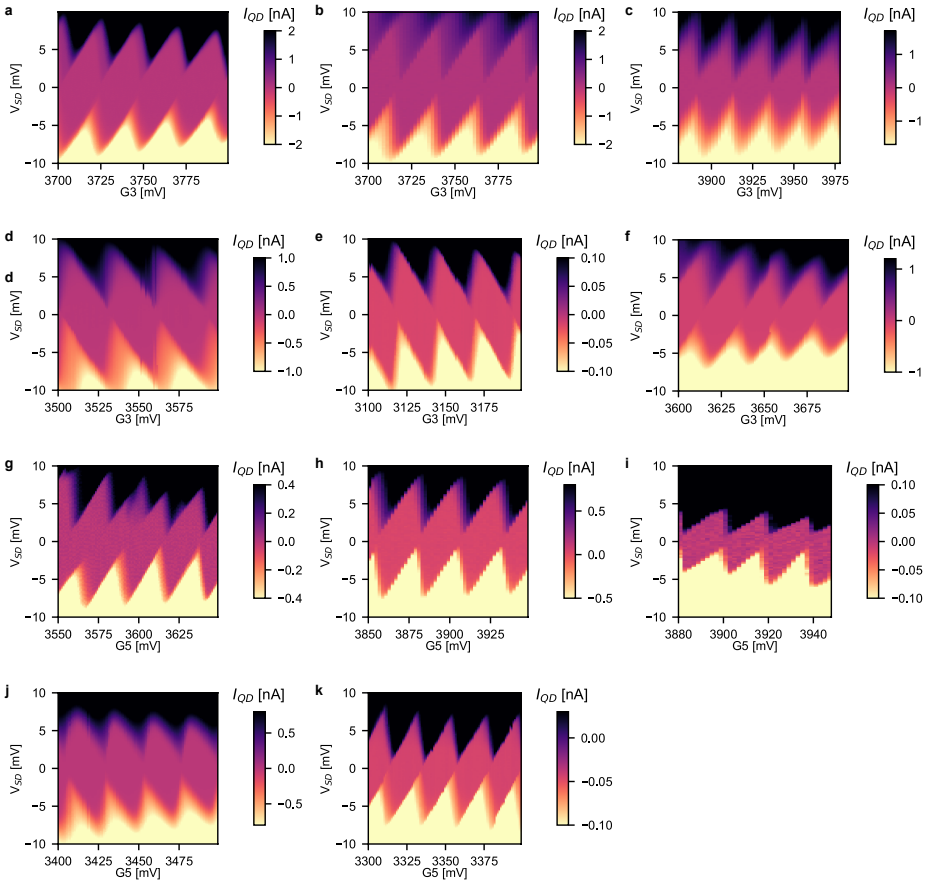


Figure 7.21.: **Coulomb diamonds.** Typical Coulomb blockade diamonds measured in the multi-electron regime, taken on four different samples from the same wafer for dots under gate G3 (**a-f**) and under gate G5 (**g-k**). The dot in the main text, is the dot in **i**. From these diamonds, the quantum dot charging energy and the gate lever arms are determined. Coulomb diamonds are measured by scanning a gate voltage versus the bias voltage applied between the source and the drain contact. When the electrochemical potential of the quantum dot falls outside the bias window, the current through the quantum dot is blocked, i.e. the sample is in Coulomb blockade. Once the electrochemical potential of the quantum dot is aligned within the bias window, Coulomb blockade is lifted. The bias window increases along the vertical axis, hence Coulomb blockade is lifted over a wider gate voltage range. The regions of blockaded current have the characteristic diamond shape. Here, we extract an average charging energy of $8.9 \pm 0.1$ meV (lever arm: $0.37 \pm 0.02$ meV/mV) for the dot under G3 (**a**, **c**, **e**, **g**, **i**, **k**) and an average charging energy of $8.0 \pm 1.4$ meV for the dot under G5 (**b**, **d**, **f**, **h**, **j**). The larger standard deviation in the charging energy of the dot under G5 is mainly caused by the charging energy of the dot in **f** being 5.2 meV, as opposed to the other dots being between 8.7 and 9.0 meV. The average lever arm for G5 dot is $0.36 \pm 0.1$ meV/mV.

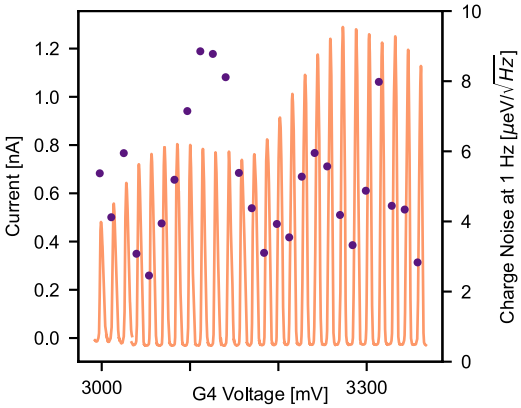


Figure 7.22.: **Charge noise measurements.** Coulomb blockade peaks in the multi- electron regime (orange line) and the power spectral density at 1 Hz of the quantum dot potential fluctuations measured at the flank of each peak (purple dots). The power spectral density shows a $1/f$ slope that is characteristic of charge noise in solid-state devices [164]. See main text for further discussion.

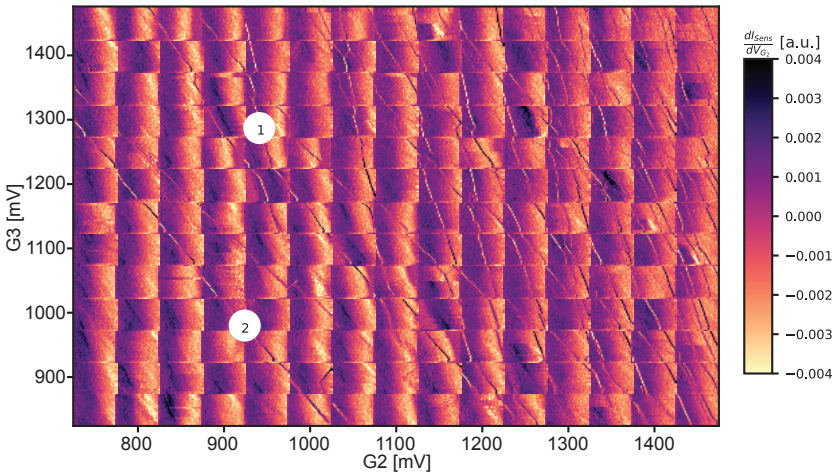


Figure 7.23.: **Charge stability diagram for the few-electron regime.** Charge stability diagram for the few-electron regime of the samples in which qubit 1 and qubit 2 are measured. Smaller charge sensing maps are stitched together to obtain one large map. As pointed out in the main text, the Coulomb peaks become more irregular towards the single-electron regime, indicating dots forming under adjacent gates. Although we observe several spurious dots, the few-electron regime usually looks rather similar to this map. The approximate gate voltages at which qubit 1 and qubit 2 are measured are indicated.

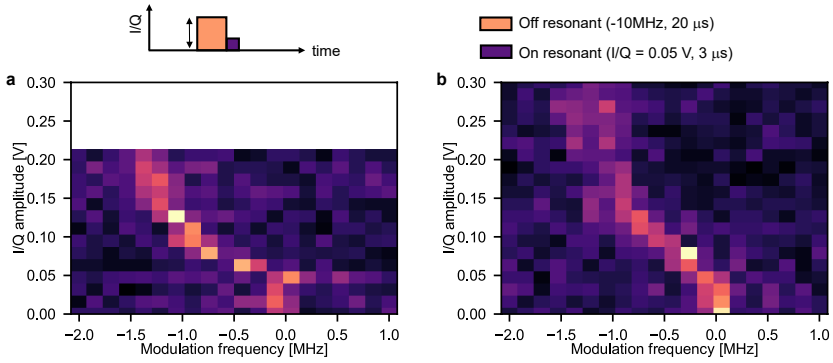


Figure 7.24.: **Frequency shift due to off-resonant microwave pulse amplitude.** Microwave spectroscopy of **a,** qubit 1 and **b,** qubit 2 as a function of the I/Q amplitude of an off-resonant microwave pre-burst (orange in schematic) that is applied immediately before the microwave spectroscopy burst (purple in schematic). Both qubit 1 and qubit 2 show similar behavior with the qubit frequency shifting to a lower frequency when the I/Q amplitude of the off-resonant microwave pre-burst is above 0.05 V. The microwave output power at an I/Q amplitude of 0.2 V is 6 dBm and the LO frequency is 13.072 GHz for qubit 1 and 13.053 GHz for qubit 2 (different tuning than in the main text). The off-resonant burst is 10 MHz away from the LO frequency with a duration of 20 $\mu$s. The spectroscopic microwave burst has an I/Q amplitude of 0.05 V with a duration of 3 $\mu$s.

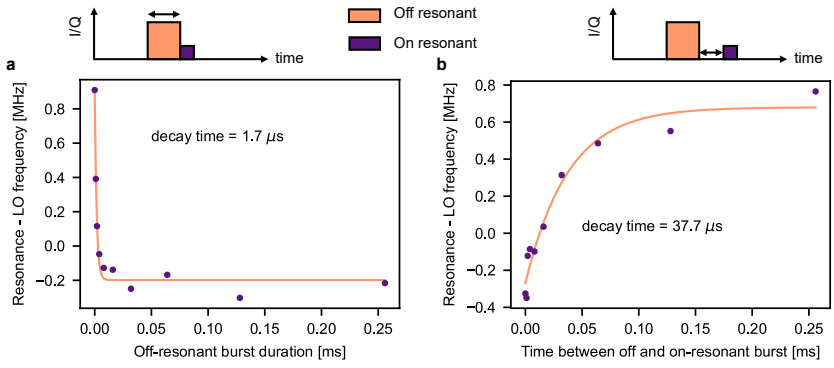


Figure 7.25.: **Time dependent frequency shift of qubit 1.** In these measurements we perform microwave spectroscopy of the qubit at low power to find the qubit resonance frequency. Before the microwave spectroscopy burst (purple in schematic), we apply an off-resonant burst. **a,** The resonance frequency of the qubit as a function of the duration of the off-resonant burst applied before spectroscopy (purple dots). An exponential fit gives a time constant of 1.7 $\mu$s. **b,** The resonant frequency of the qubit as a function of the time between the off-resonant and spectroscopy pulse. An exponential fit gives a time constant of 37 $\mu$s. The time dependence of the resonance frequency of the qubit while turning on and off the microwave signal indicates that the frequency shift is related to heating. The off-resonant burst is applied 5 MHz away from the LO and has an I/Q amplitude of 0.2 V. The spectroscopy burst has an I/Q amplitude of 0.05 V and a duration of 3.5 $\mu$s. The LO frequency is 17.1428 GHz and the microwave output power is 13 dBm at I/Q amplitude of 0.2 V.

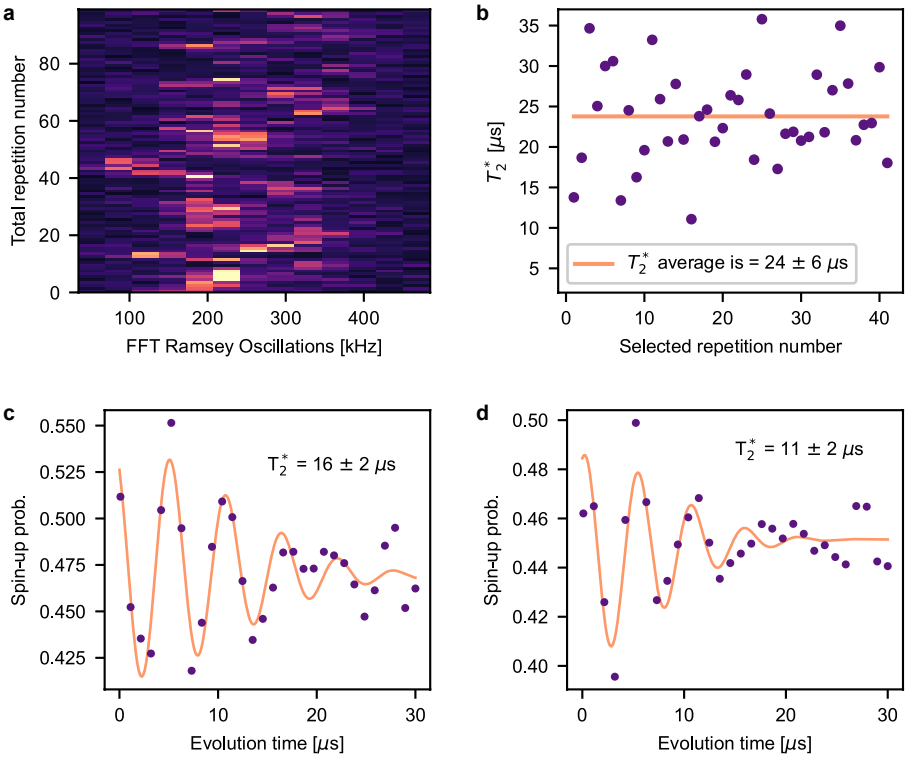


Figure 7.26.: **Ramsey analysis over time. a,** Fast Fourier transform (FFT) of a Ramsey experiment. The data consists of 100 traces, each trace is an average of 200 repetitions. The entire measurement takes three hours in total. The FFT of the Ramsey fringes shows frequency jumps over the timescale of the measurement. Each trace is fitted individually with a decaying Gaussian curve and the fit is analysed by calculating the mean square error. We keep the 41 traces with mean square error below a given threshold. **b,** Extracted $T_2^*$ for the selected traces (purple dots). The average of the $T2^*$ times of the selected traces is 24±6 $\mu$s (orange line). **c,** Ramsey decay curve. The data points are the averaged data of the 41 selected traces. The fit gives a $T_2^*$ time of 16±2 $\mu$s. **d,** Ramsey decay curve. The data points are the average of all 100 traces of the two hour and 40 minute measurement. The fit gives a $T_2^*$ time of 11±2 $\mu$s.

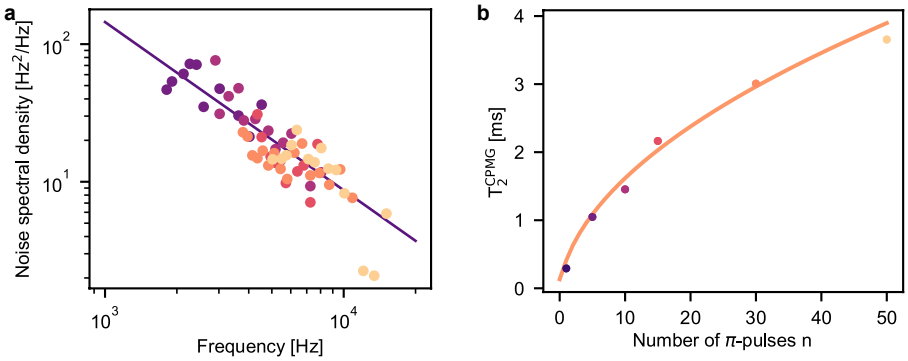


Figure 7.27.: **Noise analysis for qubit 1. a,** Dynamical decoupling pulses for which the time between two subsequent $\pi$-pulses is fixed, can act as a filter function for Gaussian noise [201, 266]. The filter function peaks at a frequency of $f_0 = \frac{n}{2t_{wait}}$, with $n$ the number of $\pi$-pulses and $t_{wait}$ the evolution time. When the filter is sufficiently narrow around the frequency $f_0$, the noise within the bandwidth can be regarded as constant. We can use this to relate the amplitude of the CPMG decay, $A_{CPMG}$, for each wait time and number of $\pi$ pulses, to the dominant noise spectrum for the qubit: $S(f_0) = -\ln(A_{CPMG})/2\pi^2 t_{wait}$ [50, 267]. Here, we plot the noise spectrum, $S(f)$ as a function of frequency for the data shown in Fig. 4c of the main text. We only take data points into account for which $0.15 < A_{CPMG} < 0.85$. We assume that the noise spectrum dominating spin decoherence is described by a power law and use the fit function $Bf^{-\gamma}$. We obtain $\gamma = 1.2 \pm 0.1$ and a noise value at 1 Hz of $B = 820 \pm 750$ Hz/$\sqrt{\text{Hz}}$. This agrees well with the fitting of the individual CPMG curves and the $T_{2,CPMG}$ scaling in Fig. 7.4 of the main text. Using the susceptibility of the qubit resonance frequency to a voltage change of a nearby gate and the energy lever arm of that gate we can compare the noise value B to charge noise. With this conversion we obtain $B = 29 \pm 27$ $\mu$eV/$\sqrt{\text{Hz}}$. **b,** Following [201], we now use the filter function as described in **a** to estimate the noise decay and the noise level at 1 Hz that gives the given $T_{2,CPMG}$ for the number of $\pi$-pulses and fit this to our data. We obtain $\gamma = 1.06 \pm 0.13$ and $B = 30 \pm 18$ $\mu$eV/$\sqrt{\text{Hz}}$. This is comparable to the results obtained in **a**.

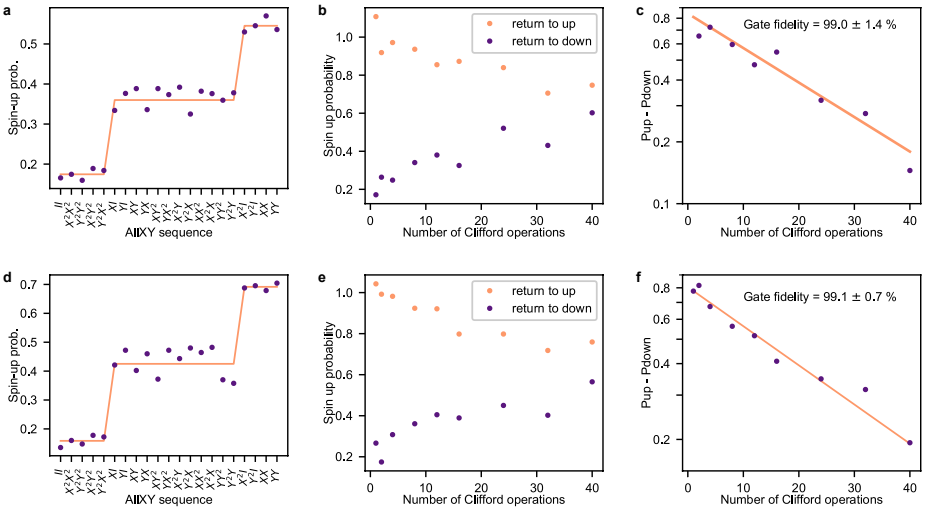


Figure 7.28.: **AllXY and Randomized benchmarking. a, d,** To check the calibration of the single-qubit gates we perform an AllXY sequence [268] on **a,** qubit 1 and **d,** qubit 2. Each data point corresponds to the outcome after sequentially applying two gates from the set I, X, $X^2$, Y, $Y^2$, where X and Y indicate 90° rotations. The data points should ideally follow a staircase pattern (solid line) and deviations from this indicate calibration errors. **b, c, e, f,** To determine the single-qubit gate fidelity, we perform randomized benchmarking [263, 269]. In randomized benchmarking, we randomly select $p$ gates from a set of 24 gates that form the Clifford group and apply them to the qubit. At the end of the sequence we apply an inverting gate from the Clifford group that ideally takes the qubit state back to either $|0\rangle$ or $|1\rangle$. In this experiment, the Clifford gates are decomposed to the set of primitive gates I, $\pm$X, $\pm X^2$, $\pm$Y, $\pm Y^2$. On average a Clifford gate contains 1.875 primitive gates. **b, e,** Normalized spin-up probability as a function of the number of Clifford operations applied for **b,** qubit 1 and **e,** qubit 2. The orange and purple data points correspond to sequences producing a net Clifford of $X^2$ or I, respectively, ideally taking the spin to either spin up or spin down. Each data point corresponds to 40 randomizations of the Clifford sequence and the normalization is done by additional calibration experiments where we apply either just I or $X^2$ to the qubit. **c, f,** The difference between the purple and orange data points in **b, e,** is fitted with and exponential of the form $VP_c^p$. From this we derive an average Clifford-gate fidelity of $F_C = 1-(1-P_c)/2$ of $98.1 \pm 2.7\%$ and $98.2 \pm 1.4\%$ for qubit 1 and qubit 2 respectively. This translates to a primitive gate fidelity of $99.0 \pm 1.4\%$ and $99.1 \pm 0.7\%$ for Q1 and Q2.

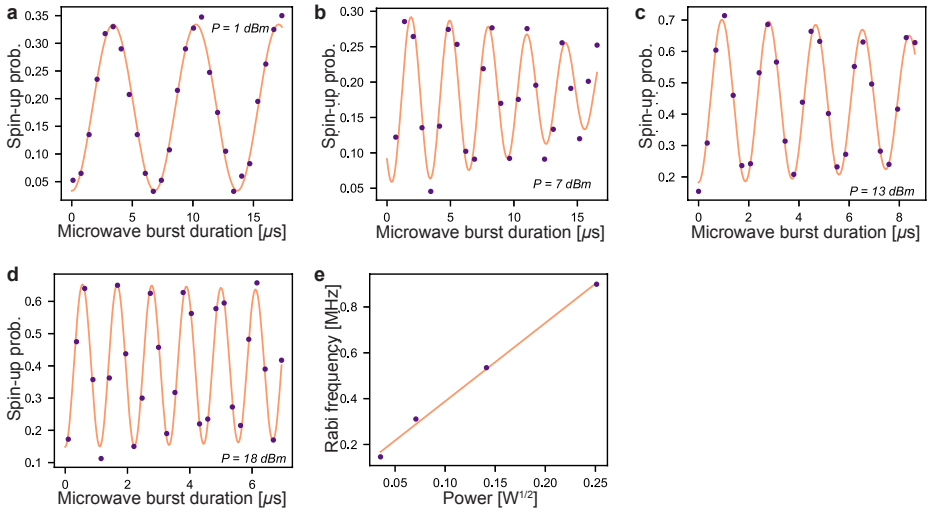


Figure 7.29.: **Rabi oscillations for qubit 2. a-d,** Rabi oscillation of qubit 2 measured for different output powers of the microwave source. **e,** The extracted Rabi frequency is plotted versus the square root of the applied power, showing the expected linear dependence.

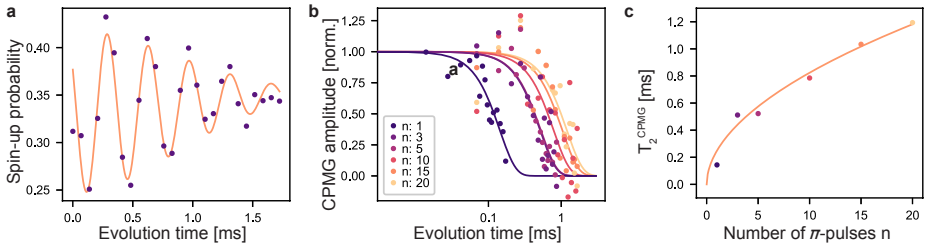


Figure 7.30.: **Coherence of qubit 2. a,** CPMG-curve for qubit 2 for $n = 20$. Fitting this curve, as described in the Experimental methods section, gives $T_{2,CPMG} = 1.2 \pm 0.2$ ms. **b,** Analogously to the case of qubit 1 (see main text), we demodulate and normalize the CPMG amplitude as a function of evolution time for different numbers of $\pi$ pulses, giving the CPMG amplitude. **c,** The measured CPMG decay time as a function of the number of $\pi$-pulses. The orange line represents a fit through the data (excluding $n = 1$) following $T_2^{\mathrm{CPMG}} \propto n^{(\gamma/(\gamma+1))}$. We extract $\gamma = 1.51 \pm 0.15$. Performing a similar analysis as has been done for qubit 1 (see Supplementary Fig. 7.27) gives unreliable results.

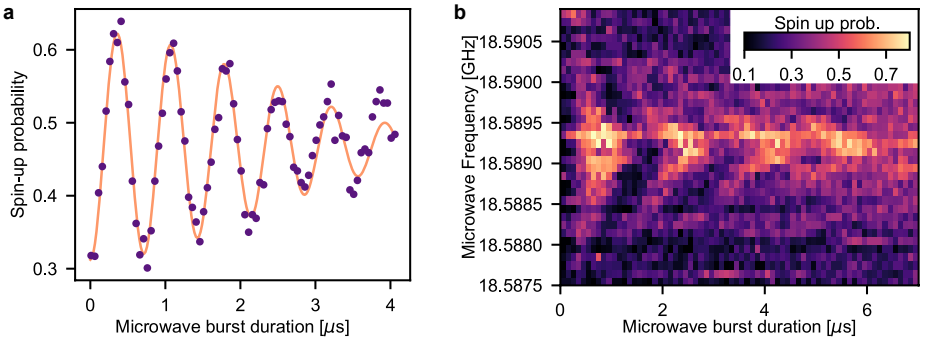


Figure 7.31.: **Rabi oscillations for qubit 3. a,** Rabi oscillation for a third qubit measured on a different device than qubits 1 and 2. The qubit was measured at an external magnetic field of $B = 0.675$ T, giving a Larmor frequency of 18.757 GHz. From fitting the curve, we extract a Rabi frequency of 1.4 MHz. **b,** Spin-up probability versus burst duration and microwave frequency in a slightly different tuning regime. The expected Chevron pattern is visible. We observed a second (spurious) quantum dot in the vicinity of qubit 3 and expect that hybridization with this extra quantum dot is limiting the $T_2^*$ and also the $T_{2,Rabi}$ of qubit 3.

| Paper | | $T_1$ (B-field) [ms] | $T_2^*$ [us] (int time) | $T_{2,Hahn}$ [us] | $T_{2,CPMG}$ ($\pi$) [us] | T$\pi$[us] | $F_{1Q,gate}$ [%] | Substrate | Drive |
|---|---|---|---|---|---|---|---|---|---|
| Zwerver et al. (2021) | Q1 | 1600 (1) | 24(100s) | 292 | 3700 (50) | 0.9 | 99.0 | $^{28}$SiMOS | ESR |
| | Q2 | - | — | 140 | 1200 (20) | - | 99.1 | $^{28}$SiMOS | ESR |
| Veldhorst et al. (2014) [49, 270] | Q1 | — | 120 | 1200 | 28000 (500) | 1.6 | 99.6 | $^{28}$SiMOS | ESR |
| Chan et al. (2020) [270] | Q2 | — | 61 | — | — | — | — | $^{28}$SiMOS | ESR |
| | Q3 | — | 30 | — | — | — | — | $^{28}$SiMOS | ESR |
| Yang et al. (2019) [67] | | $\sim$ 1000 | 33 | 400 | 6700 (122) [159] | - | 99.9 | $^{28}$SiMOS | ESR |
| Huang et al. (2019) [125] | Q1 | - | 24.3 | 290 | - | 1 | 99.3 | $^{28}$SiMOS | ESR |
| | Q2 | | 10.5 | 33.5 | - | - | 99.4 | $^{28}$SiMOS | ESR |
| Yang et al. (2020) [123] | Q1 | $\sim$ 500 | 12.3 | 200 | - | $\sim$ 0.9 | 99.76 | $^{28}$SiMOS | EDSR |
| Petit et al. (2020a) [124] | Q1 | - | 2.1 | - | - | 0.45 | 98.7 | $^{28}$SiMOS | ESR |
| | Q2 | - | 2.7 | - | - | 0.45 | 99.3 | $^{28}$SiMOS | ESR |
| Petit et al. (2020b) [197] | Q1 | - | 2.3 | - | 63 (15) | - | - | $^{28}$SiMOS | ESR |
| *Measured above 1 K* | Q2 | - | 2.9 | - | 44 (15) | - | - | $^{28}$SiMOS | ESR |
| Yang et al. (2013) [117] | | 2600 (1.25) | - | - | - | - | - | $^{Nat}$SiMOS | - |
| Ciriano-Tejel et al. (2021) [70] | D1 | 280 (1) | - | - | - | - | - | $^{28}$SiMOS | - |
| | D2 | 9000 (1) | - | - | - | - | - | $^{28}$SiMOS | - |
| Petit et al. (2018) [118] | | 145 | - | - | - | - | - | $^{28}$SiMOS | - |
| Maurand et al (2016) [253] | | $>$ 0.175 | 0.06 (2s) | 0.245 | - | $\sim$ 0.01 | - | $^{Nat}$SiMOS | - |
| Xue et al. (2021) [105] | Q1 | 100.6 (0.43) | 21.64 | - | - | - | - | $^{28}$Si/SiGe | EDSR |
| | Q2 | 95.0 (0.43) | 10.08 | - | - | - | - | $^{28}$Si/SiGe | EDSR |
| Struck et al. (2020) [157] | Q1 | — | 21 | - | 128 | - | - | $^{28}$Si/SiGe | EDSR |
| Yoneda et al. (2019) [50] | | $>$ 100 | 20 | 99 | 3100 (2400) | 0.12 | 99.9 | $^{28}$Si/SiGe | EDSR |
| Sigillito et al. (2019) [271] | Q1 | - | 2.6 | 41 | - | - | - | $^{28}$Si/SiGe | EDSR |
| | Q2 | - | 1.5 | 31 | - | - | - | $^{28}$Si/SiGe | EDSR |
| | Q3 | - | 10.4 | 72 | - | - | - | $^{28}$Si/SiGe | EDSR |
| | Q4 | 52 | 9.4 | 109 | - | - | - | $^{28}$Si/SiGe | EDSR |
| Takeda et al. (2021) [106] | Q1 | 4.3 | 1.82 | 28.1 | - | 0.1 | 99.43 | $^{28}$Si/SiGe | EDSR |
| | Q2 | 2.67 | 1.69 | 20.5 | - | 0.1 | 99.57 | $^{28}$Si/SiGe | EDSR |
| | Q3 | 1.31 | 1.69 | 45.8 | - | 0.1 | 99.91 | $^{28}$Si/SiGe | EDSR |
| Zajac et al. (2018) [198] | Q1 | 22 | 1.4 | 80 | - | 0.11 | 99.7 | $^{Nat}$Si/SiGe | EDSR |
| | Q2 | - | 1.2 | 22 | - | $\sim$ 0.1 | 99.3 | $^{Nat}$Si/SiGe | EDSR |
| Watson et al. (2018) [104] | Q1 | $>$ 50 | 1 | 19 | - | 0.25 | 99.3 | $^{Nat}$Si/SiGe | EDSR |
| | Q2 | 3.7 | 0.6 | 7 | - | 0.25 | 98.9 | $^{Nat}$Si/SiGe | EDSR |
| Kawakami et al. (2016) [267] | | - | 0.37 | 70 | 400 | 0.37 | 98.99 | $^{Nat}$Si/SiGe | EDSR |
| Borjans et al. (2018) [69] | D1, dot 1 | 65 (0.2) | - | - | - | - | - | $^{Nat}$Si/SiGe | Micromagnet |
| | D1, dot 2 | 160 (0.2) | - | - | - | - | - | $^{Nat}$Si/SiGe | Micromagnet |
| | D2, dot 2 | 5000 (0.4) | - | - | - | - | - | $^{Nat}$Si/SiGe | - |
| | D2, dot 3 | $\sim$ 500 (1) | - | - | - | - | - | $^{Nat}$Si/SiGe | - |
| | D2, dot 5 | $\sim$ 500 (1) | - | - | - | - | - | $^{Nat}$Si/SiGe | - |
| | D2, dot 6 | $\sim$ 2000 (1) | - | - | - | - | - | $^{Nat}$Si/SiGe | - |
| Simmons et al. (2011) [185] | | 2800 (1.85) | - | - | - | - | - | $^{Nat}$Si/SiGe | - |
| Hollmann et al. (2020) [170] | | $\sim$ 1000 (1) | - | - | - | - | - | $^{28}$Si/SiGe | Nanomagnet |

Table 7.1.: **Qubit metrics for single qubits in silicon.** The results obtained in this study compared to qubit poerformance in silicon of recent works. Data are either extracted from the publications directly, or by analysing the figures published in the work. The table respectively lists $T_1$ with the relevant magnetic field, $T_2^*$ with the relevant integration time, $T_{2,Hahn}$, $T_{2,CPMG}$, the time it takes to do a $\pi$-rotation ($T_\pi$) and the single-qubit gate fidelity.

# 8 CONCLUSION AND OUTLOOK

*One never notices what has been done; one can only see what remains to be done*

Marie Curie

## 8.1 CONCLUSION

The phenomenal predictions of quantum mechanical theory can be harnessed in quantum technology. Although we do not fully comprehend the riddles of quantum mechanics yet, we are able to catch and control bits of the quantum world to an increasing extent. Single electrons can be captured and their spin can be controlled to function as a qubit. In this thesis, we explored the potential of these spin qubits to scale to larger systems. This quest was threefold and the results found in this thesis are summarized below:

- In Chapter 5, we explore the ability to scale the number of quantum dots. We do so by developing a tuning method for a platform-independent $N \times M$ quantum dot array that makes use of cross-capacitance compensation. We demonstrate the method by tuning a linear array of eight GaAs quantum dots to the regime where they contain exactly one electron each.
- Chapter 6 presents ongoing work about electron shuttling. The electron is shuttled through an array of up to four neighbouring quantum dots up to 1000 times, corresponding to a distance of approximately 80 $\mu$m. During shuttling, the spin orientation or the electron is preserved. This forms a promising base for a quantum link.
- In collaboration with Intel, in Chapter 7 we harness the experience of the semiconductor industry by manufacturing a quantum chip and controlling a qubit on it. We demonstrate that industrial manufacturing on 300-mm wafers allows for high-yield and reasonable cross-wafer uniformity of the samples, while allowing for well-defined quantum dots and qubits with key performance indicators comparable to state-of-the-art spin-qubit results.



## 8.2 REFLECTIONS AND NEAR-TERM EXPERIMENTS

In this section, we reflect on the results in this thesis and propose near-term experiments.

### 8.2.1 Cross-capacitance compensation for scaling

The work in this thesis started in the midst of the transition to silicon. Work with silicon was still in its infancy and fabrication, tuning and measurement was pioneering work; the smaller dots, overlapping gate architecture, heavy mass and valley splitting posed challenges and as a result, no more than two silicon quantum dots had been demonstrated. For the projects that were not directly silicon-related, one often turned to the convenience of GaAs devices. Also here, scaling was a hurdle and dealing with the cross capacitance from gates to neighbouring quantum dots tremendously slowed down scaling beyond three quantum dots. By making use of cross-capacitance compensation, we developed a platform-independent technique to deterministically tune up quantum dots one by one, without compromising the previously tuned quantum dots. Moreover, we developed material platform-independent metrics to test and compare the performance of silicon samples to advance the fabrication of multi-quantum-dot devices. Today, it is hard to imagine the tuning struggles we had and

the idea of using cross-capacitance compensation for the tuning of both the electrochemical potential of the (silicon) quantum dot (Chapter 5, [107]), and for the tunnel barriers between quantum dots [135] provides for excellent quantum dot control and is widely used in the field [106, 218, 248, 271, 272]. Near-term experiments should focus on scaling the devices to two-dimensional grids of quantum dots, where these quantum dots connect to at least three neighbours.

### 8.2.2 Deterministic teleportation

The shuttling results are a compelling benchmark towards the creation of long-range coherent qubit connectors in silicon, yet coherent shuttling beyond two quantum dots [238, 239] remains to be demonstrated. As multi-qubit registers in silicon and germanium become more common [72, 106, 272], the quantum link becomes the bottleneck in the demonstration of scalable quantum computing architectures. Future efforts should initially focus on monitoring the coherence time of a single qubit while shuttling. For slowly varying and spatially uncorrelated dephasing noise, shuttling is expected to lead to motional narrowing, as in GaAs [237], extending $T_2^*$ while shuttling. The quantum link can be further explored by creating an entangled pair, for which one of the qubits is shuttled over the array. The shuttle fidelity can be determined by means of Bell-state tomography. The functionality of the link can be explored by means of simple quantum algorithms, such as deterministic quantum teleportation. The deterministic teleportation protocol [273] is appealing compared to conditional teleportation [87, 248], as it requires the combination of two-qubit gates with shutting and high-fidelity readout. As a result, it will provide the smallest possible combination of a quantum processor with a quantum link [54]. Just as with conditional teleportation, the deterministic teleportation protocol requires two nodes, Alice and Bob, to share an entangled state. Moreover, Alice has an additional qubit, which state she wants to teleport. Now, instead of performing a measurement of her two qubits in the Bell-basis, as she would do for conditional teleportation, Alice performs two $\sqrt{\text{SWAP}}$-gates on her qubits and then measures them in the $|\uparrow\downarrow\rangle$-basis. Depending on the measurement outcome, communicated classically, Bob has to perform a single-qubit rotation to retrieve Alice's original state [273].

A more elegant way of shuttling is provided by the electron smoothly surfing in a travelling potential wave, or 'conveyer-belt-mode shuttling'. Conveyer belt shuttling circumvents the necessity to form quantum dots all along the connecting link. The potential wave can be created by applying a sine-wave pulse to the metallic gates with a phase shift of $\pi/2$ between the signal applied to neighbouring gates. After four gates, the pulse sequence is repeated. Although this form of shuttling seems more convenient, it also put some constraints on the system. As the period of the waveform includes four gates, ideally, every fifth gate of this so-called conveyor belt is connected. This puts requirements on the sample uniformity. Moreover, charge noise and potential disorder from charged defects could deform the potential landscape, or make the electron hop out. Coherently shuttling an electron in a conveyor-belt

manner without orbital, or valley excitations remains to be demonstrated. Yet theoretical studies estimate a transfer error of $10^{-3}$ for shuttling over a 10-$\mu$m link in a Si/SiGe device [244].

### 8.2.3 High-yield device fabrication

The collaboration with Intel demonstrated that spin qubits in electrically-defined, silicon quantum dots are indeed compatible with the semiconductor industry. The capability of high-yield device fabrication, is a crucial feature when scaling to the millions of qubits that are needed for full-scale quantum computers. Next, the high-volume approach that was developed here, should be advanced to low-temperatures. The capability of comparing and measuring large data qualities at both room temperature and low temperature will provide statistics that expand our understanding of Loss-DiVincenzo qubits in quantum dots and will benefit the improvement of processing conditions to target higher uniformity and lower charge noise. With the installation of a wafer-scale cryogenic probe station, initial measurements have been performed. Simultaneously, devices with tens of gates can readily be fabricated on each wafer. Such high-yield devices are particularly of interest for pioneering long-range shuttling. For example, by tuning the device with the $N + 1$-method and then performing deterministic teleportation between qubits at either end of the array.

## 8.3 THE NISQ ERA; FROM A HANDFUL OF QUBITS TO QUANTUM ADVANTAGE

It has been forty years since Richard Feynman noted that *it is impossible to represent the results of quantum mechanics with a classical universal device* and he first spoke of quantum computers [25]. Since then, the exploration and development of quantum devices has grown rapidly, with the first algorithms that demonstrate quantum advantage being performed [44, 45]. Yet, practical quantum computations require many more qubits; a recent study estimates the need of 20 million qubits to enable factorization of a number that is classically intractable, given an error rate per qubit of $10^{-3}$ [274]. The scaling effort should, however, not be one-dimensionally focussed on qubit quantity, as is often done. The road towards quantum advantage and eventually quantum practicality requires both a high qubit number and qubits with a low error rate[1] [245]. Figure 8.1 illustrates the latest achievements for several qubit platforms. From here, the road towards quantum practicality seems still long. But there are interesting stops along the way; when exceeding 50 high-quality qubits, we enter the NISQ era. Upon further scaling, the NISQ era allows quantum algorithms, albeit noisy, to outperform classical computers and to have some useful applications [29]. Spin qubits seem to be a bit behind, but recent developments in the error rates for single- [71] and two-qubit gates [51, 52, 229], multi-qubit algorithms [72, 272] and the execution of phase error-correction protocols [275, 276] initiated a fast catch-up. Although scaling is a multi-dimensional challenge and this outlook is far from extensive, advancement should mainly be sought in the simultaneous stepping along these two axes.

[1] an error rate in the order of $\epsilon = 10^{-5}$, requires $10^4$ physical qubits per logical qubit to achieve the target error probability $< 10^{-15}$ [245]

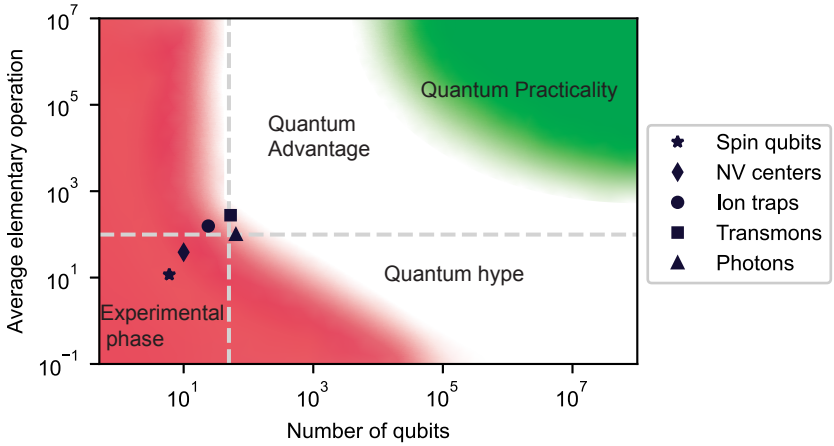


Figure 8.1.: **Current status of different types of qubits.** The status of different qubit platforms as expressed in maximum qubit number that is reported and their corresponding average number of elementary two-qubit operations. The average number of elementary operations before an error occurs, is defined as one divided by error rate, or $1/(1-\mathcal{F})$, with $\mathcal{F}$ the gate fidelity. Data extracted from: Si spin qubits [272], NV centers in diamond [277], Ion traps [278], Transmons [44], Photons [45]. The grey dotted line represent the 50 qubit threshold (horizontal) and the error correction threshold of 99% fidelity as determined in [43] (vertical). Most platforms are currently still residing in the experimental phase, steadily moving towards the NISQ era [29] and quantum advantage.

### 8.3.1 Qubit quantity

The importance of a high sample yield for an increasing number of qubits per chip is emphasized in Fig. 8.2. Under the naive assumption that a qubit works when its metallic gates work, a correlation between gate yield and device yield is plotted for different numbers of qubits. We assumed an average of 2.1 gates per qubit, including plunger and barrier gates as well as overhead, such as accumulation gates and striplines. With the number of qubits growing, device yield rapidly falls with decreasing gate yield; even with a gate yield of 99.5%, the yield for a 1000-qubit device is smaller than $10^{-4}$. For such qubit numbers the options are threehold; either we need to accept non-working qubits on the devices, we need to increase the gate yield, or we decrease the average number of gates per qubit, for example as in a crossbar architecture [55]. The latter puts extra constraints on sample uniformity. Industrial manufacturing seems to be able to meet the yield requirement; chapter 7 reports a *device* yield of 98%, yet the *gate* yield already exceeded 99%. Yet, this device yield is characterized at room temperature. Although an initial analysis on the correlation between room-temperature low-temperature data is included in chapter 7, it would be instructive to extend this analysis. High-volume device testing, both at room temperature and low temperature, allows to define, compare and improve device performance, both with regards to device yield and sample uniformity. Ideally, a correlation is found between room-temperature metrics and qubit performance, such that room-temperature measurements can already predict qubit be-

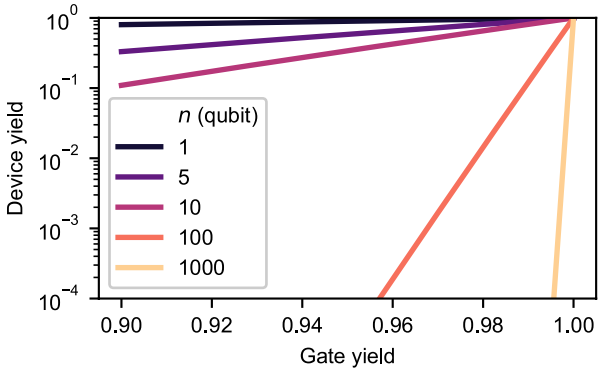


Figure 8.2.: **Device yield for given metallic gate yield** The yield of an *n*-qubit device as a function of gate yield, under the simplified assumption that a qubit contains 2.1 gates on average and that if the gates work, the qubits work. Figure inspired on [279].

haviour. Interesting metrics to compare are subthreshold slope, charge noise and coherence time.

Efforts in Si and Ge spin qubits have exclusively focussed on linear and $2 \times 2$ qubit arrays where each qubit is connected to up to two neighbouring, with limited the utilization of the second dimension. Both the most commonly-referenced method for error correction [43] as well as scaling architectures for spin qubits [54–56, 249] assume connectivity in square lattices with nearest-neighbour connectivity to at least three qubits. Qubit arrays beyond $2 \times 2$ put extra strain on gate architectures and sample uniformity. Quantum dots can either be formed by individual, overlapping gate electrodes, or dots can be formed by means of shared gate control. The space for the former can best be found in the three-dimensional plane by using interconnecting vias. The latter requires a leap in sample uniformity. Both methods can be explored via simple 2-D arrays, such as a cross architecture, where one qubit is connected to four other qubits, or a $3 \times 2 \times 3$-array. Either way, there is plenty of room at the second dimension.



### 8.3.2 Qubit quality

Following Devoret and Schoelkopf [38], we can benchmark the progress of both single-qubit and two-qubit operations over the years, see Fig. 8.3. The improvement of spin qubits is evident with both single-qubit and two-qubit gate error rates now residing below $10^{-2}$. Naively, we could follow a linear fit through the data points on a logarithmic scale and create a Moore's law equivalent for spin qubits, predicting a $10^{-8}$ single qubit error rate by 2040. However, we better substantiate the room for improvement that lead to such wild predictions. Errors can accumulate through a lack of calibration. As the number of qubits increases, the need for fast, well-defined (automatic) calibration protocols that consider both individual qubit properties and qubit crosstalk increases. Additionally, well-tuned qubit gates, such as the net-zero gate, could potentially create an echo-effect for noise fluctuation and increase gate fidelity [284].

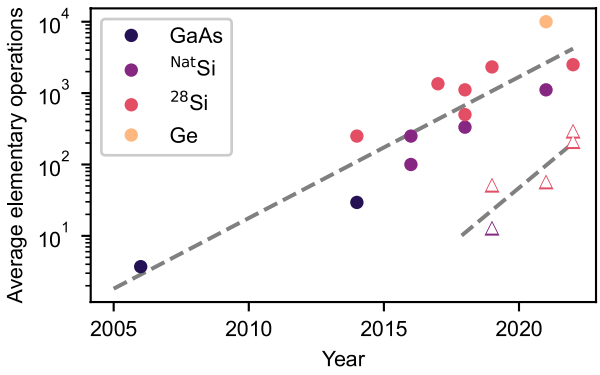


Figure 8.3.: **Spin qubit improvement over the years.** Exponential progress in the performance of spin qubits in electrically-defined quantum dots. The average number of elementary operations is defined as $1/(1-\mathcal{F})$ for single qubits (closed circles) and two-qubit interactions (open triangles), with $\mathcal{F}$ the gate fidelity. Singe-qubit data is extracted from (per year from low to high): [49, 50, 67, 71, 78, 106, 159, 198, 267, 272, 280–282]. The two-qubit data is extracted from (per year from low to high): [51, 52, 125, 199, 283]. The fitted lines are a guide to the eye.

Moreover, the error rate is determined both by the qubit coherence time and the qubit rotation speed.

Spin qubit coherence is currently mainly limited by charge noise, caused by two-level fluctuators and defects in the material stack [238]. Charge noise is rather poorly understood to the level where there is no unambiguous metric that clearly defines it. Reduction in charge noise could be accomplished by formulating a well-defined metric that facilitates charge noise understanding. Moreover, parallel and collaborative efforts of material physicists and quantum dot physicists can focus on studying the number of particular defects, their effects on qubit coherence and ways to reduce them. There are indications that defects in the gate oxide and at the oxide interface are the main contributor to charge noise [160]. A deeper quantum well, as well as cleaner oxides could potentially contribute to increasing qubit coherence.

Qubit driving is at this point sufficiently hampered by the heating generated by the pulses for qubit driving, see chapter 7 of this thesis. This heating puts restraints to the power that can be used to drive the qubits and hence limits the Rabi frequency. It would be instructive to better understand this heating effect and study its relation to qubit frequency and electron temperature. Perhaps a driving sweet-spot could be found.

As both the number of qubits and the qubit fidelities increase, a proof-of-principle experiment that could be performed on the way towards quantum advantage, is an error correction stabilizer protocol beyond the repetition code. An example within reach would be a distance-3 color code, that combines a two-dimensional array with 10 high-fidelity qubits [245].



## 8.4 FROM QUANTUM ADVANTAGE TO QUANTUM PRACTICALITY

Quantum advantage with silicon and germanium spin qubits seems feasible. Yet the road towards quantum practicality has many more challenges across all layers of the quantum gate stack, among which the management of all the control lines. Ref. [285] proposes an equivalent for Rent's rule for quantum computers, where they distinguish gate wiring, chip wiring, I/O lines and room-temperature wiring separately. The first two can be significantly reduced by sharing gate architectures [55], or by adding control electronics on the chip, such as waveform generators [105], or transistor-based switches to control floating gates [250, 286]. The heating associated with the latter could impose constraints for the temperature at which this system can be operated, requiring quantum logic at around 4 K [123, 124, 287]. Such efforts require an increasing collaboration between specialists from different fields, among which physicists, electrical engineers and information scientists. This may lead one to conclude that, although we may find several physics questions along the way, the road towards fault-tolerant quantum computation is slowly moving away from science and starts leaning towards engineering. Is quantum computing then becoming a mere engineering field? I think it is not. We are just at the beginning: the study of quantum mechanics and elements allowed by practical quantum computation will open a new chapter in physics. And, as the chained people in Plato's cave, we may not be able to turn around and see the actual Forms that make up the physical laws. But quantum computers will enrich the shadows that we can see and hence allow us to interpret the Forms more and more thoroughly and eventually increase our comprehension.

# APPENDIX A: VIRTUAL GATE MATRICES

The following matrices show examples of cross-capacitance matrices generated while tuning up the first three QDs of an array and one sensing dot. See main text for details on the procedure. The matrices include the gates for six QDs and two sensing dots and are ordered as following: $X_1$, $B_1$, $P_2$, $B_2$, $P_3$, $B_3$, $P_4$, $B_4$, $P_5$, $B_5$, $P_6$, $B_6$, $P_7$, $B_7$, $X_2$.

$$A_1 = \begin{pmatrix}
1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0
\end{pmatrix}$$

$$A_2 = \begin{pmatrix}
1.0 & 0.05 & 0.1 & 0.07 & 0.05 & 0.04 & -0.02 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.03 \\
0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
-0.2 & 0.73 & 0.98 & 0.81 & 0.3 & 0.19 & 0.06 & 0.0 & 0.01 & 0.02 & 0.0 & 0.0 & 0.0 & 0.0 & 0.01 \\
0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.01 & 0.23 & 0.41 & 0.97 & 1.0 & 0.69 & 0.15 & 0.02 & 0.01 & 0.0 & 0.0 & 0.0 & 0.0 & 0.02 & 0.02 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0
\end{pmatrix}$$

A

$$A_4' = \begin{pmatrix}
1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.75 & 0.01 & -0.16 & -0.12 & 0.56 & 0.84 & 1.0 & 0.91 & 0.22 & 0.05 & 0.11 & 0.2 & 0.08 & -0.02 & 0.03 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0
\end{pmatrix}$$

$$A_4 = \begin{pmatrix}
1.0 & 0.05 & 0.1 & 0.07 & 0.05 & 0.04 & -0.02 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.03 \\
0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.2 & 0.73 & 0.98 & 0.81 & 0.3 & 0.19 & 0.06 & 0.0 & 0.01 & 0.02 & 0.0 & 0.0 & 0.0 & 0.0 & 0.01 \\
0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.01 & 0.23 & 0.41 & 0.97 & 1.0 & 0.69 & 0.15 & 0.02 & 0.01 & 0.0 & 0.0 & 0.0 & 0.0 & 0.02 & 0.02 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.79 & 0.06 & 0.15 & 0.34 & 0.55 & 1.23 & 1.06 & 0.92 & 0.23 & 0.05 & 0.11 & 0.2 & 0.07 & -0.01 & 0.07 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0 & 0.0 \\
0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 0.0 & 1.0
\end{pmatrix}$$

We noticed that the screening effects from $P_4$ and $B_4$ were limited, and took $A_5'$ to be the identity in this case, so $A_5 = A_4$. For subsequent dots, we did remeasure the cross-talk (step 5 in the protocol).

# APPENDIX B: DATA AVAILABILITY

B

Datasets and analysis scripts supporting the findings in chapter 5 of this thesis are available at https://doi.org/10.5281/zenodo.2620418.

Datasets and analysis scripts supporting the conclusions of chapter 7 of this thesis are available at https://doi.org/10.5281/zenodo.4478855.

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*is by standing on the shoulders of Giants*

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QuTech such a good place. I miss our runs together, where you effortlessly continue for 15 km extra, and our conference tradition of assigning cartoon characters to everyone. **Udit**, my Iceland-organising-partner-in-crime. And it was fantastic! Your positive energy makes everyone smile. Thank you for fabbing the Qubyte. Your decision to spend the last months of your PhD on the shuttle project was exactly the motivational push I needed. You are a very talented teacher and I am sure you will do an amazing job in India. **Guoji**, you are the embodiment of the work hard, play hard principle and I am inspired by how you always seamlessly seem to balance those two. You are one of the most motivated, talented scientists that I know and I'm looking forward to seeing the next steps that you will take with the Intel samples. Thank you for always making sure that no free food was gone to waste. **Stephan**, you are an explosion of ideas, creativity and physics intuition and I'm happy to see that the multi-qubit project took off. Thank you that you matched my craziness on many levels, among which editing a movie until dawn and sharing our love for M&M's. I hope to drink many more ~~beers~~ wines with you to talk about your start ups. **Sjaak**, when we started our PhD's, I was convinced we would collaborate for four years. Although this being far from reality, I really enjoyed the (sometimes deep) conversations we had that sharpened my thoughts and were just a good motivation. Your drive to understand everything to the very last detail is unequalled and I hope it brings you far in Kopenhagen and beyond. **Christian**, together we discovered all ins and outs of the Qubyte. I could always count on you to keep on trying when things did not seem to work, to go on a chocolate break, or on your excellent baking skills. Your feeling for and knowledge of the equipment is amazing. Thank you for your patience, friendliness and helpfulness, it made the lab a better place. **JP**, you guided me through the first steps of my PhD with elegance and laughter. And even years later, I can always knock on your door with questions and for advice. Your feeling for physics is impressive and your stories are unmatched. You are truly the (wacky) wizard and I hope your Australian lab will soon start to flourish. **Xiao**, you are a walking paper library. I could always count on you to be in the lab, or to share the latest gossip. Thank you for guiding us to a jazz bar in Chicago, that was a fun night! **Delphine**, your motivation to optimize all sorts of processes in the lab and in fab resulted in spectacular results. Thank you for the runs that we could both use to vent, the talks and the pre-running dinners. It was a joy to have you around. **Sergey**, your fab knowledge is unparalleled. The passion, expertise and patience with which you handle and explain all fab- and sample-related problems accelerated our search for working SiGe devices. **Mateusz**, I admire the fact that, no matter what happens, you are always relaxed. The last years you grew to be the nestor of our lab, being the indispensable advisor to almost all projects. Thank you for managing us all through the March Meeting with so much ease. We still have to eat cheesecake one day. **Patrick**, your thorough and deep understanding of spin-qubit physics is otherwordly. Thank you for always being happy to explain some physical details to me and for driving me from the airport to San Sebastian with my crutches. I wish you all the best at IBM. **Tzu-Kan**, I admire how quickly you got yourself comfortable with the spin-qubit know-how. Your creativity and patience has propelled many projects in the lab and I am sure you will thrive as a group leader. I wish you all the luck with that! **Max**, you are amazing. You manage to bring an extra level to all projects that you co-author, yet you

always seem to have time for every single question and discussion. It is more than deserved that you got the grant and I cannot wait to see the amazing things you will do with it. **Nodar**, the big friendly giant. You seem to be relaxedness itself. Thank for always making time for discussions and suggestions to bring the shuttle project further. I had fun negotiating with you about fridge time. The pole-dancing skills that you demonstrated in Iceland are unequaled (at least in our group). **Tom**, I always looked up to you when you were in Delft and I am happy to have pushed the Intel project with you, both on our own side of the Atlantic. Thank you for the beers, the hikes and the MBA game we went to in Portland. **Alice**, I admire the perseverance you showed during your tumultuous PhD and enjoyed the friendliness that you brought to the lab. I am so happy to see that everything came together so nicely and wish you all the luck in China! **Florian**, keep on smiling (or putting your finger between your teeth) and you will have as many qubits in two dimensions as you want! **Pablo**, thank you for the music that you literally and figuratively brought the last two years. You possess the exceptional combination of a deep physics intuition and a deep social intuition that, I am sure, will greatly improve our lab. Please, don't fall in the trap of not saying 'no' enough. I hope to have many discussion on the foundations and interpretations of QM with you in the future! **Sander**, your endless patience and your solution for everything is the backbone of our scientific efforts. **Jurgen**, your helpfulness and motivation make you an asset to the lab. I hope you get to follow the paths that inspire you most. **Oriol**, your perseverance and drive will get you far. And, hopefully, hot! **Xin**, good luck with the quantum simulation project. **Brennan**, I really enjoyed the discussions on the interpretations of quantum mechanics with you and the well-funded arguments you brought in. I was glad to see you join our group and stay. I am convinced that your drive to understand everything will bring you great results, the first ones already coming in. **Maxim**, your humour makes the lab brighter and your candy makes the lab sweeter. I cannot wait to see some shuttling soon. **Liza** and **Eline**, it is very good to see the group getting a louder female voice. Good luck with your projects, I am sure they will thrive.

**Toivo**, thank you for introducing me in the spin qubit world and emphasizing the importance of the work hard, play hard principle. I still find it interesting to see how different our paths went and wish you all the luck in Africa. And **Takafumi**, thank you for teaching me all the shuttling basics with so much patience. Thank you, **Pieter**, for being the third force behind the Qubyte project and always being interested in follow-up work. Good luck with the demonstrator, I cannot wait to work with six qubits in the cloud. **Lara**, it is so nice to have you join the fab team. Your drive to help everyone will result in great samples soon! **Kostas**, it was fun having you around and learning some Greek words. **Luc**, thank you for helping out with all sort of software struggles. **Amir**, **Andrea**, **Gabriel**, **Nima**, **James**, **Haruki**, thank you for all your help and all the chats over the years.

**Brian**, thank you for the good discussions we had on all kinds of topics. I felt that you were one of the first people who valued me as a scientist and that really boosted my confidence! I have great memories of our time in Portland with you and **Luca**. Luca, your great understanding of code and data made your projects flourish. Thank you for your help with the code. **Will**, it was amazing to see you grow as a physicist with as a result, you holding the single-qubit-gate-fidelity record for spin qubits. More than deserved. Your musical talent is beyond sensational

and I hope to often hear you play an amazing jazz solo, single-handedly, whilst holding a beer in your other hand. Enjoy Kopenhagen! **Nico**, although we started on the same day, we followed very different paths. I always enjoyed to share the office with you and bash on all the bureaucratics that came with doing a PhD. **Gertjan**, your dry humour and talent for writing graduation songs are unmatched. **Marcel**, thank you for so precisely arranging all dipstick issues. **Hanifa**, you are a bouncing ball of enthusiasm and whit. Simultaneously, you strive for a deep physics understanding. It was a joy to share an office, HT, and I am looking forward to hearing about 3D quantum dot arrays. **Francesco**, I took a lot of joy in the occasional half-Italian, half-English conversations we had in the hallway. **Luka**, your structured way of working will hopefully lead to extensive qubit arrays. It was a blast to discover Chicago with you. **Mario**, thank you for all your willingness to help and think along for the statistics part of the semiconductor manufacturing paper, it made it stronger. **Alberto**, I always enjoyed you tearing along when I was biking from Rotterdam to Delft, quickly looking back and waving. **Roy**, **Marco**, **David**, **Chien-An**, **Corontin**, **Valentin**, **Job**, **LaReine**, **Diego**, **Davide**, **Lucas**, **Slava** and **Mohammad**, thank you for making the spin qubit team the inspiring team it was and is to work in.

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**Marja**, thank you so much for making the whole spin qubit group run so smoothly by being so accurate and attentive. And thank you for the many nice chats that we had that provided a perfect break. **Chantal**, **Joanna**, **Jenny**, **Helena**, **Grazia**, thank you for making everyone's life at QuTech easier.

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CURRICULUM VITÆ

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## Anne Marije Jeanette ZWERVER

March 3, 1989 — Born in 's Gravenhage, the Netherlands.

### EDUCATION

2001–2007 — Secondary School - Gymnasium, *cum laude*
Barlaeus Gymnasium, Amsterdam, the Netherlands

2008-2012 — Bachelor of Science in Systems Engineering, Policy Analysis & Management
Delft University of Technology, Delft, the Netherlands

2009 - 2015 — Bachelor of Science and Master of Science in Applied Physics
Delft University of Technology, Delft, the Netherlands
*BSc. Thesis:* Pressure for a new cooling system; Study of the magnetocaloric effect of $Mn_xFe_{1.95-x}P_ySi_{1-y}$ by addition of hydrogen and under hydrostatic pressure
*Supervisors:* Prof. dr. E.H. Brück, Dr. F. Guillou and Dr. L. Caron
*MSc. Thesis:* Towards cavity-enhanced spin-photon entanglement in diamond
*Supervisors:* Dr. S. Bogdanović and Prof. dr. ir. R. Hanson

2017-2021 — Ph.D. in experimental Physics
Delft University of Technology, Delft, the Netherlands
*Thesis:* Scaling spin qubits in quantum dots; more - distant - industrial
*Promotor:* Prof. dr. ir. L. M. K. Vandersypen

### PROFESSIONAL EXPERIENCE

2012–2013 — President Delftsch Studenten Corps, Delft, the Netherlands
2016–2017 — Engineering consultant at Bluerise, Delft, the Netherlands
2017–2018 — Developer and teacher of a highschool course on Quantum Computing, Amsterdam, the Netherlands

## SCIENTIFIC PUBLICATIONS

5. *Qubits made by advanced semiconductor manufacturing*
   **A.M.J. Zwerver**, T. Krähenmann, T.F. Watson, L. Lampert, H.C. George, R. Pillarisetty, S.A. Bojarski, P. Amin, S.V. Amitonov, J.M. Boter, R. Caudillo, D. Corras-Serrano, J.P. Dehollain, G. Droulers, E.M. Henry, R. Kotlyar, M. Lodari, F. Luthi, D.J. Michalak, B.K. Mueller, S. Neyens, J. Roberts, N. Samkharadze, G. Zheng, O.K. Zietz, G. Scappucci, M. Veldhorst, L.M.K. Vandersypen, J.S. Clarke
   In print with Nature Electronics (2022)

4. *Atomic fluctuations lifting the energy degeneracy in Si/SiGe quantum dots*
   B. Paquelet Wuetz, M.P. Losert, S. Koelling, L.E.A. Stehouwer, **A.M.J. Zwerver**, S.G.J. Philips, M.T. Mądzik, X. Xue, G. Zheng, M. Lodari, S.V. Amitonov, N. Samkharadze, A. Sammak, L.M.K. Vandersypen, R. Rahman, S.N. Coppersmith, O. Moutanabbir, M. Friesen, G. Scappucci
   Preprint at ArXiv: arXiv:2112.09606 (2021)

3. *On-chip integration of Si/SiGe-based quantum dots and switched-capacitor circuits*
   Y. Xu, F.K. Unseld, A. Corna, **A.M.J. Zwerver**, A. Sammak, D. Brousse, N. Samkharadze, S.V. Amitonov, M. Veldhorst, G. Scappucci, R. Ishihara, and L.M.K. Vandersypen,
   Applied Physics Letters **117**, 144002 (2020).

2. *Loading a quantum-dot based "Qubyte" register*
   C. Volk*, **A.M.J. Zwerver***, U. Mukhopadhyay, P.T. Eendebak, C.J. van Diepen, J.P. Dehollain, T. Hensgens, T. Fujita, C. Reichl, W. Wegscheider and L.M.K. Vandersypen,
   npj Quantum Information **5**, 29 (2019).

1. *Design and low-temperature characterization of a tunable microcavity for diamond-based quantum networks*
   S. Bogdanović, S.B. van Dam, C. Bonato, L.C. Coenen, **A.M.J. Zwerver**, B. Hensen, M.S.Z. Liddy, T. Fink, A. Reiserer, M. Lončar and R. Hanson,
   Applied Physics Letters **110**, 171103 (2017).

## CONFERENCE PROCEEDINGS

3. *Si MOS and Si/SiGe quantum well spin qubit platforms for scalable quantum computing*
   R. Pillarisetty, T.F. Watson, B. Mueller, E. Henry, H.C. George, S. Bojarski, L. Lampert, F. Luthi, R. Kotlyar, O. Zietz, S. Neyens, F. Borjans, R. Caudillo, D. Michalak, R. Nahm, J. Park, M. Ramsey, J. Roberts, S. Schaal, G. Zheng, T. Krähenmann, M. Lodari, **A.M.J. Zwerver**, M. Veldhorst, G. Scappucci, L.M.K. Vandersypen, J.S. Clarke,
   In 2021 IEEE International Electron Devices Meeting (IEDM), (IEEE, San Francisco, 2021).

*These authors contributed equally to this work.

2. *High Volume Electrical Characterization of Semiconductor Qubits*
   R. Pillarisetty, H.C. George, T.F. Watson, L. Lampert, N. Thomas, S. Bojarski, P. Amin, R. Caudillo, E. Henry, N. Kashani, P. Keys, R. Kotlyar, F. Luthi, D. Michalak, K. Millard, J. Roberts, J. Torres, O. Zietz, T. Krähenmann, **A.M.J. Zwerver**, M. Veldhorst, G. Scappucci, L.M.K. Vandersypen and J.S. Clarke,
   In 2019 IEEE International Electron Devices Meeting (IEDM), pp. 31.5.1-31.5.4 (IEEE, San Francisco, 2019).

1. *Qubit Device Integration Using Advanced Semiconductor Manufacturing Process Technology*
   R. Pillarisetty, N. Thomas, H.C. George, K. Singh, J. Roberts, L. Lampert, P. Amin, T.F. Watson, G. Zheng, J. Torres, M. Metz, R. Kotlyar, P. Keys, J.M. Boter, J.P. Dehollain, G. Droulers, G. Eenink, R. Li, L. Massa, D. Sabbagh, N. Samkharadze, C. Volk, B.P. Wuetz, **A.M.J. Zwerver**, M. Veldhorst, G. Scappucci, L.M.K. Vandersypen and J.S. Clarke,
   In 2018 IEEE International Electron Devices Meeting (IEDM), pp. 6.3.1-6.3.4 (IEEE, New York, 2018).

## NON-SCIENTIFIC PUBLICATIONS

3. Quantumfysica op grote schaal, *Nederlands Tijdschrift voor Natuurkunde*, in press

2. Proefjes, *Nederlands Tijdschrift voor Natuurkunde*, maart 2021

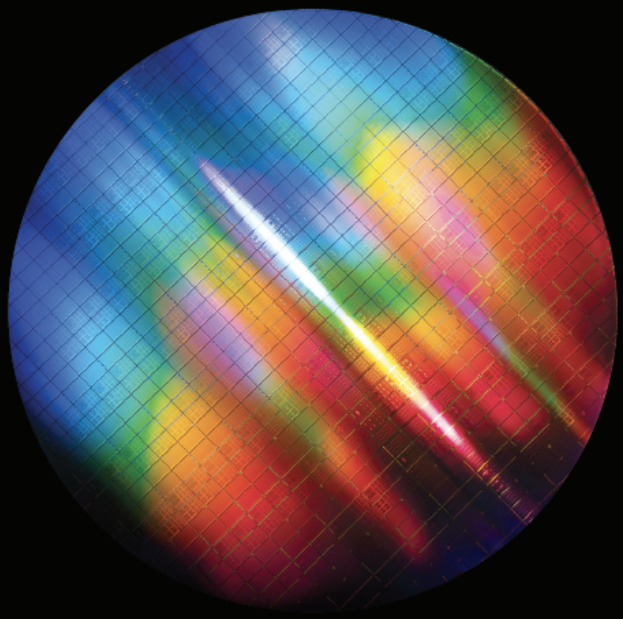
1. Several blogposts, *Bits of Quantum, QuTech blog*, april 2019 - now

## AWARDS

1. Scientific Poster Award, Physics@Veldhoven, 2022

*If you want to view paradise,*
*Simply look around and view it,*
*Anything you want to, do it,*
*Want to change the world,*
*There is nothing to it.*

[Willy Wonka]



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