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Embedded High-Density Trench Capacitors for Smart Catheters

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***Abstract*—Our work presents embedded high-density oxide-nitride-oxide (ONO) trench capacitors for power supply decoupling in the next generation of smart catheters. These millimeter-scale smart catheters are using a novel integration platform, Flex-to-Rigid (F2R). In the F2R platform, various functional modules are fabricated or assembled on thin silicon islands. They are connected by flexible interconnects and can be folded into arbitrary shapes to facilitate small form-factor integration. Trench decoupling capacitors have the advantage of being integrated into the thin silicon islands of F2R to reduce the parasitic inductances and space consumption. Additionally, their small surface openings can be closed by layer deposition to enable follow-up processes on the closed-up surface. For demonstration, high aspect ratio (1.1:25 and 1.2:30) ONO trench capacitors with total areas of 300x300 µm^2 and 1000x1000 µm^2 are fabricated on planar wafers, and a 700 nm and a 1 µm thick plasma-enhanced chemical vapor deposition (PECVD) SiO_2 layers are deposited to test the trench closing process. The F2R compatible ONO trench capacitors have capacitance densities of 6.17 nF/mm^2 and 10.12 nF/mm^2, combined with breakdown voltages ranging from 28 to 30 V.**

Keywords—Trench Capacitors, smart catheters, HAR (High Aspect Ratio), intravascular ultrasound (IVUS) catheter, Flex-to-Rigid (F2R), micro-assembly.

I. INTRODUCTION

With 17.8 million deaths in 2016, cardiovascular diseases (CVDs) have become one of the leading causes of death [1]. Fortunately, most of the CVDs can be well diagnosed and treated by minimally invasive procedures, where smart catheters with imaging and sensing functions are the "eyes and ears" of the cardiologist.

Angioplasty, also known as "stenting," is one of the most common minimally invasive procedures to treat CVD. Before the stenting procedure, a guidewire is inserted along the artery to guide the direction into the diseased coronary artery. To determine the dimension and the position of the required stent, the cardiologist may opt to slide an IVUS catheter over the guidewire, reaching the point of intervention (Fig.1 (a))[2]. The IVUS catheter has a smart tip on its distal end, which includes arrays of ultrasound transducers and application-specific integrated circuits (ASICs). The high-frequency ultrasound transducers create radial cross-section images of the diseased coronary artery. With specific image processing techniques, 3D images can be generated to inspect the stenosis and to allow for optimal stent selection.

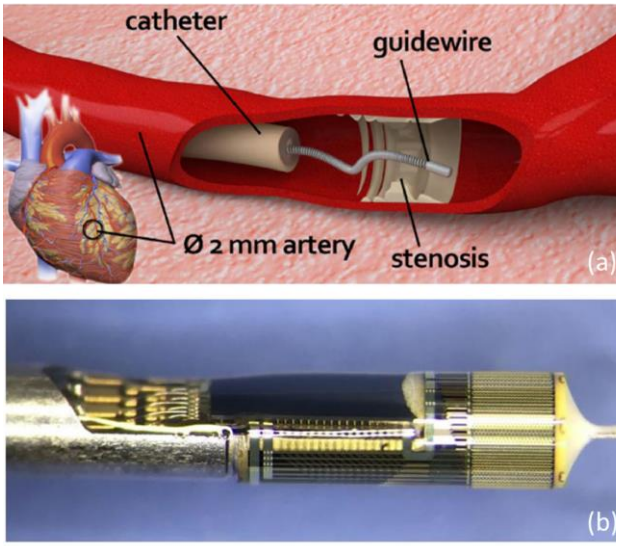

Fig. 1 (a) A guidewire is inserted along the artery, reaching the point of intervention, and the IVUS catheter is slid over the guidewire [2]. (b) Smart tip of the IVUS catheter developed by Philips Research.

Fig.1 (b) presents the smart tip of the IVUS catheter. It has a cylindrical shape with a diameter of around 1 mm and a length of a few millimeters. It contains a cylindrical micro-electro-mechanical system (MEMS) CMUT ultrasound transducer array, several ASICs for data management, capacitors for power supply decoupling, and other electrical passive components. One of the main challenges is to integrate all the modules above into the millimeter-scale smart catheter tip. This integration challenge applies to other smart catheters as well, which hampers their further miniaturization and multi-functional integration. Conventional PCB and flex-foil integration can easily exceed the available space budget. Therefore, new technology was developed to enable miniaturized heterogeneous integration, which not only guarantees reliable electrical interconnections but also can be mass-produced.

In the next section of this paper, we introduce this integration platform, Flex-to-Rigid (F2R). The idea of integrating trench capacitors in F2R is also introduced there. In the third section, the process development for high aspect

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ratio ONO trench capacitors on planar wafers is discussed. The closing of the trenches will be explored. Finally, the electrical properties of the trench capacitors that fabricated on planar wafers will be presented.

II. Flex-to-Rigid (F2R) and Trench Capacitor Integration

A. F2R integration platform for smart catheters

The novel micro-fabrication integration platform Flex-to-Rigid (F2R) has been developed for system integration in smart catheters [3]. The F2R platform contains multiple individual thin silicon islands that are connected by flexible interconnects. Various functional modules or components can be fabricated or assembled onto the thin silicon islands. Due to the flexible interconnections, the thin silicon islands can be folded into arbitrary shapes to facilitate small form-factor integration in smart catheters.

The general process steps of the F2R platform are introduced in Fig. 2. The starting substrate is a silicon on insulator (SOI) wafer with a 40 µm thick device layer and a 380 µm thick handle layer. The F2R process begins with the deep reactive ion etching (DRIE) of trenches into the device layer, landing on the buried oxide layer of the SOI wafer to define the outline of each of the silicon islands. The hard etch mask for this trench etching is a patterned 700 nm thick PECVD SiO_2 layer. Next, the isolation trenches are closed by another thick PECVD SiO_2 layer deposition [4]. Due to the closure of the isolation trenches, the planar wafer surface allows further manufacturing of electrical devices, such as MEMS components on the isolated silicon islands (Fig. 2(a)). The polymer-metal-polymer flexible interconnects are then fabricated to connect electrical devices on different islands (Fig. 2(b)). To release the thin silicon islands, a DRIE step is applied from the backside of the wafer to remove the silicon underneath each thin silicon islands (Fig. 2 (c)). After the F2R process, bare die ASICs can be flip-chipped, and discrete electrical components such as capacitors can be assembled on the silicon islands. Finally, the thin silicon islands are wrapped and folded into the desired shape to fit into the tip of the smart catheters (Fig. 2(d)).

B. Trench capacitor integration in F2R

Capacitors for power supply decoupling are essential components in the smart catheter integrated systems. The current solution is to flip-chip surface-mounted discrete capacitors onto the thin silicon islands in the F2R platform. However, the large dimensions of these discrete capacitors hamper the miniaturization of the smart catheters. Moreover, the assembly of the discrete capacitors introduces parasitic inductances that imperil their electrical performance.

The trench capacitor is known for its high capacitance density [5]. Additionally, its small surface opening makes it possible to close the trenches from the top and enables follow-up processing. To integrate the trench capacitors in the F2R process, trench capacitors are preferred to be first fabricated on the SOI wafer and then be closed by a 700 nm thick PECVD SiO_2 layer deposition. This SiO_2 layer can be directly used as the isolation trench etching hard mask to start the F2R process. The trench capacitors can be embedded into the thin silicon islands where the ASICs will be flip-chipped onto, which can significantly reduce the parasitic inductances caused by long interconnect connections as well as offers a significant space reduction.

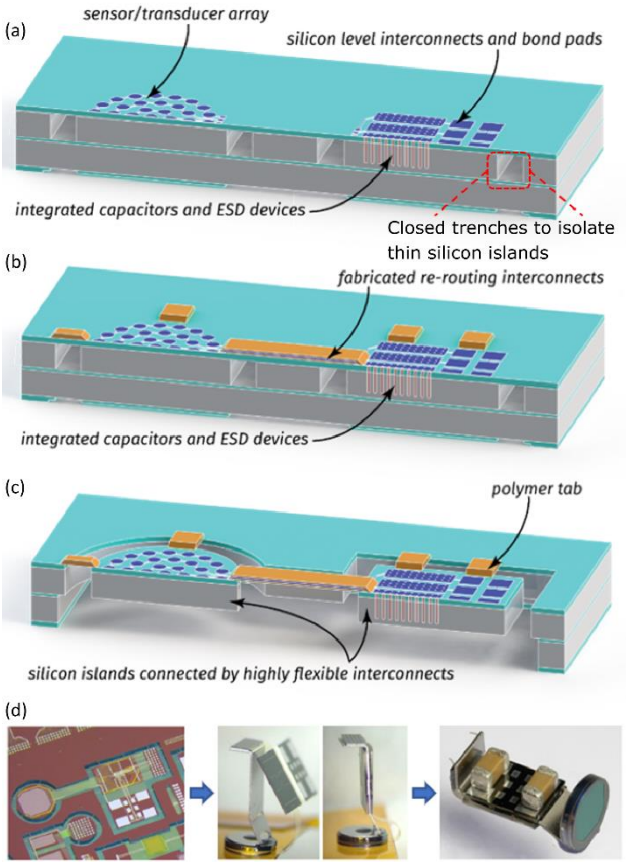

Fig. 2 Flex-to-Rigid (F2R) platform process flow for minimally system integration. (a) Etch and close isolation trenches for the thin silicon islands, then fabricate electrical devices on planar wafer surface; (b) Fabricate flexible interconnects to connect all the electrical systems; (c) Release F2R structure by removing the silicon underneath each thin silicon islands; (d) Release F2R structures and assemble into arbitrary shapes.

III. Fabrication of Trench Capacitor Demonstrators

The trench capacitor demonstrators for F2R integration are fabricated on planer wafers for proof of concept. To fit in the thin silicon islands of F2R, the depth of the trench capacitors should be below 40 µm, and the opening of the trenches needs to be as small as possible to enable trench closure. Therefore, the process for high aspect ratio (HAR) trench capacitors and methods for trench closure needs to be developed. After the fabrication of the trench capacitors, we perform the trench closing test by depositing a PECVD SiO_2 layer on the trench openings followed by SEM inspection.

A. Process flow for trench capacitors

A schematic representation of the trench capacitor process is shown in Fig. 3. The fabrication starts with a highly doped n-type silicon substrate that functions as the bottom electrode of the trench capacitor. First, a 700 nm thick PECVD SiO_2 layer is deposited and patterned by the trench etching mask, creating SiO_2 hard etch mask with pore diameters of 1 µm and 1.1 µm. The pores from the SiO_2 mask are then DRIE etched into the doped silicon substrate to form trenches. The HAR trench etching recipe that was developed will be described in the next sub-section. The SiO_2 mask is subsequently removed by wet etching and followed by an oxygen plasma 45 minutes at 130°C to remove passivation residues from the trench

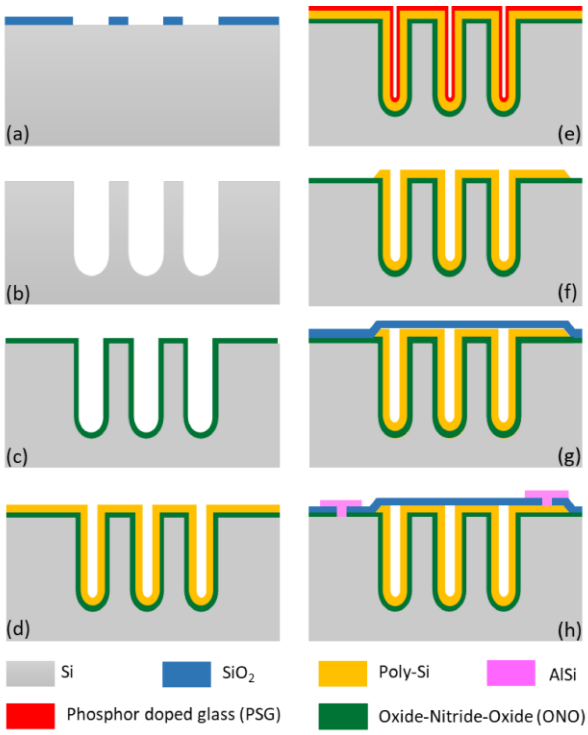

Fig 3 Process flow for embedded high-density trench capacitor. (a) Pattern SiO2 mask for trench DRIE; (b) DRIE etch HAR trenches; (c) Deposit Oxide-Nitride-Oxide (ONO) dielectric layer; (d) Deposit poly-Si as the top electrode; (e) Deposit phosphor doped glass (PSG) and anneal to dope poly-Si; (f) Remove PSG and pattern poly-Si, create slope on the poly-Si edge; (g) Deposit SiO_2 to close trench; (h) Etch SiO_2 landing on substrate and poly-Si, deposit and pattern metal contact.

etching step inside the deep and narrow trenches. The trench etching process also introduces undesired silicon scallops on the sidewall of etched trenches that will jeopardize the breakdown voltage of the trench capacitors. The unwanted silicon scallops can be reduced by thermal oxidation and wet etching steps, but unfortunately, cannot be removed entirely.

The next step is to deposit the ONO dielectric layer in the trenches. The ONO dielectric layer of our fabricated trench capacitors consists of a 5 nm thermal oxide layer, a 15 nm low-pressure chemical vapor deposition (LPCVD) silicon nitride layer, and a 30 nm LPCVD TEOS layer. The thermal oxidation and the LPCVD processes guarantee proper layer coverages inside the HAR trenches. The thickness of each dielectric layer can be adjusted according to the desired capacitance density and breakdown voltage. A 300 nm thick layer of polycrystalline silicon (poly-Si) is deposited on the dielectric layers as the top electrode of the capacitor. To reduce the series resistance of the top electrode, an 85 nm thick phosphor doped glass (PSG) is deposited as a solid dopant source, and a 30 min annealing step at 1000 °C migrates the dopant atoms from the PSG into the poly-Si. The PSG layer is removed by buffered HF (BOE7:1), and poly-Si sheet resistance of around 1.1 mΩ·cm is be obtained after the doping process.

To pattern the top poly-Si electrode, 1.3 µm positive photoresist is coated onto the wafer. Because of the sub-micron diameter of the trench openings after the dielectric and poly-Si deposition, 1.3 µm positive photoresist is thick enough to cover the trenches during resist spinning. The patterned photoresist is then hard-baked to create a slope on the edge. This slope is transferred into the poly-Si during the dry etching process to provide better step coverage for the follow-up processes. Again, an oxygen plasma for 45 minutes at 130°C is applied to remove the photoresist residues inside the trenches.

A 700 nm thick PECVD low-stress SiO2 layer is subsequently deposited to close the trenches. Next, contact openings are dry-etched through the closing SiO2 layer, landing on the Si substrate and the poly-Si. Finally, 1 µm AlCu1% is deposited and wet-etched to make contact with the top and bottom electrodes.

B. Development of HAR trench etching process

The HAR trench etching step is the bottleneck in the whole trench capacitor process. It is a Bosch etching process and each etching cycle includes alternating introductions of the etching phase, the deposition phase, and the boost phase. It starts with the etching phase, where the etching target, silicon substrate in our case, is isotropically etched. During the deposition phase, a thin Teflon-like passivation film is deposited on the isotropically etched surface. The anisotropic etching in the boost phase removes only the bottom part of the passivation film, thereby leaving the sidewall protected and allowing the new etching phase to continue etching deeper [6].

The SiO_2 mask for trench etching has pores with diameters of 1 µm & 1.1 µm. The small trench diameters limit the in-outflow of the reactive ions or radicals during DRIE etching and also cause the etching species to collide. The collision of the etching species leads to unwanted horizontal etching inside the trenches and hence results in rough sidewalls and uneven width of the trenches. The etching recipe is therefore split into two parts, a "start DRIE" transfers the trench diameter from the SiO_2 mask into silicon. This is followed by a "main DRIE" to complete the remainder of the trench etching.

To transfer the oxide hard mask into silicon, the DRIE process usually starts with the anisotropic etching cycle and results in around 200-300 nm under-etch. The "start DRIE" part is aiming to minimize this under-etch caused by the anisotropic etching cycle. Bias power, the power to accelerate the ions bombarding the etch target, is a crucial parameter in the DRIE etching cycles. Sufficient bias power is necessary to break through the passivation layer from the deposition phase, while excessive bias power results in large unideal under-etch.

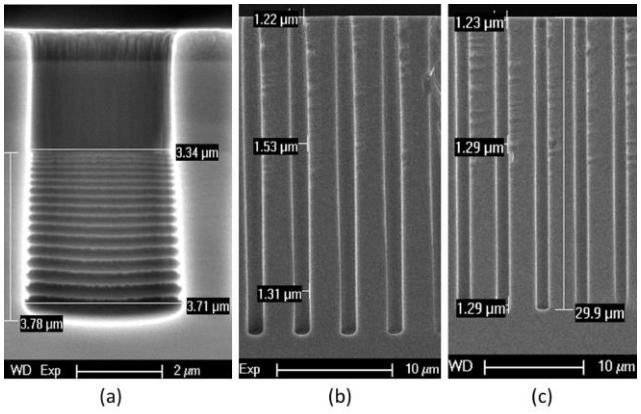

Fig.4 SEM images of the trench etching tests (a) Cross-section image of the ramped-up bias power test. 30 etching cycles were applied, only 20 scallops can be identified in the silicon; (b) "Belly" trenches etched before the optimization in the etching cycles, the trenches are wider in the middle; (c) trenches etched with optimized HAR recipe, without unwanted horizontal etching, and minimized trench wall roughness.

The balancing of the bias power on under-etch is investigated. Thirty etching cycles with ramped up bias power are applied to break through and etch into the silicon. Fig. 4 (a) shows the cross-section SEM image of the ramped-up bias power test. The top part is the SiO_2 mask, and the bottom part has the scallops etched into silicon. Only 20 scallops are identified from the cross-section image, which indicates that the bias power was insufficient to break through the passivation layer during the first ten etching cycles. The 15th cycles show an under-etch of around 100 nm, and the later etching cycles give an under-etch of 200-300 nm. Therefore, the bias power corresponded to the 15th cycle is chosen.

The challenge for the "main DRIE" part is the control of the etching species. We optimized the etching recipe so that the etching species could flow in and out freely during the etching cycles, which reduces the unwanted horizontal etching caused by the species collision. A comparison can be seen from Fig.4 (b) and Fig. 4 (c). Fig. 4 (b) shows the "belly" trenches etched before optimization. The top and bottom of the trench are 1.22 µm and 1.31 µm, while the middle of the trench is around 300 nm wider because of the unwanted horizontal etching. In Fig. 4 (c), the "belly" is significantly reduced after the optimization. The horizontal etching can also affect the roughness of the trench wall. Lower processing temperature is chosen to provide a thicker passivation layer during the etching process and protect the trench wall from the collision effect.

The trenches are finally etched with the "start DRIE" and the "main DRIE" combined recipe. For SiO_2 masks with pore diameters of 1 µm and 1.1 µm, the etching recipe results in trenches with a diameter of 1.1 µm, a depth of 25 µm, and trenches with a diameter of 1.2 µm, a depth of 30 µm. The roughness of the trench wall can be further optimized by the subsequent thermal oxidation step in the process.

C. Closing of the trench capacitors

As explained previously, the fabricated trench capacitors are preferable to be closed by a 700 nm low-stress PECVD SiO2 layer. The closure test is carried out on the capacitors with trench diameters of 1.1 µm and 1.2 µm. After the dielectric and poly-Si deposition inside the trenches, the openings left to be closed are around 350 nm and 480 nm respectively. Fig. 5 shows SEM cross-section images of the closure test. The 700 nm PECVD SiO2 layer is not sufficient to close the openings. The 1.1 µm diameter trench capacitors still have a gap of around 75 nm, and the 1.2 µm diameter trench capacitors still have a gap of around 188 nm. To proof the trench closure concept, a 1 µm PECVD SiO2 layer is deposited to close the 1.1 µm diameter trench capacitors (Fig. 5(c)).

A thicker PECVD SiO2 layer would be the most natural solution, but the thicker SiO2 layer interferes with the remainder of the F2R process. One solution is to have a thicker poly-Si layer as the top electrode, which will result in smaller openings to be closed. However, the PSG deposition for poly-Si doping also needs a sufficiently wide opening for a uniform deposition inside the trenches. Further tests are required to define the optimal poly-Si thickness. Ideally, in-situ doped poly-Si deposition can also solve the problem, but it requests specific deposition tools. Another solution is to add an extra poly-Si or LPCVD TEOS layer to narrow down the openings further after the PSG is removed, but this additional layer also introduces more residue stress issues.

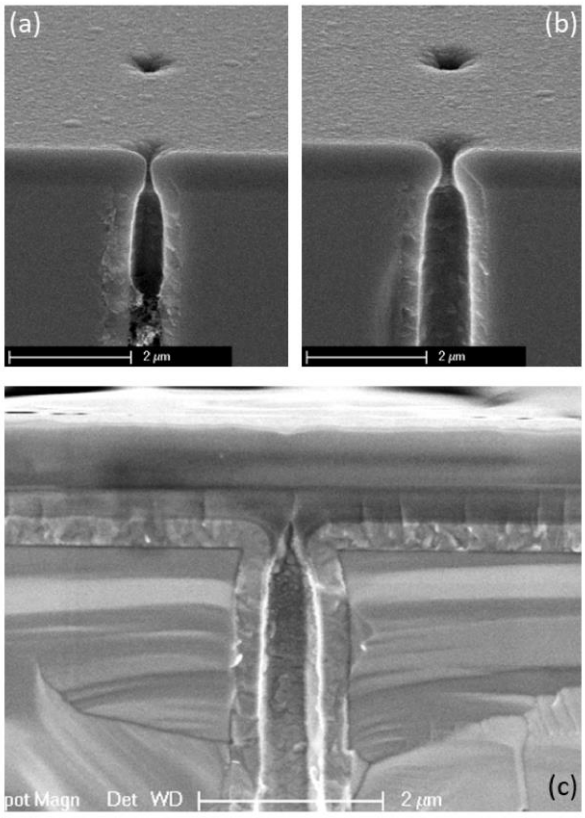

Fig. 5 SEM cross-section images of (a) 700 nm PECVD SiO_2 deposited on 1.1 µm diameter trench capacitors, (b) 700 nm PECVD SiO_2 deposited on 1.2 µm diameter trench capacitors, and (c) 1 µm PECVD SiO_2 closing the 1.1 µm diameter trench capacitors.

I. RESULTS & DISCUSSION

ONO trench capacitors with trenches of Ø1.1 µm/ 25 µm in-depth and ONO trench capacitors with trenches of Ø1.2 µm/ 30 µm in-depth are fabricated on planer wafers. The trenches were designed on a pitch of 4 µm, with total capacitor areas of 300x300 µm^2 and 1000x1000 µm^2. Flat capacitors with the same total capacitor areas are produced for comparison. Fig. 6 shows an SEM cross-section image of a Ø1.2 µm trench capacitor with all deposited layers before the trench closing step. The SEM image shows that the 100 nm PSG layer, the 300 nm poly-Si, and ONO dielectric layers all have sufficient and uniform coverage inside the trench surface and the trench corners.

The electrical characterization results are presented in Fig. 7. The C-V characteristics of the fabricated capacitors were carried out at 10 kHz. Compared with a capacitance density of 0.925 nF/mm^2 for the flat capacitors, the Ø1.1 µm & Ø1.2 µm trench capacitors have a capacitance density of 6.17 nF/mm^2 and 10.12 nF/mm^2 respectively. I-V characterization was performed to study the breakdown voltage of the capacitors. The Ø 1.1 µm trench capacitor with total areas of 300x300 µm^2 and 1000x1000 µm^2 have breakdown voltages of 32 V and 28.5 V respectively. In comparison, the 300x300 µm^2 and 1000x1000 µm^2 flat capacitors have breakdown voltages of 41 and 36 V, respectively. In general, the capacitors with a larger total area have lower breakdown voltage, and the trench capacitors have lower breakdown voltage compared to the flat capacitors.

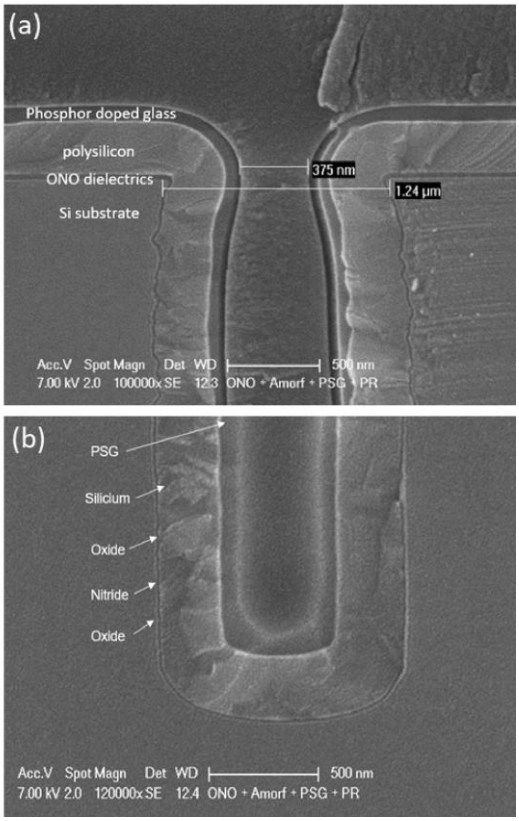

Fig. 6 SEM cross-section image of (a) top part and (b) bottom part of the Ø1.2 µm/ 30 µm trench capacitor with all deposited layers before the PSG removal and trench closing step.

There are a few possible explanations for the breakdown voltage performances. The capacitors with larger total areas have larger functional areas so that the chance for a defect in the dielectric layers is increased, hence resulting in lower breakdown voltages. Trench capacitors not only have larger functional areas but also have complicated topographies. Sharp corners of trench openings, bottom corners inside trenches, and the roughness of trench walls all contribute to lower breakdown voltages. Process optimizations to reduce the non-ideal topographies in the trench capacitors are possible measures to improve the breakdown voltage.

II. CONCLUSION

A novel platform F2R for smart catheter integration is introduced. To integrate decoupling capacitors in F2R, a HAR trench etching recipe is created to achieve a maximum aspect ratio of 1.2:30. The Ø1.1 µm and Ø1.2 µm trench capacitors were not closed by the desired 700 nm thick PECVD SiO_2 layer. However, closing the trench capacitors with 1 µm thick PECVD SiO_2 proves the trench closing concept and further development is needed. The capacitance density of trench capacitors has increased a factor of 11 compared with flat capacitors, and breakdown voltages of the trench capacitors are around 30 V.

Future work will focus on further improving the breakdown voltage and the capacitance density, optimizing the trench closing process, and assessing the stress introduced by trench capacitors in the thin silicon island of the F2R platform.

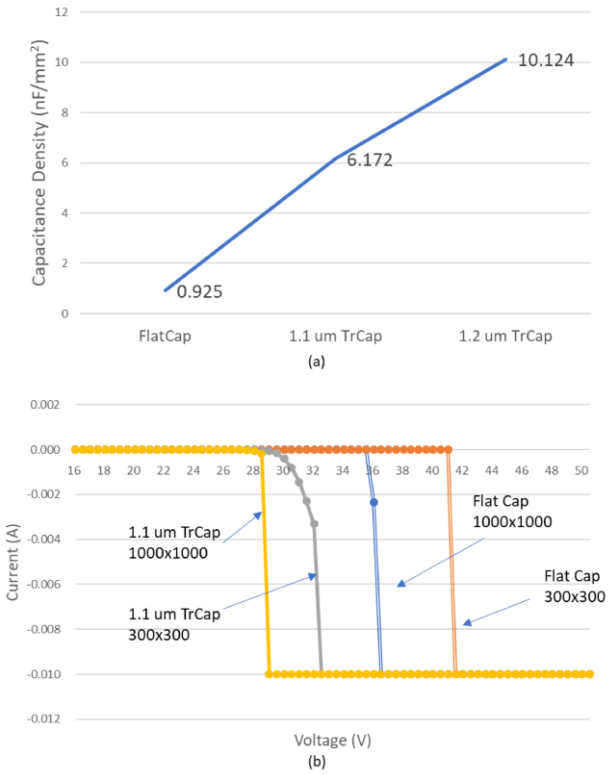

Fig. 7 Electrical characterization of ONO Trench Capacitors vs ONO Flat Capacitors. (a) Capacitance density (nF/mm^2) of fabricated flat capacitor, trench capacitor with Ø1.1 µm trenches and trench capacitor with Ø1.2 µm trenches; (b) Breakdown voltage of 1000x1000 µm Ø1.1 µm trench capacitor, 300x300 µm Ø1.1 µm trench capacitor, 1000x1000 µm flat capacitor and 300x300 µm flat capacitor; Ø1.1 µm and Ø1.2 µm trench capacitors share similar breakdown characteristics.

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