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Xiao, Yidi ; Rivandi, Hassan; Costa, Tiago L.

DOI
10.1109/BioCAS58349.2023.10388859

Publication date
2023

Document Version
Final published version

Published in
Proceedings of the 2023 IEEE Biomedical Circuits and Systems Conference (BioCAS)

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Yidi Xiao
Microelectronics department
Delft University of Technology
Delft, The Netherlands
y.xiao-13@student.tudelft.nl

Hassan Rivandi
Microelectronics department
Delft University of Technology
Delft, The Netherlands
h.rivandi@tudelft.nl

Tiago L. Costa
Microelectronics department
Delft University of Technology
Delft, The Netherlands
t.m.l.dacosta@tudelft.nl

2023 IEEE Biomedical Circuits and Systems Conference (BioCAS) | 979-8-3503-0026-0/23/$31.00 ©2023 IEEE | DOI: 10.1109/BioCAS58349.2023.10388859

***Abstract*—Emerging ultrasound (US) biomedical applications, from battery-powered US imaging to US neuromodulation, demand wearable form factor and power-efficient US transmitters. Fulfilling these specifications demands a high-frequency and power-efficient 2D US phased-array transmitter directly integrated with the ASIC. In such systems, pulsers are the most power-hungry block owing to delivering high-voltage pulses to the US transducers. This paper presents a power-efficient high-voltage pulser to drive a 2D phased-array of piezoelectric transducers. The proposed pulser employs two storage capacitors per channel to save the charge of the US transducer and reuse it in the next phase. Moreover, utilizing a stack of two low-voltage CMOS transistors enables delivering 15-MHz pulses with an amplitude of 10 V to the piezoelectric transducers. The proposed pulser is designed and simulated in 180 nm CMOS technology. The simulation results demonstrate that the proposed pulser reduces the power consumption by 40.9% compared to the conventional class D pulser.**

***Index Terms*—high-voltage pulser, power-efficient driver, stacked architecture, charge recycling.**

I. Introduction

In recent years, new ultrasound (US) biomedical applications have been surfacing, such as ultrasound neuromodulation [1]–[3], battery-powered wireless ultrasound imaging [4]–[6], and ultrasonic power transfer and communication for medical implants [7]–[9]. These emerging applications demand 2D US phased-array transmitters to focus US waves, which not only generate a fine volumetric spatial resolution and high-intensity US focal spot but also allow to change the focal spot location electronically [10]. On the other hand, these US transmitters suffer from poor power efficiency, limiting the performance of these biomedical applications. Thus, a power-efficient 2D US phased array transmitter is needed for further advances in these emerging applications, which can be achieved by improving the electroacoustic conversion efficiency of US transducers and developing low-power ASICs.

Among the building blocks of a 2D US phased-array circuit, shown in Fig. 1, the HV pulsers play a dominant role in the power consumption of the whole ASIC since they dissipate current from an HV power supply [11]. A class D amplifier employing two HV transistors is the most common way to implement an HV pulser. However, this structure not only occupies a large area but also results in higher parasitic capacitance and hence excessive dynamic power consumption [12]. Previous studies [13]–[23] have tried to improve the power efficiency of the HV pulser by adopting various techniques.

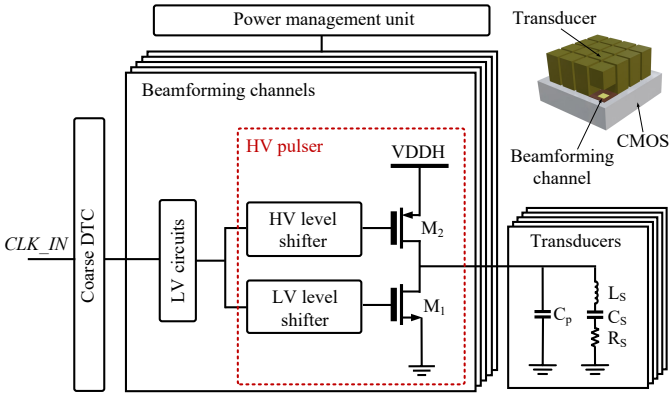

Fig. 1. System architecture of a 2D US phased-array transmitter ASIC.

[13] has utilized a stack of low-voltage transistors to reduce the parasitic capacitance. [14] has used an energy replenishing technique using an inductor that occupies a large area. [15]–[18] have introduced multi-level pulse-shaping methods; however, adopting these techniques to a 2D phased-array results in a large occupied area per channel and hence a huge ASIC. [19] and [20] have used a charge redistribution method by connecting both terminals of the US transducer together. This technique is only suitable for capacitive micro-machined ultrasound transducers (CMUTs) and piezoelectric micro-machined ultrasound transducers (PMUTs), in which both terminals of the transducer are accessible. [21], [22] have utilized a large external capacitor to store the charge of the US transducers for robotic vision and energy harvesting applications. This work aims to improve the power efficiency of the HV pulser by utilizing a charge recycling method suitable for high-frequency phased arrays of piezoelectric transducers. Considering the tradeoff between frequency and budget area per channel, the frequency was set to 15 MHz corresponding to a budget area per channel of 50×50 μm^2 [24]. Two small capacitors per beamforming channel are utilized to save the charge of the US transducer in the discharging phase and reuse it in the next charging phase. As a result, the proposed circuit reduces the power consumption by 40.9% compared to the conventional HV pulser.

This paper is organized as follows: Section II describes the proposed charge recycling technique, and Section III presents the circuit implementation. Section IV provides the simulation results, and Section V concludes the paper.

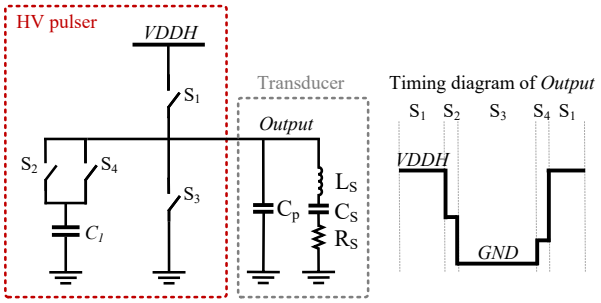

Fig. 2. System-level architecture of the proposed charge recycling technique using one storage capacitor.

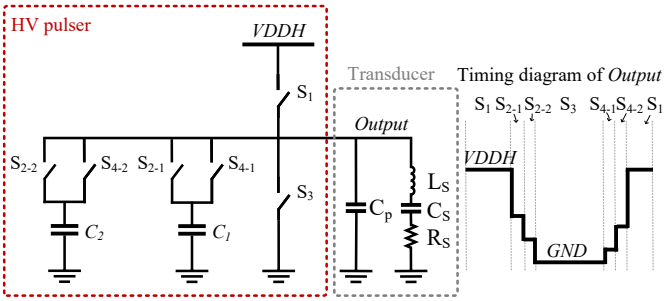

Fig. 3. System-level architecture of the proposed power-efficient HV pulser utilizing two parallel storage capacitors.

II. Proposed Power-Efficient HV Pulser

Since piezoelectric transducers have higher electroacoustic conversion efficiency than CMUTs and PMUTs [10], they improve the overall power efficiency of the 2D US phased-array transmitter. While CMUTs and PMUTs are CMOS-compatible [25], piezoelectric transducers follow a different fabrication and integration process [10]. As a result, one terminal of piezoelectric transducers in the 2D array is connected to their corresponding beamforming channel, while the other terminal of the piezoelectric transducers is connected to a shared ground. Therefore, the current charge redistribution techniques for CMUTs and PMUTs cannot be applied to piezoelectric transducers. This paper aims to design a power-efficient high-voltage pulser for a 2D array of piezoelectric transducers, where only one terminal of the piezoelectric transducers is accessible to the HV pulser.

As shown in Fig. 1, the conventional pulser charges the transducer to $VDDH$ in the first phase and discharges it to the ground in the next phase, suffering from CV^2f caused by the parasitic capacitance, C_p, of the transducer. Although this results in a huge loss, it does not contribute to the electroacoustic conversion [14]. To achieve a power-efficient pulser for piezoelectric transducers, a parallel capacitor to the US transducer can be utilized to save the transducer charge and reuse it in the next phase, as shown in Fig. 2. The principle of the operation is as follows: at first, only S_1 is closed, charging the US transducer to $VDDH$. The total charge stored in the transducer is

$$Q_0 = C_p \times VDDH \tag{1}$$

Where C_p is the parasitic capacitance of the piezoelectric transducer. In the next phase, S_1, S_3 and S_4 are open and S_2 is closed. Then, C_p and C_1 share their charge. Assume that C_1 has an initial charge of Q_1; the charge sharing is as follows

$$Q_0 + Q_1 = (C_1 + C_p) \times V_1 \tag{2}$$

Therefore, the charge stored in C_1 is

$$Q_1 = C_1 \times V_1 = \frac{C_p \times VDDH + Q_1}{C_1 + C_p} \times C_1 \tag{3}$$

And the energy stored in C_1 is

$$E_1 = \frac{1}{2} C_1 \times V_1^2 = \frac{1}{2} \frac{(C_p \times VDDH + Q_1)^2}{C_1 + 2C_p + \frac{(C_p)^2}{C_1}} \tag{4}$$

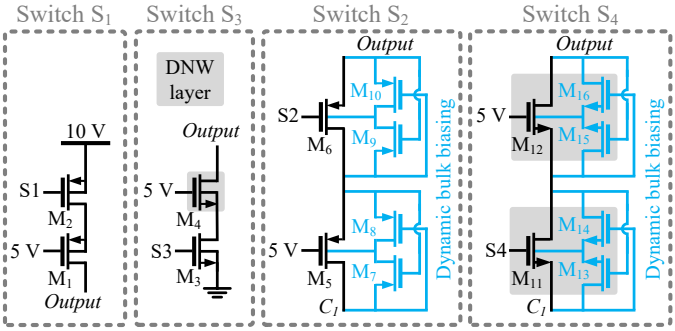

Fig. 4. Circuit diagram of HV switches for proposed power-efficient pulser.

In the third phase, S_3 discharges the residual charge of the US transducer to the ground. Next, like the second phase, S_4 connects the transducer and C_1 together while other switches are open. Then, C_1 shares its charge with C_p, similar to Equation (3). This equation proves that when $C_1 = C_p$, the recycled charge is the highest.

To save power further, more parallel capacitors can be added. As shown in Fig. 3, two storage capacitors are utilized in parallel to the US transducer. According to Equation (3), C_1=C_2=C_p to recycle the maximum charge. In this structure, at first, S_1 charges the transducer to $VDDH$. In the next phase, S_{2-1} save the charge of the transducer to C_1 while other switches are open. Then, the remaining charge of the transducer is shared with C_2 via S_{2-2}. S_3 discharges the transducer to the ground in the following step. Then, S_{4-2} and S_{4-1} transfer the charge of C_2 and C_1 to the US transducer. More charge can be recycled by adding more storage capacitors; however, it results in more occupied area and switching loss. Therefore, the topology of two storage capacitors is chosen to gain the highest power efficiency.

III. Transistor Level Implementation

Conventional class D pulsers utilize HV transistors to deliver HV pulses to the US transducers. However, these HV transistors occupy a relatively large area, posing severe challenges in designing a power-efficient HV pulser for a high-frequency 2D phased-array ASIC. Furthermore, they add large parasitic capacitance to the output node, which degrades the power efficiency. To overcome these problems, this work has utilized standard 5-V CMOS transistors to implement the HV switches required for the proposed power-efficient pulser. Considering the limited area per channel for a 2D US

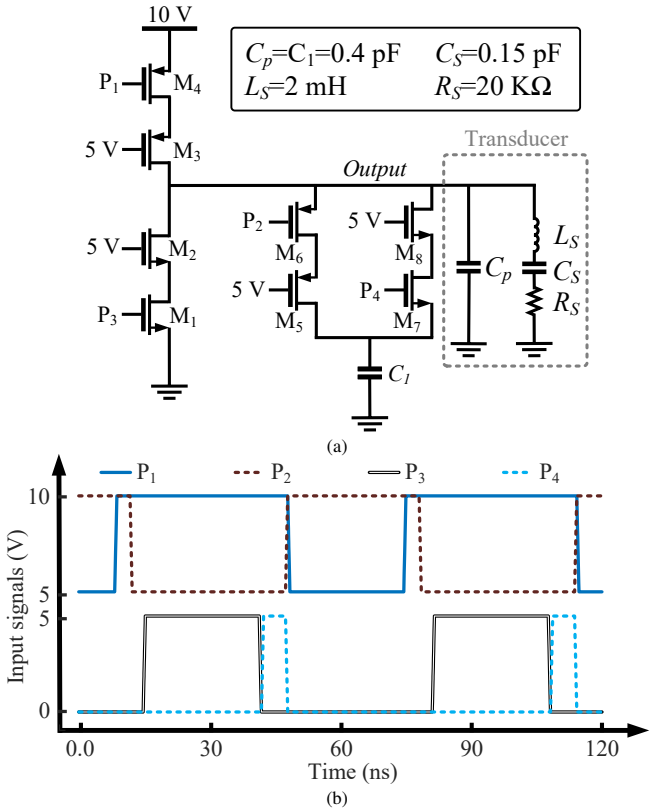

Fig. 5. (a) The schematic and (b) the timing diagram of the proposed HV pulser utilizing one-step charge recycling.

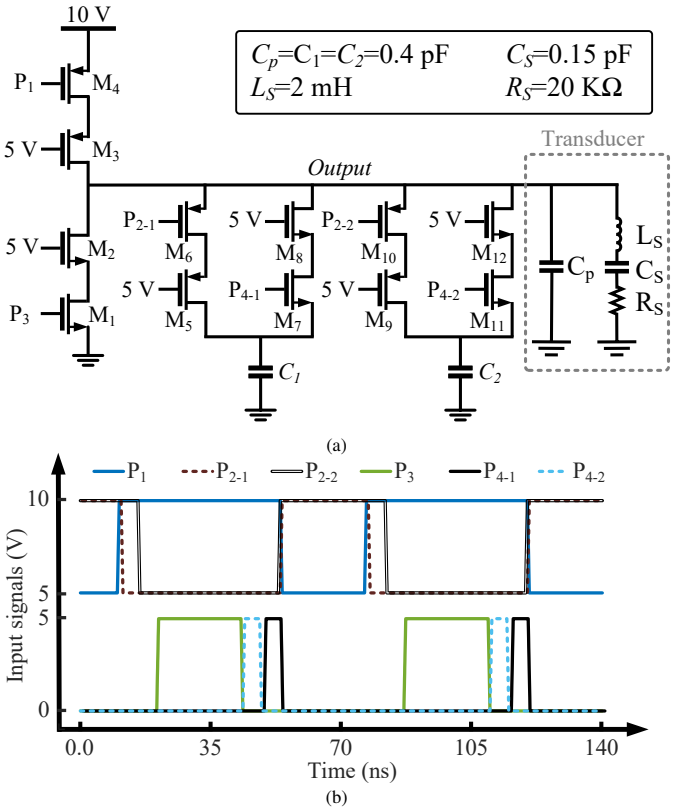

Fig. 6. (a) The schematic and (b) the timing diagram of the proposed two-step charge recycling HV pulser.

phased-array ASIC, the driving voltage of the proposed pulser was set to 10 V. In the proposed structure, Fig. 2, charging (i.e., S_1) and discharging (i.e., S_3) switches are connected to the output node and fixed power rails. Thus, a stack of two PMOS transistors and two NMOS transistors are used to implement S_1 and S_3, to ensure that the V_{GS} and V_{DS} of these transistors never exceed 5 V. Since one terminal of these switches is applied to a fixed potential, the bulks of these transistors are connected to their source, requiring an NMOS transistor in Deep-NW, as depicted in Fig. 4. The charge recycling switches, S_2 and S_4 in Fig. 2, are connected between two variable nodes. The output node and the voltage over C_1 change from 0 to 10 V. To implement S_2, a stack of two PMOS transistors is utilized, as illustrated in Fig. 4. While M_5 is biased to a fixed potential of 5 V, M_6 turns on and off the switch controlled by a 5-10 V pulse. As shown in Fig. 4, S_4 is implemented using a stack of two NMOS transistors, which is controlled by M_7. Moreover, dynamic bulk biasing is utilized to confirm that the bulk of the transistors is connected to a safe potential during low-to-high and high-to-low transitions.

The power-efficient one-step HV pulser, Fig. 2, is implemented utilizing the stacked switches, as depicted in Fig. 5(a). The bulk connection and deep-NW layer have not been shown to avoid complexity. The timing diagram of the proposed circuit is illustrated in Fig. 5(b), describing the principle of the operation. In the first phase, P_1 goes from 10 V to 5 V. As a result, M_4 charges the $Output$ to 10 V. In the next phase, P_1 and P_2 change to 10 V and 5 V. Therefore, M_4 is off, and M_6 is on, discharging C_p to C_1. They share their charges until acquiring the same potential. Then, P_3 moves from 0 to 5 V; thus, the residual charge of the transducer is discharged to the ground. While P_2 is still 5 V to ensure that V_{GS} of M_6 does not exceed 5 V, M_7 prevents discharging of C_1. Finally, P_4 goes to 5 V, allowing C_1 to share its charge with C_p. Consequently, the charge of the transducer is recycled for the next phase, resulting in a power-efficient pulser.

In order to improve the power efficiency further, the HV pulser in Fig. 3 is proposed, which allows recycling more charges using two parallel capacitors. Fig. 6(a) and Fig. 6(b) depicts the circuit diagram of this HV pulser. Similar to the pulser in Fig. 5(a), M_4 charges $Output$ to 10 V in the first phase. Then, M_4 is turned off, and P_{2-1} turns on M_6, which transfers a portion of the transducer's charge to C_1. In the next phase, P_{2-2} turns on M_{10}, and the transducer shares its charge with C_2. By the end of these two phases, the remaining charge of the transducer is discharged to the ground through M_1. Then, the charge over the transducers is transferred back to the transducer using M_{11} and M_7 in two consecutive phases of P_{4-2} and P_{4-1}. In the end, M_4 charges the transducer to 10 V in the next cycle.

Although conventional HV pulser requires one level shifter to turn on and off the HV PMOS, the proposed HV pulsers in Fig. 5(a) and Fig. 6(a) require two and three level shifters which may affect the power efficiency. To avoid excessive power consumption by the level shifters, this work has used low-power latch-based level shifters. Furthermore, beamform-

TABLE I.
COMPARISON OF THIS WORK WITH STATE-OF-THE-ART US HV PULSERS

	[14]	[15]	[16]	[20]	This work
CMOS process	0.18-μm HV	0.18-μm HV	0.18-μm HV	0.18-μm LV	0.18-μm LV
Frequency (MHz)	1	2.5	1	5	15
Driving Vpp (V)	30	30	27	13.2	10
Load	PZT	CMUT	PMUT	PMUT	PZT
Pulser type	charge recycling	multi-level	supply multiplier	charge recycling	charge recycling
Power reduction related to Conv. HV pulser	73.1%	38%	62.9%	32.8%	40.9%
Verification	measurement	measurement	measurement	measurement	simulation

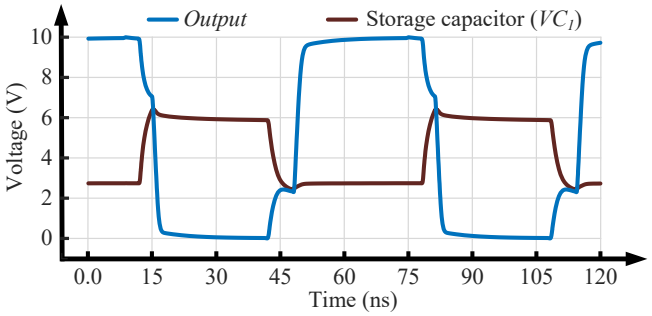

Fig. 7. Transient waveforms of the proposed one-step charge recycling pulser.

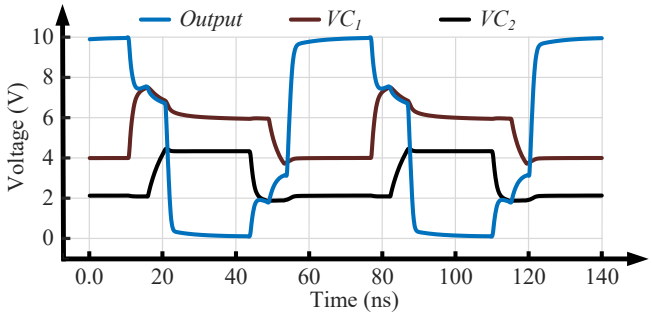

Fig. 8. Transient waveforms of the proposed two-step charge recycling pulser.

ing channels with the same phase in a 2D phased-array ASIC can be applied to a shared level shifter, reducing the effect of the level shifter on the overall power efficiency.

IV. Simulation Results

The proposed HV pulsers have been designed and simulated in TSMC 0.18-μm CMOS technology. To evaluate the functionality of the proposed circuit, four 15-MHz external clocks, as depicted in Fig. 5(b), were applied to the one-step charge recycling HV pulser. Fig. 7 shows the transient output waveform and the voltage of the storage capacitor, revealing the recycling functionality of the proposed pulser. While the conventional HV driver consumes 1.17 mW, the proposed one-step charge recycling HV pulser consumes 901 μW. As a result, the proposed HV pulser shows 29.8% power saving compared with the conventional HV pulser utilizing HV transistors. It is worth mentioning that the power saving of the proposed circuit compared with the conventional HV pulser using stacked architecture is 23.1%.

To validate the functionality of the proposed two-step charge recycling HV pulser, six 15-MHz external clocks were applied to the circuit, as depicted in Fig. 6(b). Fig. 8 illustrates the voltage of the storage capacitors and the HV pulser's output waveform, verifying the proposed circuit's power-saving functionality. The voltage of the first storage capacitor, VC_1, changes between 4 V to 6 V, and the voltage of the second capacitor, VC_2, varies between 2 V to 4 V. In the first phase, the transducer is charged to 10 V. Then, the charge of the transducer is shared with C_1, resulting in a drop in the output voltage from 10 V to 7.5 V. In the next phase, the transducer's charge is shared with C_2, causing a voltage drop from 7.5 V to 6.5 V. After discharging the transducer to the ground, the charge of C_2 and C_1 is shared with the transducer, which increases the transducer's voltage from 0 to 3.1 V in two consecutive phases. The proposed two-step charge recycling HV pulser consumes 830 μW of power, including the power consumed by the required level shifters. Therefore, the proposed HV pulser shows 40.9% and 33.6% power saving compared to the conventional HV pulsers using HV transistors and the stacked architecture.

Table I compares the proposed two-step charge recycling HV pulser with the state-of-the-art power-efficient HV pulsers. The proposed HV pulser operates at 15 MHz, the highest among other works. Furthermore, it delivers 10 V pulses to the piezoelectric transducers, which is sufficient for US stimulation and power delivery application. The proposed two-step charge recycling HV pulser achieves 40.9% power reduction related to the conventional HV pulser, which is higher than the power reduction in [15] and [20]. The techniques presented in [14] and [16] provides better power reduction; however, they are not applicable to a 2D array of high-frequency piezoelectric transducers. In summary, to the best of the authors' knowledge, the proposed US HV pulser constitutes the first power-efficient HV pulser that operates at 15 MHz and can be integrated with a 2D array of piezoelectric transducers, which highly empowers the US neuromodulation and ultrasonic powering preclinical research.

V. Conclusion

This work presents a high-frequency power-efficient HV pulser for US biomedical applications. The proposed pulser utilizes a per-channel two-step charge recycling method to reduce power consumption by 40.9% relative to the conventional US HV pulser. The presented US HV pulser delivers 15-MHz pulses with an amplitude of 10 V to the US transducers. Unlike other works, this method can be applied to a high-frequency 2D array of piezoelectric transducers, resulting in better electroacoustic conversion efficiency and spatial resolution demanded by US neuromodulation and ultrasonic power transfer applications.

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