A CMOS process compatible charge-modulated FGFET based ion sensor for integration into Organ-on-Chip platforms

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Challenge the future

A CMOS PROCESS COMPATIBLE CHARGE-MODULATED FGFET BASED ION SENSOR FOR INTEGRATION INTO ORGAN-ON-CHIP PLATFORMS

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ABSTRACT

Drug development is an entire area of research that partly exploits the developments from biomedical research. Understanding the diseases that affect humanity fatally is critical to our existence. Researchers have studied various molecules and genetic compounds that are responsible for the proliferation of these diseases in the human body. For this purpose, by-far, animal testing has been used most extensively in drug development. Several human physiological models have also been developed to test the efficacy of new therapies. However, it is very difficult to accurately model human diseases in-vitro which has led to failure of several potential drugs.

Consequentially, Organ-on-Chip (OOC) platforms have been developed to serve this purpose. They are specially designed to mimic human organs on a microlevel. Within such controlled microenvironments, biological and electrochemical cues can be well monitored. Stretchable Microelectrode Arrays (SMEA) are commonly used membrane based OOC platforms with suspended electrodes on the stretchable membrane, that are responsible for electrical stimulation. Additionally, several configurations of ion sensors such as Organic Electrochemical Transistors (OECT), Organic Thin-Film Transistors (OTFT) and so on have also been used for integration into OOCs. However, most such devices make use of reference electrodes for biasing the transistors that do not provide for easy integration into standard CMOS fabrication technology. Further, the reference electrodes also can disintegrate and affect the electrolyte over extended periods of biasing.

In this thesis, a reference electrode-less floating gate ion sensor has been proposed that can be realized with low-cost standard CMOS technology. The Charge-modulated Floating Gate FET (FGFET) has been designed, microfabricated and electrically characterized. The device makes use of a standard transistor design with a built-in control capacitor that acts as the reference electrode and sets the working point of the transistor. The gate electrodes are extended on an active sensing area that is bound by a glass cylinder containing the electrolyte. This delimits the rest of the device from the ionic solution. The change in current output of the device in response to ionic charge variation with different concentrations of the electrolyte was tested and the results have been shown here-in. The device shows a sensitivity of 0.4 ampere per molar concentration of electrolyte or 0.4A/M, which is very good for research purposes as was intended in this study. Further, the sensing area is fabricated as a free-standing PDMS membrane with suspended gate electrode extensions, which further validates the potential of the Charge-modulated FGFET to be integrated into stretchable OOC platforms. The easy microfabrication process and good sensitivity of the device presented in this work is an important step towards the integration of ion sensors for OOC applications.

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1

INTRODUCTION

Biomedical research nowadays encompasses a broad scientific field that has the potential to prevent and treat rare and fatal diseases in humans. This general field of research includes many areas of both life and physical sciences. Thus, this synergy enables biomedical researchers to study biological processes and diseases with a vision to develop effective treatments and eventually cures.

Drug development forms a whole area of research that partly exploits the developments from biomedical research. It begins with the understanding of the diseases that affect animals, mostly at the cellular or molecular level. It is by understanding of these disease processes and pathways that targets for new treatments are identified. This could possibly be a protein or another molecular compound that is indispensable for the disease process. These compounds could react with the new treatment drugs, for example, by blocking an essential receptor [1]. Once a potential target has been identified, researchers will then search for a molecule or compound that acts on this target. Historically, plants, fungi as well as marine animals have been studied as they generate compounds that can essentially provide the base for potential drugs. However, in recent times, scientists have also begun to create new molecules for these studies. Genetic and molecular biology studies have played a key role in this front. With current knowledge, it is possible to investigate a large pool of such compounds and streamline them down to just 10 or 20 that could theoretically interfere with diseases. It is after this, that the next step is majorly to confirm whether the drugs and molecules are safe for humans. However, before any foreign molecules are tested on humans, it is necessary to conduct safety tests to determine if the molecules will react with the human body. This is usually done via the means of some computerized pathophysiological models, or by animal testing. Only about half of these new potential compounds make it through this stage. The 5 out of 10 compounds that remain are now ready for human-testing.

Evidently, the discovery and development of new medicines and therapies is a complex process and requires careful scientific research. Pharmaceutical companies, nowadays spend tens of billions of dollars in testing of several potential drugs. Most of this testing techniques rely on in-vitro testing. However, many human diseases are still unable to be accurately modelled in-vitro, limiting understanding and therapy development. In-vitro

testing is limited in its ability to prove the efficacy of new therapies as cells might not react the same way as they would when outside their natural environment.

The failure of in-vitro testng and its subsequent consequences can be demonstrated by the example of Vioxx, a drug that was developed in the year of 1999 [2]. The pharmaceutical company Merck introduced this new arthritis drug after consultation and approval by the Food and Drug Administration (FDA). Coming at a time when arthritis was affecting a massive number of people in and around the world, this drug proved to be a huge success in the pharmaceutical market. More than 80 million prescriptions and 2 million daily users were reported already by the end of September [3]. However, inspite of this, Merck voluntarily decided to call this drug off of the market on September 30, 2004. It was determined, that the drug was known to cause or even induce heart attacks and strokes and a variety of other side-effects. The death toll were estimated to be around 50,000 to even 500,000. Since a large part of the data is derived from drug testing on animals, the corresponding results could not easily be translated onto human patients. Had the drug been tested before using a much reliable method, especially for that of toxicity, this would have improved patient safety and guaranteed quality of human life. It is quite clear that testing on animals is expensive and comes with numerous ethical issues, in addition to the fact that they are not able to mimic human physiology and genomic models well enough to accurately test the effects of these on human life.

The majority of these tests, so far, have relied on bulk optical techniques such as those of immunofluorescence end-point detection, microscopic cell imaging among others. These methods are beneficial to acquire and analyze the information of cell cultured microenvironments [4]. The intrinsic inability of purely optical methods to capture in vivo biological phenomenon is a major limitation in these methods which causes specific data to be missing from measurements. These in addition involve mechanical, chemical and topographical cues. For instance, a more complete view can be easily obtained if contractile stresses, bioelectrical activities, pH level, calcium, potassium and oxygen concentration could be quantitatively measured in a spatio-temporal manner for a culture of heart cells [5]. Monitoring bioelectrical activity of heart cells has been studied by several groups and many of them report several novel approaches to monitor this electrical extracellular activity by using microelectrode arrays in cell cultures [6]. Alternative detection and analysis methods are still necessary to enable the monitoring of some biochemical, physical and mechanical signals within these microenvironments, specifically with a quantifiable and real-time approach[7]. Likewise, an intrinsic limitation is its poor scalability since most of the characterization techniques used by this technology are bulky and so restricting the full integration and mass implementation of the technology [8]. Further, it encompasses several ethical issues, faced by animal testing which are widely contested today. Debate surrounding the breeding of test animals for medical research is increasing day-by-day. It is also an expensive process, partly because of the necessary testing required for human toxicity and efficacy of drugs. Such limitations of current planar, static cell culture systems or animal models result in the high drug failure rates seen in clinical trials, a limitation that can cost pharmaceutical companies billions of dollars.

These issues highlight the urgent need for more physiologically relevant models of human

organs, and have fuelled the development of organs-on-chips. As a result of this, the necessity of developing self-integrated monitoring structures was identified as crucial. Microfabricated Organ-on-Chip (OOC) platforms are such devices that are developed for satisfying this need, and are highly studied in current academia as well as the industry. The end goal is that these models will lead to more accurate detection of toxicity or efficacy problems and reduce the amount of drugs failing in human clinical trials.

1.1. ORGAN-ON-CHIP

Organ-on-Chips are relatively new and novel cell culture platforms that overcome the limitations of conventional drug-testing methodologies. These devices are specially designed to mimic the minimal unit of human organs. To do so, different cell types and tissues are cultured in specially designed microstructures that resemble such particular microenvironments of the human body. Within such controlled microenvironments, biochemical and mechanical cues can be well controlled and monitored. It is to be noted that even for these devices, research is still in a very early stage.

OOC models are potentially valuable for the development of new drug compounds and as drug screening devices [9]. Some reports [10] [11] have also indicated that in-vitro human stem cell based models are, in a few cases, already far more accurate than animal models. iPS technology is a recently developed experimental method that allows in vitro culturing of well defined and reproducible human tissue with a certain genomic profile [12]. This technique is actually beneficial in creating stem cell models which can explain to researchers, the various ways in which human cells would normally respond in-vivo. This would further allow researchers to study investigate the functioning of both healthy and diseased tissues under the influence of new drugs. This would also be far superior to animal models, more ethical and cost-efficient since mass production is possible.

Several OOC models have been studied in the academia. The following subsection offers an insight to some such models.

1.1.1. LUNG-ON-CHIP

The development of new solutions to treat pulmonary diseases has become a goal of primary importance today. Globally, pulmonary diseases are the fifth major cause of death in the world and are soon predicted to become the third by 2020 [13] [14]. In this context, it is critical to be able to develop lung-on-chip models to facilitate newer and better treatments.

The team of Huh *et al.* [14] from the Wyss Institute of Biologically Inspired Design at Harvard were one of the first in the world to have successfully been able to manage to reproduce and subsequently observe the functions of the human body in-vitro or outside the human body. The model fabricated by them has been shown in Fig. 1.1. The lung-on-chip developed trough softlithography comprises of two microchannels separated by a porous membrane. The entire device was fabricated using polydimethylsiloxane (PDMS) and the mebrane covered in collagen for better cell adhesion. This enabled the separation of epithelial cells in contact with air on one side and endothelial cells in contact with nutritions fluid (in lieu of blood) on the other side.

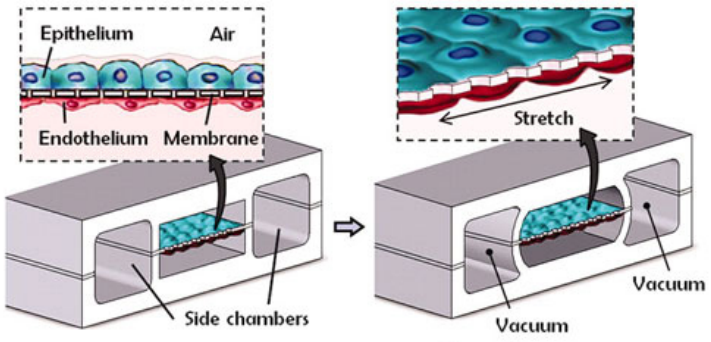


Figure 1.1: Lung-on-Chip as fabricated by Huh et. al. [14]

Further, in order to test the functioning of the chip in reproduction to a normal human lung, Huh *et al.* [14] introduced bacterial cultures in the air flow and white blood cells in the blood flow. Just like in the human body, The inflammatory response of the white blood cells was triggered as they moved to the epithelial cells side to fight the bacteria. However, sensors to detect the barrier movement, or fluid flow, pressure or even migration of the cells haven't yet been integrated in such a device.

1.1.2. BRAIN-ON-CHIP

Brain-on-Chip are modular devices in which the neuronal cells and the device itself follow a close transfer of information with each other. Neuronal stimulation has been achieved with devices that are interfaced with the cell-culture medium directly [15]. The tissue is present in an electrolyte form and contained in a glass vessel on the surface of the device. The device has a voltage-sensitive site, which has several metal electrodes that are inturn connected to the readout circuitry [16]. Micro-electrode Arrays (MEA) have been used commercially in the market for electrical stimulation on the surface of the device. These consist of a 2D array of electrodes branched out from each other with an insulator medium in between. These electrodes serve as monitoring or electrical stimulation structures are key in electrochemical characterization of the brain cells. They provide for a better understanding of the electrical activity of our brain.

Research has also been able to reproduce a small part of the brain, the blood-brain barrier on a chip [17]. This barrier has an essential function, as it protects the brain from all pathogens in the blood flow and only lets through nutrients to the brain. However, it also restricts some active sites from accessing the brain tissue, for example the medicine to treat Parkinson's disease [18]. Hence, in such a case, the development of brain-on-chip is soughtafter as these devices allows to test the fluid flow under physiologically relevant conditions [19]. This mimics the flow of blood and allows the brain cells to properly differentiate and mature. Nowadays, brain-on-chips have proved to be more accurate than static cultures to predict permeability of the blood-brain barrier [18] [20].

Recently, a drug-delivery system for integration into OOC platforms has been fabricated by the Delft University of Technology in collaboration with Philips Research Center [21]. The device fabricated is a PDMS membrane enclosing a microchannel for drug-delivery of the chemical required for cortical spreading depression (CSD) onto a site that houses

the brain tissue. The electrical activity of the brain cells is then studied before and after the drug introduction. However, this electrical monitoring is performed with an external readout circuitry. The integration of sensors for monitoring such electrical acitivity is yet to be realized.

1.1.3. CANCER-ON-CHIP

It has also been made possible nowadays to mimic the metastasis of such tumor cells. The invasion of carcinogenic cells from the main tumor-site in the body to other secondary sites of the organs is called metastasis [22]. It is interesting to note here that a tumor can easily be compared to an organ as it also has a micro-environment which provides the tumor cells with certain biochemical and mechanical stimulation which, in-turn, provides these tumor cells to become cancerous and metastasize into furthermore cancerous cells. This kind of metastasis progression of cancer is a very special phenomenon and most of the factors trigerring it are still unknown to us. Thus, the concept of Organ-on-Chip is of particular interest due to its capability to replicate the tumor micro-environment and also to study the periodic activation of this environment that leads towards the metastasis.

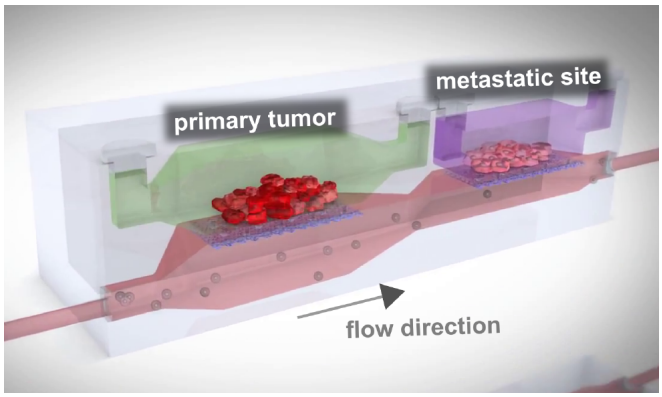


Figure 1.2: Conceptualization of the device [23]. The tumor and metastatic site are separated by a porous PDMS membrane. The direction of movement of the cancer cells is from the tumor to the metastatic site, via the porous membrane that represents the blood-vessels.

An example of this is a device developed by the Eindhoven University of Technology in the form of a multi-chamber microfluidic device [23]. This device enables us to study cancer cell migration through the blood stream, before it finally reaches the second metastatic site, as shown in Fig 1.2. The tumor and the metastatic site are conceived as endothelial cells seperated by a porous membrane. This represents the blood-vessel lining in the human body. This porous membrane is where the transition to cancer and invasion of the blood vessels occurs and is a very important feature of the device as shown in Fig. 1.3.

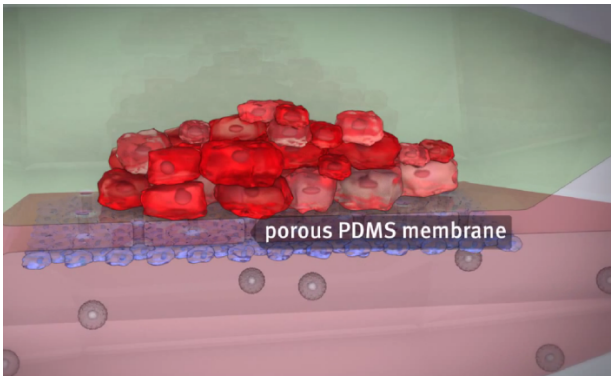


Figure 1.3: Co-culture of 3D tumor cells and a 2D endothelial cell monolayer separated by a porous membrane [23].

As was pointed out for lung-on-chips, it would perhaps be beneficial to integrate sensors in the device, that can give monitor cell behaviour or the fluid flow properties across the porous barrier.

1.1.4. HEART-ON-CHIP

In the mammalian body, the heart is one of the most vital organs. It is responsible for supplying nutrients and oxygen to the organs via the pumping of blood. It has a very important characteristic of autorhythmicity, which is also modulated by the endocrine and nervous systems.

Cardiovascular (CVD) diseases are a condition of the body that fatally affect the heart. CVDn nowadays has become major cause of death globally. It was established in 2012, that 17.5 million people died of CVDs globally. This has sparked a major interest in researchers investigating the cause for these diseases and their subsequent treatment. The need to understand the heart better has lead to the development of heart-on-chip models. With the help of microfabrication technology, this has now turned into a plausible reality. Just like the previous models for drug-testing, these models also allow for in-vitro testing of drugs and pathogens that plague the heart and cause CVDs.

A heart-on-chip is a novel and simple method to reproduce the cardiac tissue in three dimensions and measuring the effects of the organ's exposure to foreign substances. This makes it possible to study the response of cardiomyocytes to external stimuli.

Several physiologically relevant models have been studied for drug and cardiotoxicity screening. In 2014, Xiao Y. *et al.* [24], demonstrated that human embryonic stem cells and rat neonatal derived cardiomyoctyes could be used microfabricate a cardiac biowire bioreactor for pharamceutical drug testing. The spontaneous beating of the biowires could be slowed down by treatment with nitric oxide, carried by the medium into the chamber. There have also been examples of microfluidic devices that generate cardiac-like flow in a continuous closed-culture system [25]. The heart is also a rare organ with active tissues that show tissue contractions. These tissues are known to have a better cardiac differentiation when stimulated by a stretching pulse, as demonstrated by Zhuang et. al. [26].

For drug development, it is also necessary for these devices to be able to respond to chemical stimuli within a varying range of doses. Agarwal *et al.* [27] tested isprotenerol, a medicine used to treat heart failure or bradycardia, on a rat cells based heart-on-chip, in doses between 1nM and 0.1mM. The experiments, although conducted on non-human cells, demonstrate the potential of heart-on-chips to test a wide range of medicinal concentrations.

Moreover, the I-Wire Heart-on-Chip is a device created at Vanderbilt University by the team of Sidorov et. al., [28]. Described more precisely, the team developed a PDMS casting mold and added it into a six-well plate, as shown in Fig. 1.4, with a channel on each side for insertion of titanium anchoring wires. Following this, a 3D cardiac tissue was then engineered and and cultured in this plate using ventricular cells. As explained by them, different types of cells are necessary in order to generate the proper cardiac tissue structure. Hence, they used both cardiomyocytes as well as cells from the the extra-cellular matrix formation. For easier culturing, the cells were placed in a culture medium and within 5-6 days of culture, the cells begun to beat synchronously and within 13-15 days, muscular fibers were formed. The contractions occurring as a result of this, were monitored via the means of an optical microscope with a cantilever probe attached to the condensor of the microscope. The action potential was also measured using electrodes. A silver chloride electrode was used to serve as the reference electrode [28]. Moreover, the anchoring titanium wires were used for voltage stimulation.

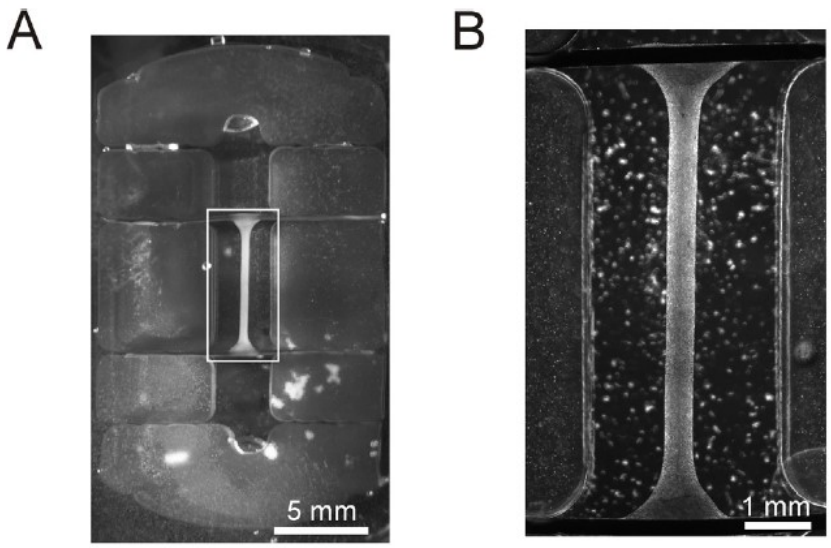
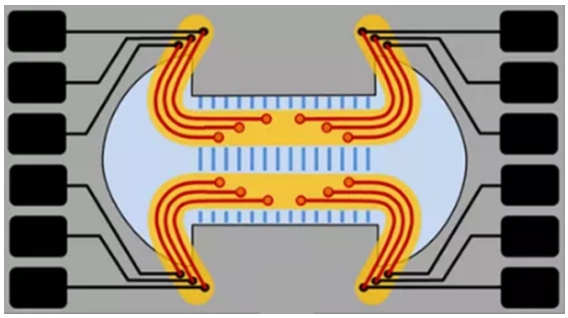


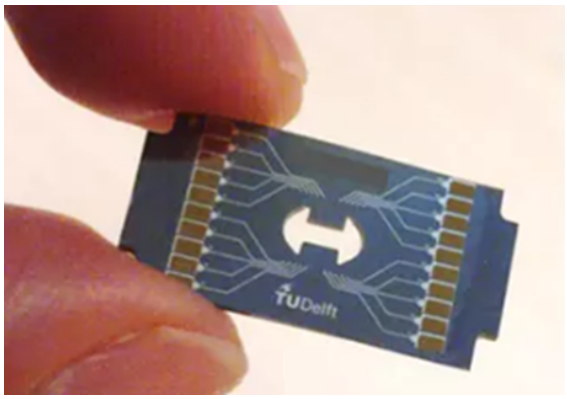
Figure 1.4: A) Six parts PDMS casting mold is obervable [28]. B) Two channels on each side of the culture for adding of wires. These wires allow direct and continuous measurements without the help of external devices [28].

This study was however limited to the use of external electrodes for sensing and monitoring the electrochemical activity of the cells. To accurately measure and model the human body functions, such as the ionic activity occurring when the heart pumps blood to vital organs, this cellular model is not sufficient. This has lead to new investigation in the field of heart-on-chips.

The lack of electrical monitoring techniques for these platforms has recently motivated the development of a robust model with integrated sensing technology. Mostly, nowadays for cardiotoxicity screening, Multi-Electrode-Arrays based devices are fabricated and characterized with human heart cell cultures. In a project by Gaio et. al. [29], the authors have fabricated a low-cost and accurate heart-on-chip device. This concept was developed by the Delft University of Technology in collaboration with the Leiden University Medical Center and Philips Research Center and is called the Cytostretch [29]. It works by addressing certain challenges and to create a more physiologically relevant environment for the heart muscle cells to mature, resulting in a more reliable heart model. The basic model of the platform consists of a stretchable microelectrode-array, made in silicon with polydimethylsiloxane (PDMS) as the flexible substrate for the cells. Titanium nitride interconnects that are stretchable, are fabricated on the thin PDMS membrane. These are meant to connect the electrodes to the bondpads, that are patterned on the edge of the device. Additionally, there are microgrooves that are etched on the PDMS membrane that permit the cells to be aligned in a specific direction only. It has a dog-bone structure, as can be seen in Fig. 1.5. This specifically allows for the straining of the cells in the direction perpendicular to the length of the device. This novelty along with the microgrooves allow for the cells to be aligned in a specific direction on the membrane. This also makes the unidirectional straining of cells possible. Through experiments, it was found that after 3 days of culturing cardiomyocytes on top of the Cytostretch, the cells started beating on top of the stretchable PDMS membrane, signifying good functionality and viability.



(a)



(b)

Figure 1.5: a) Schematic of the Cytostretch device. b) The actual SMEA chip with the electrodes connected to PCB [29].

Thus the cytostretch proved to be a fully microfabricated heart-on-chip device that allows for a dynamic environment for the cell culture through stretching of the PDMS membrane. During the experiments, the Cytostretch device also worked by measuring change in the extracellular field potential of cardiomyocytes to indicate possible heart failure. If the membrane is inflated above the regular value, this mimics increased cardiac activity. Most importantly, this device provided for a platform to integrate sensing electrodes in a flexible membrane thereby better resembling physiological conditions.

1.2. NEED FOR SENSOR-INTEGRATION IN OOCS

The field of OOCs is continuously evolving. Although the Cytostretch already makes up for an OOC with integrated sensing electrodes, there is still a need for more sophisticated sensor integrated OOCs that can provide continuous information about the electrical or chemical activities of cell cultures on the device in real-time. To achieve such a goal, several criteria need to be ensured. One of the key criteria is to integrate these sensors into the devices to monitor the physical and electrochemical characteristics associated with the functioning of OOC models.

1.2.1. MONITORING CHEMICAL GRADIENTS AND ELECTRICAL PARAMETERS

Chemical stimulation is an important parameter that has to be taken in to account to develop and maintain physiologically relevant OOC platforms. Thanks to microfluidic devices integrated with detection platforms, it is possible to control and tune the fluid flow of the chemical agents in such OOC devices. This has been made possible through a microfluidic device that operates with the pressure feedback control from the drug delivery technique in the chip [30], that delivers the drug to the tissue site via a fluid pumping technique. It is also possible to use a small amount of chemicals to generate, measure and control an oxygen gradient inside microfluidic channels [31].

Additionally, measurement of dissolved oxygen (DO), even combined with sensors for pH, glucose and lactate, are important criteria for the development of OOC devices. The first widespread DO sensor configuration commonly adopted was proposed by Wolf *et al.*, [32], consisting of a platinum working electrode as the cathode and a silver chloride electrode as the reference electrode, and anode for detecting the current from oxygen reduction reaction [32]. Several different elements are present in our body in ionic form which regulate our bodily functions on a day-to-day basis. They help regulate body fluids, muscular activity, blood pressure and so on. Electrochemical sensor architecture is getting more and more important nowadays especially with the emergence of various sensor configurations to detect such ions on OOC platforms. Hence, other solutions were considered such as transistor based sensors, for detection of ions. Several optical sensors have also been studied [33] [34], but relying on optical techniques, optrodes suffer from small-range measurements [35].

1.3. SCOPE OF THE THESIS

In a changing scenario of such biomedical electronic devices, considerable effort has been put into the development of more and more transistor-based devices for biosensing and electrophysiological monitoring of electrogenic cells. However, the ability of such devices

to be incorporated in standard CMOS technology has been fairly debatable. Also important is the detection of ions in this regard, as several different ions are present in the human body that regulate our cardiovascular, neural, muscular activities amongst others. The failure of optrodes in the electrochemical measurement regard, has prompted the use of transistor based solutions to sense ions in OOCs. In this context, the goal of the thesis is to develop and integrate a charge-modulated FET based ion sensor (Ca^{+2}, K^{+}, H^{+}) for integration into an OOC platform developed with standard CMOS process technology. The possibility of several transistor-based configurations for the development and integration of an ion sensor into an OOC platform has been studied. Keeping in mind the standard CMOS fabrication process for the sensor relevant, a novel design for such an integratable ion sensor has been proposed, designed, fabricated and characterized.

1.4. OUTLINE OF THE THESIS

Chapter 2 deals with the state-of-the-art and the background technology already available for such sensors. Chapter 3 talks about the design and modeling of the sensor itself. Chapters 4 and 5 are mainly about with the fabrication process and the electrochemical characterization of the device respectively.

2

Ion-sensing Technologies for OOC Applications

Now that the importance of integrating ion-sensing technologies for OOC platforms has been established, it is important to study the different arrangements for sensors for the detection of ions that have been developed in the past. It is important to be able to successfully integrate these ion sensors in standard microfabrication technology for easier mass scale reproduction. Some of the most important configurations in this regard have been made with soft materials where low cost or high-throughput fabrication is desired. Mechanical compatibility with soft tissue is also a very important characteristic that is required. Some of these technologies will be studied in the following section.

2.1. State-of-the-Art

The invention of the transistor in the year 1947 heralded the era of microelectronics [36]. Occupying a particularly major part of the semiconductor manufacturing industry, these miniaturized devices are mainly made of semiconductors, dielectrics and metals[36]. They are usually the core of integrated circuits, which are the building blocks of any electronic device. Organ-on-Chips are no exception to this. Transistor based devices have, and are currently being used as sensors in OOC platforms [37] [38]. However, in addition to this, there are several organic material based designs that are being used to develop these OOCs as well. These are truly multidisciplinary devices, combining both biology with engineering.

2.1.1. (Stretchable) Microelectrode Arrays

The most conventional method that has been used to detect and quantify the bio-electrical activity of cells is the usage of microelectrode arrays. Microelectrode arrays are useful tools in studying the electrophysiology of living cells seeded on the devices. Excitable cells under the influence of electrical stimuli would produce extra-cellular field potentials. These MEAs enable researchers to quantify and map this electrical response [39]. However, MEAs traditionally have been fabricated on rigid substrates. This therefore limits the study of in-situ mechanical stimulation of the OOC device. Thus embedding the electrode array onto the surface of a stretchable membrane enables the application of physiologically relevant mechanical stretch to the cardiomyocytes cultured on the membrane. These devices can

replicate the in vivo stretching and contraction of cells during electrical measurement and also enables in situ maturation of the cultured stem cell derived cardiomyocytes.

Lately, SMEAs have become important tools in biomedical research. As the substrate is no longer rigid, this allows for mechanical stimulation under the presence of electrical stimuli and thus enables better investigation on the mechanobiology of the cultured cell medium. Although the metallic interconnects might be robust in the relaxed state of the membrane, it is also important to check the strain of these electrode interconnects under strain when the membrane bends. This has lead to the study of several alternative materials to fabricate the electrical interconnects in such SMEAs as conventionally metals are more commonly used which are not inherently stretchable [40] [41]. A good example of an SMEA with suspended electrodes is the Cytostretch discussed in Chapter 1. A more detailed image of the Cytostretch has been shown in Fig. 2.1.

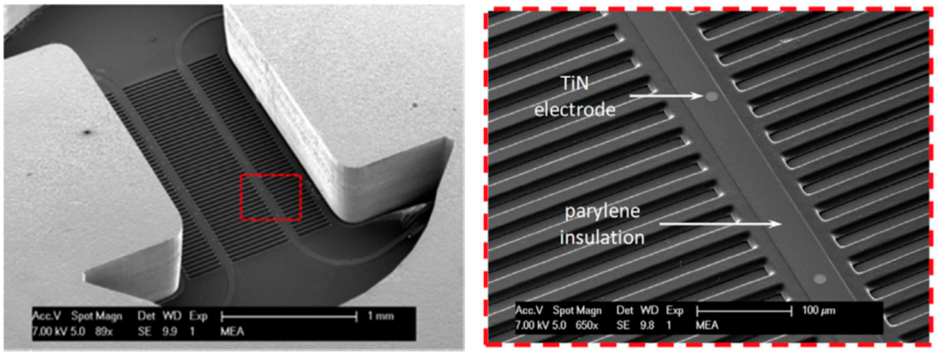


Figure 2.1: The Cytostretch, a conventional SMEA platform as developed by the TU Delft and Philips [29]. a) A SEM image of the Cytostretch chip from the back b) Inset depicts the area highlighted in (a) showing the transversal micro-grooves, the exposed TiN electrodes and parylene insulation of the metal tracks.[29]

Currently, SMEAs are usually fabricated directly on PDMS. Additionally, they use stretchable conducting materials for the electrical interconnects that are not compatible with standard microfabrication techniques [42]. Although, it is possible to fabricate stretchable interconnects by using other conductive materials such as liquid metal alloys and conductive particle doped elastomers, these materials are not suited for standard microfabrication processing technology [39]. It is also possible to design the interconnects in serpentine patterns which can accommodate the strain exerted during membrane stretching and bending. However, they are limited by the fact that they occupy a large surface area on the die and can result in degrading of the surface topography of the device. Since interconnects should minimally alter the surface property of the device, this is not particularly desirable in SMEA fabrication. Additionally, the fatigue lifetime of the interconnects is reduced after repeated bending and stretching of the membrane [39] Thus it would be beneficial to find a way to integrate electrodes into the stretchable membranes in OOCS without altering the main topography of the device as much.

2.1.2. ORGANIC ELECTROCHEMICAL TRANSISTOR

Interest in organic materials and particularly their potential for low-cost fabrication over large areas led to the development of a new type of sensing device design. A particular organic transistor configuration that is of special interest in the context of Organ-on-Chip platforms is the organic electrochemical transistor (OECT). Originally developed by White *et al.* in the 1980s [43], OECTs are planar devices consisting of three electrodes. The source and the drain are connected by a conductive polymer which acts as the channel. The channel and the gate electrode are further separated by an electrolyte which acts as the gate dielectric. The organic semiconductor film is in contact with an electrolyte, in which the gate is immersed. Refer Fig. 2.2.

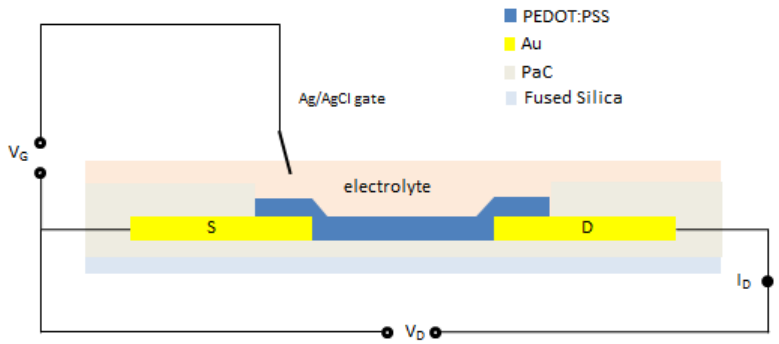


Figure 2.2: A schematic cross-section of a conventional OECT with PEDOT:PSS conductive channel.

The OECT mainly relies on ions that are injected from the electrolyte into the organic film, thereby changing its doping state and hence its conductivity. The operation is controlled by the voltages applied to the gate (V_G) and to the drain (V_D), which are in turn referenced by the source electrode.

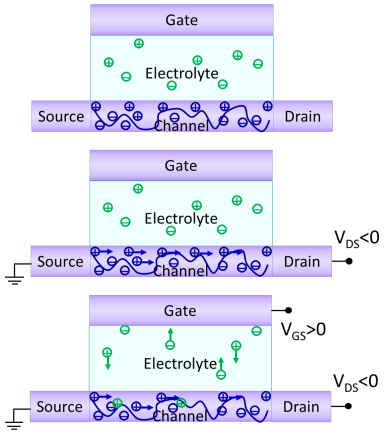


Figure 2.3: The functioning of an OECT explained schematically [44]. Without any biasing applied between the drain and the source, there is no current flow in the channel. When the drain to source voltage is negative, the polymer channel begins to conduct. As the gate to source voltage is positively biased, ion penetration begins from the electrolyte into the conductive PEDOT:PSS channel.

The functioning of the OECT can be explained by the way charge modifications occur in the conductive polymer channel as shown in Fig. 2.3. A commonly used polymer for

this purpose is poly(3,4-ethylenedioxy-thiophene):poly(styrene sulfonate) (PEDOT:PSS), a polythiophene derivative. This polymer has the property of becoming a p-type semiconductor when doped with PSS. In its pristine state PEDOT:PSS is partially doped. When a negative potential is applied to the drain with respect to source, ionic charge variations occur in the conducting polymer channel and current flow is established. Keeping the gate positively biased, the polymer channel is penetrated by ions arising from the electrolyte. This neutralizes the PSS charge in the PEDOT:PSS and semiconductor de-doping occurs according to the chemical reaction:

$$PEDOT^{-}:PSS^{-} + M^{-} + e^{-} <=> PEDOT^{-}:PSS^{0} + M^{+}:PSS^{-}$$

Thus, the gate potential modulates the electrochemical de-doping of the semiconductor.

ION SELECTIVE OECT

The importance of detecting specific ions has prompted the development of ion-selective organic electrochemical transistor sensors (IS-OECT). The first development in this front was reported by Sessolo *et al.* [45] and then by another team independently worked on the coupling of such OECTs with polymeric membranes that permits the passage of specific ions [46]. Fig. 2.4 shows the schematic of one such IS-OECT.

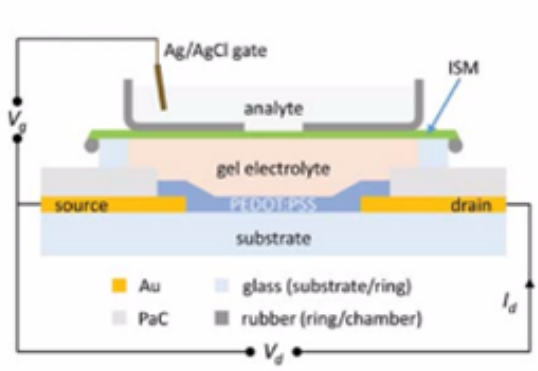


Figure 2.4: Cross section schematic of an IS-OECT. A reference electrode can be seen dipped in the analyte solution of interest. And ion-selective membrane separates the gel electrolyte from the analyte being studied.

A polyvinylchloride based potassium-selective membrane was chosen to be placed between a gel-electrolyte and the analyte of interest, separating the channel from the OECT gate. It was observed, that by increasing the concentration of the analyte there was an increase in the drain current which was proportional to the ionic concentration of the potassium (K^{+}) ions. This was, in turn, attributed to the increase in the number of K^{+} ions penetrating the channel and de-doping it, or even to the decrease of the electrolyte resistance.

Fig. 2.5 shows the calibration curve of the drain current and the effective membrane voltage versus ion concentration for pure KCl and $NaCl$ solutions. The sensitivity of the membrane to K^{+} ions is an order of magnitude higher than that of the Na^{+} ions, and hence confirms the ion-selectivity of the membrane in question.

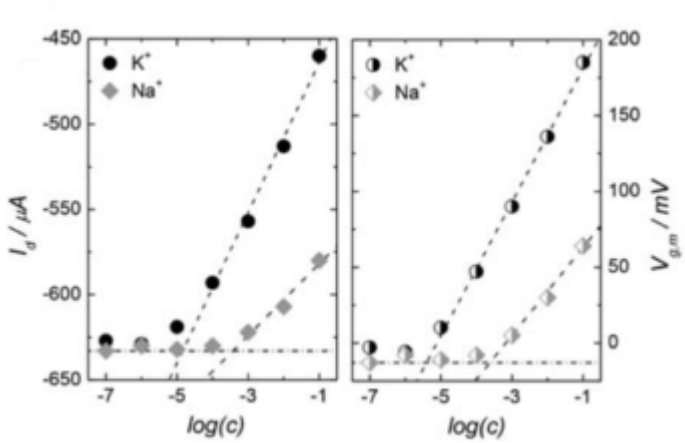


Figure 2.5: Calibration curves (I_d, V_{gm}, vs. concentration) of pure KCl and NaCl solutions performed using ion selective OECT (IS-OECT) [46].

THE ORGANIC TFT

OECT configurations allow for the addressing of a wide variety of novel applications of biosensors ranging from in-vitro to in-vivo cell biology. They also qualitatively address the unsolved problems of mechanical adaptability. OECTs, however, branch out to a broader transistor type, called Organic Thin Film Transistors (OTFTs). OTFTs have not yet comprehensively been developed for the purposes of OOC. This could essentially be due to two important reasons: 1) they usually need to be operated at relatively high voltages (usually tens of volts); 2) the charge carrier mobility in organic semiconductors is orders of magnitude smaller than what generally is measured in their standard inorganic counterparts, putting a serious limit on the frequency range of the electrical signals that might be applied as input to the organic amplifiers [37]. They have, by-far, been based on conjugated polymers, oligomers, or other molecules that have been envisioned as a viable alternative to more traditional, mainstream thin-film transistors (TFTs) based on inorganic materials.

Recently Benfenati V. et. al [38], were successful in fabricating an organic transistor to record the bidirectional stimulation of neurons, as shown in Fig. 2.6. However the organic transistor employed in the experiments is always operated in the off-state and thus, cannot be described as an actual amplifying transducer for cell activity. A SEM image of the active channel of the device has been shown in Fig. 2.7. Also, device fabrication of OTFTs necessitates the use of organic materials and polymers. Working with polymers, fabrication processes with several complex steps are necessary in order to process/fabricate an OTFT of the simplest nature.

Due to the relative low mobility of the organic semiconductor layers, OTFTs cannot rival the performance of field-effect transistors based on single-crystalline inorganic semiconductors, such as Si and Ge, which have charge carrier mobilities about three orders of magnitudes higher.

Most of the new techniques for detection of molecular charges share the advantage of a direct electronic readout and label-free detection [45]. Their fabrication can be carried out using relatively low-cost techniques. They also offer high current modulation and have

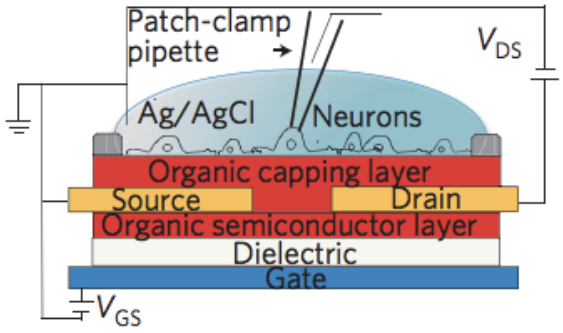


Figure 2.6: A schematic of the device fabricated by Benfenati *et al.* [38] for extracellular recording.

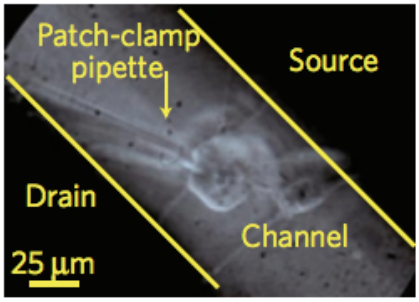


Figure 2.7: SEM image of the active channel of the device fabricated by Benfenati *et al.* [38].

higher SNR and lower detection limit, thereby achieving higher sensitivity and higher amplification of response [47]. Several OECTs have been developed with high stability in aqueous medium [48] [49]. Further they can also be used to locally amplify the signal even at very low voltages.

2.1.3. ION-SENSING FIELD EFFECT TRANSISTOR

Ionic species in the device incorporated during manufacturing of insulated gate field effect transistors (IGFET) introduce variations in the threshold voltage. The concept introduced by P. Bergveld in 1970 was that of a novel Ion-Sensing Field Effect Transistor [50]. It was based on the idea of measuring the activity of an ionic species in an aqueous solution to which the gate insulator is directly exposed. It is a potentiometric device and is very often, conventionally referred to as a pH sensor. They also have the advantage of being solid-scale micro devices with characteristic short response time and are produced using established electronics manufacturing.

EXTENDED GATE ISFET

Starting from the 1980s, a sensitive film could be incorporated on top of the floating gate giving rise to an extended gate Field-Effect transistor [51]. This type of technology can be well applied in the context of ion sensors applicable in Organ-on-Chip platforms as extended gate ion-sensing FETs (EG-ISFET). The EG-ISFET can be seen as a special type of MOSFET, with the gate electrode extended at a certain distance from the channel. When a positive voltage is applied to the common gate with respect to the source of n-channel MOSFET, electrons (which are the minority carrier in the substrate) are attracted to the surface and create a conducting channel between the source and the drain. The conduc-

tivity of this channel can thus be modulated by the strength of the electric field that exists in the gate insulator between the poly-gate electrode and the silicon.

Ishige et. al., developed another extended gate ISFET based enzyme sensor that was capable of detecting and measuring changes in the redox potential derived from enzyme-catalyst reaction [52]. However, this sensor was not able to detect changes in pH or ionic concentrations in the cell medium. Thus, it is likely that the changes in potential are caused due to the enzyme-catalyzed reaction and not the variation of ionic charge concentration under the gate extension of the FET sensor. More recently, in order to improve the performance of general ISFETs, another type of ISFET, the so-called region ISFET (RISFET), has been proposed by Risveden *et al.* [53]. The most interesting feature of the RISFET is that it has a specific region on the device that is lined with sensing electrodes. This area is where the ionic reactions from the electrolyte occur and result in changes in the threshold voltage of the RISFET.

2.2. CHALLENGE OF THE REFERENCE ELECTRODE BASED DESIGN

Ion sensors offer several advantages that are beneficial for their integration in OOC devices. At the same time, however, most of them also do share one major drawback which limits their performance and present some challenges in fabrication. This is essentially the need for reference electrodes. These electrodes are needed to set the voltage drop between the solution containing the molecules and the substrate and are most commonly shared by all sensors on the chip. This also sets the operating point of the transistor. The integration of these reference electrodes should largely be determined by their ease of fabrication. This is done either using standard CMOS processes or a combination of standard CMOS process coupled with organic materials and various different polymers. However, the electrodes are usually fabricated with $Ag/AgCl$, which cannot be easily integrated into a standard CMOS process thus preventing the realization of extremely low-cost, disposable devices. Further these electrodes, when dipped into the culture medium for a long time, result in continuous dissolution of the $AgCl$ layer into the solution causing slow degradation of the electrode potential over time [54]. This can change the potential being read from the electrolyte, as the ionic activity of the solution will also change. Also, applying biasing voltage to the cell culture can affect the cell or lipid bilayer integrity over an extended period of biasing.

2.3. THE CHARGE-MODULATED FGFET BASED DESIGN

Since the OECTs usually also encompass the use of several polymer layers, it also poses a challenge to ease of fabrication. Hence, an easy-to-implement design is necessary in the case of such an ion sensor, that can easily be integrated in standard CMOS processing. Keeping these criteria in mind, the design for a Charge-Modulated Floating-Gate Field-Effect-Transistor or Charge-modulated FGFET has been proposed. This device eliminates the use of a reference electrode, by biasing the transistor by means of a floating capacitor. The sensing area delimits the rest of the device from the electrolyte and is flanked by the gate extensions on all sides, only which remain in contact with the ions.

A detailed study of the design, modeling, fabrication and characterization of the device is presented in the following chapters.

3

DESIGN OF THE CHARGE-MODULATED FGFET

As discussed in chapter 2, the model of an FG-ISFET was selected for developing the ion sensor. A solid-state device has been proposed that is capable of detecting change in current from changes in the surface charge density in the active sensing area due to the presence of ions without the means of a biasing electrode. It allows direct detection of small changes in ionic activity with no need for complex, additional process steps and can completely be integrated into a CMOS and inexpensive process.

3.1. CONCEPT

The device structure proposed is based on an evolution of the floating-gate MOS transistor device developed by Barbaro *et al.* [55]. A cross section of the proposed transistor is shown in Fig. 3.1 The structure is composed of a floating gate transistor (M_0), a control gate that acts as a reference electrode (V_{CG}) and an active sensing area operated by charge induction (A_S), which is located behind the cross-sectional schematic where the floating gate electrode is extended and suspended on the free-standing PDMS membrane. This is more clearly illustrated in Fig. 3.2.

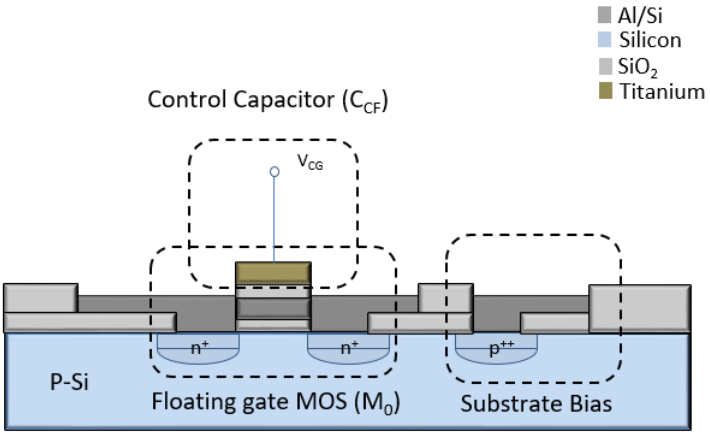
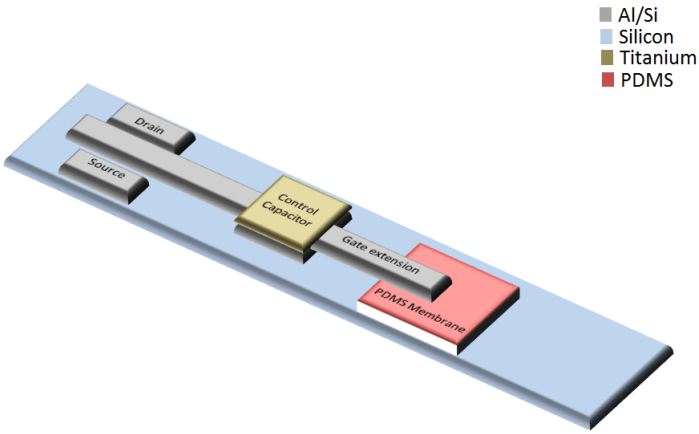
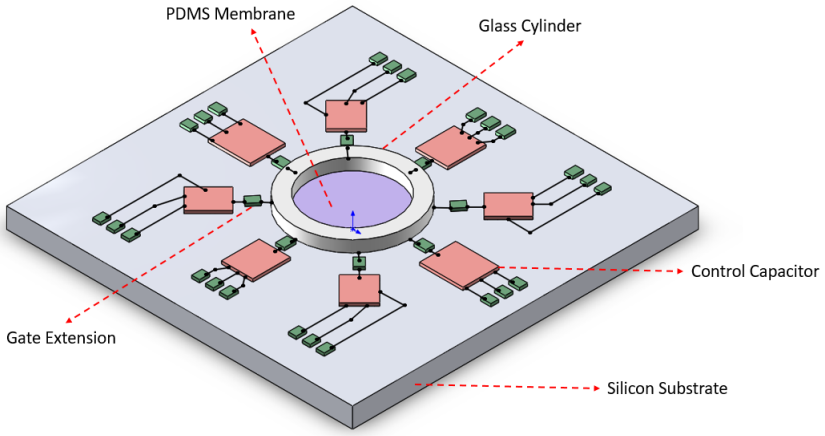


Figure 3.1: Cross-sectional schematic of the proposed Charge-modulated FGFET device.

The sensing area can be reached via a standard opening in the SiO_2 passivation layer. The gate extensions on the free-standing PDMS membrane are bound by a glass ring containing the cell culture.



(a)



(b)

Figure 3.2: a) Simplified 3D diagram of the proposed Charge-modulated FGFET. Here, the sensing area with the PDMS membrane can be seen more clearly. b) Experimental setup view

3.2. WORKING PRINCIPLE

The sensing principle of the device is based on the changes in threshold voltage (V_{TH}) introduced due to changes in ionic charge concentrations occurring in close proximity of the sensing area. A schematic of the working of this Charge-modulated FGFET has been shown in Fig. 3.3. This change in the V_{TH} of the MOS transistor causes a modulation of the charge carrier density inside the channel. Consequentially a variation in the output current I_D is expected. Thus the control capacitor and the active area together determine the actual voltage difference V_{FG} between the floating gate and silicon bulk so they determine the drain current of the MOSFET transistor. The final voltage is determined by the superposition of each source.

The need for a reference electrode is eliminated since the capacity to turn-on the FET is regulated by the presence of an integrated control electrode capacitively coupled to the floating-gate of the MOS transistor. This essentially sets the working point of the transistor. Hence, the detection mechanism is triggered by the differences in the effective threshold voltage. and not by absolute values.

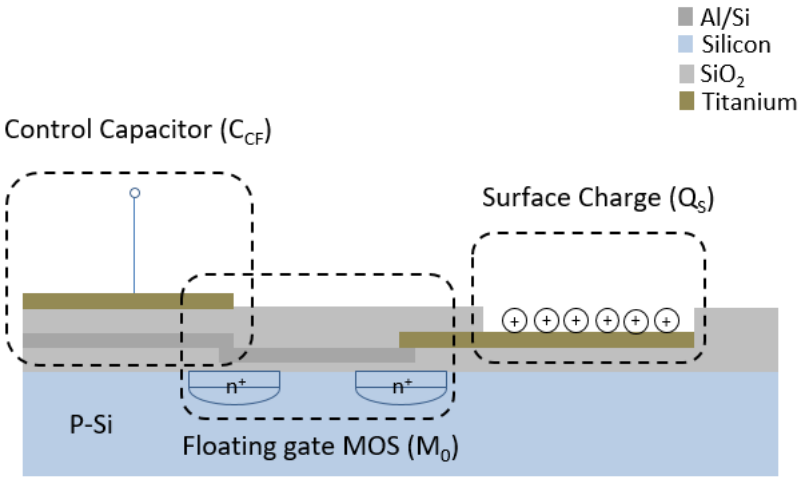


Figure 3.3: Working Principle.

The active area plays a very key role in this design. Without the active sensing area, the device structure could simply be called a conventional floating gate transistor. The device basically behaves as governed by the electrostatic laws of induction. The surface charge Q_S that is bound within the sensing area creates an electric field, thereby causing a separation of charges in the silicon layer. This results in a charge Q_i being induced on the top surface of the floating gate. Now according to the principle of conservation of charge, the total charge appearing in the actual gate should remain constant. This generates another layer of charges of the opposite nature $-Q_i$ to appear on the bottom surface as well. This results in significant charge mobility underneath the active sensing area. The carriers are either attracted or repelled. This causes an electric field to be generated and thus results a voltage drop (V_{FG}) between the bulk of the substrate and the floating gate. Hence the device may be activated depending on the voltage V_{FG} and thus produce a drain current. It should be noted here that since the bulk is p-type and the surface bound charge Q_S is positive, the transistor device would be turned-on as the voltage drop V_{FG} is positive. Thus considering the application and effect of the control capacitor, it is possible to model the device as a conventional MOS transistor with a threshold voltage that is adapted to this design.

3.3. MATHEMATICAL MODELING

The mathematical modeling for the Charge-modulated FGFET has been designed based on a previous study undertaken by Barbaro *et al.* [55]. In this device, the floating gate voltage (V_{FG}) w.r.t the silicon body, is basically set by two major functionings. As the charge

Table 3.1: Geometric and Process Parameters [55]

Parameter	Meaning	Units
V_{FG}	Voltage between silicon substrate and floating gate	V
V_{CG}	Control voltage of the capacitor	V
V_{TH}	Threshold voltage	V
V_{THF}	Effective threshold voltage	V
C_{CF}	Capacitance of the control capacitor	F
C_{FB}	Capacitance between the floating gate and silicon body	F
Q_S	Surface charge in sensing area	C
Q_i	Induced charge on silicon due to Q_S	C
Q_{F0}	Trapped electric charge in the floating gate	C
C_{fringe}	Field effect of the control capacitor	F/m
t_d	Dielectric thickness	m
A_{CF}	Surface area of the control capacitor	m^2
P_{CF}	Perimeter of the control capacitor	m
A_S	Sensing area	m^2
t_{ox}	Gate oxide thickness	m^2

conservation principle suggests, the total charge in the floating gate must remain constant, since it is completely isolated and no external charge injection mechanism is applied. Expressing the charge equations in terms of capacitances (all voltage expressions are w.r.t the silicon substrate voltage)

$$Q_{F0} = Q_i(Q_S) + Q_{CCF} + Q_{CFB}$$

$$= Q_i(Q_S) + C_{CF}(V_{FG} - V_{CG}) + C_{FB}V_{FG} \tag{3.1}$$

$$V_{FG} = \frac{C_{CF}}{C_{CF} + C_{FB}} V_{CG} + \frac{Q_{F0} - Q_i(Q_S)}{C_{CF} + C_{FB}} \tag{3.2}$$

where Q_{F0} is the total charge within the floating gate. It is to be noted here that Q_{F0} might not be constant across all devices as it depends on the microfabrication process. Q_S is the surface charge while Q_i is the charge induced on the silicon due to Q_S. Equation 3.2 denotes the relationship between the control gate voltage, surface charge and the floating-gate voltage. Thus, drain current of the MOS transistor M_0 is determined by both the voltage of the control gate V_{CG} and surface charge Q_S.

The change in the effective threshold voltage (V_{THF}) of the MOS transistor can now be modeled according to the effect from all the other voltage sources. The threshold voltage of the device can be modulated depending upon the surface charges that are present on the active area.

$$V_{FG} - V_{TH} = V_{CG} - V_{THF}$$

$$\frac{C_{CF}}{CCF+C_{FB}} V_{CG} + \frac{Q_{F0}-Q_iQ_S}{C_{CF}+C_{FB}} - V_{TH}$$

$$\approx V_{CG} - (V_{TH} - \frac{Q_{F0} - Q_i(Q_S)}{C_{CF} + C_{FB}})$$

$$V_{THF} \approx V_{TH} - \frac{Q_{F0} - Q_i Q_S}{C_{CF} + C_{FB}} \tag{3.3}$$

It is important to note here that the above simplification is possible only when $C_{CF} >> C_{FB}$. Thus, due to the effect of the control capacitor acting as the reference electrode, it is possible to detect both negative as we well as positive charges via the Charge-modulated FGFET. A negative charge on the surface, i.e. Q_S results in a positive shift of the threshold voltage while a positive charge will cause a negative change in the V_{THF}. This is the case for an NMOS transistor. The opposite would come into play for a p-type MOS transistor.

As is evident from the modeling, the threshold voltage of the transistors is now dependent on the surface charge on the sensing area (Q_S) and the capacitance of the control structures. The control capacitor capacitance (C_{CF}) is dependent on the area of the capacitor plates (A_{CF}) and the dielectric thickness (t_d). However, in addition to A_{CF} and the gate oxide thickness t_{ox}, the capacitance between the floating gate and the silicon bulk i.e. C_{FG}, depends on the area of the sensing site, A_S, as well. Individually, C_{CF} and C_{FG} can be expressed as the following,

$$C_{CF} = \frac{A_{CF}\epsilon_{ox}}{t_d} + C_{fringe}P_{CF} \tag{3.4}$$

$$C_{FB} = \frac{A_{CF}\epsilon_{OX}}{t_{ox}} + \frac{A_S\epsilon_{OX}}{t_{ox}} \tag{3.5}$$

The meaning of each parameter in the modeling equations is given in Tab. 3.1

Since the capacitance will be dependent on the design of the device that is pre-decided during modeling, every parameter in 3.3 can be considered constant. Thus the change in V_{TH} can be attributed only to varying charge concentration in the sensing area i.e. only Q_S would now be responsible for the field effect modulation in the device. Every parameter can also be linked to the trapped charge as a consequence of the manufacturing process.

3.4. DESIGN

The charge-modulated FGFET has been designed based on theoretical calculations of the modeling parameters as established in the previous section. The control capacitor is designed with 500µm sides thus yielding a surface area of $2.5x10^{-7}m^2$. The reason A_{CF} is chosen to be so big is in order to have a high C_{CF} so as to satisfy the criteria of $C_{CF} >> C_{FB}$ as obtained from 3.4 and 3.5. A_S is the area of the extended gate electrode in contact with the ionic solution. To be able to have the smallest value of C_{FB} possible the gate extension is chosen to have 80µm sides and thus a total area of $6.4x10^{-9}m^2$. t_d is also taken to be the minimum value possible. Since at the Else Kooi Laboratory (EKL), the minimum thickness of silicon dioxide that can be deposited using PECVD is $50nm$, that was the preferred thickness for the dielectric. The thickness of the gate oxide deposited was at 200nm.

Using 3.4 and 3.5, C_{CF} was calculated to be $172pF$ and C_{FB} at $40pF$. Thus, all simplifications are valid as $C_{CF} >> C_{FB}$.

Table 3.2: Process Parameter Values

Parameter	**Value**	**Units**
C_{CF}	$172x10^{-12}$	F
C_{FB}	$40x10^{-12}$	F
P_{CF}	$500x10^{-6}$	m
A_{CF}	$2.5x10^{-7}$	m^2
C_{fringe}	0	F/m
t_d	50	nm
A_S	$6.4x10^{-9}$	m^2
$\epsilon_{OX} = \epsilon_0\epsilon_r$	$3.45x10^{-11}$	
t_{ox}	$200x10^{-9}$	m

All the values of the process parameters have been summarised in Tab. 3.2.

4

FABRICATION OF THE CHARGE-MODULATED FGFET

The device has been fabricated using standard CMOS technology, providing low-cost, large-scale-of-integration capabilities. It was fabricated in the EKL facility of the Electrical Engineering, Mathematics and Computer Science (EEMCS) Department of TU Delft.

4.1. SINGLE DIE LAYOUT

The mask for the device was designed using the Tanner L-Edit IC Layout software. The mask design of the IC corresponds to the conceptual design of the device, as discussed in 3.1. A single die appears as in Fig. 4.1, which is also the mask design with all layers. The die size is 10x10mm, and every wafer has 52 copies of the die.

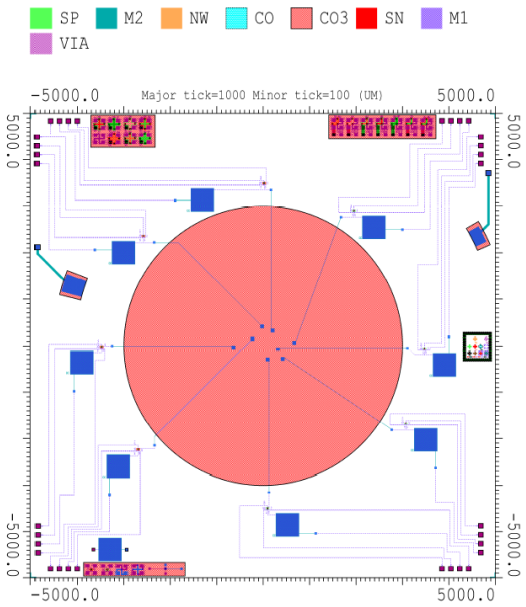


Figure 4.1: The layout of one single die. The die size is 10,000 x 10,000 µm and every colour depicts an individual mask. The bondpads are visible on each of the four corners of the die. The red circle in the center is the active sensing area where the free-standing PDMS membrane is fabricated. The blue squares depict the control capacitors that act as the reference electrode.

A single die consists of 4 PMOS transistors and 4 NMOS transistors with varying W/L ratios of the channel namely 2:10, 2:15, 2:20 and 2:25. The width of the channel is kept constant at 2µm for all transistors for easier comparison of results. The active sensing area is present on the center of the device, where the cylinder is attached to the die. This is meant to contain the electrolyte to measure the drain current response of the Charge-modulated FGFET to varying ionic concentrations. The bondpads for the source, drain, substrate bias and the control capacitor biasing have been placed in the four corners of the die. Only the bondpad for biasing the gate is placed next to the sensing area.

A zoomed-in image of the mask with its different layers can be seen more in Fig. 4.2.

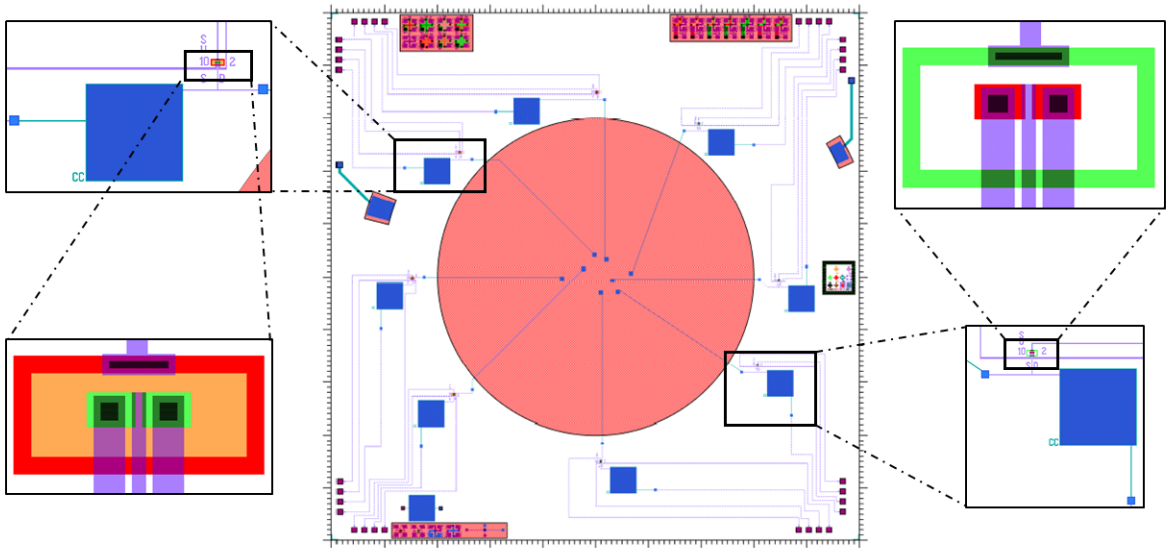


Figure 4.2: The layout of the mask with individual transistors and their active channels zoomed into.

The mask consists of 2 reticles with 4 layers in each reticle. The complete mask layout has been given in Appendix A.

4.2. PROCESS FLOW

The flowchart for the BiCMOS process was used as the base to fabricate the transistors. However, all the design parameters of the process flow were accordingly modified in order to get the best possible results for this study. The final detailed flowchart has been added in Appendix B, also outlying all the process parameters.

The proposed fabrication process flow has been shown in Fig. 4.3. Silicon served as the substrate. The process began by the ionic implantation of the n-well and p-boundaries for the MOS transistor structures as shown in step 1 of Fig. 4.3. After implantation, a layer of SiO_2 of 200nm was deposited to define the gate oxide, as shown in step 2. This was done using thermal oxidation in the furnace. Since the consumption of implanted silicon is faster

during thermal oxidation, the doped regions were expected to have twice the thickness of SiO_2 than the undoped regions.

Subsequently, the contacts for the source, drain and the substrate biasing points were opened up, as shown in step 3, in order to have perfect contact with the metal layer. This was done by wet etching the wafers in BHF 1:7 until the backside was completely hydrophobic. Since the doped regions have twice as thick oxide as the undoped regions, contact openings were etched for twice the time to etch the backside completely. Following this, first metalization was done by sputtering 600nm of Al/Si at 25°C, as in step 4. Aluminum with 1%Si was chosen, rather than pure aluminum to have good adhesion with the silicon substrate underneath. The Al/Si was plasma etched to build up all the interconnects, the bondpads and the bottom electrode of the control capacitor that is meant to bias the floating gate. This is shown in step 5. Preliminary electrical measurements of the transistors could already be performed at this stage.

A very thin layer of oxide was then deposited (50nm) by PECVD, which serves as the dielectric between the parallel plate capacitors, as shown in step 6. Following this, two vias were opened up, per transistor, in order to be able to access the top electrode of the control capacitor and the gate extension, during second metalization. This was done using plasma etch, as the BHF 1:7 wet etch couldn't be used anymore, since the aluminum layer would immediately be attacked. 200nm titanium was then sputtered at 25°C and etched to create the top electrode of the control capacitor and gate extensions, and also their bondpads for electrical characterization. This is shown in step 7 and 8. Since everywhere else the device was now covered in a thin layer of SiO_2, this was followed by plasma etch of the oxide to opening up the contacts to the bondpads as well as the active sensing area to expose the extended gates to the ionic solution, as shown in step 9. At this stage, the electrochemical characterization for the devices was performed to make sure that the Charge-modulated FGFETs are actually responsive.

Finally the gates had to be suspended on a PDMS membrane and the membrane released. 6µm SiO_2 was deposited on the backside by PECVD, to serve as the passivation layer during Silicon etching, as shown in step 10. This was patterned using plasma etch for 12 minutes to open the area for the PDMS membrane to be released (step 11). 9µm PDMS was spin coated on the frontside (step 12) and a 200nm layer of Al/Si was sputtered on top of it at 25°C (step 13). This acted as a passivation layer to protect the PDMS during deep reactive ion etching (DRIE) of the silicon substrate from the backside, as the Al/Si frontside faced the chuck surface in the etcher which may be contaminated with particles. Finally the silicon substrate is etched using DRIE, as shown in step 14. The wafer was of standard thickness, that is 525 µm. Calculating an etch rate of 1.5µm per cycle, in total 360 cycles were performed in the DRIE process, at 20°C. Finally the Al/Si on the frontside is etched in PES for 6 mins and the PDMS membrane, with the suspended gate extensions is released.

It is difficult to be able to show the fabrication flow via the device cross-section w.r.t the PDMS membrane release as the membrane is only present in the center of every die. Hence, in Fig. 4.4 a cross-sectional schematic of the device has been made, after membrane release, to make the process flow more understandable.

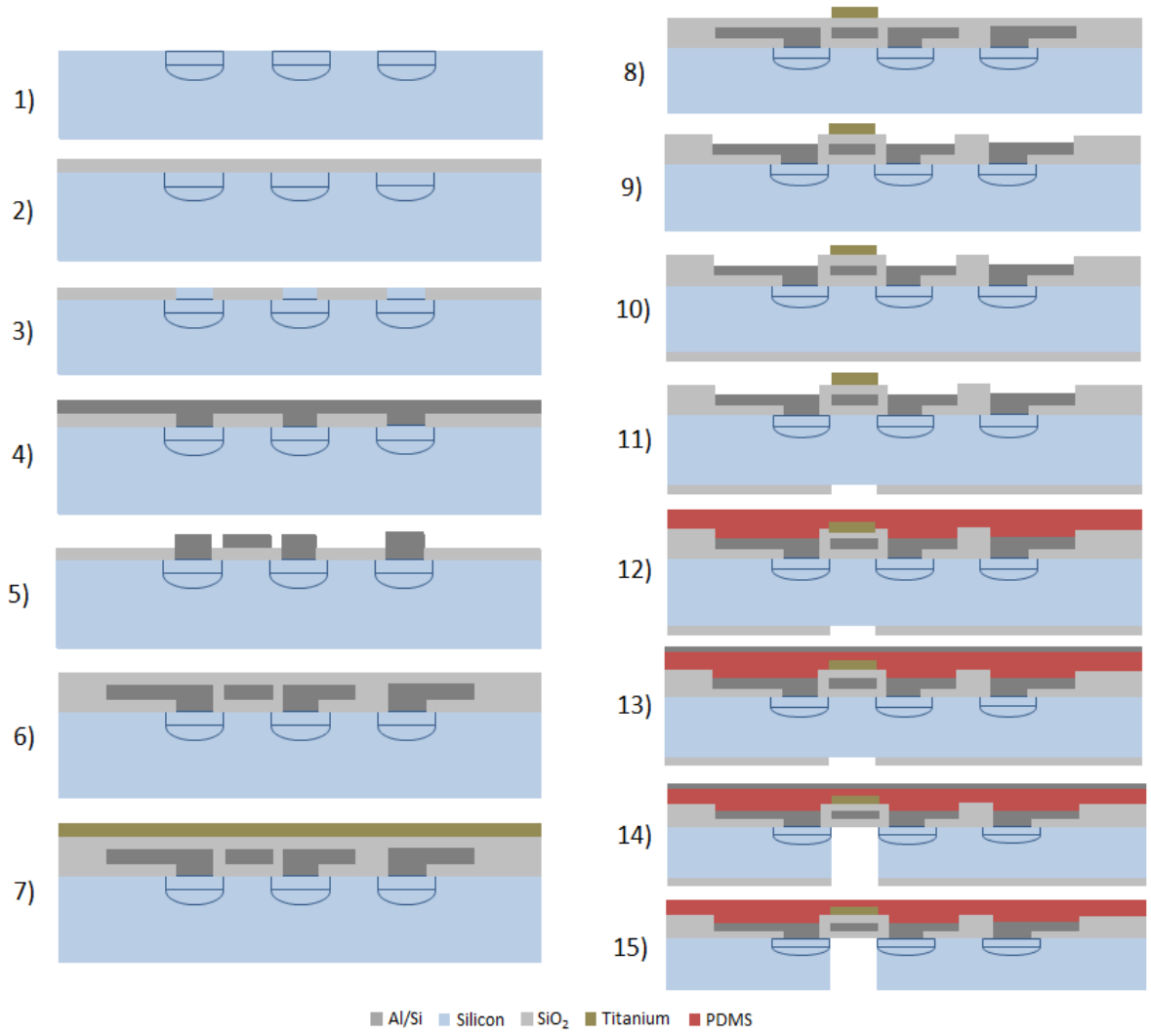


Figure 4.3: Proposed Fabrication Process Flow.

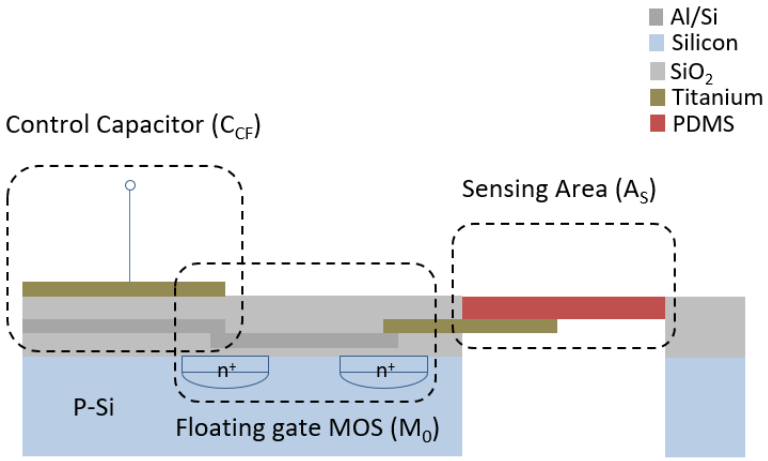


Figure 4.4: Cross-sectional schematic of the Charge-modulated FGFET after membrane release.

4.3. TITANIUM ETCH WITH SOFT LANDING ON SiO_2 LAYER

The design of the device is such that a very thin layer of oxide is chosen as the dielectric deposited by PECVD. This is on top a very thick layer of aluminum viz. $600nm$. The thickness of the metal layers are not relevant in this study, as they do not impose any restrictions on the electrical measurements. In Fig. 4.5, the transistor features have been shown, just after the aluminum etch. However, there were problems encountered especially during the patterning of the Titanium layer.

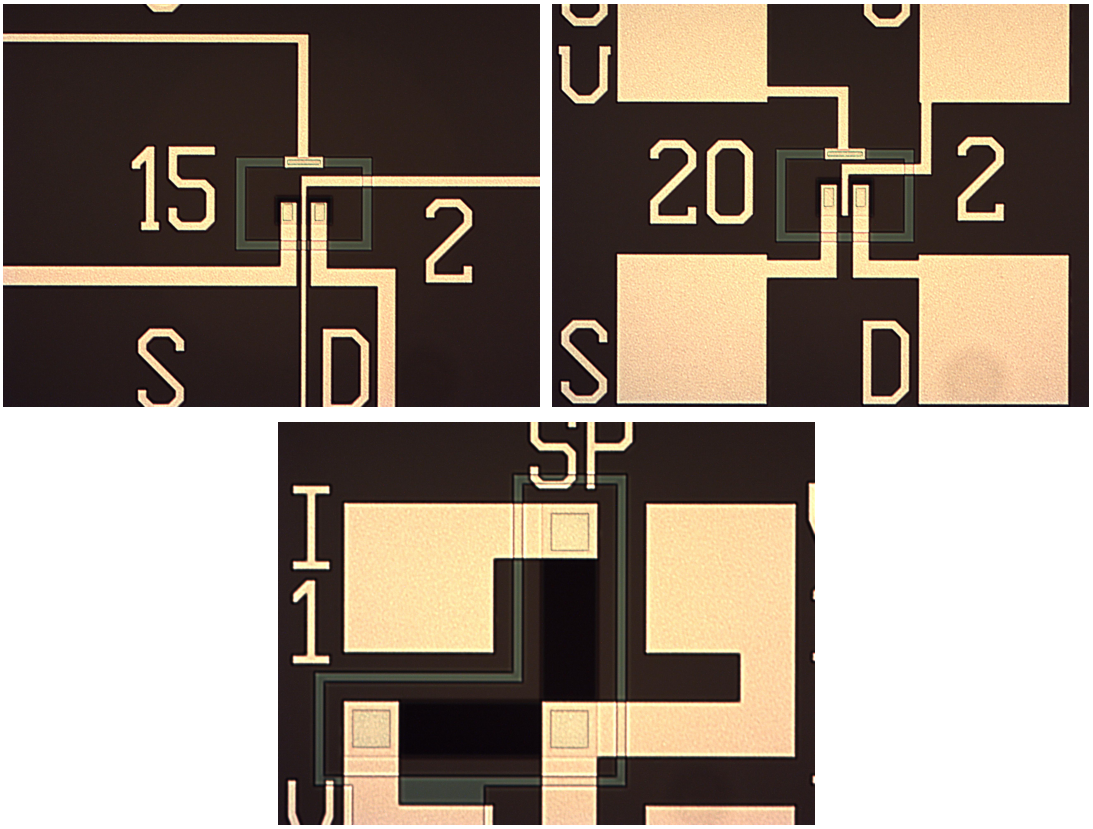
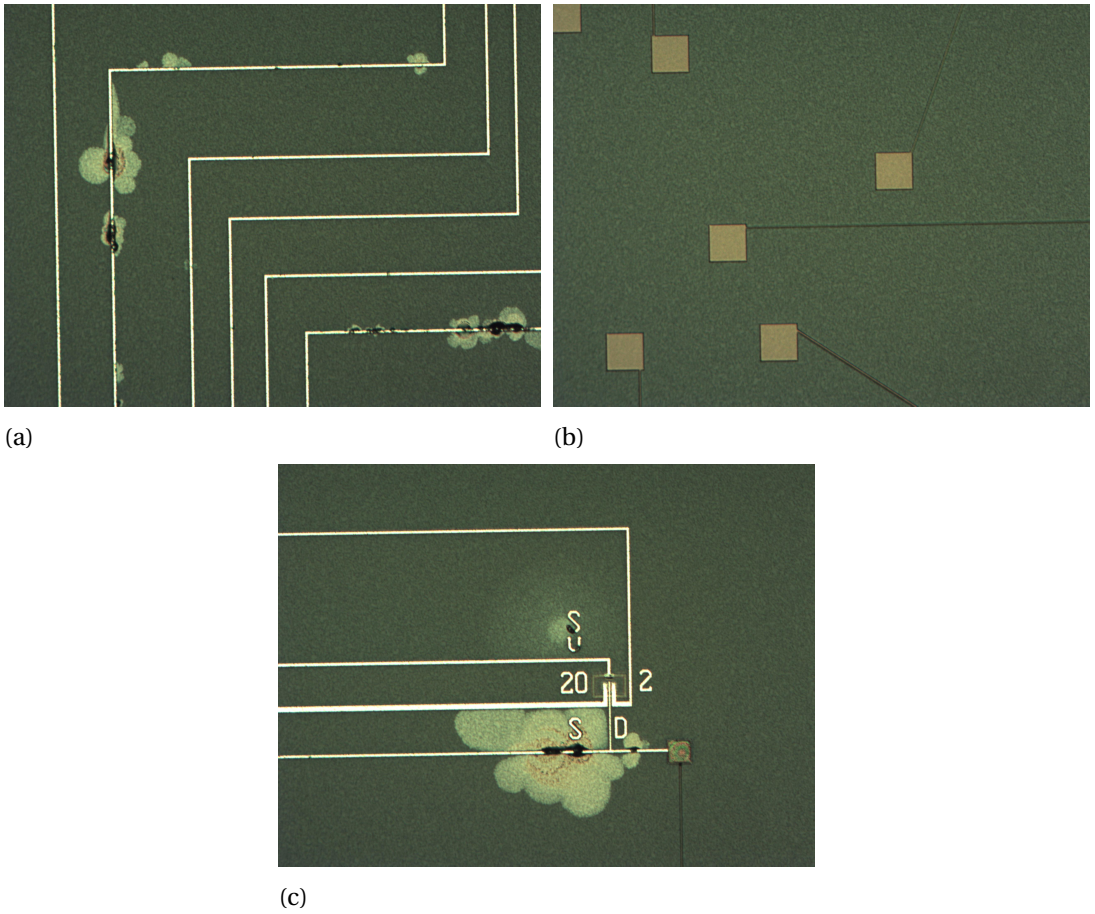


Figure 4.5: Device and test structure after 1st metalization, with aluminum layer.

4.3.1. CHALLENGES WITH PLASMA ETCHING

The patterning of titanium was initially done using plasma etching in Trikon Omega 201. However, the recipe is not conditioned for end-point detection. Making a soft-landing on SiO_2 without etching away any of the oxide layer was a major challenge. 200nm of titanium was meant to be etched. Initially the wafers were subjected to 18 secs of total etch time as usually $100nm$ of titanium etched away in ≈18 secs. From here-on, trial-and-error had to be performed in order to understand the exact etch time to pattern the rest of the titanium. Starting off from an extra 12 sec etch, thus a total etch time of 30 secs, the titanium was observed to have been almost completely etched away, except for the corners at which the interconnects bend. There were still residues of titanium attached the aluminum that needed to be etched away. The sensing area appeared to be completely titanium free and cleanly etched. However, the oxide underneath also appeared to have started etching

away in certain areas with large circular spots visible. All of these have been shown via photographs from the optical microscope, as shown in Fig. 4.6.



(a) (b)

(c)

Figure 4.6: Photographs of the die after a 30 sec plasma etch. a) Titanium still present in interconnect bend corners. b) Titanium appeared to have been completely etched away from the sensing area leaving cleanly patterned gate extensions. c) Areas around some transistors showed over-etch of the oxide layer underneath.

Following this, the etch total etch time was reduced to 25 secs and the corresponding results were observed. This time, surprisingly, the titanium wasn't etched away completely in all regions of the die. However, the oxide was appeared to have already started to etch away in several regions of the die leaving large circular spots as before. It was an interesting observation, as the total etch time in this attempt was shorter than the previous one. Fig. 4.7 shows pictures of the wafer after the 25 sec plasma etch.

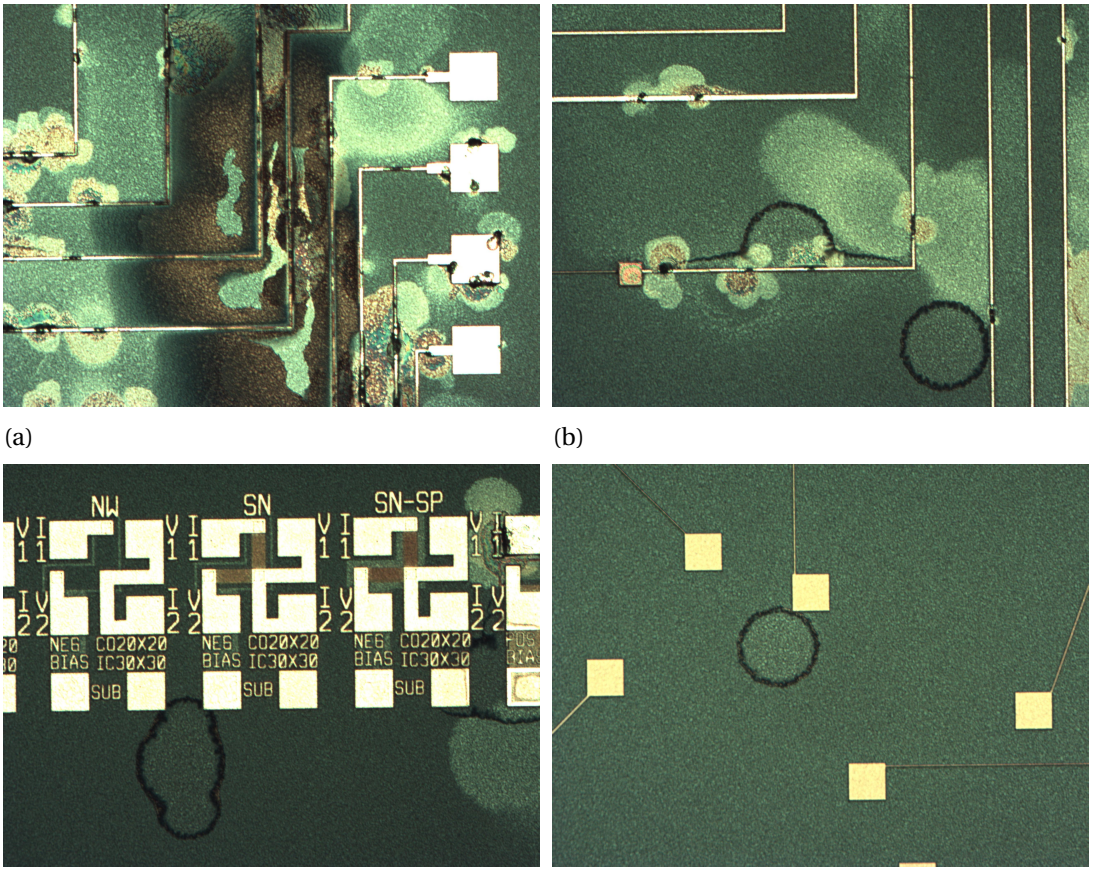


Figure 4.7: a) and b) show the dirty areas left behind due to under-etch of the Ti layer after 25 sec plasma etch. c) and d) are the areas of oxide over-etch leaving behind large circular spots on the die.

4.3.2. OXALIC ACID ETCHING OF TITANIUM

In order to counter this problem of dry etching of Titanium, part plasma etch and part wet etch was performed. Oxalic acid ($C_2H_2O_4$) was found to be highly selective to titanium [56] [57]. Using this, the SiO_2 and Al/Si layer underneath could be kept completely preserved. Some test wafers, with titanium on top of oxide and aluminum, were etched first to calculate the metal etch rate and selectivity in oxalic acid. It was found to be ≈ 60nm/min, and highly selective to titanium. The process wafers were then first subjected to plasma etching for 18 secs to etch ≈100nm of titanium and then kept dipped in 10% oxalic acid at 90°C for 2 mins to etch away the remaining titanium leaving a clean oxide surface underneath.

4.4. DEVICES FOR ELECTROCHEMICAL CHARACTERIZATION

After the titanium was patterned, the opening of the bondpads remained. The SiO_2 was etched in Drytek Triode 384T, using the standard oxide etch recipe, and the devices were ready for electrochemical characterization. Some wafers were diced and taken out for measurements, to verify the proof-of-concept and working of the Charge-modulated FGFET ion sensor at this stage. The results of the characterization have been detailed in Chapter 5. Some pictures of the dies at this stage, before membrane deposition and release have been shown in Fig. 4.8 and Fig. 4.9.

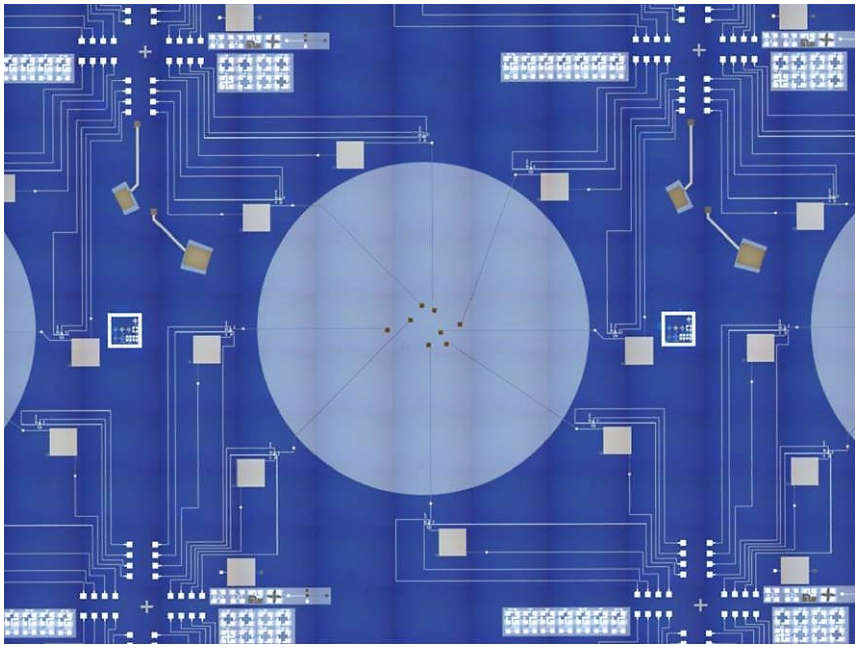


Figure 4.8: A complete layout of one die in a wafer before PDMS membrane deposition and release.

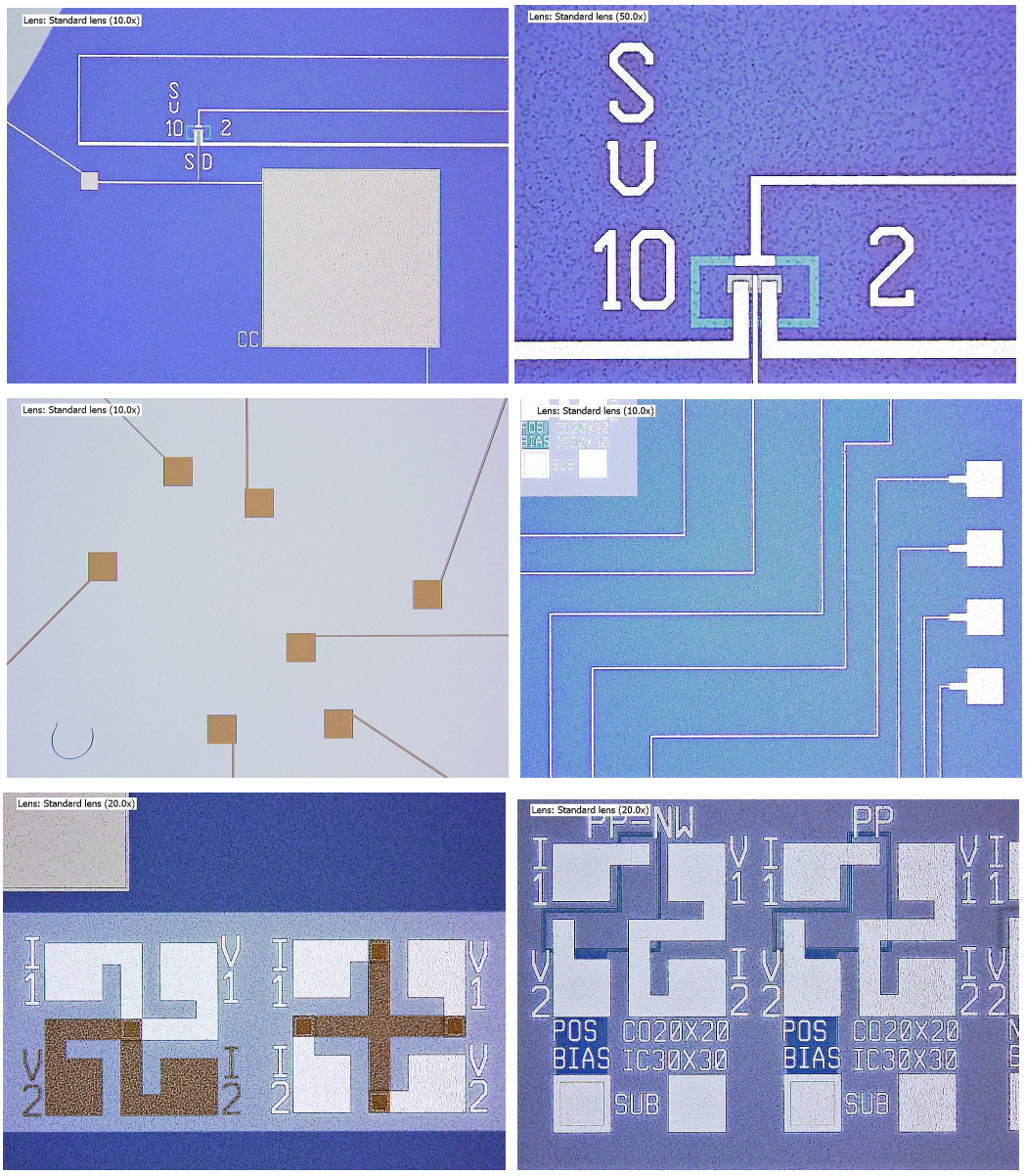


Figure 4.9: Final devices for electrochemical characterization. The PDMS membrane still has to be deposited and released, to prove the ability of the devices to be integrated in an OOC platform.

4.5. FINAL FABRICATION RESULTS

The wafers that were left for further processing were deposited with PDMS on the frontside. A thick layer of SiO_2 was deposited on the backside to serve as a passivation layer during silicon etch. DRIE was performed to etch away the silicon from the backside and the membrane in the sensing area was released. Fig. 4.10 shows a photograph of the wafer frontside after PDMS membrane release, while Fig. 4.11 shows the frontside of the wafer with the sensing area zoomed-into, which clearly shows the gate electrodes suspended on the free-standing membrane. Fig. 4.12 shows a photograph of the backside of the wafer after membrane release. Lastly, Fig. 4.13 shows pictures of the final devices taken under a laser scanning microscope. Some pictures of the final membrane released die have also been shown in Fig. 4.14.

Figure 4.10: Frontside of the wafer after PDMS membrane release.

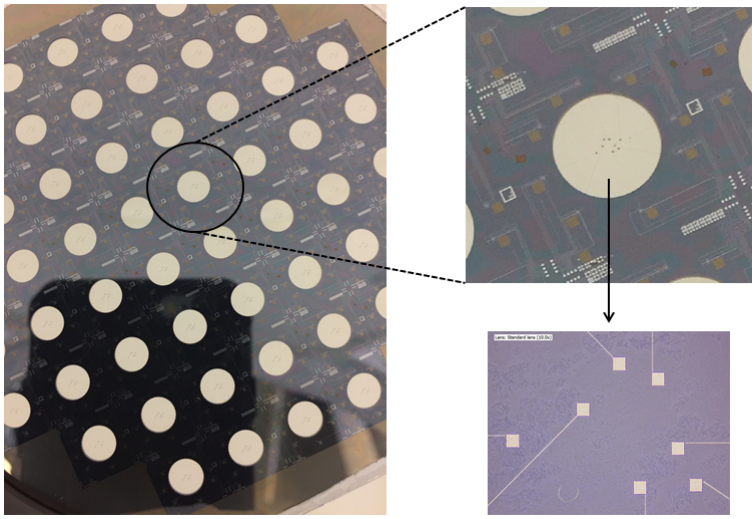


Figure 4.11: Suspended gate electrode extensions on the transparent PDMS membrane.

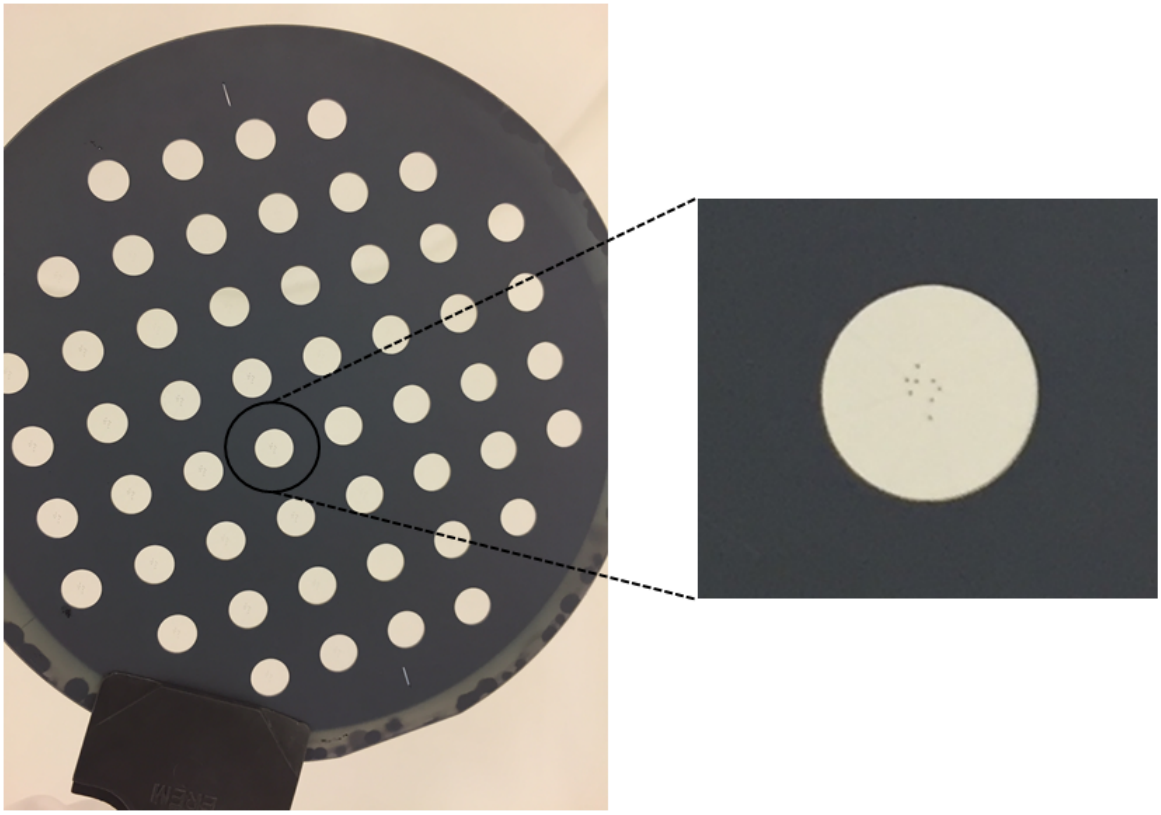


Figure 4.12: Backside of the wafer after PDMS membrane release. The transparency of the membrane is highlighted by the inset where-in the gate extensions are clearly visible.

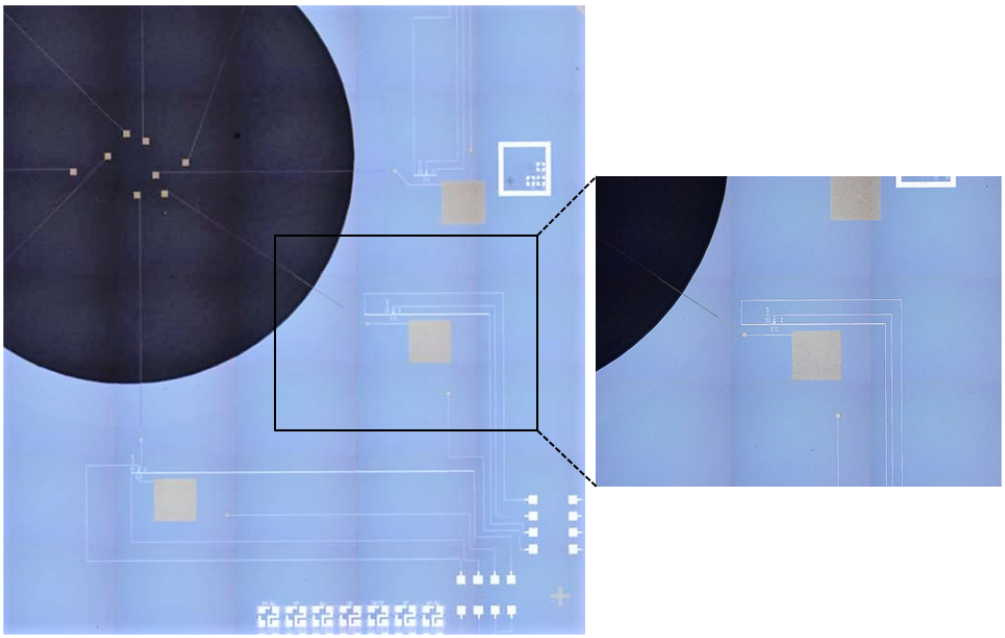


Figure 4.13: Photograph of a die after PDMS membrane release taken under an optical microscope. The membrane is transparent and hence appears black as the stage of the microscope is black in color. The inset shows a close-up of the transistor structure completely preserved.

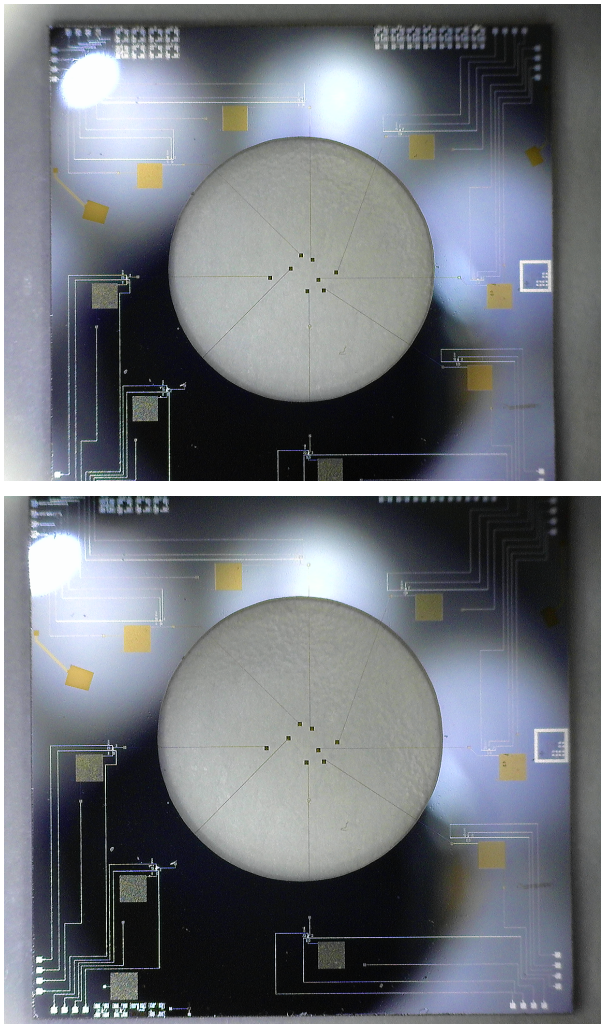


Figure 4.14: Microscope pictures of a final die with the PDMS membrane released. There appears to be a lot of reflection coming off the chip, as keeping the microscope light on was necessary to obtain clear view of the features. The tiny particles that are visible are dirt particles from the storage box.

As we can see from the figures, the electrodes are preserved as they were prior to membrane release. This further qualifies the device to be easily integrated into a stretchable OOC platform since both the electrodes and the membrane could completely survive the release process.

4.6. CONCLUSION

The Charge-modulated FGFET was successfully fabricated and the gate electrodes were suspended on a free standing PDMS membrane. There were certain problems with the etching of titanium with a silicon oxide underneath. However, that was resolved by etching of titanium with oxalic acid. The high selectivity of titanium to oxalic acid was also an interesting new finding for this study. The ability of both the membrane and the gate electrodes to fully survive the membrane release process also proves the potential of the integration of the Charge-modulated FGFETs into OOC applications.

5

Electrical and Electrochemical Characterization Results

The Charge-modulated FGFET ion sensors were electrically characterized in the Cascade 33 automatic probe station using the Agilent IC-CAP 2012 software. 4 probes and 5 probes measurement were made, the results of which are detailed in the following sections. For easier comparison, only the MOS transistors with 2:25 W/L ratio have been characterized. For reference, all the raw measurement data so obtained has been added in Appendix C.

5.1. Device Electrical Characterization

After the second metalization and patterning, the electrical measurements for the devices were performed. Output and transfer characteristics were obtained for both PMOS and NMOS devices. These measurements were taken without any electrolyte in actual contact with the sensing area.

5.1.1. Transfer Characteristics

The I_D vs. V_G measurements for the MOSFETs were performed. The gate voltage was swept from -5V to 5V. The substrate was biased at $0V$ and $V_{DS} = -3V$ for PMOS and $V_{DS} = 3V$ for NMOS. The drain current is measured by the instrument simultaneously. The results have been illustrated in Fig. 5.1 and Fig. 5.2.

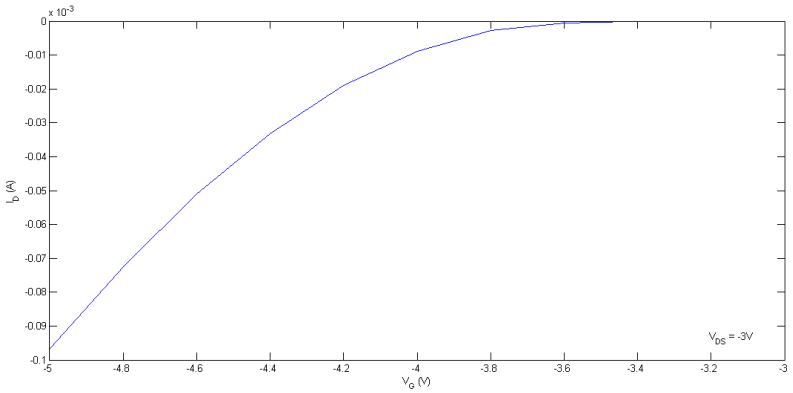


Figure 5.1: Measured transfer characteristics of the Charge-modulated FGFET, PMOS 2:25.

As can be observed from the curve in Fig. 5.1, the V_{TH} for the PMOS is relatively high viz. ≈ -3.7V. Higher threshold voltage would imply that the MOSFET requires higher voltage to "turn-on". This is most likely due to fabrication flaws. In order for the inversion layer to become a channel, it is necessary to mirror the charges on both sides of the channel. This is related to the doping of the substrate and perhaps the dosage of implantation could be adjusted during processing to make the PMOS respond better.

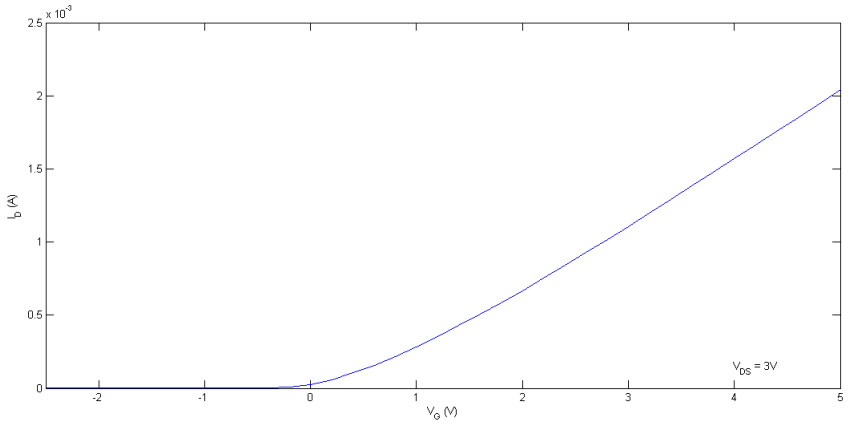


Figure 5.2: Measured transfer characteristics of the charge-modulated FGFET, NMOS 2:25.

Since the V_{TH} from the NMOS transfer plot is not visible clearly enough and appears to be in the negative voltage region, Fig. 5.3 gives a zoomed-in version of the plot for better understanding of the same.

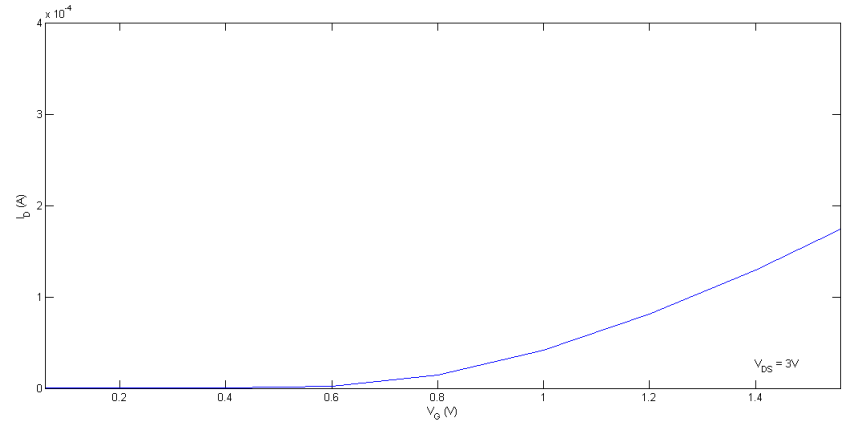


Figure 5.3: Zoomed-in transfer characteristics plot for the Charge-modulated FGFET, NMOS 2:25. The threshold voltage appears to be around 0.6V.

Thus, from the above plot, the V_{TH} for the NMOS appears to be signifcantly better at ≈0.6V. Hence, it is more likely that the NMOS is more robust and sensitive than the PMOS structures. As pointed out arlier, this could possibly be attributed to the dosage of implantation during doping of the substrate. The fact that the NMOS is fabricated within the bulk of the p-type substrate itself, is perhaps a crucial reason for its better functioning, while the PMOS is fabricated within n-well regions that are doped in the substrate bulk.

5.1.2. OUTPUT CHARACTERISTICS

To determine the output characteristics of the device, measurements of I_D were performed against varying V_{DS}. The drain-to-source voltage was varied from 0 to -8V. The gate voltage was swept from -5 to -8V, in-case of the PMOS, and the resulting I_D was measured as shown in Fig. 5.4.

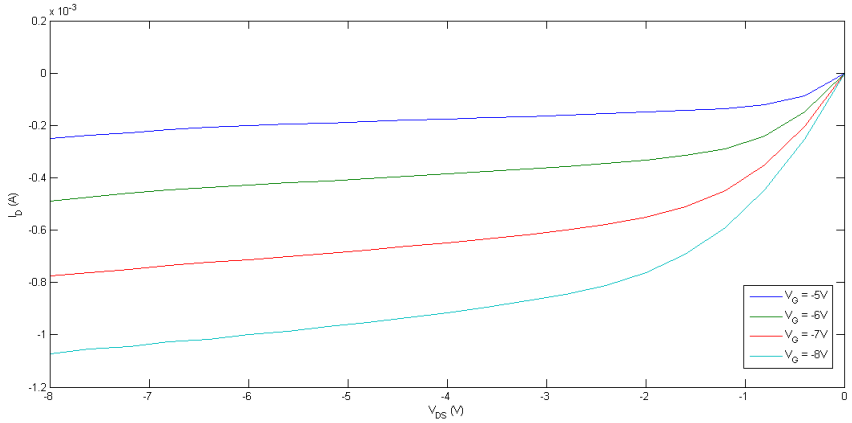


Figure 5.4: Measured output characteristics of the Charge-modulated FGFET, PMOS 2:25.

Similarly for the NMOS, the gate voltage was swept from 5 to 8V and drain-to-source voltage from 1 to 8V. The resulting I_D was measured, as shown in Fig. 5.5.

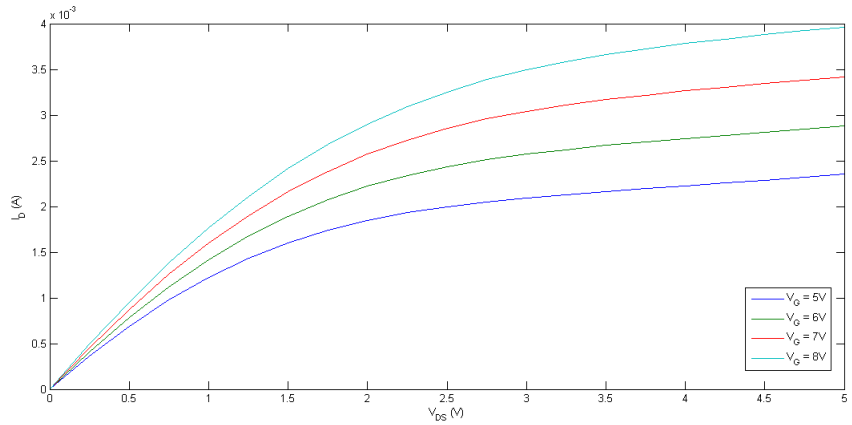


Figure 5.5: Measured output characteristics of the Charge-modulated FGFET, NMOS 2:25.

5.2. POST-INCUBATION DEVICE CHARACTERISTICS

Another important requirement was the stability of the devices over time in a humid environment. Since the Charge-modulated FGFET is meant to be integratable in an OOC platform, it is important to verify the robustness of the device in humid conditions, similar to the physiological conditions of the human body.

In order to do so, three dies were kept in an incubator at 37°C and 90% humidity for 7 days. The setup has been shown in Fig. 5.6. The setup was checked from time-to-time to

ensure there was always water left in the petri dish. On the final day, the output and transfer characteristics of the devices studied again, as shown in Fig. 5.7 and Fig. 5.8.

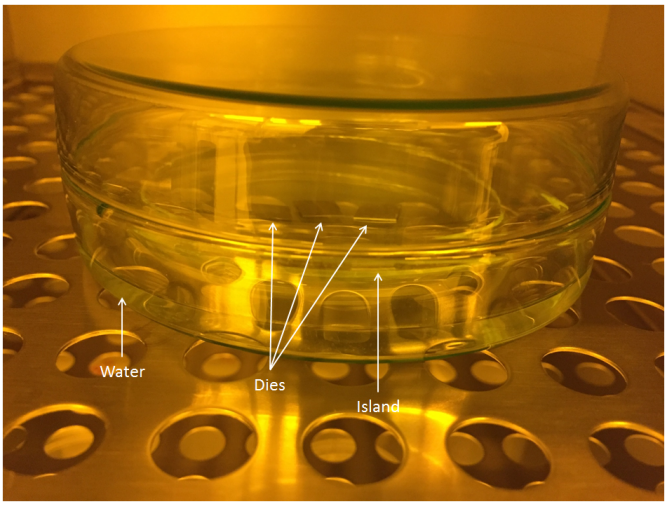


Figure 5.6: Incubation Setup

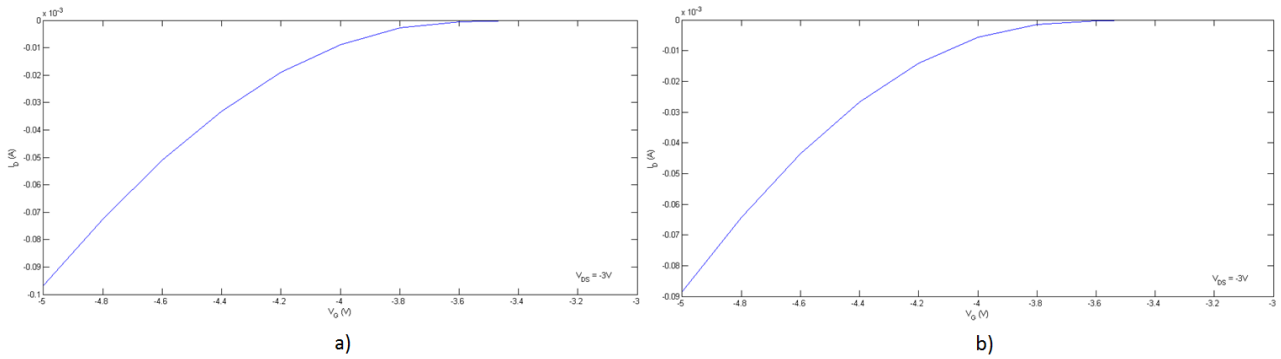


Figure 5.7: Measured transfer characteristics of the PMOS 2:25 a) before incubation and b) post incubation at 37°C and 90% humidity for 7 days.

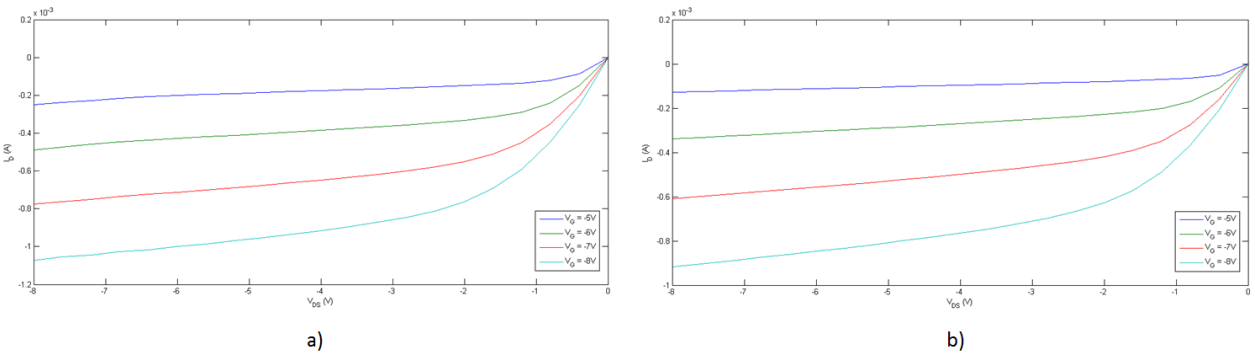


Figure 5.8: Measured output characteristics of the PMOS 2:25 a) before incubation and b) post incubation at 37°C and 90% humidity for 7 days.

As is evident from the PMOS characteristics here, the current seems to have degraded after incubation. However, the transistor behaviour was completely preserved. This further

proved the fact that it is in-fact better to encapsulate the sensing area from the rest of the device as humidity effects the electrical output of the ionic sensors.

5.3. DEVICE ELECTROCHEMICAL CHARACTERIZATION

Next, the electrochemical characterization of the device was performed using ionic solutions of varying concentrations. In order to limit the solution only to the sensing area, cloning cylinders made of ground borosilicate glass were attached onto the sensing areas of the dies. The gluing of the cylinders was done manually, die-by-die, using a medical grade two-component epoxy, EPOTEK 353ND-T. Then curing was done by baking the cylinder-attached dies in the oven at 75°C for 90 minutes.

It was observed at this stage that in some dies, the bondpads close to the sensing area were contaminated by epoxy bleeding during baking. This rendered the dies useless for electrochemical characterization, as the bondpads were covered in epoxy. This has been shown in Fig. 5.9

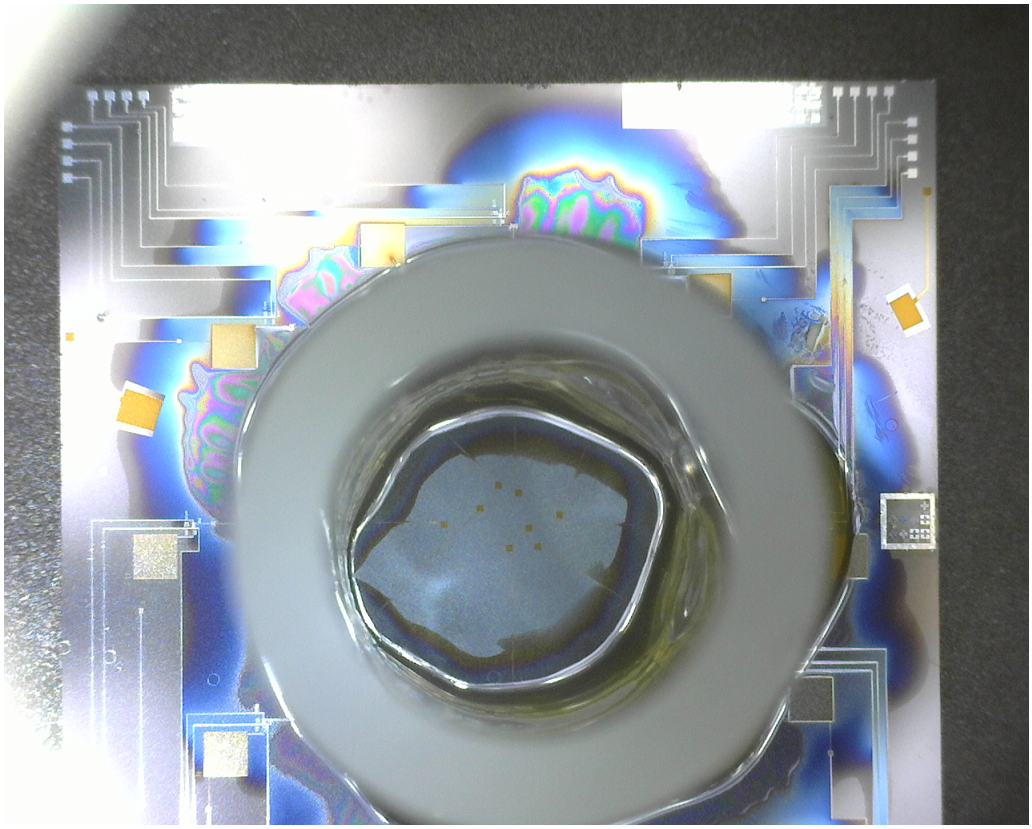


Figure 5.9: Epoxy bleeding in a cylinder attached die.

For the rest of the dies in which epoxy bleed hadn't contaminated the bondpads, like in Fig. 5.10, a leakage test was done using DI water so as to foresee any possible leaks that can cause the solution to leak-out and contaminate the bondpads. Once the leakage test was done, the dies were ready for electrochemical characterization.

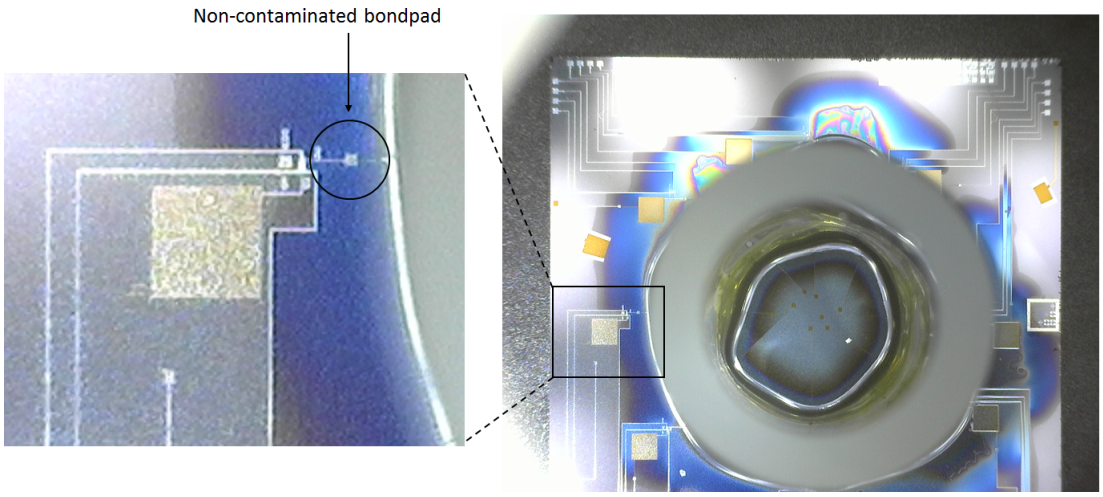


Figure 5.10: Example of a cylinder attached die with all bondpads intact.

5.3.1. ELECTROLYTE CONCENTRATIONS

Potassium (K^+) is the primary cation found within cells of the human body. An exchange of sodium and potassium across the muscle cells causes a gradient in the electric potential which is responsible for our heartbeat [58]. Due to the significance of potassium ions for such cardiovascular functions, a potassium based solution was chosen as the electrolyte for testing the Charge-modulated FGFET. The salt used for preparing the electrolyte was Potassium Chloride (KCl). However, it was only available as a 3M solution in pre-packaged bottles. Hence, using the dilution equation $C_1V_1 = C_2V_2$, different concentrations of the electrolyte were made using DI water and this 3M KCl solution as the reference. The different concentration parameters are listed in Tab 5.1.

Table 5.1: Electrolyte Concentration Values

C_1 (M)	V_1(µL)	C_2(µM)	V_2(mL)
3	1.5	300	15
	2.25	450	
	3	600	
	3.5	700	

These values of concentration were chosen for this study due to the resolution of the micropipette that was used to prepare the solution. Since the minimum resolution of the micropipette was 1µL, solution concentrations of lower than 200µM could not be prepared.

5.3.2. TRANSFER CHARACTERISTICS AT VARYING IONIC CONCENTRATIONS

Now that the solutions were prepared, one-by-one each solution was pipetted out into the cylinder and the dies were loaded into the Cascade 33 for measurements. Extreme care was taken to position the die and needles in a way so as to avoid collision of the probes with each other, and with the 8mm high cloning cylinder attached onto the die. A picture of the measurement set-up is shown in Fig. 5.11.

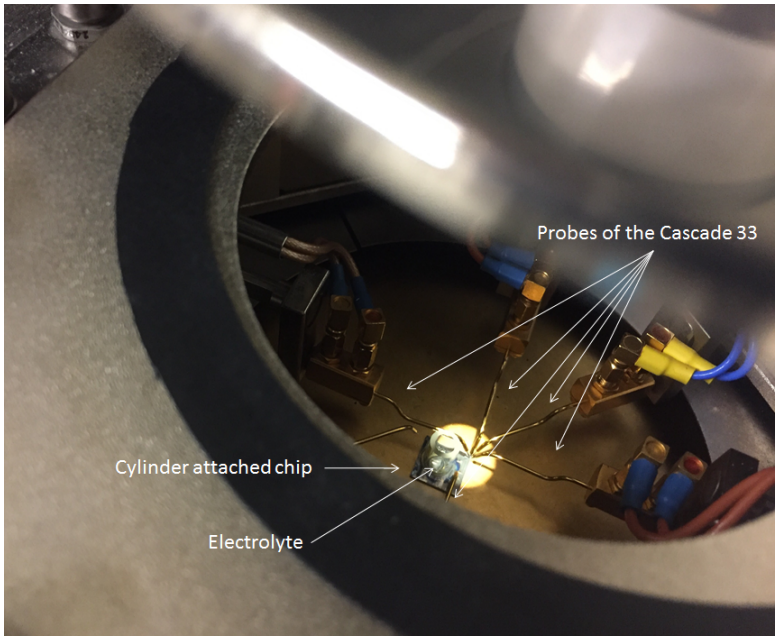


Figure 5.11: Electrochemical Measurement Setup in the Cascade 33.

Now to obtain the transfer characteristics at varying ionic concentrations of the electrolyte, it was necessary to sense the drain current for a given control-gate voltage. Just like the dry measurements, the gate voltage was swept from -5 to 5V. The substrate was biased at $0V$ and $V_{DS} = -3V$. However, this time, the reference biasing was done by biasing the control capacitor at 2V. The drain current was measured by the instrument simultaneously. The results have been shown in Fig. 5.12.

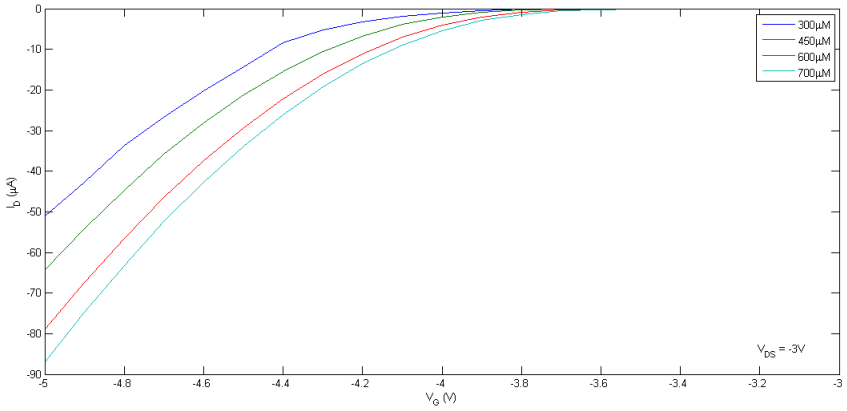


Figure 5.12: Transfer characteristics of the Charge-modulated FGFET, PMOS 2:25, for varying ionic concentrations.

As is clearly visible in the plot, the FGFET had a varying current response to changing surface charge density. Higher concentrations of the KCl solution provide for higher surface charge density in the sensing area. This causes charge separations in the floating gate which leads to a modulation of the threshold voltage of the device leading to an increase in

the drain current and thus bending the curve downwards.

Data was also obtained by biasing the capacitor at several different values of voltage (100mV, 1V, 2V, 4V, 6V). The device continued to respond with varying I_D values for different ionic concentrations. However, for uniformity of the plots in the report, and for simplicity purposes, data obtained at only one particular value of control biasing i.e. 2V was chosen to be plotted in this thesis.

To measure the sensitivity of the PMOS, it was essential to obtain the change in I_D at different ionic concentrations of the electrolyte w.r.t the reference I_D obtained from the transfer characteristics of the device without the presence of any electrolyte (Fig. 5.1). Hence the reference curve was plotted again, along with the transfer characteristics at different ionic concentrations and the drain current for varying concentrations was noted at a specific V_G value, -4.5V, as shown in Fig. 5.13. ΔI_D was calculated from this.

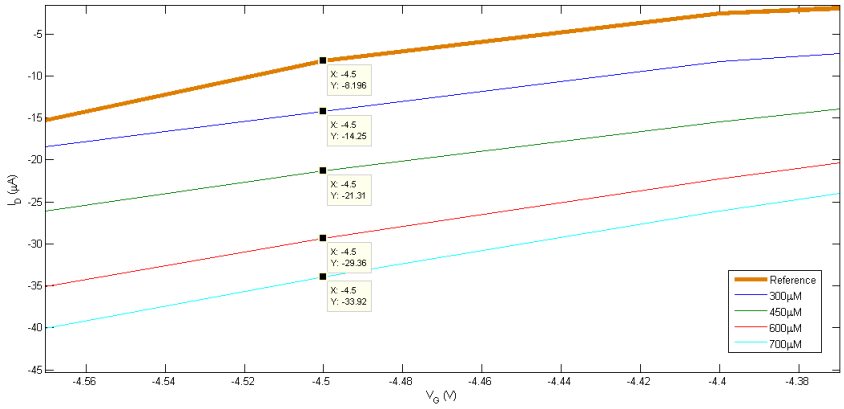


Figure 5.13: Plot to obtain ΔI_D for varying ionic concentrations, for the Charge-modulated FGFET, PMOS 2:25.

The calculated ΔI_D has been given in Table 5.2.

Table 5.2: ΔI_D for PMOS 2:25 at different ionic concentrations.

V_G (V)	Concentration (µM)	I_D(µA)	I_D (Reference)(µA)	ΔI_D (µA)
- 4.5	300	14.25	8.196	6.054
	450	21.31		13.114
	600	29.36		21.164
	700	33.92		25.724

Using this data, the calibration curve for the PMOS device was then plotted and has been shown in Fig. 5.14.

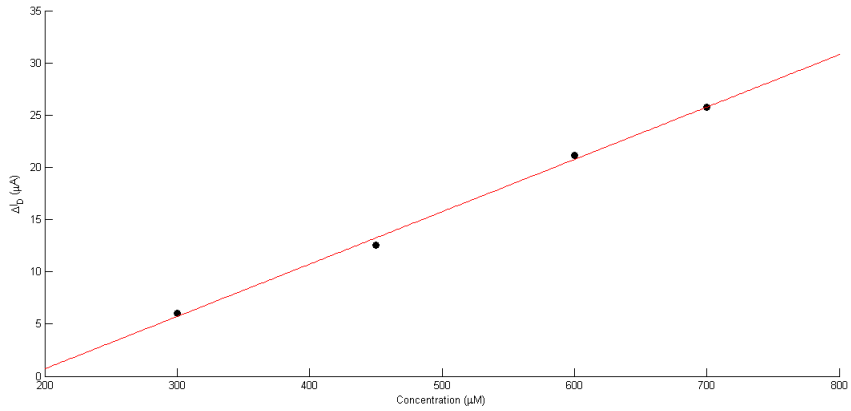


Figure 5.14: Calibration curve for the Charge-modulated FGFET, PMOS 2:25.

Calculating the slope of the calibration curve, the sensitivity of the PMOS was obtained at 0.04 ampere per molar concentration of solution, or 0.04A/M.

Similarly, the transfer characteristics for the NMOS was obtained at varying ionic concentrations of the electrolyte as shown in Fig. 5.15. The control capacitor was kept biased at 2V.

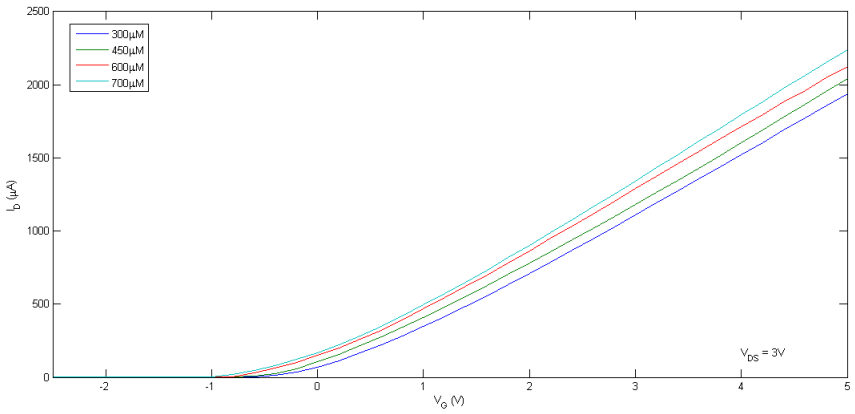


Figure 5.15: Transfer characteristics of the charge-modulated FGFET, NMOS 2:25, for varying ionic concentrations.

As can be seen here, the NMOS 2:25 has higher I_D output for corresponding change in electrolyte concentration than the PMOS 2:25. The current output is in the order of 1000 μA while for the PMOS 2:25, the output was in the order of 10 μA. This already suggests that the NMOS 2:25 should have higher sensitivity.

Now, similar to the PMOS device, to obtain the sensitivity, the reference transfer characteristic curve from Fig. 5.2 was plotted along side Fig. 5.15. The drain current for varying concentrations was noted at a specific V_G value, 4.5V, as shown in Fig. 5.16. ΔI_D was calculated from this and the results have been tabulated in Table 5.3.

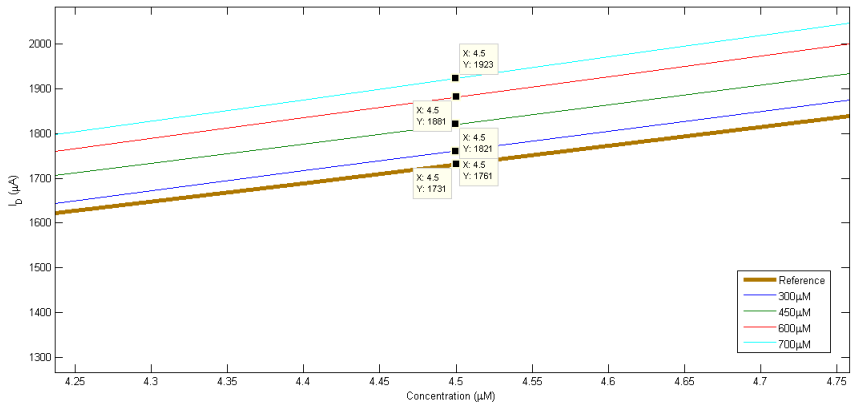


Figure 5.16: Obtaining ΔI_D from the transfer characteristics plot at varying concentrations of the electrolyte for the Charge-modulated FGFET, NMOS 2:25.

Table 5.3: ΔI_D for NMOS 2:25 at different ionic concentrations.

V_G (V)	Concentration (µM)	I_D(µA)	I_D (Reference)(µA)	ΔI_D (µA)
4.5	300	1761	1731	30
	450	1821		90
	600	1881		150
	700	1923		192

The calibration curve for the NMOS device is shown in Fig. 5.17.

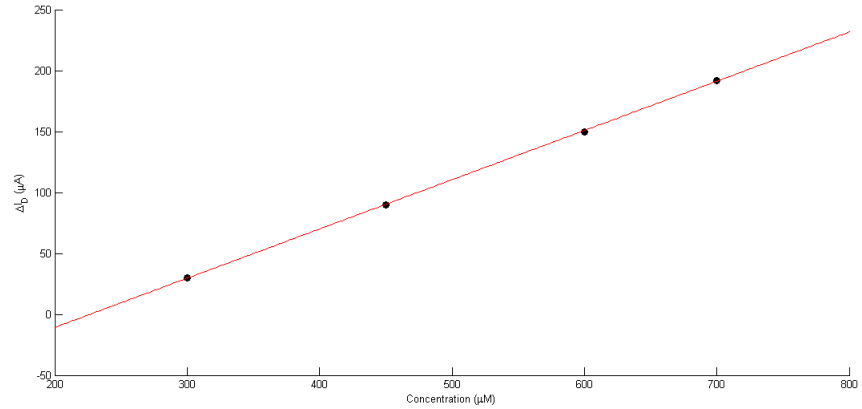


Figure 5.17: Calibration curve for the Charge-modulated FGFET, NMOS 2:25.

The slope of the calibration curve gave the sensitivity of the NMOS 2:25. This was calculated to be 0.4 ampere per molar concentration of solution or 0.4A/M.

5.4. DEVICE ELECTRICAL CHARACTERIZATION POST PDMS MEMBRANE RELEASE

The output and input characteristics of the NMOS 2:25 were measured again after the PDMS membrane release. The transfer characteristics was plotted alongside the curve from Fig. 5.2 while the output characteristics were plotted alongside Fig. 5.5 to verify the device functioning after the membrane was released. The results have been shown in Fig. 5.18 and Fig. 5.19.

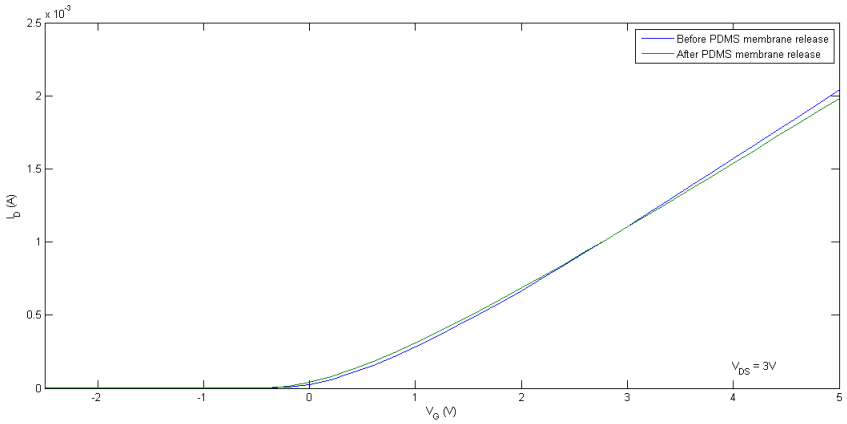


Figure 5.18: Transfer characteristics for the Charge-modulated FGFET, NMOS 2:25, before and after PDMS membrane release, plotted together.

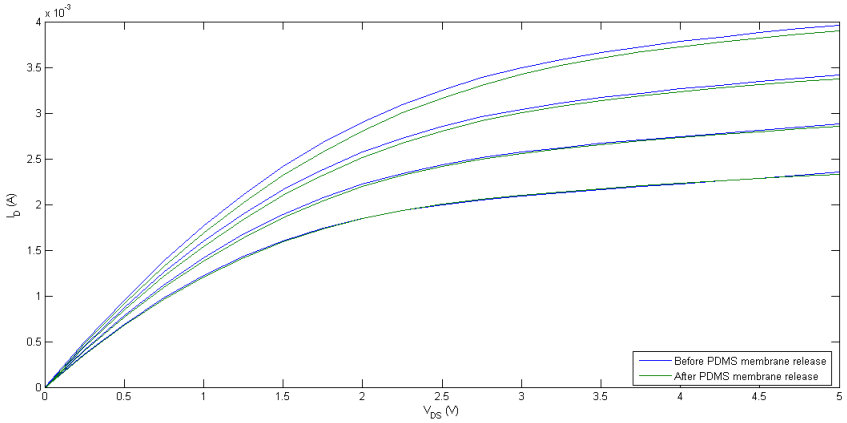


Figure 5.19: Ouput characteristics for the Charge-modulated FGFET, NMOS 2:25, before and after PDMS membrane release, plotted together.

As can be seen from the curves, there appeared to have been no significant change in the transistor characteristics of the device even after the PDMS membrane release. All the characteristics are completely preserved, which proves the device's potential to be integrated into a stretchable OOC platform.

5.5. DISCUSSION

As can already be observed from Fig. 5.15, the NMOS 2:25 has better sensitivity than the PMOS 2:25. The device exhibits higher change in current in the order of 100 μA, for corresponding change in concentration of ions in the electrolyte. This is further proved to be true via the calibration curve, where-in the plot is almost completely linear. Further the measured sensitivity of the NMOS 2:25 (0.4 A/M) was also 10 times better than the PMOS 2:25 (0.04 A/M), as was also observed from the calibration curves of the two devices. This can possibly be attributed to the better inherent V_{TH} of the NMOS devices, as was discussed earlier. This can be made better by modifying the implantation dosage of the doped regions during the microfabrication process. It might also be beneficial to decrease the gate insulator thickness to obtain a lower threshold voltage and thus increased drain current change. Body effect of the MOSFET could also play a role since the NMOS is fabricated in the bulk of the substrate itself while the PMOS is fabricated in the n-well regions implanted within the p-type substrate.

Further, all transistor characteristics were perfectly preserved, even after membrane release. This exhibits the fact that the device could be integrated into flexible OOC platforms in the future.

5.6. CONCLUSION

The Charge-modulated FGFET exhibited the ability to sense the change in drain current for a given control-gate voltage. This proved the device's ability to be used without the means of a reference electrode for biasing, since the working point of the device was set by means of the control capacitor. Further, the NMOS devices were 10 times more sensitive and had better electrical response than the PMOS. The NMOS device characteristics also remained almost completely unharmed, after the PDMS membrane deposition and release. This makes the NMOS configuration of the Charge-modulated FGFET more desirable for large-scale-of-integration capabilities in OOC platforms.

6

Conclusion and Future Scope

In this thesis, a novel FGFET based ion sensor was fabricated that is capable of detecting changes in ionic concentrations occuring in the sensing area. The need for a reference electrode is eliminated, as biasing the control capacitor sets the working point of the device. This provides for low-cost standard CMOS fabrication. Further the gate electrodes are suspended on a free standing PDMS membrane, which validates the Charge-modulated FGFET's ability to be integrated into a stretchable OOC platform.

However, in this study, it was only possible to do the device electrochemical characterization before the PDMS membrane deposition and not after membrane release. It would be beneficial to design another individual mask to be able to open the bondpads after PDMS deposition. The chip would have to be flipped over before the cloning cylinder is attached to the die. This would allow the gate electrode extensions on the suspended membrane to be in contact with the electrolyte. This has been illustrated in Fig. 6.1

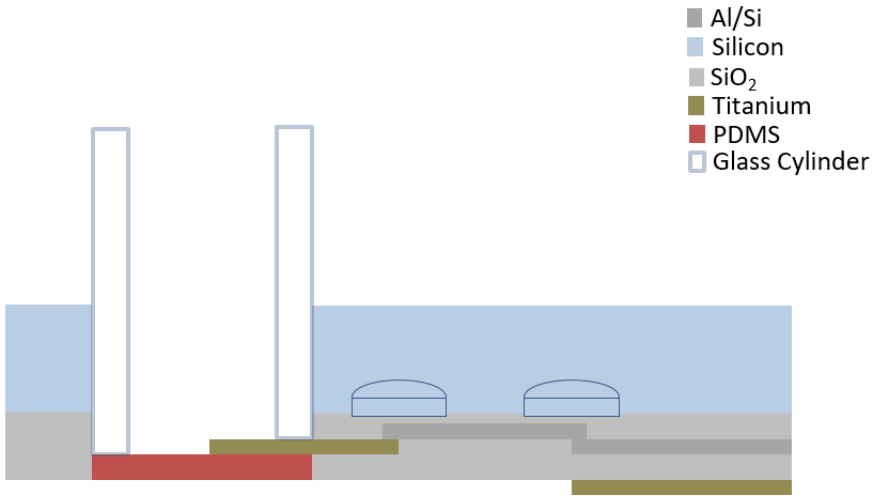


Figure 6.1: Possible setup for electrochemical characterization after membrane release. The chip is flipped over and the cylinder attached to the backside of the die.

However, this would also mean that the bondpads for measurements would be behind the chip. Hence, measurements in Cascade 33 won't be possible anymore as the backside of the chip faces the chuck and is held in place using vacuum. As an alternative, a PCB could be designed and the bondpads could be soldered to the PCB. This would enable easier electrical and electrochemical characterization. In addition, since the cylinder would be attached to the backside of the chip, this prevents the bondpads, on the front side, from being contaminated by epoxy bleeding. Thus the frontside would remain completely unharmed from external factors. It could also be interesting to measure the characteristics of the other MOSFET transistors with varying W/L ratio to study the effect of channel length modulation on the sensitivity of the Charge-modulated FGFET.

It could also be possible to investigate the application of other flexible conductive materials for the fabrication of the gate electrode extensions. Since the membrane itself is stretchable, this would further reduce the strain on the electrodes during bending. This could provide for a reasonably high-quality ion-sensing device for already available stretchable OOC platforms.

A

Mask Design

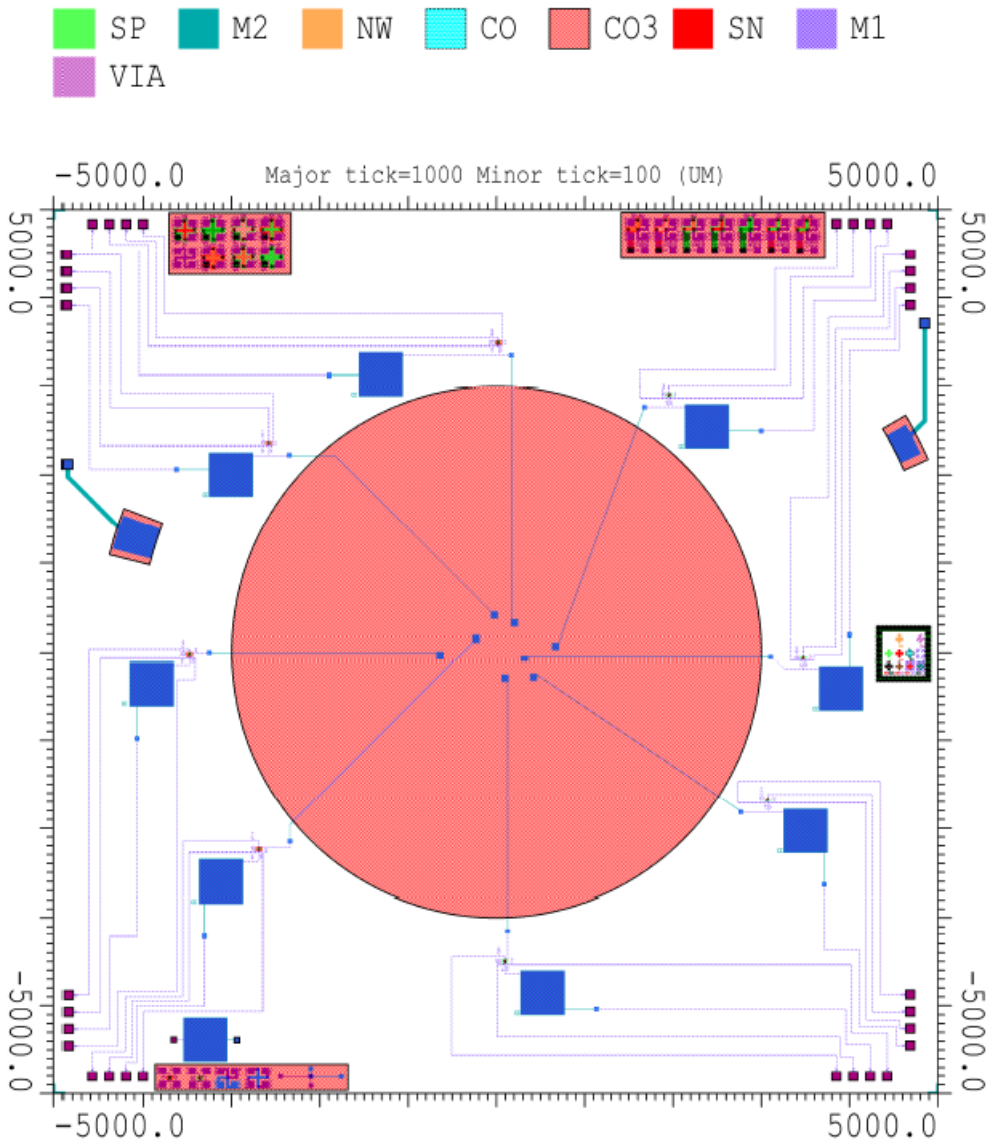


Figure A.1: Full mask layout with all layers.

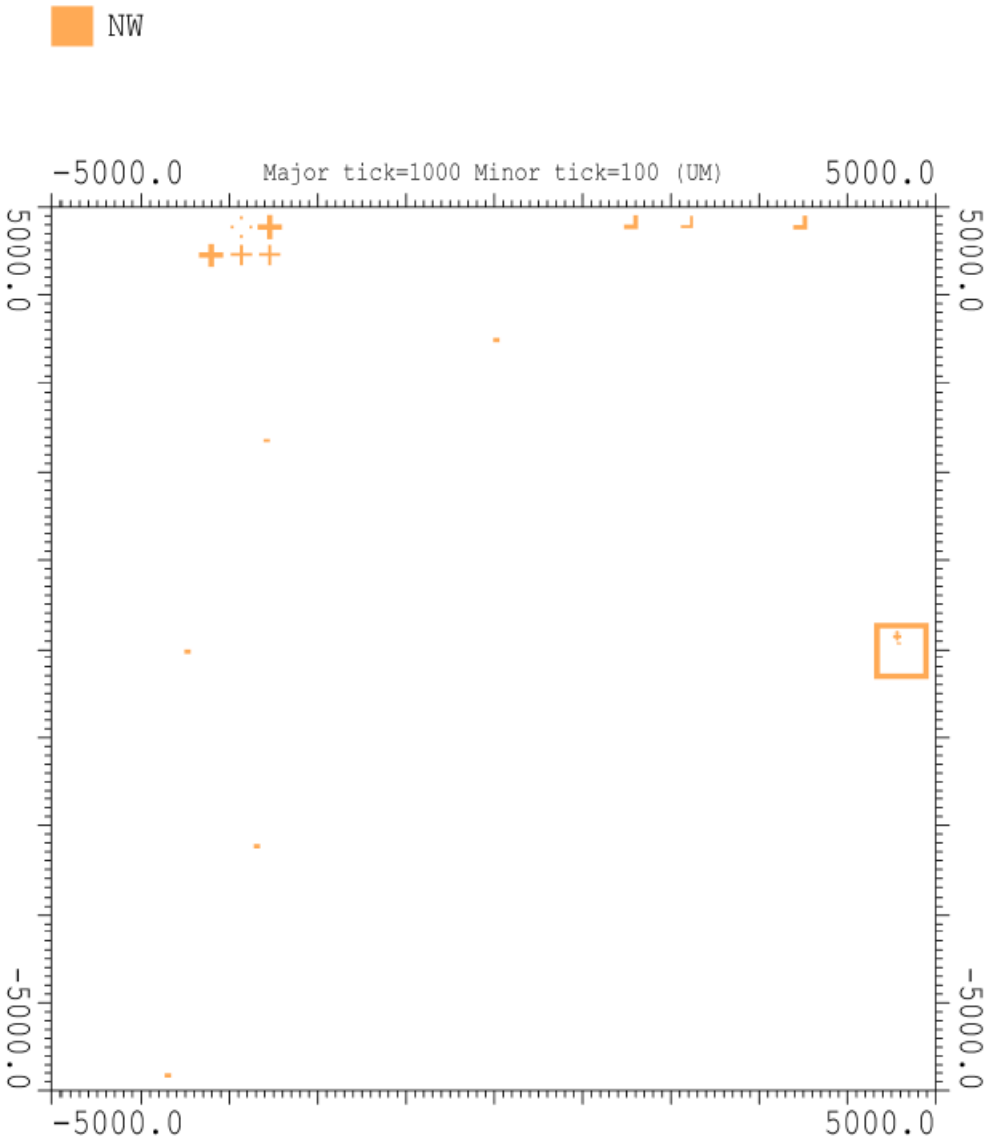


Figure A.2: Mask design for the N-Well definition.

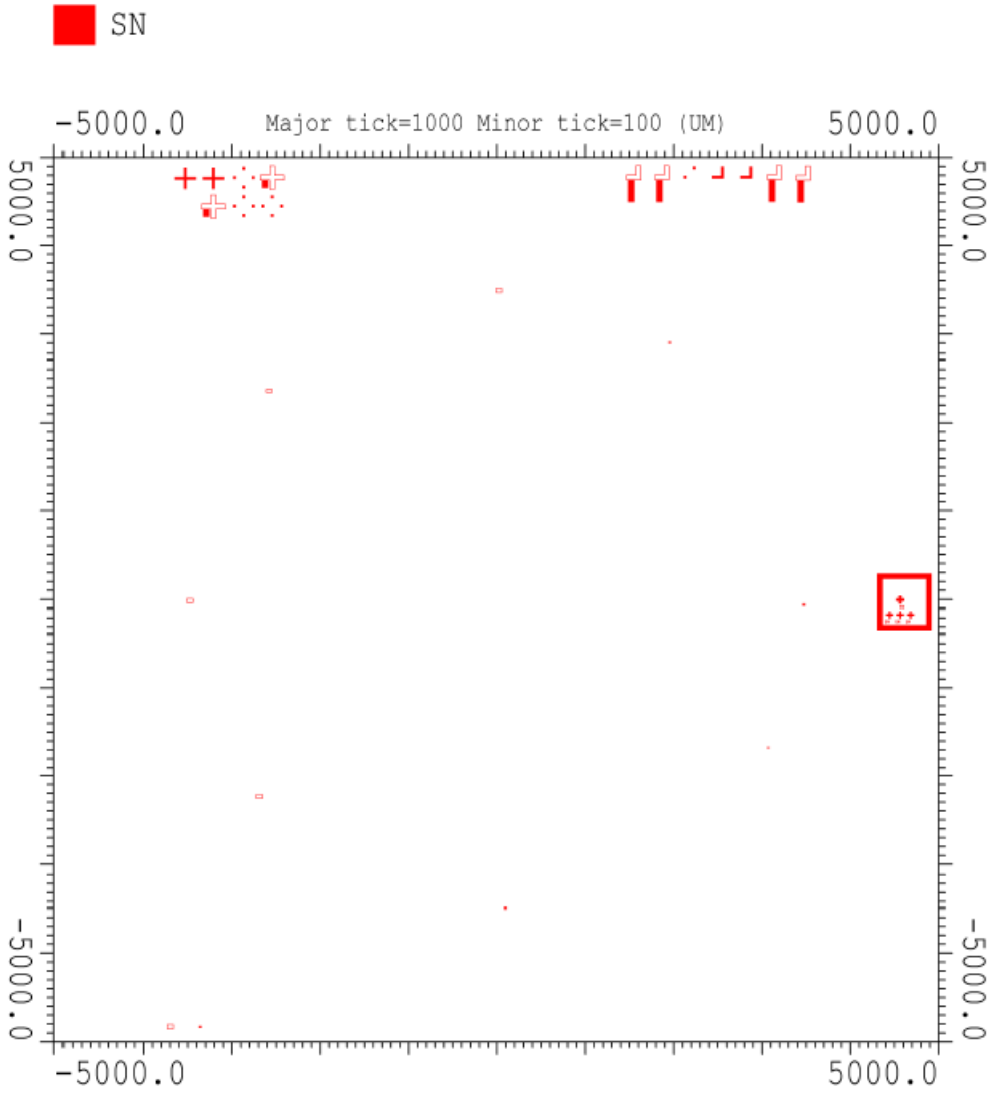


Figure A.3: Mask design for the shallow-N layer definition.

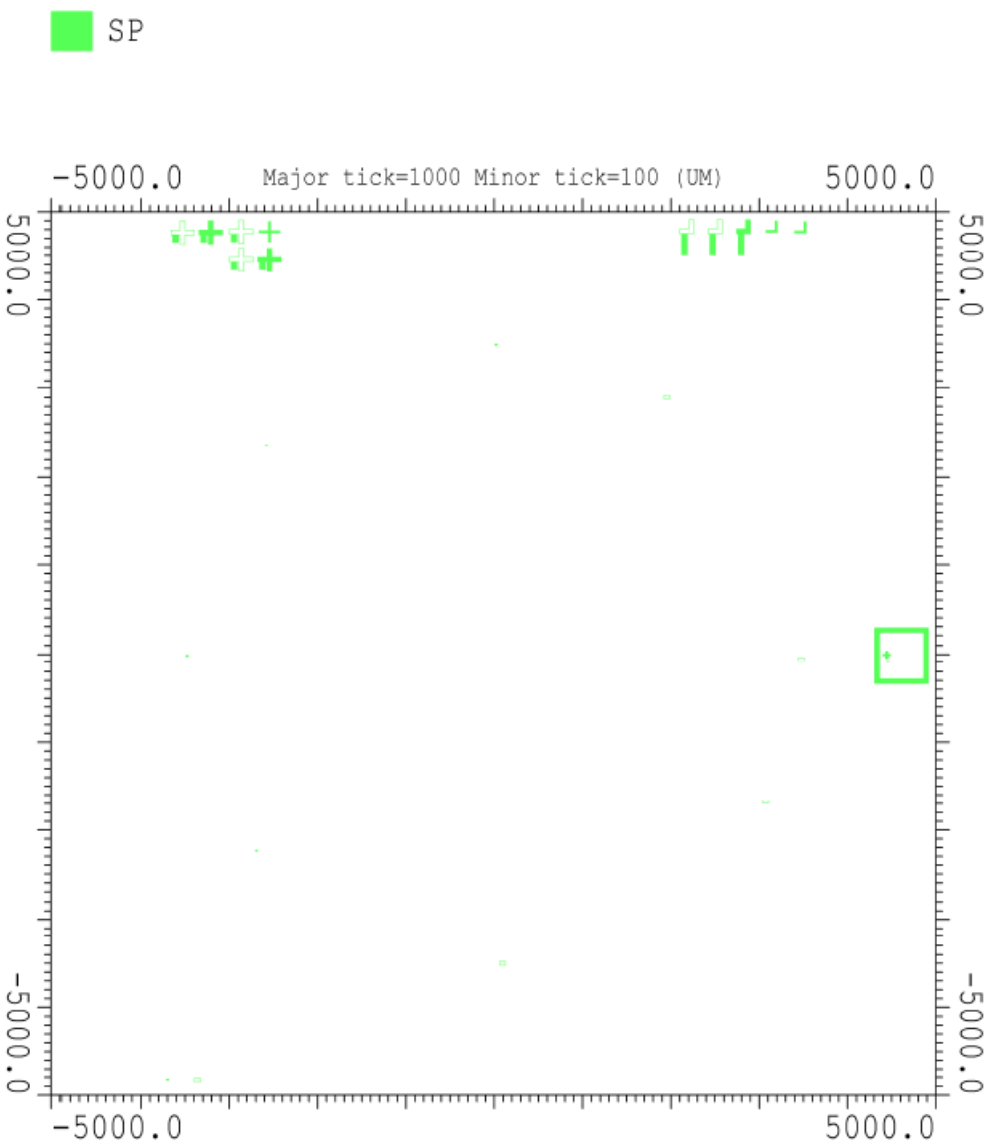


Figure A.4: Mask design for the shallow-P layer definition.

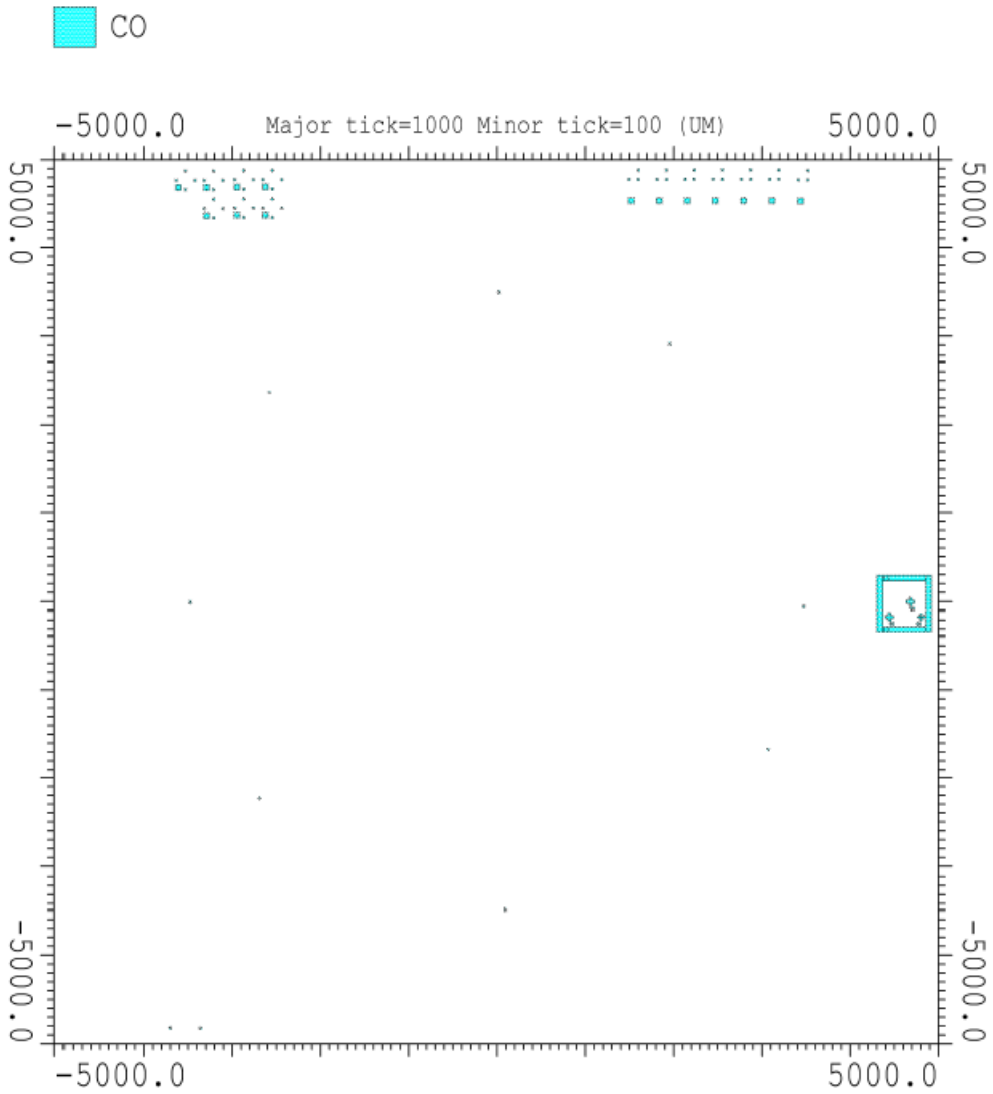


Figure A.5: Mask design for the contact openings in the gate oxide before first metalization.

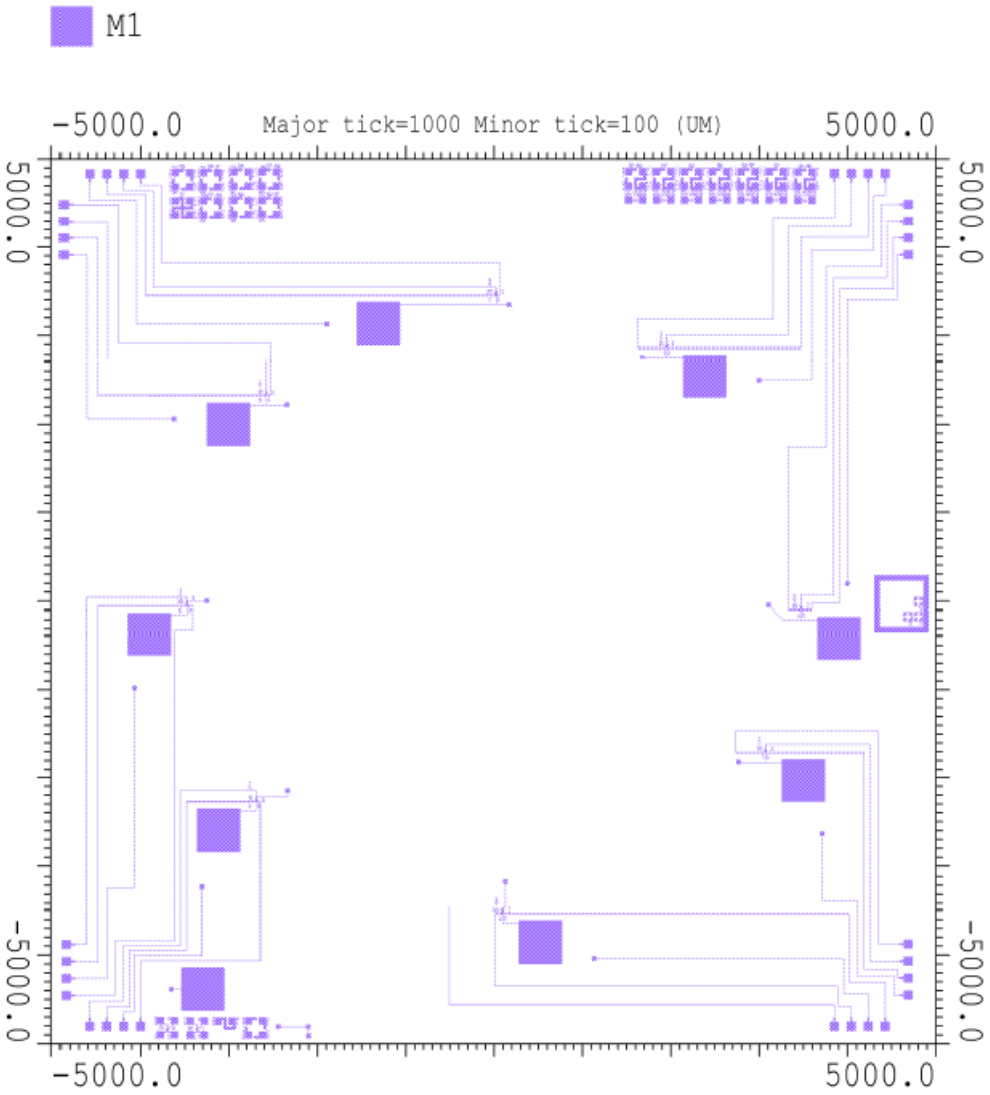


Figure A.6: Mask design for the IC definition.

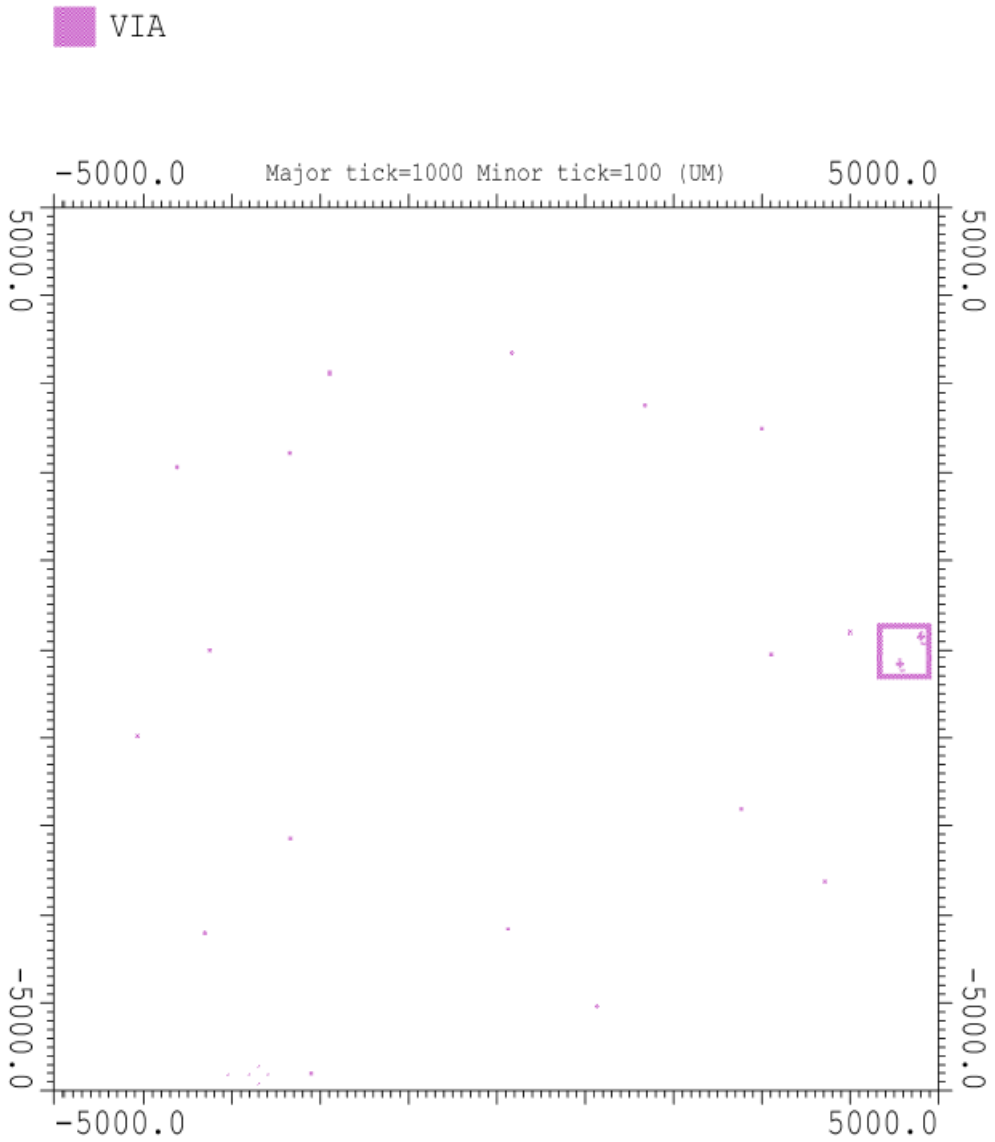


Figure A.7: Mask design for defining the vias in the oxide layer before second metalization.

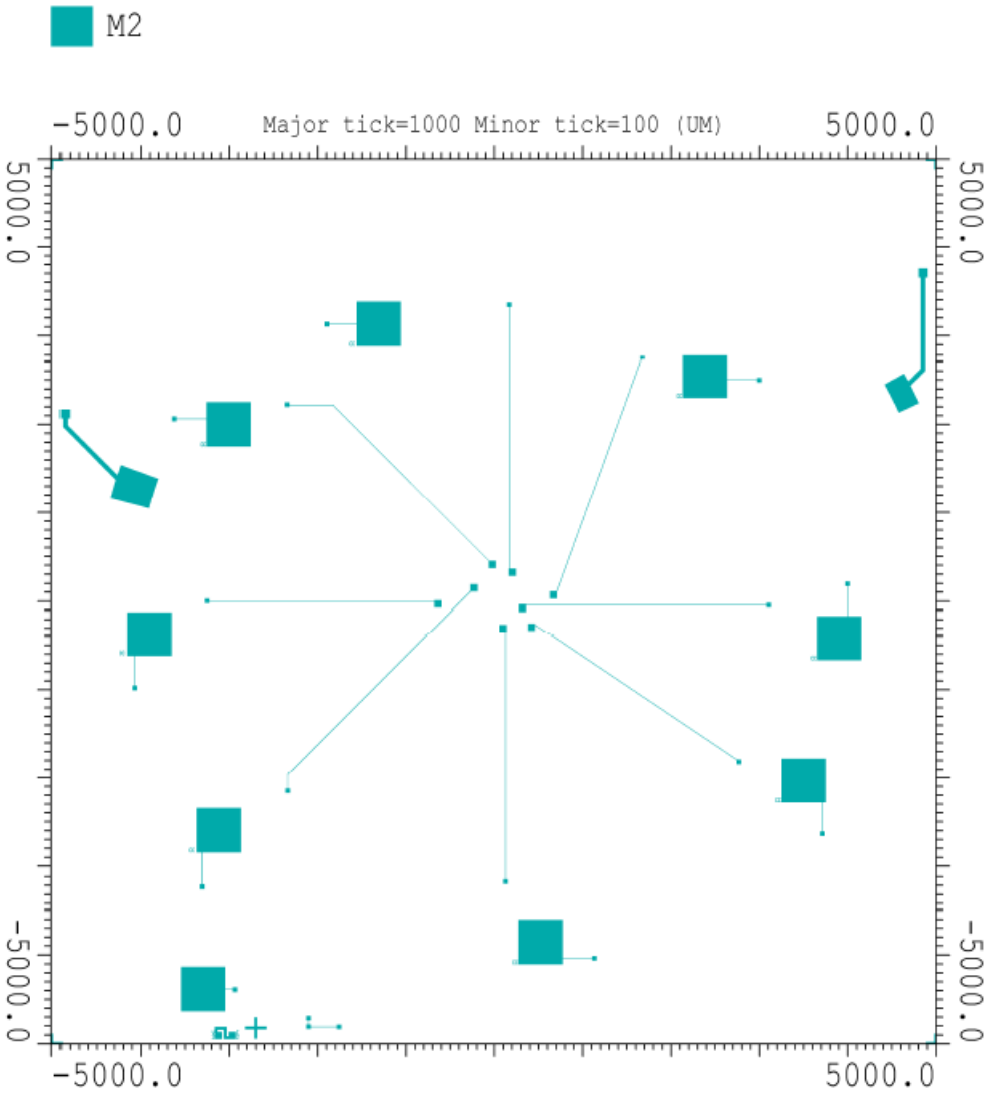


Figure A.8: Mask design for the titanium patterning.

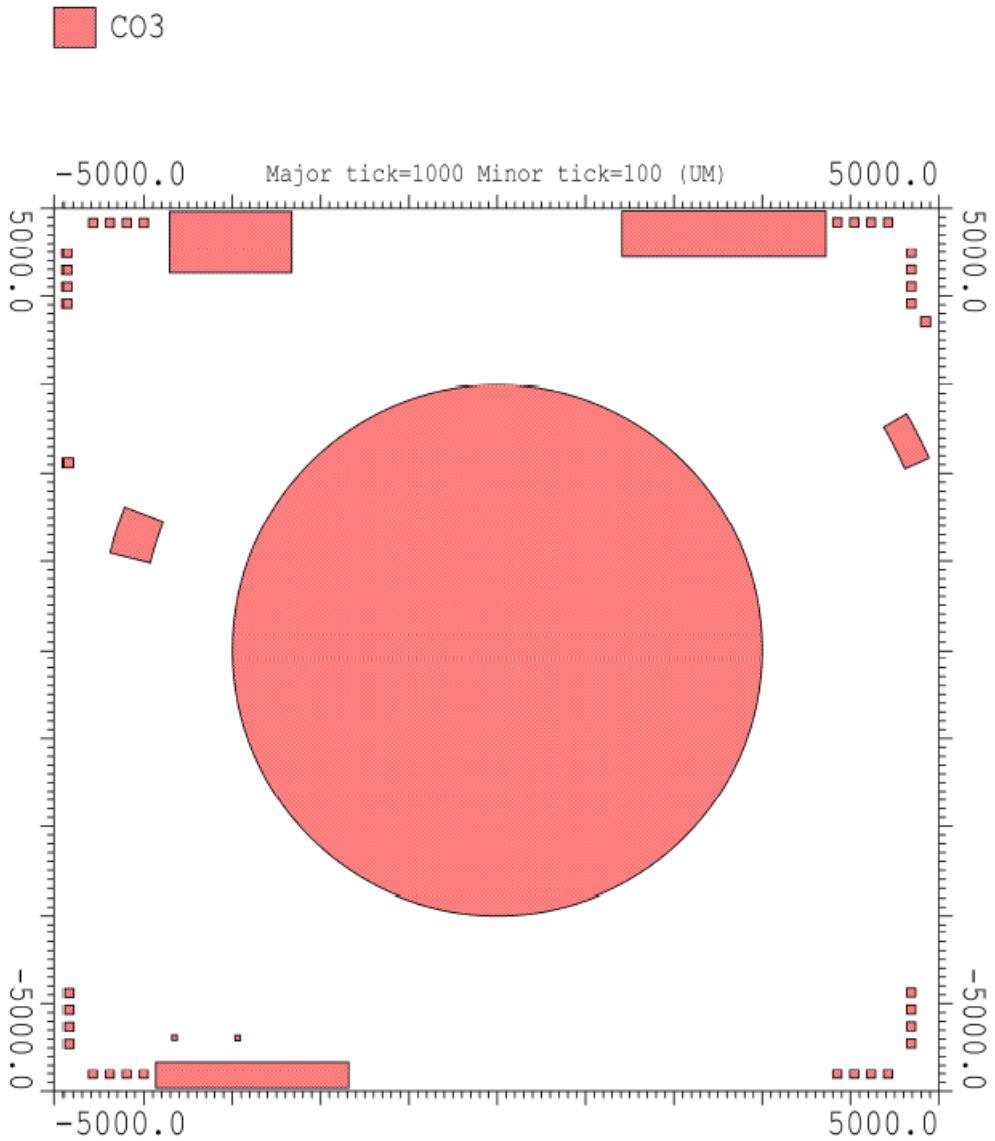


Figure A.9: Mask design for defining the contacts opening for the bondpads and the sensing area for electrical characterization.

B

Detailed Flowchart

Starting Material

10 Single side polished (L_{RES}) wafers with the following specifications:

Type: p/B (p-type, boron)
Orientation: <100>
Resistivity: 2-5ωcm
Thickness: 525 µm
Diameter: 100mm

1. CLEANING: HNO_3 99% and 69.5%

- Clean: 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use wet bench "HNO_3 99% (Si) and the carrier with red dot.
- Rinse: Rinse in the Quick Dump Rinser with the standard program until resistivity is 5MΩ.
- Clean: 10 minutes in concentrated nitric acid at 110°C. This will dissolve metal particles. Use wet bench "HNO_3 69.5, 110C% and the carrier with the red dot.
- Rinse: Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5MΩ.
- Dry: Use the Semitool "rinser/dryer" with the standard program and the white carrier with a red dot.

2. COATING AND BAKING

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:

- A treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas.

- Spin coating of Shipley SPR3012 positive resist, dispensed by a pump.
- A soft bake at 95°C for 90 seconds.
- An automatic edge bead removal with a solvent

Always check the relative humidity (48 ± 2%) in the room before coating, and follow the instructions for this equipment.
Use program "Co - 3012 - zero layer". There will be a larger edge bead removal.

3. ALIGNMENT AND EXPOSURE

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper.
Follow the operating instructions from the manual when using this machine.

Expose masks COMURK, with job "ZEFWAM" and the correct exposure energy 125mJ.
This results in alignment markers for the stepper and contact aligner.

4. DEVELOPING

Use the developer station of the EVG120 system to develop the wafers. The process consists of:

- A post-exposure bake at 115°C for 90 seconds.
- Developing with Shipley MF322 with a single puddle process
- A hard bake at 100°C for 90 seconds

Always follow the instructions for this equipment.
Use program "Dev - SP".

5. INSPECTION: Linewidth and Overlay

Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

6. PLASMA ETCHING: Alignment markers (URKs) in Silicon

Use the Trikon Ωmega 201 plasma etcher.
Follow the operating instructions from the manual when using this machine.
It is not allowed to change the process conditions and times from the etch recipe!

Use sequence URK_NPD (with a platen temperature of 20°C) to etch 120nm deep ASM URK's into the Si.

7. LAYER STRIPPING: Photoresist

Strip resist: Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use program 1: 1000 watts power and automatic endpoint detection + 2 min. overetching.

8. CLEANING: HNO_3 99% and 69.5%

- Clean: 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use wet bench "HNO_3 99% (Si) and the carrier with red dot.
- Rinse: Rinse in the Quick Dump Rinser with the standard program until resistivity is 5MΩ.
- Clean: 10 minutes in concentrated nitric acid at 110°C. This will dissolve metal particles. Use wet bench "HNO_3 69.5, 110C% and the carrier with the red dot.
- Rinse: Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5MΩ.
- Dry: Use the Semitool "rinser/dryer" with the standard program and the white carrier with a red dot.

9. DRY OXIDATION: DIRT BARRIER

Furnace no: A1
Program name: DIBARVAR
Total time: 1 hr 50 min
Oxidation time: 35 min
Program no: N13

10. MEASUREMENT: OXIDE THICKNESS

Use the Leitz MPV-SP measurement system to measure the oxide thickness:

Program: Th. SiO2 on Si, <50nm auto5pts
Oxide thickness: 20-22 nm

11. COATING AND BAKING

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:

- A treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas.
- Spin coating of Shipley SPR3012 positive resist, dispensed by a pump.
- A soft bake at 95°C for 90 seconds.
- An automatic edge bead removal with a solvent

Always check the relative humidity (48 ± 2%) in the room before coating, and follow the instructions for this equipment.
Use program "Co - 3012 - 2.1µm".

12. ALIGNMENT AND EXPOSURE

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper.
Follow the operating instructions from the manual when using this machine.

Use the mask “EC2204-V1_NW-SN-SP-CO” in box 486, jobname “Diesize_10mm/DIE10x10_4IMG”, layer “IMAGE 03”, with an energy of 320 $mJcm^{-2}$.

13. DEVELOPING

Use the developer station of the EVG120 system to develop the wafers. The process consists of:

- A post-exposure bake at 115°C for 90 seconds.
- Developing with Shipley MF322 with a single puddle process
- A hard bake at 100°C for 90 seconds

Always follow the instructions for this equipment.
Use program "Dev - SP".

14. INSPECTION: Linewidth and Overlay

Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

15. PHOSPHORUS IMPLANTATION: N-WELL DEFINITION

Use the Ion Implanter.
Follow the operating instructions from the manual when using this machine.

Ion: P^+
Energy: 150keV
Dose: 6.0E12 ions/cm^2

16. LAYER STRIPPING: Photoresist

Strip resist: Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use program 1: 1000 watts power and automatic endpoint detection + 2 min. overetching.

17. CLEANING: HNO_3 99% and 69.5%

- Clean: 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use wet bench "HNO_3 99% (Si) and the carrier with red dot.
- Rinse: Rinse in the Quick Dump Rinser with the standard program until resistivity is 5MΩ.
- Clean: 10 minutes in concentrated nitric acid at 110°C. This will dissolve metal particles. Use wet bench "HNO_3 69.5, 110C% and the carrier with the red dot.
- Rinse: Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5MΩ.
- Dry: Use the Semitool "rinser/dryer" with the standard program and the white carrier with a red dot.

18. ANNEALING: N-WELL DRIVE IN

Furnace no: A1
Program name: OA002
Total time: 6 hr 55 min
Program no: N5

19. MEASUREMENT: OXIDE THICKNESS

Use the Leitz MPV-SP measurement system to measure the oxide thickness:

Program: Th. SiO2 on Si, >50nm auto5pts
Oxide thickness: 200-250 nm

20. OXIDE STRIPPING

- Etchant: Use wetbench “BHF (1:7)”; use the carrier with the blue dot.
- Etch time: Depends on the oxide thickness and composition. Etch until the whole wafer is hydrophobic. The etch rate of thermally grown oxide is 1.3 ± 0.2 nm/s at 20°C.
- QDR: Rinse in the Quick Dump Rinser with the standard programe until the resistivity is 5MΩ.
- Rinse: Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5MΩ.
- Drying: Use the µProcess Avenger with the standard program, and the white carrier with a red dot.

21. CLEANING: HNO_3 99% and 69.5%

- Clean: 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use wet bench "HNO_3 99% (Si) and the carrier with red dot.
- Rinse: Rinse in the Quick Dump Rinser with the standard program until resistivity is 5MΩ.
- Clean: 10 minutes in concentrated nitric acid at 110°C. This will dissolve metal particles. Use wet bench "HNO_3 69.5, 110C% and the carrier with the red dot.
- Rinse: Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5MΩ.
- Dry: Use the Semitool "rinser/dryer" with the standard program and the white carrier with a red dot.

22. DRY OXIDATION: DIRT BARRIER

Furnace no: A1
Program name: DIBARVAR
Total time: 1 hr 50 min
Oxidation time: 35 min
Program no: N13

23. MEASUREMENT: OXIDE THICKNESS

Use the Leitz MPV-SP measurement system to measure the oxide thickness:

Program: Th. SiO2 on Si, <50nm auto5pts
Oxide thickness: 20-25 nm

24. COATING AND BAKING

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:

- A treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas.
- Spin coating of Shipley SPR3012 positive resist, dispensed by a pump.
- A soft bake at 95°C for 90 seconds.
- An automatic edge bead removal with a solvent

Always check the relative humidity (48 ± 2%) in the room before coating, and follow the instructions for this equipment.
Use program "Co - 3012 - 1.4µm".

25. ALIGNMENT AND EXPOSURE

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper.
Follow the operating instructions from the manual when using this machine.

Use the mask “EC2204-V1_NW-SN-SP-CO” in box 486, jobname “Diesize_10mm/DIE10x10_4IMG”, layer “IMAGE 04”, with an energy of 120 $mJcm^{-2}$.

26. DEVELOPING

Use the developer station of the EVG120 system to develop the wafers. The process consists of:

- A post-exposure bake at 115°C for 90 seconds.
- Developing with Shipley MF322 with a single puddle process
- A hard bake at 100°C for 90 seconds

Always follow the instructions for this equipment.
Use program "Dev - SP".

27. INSPECTION: Linewidth and Overlay

Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

28. ARSENIC IMPLANTATION: SN DEFINITION

Use the Ion Implanter.
Follow the operating instructions from the manual when using this machine.

Ion: As^+
Energy: 40keV
Dose: 5.0E15 ions/cm^2

29. LAYER STRIPPING: Photoresist

Strip resist: Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use program 1: 1000 watts power and automatic endpoint detection + 2 min. overetching.

30. CLEANING: HNO_3 99% and 69.5%

- Clean: 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use wet bench "HNO_3 99% (Si) and the carrier with red dot.
- Rinse: Rinse in the Quick Dump Rinser with the standard program until resistivity is 5MΩ.

- Clean: 10 minutes in concentrated nitric acid at 110°C. This will dissolve metal particles. Use wet bench "HNO_3 69.5, 110C% and the carrier with the red dot.
- Rinse: Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5MΩ.
- Dry: Use the Semitool "rinser/dryer" with the standard program and the white carrier with a red dot.

31. COATING AND BAKING

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:

- A treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas.
- Spin coating of Shipley SPR3012 positive resist, dispensed by a pump.
- A soft bake at 95°C for 90 seconds.
- An automatic edge bead removal with a solvent

Always check the relative humidity (48 ± 2%) in the room before coating, and follow the instructions for this equipment.
Use program "Co - 3012 - 1.4µm".

32. ALIGNMENT AND EXPOSURE

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper.
Follow the operating instructions from the manual when using this machine.

Use the mask “EC2204-V1_NW-SN-SP-CO” in box 486, jobname “Diesize_10mm/DIE10x10_4IMG”, layer “IMAGE 01”, with an energy of 120 $mJcm^{-2}$.

33. DEVELOPING

Use the developer station of the EVG120 system to develop the wafers. The process consists of:

- A post-exposure bake at 115°C for 90 seconds.
- Developing with Shipley MF322 with a single puddle process
- A hard bake at 100°C for 90 seconds

Always follow the instructions for this equipment.
Use program "Dev - SP".

34. INSPECTION: Linewidth and Overlay

Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

35. BORON IMPLANTATION: SP DEFINITION

Use the Ion Implanter.
Follow the operating instructions from the manual when using this machine.

Ion: B^+
Energy: 15keV
Dose: 5.0E15 ions/cm^2

36. LAYER STRIPPING: Photoresist

Strip resist: Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use program 1: 1000 watts power and automatic endpoint detection + 2 min. overetching.

37. CLEANING: HNO_3 99% and 69.5%

- Clean: 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use wet bench "HNO_3 99% (Si) and the carrier with red dot.
- Rinse: Rinse in the Quick Dump Rinser with the standard program until resistivity is 5MΩ.
- Clean: 10 minutes in concentrated nitric acid at 110°C. This will dissolve metal particles. Use wet bench "HNO_3 69.5, 110C% and the carrier with the red dot.
- Rinse: Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5MΩ.
- Dry: Use the Semitool "rinser/dryer" with the standard program and the white carrier with a red dot.

38. ANNEALING: OXIDATION

Furnace no: C1
Program name: ICTOXA
Total time: 2 hr 25 min
Program no: N6

39. MEASUREMENT: OXIDE THICKNESS

Use the Leitz MPV-SP measurement system to measure the oxide thickness:

Program: Th. SiO2 on Si, >50nm auto5pts
Oxide thickness: 97-104 nm on undoped areas; 210 nm on NW, SN and SP doped areas

40. COATING AND BAKING

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:

- A treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas.
- Spin coating of Shipley SPR3012 positive resist, dispensed by a pump.
- A soft bake at 95°C for 90 seconds.
- An automatic edge bead removal with a solvent

Always check the relative humidity (48 ± 2%) in the room before coating, and follow the instructions for this equipment.
Use program "Co - 3012 - 1.4µm".

41. ALIGNMENT AND EXPOSURE

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper.
Follow the operating instructions from the manual when using this machine.

Use the mask “EC2204-V1_NW-SN-SP-CO” in box 486, jobname “Diesize_10mm/DIE10x10_4IMG”, layer “IMAGE 02”, with an energy of 120 $mJcm^{-2}$.

42. DEVELOPING

Use the developer station of the EVG120 system to develop the wafers. The process consists of:

- A post-exposure bake at 115°C for 90 seconds.
- Developing with Shipley MF322 with a single puddle process
- A hard bake at 100°C for 90 seconds

Always follow the instructions for this equipment.
Use program "Dev - SP".

43. INSPECTION: Linewidth and Overlay

Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

44. WINDOW ETCHING

- Rinse: Use wetbench "H2O/TRITON X-100" and the special carrier with the blue dot; added to the tank: 1 ml Triton X-100 per 5000 ml demi water. Rinse for 1 minute.
- Etchant: Use wetbench "BHF (1:7)"; use the carrier with the blue dot.
- Etch time: The oxide in the SN regions is about 200 nm thick, the oxide thickness outside the SN regions and on the backside of the wafer is about 100 nm thick. Therefore, the required etch-time for the CO-SN combinations is about twice the time to obtain a hydrophobic back side of the wafer. Etch till the CO-windows in the SN areas are open.
- QDR: Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5MΩ.
- Drying: Use the µProcess Avenger with the standard program, and the white carrier with a red dot.

45. INSPECTION

Visually inspect the wafers through a microscope, and check if the contact openings are indeed open.

46. MEASUREMENT: OXIDE THICKNESS

Use the Leitz MPV-SP measurement system to measure the oxide thickness:

Program: Th. SiO2 on Si, >50nm auto5pts
Oxide thickness: 0nm on CO windows

47. RESIST STRIPPING AND CLEANING: ACETONE, HNO_3 99% and 69.5%

- Strip Resist: Use wet bench "Acetone" and the carrier with two red dots.
  Dissolve the PR in acetone, temp 40°C. Time = ±1 min.
- Clean: 10 minutes in fuming nitric acid at ambient temperature. This will dissolve organic materials. Use wet bench "HNO_3 99% (Si) and the carrier with red dot.
- Rinse: Rinse in the Quick Dump Rinser with the standard program until resistivity is 5MΩ.
- Clean: 10 minutes in concentrated nitric acid at 110°C. This will dissolve metal particles. Use wet bench "HNO_3 69.5, 110C% and the carrier with the red dot.
- Rinse: Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5MΩ.
- Dry: Use the Semitool "rinser/dryer" with the standard program and the white carrier with a red dot.

48. MARANGONI

- Etchant: Standard 0.55% HF solution
- Etch time: 4 minutes
- QDR: Rinse in DI Water : IPA

49. ALUMINUM SPUTTERING: FIRST METALLIZATION

Use the TRIKON SIGMA sputter coater for the deposition of an aluminum metal layer on the wafers.
The target must exist of 99% Al and 1% Si, and deposition must be done at 25°C. Follow the operating instructions from the manual when using this machine.

Use recipe “AlSi_675nm_25” to sputter a 600 nm thick layer.

Note: Check the wafers after aluminum deposition. Metal residuals should be not present on the edge neither on the frontside nor the backside of the wafer.

50. COATING AND BAKING

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:

- A treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas.
- Spin coating of Shipley SPR3012 positive resist, dispensed by a pump.
- A soft bake at 95°C for 90 seconds.
- An automatic edge bead removal with a solvent

Always check the relative humidity (48 ± 2%) in the room before coating, and follow the instructions for this equipment.
Use program "Co - 3012 - 1.4µm".

51. ALIGNMENT AND EXPOSURE

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper.
Follow the operating instructions from the manual when using this machine.

Use the mask “EC2204-V1_M1-VIA-M2-CO3” in box 486, jobname “Diesize_10mm/DIE10x10_4IMG”, layer “IMAGE 03”, with an energy of 120 $mJcm^{-2}$.

52. DEVELOPING

Use the developer station of the EVG120 system to develop the wafers. The process consists of:

- A post-exposure bake at 115°C for 90 seconds.
- Developing with Shipley MF322 with a single puddle process
- A hard bake at 100°C for 90 seconds

Always follow the instructions for this equipment.
Use program "Dev - SP".

53. INSPECTION: Linewidth and Overlay

Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

54. PLASMA ETCHING OF ALUMINUM

For aluminum etching use the Trikon Ωmega 210 plasma etcher. Follow the operating instructions from the manual when using this machine.
Use program “AlSi06_350” and set the platen temperature to 25°C in order to etch the aluminum layer. Total etch time must be 2 mins 30 secs to etch the aluminum completely and land on oxide layer underneath.

55. LAYER STRIPPING: Photoresist

Strip resist: Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use program 1: 1000 watts power and automatic endpoint detection + 2 min. overetching.

56. CLEANING: HNO_3 99% (Metals)

- Clean: 10 minutes in concentrated nitric acid. Use wet bench "HNO_3 99% (Metals)" and the carrier with the red and yellow dots.
- Rinse: Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5MΩ.
- Dry: Use the Semitool "rinser/dryer" with the standard program and the white carrier with a black dot.

57. PECVD DEPOSITION: DIELECTRIC DEFINITION (50nm Silicon Oxide)

Use the Novellus Concept One PECVD reactor.
Follow the operating instructions from the manual when using this machine.
Use group: undoped oxides (recipe xxxsiostd) to deposit a 50 nm thick SiO2 layer.
Change time to 1 sec/station to get the right thickness of oxide.

58. 39. MEASUREMENT: OXIDE THICKNESS

Use the Leitz MPV-SP measurement system to measure the oxide thickness:

Program: Novellus SiO2 on Al350 > 50
Oxide thickness: ≈ 53-56 nm on Al bottom cap. Plates and bondpads

59. COATING AND BAKING

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:

- A treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas.
- Spin coating of Shipley SPR3012 positive resist, dispensed by a pump.
- A soft bake at 95°C for 90 seconds.
- An automatic edge bead removal with a solvent

Always check the relative humidity (48 ± 2%) in the room before coating, and follow the instructions for this equipment.
Use program "Co - 3012 - 1.4µm".

60. ALIGNMENT AND EXPOSURE

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper.
Follow the operating instructions from the manual when using this machine.

Use the mask “EC2204-V1_M1-VIA-M2-CO3” in box 486, jobname “Diesize_10mm/DIE10x10_4IMG”, layer “IMAGE 04”, with an energy of 120 $mJcm^{-2}$.

61. DEVELOPING

Use the developer station of the EVG120 system to develop the wafers. The process consists of:

- A post-exposure bake at 115°C for 90 seconds.
- Developing with Shipley MF322 with a single puddle process
- A hard bake at 100°C for 90 seconds

Always follow the instructions for this equipment.
Use program "Dev - SP".

62. INSPECTION: Linewidth and Overlay

Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

63. DRY ETCHING TO OPEN VIAS

Use the Drytek Triode 384T plasma etcher.
Follow the operating instructions from the manual when using this machine.
It is not allowed to change the process conditions from the etch recipe, except for the etch times!

Use recipe STDOXIDE to etch the oxide layer with a soft landing on the layer underneath.
Use a total etch time of 8 secs.

64. INSPECTION

Visually inspect the wafers through a microscope, and check if the vias are indeed open.

65. MEASUREMENT: OXIDE THICKNESS

Use the Leitz MPV-SP measurement system to measure the oxide thickness:

Program: Novellus SiO2 Nf=1.46
Oxide thickness: 0 nm. on vias

66. LAYER STRIPPING: Photoresist

Strip resist: Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use program 1: 1000 watts power and automatic endpoint detection + 2 min. overetching.

67. CLEANING: HNO_3 99% (Metals)

- Clean: 10 minutes in concentrated nitric acid. Use wet bench "HNO_3 99% (Metals)" and the carrier with the red and yellow dots.
- Rinse: Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5MΩ.
- Dry: Use the Semitool "rinser/dryer" with the standard program and the white carrier with a black dot.

68. TITANIUM SPUTTERING: SECOND METALLIZATION

Use the TRIKON SIGMA sputter coater for the deposition of an titanium metal layer on the wafers.
The target must exist of 100% Ti, and deposition must be done at 25°C. Follow the operating instructions from the manual when using this machine.

Use recipe “Ti_200nm_25C” to sputter a 200 nm thick layer.

69. COATING AND BAKING

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:

- A treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas.
- Spin coating of Shipley SPR3012 positive resist, dispensed by a pump.
- A soft bake at 95°C for 90 seconds.
- An automatic edge bead removal with a solvent

Always check the relative humidity (48 ± 2%) in the room before coating, and follow the instructions for this equipment.
Use program "Co - 3012 - 2.1µm".

70. ALIGNMENT AND EXPOSURE

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper.
Follow the operating instructions from the manual when using this machine.

Use the mask “EC2204-V1_M1-VIA-M2-CO3” in box 486, jobname “Diesize_10mm/DIE10x10_4IMG”, layer “IMAGE 01”, with an energy of 320 $mJcm^{-2}$.

71. DEVELOPING

Use the developer station of the EVG120 system to develop the wafers. The process consists of:

- A post-exposure bake at 115°C for 90 seconds.
- Developing with Shipley MF322 with a single puddle process
- A hard bake at 100°C for 90 seconds

Always follow the instructions for this equipment.
Use program "Dev - SP".

72. INSPECTION: Linewidth and Overlay

Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

73. PLASMA ETCHING OF 100nm TITANIUM

For aluminum etching use the Trikon Ωmega 210 plasma etcher. Follow the operating instructions from the manual when using this machine.

Use program “Ti_100nm” and set the platen temperature to 25°C in order to etch the titanium layer. Total etch time must be 18 secs to etch 100nm of titanium.

74. WET ETCH OF TITANIUM OF REMAINIG 100nm TITANIUM: Etch Ti layer in Oxalic Acid (MEMSLab or SALab)

- Bath: Prepare a bath of 10% Oxalic Acid.
- : Temp: Use the hotplate at a temperature of 90°C.
- Time: Etch until all of the Ti is removed. Approximately 2 mins.
- Rinse: Rinse in a seperate water container to rinse the wafers for 4 minutes.
- Dry: Use the single wafer dryer.

75. LAYER STRIPPING: Photoresist

Strip resist: Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use program 1: 1000 watts power and automatic endpoint detection + 2 min. overetching.

76. CLEANING: HNO_3 99% (Metals)

- Clean: 10 minutes in concentrated nitric acid. Use wet bench "HNO_3 99% (Metals)" and the carrier with the red and yellow dots.
- Rinse: Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5MΩ.
- Dry: Use the Semitool "rinser/dryer" with the standard program and the white carrier with a black dot.

77. COATING AND BAKING

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:

- A treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas.
- Spin coating of Shipley SPR3012 positive resist, dispensed by a pump.
- A soft bake at 95°C for 90 seconds.
- An automatic edge bead removal with a solvent

Always check the relative humidity (48 ± 2%) in the room before coating, and follow the instructions for this equipment.
Use program "Co - 3012 - 2.1µm".

78. ALIGNMENT AND EXPOSURE

Processing will be performed on the ASML PAS5500/80 automatic wafer stepper.
Follow the operating instructions from the manual when using this machine.

Use the mask “EC2204-V1_M1-VIA-M2-CO3” in box 486, jobname “Diesize_10mm/DIE10x10_4IMG”, layer “IMAGE 02”, with an energy of 320 $mJcm^{-2}$.

79. DEVELOPING

Use the developer station of the EVG120 system to develop the wafers. The process consists of:

- A post-exposure bake at 115°C for 90 seconds.
- Developing with Shipley MF322 with a single puddle process
- A hard bake at 100°C for 90 seconds

Always follow the instructions for this equipment.
Use program "Dev - SP".

80. INSPECTION: Linewidth and Overlay

Visually inspect the wafers through a microscope, and check the line width and overlay. No resist residues are allowed.

81. DRY ETCHING TO OPEN SENSING AREA AND CONTACTS FOR BONDPADS

Use the Drytek Triode 384T plasma etcher.
Follow the operating instructions from the manual when using this machine.
It is not allowed to change the process conditions from the etch recipe, except for the etch times!

Use recipe STDOXIDE to etch the oxide layer with a soft landing on the layer underneath.
Use a total etch time of 8 secs.

82. INSPECTION

Visually inspect the wafers through a microscope, and check if the vias are indeed open.

83. MEASUREMENT: OXIDE THICKNESS

Use the Leitz MPV-SP measurement system to measure the oxide thickness:

Program: Novellus SiO2 Nf=1.46
Oxide thickness: 0 nm. on contact openings

84. LAYER STRIPPING: Photoresist

Strip resist: Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma. Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use program 1: 1000 watts power and automatic endpoint detection + 2 min. overetching.

85. CLEANING: HNO_3 99% (Metals)

- Clean: 10 minutes in concentrated nitric acid. Use wet bench "HNO_3 99% (Metals)" and the carrier with the red and yellow dots.
- Rinse: Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5MΩ.
- Dry: Use the Semitool "rinser/dryer" with the standard program and the white carrier with a black dot.

86. PECVD DEPOSITION: 6000nm oxide on backside (hard mask for Si DRIE)

Use the Novellus Concept One PECVD reactor.
Follow the operating instructions from the manual when using this machine.
Use group: undoped oxides (recipe xxxsiostd) to deposit a 6000 nm thick SiO2 layer.
Change time to 90 sec/station to get the right thickness of oxide.

87. COATING AND BAKING BACKSIDE

Use the coater station of the EVG120 system to coat the wafers with photoresist. The process consists of:

- A treatment with HMDS (hexamethyldisilazane) vapor, with nitrogen as a carrier gas.
- Spin coating of Shipley SPR3012 positive resist, dispensed by a pump.
- A soft bake at 95°C for 90 seconds.
- An automatic edge bead removal with a solvent

Always check the relative humidity (48 ± 2%) in the room before coating, and follow the instructions for this equipment.
Use program "Nlof - 3µm - noEBR".

88. ALIGNMENT AND EXPOSURE

Alignment and exposure will be done with the EVG 420 Contact Aligner. Follow the operating instructions from the manual when using this machine.

Use the mask “EC1940_V1_HOLES” in box 455, contact time must be 25 s with hard contact.

89. DEVELOPING

Use the developer station of the EVG120 system to develop the wafers. The process consists of:

- A post-exposure bake at 115°C for 90 seconds.
- Developing with Shipley MF322 with a single puddle process
- A hard bake at 100°C for 90 seconds

Always follow the instructions for this equipment.
Use program "Dev - Liftoff".

90. PLASMA ETCHING: Open 6000nm PECVD SiO_2 on backside

Use the Drytek Triode 384T plasma etcher.
Follow the operating instructions from the manual when using this machine.
It is not allowed to change the process conditions from the etch recipe, except for the etch times!

Use recipe STDOXIDE to etch the oxide layer with a soft landing on the layer underneath.
Use a total etch time of 12 mins.

91. INSPECTION

Visually inspect the wafers through a microscope, and check if the holes are indeed open.
No residues are allowed.

92. LAYER STRIPPING: Photoresist Backside

Strip resist: Use the Tepla Plasma 300 system to remove the photoresist in an oxygen plasma.
Follow the instructions specified for the Tepla stripper, and use the quartz carrier.
Use program 1: 1000 watts power and automatic endpoint detection + 2 min. overetching.

93. CLEANING: HNO_3 99% (Metals)

- Clean: 10 minutes in concentrated nitric acid. Use wet bench "HNO_3 99% (Metals)" and the carrier with the red and yellow dots.
- Rinse: Rinse in the Quick Dump Rinser with the standard program until the resistivity is 5MΩ.

- Dry: Use the Semitool "rinser/dryer" with the standard program and the white carrier with a black dot.

94. PDMS PREPARATION

In this step the preparation of the PDMS will be done using the elastomer PDMS Sylgard 184 and its curing agent.

Pour 20 g of the PDMS elastomer in the disposable cup and 2 g of curing agent by using a pipette. Depending on the number of wafers to be processed these amounts could vary but the ratio between the elastomer and curing agent must be keep on 10:1.

Don't forget protecting the weighting machine of any leakage of elastomer or curing agent during the preparation of the material. Use for this a towel to protect the plate of the machine.

95. PDMS MIXING AND DEGASSING

For mixing the PDMS elastomer and curing agent use the Thinky Speedmixer. Make sure that the cup holder is properly located in the machine. Determine the total weight of the cup and the holder and adjust the machine according to this value. Follow the instructions established for this machine.

Select program 01, check the parameters for each step if necessary and then start the process.

96. PDMS LAYER DEPOSITION

For the deposition of the 9 um PDMS layer use the Polos Manual Spinner 1 Cl100. Cover both the bottom and the ring of the spinner with aluminum foil to avoid residues of the polymer on the machine.

Pour the PDMS elastomer and curing agent mixture to cover about 2/3 parts of the wafer.
Select the folder (William) and the right recipe xx-pdms-tmp) to spin the material.

97. BACKSIDE AND FRONTSIDE PDMS CLEANING

Leave the wafer in the Lanz coater with vacuum on.
Use a cotton swab soaked in Acetone for cleaning the wafer backside and the frontside edge. Remove the PDMS from the edge of the wafer at least 4 mm deep towards the center of the wafer to avoid particles on the edge of the wafer.
Check also the backside of the wafer and remove any residual.

Note: Residuals are not allowed neither on the frontside nor the backside of the wafer.

98. PDMS BAKING

For baking of the PDMS layer use the Memmert Oven with the dedicated carrier (PDMS). Set the temperature level to 90 °C. Establish the temperature level prior to this step since it takes some time because the heat capacity if the oven is high.

Bake the PDMS layer at 90 °C for 60 min. DON'T FORGET TO STRIP THE RESIST FROM THE BACKSIDE.

Note: Check again at the end of the processing if any residual is present. Residuals are not allowed neither on the frontside nor the backside of the wafer.

99. ALUMINUM SPUTTERING FRONTSIDE (to protect PDMS layer during DRIE)

Use the TRIKON SIGMA sputter coater for the deposition of an aluminium metal layer on the wafers. The target must exist of 99% Al and 1% Si, and deposition must be done at 25°C. Follow the operating instructions from the manual when using this machine.

Use recipe "AlSi_225nm_25" to sputter a 225 nm thick layer.

Note: Check the wafers after aluminum deposition. Metal residuals should be not present on the edge neither on the frontside nor the backside of the wafer.

100. PLASMA ETCHING SILICON BACKSIDE

Use the Rapier Omega i2L DRIE etcher.
Follow the operating instructions from the manual when using this machine.

Use sequence "Waferlayer" (with a platen temperature of 20ºC) to etch the Si layer and stop on SiO2.
Approximate total etch time: 60min/360 cycles.

101. INSPECTION

Visually inspect the wafers through a microscope, and check if the holes are indeed open. No residues are allowed.

103. REMOVAL OF ALUMINUM (MEMSLab or SALab)

Prepare a special bath of PES to remove the aluminium layer with PES for 6 min. Dry them by using the single wafer spinner.

104. ELECTRICAL CHARACTERIZATION

C

Electrical and Electrochemical Measurement Data

C.1. PMOS 2:25

C.1.1. Transfer Characteristics

```
BEGIN_HEADER
 ICCAP_INPUTS
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vs         V  DEFAULT GROUND HRSMU2 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vbias      V  DEFAULT GROUND HRSMU4 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Sweep Order> <Start> <Stop> <# of Points> <Step Size>
  Vg         V  DEFAULT GROUND HRSMU3 0.1 LIN        1    5          -5         51    -0.2
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vd         V  DEFAULT GROUND HRSMU1 0.1 CON       -3
 ICCAP_OUTPUTS
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Id         I  DEFAULT GROUND HRSMU1 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ig         I  DEFAULT GROUND HRSMU3 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Is         I  DEFAULT GROUND HRSMU2 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ibias      I  DEFAULT GROUND HRSMU4 M
  R          U
END_HEADER

BEGIN_DB
 ICCAP_VAR Vs         0
 ICCAP_VAR Vbias      0
 ICCAP_VAR Vd         -3

 Vg              Id
  5               -1.8248e-010
  4.8             -1.6253e-010
  4.6             -1.3022e-010
  4.4             -1.0522e-010
  4.2             -9.534e-011
  4               -8.494e-011
  3.8             -7.579e-011
  3.6             -7.109e-011
  3.4             -6.726e-011
  3.2             -6.43e-011
  3               -6.129e-011
  2.8             -5.893e-011
  2.6             -5.731e-011
  2.4             -5.562e-011
```

```
  2.2             -5.428e-011
  2               -5.326e-011
  1.8             -5.253e-011
  1.6             -5.161e-011
  1.4             -5.113e-011
  1.2             -5.069e-011
  1               -4.995e-011
  0.8             -4.967e-011
  0.6             -4.95e-011
  0.4             -4.916e-011
  0.2             -4.908e-011
  0               -4.89e-011
  -0.2            -4.871e-011
  -0.4            -4.861e-011
  -0.6            -4.838e-011
  -0.8            -4.82e-011
  -1              -4.805e-011
  -1.2            -4.788e-011
  -1.4            -4.776e-011
  -1.6            -4.779e-011
  -1.8            -4.793e-011
  -2              -4.848e-011
  -2.2            -4.955e-011
  -2.4            -5.097e-011
  -2.6            -5.343e-011
  -2.8            -7.12e-011
  -3              -3.0162e-010
  -3.2            -3.4627e-009
  -3.4            -4.4026e-008
  -3.6            -4.4238e-007
  -3.8            -2.5437e-006
  -4              -8.196e-006
  -4.2            -1.8198e-005
  -4.4            -3.2565e-005
  -4.6            -5.0942e-005
  -4.8            -7.3132e-005
  -5              -9.863e-005
END_DB
```

C.1.2. OUTPUT CHARACTERISTICS

```
BEGIN_HEADER
 ICCAP_INPUTS
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vs         V  DEFAULT GROUND HRSMU2 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vbias      V  DEFAULT GROUND HRSMU4 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Sweep Order> <# of Values> <Value 1> <Value 2> <Va
  Vg         V  DEFAULT GROUND HRSMU3 0.01 LIST       2 4 -5 -6 -7 -8
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Sweep Order> <Start> <Stop> <# of Points> <Step Si
  Vd         V  DEFAULT GROUND HRSMU1 0.1 LIN        1    0          -8         21   -0.4
 ICCAP_OUTPUTS
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Id         I  DEFAULT GROUND HRSMU1 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ig         I  DEFAULT GROUND HRSMU3 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Is         I  DEFAULT GROUND HRSMU2 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ibias      I  DEFAULT GROUND HRSMU4 M
  R          U
END_HEADER

BEGIN_DB
 ICCAP_VAR Vs         0
 ICCAP_VAR Vbias      0
 ICCAP_VAR Vg         -5

 #Vd             Id
  0              3.7626e-010
```

```
  -0.4            -8.7019e-005
  -0.8            -0.00012187
  -1.2            -0.00013521
  -1.6            -0.00014367
  -2              -0.00014986
  -2.4            -0.00015585
  -2.8            -0.00016118
  -3.2            -0.0001659
  -3.6            -0.00017063
  -4              -0.00017559
  -4.4            -0.00018026
  -4.8            -0.00018478
  -5.2            -0.00018992
  -5.6            -0.00019419
  -6              -0.00019937
  -6.4            -0.00020663
  -6.8            -0.00021616
  -7.2            -0.00022712
  -7.6            -0.00023862
  -8              -0.00025029
END_DB

BEGIN_DB
 ICCAP_VAR Vs         0
 ICCAP_VAR Vbias      0
 ICCAP_VAR Vg         -6

 #Vd              Id
  0               8.3961e-010
  -0.4            -0.00014867
  -0.8            -0.0002399
  -1.2            -0.00028832
  -1.6            -0.00031529
  -2              -0.00033191
  -2.4            -0.00034476
  -2.8            -0.00035608
  -3.2            -0.00036636
  -3.6            -0.00037683
  -4              -0.00038574
  -4.4            -0.00039334
  -4.8            -0.00040184
  -5.2            -0.00041121
  -5.6            -0.0004187
  -6              -0.00042718
  -6.4            -0.00043776
  -6.8            -0.00044584
  -7.2            -0.00045851
  -7.6            -0.00047284
  -8              -0.00048799
END_DB

BEGIN_DB
 ICCAP_VAR Vs         0
 ICCAP_VAR Vbias      0
 ICCAP_VAR Vg         -7

 #Vd              Id
  0               9.683e-009
  -0.4            -0.00020432
  -0.8            -0.00035147
  -1.2            -0.00045
  -1.6            -0.0005116
  -2              -0.00055091
  -2.4            -0.00057774
  -2.8            -0.00059888
  -3.2            -0.000618
  -3.6            -0.00063304
  -4              -0.00064834
  -4.4            -0.00066223
  -4.8            -0.00067541
```

```
  -5.2            -0.00068971
  -5.6            -0.00070138
  -6              -0.0007119
  -6.4            -0.000724
  -6.8            -0.00073573
  -7.2            -0.00074873
  -7.6            -0.00076189
  -8              -0.00077606
END_DB

BEGIN_DB
 ICCAP_VAR Vs         0
 ICCAP_VAR Vbias      0
 ICCAP_VAR Vg         -8

 #Vd              Id
  0               2.0508e-007
  -0.4            -0.0002526
  -0.8            -0.00044711
  -1.2            -0.00059085
  -1.6            -0.00069259
  -2              -0.00076113
  -2.4            -0.00081015
  -2.8            -0.00084415
  -3.2            -0.00087132
  -3.6            -0.00089432
  -4              -0.00091734
  -4.4            -0.00093339
  -4.8            -0.0009522
  -5.2            -0.00096947
  -5.6            -0.00098687
  -6              -0.00099789
  -6.4            -0.00101697
  -6.8            -0.00102602
  -7.2            -0.0010445
  -7.6            -0.00105536
  -8              -0.00107202
END_DB
```

C.1.3. POST-INCUBATION

TRANSFER CHARACTERISTICS

```
BEGIN_HEADER
 ICCAP_INPUTS
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vs         V  DEFAULT GROUND HRSMU2 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vbias      V  DEFAULT GROUND HRSMU4 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Sweep Order> <Start> <Stop> <# of Points> <Step Si
  Vg         V  DEFAULT GROUND HRSMU3 0.1 LIN        1    5          -5         51   -0.2
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vd         V  DEFAULT GROUND HRSMU1 0.1 CON        -3
 ICCAP_OUTPUTS
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Id         I  DEFAULT GROUND HRSMU1 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ig         I  DEFAULT GROUND HRSMU3 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Is         I  DEFAULT GROUND HRSMU2 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ibias      I  DEFAULT GROUND HRSMU4 M
  R          U
END_HEADER

BEGIN_DB
 ICCAP_VAR Vs         0
 ICCAP_VAR Vbias      0
 ICCAP_VAR Vd         -3
```

```
 #Vg              Id
  5               -5.9e-011
  4.8             -5.723e-011
  4.6             -5.681e-011
  4.4             -5.571e-011
  4.2             -5.484e-011
  4               -5.417e-011
  3.8             -5.358e-011
  3.6             -5.307e-011
  3.4             -5.257e-011
  3.2             -5.229e-011
  3               -5.194e-011
  2.8             -5.169e-011
  2.6             -5.134e-011
  2.4             -5.11e-011
  2.2             -5.09e-011
  2               -5.059e-011
  1.8             -5.046e-011
  1.6             -5.047e-011
  1.4             -5.022e-011
  1.2             -5.016e-011
  1               -4.996e-011
  0.8             -4.98e-011
  0.6             -4.968e-011
  0.4             -4.966e-011
  0.2             -4.976e-011
  0               -5.175e-011
  -0.2            -5.478e-011
  -0.4            -5.61e-011
  -0.6            -5.678e-011
  -0.8            -5.565e-011
  -1              -5.644e-011
  -1.2            -5.804e-011
  -1.4            -5.953e-011
  -1.6            -6.033e-011
  -1.8            -6.012e-011
  -2              -6.015e-011
  -2.2            -6.102e-011
  -2.4            -6.159e-011
  -2.6            -6.251e-011
  -2.8            -7.12e-011
  -3              -1.8042e-010
  -3.2            -1.6944e-009
  -3.4            -2.1583e-008
  -3.6            -2.2454e-007
  -3.8            -1.4937e-006
  -4              -5.6693e-006
  -4.2            -1.4058e-005
  -4.4            -2.6714e-005
  -4.6            -4.3547e-005
  -4.8            -6.4242e-005
  -5              -8.8499e-005
END_DB
```

Output Characteristics

```
BEGIN_HEADER
 ICCAP_INPUTS
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vs         V  DEFAULT GROUND HRSMU2 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vbias      V  DEFAULT GROUND HRSMU4 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Sweep Order> <# of Values> <Value 1> <Value 2> <Value 3>
  Vg         V  DEFAULT GROUND HRSMU3 0.01 LIST       2 4 -5 -6 -7 -8
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Sweep Order> <Start> <Stop> <# of Points> <Step Size>
  Vd         V  DEFAULT GROUND HRSMU1 0.1 LIN        1    0          -8         21   -0.4
 ICCAP_OUTPUTS
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Id         I  DEFAULT GROUND HRSMU1 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
```

```
  Ig          I  DEFAULT GROUND HRSMU3 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Is          I  DEFAULT GROUND HRSMU2 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ibias       I  DEFAULT GROUND HRSMU4 M
  R           U
END_HEADER

BEGIN_DB
 ICCAP_VAR Vs          0
 ICCAP_VAR Vbias       0
 ICCAP_VAR Vg          -5

 #Vd              Id
  0               1.131e-009
  -0.4            -5.0326e-005
  -0.8            -6.4634e-005
  -1.2            -7.0731e-005
  -1.6            -7.5271e-005
  -2              -7.9218e-005
  -2.4            -8.2883e-005
  -2.8            -8.6311e-005
  -3.2            -8.9637e-005
  -3.6            -9.2917e-005
  -4              -9.6127e-005
  -4.4            -9.929e-005
  -4.8            -0.0001024
  -5.2            -0.00010555
  -5.6            -0.00010876
  -6              -0.00011201
  -6.4            -0.00011507
  -6.8            -0.00011832
  -7.2            -0.00012153
  -7.6            -0.0001249
  -8              -0.0001281
END_DB

BEGIN_DB
 ICCAP_VAR Vs          0
 ICCAP_VAR Vbias       0
 ICCAP_VAR Vg          -6

 #Vd              Id
  0               8.433e-009
  -0.4            -0.00010882
  -0.8            -0.0001704
  -1.2            -0.0002001
  -1.6            -0.00021642
  -2              -0.00022818
  -2.4            -0.00023801
  -2.8            -0.00024689
  -3.2            -0.00025515
  -3.6            -0.00026284
  -4              -0.00027035
  -4.4            -0.00027757
  -4.8            -0.00028458
  -5.2            -0.00029153
  -5.6            -0.00029832
  -6              -0.00030515
  -6.4            -0.0003119
  -6.8            -0.00031869
  -7.2            -0.00032534
  -7.6            -0.00033196
  -8              -0.00033878
END_DB

BEGIN_DB
 ICCAP_VAR Vs          0
 ICCAP_VAR Vbias       0
 ICCAP_VAR Vg          -7
```

```
 #Vd              Id
  0               1.3767e-008
  -0.4            -0.00016019
  -0.8            -0.00027419
  -1.2            -0.00034781
  -1.6            -0.00039197
  -2              -0.00042012
  -2.4            -0.00044066
  -2.8            -0.00045771
  -3.2            -0.00047274
  -3.6            -0.00048638
  -4              -0.00049927
  -4.4            -0.0005115
  -4.8            -0.00052319
  -5.2            -0.00053442
  -5.6            -0.00054542
  -6              -0.00055624
  -6.4            -0.00056675
  -6.8            -0.00057721
  -7.2            -0.00058766
  -7.6            -0.00059791
  -8              -0.00060819
END_DB

BEGIN_DB
 ICCAP_VAR Vs         0
 ICCAP_VAR Vbias      0
 ICCAP_VAR Vg         -8

 #Vd              Id
  0               1.4191e-008
  -0.4            -0.0002057
  -0.8            -0.00036714
  -1.2            -0.00048716
  -1.6            -0.00057133
  -2              -0.00062853
  -2.4            -0.0006683
  -2.8            -0.00069854
  -3.2            -0.00072347
  -3.6            -0.00074509
  -4              -0.00076472
  -4.4            -0.00078284
  -4.8            -0.00079992
  -5.2            -0.00081648
  -5.6            -0.00083207
  -6              -0.00084728
  -6.4            -0.00086185
  -6.8            -0.00087625
  -7.2            -0.00089043
  -7.6            -0.00090456
  -8              -0.00091847
END_DB
```

C.1.4. Transfer Characteristics at varying Ionic Concentrations of Electrolyte

300µM

```
BEGIN_HEADER
 ICCAP_INPUTS
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vs         V  DEFAULT GROUND HRSMU2 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vbias      V  DEFAULT GROUND HRSMU4 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Sweep Order> <Start> <Stop> <# of Points> <Step Size>
  Vg         V  DEFAULT GROUND HRSMU3 0.01 LIN       1    0          -5         51   -0.1
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vd         V  DEFAULT GROUND HRSMU1 0.1 CON        -3
```

```
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  V_cap      V  DEFAULT GROUND VSU1 0.1 CON 2
 ICCAP_OUTPUTS
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Id         I  DEFAULT GROUND HRSMU1 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ig         I  DEFAULT GROUND HRSMU3 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Is         I  DEFAULT GROUND HRSMU2 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ibias      I  DEFAULT GROUND HRSMU4 M
  R          U
END_HEADER

BEGIN_DB
 ICCAP_VAR Vs         0
 ICCAP_VAR Vbias      0
 ICCAP_VAR Vd         -3
 ICCAP_VAR V_cap      2

 #Vg              Id
  0               -6.27e-011
  -0.1            -7.816e-011
  -0.2            -7.701e-011
  -0.3            -6.952e-011
  -0.4            -7.395e-011
  -0.5            -8.887e-011
  -0.6            -7.196e-011
  -0.7            -6.71e-011
  -0.8            -7.323e-011
  -0.9            -7.198e-011
  -1              -7.491e-011
  -1.1            -7.252e-011
  -1.2            -6.122e-011
  -1.3            -6.581e-011
  -1.4            -3.415e-011
  -1.5            -5.766e-011
  -1.6            -7.627e-011
  -1.7            -1.0025e-010
  -1.8            -6.36e-011
  -1.9            -6.868e-011
  -2              -6.393e-011
  -2.1            -7.01e-011
  -2.2            -6.789e-011
  -2.3            -6.463e-011
  -2.4            -6.841e-011
  -2.5            -8.749e-011
  -2.6            -5.345e-011
  -2.7            -7.261e-011
  -2.8            -8.366e-011
  -2.9            -7.554e-011
  -3              -6.943e-011
  -3.1            -1.2196e-010
  -3.2            -2.2416e-010
  -3.3            -5.9824e-010
  -3.4            -2.0238e-009
  -3.5            -7.7143e-009
  -3.6            -2.4639e-008
  -3.7            -4.4505e-008
  -3.8            -1.5966e-007
  -3.9            -4.1083e-007
  -4              -9.9629e-007
  -4.1            -1.8648e-006
  -4.2            -3.2964e-006
  -4.3            -5.1713e-006
  -4.4            -8.327e-006
  -4.5            -1.4253e-005
  -4.6            -2.0249e-005
  -4.7            -2.673e-005
  -4.8            -3.3748e-005
```

```
  -4.9            -4.2703e-005
  -5              -5.101e-005
END_DB
```

450µM

```
BEGIN_HEADER
 ICCAP_INPUTS
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vs         V  DEFAULT GROUND HRSMU2 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vbias      V  DEFAULT GROUND HRSMU4 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Sweep Order> <Start> <Stop> <# of Points> <Step Size>
  Vg         V  DEFAULT GROUND HRSMU3 0.01 LIN       1    0          -5         51   -0.1
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vd         V  DEFAULT GROUND HRSMU1 0.1 CON        -3
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  V_cap      V  DEFAULT GROUND VSU1 0.1 CON 2
 ICCAP_OUTPUTS
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Id         I  DEFAULT GROUND HRSMU1 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ig         I  DEFAULT GROUND HRSMU3 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Is         I  DEFAULT GROUND HRSMU2 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ibias      I  DEFAULT GROUND HRSMU4 M
  R          U
END_HEADER

BEGIN_DB
 ICCAP_VAR Vs         0
 ICCAP_VAR Vbias      0
 ICCAP_VAR Vd         -3
 ICCAP_VAR V_cap      2

 #Vg              Id
  0               -1.0071e-008
  -0.1            -1.2347e-008
  -0.2            -1.277e-008
  -0.3            -1.1182e-008
  -0.4            -1.248e-008
  -0.5            -1.1161e-008
  -0.6            -1.0689e-008
  -0.7            -1.0488e-008
  -0.8            -1.0321e-008
  -0.9            -1.1732e-008
  -1              -1.071e-008
  -1.1            -1.0549e-008
  -1.2            -1.0468e-008
  -1.3            -1.0403e-008
  -1.4            -1.1506e-008
  -1.5            -1.0449e-008
  -1.6            -1.0459e-008
  -1.7            -1.0482e-008
  -1.8            -1.0645e-008
  -1.9            -1.048e-008
  -2              -9.966e-009
  -2.1            -1.0162e-008
  -2.2            -1.0548e-008
  -2.3            -1.0309e-008
  -2.4            -1.0118e-008
  -2.5            -1.0444e-008
  -2.6            -1.0424e-008
  -2.7            -1.0441e-008
  -2.8            -1.0179e-008
  -2.9            -1.002e-008
  -3              -1.0337e-008
  -3.1            -8.772e-009
  -3.2            -7.2017e-009
  -3.3            -7.9399e-009
```

```
  -3.4            -9.2236e-009
  -3.5            -1.801e-008
  -3.6            -4.4212e-008
  -3.7            -1.2585e-007
  -3.8            -3.5596e-007
  -3.9            -9.0757e-007
  -4              -2.0054e-006
  -4.1            -3.8856e-006
  -4.2            -6.7393e-006
  -4.3            -1.0555e-005
  -4.4            -1.5446e-005
  -4.5            -2.1314e-005
  -4.6            -2.8143e-005
  -4.7            -3.5895e-005
  -4.8            -4.4612e-005
  -4.9            -5.4176e-005
  -5              -6.4406e-005
END_DB
```

600µM

```
BEGIN_HEADER
 ICCAP_INPUTS
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vs         V  DEFAULT GROUND HRSMU2 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vbias      V  DEFAULT GROUND HRSMU4 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Sweep Order> <Start> <Stop> <# of Points> <Step Si
  Vg         V  DEFAULT GROUND HRSMU3 0.01 LIN        1    0          -5         51   -0.1
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vd         V  DEFAULT GROUND HRSMU1 0.1 CON        -3
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Sweep Order> <Value>
  V_cap      V  DEFAULT GROUND VSU1 0.1 CON   2
 ICCAP_OUTPUTS
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Id         I  DEFAULT GROUND HRSMU1 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ig         I  DEFAULT GROUND HRSMU3 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Is         I  DEFAULT GROUND HRSMU2 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ibias      I  DEFAULT GROUND HRSMU4 M
  R          U
END_HEADER

BEGIN_DB
 ICCAP_VAR Vs         0
 ICCAP_VAR Vbias      0
 ICCAP_VAR Vd         -3
 ICCAP_VAR V_cap      2

 #Vg             Id
  0              -5.275e-011
  -0.1           -5.78e-011
  -0.2           -6.448e-011
  -0.3           -6.811e-011
  -0.4           -6.746e-011
  -0.5           -7.104e-011
  -0.6           -7.058e-011
  -0.7           -5.962e-011
  -0.8           -6.037e-011
  -0.9           -6.061e-011
  -1             -5.907e-011
  -1.1           -5.75e-011
  -1.2           -5.708e-011
  -1.3           -5.716e-011
  -1.4           -5.748e-011
  -1.5           -5.774e-011
  -1.6           -5.799e-011
  -1.7           -5.871e-011
  -1.8           -6.034e-011
```

```
  -1.9            -6.205e-011
  -2              -6.331e-011
  -2.1            -6.454e-011
  -2.2            -6.558e-011
  -2.3            -6.64e-011
  -2.4            -6.693e-011
  -2.5            -6.725e-011
  -2.6            -6.759e-011
  -2.7            -6.858e-011
  -2.8            -7.177e-011
  -2.9            -8.419e-011
  -3              -1.3015e-010
  -3.1            -2.9477e-010
  -3.2            -9.1602e-010
  -3.3            -3.2056e-009
  -3.4            -1.12435e-008
  -3.5            -3.9529e-008
  -3.6            -1.2693e-007
  -3.7            -3.6857e-007
  -3.8            -9.5308e-007
  -3.9            -2.1178e-006
  -4              -4.0988e-006
  -4.1            -7.0732e-006
  -4.2            -1.10945e-005
  -4.3            -1.6123e-005
  -4.4            -2.2245e-005
  -4.5            -2.9363e-005
  -4.6            -3.7468e-005
  -4.7            -4.6537e-005
  -4.8            -5.6468e-005
  -4.9            -6.7378e-005
  -5              -7.8928e-005
END_DB
```

700µM

```
BEGIN_HEADER
 ICCAP_INPUTS
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vs         V  DEFAULT GROUND HRSMU2 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vbias      V  DEFAULT GROUND HRSMU4 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Sweep Order> <Start> <Stop> <# of Points> <Step Size>
  Vg         V  DEFAULT GROUND HRSMU3 0.01 LIN       1    0          -5         51   -0.1
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vd         V  DEFAULT GROUND HRSMU1 0.1 CON        -3
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Sweep Order> <Value>
  V_cap      V  DEFAULT GROUND VSU1 0.1 CON 2
 ICCAP_OUTPUTS
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Id         I  DEFAULT GROUND HRSMU1 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ig         I  DEFAULT GROUND HRSMU3 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Is         I  DEFAULT GROUND HRSMU2 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ibias      I  DEFAULT GROUND HRSMU4 M
  R          U
END_HEADER

BEGIN_DB
 ICCAP_VAR Vs         0
 ICCAP_VAR Vbias      0
 ICCAP_VAR Vd         -3
 ICCAP_VAR V_cap      2

 #Vg              Id
  0               -2.3119e-010
  -0.1            -2.8134e-010
  -0.2            -2.9419e-010
```

```
  -0.3            -3.0056e-010
  -0.4            -2.924e-010
  -0.5            -2.8644e-010
  -0.6            -2.7923e-010
  -0.7            -2.768e-010
  -0.8            -2.6293e-010
  -0.9            -2.4639e-010
  -1              -2.3987e-010
  -1.1            -2.3618e-010
  -1.2            -2.2995e-010
  -1.3            -2.2646e-010
  -1.4            -2.3085e-010
  -1.5            -2.516e-010
  -1.6            -3.467e-010
  -1.7            -3.2067e-010
  -1.8            -3.1297e-010
  -1.9            -3.2282e-010
  -2              -3.4714e-010
  -2.1            -3.2647e-010
  -2.2            -3.375e-010
  -2.3            -3.5405e-010
  -2.4            -3.2504e-010
  -2.5            -3.5592e-010
  -2.6            -2.8834e-010
  -2.7            -2.7223e-010
  -2.8            -2.8454e-010
  -2.9            -2.8888e-010
  -3              -4.0145e-010
  -3.1            -1.4182e-009
  -3.2            -2.2661e-009
  -3.3            -5.7971e-009
  -3.4            -1.8527e-008
  -3.5            -6.3888e-008
  -3.6            -2.0095e-007
  -3.7            -5.6505e-007
  -3.8            -1.3888e-006
  -3.9            -2.9428e-006
  -4              -5.4198e-006
  -4.1            -8.9621e-006
  -4.2            -1.3593e-005
  -4.3            -1.9294e-005
  -4.4            -2.6087e-005
  -4.5            -3.3921e-005
  -4.6            -4.27e-005
  -4.7            -5.2494e-005
  -4.8            -6.3159e-005
  -4.9            -7.4727e-005
  -5              -8.7067e-005
END_DB
```

C.2. NMOS 2:25

C.2.1. TRANSFER CHARACTERISTICS

```
BEGIN_HEADER
 ICCAP_INPUTS
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vs         V  DEFAULT GROUND HRSMU3 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vbias      V  DEFAULT GROUND HRSMU1 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Sweep Order> <Start> <Stop> <# of Points> <Step Si
  Vg         V  DEFAULT GROUND HRSMU4 0.1 LIN        1    -5         5          51   0.2
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vd         V  DEFAULT GROUND HRSMU2 0.1 CON        3
 ICCAP_OUTPUTS
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Id         I  DEFAULT GROUND HRSMU2 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
```

```
  Ig          I  DEFAULT GROUND HRSMU4 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Is          I  DEFAULT GROUND HRSMU3 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ibias       I  DEFAULT GROUND HRSMU1 M
  R           U
END_HEADER

BEGIN_DB
 ICCAP_VAR Vs          0
 ICCAP_VAR Vbias       0
 ICCAP_VAR Vd          3

 #Vg              Id
  -5              3.2907e-010
  -4.8            3.2848e-010
  -4.6            3.2852e-010
  -4.4            3.2839e-010
  -4.2            3.28e-010
  -4              3.2797e-010
  -3.8            3.2789e-010
  -3.6            3.2783e-010
  -3.4            3.2806e-010
  -3.2            3.2793e-010
  -3              3.2788e-010
  -2.8            3.2782e-010
  -2.6            3.2753e-010
  -2.4            3.274e-010
  -2.2            3.2694e-010
  -2              3.2711e-010
  -1.8            3.2724e-010
  -1.6            3.272e-010
  -1.4            3.2722e-010
  -1.2            3.2753e-010
  -1              3.3827e-010
  -0.8            1.1075e-009
  -0.6            5.5124e-008
  -0.4            1.9239e-006
  -0.2            1.4225e-005
  0               4.1587e-005
  0.2             8.0874e-005
  0.4             0.00012955
  0.6             0.00018506
  0.8             0.00024634
  1               0.00031186
  1.2             0.0003811
  1.4             0.00045387
  1.6             0.0005289
  1.8             0.00060643
  2               0.00068559
  2.2             0.0007666
  2.4             0.0008488
  2.6             0.00093214
  2.8             0.00101692
  3               0.00110232
  3.2             0.0011889
  3.4             0.0012758
  3.6             0.0013631
  3.8             0.0014512
  4               0.0015394
  4.2             0.0016282
  4.4             0.0017165
  4.6             0.0018049
  4.8             0.0018936
  5               0.0019814
END_DB
```

C.2.2. OUTPUT CHARACTERISTICS

```
BEGIN_HEADER
 ICCAP_INPUTS
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vs         V  DEFAULT GROUND HRSMU3 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vbias      V  DEFAULT GROUND HRSMU1 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Sweep Order> <Start> <Stop> <# of Points> <Step Si
  Vd         V  DEFAULT GROUND HRSMU2 0.1 LIN        1    0          5          21   0.25
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Sweep Order> <Start> <Stop> <# of Points> <Step Si
  Vg         V  DEFAULT GROUND HRSMU4 0.01 LIN        2    5          8          4    1
 ICCAP_OUTPUTS
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Id         I  DEFAULT GROUND HRSMU2 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ig         I  DEFAULT GROUND HRSMU4 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Is         I  DEFAULT GROUND HRSMU3 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ibias      I  DEFAULT GROUND HRSMU1 M
  R          U
END_HEADER

BEGIN_DB
 ICCAP_VAR Vs         0
 ICCAP_VAR Vbias      0
 ICCAP_VAR Vg         5

 #Vd              Id
  0               -4.3252e-006
  0.25            0.00035819
  0.5             0.00067771
  0.75            0.00096238
  1               0.0012097
  1.25            0.0014195
  1.5             0.0015938
  1.75            0.0017349
  2               0.0018462
  2.25            0.0019328
  2.5             0.0020003
  2.75            0.0020542
  3               0.002099
  3.25            0.0021376
  3.5             0.0021717
  3.75            0.0022033
  4               0.0022319
  4.25            0.0022589
  4.5             0.0022838
  4.75            0.0023077
  5               0.0023302
END_DB

BEGIN_DB
 ICCAP_VAR Vs         0
 ICCAP_VAR Vbias      0
 ICCAP_VAR Vg         6

 #Vd              Id
  0               -8.1321e-006
  0.25            0.00040229
  0.5             0.00076416
  0.75            0.00109217
  1               0.0013842
  1.25            0.0016382
  1.5             0.0018574
  1.75            0.0020419
  2               0.0021933
  2.25            0.0023167
  2.5             0.0024157
  2.75            0.0024949
```

```
  3               0.0025586
  3.25            0.0026113
  3.5             0.0026569
  3.75            0.0026971
  4               0.002733
  4.25            0.0027661
  4.5             0.0027967
  4.75            0.0028256
  5               0.0028525
END_DB

BEGIN_DB
 ICCAP_VAR Vs         0
 ICCAP_VAR Vbias      0
 ICCAP_VAR Vg         7

 #Vd              Id
  0               -1.3826e-005
  0.25            0.00044385
  0.5             0.00084384
  0.75            0.0012114
  1               0.001543
  1.25            0.0018377
  1.5             0.0020972
  1.75            0.0023219
  2               0.0025121
  2.25            0.0026724
  2.5             0.002805
  2.75            0.0029139
  3               0.0030025
  3.25            0.003075
  3.5             0.0031358
  3.75            0.0031879
  4               0.003233
  4.25            0.0032739
  4.5             0.0033106
  4.75            0.0033448
  5               0.0033767
END_DB

BEGIN_DB
 ICCAP_VAR Vs         0
 ICCAP_VAR Vbias      0
 ICCAP_VAR Vg         8

 #Vd              Id
  0               -1.986e-005
  0.25            0.00048207
  0.5             0.00091682
  0.75            0.0013199
  1               0.0016879
  1.25            0.0020197
  1.5             0.0023167
  1.75            0.0025779
  2               0.0028047
  2.25            0.0030003
  2.5             0.0031663
  2.75            0.0033064
  3               0.0034223
  3.25            0.0035188
  3.5             0.0035989
  3.75            0.0036668
  4               0.0037245
  4.25            0.0037749
  4.5             0.0038199
  4.75            0.0038606
  5               0.0038982
END_DB
```

C.2.3. TRANSFER CHARACTERISTICS FOR VARYING IONIC CONCENTRATIONS OF THE ELECTROLYTE

300µM

```
BEGIN_HEADER
 ICCAP_INPUTS
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vs         V  DEFAULT GROUND HRSMU3 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vbias      V  DEFAULT GROUND HRSMU1 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Sweep Order> <Start> <Stop> <# of Points> <Step Si
  Vg         V  DEFAULT GROUND HRSMU4 0.01 LIN       1    -5         5          51   0.2
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vd         V  DEFAULT GROUND HRSMU2 0.1 CON        3
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Sweep Order> <Value>
  V_cap      V  DEFAULT GROUND VSU1 0.1 CON 2
 ICCAP_OUTPUTS
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Id         I  DEFAULT GROUND HRSMU2 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ig         I  DEFAULT GROUND HRSMU4 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Is         I  DEFAULT GROUND HRSMU3 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ibias      I  DEFAULT GROUND HRSMU1 M
  R          U
END_HEADER

BEGIN_DB
 ICCAP_VAR Vs         0
 ICCAP_VAR Vbias      0
 ICCAP_VAR Vd         3
 ICCAP_VAR V_cap      2

 #Vg              Id
  -5              9.2539e-009
  -4.8            1.01178e-008
  -4.6            8.6539e-009
  -4.4            7.3401e-009
  -4.2            6.0579e-009
  -4              4.7054e-009
  -3.8            3.7e-009
  -3.6            2.9345e-009
  -3.4            2.2525e-009
  -3.2            1.6218e-009
  -3              1.3681e-009
  -2.8            1.1453e-009
  -2.6            8.6847e-010
  -2.4            6.9978e-010
  -2.2            6.1248e-010
  -2              5.4803e-010
  -1.8            6.381e-010
  -1.6            1.6079e-008
  -1.4            1.2271e-007
  -1.2            2.4972e-007
  -1              3.5697e-007
  -0.8            6.7644e-007
  -0.6            2.9248e-006
  -0.4            1.2782e-005
  -0.2            3.555e-005
  0               7.0311e-005
  0.2             0.00011345
  0.4             0.00016451
  0.6             0.00022115
  0.8             0.00028236
  1               0.00034711
  1.2             0.00041487
  1.4             0.00048574
  1.6             0.00055855
  1.8             0.00063368
```

```
  2               0.00070997
  2.2             0.00078817
  2.4             0.00086717
  2.6             0.00094733
  2.8             0.00102836
  3               0.00111045
  3.2             0.0011925
  3.4             0.001275
  3.6             0.001357
  3.8             0.0014404
  4               0.0015228
  4.2             0.001606
  4.4             0.0016889
  4.6             0.0017724
  4.8             0.0018556
  5               0.0019395
END_DB
```

450µM

```
BEGIN_HEADER
 ICCAP_INPUTS
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vs         V  DEFAULT GROUND HRSMU3 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vbias      V  DEFAULT GROUND HRSMU1 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Sweep Order> <Start> <Stop> <# of Points> <Step Size>
  Vg         V  DEFAULT GROUND HRSMU4 0.01 LIN       1    -5         5          51   0.2
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vd         V  DEFAULT GROUND HRSMU2 0.1 CON        3
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Sweep Order> <Value>
  V_cap      V  DEFAULT GROUND VSU1 0.1 CON 2
 ICCAP_OUTPUTS
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Id         I  DEFAULT GROUND HRSMU2 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ig         I  DEFAULT GROUND HRSMU4 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Is         I  DEFAULT GROUND HRSMU3 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ibias      I  DEFAULT GROUND HRSMU1 M
  R          U
END_HEADER

BEGIN_DB
 ICCAP_VAR Vs         0
 ICCAP_VAR Vbias      0
 ICCAP_VAR Vd         3
 ICCAP_VAR V_cap      2

 #Vg             Id
  -5             5.9853e-009
  -4.8           5.8733e-009
  -4.6           5.3275e-009
  -4.4           4.917e-009
  -4.2           4.291e-009
  -4             3.7523e-009
  -3.8           3.174e-009
  -3.6           2.6948e-009
  -3.4           2.2123e-009
  -3.2           1.9117e-009
  -3             1.5047e-009
  -2.8           1.348e-009
  -2.6           1.163e-009
  -2.4           1.0139e-009
  -2.2           7.4603e-010
  -2             6.2049e-010
  -1.8           5.4606e-010
  -1.6           5.0175e-010
  -1.4           4.9809e-010
  -1.2           2.5923e-009
```

```
  -1              6.0995e-008
  -0.8            7.2338e-007
  -0.6            7.0634e-006
  -0.4            2.5719e-005
  -0.2            5.8813e-005
  0               0.00010524
  0.2             0.0001573
  0.4             0.0002151
  0.6             0.00027667
  0.8             0.00034223
  1               0.00041049
  1.2             0.0004812
  1.4             0.00055267
  1.6             0.00062626
  1.8             0.00070255
  2               0.00077991
  2.2             0.0008588
  2.4             0.00093865
  2.6             0.0010192
  2.8             0.00110147
  3               0.0011808
  3.2             0.0012625
  3.4             0.0013455
  3.6             0.0014303
  3.8             0.0015161
  4               0.001602
  4.2             0.0016909
  4.4             0.001777
  4.6             0.0018646
  4.8             0.0019525
  5               0.0020395
END_DB
```

600µM

```
BEGIN_HEADER
 ICCAP_INPUTS
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vs         V  DEFAULT GROUND HRSMU3 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vbias      V  DEFAULT GROUND HRSMU1 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Sweep Order> <Start> <Stop> <# of Points> <Step Si
  Vg         V  DEFAULT GROUND HRSMU4 0.01 LIN        1    -5         5          51   0.2
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vd         V  DEFAULT GROUND HRSMU2 0.1 CON        3
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Sweep Order> <Value>
  V_cap      V  DEFAULT GROUND VSU1 0.1 CON  2
 ICCAP_OUTPUTS
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Id         I  DEFAULT GROUND HRSMU2 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ig         I  DEFAULT GROUND HRSMU4 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Is         I  DEFAULT GROUND HRSMU3 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ibias      I  DEFAULT GROUND HRSMU1 M
  R          U
END_HEADER

BEGIN_DB
 ICCAP_VAR Vs         0
 ICCAP_VAR Vbias      0
 ICCAP_VAR Vd         3
 ICCAP_VAR V_cap      2

 #Vg             Id
  -5             5.5487e-010
  -4.8           5.9617e-010
  -4.6           6.3625e-010
  -4.4           6.8203e-010
  -4.2           7.191e-010
```

```
  -4              7.5082e-010
  -3.8            7.8826e-010
  -3.6            8.1179e-010
  -3.4            8.3286e-010
  -3.2            8.4693e-010
  -3              8.8e-010
  -2.8            7.9654e-010
  -2.6            7.1014e-010
  -2.4            6.359e-010
  -2.2            5.846e-010
  -2              5.3936e-010
  -1.8            5.1067e-010
  -1.6            4.5787e-010
  -1.4            4.529e-010
  -1.2            5.876e-010
  -1              6.7903e-008
  -0.8            5.3089e-006
  -0.6            2.8123e-005
  -0.4            6.0335e-005
  -0.2            0.000100347
  0               0.00014834
  0.2             0.00020155
  0.4             0.00026014
  0.6             0.00032338
  0.8             0.00039281
  1               0.00046657
  1.2             0.0005431
  1.4             0.0006217
  1.6             0.00070148
  1.8             0.00078291
  2               0.00086538
  2.2             0.00094878
  2.4             0.00103262
  2.6             0.00111781
  2.8             0.0012035
  3               0.0012886
  3.2             0.0013743
  3.4             0.0014593
  3.6             0.0015445
  3.8             0.0016295
  4               0.0017132
  4.2             0.0017976
  4.4             0.0018319
  4.6             0.0019624
  4.8             0.0020457
  5               0.0021247
END_DB
```

700µM

```
BEGIN_HEADER
 ICCAP_INPUTS
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vs         V  DEFAULT GROUND HRSMU3 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vbias      V  DEFAULT GROUND HRSMU1 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Sweep Order> <Start> <Stop> <# of Points> <Step Size>
  Vg         V  DEFAULT GROUND HRSMU4 0.01 LIN       1    -5         5          51   0.2
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vd         V  DEFAULT GROUND HRSMU2 0.1 CON        3
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Sweep Order> <Value>
  V_cap      V  DEFAULT GROUND VSU1 0.1 CON 2
 ICCAP_OUTPUTS
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Id         I  DEFAULT GROUND HRSMU2 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ig         I  DEFAULT GROUND HRSMU4 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Is         I  DEFAULT GROUND HRSMU3 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ibias      I  DEFAULT GROUND HRSMU1 M
```

```
  R          U
END_HEADER

BEGIN_DB
 ICCAP_VAR Vs         0
 ICCAP_VAR Vbias      0
 ICCAP_VAR Vd         3
 ICCAP_VAR V_cap      2

 #Vg              Id
  -5              2.5371e-006
  -4.8            2.4672e-006
  -4.6            2.4133e-006
  -4.4            2.3707e-006
  -4.2            2.4252e-006
  -4              2.3305e-006
  -3.8            2.276e-006
  -3.6            2.2558e-006
  -3.4            2.2675e-006
  -3.2            2.2278e-006
  -3              2.1815e-006
  -2.8            2.1945e-006
  -2.6            2.2088e-006
  -2.4            2.2316e-006
  -2.2            2.114e-006
  -2              2.1268e-006
  -1.8            2.1266e-006
  -1.6            2.0724e-006
  -1.4            2.1034e-006
  -1.2            2.0788e-006
  -1              2.6001e-006
  -0.8            2.1264e-005
  -0.6            4.7637e-005
  -0.4            8.028e-005
  -0.2            0.00012112
  0               0.00016941
  0.2             0.00022382
  0.4             0.0002835
  0.6             0.00034807
  0.8             0.00041861
  1               0.00049406
  1.2             0.00057216
  1.4             0.00065227
  1.6             0.00073402
  1.8             0.00081811
  2               0.00090307
  2.2             0.0009895
  2.4             0.00107684
  2.6             0.0011656
  2.8             0.0012543
  3               0.0013432
  3.2             0.001433
  3.4             0.0015227
  3.6             0.0016129
  3.8             0.0017033
  4               0.0017939
  4.2             0.0018641
  4.4             0.0019037
  4.6             0.0020634
  4.8             0.002153
  5               0.0022417
END_DB
```

C.2.4. POST PDMS MEMBRANE RELEASE

TRANSFER CHARACTERISTICS

```
BEGIN_HEADER
 ICCAP_INPUTS
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
```

```
  Vs          V  DEFAULT GROUND HRSMU3 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vbias       V  DEFAULT GROUND HRSMU1 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Sweep Order> <Start> <Stop> <# of Points> <Step Size>
  Vg          V  DEFAULT GROUND HRSMU4 0.1 LIN        1    -5          5           51    0.2
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vd          V  DEFAULT GROUND HRSMU2 0.1 CON        3
 ICCAP_OUTPUTS
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Id          I  DEFAULT GROUND HRSMU2 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ig          I  DEFAULT GROUND HRSMU4 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Is          I  DEFAULT GROUND HRSMU3 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ibias       I  DEFAULT GROUND HRSMU1 M
  R           U
END_HEADER

BEGIN_DB
 ICCAP_VAR Vs         0
 ICCAP_VAR Vbias      0
 ICCAP_VAR Vd         3

 #Vg              Id
  -5              3.2907e-010
  -4.8            3.2848e-010
  -4.6            3.2852e-010
  -4.4            3.2839e-010
  -4.2            3.28e-010
  -4              3.2797e-010
  -3.8            3.2789e-010
  -3.6            3.2783e-010
  -3.4            3.2806e-010
  -3.2            3.2793e-010
  -3              3.2788e-010
  -2.8            3.2782e-010
  -2.6            3.2753e-010
  -2.4            3.274e-010
  -2.2            3.2694e-010
  -2              3.2711e-010
  -1.8            3.2724e-010
  -1.6            3.272e-010
  -1.4            3.2722e-010
  -1.2            3.2753e-010
  -1              3.3827e-010
  -0.8            1.1075e-009
  -0.6            5.5124e-008
  -0.4            1.9239e-006
  -0.2            1.4225e-005
  0               4.1587e-005
  0.2             8.0874e-005
  0.4             0.00012955
  0.6             0.00018506
  0.8             0.00024634
  1               0.00031186
  1.2             0.0003811
  1.4             0.00045387
  1.6             0.0005289
  1.8             0.00060643
  2               0.00068559
  2.2             0.0007666
  2.4             0.0008488
  2.6             0.00093214
  2.8             0.00101692
  3               0.00110232
  3.2             0.0011889
  3.4             0.0012758
  3.6             0.0013631
  3.8             0.0014512
```

```
  4               0.0015394
  4.2             0.0016282
  4.4             0.0017165
  4.6             0.0018049
  4.8             0.0018936
  5               0.0019814
END_DB
```

OUTPUT CHARACTERISTICS

```
BEGIN_HEADER
 ICCAP_INPUTS
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vs         V  DEFAULT GROUND HRSMU3 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Value>
  Vbias      V  DEFAULT GROUND HRSMU1 0.1 CON        0
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Sweep Order> <Start> <Stop> <# of Points> <Step Si
  Vd         V  DEFAULT GROUND HRSMU2 0.1 LIN        1    0          5          21   0.25
! <Name>  <Mode> <+ Node> <- Node> <Unit> <Compliance>  <Sweep-type> <Sweep Order> <Start> <Stop> <# of Points> <Step Si
  Vg         V  DEFAULT GROUND HRSMU4 0.01 LIN        2    5          8          4    1
 ICCAP_OUTPUTS
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Id         I  DEFAULT GROUND HRSMU2 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ig         I  DEFAULT GROUND HRSMU4 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Is         I  DEFAULT GROUND HRSMU3 M
! <Name>  <Mode> <To Node> <From Node> <Unit>  <Type>
  Ibias      I  DEFAULT GROUND HRSMU1 M
  R          U
END_HEADER

BEGIN_DB
 ICCAP_VAR Vs         0
 ICCAP_VAR Vbias      0
 ICCAP_VAR Vg         5

 #Vd              Id
  0               -4.3252e-006
  0.25            0.00035819
  0.5             0.00067771
  0.75            0.00096238
  1               0.0012097
  1.25            0.0014195
  1.5             0.0015938
  1.75            0.0017349
  2               0.0018462
  2.25            0.0019328
  2.5             0.0020003
  2.75            0.0020542
  3               0.002099
  3.25            0.0021376
  3.5             0.0021717
  3.75            0.0022033
  4               0.0022319
  4.25            0.0022589
  4.5             0.0022838
  4.75            0.0023077
  5               0.0023302
END_DB

BEGIN_DB
 ICCAP_VAR Vs         0
 ICCAP_VAR Vbias      0
 ICCAP_VAR Vg         6

 #Vd              Id
  0               -8.1321e-006
  0.25            0.00040229
  0.5             0.00076416
  0.75            0.00109217
```

```
  1               0.0013842
  1.25            0.0016382
  1.5             0.0018574
  1.75            0.0020419
  2               0.0021933
  2.25            0.0023167
  2.5             0.0024157
  2.75            0.0024949
  3               0.0025586
  3.25            0.0026113
  3.5             0.0026569
  3.75            0.0026971
  4               0.002733
  4.25            0.0027661
  4.5             0.0027967
  4.75            0.0028256
  5               0.0028525
END_DB

BEGIN_DB
 ICCAP_VAR Vs         0
 ICCAP_VAR Vbias      0
 ICCAP_VAR Vg         7

 #Vd              Id
  0               -1.3826e-005
  0.25            0.00044385
  0.5             0.00084384
  0.75            0.0012114
  1               0.001543
  1.25            0.0018377
  1.5             0.0020972
  1.75            0.0023219
  2               0.0025121
  2.25            0.0026724
  2.5             0.002805
  2.75            0.0029139
  3               0.0030025
  3.25            0.003075
  3.5             0.0031358
  3.75            0.0031879
  4               0.003233
  4.25            0.0032739
  4.5             0.0033106
  4.75            0.0033448
  5               0.0033767
END_DB

BEGIN_DB
 ICCAP_VAR Vs         0
 ICCAP_VAR Vbias      0
 ICCAP_VAR Vg         8

 #Vd              Id
  0               -1.986e-005
  0.25            0.00048207
  0.5             0.00091682
  0.75            0.0013199
  1               0.0016879
  1.25            0.0020197
  1.5             0.0023167
  1.75            0.0025779
  2               0.0028047
  2.25            0.0030003
  2.5             0.0031663
  2.75            0.0033064
  3               0.0034223
  3.25            0.0035188
  3.5             0.0035989
  3.75            0.0036668
```

```
  4               0.0037245
  4.25            0.0037749
  4.5             0.0038199
  4.75            0.0038606
  5               0.0038982
END_DB
```

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