Wide Dynamic-Range Low-Power Current-Mode Optical Sensor Readout

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Wide Dynamic-Range Low-Power Current-Mode Optical Sensor Readout

Master's Thesis

To fulfill the requirements for the degree of
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Contents

List of Acronyms

PD Photodiode

TIA Transimpedance Amplifier

R-TIA Resistive-Transimpedance Amplifier

C-TIA Capacitive-Transimpedance Amplifier

DR Dynamic Range

ISD Current-mode Sigma- Delta

I-to-F Current-to-Frequency

ADC Analog-to-Digital Converter

VTSW Threshold Window and Chopper Switch

GBW Gain-Bandwidth Product

CMFB Common-mode Feedback

RMS Root-Mean-Square

Acknowledgments

It is my second-year master studying in TUDelft and my fifth year in the Netherlands. Looking back to the past five years, I feel like I have grown up a lot.

The two-year master's study life is special due to the Corona breakout. Most of the lessons in the first year were held online. Nevertheless, thanks to the technical support from the university and all the professors, I still had a chance to learn analog IC design knowledge that may not be learned anywhere else.

The thesis project is provided by the company Silicon Integrated. Therefore, it is a collaboration between the school and the company. I feel very grateful to take the chance to work in the company. The company provided a positive working environment, and all the people from the company, Yongjie Jin and Kerong Luo, e.g., have great personalities. They are always willing to help answer my questions. I also want to thank Xiaomeng An, who has been my roommate for more than four years. We have similar lifestyles and know each other well, which is why we can live together for such a long time. I am so glad we have become a better version of ourselves. Also, I have worked with several classmates together in the company: Guo Xu, Jinqian Yu, Jixuan Mou, and Jia Shi. We learn from each other and share unforgettable memories in both working and leisure time.

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And most importantly, I want to thank my parents. Without their love and support, I could not achieve so far. They give me the courage to face challenges and teach me how to be a good person. I feel honored to be born as their daughter, and I hope I can be their pride too.

Abstract

Optical sensor has been widely used in daily life. One of the important applications of optical sensors is the ambient light sensor installed in portable devices. The screen brightness of portable devices like smartphones is designed to be automatically adjusted based on the ambient environment. The ambient light detection is realized using optical devices like Photodiode (PD), where the incident light is converted into an analog current. The induced PD current is measured by a readout circuit so that the output of the readout circuit controls the screen brightness accordingly.

This thesis presents an energy-efficient current-mode optical sensor readout circuit that achieves a wide dynamic range. Hourglass ADC is used as the core structure of the readout circuit, applying current-to-frequency conversion. The output of the readout is the digital count within 100ms conversion time. The dark counts of the designed PD readout circuit are less than three counts. The noise count is less than one when output counts are smaller than 100 and less than 1% when output counts are more than 100. Fabricated in a 0.18μm CMOS process, the readout circuit achieves a 160dB dynamic measurement range comparable to the prior-of-art. The entire circuit consumes power of 0.113mW and occupies a chip area of 0.056mm^2.

1 Introduction

1.1 Problem Statement

Ambient light sensor has been widely used for mobile devices like smartphones for automatic screen brightness control. Photodiode (PD) is the typical sensing element in optical sensors like ambient light sensors. Ambient light sensors should be functional in dim and bright environments, sensing both dark ambient light and strong lightness from light sources. PD produces current ranging from fA to nA in different ambient environments, which means the PD readout circuit should cover a wide current measurement range. Also, the ambient light sensor must maintain a moderate speed to catch up with ambient light changes. Moreover, the PD readout should produce low leakage current and current noise since the induced PD current is small under dark environments. Optimum linearity is required for PD readout not to degrade the PD linearity severally.

The thesis project aims to design a current-mode measurement readout circuit for PD, covering a wide PD current measurement range from $2fA$ to $200nA$, or $160dB$ dynamic range (DR), while maintaining a low power consumption of less than $0.18mW$ with $1.8V$ power supply. The maximum conversion time should be less than $100ms$. Generally, the output of a PD readout is digital counts. Requirements on dark count and noise count of the readout are defined respectively: For dark count, it should be less than three; For noise count, it should be less than one when output counts are smaller than 100 and less than 1% when output counts are more than 100. The linearity of the PD readout is ensured when the coefficient of determination (R2) is larger than 0.99.

1.2 Thesis Outline

This thesis is organized as follows.

Chapter 2: Back ground and Literature Review This chapter introduces the background information and the starting point of this thesis project.

Chapter 3: Proposed Architecture In this chapter, an architecture is proposed based on project requirements. The design highlight of this proposed architecture is described here and compared with reviewed literature in chapter 2.

Chapter 4: Circuit Implementation Detailed circuit implementation of the proposed architecture is explained in the chapter.

Chapter 5: Layout and Post-Simulation Result This chapter introduces the layout and presents the evaluation result of the design based on the post-layout simulation.

Chapter 6: Conclusion and Future Work The conclusion is drawn in this chapter. Further work and further improvement advice on the architecture can be found here.

2 Background and Literature Review

2.1 Ambient Light Sensor

Optical Sensors, such as ambient light sensors, can be found in mobile devices like smartphones and tablets to adjust screen brightness based on the ambient light level automatically. The ambient light sensor should sense dim light at dark to direct sunlight at noon without saturation.

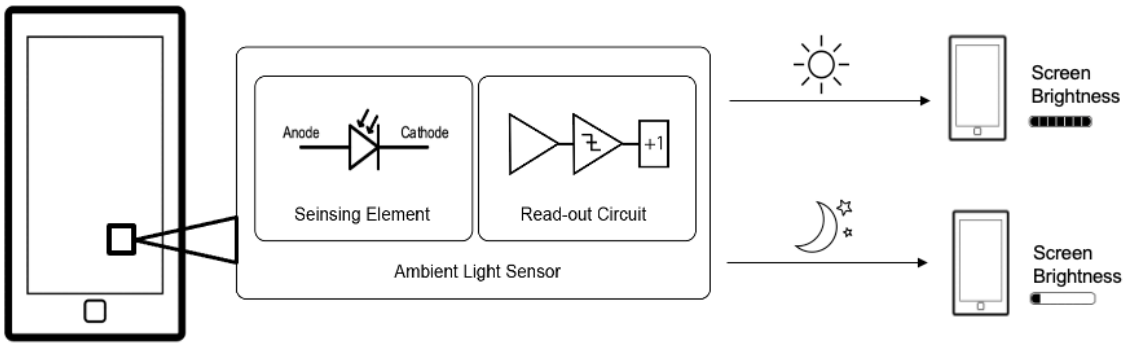


Figure 2.1: Ambient light sensor used for adjusting screen brightness

The working principle of the ambient sensor is briefly demonstrated in figure 2.1. The ambient light sensor is placed under the smartphone screen and contains Photodiode (PD) and its readout circuit. Here two extreme weather conditions are given. The screen is hard to read on sunny days due to intense sunlight. The screen brightness needs to be tuned high. On the contrary, if the ambient light is weak in a dark night, the screen brightness can be turned down for both comfort reading and battery saving.

Photodiode (PD) is the key sensing element in optical sensors, including ambient light sensors. It is essentially a device that converts light energy to electrical energy [1]. For ambient light sensing applications, it converts incident light from the environment into a certain amount of current. Figure 2.2 shows the symbol and I-V characteristics of Photodiodes. PD can be operated in two modes with different biasing voltage as indicated in I-V characteristics: photovoltaic mode and photoconductive mode. PD is reversed biased in photoconductive while zero or forward biased in photovoltaic mode. In photovoltaic mode, zero-biasing condition is preferred for ambient light sensors since the dark current produced by PD is minimized. It is beneficial since the PD current produced in a dark environment

is small. With reduced dark current, the accuracy of PD current sensing is improved. To realize the zero biasing condition, differential PD becomes a more elegant choice than single-ended PD since the differential architecture provides better rejection of common-mode interfering signals.

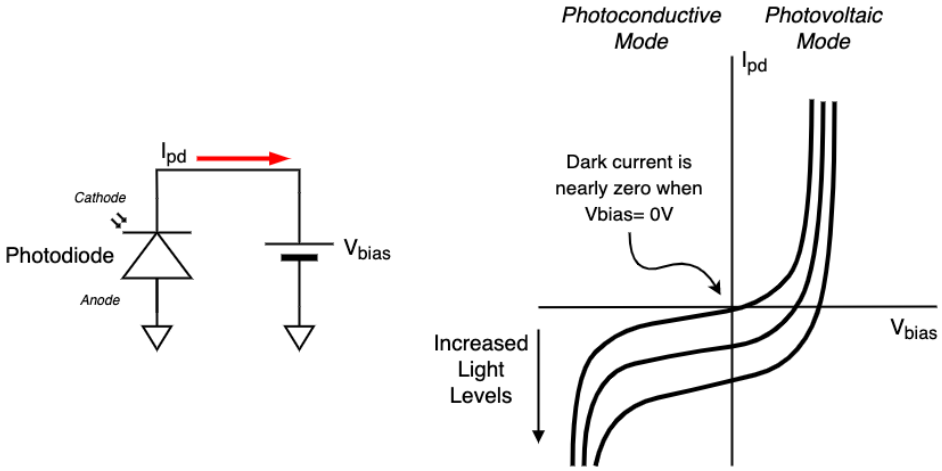


Figure 2.2: I-V Characteristics of Photodiodes

For accurate screen brightness control, high sensitivity and high dynamic range (DR) are required for PD and its readout circuit. In the rest of this chapter, some conventional current measurement methodologies are introduced, followed by comprehensive current-mode readout circuits that apply different current measurement methodologies introduced earlier.

2.2 Current Measurement Methodology

Several conventional current measurement methodologies used in the current-mode readout are introduced in this chapter. They are classified into two types: one is analog-mode based, and the other utilizes direct digitization. The essential part of the analog-mode current measurement method is Transimpedance-Amplifier (TIA) which directly converts input current into a voltage output. Therefore, besides TIA, it also requires an extra Analog-to-Digital converter (ADC) to digitize analog signal output further. Alternatively, digital data can also be directly obtained without explicit ADC using structures like current-to-frequency(I-to-F) converters or current-mode sigma-delta (ISD) modulators in the form of frequency or digital counts [2].

2.2.1 Transimpedance Amplifier (TIA)

The basic structure of the Transimpedance Amplifier can be found in figure 2.3. PD current is sent to the TIA and converted into a voltage at the output of TIA. The voltage is connected to an ADC for further processing. The feedback elements are either resistive or capacitive, producing different voltage to current behavior. The input signal can be reproduced by signal processing in the voltage domain.

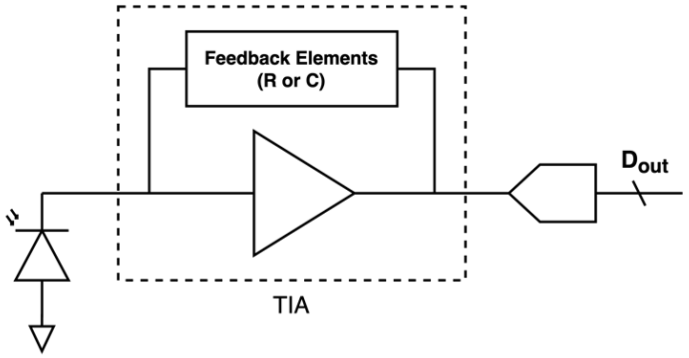


Figure 2.3: Transimpedance Amplifier(TIA)

Resistive-Transimpedance Amplifier(R-TIA)

The most straightforward and typical current measurement structure would be a transimpedance amplifier with resistive feedback. The trade-off between power, noise, and bandwidth in such a system can be configured to meet specific design requirements. However, the main design concerns for low-current measurement applications are the implementation of large feedback resistors to achieve a low noise floor.

Capacitive-Transimpedance Amplifier(C-TIA)

When the feedback resistor of a transimpedance amplifier is replaced by a feedback capacitor, the C-TIA is built, also called a charge-sensitive amplifier. Since the capacitors are noise-free components, C-TIA generally achieves low noise density compared with R-TIA. However, the integrator in this type of structure suffers from the saturation issue. And the saturation can be prevented either by the continuous-time method using a low-noise active device setting bias point or by the discrete-time method using a switch resetting integrator periodically.

2.2.2 Direct Digitization

Compared with TIA, there are also different current-mode measurement methodologies that implement direct current digitization without extra ADC. The TIA can also be part of the structure in this type of methodology.

Current-mode Sigma-delta (ISD) Modulator

Voltage-mode sigma-delta modulator is widely used as a power-efficient analog-to-digital converter for its benefit of oversampling and noise-shaping characteristics. Similarly, current-mode sigma-delta can also digitize current input while having the same benefit as a voltage-mode sigma-delta modulator. Basic structures like loop filter, quantizer, and feedback path are still included in the current-mode sigma-delta modulator and only need to be modified accordingly for its current application. Below are two examples that use the ISD modulator as its basic working principle.

Readout1: Applying ISD Modulator

The entire design behaves like a first-order sigma-delta modulator [3]. The digital IIR filter is placed within the loop to behave like a predictor. It predicts the value of the next stage based on the current stage and outputs a tri-level PWM to control the current DAC and close the loop. Just like the voltage-mode first-order sigma-delta modulator, this architecture benefits from noise shaping, and using the tri-level PWM signal helps save power effectively.

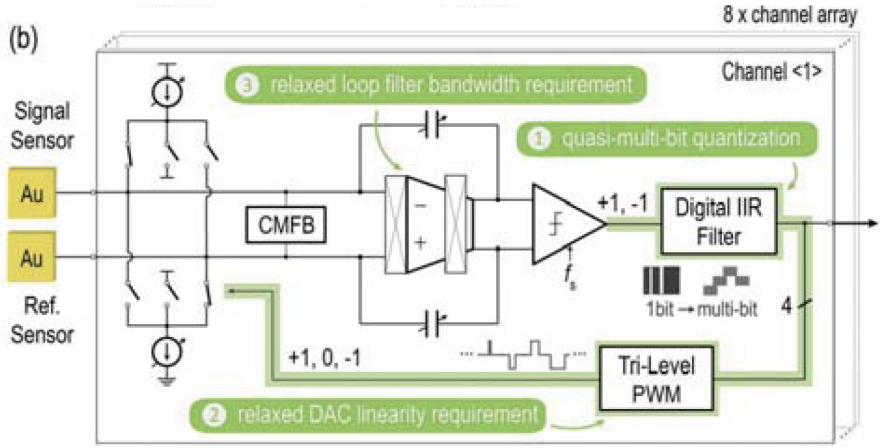


Figure 2.4: First-order delta-sigma modulator using digital IIR filter [3]

Readout2: Applying modified ISD Modulator

In this current measurement readout circuit, a modified asynchronous delta-sigma modulator is built utilizing an hourglass ADC that continuously folds the input current into a threshold window [4]. A fully differential structure is applied in this design, making it possible for an hourglass switch to periodically change the input current direction. A predictor is placed in the feedback loop to drive the current DAC that subtracted the coarse signal so that the hourglass ADC only processes the fine signal. The modified first-order delta-sigma structure achieves the first-order noise-shaping and benefits from the high dynamic range because of the hourglass ADC structure.

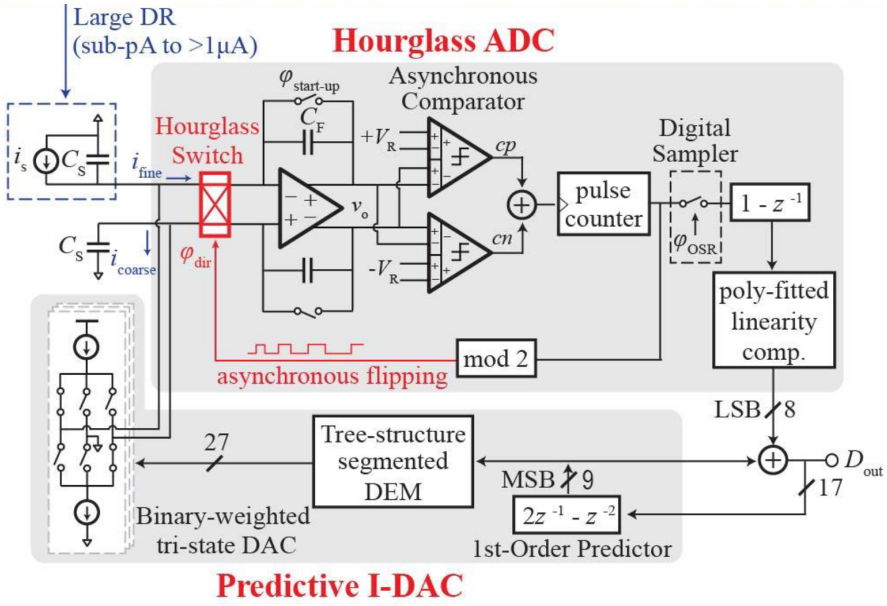


Figure 2.5: First-order delta-sigma modulator using hourglass ADC [4]

Current-to-Frequency (I-to-F) Converter

In this current measuring method, pulse trains or frequency is the final output and holds linear relation to the magnitude of input current. The basic principle behind the I-to-F converter is charge balancing. Usually, there are two phases in the measuring process. The total charge produced by PD is self-balanced or balanced by reference source between two phases. The period of two phases can be detected and represents the magnitude of PD current by obtaining a charge balancing equation. TIA can be part of the circuit in the I-to-F converter since the voltage output of the TIA can be further converted into frequency by using a quantizer like a comparator with proper threshold control. Two

I-to-F converter-based current-mode readout circuits are introduced below.

Readout3: Applying both C-TIA and I-to-F converter

This architecture implements a dual-mode design and achieves a high measurement dynamic range by combing both voltage and frequency output [5]. Essentially, two current measurement methods are involved: C-TIA combined with a differentiator that generates the voltage output and an I-to-F converter that produces the frequency output. In this structure, two pairs of capacitance in the entire circuit realize the self-charging balance, eliminate the use of an extra reference clock, and effectively minimize the reset transient and dead time.

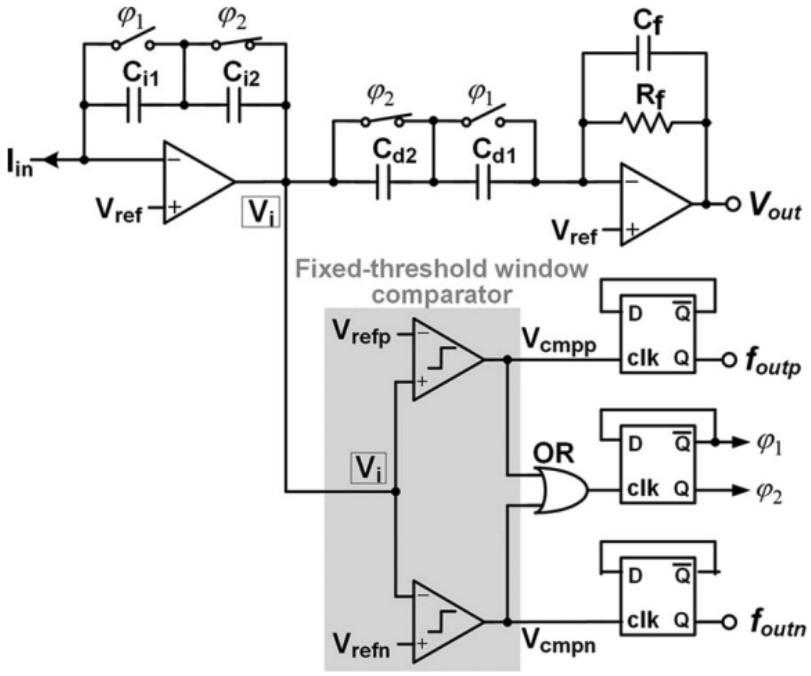


Figure 2.6: Dual-mode using current to frequency and C-TIA [5]

Readout4: Applying I-to-F converter

This ultra-low-current measurement circuit contains three main stages: an integrator in the first stage specially designed for low current input with small integration capacitance [6]. The small output swing will then be amplified in the next stage with a post-amplifier and eventually converted into a

pulse signal representing the input current level. A nested auto-zeroing technique is applied to reduce offset and charge injection for each stage, and a modified correlated double sampling technique is implemented by utilizing threshold control. Two threshold voltages of the comparator are preset, and the pulse width between those two comparing points can be obtained to represent the measured current.

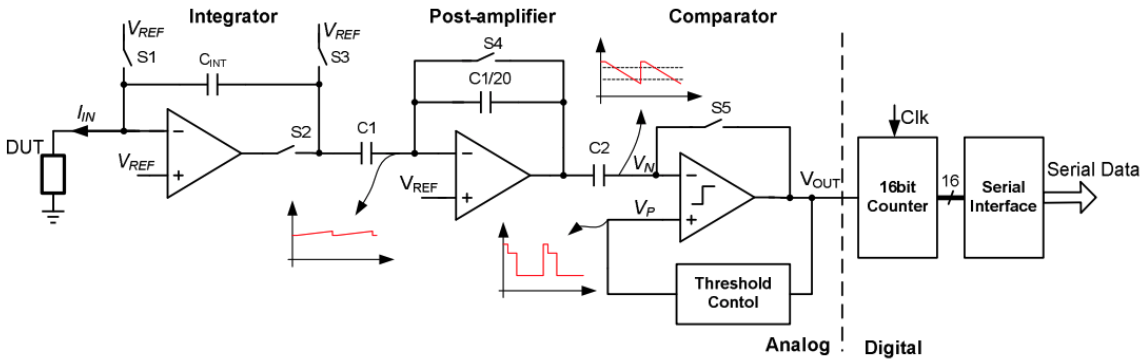


Figure 2.7: Current to frequency with modified correlated double sampling [6]

2.3 Current-mode Readout Performance Comparison

Four current-mode readout circuits are introduced in the last chapter, where the basic operating principles and design highlights for each work are demonstrated, respectively. The performance of each design is summarized in a comparison table. The design target of the thesis project is also included to provide a comprehensive comparison.

According to table 1, the first three readout circuits achieve a wide dynamic range higher than 100dB, covering current range from fA to μA. Architecture using hourglass ADC has a dynamic range of $160dB$, while the cost is the highest power consumption and largest area among the rest. Architecture using dual-mode current measurement methods achieves a dynamic range of $155dB$ but consumes much more power. The readout circuit that uses I-to-F architecture uses more advanced process technology and is suitable for ultra-low current measurement. However, one of the drawbacks is the relatively low dynamic range, only $68.5dB$. Comparing target performance with prior-of-art, readout circuit using hourglass ADC architecture shows the best match to the design target: The remarkable

high dynamic range ($160dB$) and acceptable low power of $0.295mW$ and a small area of 0.22mm^2.

Nevertheless, the minimum input current is $2fA$ from the project target and the power limit is $0.18mW$ with $1.8V$ supply. The readout circuit that implements hourglass ADC can be used as a great reference, but extra attention should be paid to saving power and improving measurement resolution.

	Design Target	VLSI19 [3]	ISSCC18 [4]	TBioCAS16 [5]	CICC12 [6]
Architecture	-	ISD	Hourglass ADC, ISD	C-TIA/I-to-F	I-to-F
Application	Optical	Bio-sensing	Bio-sensing	Bio-sensing	Bio-sensing
Process	180nm	180nm	180nm	180nm	90nm
Input Range	2fA to 200nA	123fA to 1.1μA	100fA to 10μA	123fA to 11.6μA	75fA to 200pA
Dynamic range	160dB	139dB	160dB	155dB	68.5dB
Area	-	0.11mm^2	0.2mm^2	0.091mm^2	0.065mm^2
Power@Supply Voltage	0.18mW@ 1.8V	0.05mW@ 1.8V	0.295mW@ 1.8V	5.22mW@ 1.8V	0.147mW@ 1.8V
Conversion time	100ms	100ms	400ms	5ms	250us
Input-referred Noise	0.63 fA/$\sqrt{Hz}$	30.3 fA/$\sqrt{Hz}$	58.9 fA/$\sqrt{Hz}$	20.4 fA/$\sqrt{Hz}$	0.235 fA/$\sqrt{Hz}$

Table 1: Performance comparison Prior-of-Art

3 Proposed Architecture

As is discussed at the end of the last chapter, the hourglass ADC based on an asynchronous delta-sigma modulator [4] stands out for its high dynamic measurement range and relatively low power and area cost. Considering its benefit on high dynamic measurement range, the hourglass ADC structure is implemented as the basic structure in the proposed readout circuit design.

3.1 Hourglass ADC

3.1.1 Working Principle

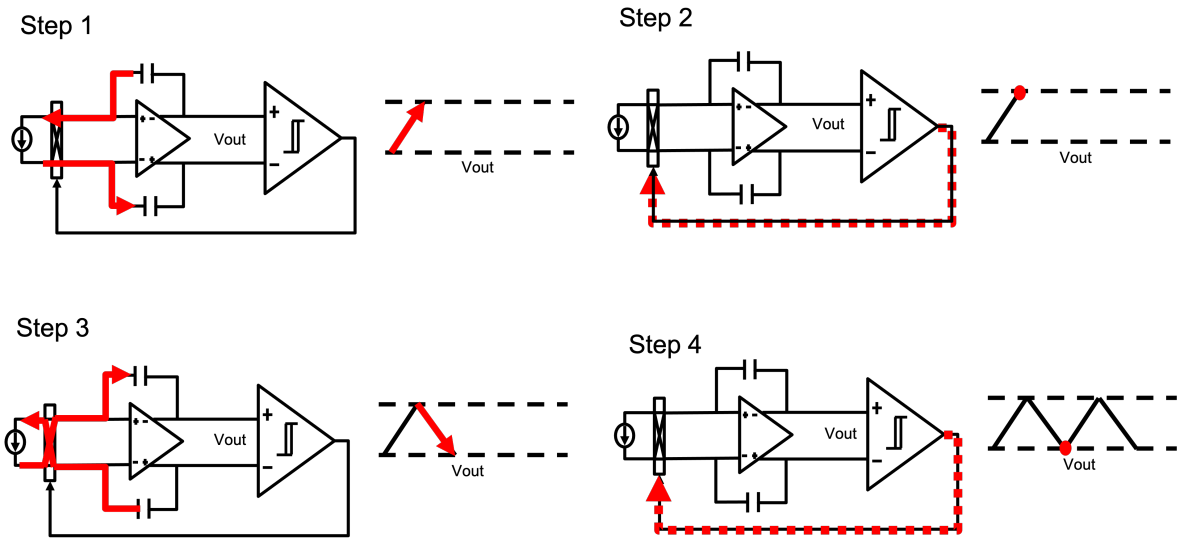


Figure 3.1: Integrator output within one cycle

The hourglass ADC structure can be simplified as a combination of a chopper, a C-TIA, and a comparator, connecting in the way shown in figure 3.1. A complete integration phase contains four steps: In step 1, the chopper is switched on so that the PD current can be integrated at the output of the integrator in one direction. The dashed line represents the threshold window set by the comparator. In the next step, when the integrator output crosses the threshold window, the comparator detects this crossing moment and triggers the chopper. In step 3, since the chopper is triggered, the input PD current starts to integrate along opposite directions but with the same slope since the PD current remains the same. Until the moment when integrator output reaches another threshold window edge, the chopper

is triggered again. The integration process repeats continuously, and the output of the integrator shows a symmetric triangle wave.

3.1.2 Main Benefit

C-TIA suffers from saturation problems, especially when the input current is large with limited supply voltage. In hourglass ADC, using a chopper, PD current is constantly folded into a pre-defined threshold window to avoid saturation. The frequency-to-current relation of the hourglass ADC can be calculated where C_f represents feedback capacitance of C-TIA, V_{thw} is the threshold window set by the comparator and T is the frequency of the triangle wave:

$$\frac{I_{pd}}{C_f} \cdot T = V_{thw} \tag{3.1}$$

This expression can derive a linearity relation between PD current I_{pd} and output frequency T. Even if the PD current is large, it is folded into a threshold window. With fixed feedback capacitance C_f and threshold window V_{thw}, the C-TIA works without limitation from the supply. In this way, the current measurement range is effectively extended by using the chopper.

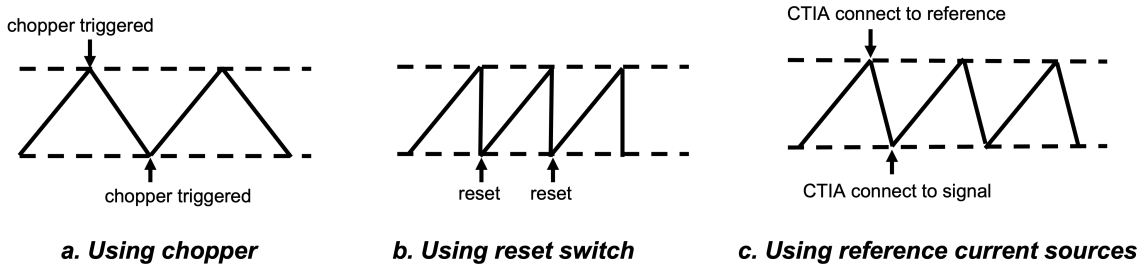


Figure 3.2: Methods that prevent C-TIA from saturation

There are also other methods to prevent C-TIA from saturation, like using a reference current source [7] or periodically reset the integrator [8]. The corresponding waveform seen from the output of C-TIA can be found in plots a, b, and c in figure 3.2. In the hourglass ADC structure, the chopper is triggered when the output voltage crosses the threshold window, and the PD current integrates with another direction. But if a reset switch is parallel to the feedback capacitance, it can reset the integrator. Once the integrator output reaches the threshold, the integrator is reset. In the next moment, the integration restarts, and the current integrates again using the same slope in the last integration

cycle. Also, a reference current source can be added along with PD. At the crossing moment, the integrator connects to the reference current source instead of PD, thus integrating the reference current in another direction. Compared with the hourglass ADC structure, architecture using a reset switch across feedback capacitance add sample noise from the reset switch, and architecture using a reference current source at the input may add extra noise from the current source.

3.1.3 Measurement Limitation

Although the hourglass ADC structure achieves a wide dynamic measurement range benefiting from current folding, the limitation is found for ultra-low current measurement.

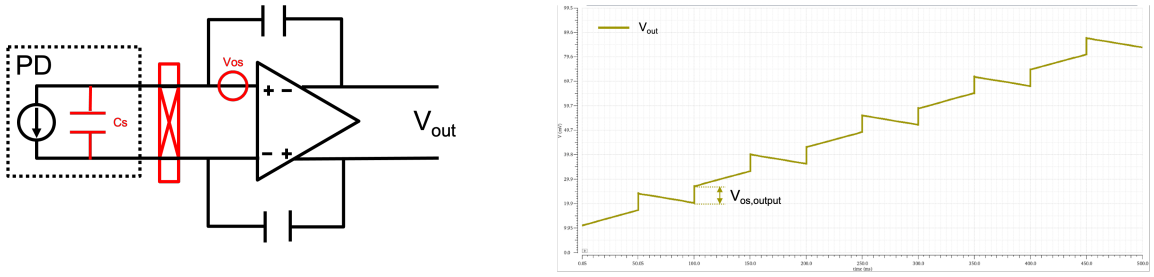


Figure 3.3: Integrator output drifting because of offset voltage

In hourglass ADC, the chopper is placed between the PD and the input of the integrator amplifier [4]. This structure has one drawback: The offset from integrator amplifier V_{os} is also chopped along with the PD current. In every chopper switching moment, the charge stored in parasitic capacitance C_s due to voltage offset is dumped to the output, resulting in a voltage step $V_{os,output}$,output that is seen at the integrator output

$$V_{os,output} = \frac{2V_{os}C_s}{C_f} \tag{3.2}$$

The parasitic capacitance C_s is around $1pF$, while the feedback capacitance Cf can be smaller than 100 fF when sensing a small input current. The offset of the integrator can be less than 100 μV after offset trimming. A plot of integrator output is generated from the simulation in figure 3.3. The offset voltage seen at output $V_{os,output}$ exceeds $1mV$, which is comparable to the smallest threshold window,

significantly eliminates measurement accuracy. Also, for a larger input current, the output frequency is increasing. The offset is accumulated in every single chopping moment and leads to output drifting.

3.2 Proposed Hourglass ADC for differential PD

A readout circuit is proposed utilizing hourglass ADC for fully differential PD. The overview of the proposed architecture can be found in figure 3.4. Compared with hourglass ADC structure introduced in chapter 3.1, some design improvements are made in the proposed architecture to meet the design target: choices of chopper position, design of threshold window and selection of gain setting. System-level noise analysis is provided in the end considering the noise requirements of the readout.

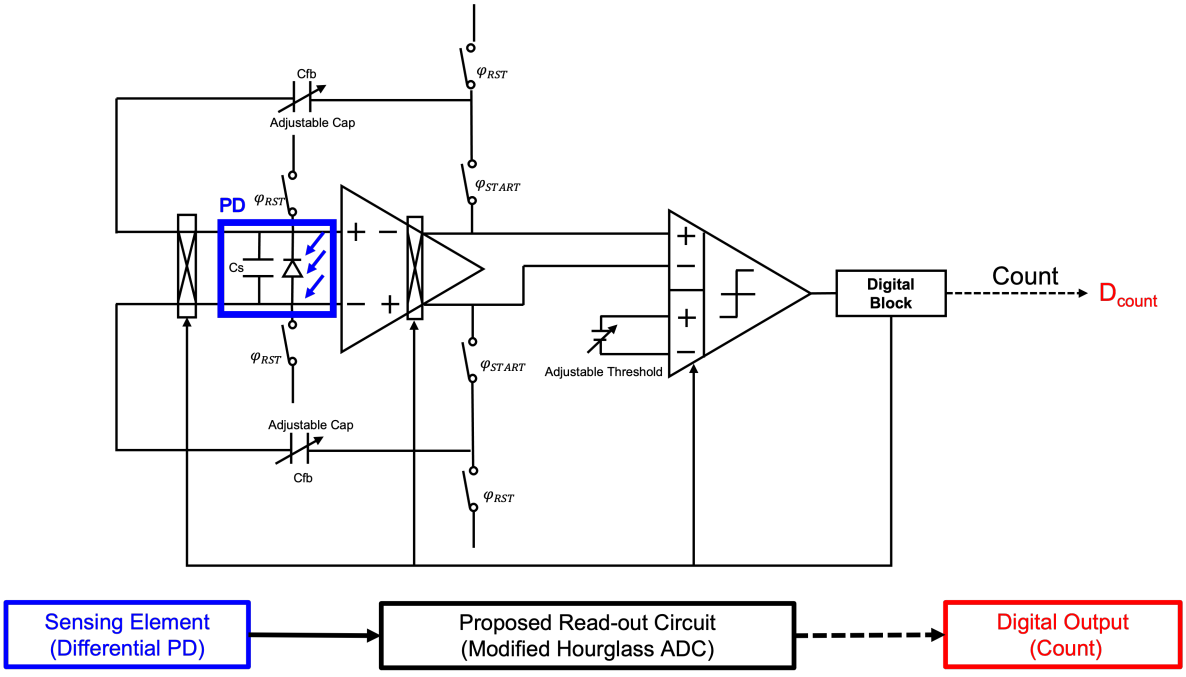


Figure 3.4: Proposed architecture overview

3.2.1 Chopper Position

One of the biggest differences between the hourglass ADC structure in the proposed architecture and the hourglass ADC in [4] is the chopper position. In the proposed architecture, the chopper is placed between PD and capacitance, as shown in figure 3.5. Compared with the structure where only one

chopper is used, the proposed architecture requires an extra chopper within the loop to ensure the negative feedback of the entire system.

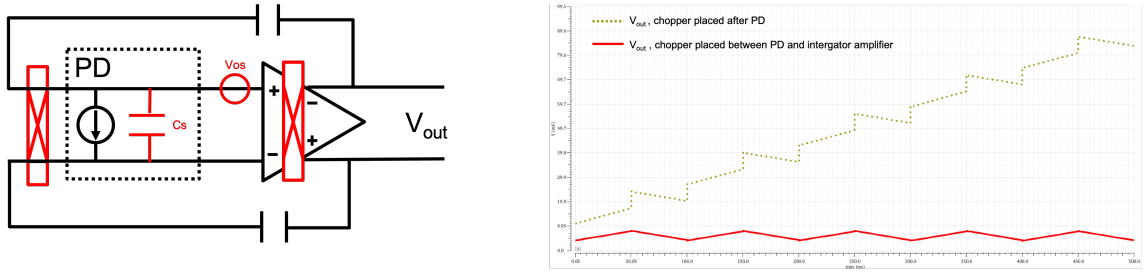


Figure 3.5: Reduced output drifting using new chopper position

As explained in chapter 3.1.3, the main cause of the output voltage drifting is the unnecessary charge dump in the switching moment. In the proposed architecture, the chopper is now connected between the PD and the feedback capacitance. Offset voltage V_{os} is added directly to the parasitic capacitance C_s without a chopper in-between. When the chopper is triggered, the voltage difference across C_s remains V_{os}. No extra charge will be dumped into the output during the chopping moment. The plot in 3.5 shows integrator output V_{out} in different chopper positions with equal offset voltage, feedback capacitance, and parasitic PD capacitance. The dashed yellow line shows output behavior when the chopper is placed after the PD. The output drifting effect is recognized. The integrator output in the new chopper position is plotted in a solid red line where the output drifting is effectively reduced.

3.2.2 Threshold Window

Another key design parameter in the proposed architecture lies in the threshold window design. Two different threshold window design options for hourglass ADC are shown in figure 3.6. The solid line is the modulated input signal after integration, and the dashed line represents the threshold window created by comparators.

Fixed Threshold Window

Two comparators can be used in an hourglass ADC structure to create a fixed threshold window: one determines the high threshold while the other determines the low threshold. Both comparators keep comparing during the entire integration phase and generate a fixed threshold window.

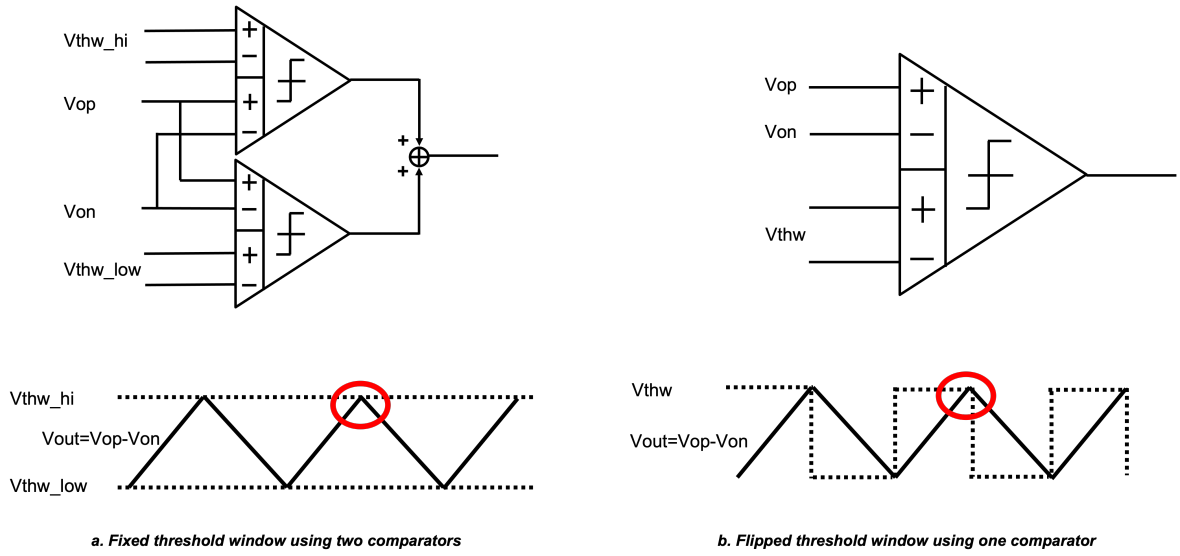


Figure 3.6: Threshold window design in hourglass ADC and proposed structure

Flipped Threshold Window

Alternatively, if only one comparator is used, the threshold window is flipped constantly between the high and low threshold. The flipping frequency is synchronized with the chopper switching frequency. One constrain for using such flipped threshold window is that the settling of the threshold window must be faster than the chopping frequency.

Comparing two different threshold window designs, both the fixed threshold window and the flipped threshold window achieve the same hourglass behavior, but the power can be saved when only one comparator is used. Also, two comparators cannot be completely equivalent in a real circuit. The accuracy of the threshold window is eliminated, therefore. For example, if the offset voltage of the two comparators is not equivalent, the voltage difference is directly added to the threshold window. Consequently, the measurement resolution of hourglass ADC is reduced when a small threshold window is applied for a small input PD current. On the contrary, if only one comparator is used, the same offset voltage appears on both high and low thresholds. The size of the threshold window remains the same.

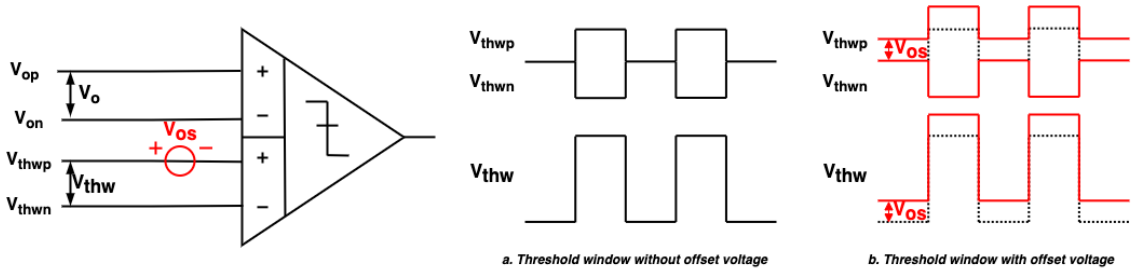


Figure 3.7: Effect of offset on threshold window using one comparator

The flipped threshold window has another benefit on meta-stability compared with the fixed threshold window. If the threshold window is fixed, the chopper determines the direction of the PD current based on the comparison result. If a small voltage variation appears on the integrator output, there is a certain possibility that an unwanted new comparison result is generated by the comparator. The chopper is trigged again before the end of a new integration period. This can be avoided using a flipped threshold window: The integrator output voltage remains the same, but the threshold is flipped to the next threshold. The comparison result is not affected regardless of any voltage variation at the integrator output.

3.2.3 Gain Setting

The frequency-to-current equation derived using the hourglass ADC structure contains two parameters that can be adjustable: Feedback capacitance C_f and threshold window V_{thw}. By adjusting C_f and V_{thw}, the output frequency changes accordingly. The measurement dynamic range can be extended when various combination of C_f and V_{thw} is chosen. C_f and V_{thw} should be small for a small input current and large for a large input current. In this way, the output frequency won't exceed a certain range, and the power of the integrator amplifier can be further saved.

Based on the design target, the readout should cover a current measurement range from $2fA$ to $200nA$ with a maximum conversation time of $100ms$. The maximum output frequency is calculated when the largest input PD current is measured. There are 13 gain settings that can be made to cover the entire measurement range. The resulting output frequency ranges from $10Hz$ to $250kHz$. The value of feedback capacitance and threshold window for each gain setting is listed in the table, and the maximum current range is calculated as well.

Gain_code	Gain	Cf	Vthw	Is_min	time_for_one count	Is_max	time_for_one _count
12	4096x	40fF	5mV	2fA	100ms	50pA	4us
11	2048x	80fF	5mV	4fA	100ms	100pA	4us
10	1024x	80fF	10mV	...	100ms	...	4us
9	512x	160fF	10mV	...	100ms	...	4us
8	256x	320fF	10mV	...	100ms	...	4us
7	128x	640fF	10mV	...	100ms	...	4us
6	64x	640fF	20mV	...	100ms	...	4us
5	32x	640fF	40mV	...	100ms	...	4us
4	16x	640fF	80mV	...	100ms	...	4us
3	8x	1.28pF	80mV	...	100ms	...	4us
2	4x	1.28pF	160mV	...	100ms	...	4us
1	2x	1.28pF	320mV	...	100ms	...	4us
0	1x	1.28pF	640mV	8.192pA	100ms	204.8nA	4us

Figure 3.8: Available gain settings

Gain-code 12

In this gain setting, C_f and V_{thw} is chosen to be $40fF$ and $5mV$. The Minimum PD current is $2fA$ with maximum time-for-one-count of $100ms$.

Gain-code 0

V_f and v_{thw} are the largest in this gain setting, with the value of $1.28pF$ and $640mV$. The maximum PD current is $204.8nA$ with minimum time-for-one-count of 4μs.

The expected frequency-to-current plot in each gain setting are shown in figure 3.9. The x-axis represents the PD current. Using 13 gain settings, the entire current measurement range varies from $2fA$ to $200nA$ (the entire x-axis), so the input range from the design target is covered. From the plot, the overlap in x-axis between adjacent gain settings are observed. In other words, intermediate PD current can be detected using several different gain settings.

A counter is added to the readout circuit to further digitize the output frequency. If determining the conversion time and knowing the exact gain setting, the count within one conversion period can be found. The expected count vs PD current plot is generated in figure 3.10 when the conversion time is $100ms$.

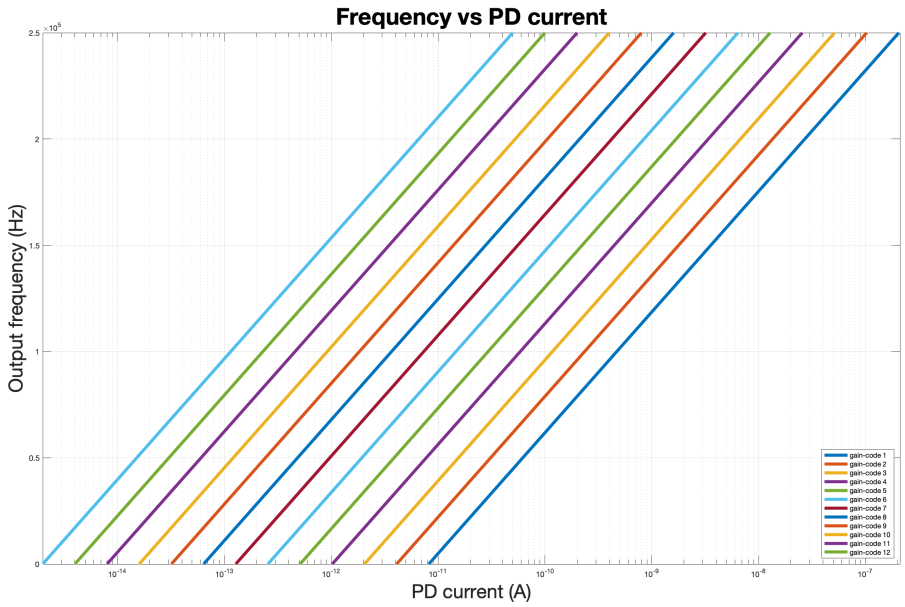


Figure 3.9: Frequency vs current with different gain settings

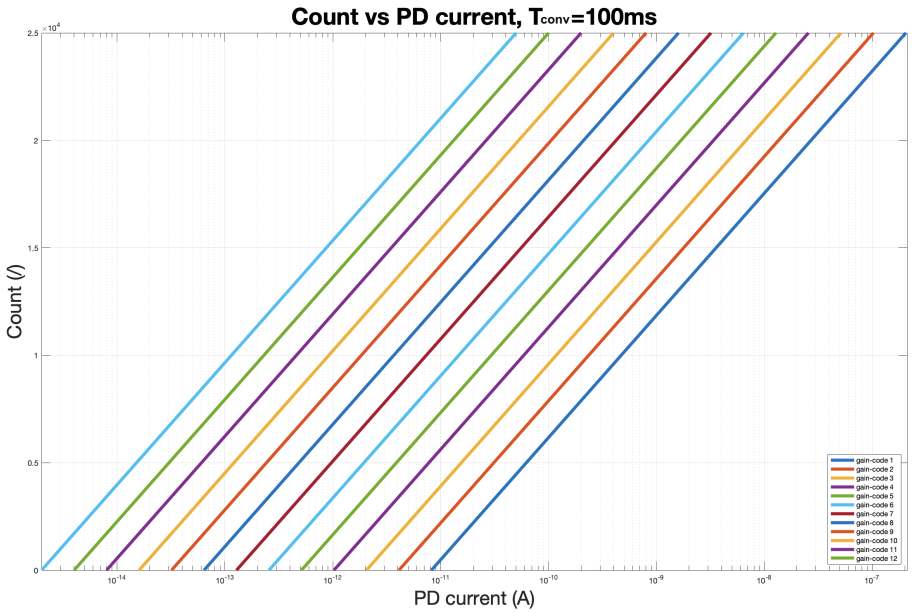


Figure 3.10: Count vs current with different gain settings when $T_{conv} = 100ms$

3.2.4 Noise Analysis

For the proposed PD readout based on hourglass ADC, counts are the final digital output. Therefore, the noise of the readout circuit is evaluated in the form of noise count. For a given integration period, the count during this period varies with the PD current input. In figure 3.10 from chapter 3.2.3, the count vs current plot shows the relation between count and input PD current with a given integration period of 100ms. It can be found that the minimum count is only 1 while more than 20k counts are generated for large input current.

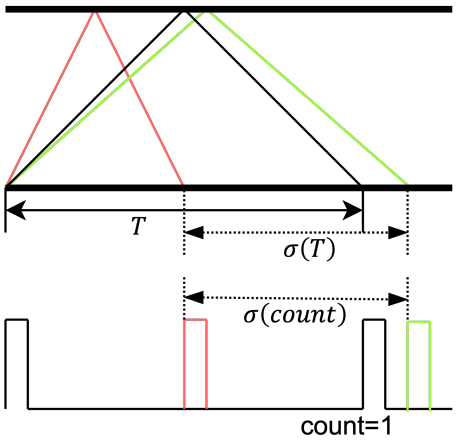


Figure 3.11: Count jitter caused by output-referred noise of integrator

As is shown in figure 3.11, the output-referred noise of the integrator together with current noise from the chopper causes the period jitter $\sigma(T)$ and results in count jitter $\sigma(count)$. When more counts are generated, the count jitter is reduced due to the noise averaging. The noise averaging effect explains how the system-level noise requirements are made related to the count: For counts smaller than 100, the count jitter should be less than one count; For counts more than 100, the count jitter should be smaller than 1%.

The root-mean-square (RMS) noise at the integrator output can be calculated based on the noise count requirement. The critical noise requirements lie on the smallest current input in each gain setting where the circuit does not benefit from noise averaging. Two examples are given below when only one count is generated in two different gain settings: gain-code 12 and gain-code 0.

Example 1: Gain-code 12

For the smallest input $I_s = 2fA$, the count is 1 when the conversion time is $100ms$. When gain-code is 12, the feedback capacitance C_f is $40fF$, and the threshold window is $5mV$.

$$\sigma(count) < 1count \tag{3.3}$$

$$\sigma(T) < 100ms \tag{3.4}$$

Since only one count is generated during the conversion period, the calculated RMS noise at integrator output within one period is not averaged with the value

$$V_{n,rms} = \sigma(T)\frac{2I_s}{C_f} = 10mV \tag{3.5}$$

Example 2: Gain-code 0

When the output count is 1, the corresponding PD current is $8.2pA$ when gain-code is 0. The feedback capacitance C_f in this gain setting is $1.28pF$, and the threshold window is $640mV$.

$$\sigma(count) < 1count \tag{3.6}$$

$$\sigma(T) < 100ms \tag{3.7}$$

Since only one count is generated during the conversion period, the calculated RMS noise at integrator output within one period is not averaged with the value

$$V_{n,rms} = \sigma(T)\frac{2I_s}{C_f} = 1.28V \tag{3.8}$$

In this thesis, noise requirements of the readout are examined at both circuit-level in chapter 4 based on the RMS noise calculated above and system-level in chapter 5 in form of noise count.

4 Circuit Implementation

4.1 Top-level Architecture

In the last chapter, the overview of the proposed architecture is given in figure 3. In this chapter, more details about the circuit design are introduced. A circuit-level overview of the proposed architecture can be found in figure 4.1, which indicates the circuit implementation of some sub-blocks, such as chopper, adjustable threshold window, and capacitance array. Digital blocks are placed at the end of the circuit to control the adjustable threshold window and two choppers and generate digital counts as the final output of the readout circuit. Some external codes and clocks are also included in the overview, including the gain setting code, the offset trimming code, the integration time, and the system clocks.

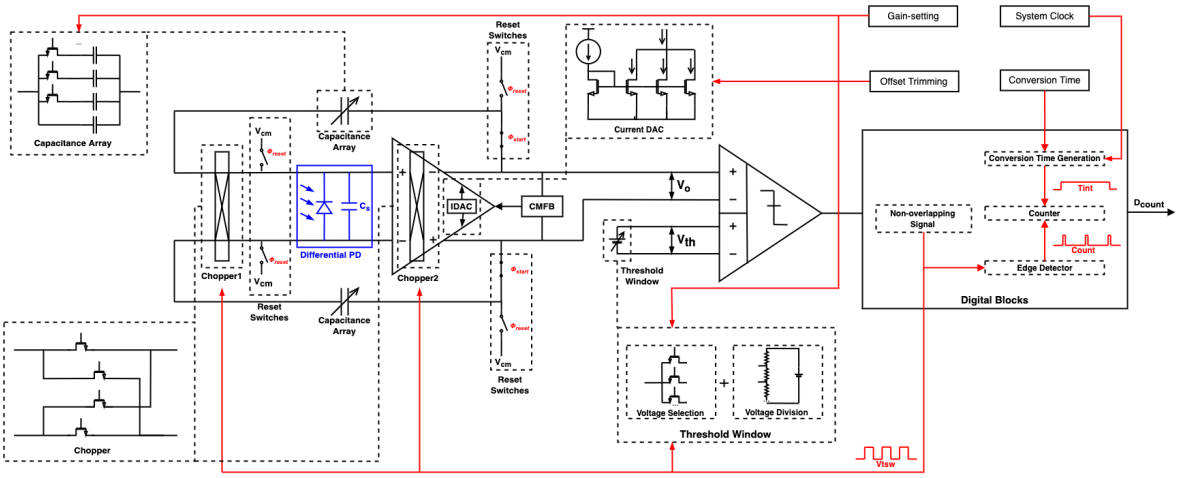


Figure 4.1: Circuit-level implementation overview of proposed architecture

Figure 4.2 presents the timing diagram of the designed readout circuit. Before the real measurement starts, there is a start-up phase when the entire circuit is reset. The integrator's input and output are connected to the common-mode voltage V_{cm} to zero-bias the PD. During this phase, when signal I_{trim} is high, the offset of the integrator amplifier is trimmed. After the start-up phase ends, the reset switches open, and the capacitance array is connected. The hourglass ADC starts working. The integrator output V_o generates a triangle wave while threshold window V_{thw} flips between high and low threshold with the same switching frequency. The driving signal of both the threshold window and two chopper

switches $Vtsw$ is sent by the counter so that the count pulse is generated. The conversion signal T_{conv} defines a pre-determined conversion period. Counts generated in this period are recorded as D_{count}.

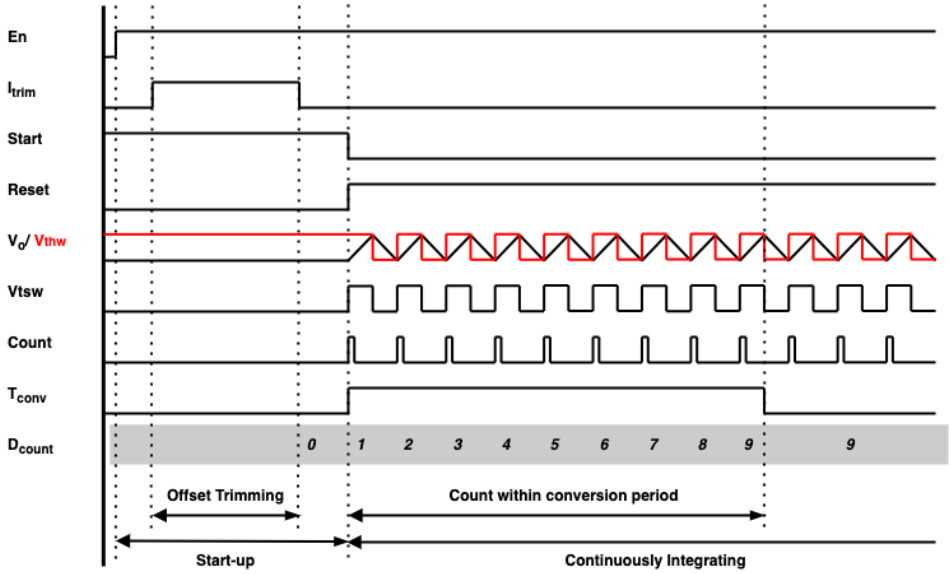


Figure 4.2: Timing diagram of proposed architecture

The circuit design details for sub-level blocks are introduced for the rest of this chapter. The introduction is divided into three parts to cover the entire readout circuit: Integrator, Comparator, and Digital Blocks. The transistor-level circuit is demonstrated in each part, followed by design considerations and relevant motivations.

4.2 Integrator

A fully differential integrator is implemented in this proposed design to utilize the hourglass behavior. The fully differential integrator contains two choppers: chopper1 and chopper2. The feedback capacitance C_f is arranged by a capacitance array which is also differential. Reset switches are placed at both input and output of the integrator amplifier to reset the integrator. The integrator amplifier is also differential, requiring common-mode feedback biasing technique. The offset of the integrator amplifier is trimmed by the external current DAC.

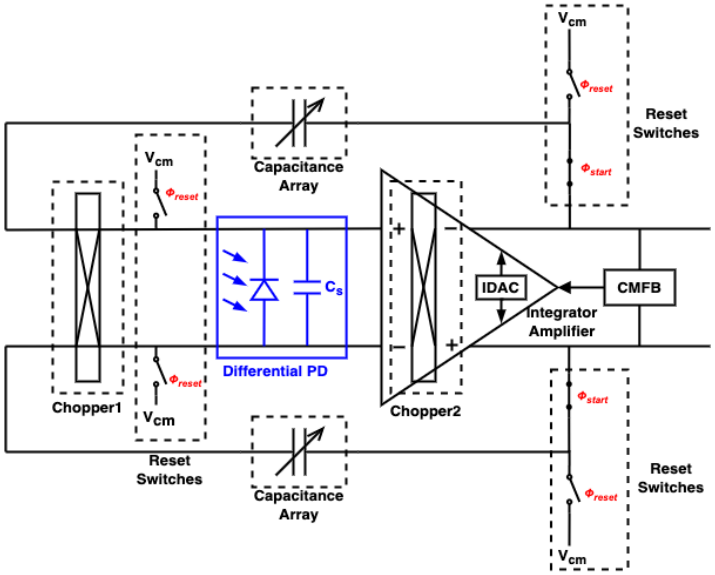


Figure 4.3: Integrator overview

4.2.1 Reset Switches

In total, three pairs of switches are included in the circuit to realize the reset scheme of the integrator. One pair of switches is placed at the input with PD and chopper1. Another side of this pair of switches is connected to the common-mode voltage V_{cm}. Rest two pairs of reset switches are placed at the output: one pair is connected between the capacitance array and output of the integrator amplifier, and another pair is connected between the capacitance array and V_{cm}.

The two pairs of switches whose one side is connected to V_{cm} are driven by the control signal ϕ_{reset}, while the rest pair is driven by ϕ_{start}. During the start-up phase, the ϕ_{reset} is high logic, and ϕ_{start} is low logic. Both the input and output of the integrator of the amplifier are connected to common-mode voltage V_{cm} to reset the integrator. The capacitance array is disconnected in this phase. At the end of the start-up phase, ϕ_{reset} turns to low logic while ϕ_{start} turns to high logic. The capacitance array is connected so that the integration process starts. The detailed timing diagram can be found in figure 4.2, including the start-up phase mentioned above.

Theoretically, once the switch is open, the switch has large resistance so that the leakage current is nearly zero. However, the switch is usually implemented by NMOS transistors in a real circuit. The

gate of the NMOS transistor is connected to the logic low voltage V_{ss} to open the switch. Because of the reversed biased junction between the source/drain to the substrate, there is always a certain amount of leakage current induced even when the transistor is off.

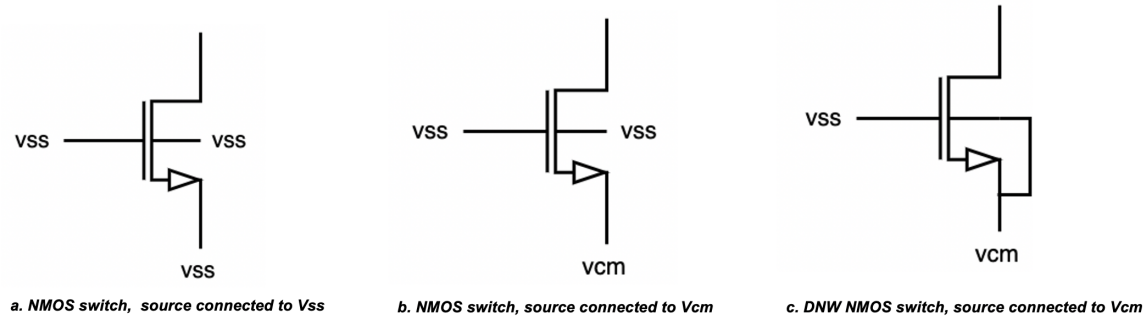


Figure 4.4: Different types of switches with different source/bulk potential

Figure 4.4 shows different types of MOS transistors in different bias conditions when the transistor is off. The gate of the MOS transistor is connected to the low logic V_{ss} to turn off the transistor. One side of the switch should be connected to the integrator amplifier while the other is connected to another potential during the reset phase, usually V_{ss}. In subplot a, a single NMOS transistor is used as a switch where one side of the transistor is connected to V_{ss}. However, a fully differential integrator amplifier is used in actual circuit design. The common-mode voltage of the amplifier is set to a positive potential V_{cm} instead of V_{ss}. Therefore, to reset the amplifier, the source of the MOS is connected to V_{cm} instead of V_{ss}. The non-zero drain/source to the substrate voltage produces junction leakage current. A better solution is given in subplot c to reduce leakage current. NMOS switches using an extra deep-n-well layer make it possible to bias the bulk of the MOS transistor to a different potential to the substrate. In subplot c, the bulk and source are connected to the same voltage V_{cm} as the source voltage, thus effectively reducing the leakage current.

4.2.2 Chopper

The structure of the conventional chopper is shown in figure 4.5. Four switches are connected in such a way that only two of them are open or closed in one chopping phase. In chapter 3.2, the final choice of the chopper in the proposed architecture is introduced and motivated. Two choppers are

used where chopper1 is placed at the input of the integrator amplifier while chopper2 is placed inside the integrator amplifier. Since the PD is also placed at the input of the integrator amplifier next to chopper1, the following error sources caused by chopper1 must be considered to minimize its effect on PD current: leakage current and equivalent input current due to chopper mismatch.

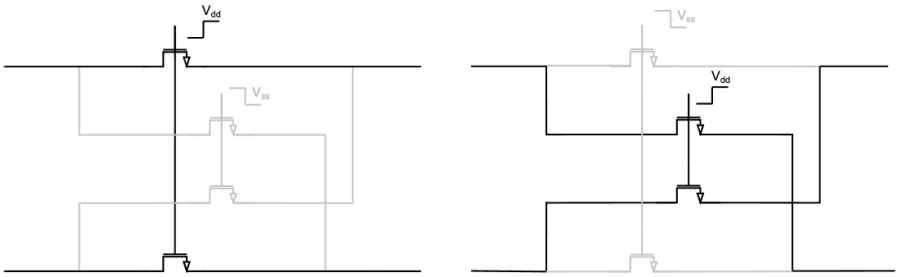


Figure 4.5: Basic working principle of chopper

Equivalent Input Current

The parasitic capacitance between the gate and source/drain of the MOS transistors is non-negligible when considering the equivalent input current caused by chopper switches. When a transistor switch turns off, the charge stored at the transistor's gate flows out of the channel. The charge is injected into the transistor's drain or source terminal through the parasitic capacitance. The effect is called charge injection. The charge injection can be canceled in a chopper if there is no mismatch between parasitic capacitance in the chopper pair. However, if the mismatch error exists, the charge disturbed in the chopper switching moment is unbalanced, causing a current spike in the switching moment. If averaging the current spike during one phase, an equivalent input current is induced.

The amount of equivalent input current is mainly determined by the charge stored in the gate of the transistor Q and the chopping frequency f

$$I_{eq} = \frac{Q}{T/2} = 2fQ \tag{4.1}$$

$$Q = C_{ox}WL(V_{gs} - V_{th}) \tag{4.2}$$

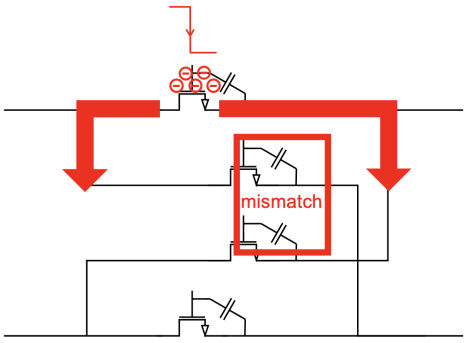


Figure 4.6: Equivalent input current caused by chopper mismatch

The chopping frequency is asynchronous to the amount of input signal: PD current. The amount of charge is determined by the gate-oxide capacitance C_{ox}, width W, length L, gate-source voltage V_{gs}, and the threshold voltage of the MOS transistor V_{th}, as shown in equation 4.2. To minimize the equivalent input, the chopper switches' length and width are chosen to be small with the value of $200nm$ and $220nm$. The induced equivalent input of the chopper is examined by running the Monte Carlo (MC) simulation, considering the mismatch of chopper switches. The equivalent input current is added to the dark current and contributes to the dark count when PD current is zero. The maximum dark offset is $3.83mV$, and the corresponding dark count is less than one count.

Name	Yield	Min	Target	Max	Mean	Std Dev	Cpk	Errors
- dark offset(summary)	100	2.812m		3.83m	3.19m	210.4u		0
dark offset_mc_mis	100	2.812m	info	3.83m	3.19m	210.4u		0

Figure 4.7: Maximum dark count due to chopper equivalent input current

Leakage Current

A chopper consists of four switches, and switches produce leakage current. For chopper switches, the total leakage current presents as the differential leakage current between two switches closing simultaneously. When there is no offset voltage from the integrator amplifier, V_{ds} for each chopper switch remain the same. Therefore, although both switches produce leakage current ($I_{leakage1} = I_{leakage2}$), there is no differential leakage current produced. When V_{ds} is unbalanced due to the offset voltage of the integrator amplifier, the differential leakage current occurs with the value $I_{leakage2} - I_{leakage1}$.

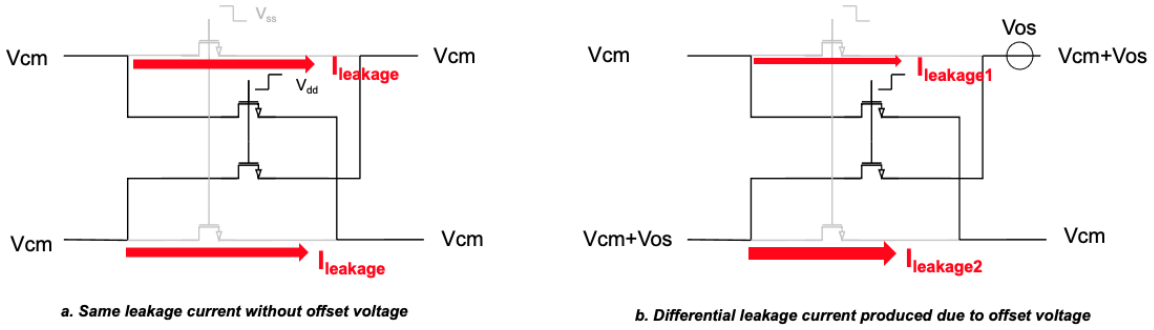


Figure 4.8: Leakage current from chopper switches

Also, like reset switches, all switches in chopper1 are NMOS transistors layout in deep-n-well to reduce the leakage current. Offset voltage and doping concentration of the NMOS switches decide the amount of leakage current instead of chopper size. The chopper leakage current is tested by applying the residue offset of the integrator amplifier, where the chopper size is the same when optimizing the equivalent input current. The maximum dark offset due to chopper leakage current is 3.62mV over PVT, resulting in less than one dark count.

		ff_0	ff_1	ss_0	ss_1	tt_0	tt_1	tt_2
		ff_lib	ff_lib	ss_lib	ss_lib	tt_lib	tt_lib	tt_lib
		-40	85	-40	85	-40	27	85
Min	Max	ff_0	ff_1	ss_0	ss_1	tt_0	tt_1	tt_2
2.299m	3.623m	2.832m	3.623m	2.299m	2.81m	2.459m	2.657m	3.128m

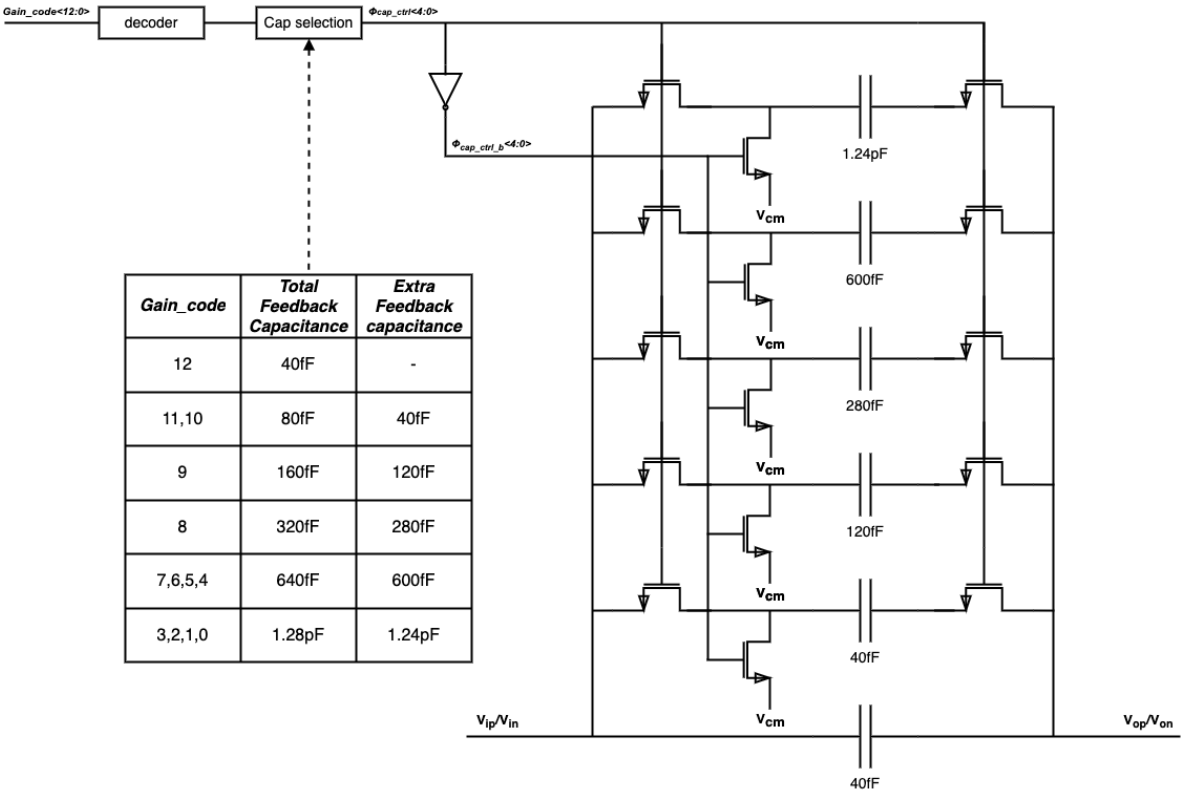
Figure 4.9: Maximum dark count due to chopper leakage current

4.2.3 Capacitance Array

The proposed architecture uses the capacitance array to increase the measurement range of the readout circuit. Earlier in chapter 3.2.3, 13 gain settings are defined in figure 3.8. According to the gain setting table, the minimum capacitance used in this design is $40fF$. It is chosen so that the conversion time for the smallest PD current is within $100ms$. The reset five pre-defined capacitance levels are $80fF$, $160fF$, $320fF$, $640fF$, and $1.28pF$. In a real circuit, the $40fF$ capacitance is always connected to the circuit. An extra capacitance is added to the $40fF$ basic capacitance according to specific gain settings for each capacitance level. Therefore, if subtracting $40fF$ capacitance, the value of extra capacitance

in each capacitance level now becomes $40fF$, $120fF$, $280fF$, $600fF$, $1.24pF$.

When a gain-code is chosen, it is first sent to a decoder. Then based on the capacitance selection table shown in figure 4.10, two opposite control signals for the switches are generated. The switches in each capacitance array are turned on or off accordingly.



Gain_code	Total Feedback Capacitance	Extra Feedback capacitance
12	40fF	-
11,10	80fF	40fF
9	160fF	120fF
8	320fF	280fF
7,6,5,4	640fF	600fF
3,2,1,0	1.28pF	1.24pF

Figure 4.10: Arrangement of capacitance array

Switches placed next to the extra capacitance are used to control the capacitance level based on gain settings. In this readout circuit design, switches are placed at the input and output of the capacitance array. If no switches exist at the output, the entire capacitance array is always connected to the output, resulting in extensive output capacitance loading. The sum of total capacitance from the capacitance array is more than $2pF$. This large output capacitance eliminates the integrator amplifier's performance and reduces the measurement accuracy. As a solution, Switches are added to avoid this

undesired effect. Now the sum of parasitic capacitance from switches becomes the output capacitance. The unit of the parasitic capacitance of a MOS switch is around fF, which is negligible compared with the minimum capacitance of $40fF$. The switches should also be placed at the input to prevent large parasitic capacitance from being added to the input. The resulting large capacitance $2pF$ is added to the parasitic capacitance from PD, severally increasing the noise contribution from the integrator amplifier.

Also, between the switch at the input and the capacitance, another switch connects the left terminal of capacitance to the common-mode voltage V_{cm}. With this additional switch, the unused capacitance array is completely disconnected from the circuit, producing less current leakage.

Like the reset and chopper switches, the input switches' leakage current needs to be concerned. Deep-n-well NMOS transistors are used for the two switches placed on the left side of the capacitance array to eliminate the leakage current.

4.2.4 Integrator Amplifier

Figure 4.11 shows the schematic overview of the fully differential two-stage amplifier with a common-mode feedback amplifier used in the integrator. As is described in chapter 3.2, a chopper is placed in the amplifier to ensure the negative feedback. And chopper2 from figure 4.3 can be recognized as the chopper between the two stages of the amplifier. The offset of the two-stage amplifier is trimmed by injecting current from the external current DAC is injected into the amplifier through a current buffer. The stability of the two-stage amplifier is compensated with Miller capacitance and resistance.
The two-stage topology is chosen to maximize the output swing. From the simulation result, the designed two-stage amplifier achieves a DC gain higher than $80dB$. The phase margin is greater than 69 degree, and the gain margin is greater than $10dB$ over PVT. The Gain-Bandwidth Product is more than $12MHz$ to provide enough gain for the highest signal frequency.

The two-stage topology is chosen to maximize the output swing. From the simulation result, the designed two-stage amplifier achieves a DC gain higher than 80dB. The phase margin is greater than 69 degree, and the gain margin is greater than 10 dB over PVT. The bode plot of the integrator amplifier is shown in figure 4.12

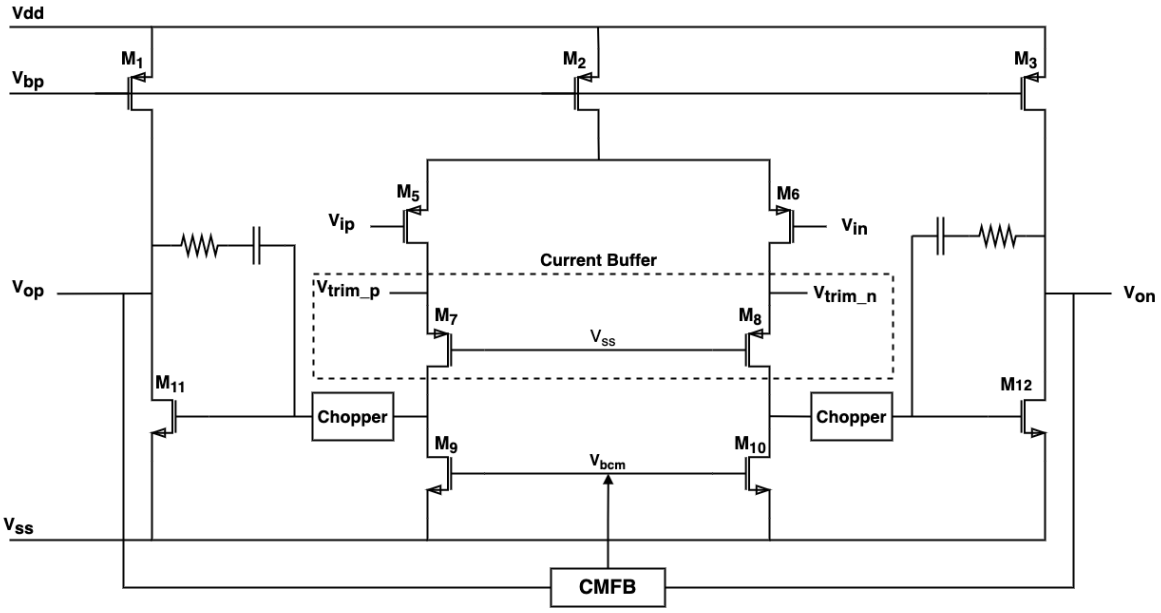


Figure 4.11: Integrator amplifier

Integrator Amplifier should provide enough gain to eliminate the distortion so that the linearity of the PD readout is ensured. The PD parasitic capacitance C_s and feedback capacitance C_f together determine the close loop gain of the integrator. For signal modulated with high frequency, the close loop gain of the integrator should be large enough so that the PD current keeps integrating at the feedback capacitance. The concept of Gain-Bandwidth Product (GBW) is used to estimate the trade-off between gain and bandwidth. In the designed integrator amplifier, the achieved GBW is 12MHz, which is at least two times larger than the close loop bandwidth in all gain settings.

Chopper in Amplifier

Since the integrator amplifier has two stages, chopper2 can be placed between the two stages. The control signal of chopper2 between the two stages is synchronized to chopper1 placed at the input of the integrator. The red curve represents the signal path in different chopping phases from figure 4.13. Both cases ensure a negative path from the input of the amplifier to the output.

Chopper2 is placed between the first and the second stage as indicated in figure 4.11. The voltage variation in the chopping point caused by the charge injection is effectively eliminated since the out-

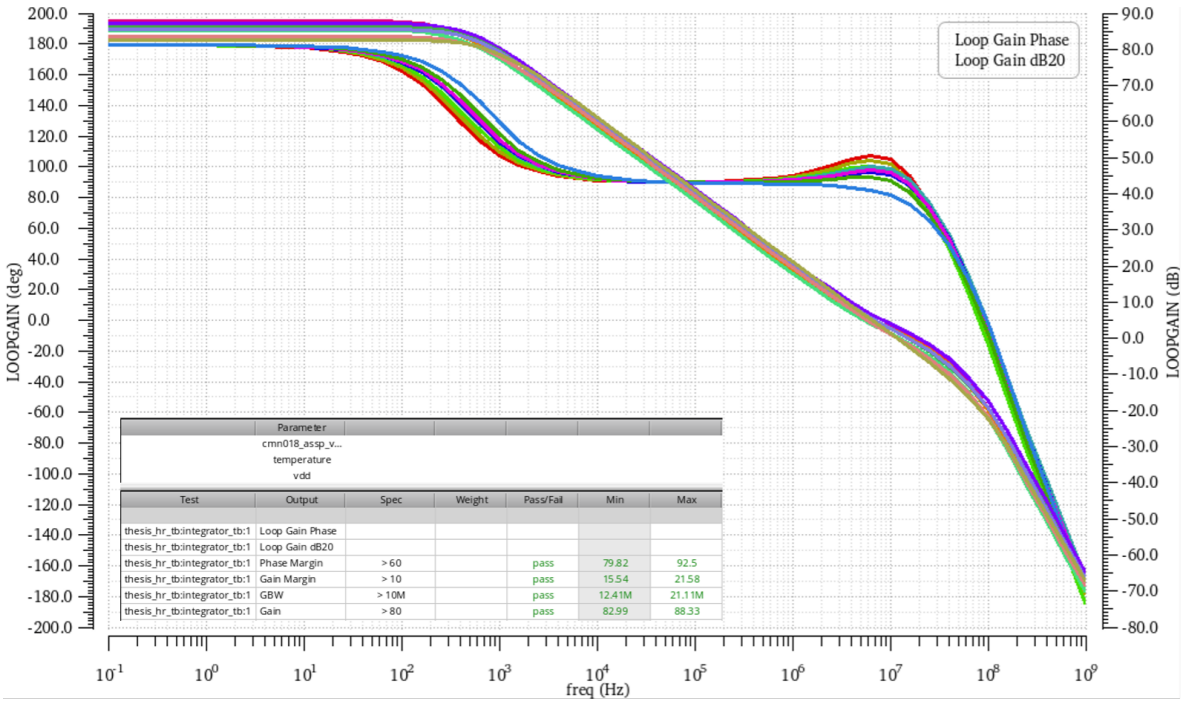


Figure 4.12: Frequency response of Integrator amplifier

put resistance of the first stage is boosted by current buffer M7 and M8. Therefore, the MOS switch used in this chopper is a typical NMOS transistor instead of NMOS in deep-n-well. Also, the size of the switches is small to minimize the charge injection.

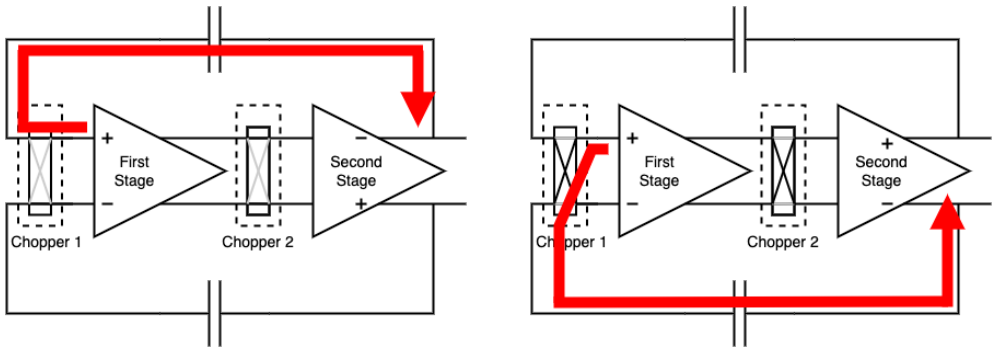


Figure 4.13: Negative feedback of integrator in two chopping phases

Common-mode Feedback Circuit

A fully differential amplifier requires a common-mode feedback (CMFB) biasing circuit. The common-mode voltage of the amplifier is set to be half of the V_{dd} to maximize the available output swing. The maximum threshold window determines the maximum voltage swing at the integrator output, which is equal to half of the threshold with a value of $320mV$.

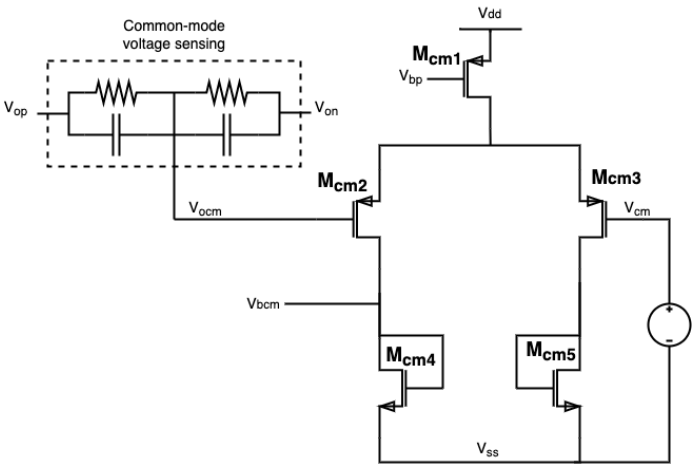


Figure 4.14: Common-mode Feedback Circuit

The schematic overview of the common-mode feedback circuit is shown in figure 4.14. Vop and Von are the differential output of the integrator. The common-mode voltage V_{ocm} is sensed through an R-C averaging circuit. The choices of the resistance value in R-C averaging are made so that the output resistance of the integrator amplifier is not severely suppressed. And the capacitance value in the R-C averaging circuit is determined so that the frequency behavior of the entire amplifier still meets the requirements. The reference common-mode voltage V_{cm} is given at one side of the CMFB circuits compared with the sensed common-mode voltage V_{ocm} at the other side. The current is balanced between two differential paths, and the biasing point V_{bcm} is defined.

Offset Trimming Technique

Transistors M_7 and M_8 in figure 4.11 compose a current buffer that is used to buffer the current from external current DAC. The offset voltage of the integrator without trimming is measured to be less than $5mV$. Suppose no offset trimming technique is applied for the integrator amplifier. In that case, the leakage current from the chopper switch, reset switches, and control switches from the capacitance array are much higher than the minimum measured PD current.

Therefore, the offset trimming technique is implemented. The current buffer is placed inside the amplifier with two current injection terminals on both sides to trim the positive or negative offset voltage. Before the integrator starts to work, there is a start-up phase to reset the integrator. The offset voltage is measured during this period. The code of the external DAC is provided based on the detected offset voltage. The corresponding current is then injected to one of the terminals: V_{trim_p} or V_{trim_n}. To compensate the offset, the injected current is converted into voltage through transistor M_7 or M_8 (gm_7 or gm_8). The current injection is continuous during the entire integration process.

An 8-bit current DAC with differential current output is implemented to realize the accurate current compensation. There is an extra bit in the current DAC to control the output current direction. The current DAC has a compensation range of $400nA$, and the compensation resolution is $1.56nA$. The transconductance of the current buffer is 65μS to cover an offset compensation range of more than $6mV$. The maximum residue offset after trimming is $60uV(3\sigma)$.

4.2.5 Integrator Noise

For an integrator, the root-mean-square (RMS) noise at the integrator output can be calculated as

$$V_{n,int,rms}^2 = {V_{n,amp}}^2(1+\frac{C_s}{C_f})^2\frac{\pi}{2}f_H \tag{4.3}$$

where $V_{n,amp}$ is the input-referred noise from integrator amplifier. C_s is the parasitic capacitance of PD and C_f is the feedback capacitance. f_H stands for the close-loop bandwidth, which is derived from the GBW of the integrator amplifier and close-loop gain

$$f_H = \frac{GBW}{1+\frac{C_s}{C_f}} \tag{4.4}$$

The integrator amplifier is a two-stage full-differential amplifier which means the main noise contribution comes from the first stage, where the noise from the differential input pair is dominate

$${V_{n,amp}}^2 = 2(\frac{4kT\gamma}{gm}+\frac{K}{C_{ox}WL}\frac{1}{f}) \tag{4.5}$$

The noise spectrum of the integrator amplifier is shown in figure 4.15. According to equation 4.3, the output RMS noise for an integrator is related to feedback capacitance C_f which is different in different gain setting. The RMS noise is largest when at gain-code 12 since the feedback capacitance C_f is smallest in this gain setting. On the contrary, when gain-code is 0, the RMS noise of the integrator is smallest. The simulation result shows that the RMS noise of integrator $V_{n,int,rms}$ is $1.39mV$ when gain-code is 12 and 303 μV when gain-code is 0.

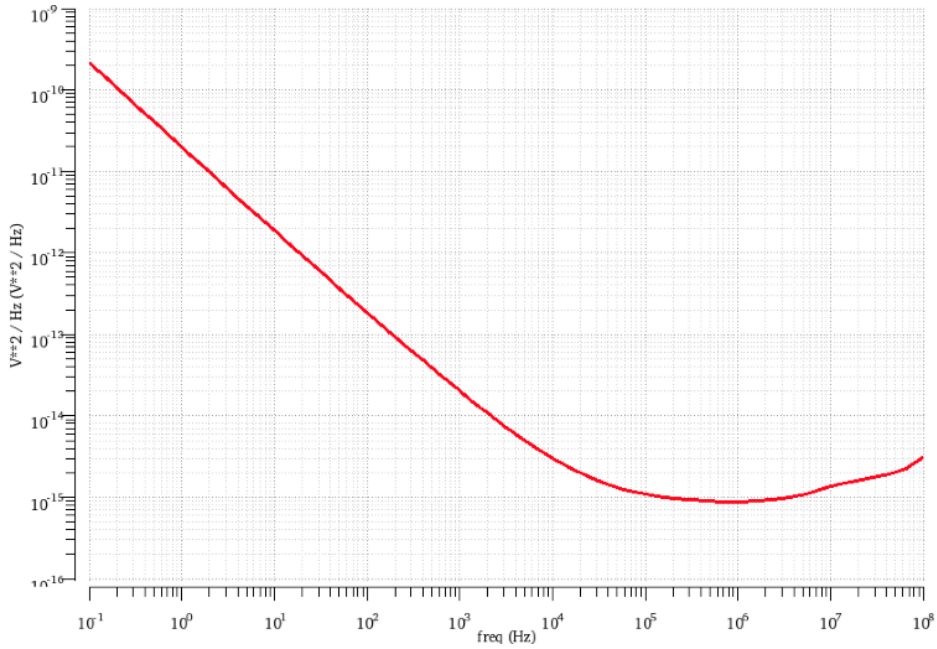


Figure 4.15: Noise spectrum of integrator amplifier

4.3 Comparator

As is discussed in chapter 3.2, only one comparator is placed after the integrator. Since the output of the integrator has two differential outputs, the comparator must have four ports for both differential input (V_{ip} and V_{in}) and differential reference (V_{thp} and V_{thn}). Two ports are connected to the integrator output, while two are connected to the threshold window. The continuous-time comparator compares the modulated signal with the threshold window during the entire measurement process.

The circuit overview of the comparator is shown in figure 4.16. It is essentially a pre-amplifier followed by a level shifter. Four equally sized input transistors $M1$, $M2$, $M3$, and $M4$ are used to create the four terminals of the comparator. The load of the pre-amplifier contains two PMOS diodes M7 and M8 and two cross-coupled latches $M7$ and $M8$. One benefit of this architecture is that it does not need a common-mode feedback circuit [9]. The first stage of the comparator utilizes a high-gain pre-amplifier and continuously amplifies the voltage difference between differential input and reference. A level shifter further enlarges the voltage difference, composed of transistors $M5$, $M10$, $M11$ and $M12$. A voltage buffer is placed at the end of the comparator to buffer the comparator output.

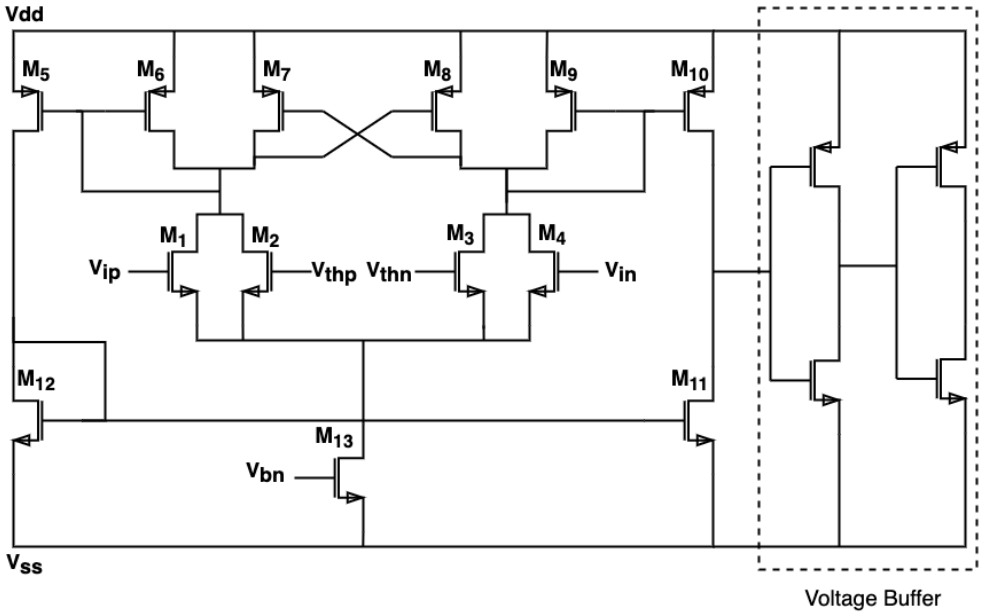


Figure 4.16: Schematic of the four-input continuous-time comparator

The delay of the comparator is within 35ns for gain-code 12 and 20ns for gain-code 0 where the input signal is modulated with the highest frequency of 250 kHz.

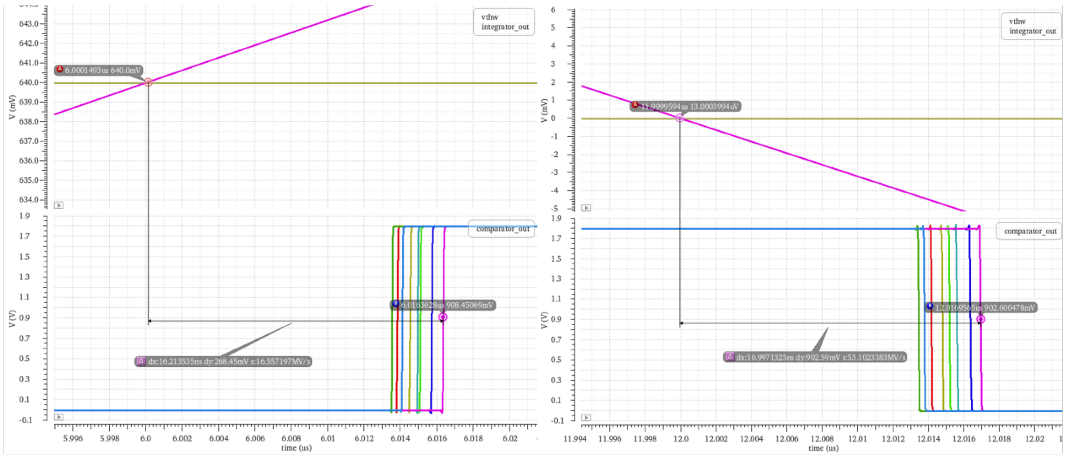


Figure 4.17: Comparator delay in rising and falling edge

4.3.1 Adjustable Threshold Window

Like the design of the capacitance array described in chapter 4.2.3, the threshold window is adjustable to increase the current measurement range. The implementation of the adjustable threshold window is shown in figure 4.18. Two selection processes are executed at the same time: one selects the threshold based on gain-code, and the other selects the window level flipping between high and low with the frequency synchronized to the chopper switching frequency.

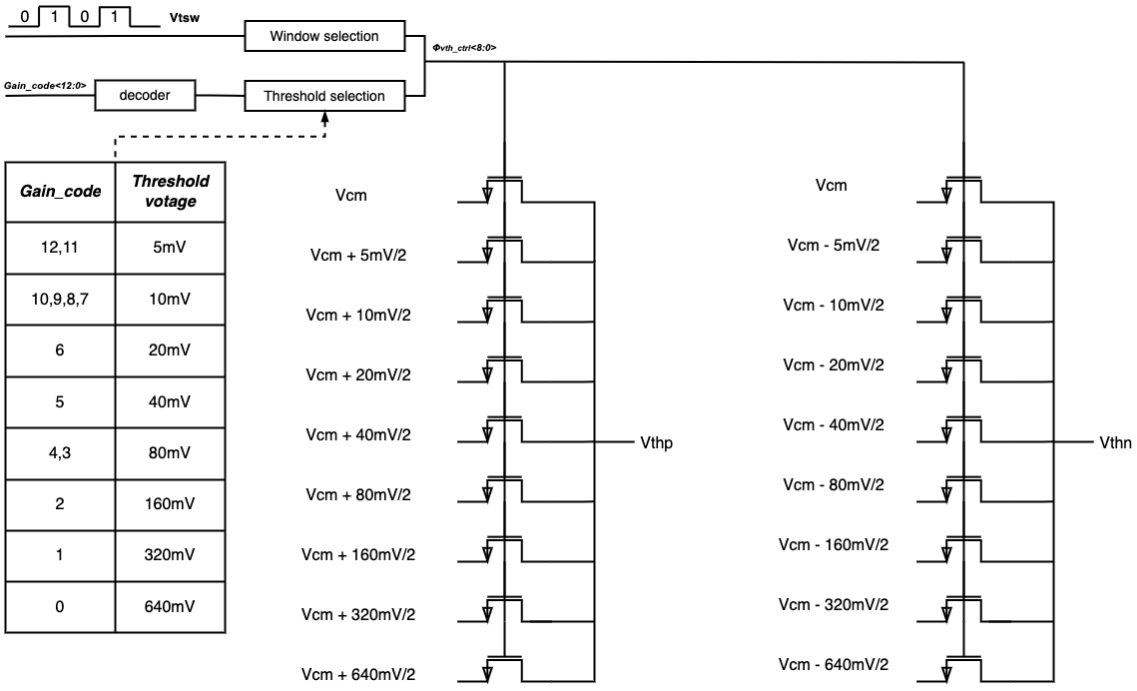


Figure 4.18: Adjustable threshold window for comparator

Reference Voltage Generation

In the reference voltage generation circuit presented in figure 4.19, two pairs of equivalent resistance voltage dividers divide the power supply voltage from V_{dd} to V_{ss}. The resistance divider is symmetrical to generate the fully differential reference voltage. A resistor trimmer is contained in the circuit to provide an accurate threshold window as well as a stable common-mode voltage of V_{cm}.

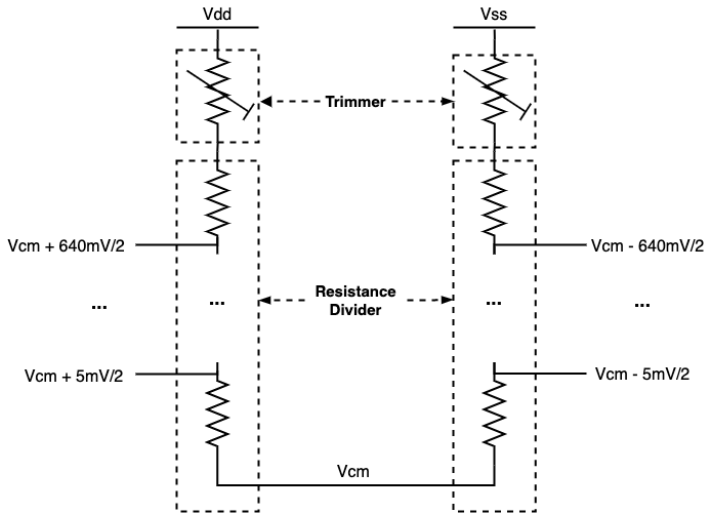


Figure 4.19: Reference voltage generation for threshold window

Threshold Selection

Switches are between the reference voltage and the differential reference terminal V_{thwp} and V_{thwn}. Like the capacitance selection introduced in the design of the capacitance array, the gain- setting table defines the threshold voltage with a given gain-code. V_{thwp} and V_{thwn} switch between different reference voltage levels accordingly.

Window Selection

In this design, the low level from the threshold window is the common-mode voltage V_{cm}, while the high level becomes the common-mode voltage plus the threshold V_{cm} + V_{thw}. The corresponding threshold voltage V_{thw} and the feedback capacitance C_f is determined based on the gain setting table. As is explained in figure 4.20, a multiplexer (MUX) is placed after the comparator. The voltage level selection is not activated until the start-up phase ends. Once the current measurement starts, the comparator is enabled. The first comparison result between the output of the integrator V_o and initial threshold voltage V_{thw} is used to drive the chopper switch and threshold voltage selection through the control signal $Vtsw$. Two MUXs execute the voltage selection before the differential comparator reference terminals V_{thwp} and Vthwn. The high threshold level is V_{cm} + $1/2V_{thw}$ for V_{thwp} and V_{cm} $1/2V_{thw}$ for V_{thwn}, respectively. The low threshold level for both terminals is the same: both are equal to common-mode voltage V_{cm}.

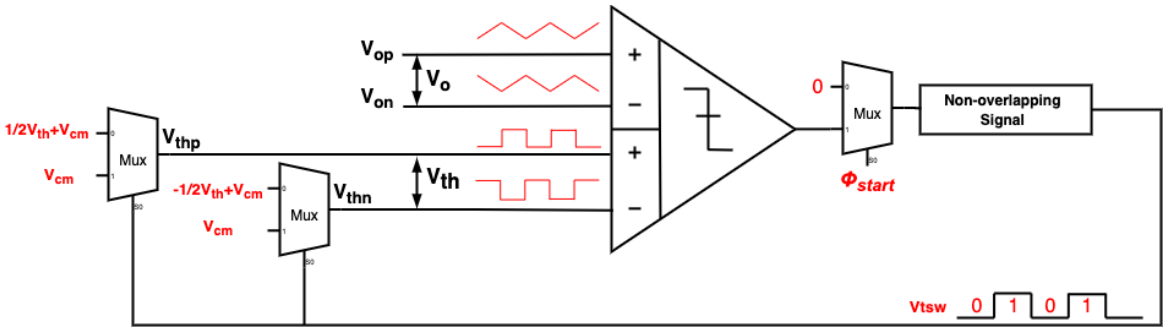


Figure 4.20: Simplified logic of comparator threshold window selection

4.3.2 Comparator Noise

Besides the noise from integrator, the noise from the continuous-time comparator also contributes to the entire noise. The input-referred RMS noise of the comparator is added together with the output-referred RMS noise from the integrator using the equation

$$V_{n,rms}^2 = V_{n,comp,rms}^2 + V_{n,int,rms}^2 \tag{4.6}$$

The RMS noise of the comparator $V_{n,comp,rms}$ is 405 μV. Therefore, the achieved total RMS noise at the integrator can be calculated using equation 4.6. The result is 1.39 mV when gain-code is 12 and 506 μV when gain-code is 0. Compared with the RMS noise determined by the noise requirements, the noise from the simulation is smaller than the noise calculated from equation 3.5 and 3.8 in chapter 3.2.4. The RMS noise requirements are fulfilled.

4.4 Digital Blocks

The digital blocks in the entire readout circuit mainly contain two parts: One for generating a control signal to drive the circuit's analog components: choppers, capacitance array, and threshold window. Another one is used to output the digital count within a given conversion time.

4.4.1 Control Signal Generation

Chapters 4.2.3 and 4.3.1 introduce the selection scheme of feedback capacitance C_f and threshold window V_{thw} for a given gain-code. For threshold window V_{thw}, the window is not fixed but flips between high and low threshold with the frequency synchronized to the chopper switching frequency.

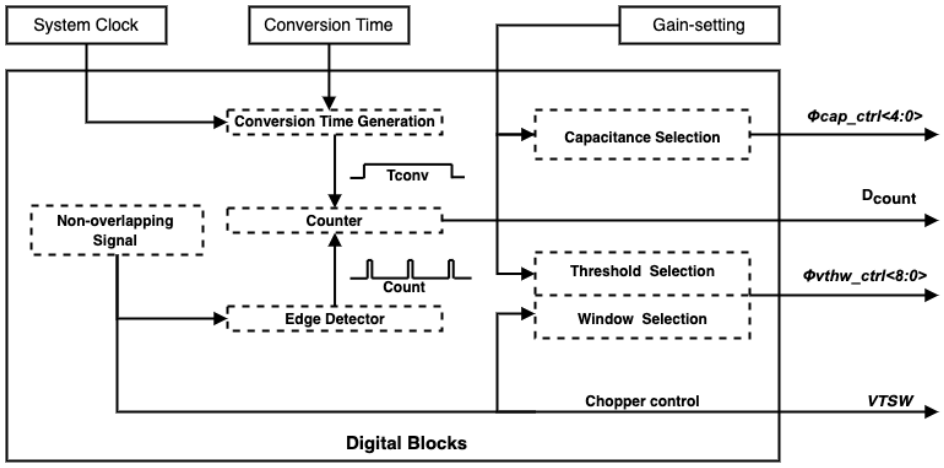


Figure 4.21: Overview of digital blocks

Two choppers in the circuit have the same switching frequency to ensure the negative feedback of the integrator. The chopper switching frequency is obtained at the comparator output. A Schmitt trigger is placed after the comparator output in real circuit design, followed by a non-overlapping signal generation circuit. The former is beneficial for increasing noise immunity near the threshold, and the latter is used to drive the complementary switches. Complementary switches are applied for capacitance array and threshold window selection since the common-mode voltage V_{cm} is half the supply.

4.4.2 Counter

An asynchronous counter is implemented to output counts within a given integration time. First, the chopper control signal is sent to an edge detector; counts are generated on each rising edge. The integration time is calculated by multiplying the integration integer N_{int} with the system clock period T_{clk}. A flag signal T_{int} is only high during the calculated integration period. The count from the edge detector is combined with the flag signal using a AND gate and then sent to the asynchronous counter so that only the counter within the calculated integration period is accumulated.

5 Layout and Post-Simulation Result

5.1 Layout

The PD readout circuit is designed using a TSMC 180*nm* CMOS technology. The layout of the chopper switch is shown in figure 5.1. Four switches are placed close to each to reduce the mismatch, and the layout is symmetrical to balance the parasitic capacitance [10]. As illustrated in chapter 4.2.2, one of the choppers is layout in the deep-n-well to minimize the leakage current. Compared with the normal NMOS, an extra N-well ring is constructed around the P-well to create a deep-n-well layer, thus isolating the source/drain from the substrate [11]. Similarly, this rule is applied to all switches that need to be layout in deep-n-well.

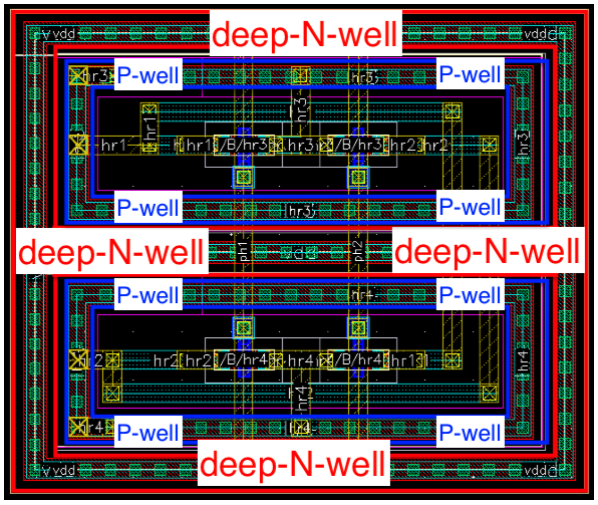


Figure 5.1: Layout of chopper in deep-n-well

The mismatch between transistors also causes errors. In the amplifier and comparator, the mismatch between the input pairs adds to the input-referred offset. Dummy transistors are added at both sides of the input transistors to eliminate the mismatch error. Additionally, the cross-coupling technique is applied to the input transistors from differential branches to provide better matching. The example is given in figure 5.2 where cross-coupling and dummy switch is applied for differential input transistors from the integrator amplifier.

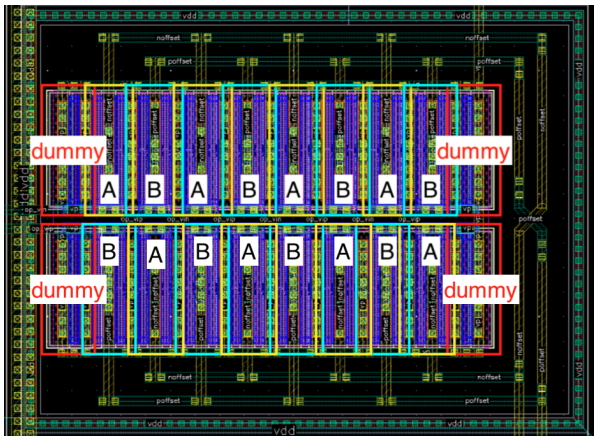


Figure 5.2: Layout of amplifier input pair applying dummy switches and cross-coupling technique

Also, to reduce the mismatch between capacitors, the capacitors from the capacitance array in a fully differential system are placed symmetrically. Figure 5.3 shows the layout of the capacitance array used in a fully-differential integrator. The capacitance occupies a large area compared with transistors. However, they are fabricated in higher layers and can be placed on top of the rest components to save the chip area.

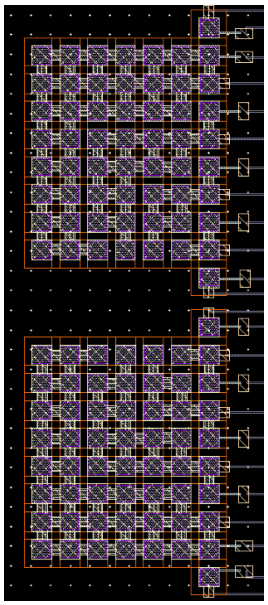


Figure 5.3: Layout of capacitance array

The layout overview of the entire design can be found in figure 5.4. The area occupied by the core circuitry is about 0.28*mm* x 0.2*mm*.

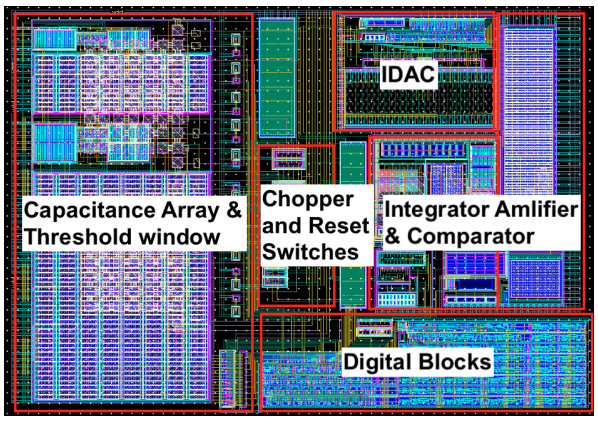


Figure 5.4: Layout of entire design

5.2 Post-Simulation

Several system-level specifications are defined to execute the performance of the designed readout. Post-simulation is implemented to check if the given specifications are met. The post-simulation result is shown in each sub-chapter and summarized to make a fair comparison with the start-of-art current measurement readout.

5.2.1 Performance Specification

The performance specification mainly contains three aspects: dark count, count linearity, and noise count. Detailed requirements for each aspect are described in the table below.

Dark Count	Dark count $<$ 3 counts
Count Linearity	Coefficient of determination (R^2) $>$ 0.99
Noise Count	Count jitter $<$ 1 count when count $<$ 100 Count jitter $<$ 1% count when count $>$ 100

Table 2: Performance Specification

5.2.2 Dark Count

As the name suggests, dark counts are generated by the readout in a dark environment. Namely, no incident light is detected by the PD. The post-simulation mimics the dark environment by setting the input PD current to zero. From the specification table, the maximum dark count within conversion time (100ms) should be less than three counts. In theory, no count should be generated when there is no input current since the PD is zero-biased. However, there are some 'leaky' components like switches existing in the system. The system produces leakage current because of the residue offset from the integrator amplifier after trimming. The leakage current is seen at the output in the form of dark counts. The amount of leakage current is less sensitive to the variation of gain setting. The system produces more count for the same input current in the largest gain setting scenario (gain-code 12). Therefore, the worst case for dark current should be checked when the feedback capacitance and threshold window are smallest.

The result in table 3 presents the dark offset and dark count over PVT. It can be proved that the dark count is less than three, which meets the performance specifications.

Dark Offset				Dark Count			
Temperature	ff corner	ss corner	tt corner	Temperature	ff corner	ss corner	tt corner
-40^{o}C	16.72mV	13.43mV	14.57mV	-40^{o}C	2.122	2.696	1.831
27^{o}C	17.81mV	13.95mV	15.79mV	27^{o}C	2.248	1.74	1.936
85^{o}C	20.11mV	16.26mV	18.11mV	85^{o}C	2.493	1.984	2.215

Table 3: Dark offset and dark current

5.2.3 Count Linearity

For this specification, the count linearity is examined by calculating the coefficient of determination (R^2) which varies from 0 to 1. A larger number of R^2 represents better linear regression of the system model [12]. The formula of R^2 is derived by

$$R^2 = 1 - \frac{SSE}{SST} \tag{5.1}$$

where SSE represents the error sum of squares, and SST represents the total sum of squares.

In post-simulation, four gain settings scenarios are checked, including the largest and smallest gain setting (gain-code 12 and gain-code 0) and two gain settings in between (gain-code 8 and gain-code 4). For each gain setting, the coefficient of determination (R^2) is calculated among its full PD current measurement range. The result from figure 5.5 shows that the coefficient of determination (R^2) is larger than 0.99 in all examined gain settings.

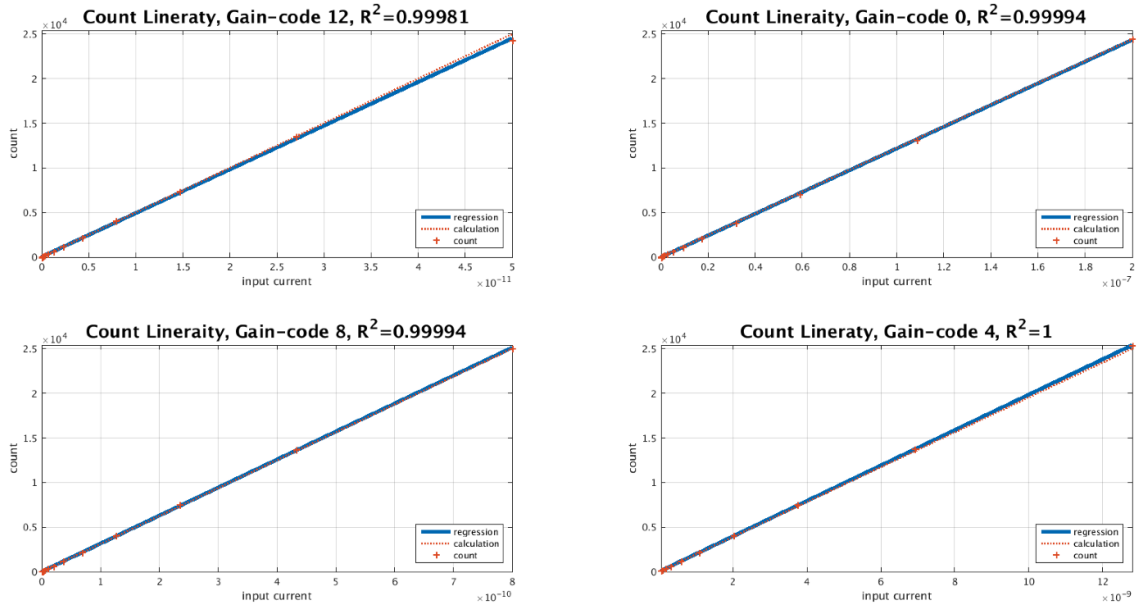


Figure 5.5: Coefficient of Determination (R^2) in different gain settings

5.2.4 Noise Count

The noise specification for the system is based on count values: count jitter $<$ 1 count when count $<$ 100; count jitter $<$ 1% count when count $>$ 100. With the same conversion time (T_{conv} = 100ms) and fixed gain setting, the output counts differ from 1 count with the smallest PD current to 25000 counts with the largest PD current. The largest and smallest gain setting (gain-code 12 and gain-code 0) cases are checked, where several examples of input PD current are given. The expected output count, count mean, and count jitter is calculated and shown in the table below.

Figure 5.6 shows the histogram plot of count for 200fA PD current input at gain-code 12 with transient noise. Table 4 presents more examples with different PD current inputs. For all the examined

cases, noise requirements are fulfilled.

Gain-code	PD current	Expected count	Count mean	Count std	Count Jitter
12	2fA	1	1	0.03	-
	200fA	100	103	0.8	0.78%
	2pA	1000	1006	9	0.89%
	20pA	10000	9650	72	0.74%
0	8.192pA	1	1	0.002	-
	819.2pA	100	97	0.04	0.04%
	8.192nA	1000	974	0.138	0.014%
	81.92nA	10000	9833	1.61	0.016%

Table 4: Count jitter for gain-code 12 and 0

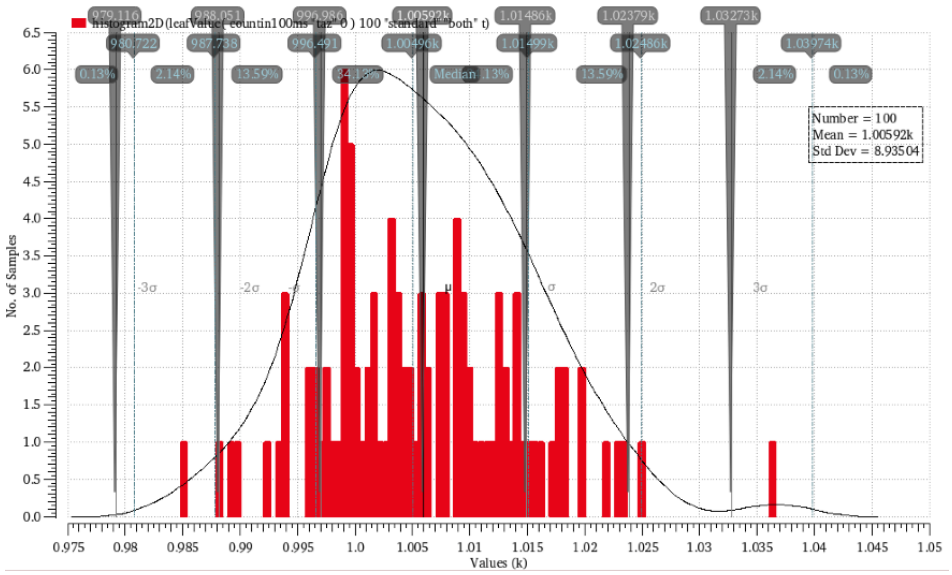


Figure 5.6: Count jitter with transient noise for 200fA PD current when gain-code is 12

5.2.5 Power Consumption

The entire readout consumes a power of $0.113mW$ with 1.8 V power supply when the counter generates most counts within $100ms$ conversion time, namely maximum input PD current is detected.

Detail sub-block level power breakdown can be found in figure 5.7. The analog components consume $0.11mW$, and the on-chip digital only consumes $16nW$. The integrator and comparator are the dominant power contributors.

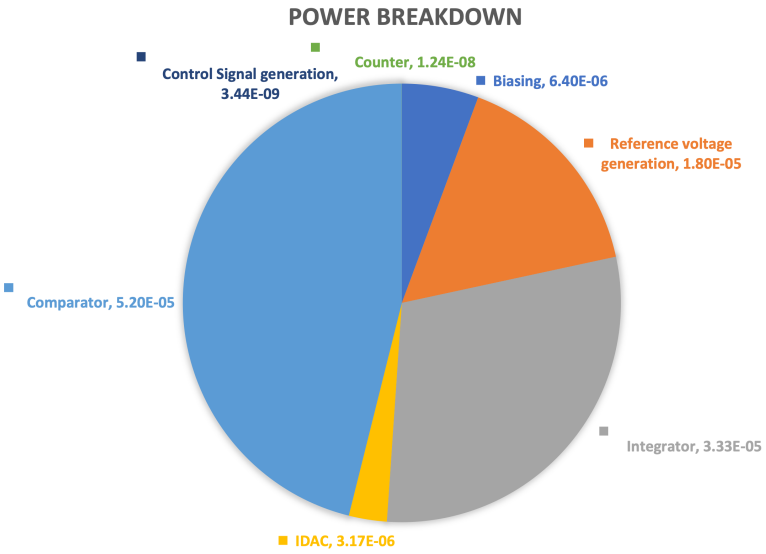


Figure 5.7: Power breakdown

5.3 Performance Summary

The complete performance from the post-simulation result is summarized in table 5 in comparison to a few state-of-art. The achieved dynamic range is $160dB$ with a minimum $2fA$ PD current. The chip area is $0.056mm^2$, and the total power consumption is $0.113mW$. The hourglass ADC is implemented both in this work and work in [4], thus achieving a wide dynamic range of $160dB$. However, the minimum measurement current in this work is the smallest with the value $2fA$, which perfectly fits the application for ambient light sensing. Compared with the work in [4], both chip area and power consumption are smaller in this work. The conversion time is successfully reduced to $100ms$.

	This Work	VLSI19 [3]	ISSCC18 [4]	TBioCAS16 [5]	CICC12 [6]
Architecture	Hourglass ADC	ISD	Hourglass ADC, ISD	C-TIA/I-to-F	I-to-F
Application	Optical	Bio-sensing	Bio-sensing	Bio-sensing	Bio-sensing
Process	180nm	180nm	180nm	180nm	90nm
Input Range	2fA to 200nA	123fA to 1.1μA	100fA to 10μA	123fA to 11.6μA	75fA to 200pA
Dynamic range	160dB	139dB	160dB	155dB	68.5dB
Area	0.056mm^2	0.11mm^2	0.2mm^2	0.091mm^2	0.065mm^2
Power@Supply Voltage	0.113mW@ 1.8V	0.05mW@ 1.8V	0.295mW@ 1.8V	5.22mW@ 1.8V	0.147mW@ 1.8V
Conversion time	100ms	100ms	400ms	5ms	250us
Input-referred Noise	0.63 fA/$\sqrt{Hz}$	30.3 fA/$\sqrt{Hz}$	58.9 fA/$\sqrt{Hz}$	20.4 fA/$\sqrt{Hz}$	0.235 fA/$\sqrt{Hz}$

Table 5: Performance summary

6 Conclusion and Future Work

6.1 Conclusion

This thesis presents theory analysis and circuit implementation for a wide dynamic-range and low-power current-mode optical sensor readout. Hourglass ADC structure can used in differential PD readout because of its wide measurement range [4]. To meet the design target, the hourglass ADC structure is chosen where the design of the chopper, threshold window, and feedback capacitance is considered to increase the measurement range further. The achieving PD measurement dynamic range is $160dB$ for the proposed architecture utilizing the ultra-low $2fA$ current measurement. The consumed power and chip area of the readout circuit in this thesis is $0.113mW$ and 0.056mm^2, making it competitive to the design in [4] that also implements hourglass ADC and some prior-of-art current-mode readout circuits.

6.2 Future Work

Since the layout work for this design has been finished, the next step would be taping out and implementing the quality test. Regarding the architecture, the possible improvement for this design would be further increasing the dynamic range. The readout in this thesis is designed for current measurement, which suits the application of ambient light measurement.

However, PD produces a larger current signal when the artificial light sources are applied along with the ambient light. The choice of ADC hourglass structure helps extend the dynamic range for the readout circuit, but the power budget limits the maximum detectable current. Therefore, if still consider using the hourglass ADC structure, a feedback loop can be added to the system. The feedback path can be either a DC compensation loop [13],[14] or a predictive current DAC [4], which helps process the significant parts of the input signal. Furthermore, the feedback path is only enabled when a large PD current is detected and is disabled when ambient light is detected. The dynamic measurement range is extended further since the feedback path compensates for a large PD current, and the power is effectively saved since the compensation is not activated all the time.

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