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On the Transient of DC Fault Current Interruption for Evaluating HVDC Cable Performance

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Abstract

This paper presents an analytical framework for understanding DC fault current interruption dynamics using fundamental electrical circuit principles. It examines the interruption mechanisms of a DC circuit breaker with a detailed HVDC cable model through Electromagnetic Transient (EMT) simulations. The research integrates analytical and numerical simulation approaches during fault conditions to assess varying parameters for the impact of DC fault current interruption on estimating the resulting cable stresses. This research aims to advance HVDC transmission technology by providing a comprehensive understanding of DC fault current interruption dynamics of cable-based networks.

1 Introduction

The rising demand for HVDC networks, driven by their efficiency in long-distance power transmission and the shift towards carbon-neutral energy supply, is evident in the implementation of $\pm 525~kV$ HVDC interconnections with 2 GW capacity in Germany. These interconnections are necessary for developing robust onshore and offshore multiterminal (MT) HVDC networks [1]. Ensuring the reliability of MT-HVDC grids necessitates rigorous quality assurance of system components.

In HVDC networks, DC-side short circuit current interruption typically involves blocking converters via valve firing control in thyristor-based LCC HVDC networks or tripping the converter transformer in half-bridge VSC HVDC networks with an AC circuit breaker. Without fault separation devices, such as DC Circuit Breaker (DCCB), the overvoltage on HVDC cables is limited. However, the operational constraints arise, impeding MT-HVDC hub development. DCCBs are crucial for rapid fault interruption in MT-HVDC hubs, which experience faster voltage decay and higher fault currents due to lower DC-side system impedance and multiple fault-feeding sources. Effective DC current interruption is essential for managing increased fault currents and transient voltages, highlighting the need for DCCBs to isolate promptly faulty cable sections. Despite being preferred, especially for offshore HVDC networks, the transient cable stresses in MT-HVDC hubs with DCCBs remain underexplored, leaving a notable knowledge gap.

Significant progress has been made in deploying DCCBs, particularly within MT-HVDC hubs [2][3]. While previous studies have examined DC fault current interruption dynamics at system levels [4], they often overlooked the interface between HVDC cables and DCCBs and the impact on cables. This paper focuses on analysing cable transients during DC fault current interruption, laying the groundwork for understanding the complex interactions and performance of HVDC cables with DCCBs.

In this contribution Section 2 describes the structure and key components of an Active Current Injection (ACI) based mechanical DCCB, emphasizing its role in DC fault current interruption by detailing its sequential operation stages: initial current injection, the main current interruption, and the final energy dissipation [5]. Section 3 provides an analytical framework, based on transient phenomena to explain the interaction between DCCBs and cables during DC fault current interruption, by considering the magnetic energy stored by the surge arrester (SA) during DC current suppression stage. Section 4 extends this analysis with transient simulations under fault conditions in a ±525 kV simplified network model, based on [6] to assess cable stresses. It also includes a sensitivity analysis of SA energy absorption characteristics, comparing 20 km and 200 km HVDC cable lengths in an EMT environment, excluding the effects of grounded joints along the cable route.

2 DC Circuit Breakers for Fault Current Interruption

2.1 General Topology

The general topology of the DCCB, which is a crucial component for interrupting DC faults in MT-HVDC hubs, is designed to handle high DC current flows during faults. To achieve rapid isolation of faulty sections, as illustrated in Figure 1, typically three functional paths are essential: the Rated Current Path (RCP), Current Commutation Path (CCP), and the Energy Absorption Path (EAP), as shown for an ACI-based mechanical DCCB.

The RCP, which is the main branch with a low resistance to minimize conduction losses, includes a mechanical switch, such as a Vacuum Interrupter (VI) that can operate under load. Additionally, the RCP comprises a Residual Current Breaker (RCB) with lower current interrupting capability, primarily to isolate the DCCB following a successful current interruption. In case of a fault, DC current, I_{dc} , is diverted, and commutated, into the CCP, allowing the VI in the RCP to initiate and complete the separation of its contacts. Consequent to this commutation action, a counteracting voltage in the CCP is generated, exceeding

the system DC voltage, U_S , that further diverts the I_{dc} into the EAP, thereby reducing the fault current. The EAP includes an SA to de-energize system inductances. Ultimately, the RCB opens to isolate the leakage current in the SA, protecting it from long-term damage.

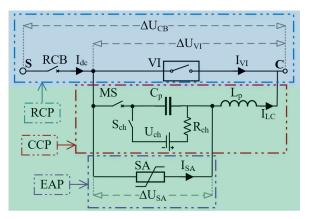


Figure 1 Structure of an ACI-based mechanical DCCB illustrating its functional paths, and components

The CCP consists of an auxiliary circuit, typically comprising a capacitor C_p , and an inductor L_p , connected in parallel with RCP. The C_p has its charging circuit with a charging switch S_{ch} , a charging resistor R_{ch} , and a DC source U_{ch} , which represents the system voltage U_S . Upon triggering the Making Switch (MS), pre-charged C_p injects an auxiliary current I_{LC} , into the circuit to create a current zerocrossing point, facilitating the neutralisation of I_{dc} in the VI. L_p and C_p determine the frequency and peak value of I_{LC} . The EAP defines and maintains the required Transient Interruption Voltage (TIV) amplitude across the VI, thereby absorbing energy. As shown in Figure 1, the EAP is connected in parallel to C_p alone and not to the entire L_p and C_p branch [5], [7]. This configuration prevents current commutation from L_p during current suppression, avoiding superimposed high-frequency oscillations on the TIV and I_{LC} .

2.2 Operation Stages

Each functional path (see Figure 1) corresponds to a specific operation stage in a DCCB. The mapping of each path to its role in these stages defines the functional properties of the DCCB (see Table 1). The fault detection already begins in the neutralisation stage with the ultimate goal of creating a local Current Zero (CZ) inside the VI by fully separating its contacts to reach its full dielectric strength. Accordingly, the DC current is interrupted and consequently commutated into the EAP. A counteracting voltage TIV is generated once CZ is created and DC current commutation is successful. The amplitude of TIV must exceed the U_S , by at least 1.5 times to effectively suppress the DC current [4]. The TIV is generated across C_p and consequently applied across VI due to their parallel arrangement. Figure 2 depicts the operating principle of an ACI-based mechanical DCCB. It correlates the RCP, CCP, and EAP to various operation stages, using an analogous colour scheme between Figure 1 and Figure 2.

Table 1 Mapping of functional paths to DCCB operation stages

Operation Stages (see Figure 2)	Functional Paths	Role
Neutralisation (Duration: t _{f,N})	RCP	Local DC current zero creation
Suppression (Duration: t _{f,S})	ССР	Generate TIV and maintain its amplitude at a higher than DC system voltage level
Energy Dissipation (Duration: t ₅ -t ₄)	EAP	Dissipate magnetic energy in system inductances

During the pre-fault period, the C_p is charged to the system voltage by U_{ch} . At fault instant t_I , the pre-fault DC load current I_0 , begins to increase with an initial rate of rise given by dI'_{dc}/dt . The inductance value L_{CLR} of the Current Limiting Reactor (CLR) defines this rate of rise of DC current. The L_{CLR} is typically connected in series with the DCCB (see Figure 3). The corresponding duration t_d (= t_2 – t_I) depends on the fault detection algorithm, and its consideration is beyond the scope of the analysis presented in this paper. Within this time t_d , a trip command is sent to the DCCB. Thereafter, during t_{act} (= t_3 – t_2), the moving contact of the VI starts separating, resulting in arcing inside the VI and reaching dielectric withstand capability at t_3 .

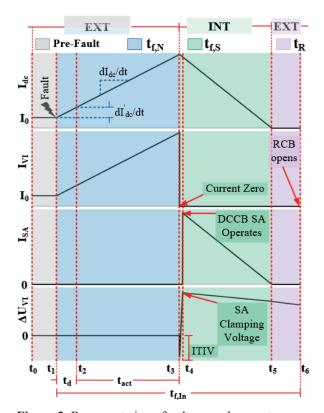


Figure 2 Representation of voltage and current waveforms in ACI-based mechanical DCCB

At t_3 , the VI contacts have adequately separated to withstand the TIV. The MS closes, causing zero crossings in the VI, which eventually stops conducting and diverts the DC fault current to the CCP. Since the VI is parallel to this branch, the voltage across it at t_3 equals the Initial Transient

Interruption Voltage (ITIV) of the capacitor. Within the instant $t_4 - t_3$, the fault current charges the C_p until its voltage reaches the SA clamping voltage at t_4 . The fault current is then diverted to the energy absorption branch, and the SA remains latched until the current drops to zero at t_5 . After the DCCB has successfully interrupted the DC current, the leakage current may persist due to low-frequency interactions between the C_p and L_{CLR} . The RCB opens at t_6 to clear the leakage current and isolate the main breaker circuit terminals "S" (Source side) and "C" (Cable side), shown in Figure 3, from the grid. The duration of $t_{f,ln}$ is the overall DC fault current interruption stage.

3 Analysis of Fault Current Interruption Dynamics

The topology of ACI-based mechanical DCCB (see Figure 1) is now implemented in a simple DC network, by adapting to the approach described in [5]. The two terminal nodes of the DCCB are illustrated in Figure 3 as "S" at the DC source side, and "C" at cable side of the single DC pole, analogous to the terminal nodes in Figure 1. Such a simplified network, adapted from [6], facilitates a fundamental analysis based on the circuit theory laws to understand the electrical behaviour of network components. At terminal "S" of the DCCB, a CLR with an inductance L_{CLR} is connected on the source, U_S , side, which is defined at a voltage value of 525 kV along with its impedance R_{dc} of 0.1 Ω for fast transient analysis. The DC bus voltage U_{DC} , is the terminal voltage to ground at the L_{CLR} . DCCB terminal voltages to ground are denoted by U_{CLR} on the "S" side and U_{cT} on the "C" side. It is noteworthy that U_{cT} defines the interface stress on HVDC cables due to DCCB operation. The voltage drop across each component in the network (see Figure 3) is denoted by " Δ ". R_f represents the fault resistance to ground at the cable's remote end. In the simulations, a bolted ground fault has been applied, resulting in a fault current I_{cf} at the cable's remote terminal, where the fault occurs.

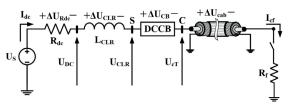


Figure 3 Simplified circuit diagram for evaluating the transient voltages due to DCCB operation [6]

3.1 Transient Instants in DC Current Interruption

During normal operation denoted as $t(0^-)$ (see Table 2), the time interval t_1-t_0 (see Figure 2) represents the period for which the circuit achieves a steady-state condition following the initial application of the DC voltage. Due to its electrical inertia, the L_{CLR} prevents the occurrence of a sudden change of I_{dc} . Accordingly, there will be an exponential increase in I_{dc} as shown by (1) contributing to charging the L_{CLR} with a time constant, τ , defined by the ratio of L_{CLR} to R_{dc} .

$$I_{dc}^{(0)-} = \frac{U_S}{R_{dc}} [1 - e^{-t/\tau}]$$
 (1)

Table 2 Overview of transient instants relative to fault occurrence for DCCB operation analysis

Transient Instants	Description	Context
t(0-)	A priori to fault	State of the network before the fault
t(0)	At the fault	Precise moment of fault inception and DC current rise (no DCCB trigger).
$t(0^+)$	A posteriori to fault	State of the network upon commutation and short circuit DC current opening

The voltage developed across different components is expressed by (2) through (5):

$$\Delta U_{Rdc}^{(0)-} = I_{dc}^{(0)-} R_{dc} = U_{S} (1 - e^{-t/\tau})$$
 (2)

$$\Delta U_{CLR}^{(0)-} = L_{CLR} \frac{d}{dt} (I_{dc}^{(0)-}) = U_{DC}^{(0)-} (e^{-t/\tau})$$
 (3)

$$\Delta U_{cab}^{(0)-} = R_{cab} I_{dc}^{(0)-}$$
 (4)

$$\Delta U_{CR}^{(0)^{-}} \cong 0 \tag{5}$$

 R_{cab} is the cable's core conductor resistance (not included in Figure 3). The voltage transient across R_{dc} exponentially rises while that across the L_{CLR} exponentially decays. The DC bus voltage, U_{DC} , and terminal voltage to ground at the HVDC cable, U_{cT} , are given by (6) and (7).

$$U_{DC}^{(0)-} = U_S - \Delta U_{Rdc}^{(0)-}$$
 (6)

$$U_{cT}^{(0)-} = U_{S} - \Delta U_{Rdc}^{(0)-} - \Delta U_{CLR}^{(0)-} = U_{DC} (1 - e^{-t/\tau})$$
 (7)

 U_{cT} , as per (7), increases exponentially. Eventually the transient state decays establishing the natural response of the network with a steady-state current $I_{dc}^{(0)}$ for a negligible ΔU_{CLR} . Thereafter, for the transient instant of t(0), as per Table 2, the fault is incepted at t_1 (see Figure 2). Equation (5) is valid until the DCCB operates upon receiving the trip command at t_2 . However, $I_{dc}^{(0)}$ continues to increase and accordingly, L_{CLR} opposes its rate of rise. Equation (1) is valid since there is no actual separation of the fault current yet, hence it continues to increase. The corresponding voltage drop across R_{dc} and L_{CLR} are expressed by (8) and (9):

$$\Delta U_{Rdc}^{(0)} = U_S \left(e^{-t/\tau} \right) \tag{8}$$

$$\Delta U_{\rm CLR}^{(0)} = L_{\rm CLR} \frac{d}{dt} (I_{\rm dc}^{(0)}) = U_{\rm DC}^{(0)} e^{-t/\tau}$$
 (9)

At t(0), $U_{cT}^{(0)}$ equals $\Delta U_{cab}^{(0)}$ since the DCCB has not yet reached the suppression stage. Accordingly, (5) remains valid. The voltage division rule gives (10) and by equating (11) and (12) we obtain (13)

$$\Delta U_{CLR}^{(0)} = U_{DC}^{(0)} \left[\frac{L_{CLR}}{L_{CLR} + Z_{cab}} \right]$$
 (10)

$$\Delta U_{cab}^{(0)} = U_{DC}^{(0)} \left[\frac{Z_{cab}}{L_{CLR} + Z_{cab}} \right]$$
 (11)

$$\Delta U_{cab}^{(0)} = U_{DC}^{(0)} - \Delta U_{CLR}^{(0)}$$
 (12)

$$U_{DC}^{(0)} \left[\frac{Z_{cab}}{L_{CLR} + Z_{cab}} \right] = U_{DC}^{(0)} - \Delta U_{CLR}^{(0)}$$
 (13)

Substituting (9) in (13):

$$U_{DC}^{(0)} \left[\frac{Z_{cab}}{L_{CLR} + Z_{cab}} \right] = U_{DC}^{(0)} - \left[U_{DC}^{(0)} e^{-t/\tau} \right]$$
 (14)

$$Z_{cab} = (L_{CLR} + Z_{cab}) (1 - e^{-t/\tau})$$
 (15)

$$\frac{Z_{\text{cab}}}{L_{\text{CLP}}} = \frac{\left(1 - e^{-t/\tau}\right)}{e^{-t/\tau}} \tag{16}$$

Equation (16) provides the relation between cable impedance, Z_{cab} and CLR having an inductance value of L_{CLR} once the fault has been incepted. Thereafter, the DC fault current detection requires the determination of an incremental current, di, which is the difference between the maximum permissible short circuit current, I_{sc} , and $I_{dc}^{(0)}$. After a certain time delay, t_d (see Figure 2) the relay will provide a trip command to enable the operation of DCCB. Accordingly, U_{DC} is written as per (17):

$$U_{DC}^{(0)} = (Z_{cab} + L_{CLR}) \frac{d(I_{dc}^{(0)})}{dt}$$
 (17)

Once the short circuit current begins increasing with a defined gradient (during $t_3 - t_1$, as shown in Figure 2), the Z_{cab} becomes irrelevant as the breakdown streamer has fully bridged the cable insulation thickness, rendering the cable impedance ineffective in influencing the fault current. Hence, (17) can be re-written and re-arranged to correlate the L_{CLR} to the di during t_d as seen in (18).

$$L_{CLR} = \frac{U_{DC}^{(0)} \cdot (t_d)}{I_{sc} - I_{dc}^{(0)}}$$
 (18)

According to (18), t_d dictates the sizing of the L_{CLR} for a permissible I_{sc} from the instant of fault inception, at t_l until the protection is activated at t_2 . This means larger values of L_{CLR} will increase t_d and accordingly delay the detection of the maximum di for a defined I_{sc} to activate the protection and initiate the DCCB operation. To calculate the fault current over time, the dynamic behaviour of the circuit must be considered. Equation (1) remains valid for implementing (18), as illustrated in Figure 4, where for the duration t_d , the short circuit current, I_{sc} , rises in the event of a fault at the rate of change given by $dI_{dc}^{(0)}/dt$, which in turn is dependent on L_{CLR} .

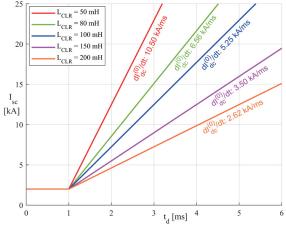


Figure 4 Impact of varying L_{CLR} on the rate of rise of short circuit current, I_{sc}

Once the VI has its contacts fully separated, the fault current commutates into the CCP. Accordingly, $I_{dc}^{(0)+}$ will exponentially decay as seen in (19).

$$I_{dc}^{(0)^{+}} = \frac{U_{S}}{R_{dc}} (e^{-t/\tau})$$
 (19)

After VI contact opening and commutation occurs, the voltage drop across DCCB, ΔU_{CB} (see Figure 3) is determined by the residual voltage ΔU_{SA} of the SA, which is connected in parallel to the C_p of the CCP (see Figure 1). The DC current behaviour upon commutation shows the effect of SA on the current interruption process.

$$\frac{d(I_{dc}^{(0)^{+}})}{dt} = \frac{U_{DC}^{(0)^{+}} - \Delta U_{CLR}^{(0)^{+}} - \Delta U_{SA}^{(0)^{+}}}{Z_{cab} + L_{CLR}}$$
(20)

To ensure successful DC current interruption, the rate of change of $I_{dc}^{(0)+}$ must be negative. Accordingly, $\Delta U_{SA}^{(0)+}$ must be greater than $U_{DC}^{(0)+}$, as per (20), to allow for a decrease in the value of $I_{dc}^{(0)+}$. Consequently, the requirement, as seen in (21) must be satisfied:

$$\frac{d(I_{dc}^{(0)^{+}})}{dt} < 0 \quad \text{for} \quad \Delta U_{SA}^{(0)^{+}} > U_{DC}^{(0)^{+}}$$
 (21)

During DCCB operation, a rapid decrease in DC current, $I_{dc}^{(0)+}$ induces a time-varying flux linkage, which results in cable overvoltage. This overvoltage is the TIV. From (20), it can be seen that the TIV, necessary for a negative rate of rise of $I_{dc}^{(0)+}$, is equal to $\Delta U_{SA}^{(0)+}$. Consequently, higher protective level of the SA would be necessary to withstand higher TIV peak. The TIV inversely relates to fault clearing times. This means, the slope of $I_{dc}^{(0)+}$ will depend on the voltage generated across DCCB i.e., $\Delta U_{SA}^{(0)+}$. The higher the $\Delta U_{SA}^{(0)+}$, the higher will be the rate of rise of negative current, i.e., the current will decay faster. To completely nullify $I_{dc}^{(0)+}$, DCCB must generate a TIV surpassing the system voltage, stressing both the cable and CLR (i.e., $Z_{cab} + L_{CLR}$, as seen in (20)) with a negative polarity voltage in reference to the system voltage.

3.2 Magnetic Energy and TIV Withstand Voltage

The decreasing DC current during the suppression stage of the DCCB operation has an associated time varying magnetic field which induces negative DC voltage in cables. Consequently, a large amount of energy is absorbed by the SA. Alongside, the magnetic energy stored in the L_{CLR} is:

$$E_{CLR} = \frac{1}{2} \cdot L_{CLR} \cdot \left(I_{dc}^{(0)^{+}} \right)^{2}$$
 (22)

Under the condition of a simplified single DC pole network, as illustrated in Figure 3, the DC voltage source continues to supply during the suppression stage. This resembles the non-blocking of converters, however missing any voltage droop effects. Consequently, a continued DC voltage infeed is ensured during the overall fault interruption stage, $t_{f,In}$. The energy supply, E_{DC} , at the DC bus, with a voltage U_{DC} can be expressed by (23):

$$E_{DC} = \frac{1}{2} \cdot L_{CLR} \cdot \left(I_{dc}^{(0)^{+}} \right)^{2} \cdot \left(\frac{\Delta U_{CLR}}{\Delta U_{CB} - \Delta U_{CLR}} \right)$$
(23)

The DCCB must dissipate the total energy, E_{CB} , as expressed by (24). This corresponds to the energy, E_{SA} , absorbed by the SA within the EAP of the DCCB during the energy discharge process that occurs during the fault suppression period, $t_{f,S}$ (as explained in Figure 2). It is defined from the instant when TIV occurs at the SA terminals, t_4 , to the end of the suppression period, t_5 , as expressed by (25).

$$E_{CB} = \frac{1}{2} \cdot L_{CLR} \cdot \left(I_{dc}^{(0)^{+}} \right)^{2} \cdot \left[1 + \left(\frac{\Delta U_{CLR}}{\Delta U_{CR} - \Delta U_{CLR}} \right) \right]$$
(24)

$$E_{SA} = \int_{t_4}^{t_5} [\Delta U_{SA}(t)] \cdot I_{SA}(t) dt = [u_k] \int_{t_4}^{t_5} I_{SA} dt \qquad (25)$$

where, $u_k = k \cdot U_{DC}$ is the threshold voltage before the SA starts conducting to clamp the TIV to the permissible level. The non-linear characteristics of the SA shows that a constant k-factor results in higher energy than that determined by simulation. The integral function of I_{SA} in (25) determines the area under the SA current I_{SA} , which is dissipated and it can be expressed by (26). The energy absorbed by SA has a direct relation with its total current, which is estimated as the maximum fault current, $I_{dc}^{(0)+}$

$$E_{SA} = (k \cdot U_{DC}) \left\{ \left[I_{dc}^{(0)^{+}} (t_5 - t_4) \right] + \frac{(1 - k)U_{DC}}{L_{CLR}} \int_{t_4}^{t_5} t \, dt \right\}$$
 (26)

$$E_{SA} = (k \cdot U_{DC} \cdot \Delta t) \left\{ I_{dc}^{(0)^{+}} + \left[\frac{(1-k)U_{DC}}{L_{CLR}} \left(\frac{t_4 + t_5}{2} \right) \right] \right\}$$
 (27)

In terms of energy balance, the energy absorbed by the SA equals the residual energy in the system. Upon operation, the SA absorbs an amount of energy equivalent to what is dissipated from the system, effectively removing it from the external network. Accordingly, (27) can be equated to

(24), to mathematically derive the relation, as seen in (28), for the DC current $I_{dc}^{(0)+}$.

$$I_{dc}^{(0)^{+}} = \left\{ \left[\frac{1}{2} \frac{L_{CLR} \left(I_{dc}^{(0)^{+}} \right)^{2}}{\left(k U_{DC}^{(0)^{+}} \Delta t \right)} \right] \left[1 + \frac{\Delta U_{CLR}^{(0)^{+}}}{\left(\Delta U_{CB}^{(0)^{+}} - \Delta U_{CLR}^{(0)^{+}} \right)} \right] \right\}$$

$$- \left\{ (1 - k) \frac{U_{DC}^{(0)^{+}}}{L_{CLR}} \frac{(t_{4} + t_{5})}{2} \right\}$$
(28)

4 Results and Discussion

The DC fault current interruption involves detection, decision-making and DCCB operational stages. The SA Protective Level (SAPL) limits the overvoltage magnitude and duration during these stages. Inadequate SAPL may prolong the fault clearing times necessitating additional protection measures or restrikes in circuit breaker operation. While the relationship between SAPL and fault clearing time is complex, higher SAPL generally facilitates faster and more reliable fault clearing by effectively suppressing overvoltage and reducing breaker failure risks. Figure 5 depicts three SA characteristics used for simulating transient stresses in DCCBs and HVDC cables.

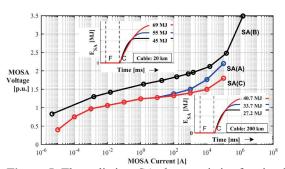


Figure 5 Three distinct SA characteristics for simulating transient stresses on DCCB and HVDC cables

Figure 6a shows the variation of I_{SA} and SA voltage, U_{SA} , over time, starting at fault inception ("F") and transitioning to the fault suppression period at "C" after successful fault neutralization. It can be observed that "SA(C)" which clamps the overvoltage at a lower level, conducts for a relatively longer time to discharge a larger current (as shown in Figure 6a) and accordingly absorbs larger energy (seen in Figure 5). Conversely, the response of SA(B) which allows a higher TIV to be generated, facilitates a faster current decay and hence a lower energy absorption in EAP. Figure 6 presents the results based on the aggregated model of the ACI-based mechanical DCCB (as seen in Figure 1). The results consist of four distinct plots, each highlighting critical interactions and associated current and voltage stresses. Figures 6a and 6c show the dynamic interaction between I_{SA} and U_{SA} (as per Figure 1 and Figure 2) for 20 km and 200 km HVDC cables, respectively. Figures 6b and 6d depict the HVDC cable stresses (as per Figure 3) during DCCB operation when clearing a far-end fault in 20 km and 200 km cables. The cable stresses correspond directly to the respective SA characteristics (as per Figure 5). It is evident that from fault inception time at "F" until the fault suppression period begins at "C", i.e., from instant t_3 to t_1 (see Figure 2), SA does not contribute to cable stresses. The impact of the SA on cable stresses is clear during the suppression period. SA(B) produces higher opposite peaks at the cable terminal, generating higher TIV within the DCCB to quickly suppress fault current. In contrast, SA(C) results in lower TIV and reduced oscillations at the cable terminals. For shorter cable lengths, a subtle impact is seen due to SA characteristics (see Figure 6b), whose impact increases for longer lengths (see Figure 6d).

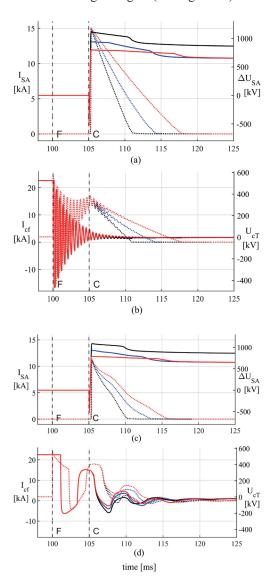


Figure 6 Dynamic interaction of I_{SA} and ΔU_{SA} for: (a) 20 km and (c) 200 km 525 kV HVDC cable; and HVDC cable current (I_{cf}) and voltage (U_{cT}) transients during DCCB operation clearing a far-end fault in: (b) 20 km and (d) 200 km 525 kV HVDC cables. Current transients and voltage stresses are depicted analogous to SA characteristic colour codes using dotted and solid lines, respectively.

The traveling wave phenomena cause superimposed current and voltage oscillations with relatively higher frequencies for faults closer to the DCCB/cable interface. Steeper changes occur in $dI_{dc}^{(0)^+}/dt$ for shorter fault distances, which does not significantly affect the TIV amplitude. The

level of TIV is maintained relatively longer for faults closer to the DCCB/cable interface. This comprehensive assessment of the SA performance to influence the oscillatory stresses of polarity reversing characteristics at cable terminals validates (20) and (21). The presented results are based on a cable-only network without grounded joints, which shall result in more complex reflection phenomena.

5 Conclusion

This paper presents an analytical framework to understand DC fault current interruption dynamics based on the electrical circuit principles. It examines ACI-based mechanical DCCB interruption mechanisms, and 525 kV HVDC cables through transient simulations in a simplified network.. The study integrates analytical and simulation approaches to evaluate SA performance during fault to define transient stresses on HVDC cables. It highlights dynamic currentvoltage interactions and quantifies energy dissipation at the DCCB-HVDC cable interface, emphasizing the need to balance DCCB functionality with cable stresses. This research aims to advance HVDC transmission technology by offering fundamental insights into DC fault current interruption dynamics in cable-based HVDC networks. Being tailored to CIGRE's investigations [6], it stimulates further scientific inquiry into DCCB and HVDC Cable interactions to improve quality control and ensure the reliability and performance of HVDC cable systems for sustainable MT-HVDC hub deployment.

6 Literature

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