An Energy-Efficient Readout Method for Piezoresistive Differential Pressure Sensors

Jiang, Hui; Makinwa, Kofi A.A.; Nihitanov, Stoyan

DOI
10.1109/IECON.2017.8216736

Publication date
2017

Document Version
Final published version

Published in
Proceedings IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society

An Energy-Efficient Readout Method for Piezoresistive Differential Pressure Sensors

Hui Jiang, Kofi A. A. Makinwa, and Stoyan Nihitanov
Electronic Instrumentation Laboratory
Delft University of Technology, The Netherlands

***Abstract*— This paper describes a low power and low noise circuit for resistive Wheatstone bridge sensor readout. The proposed readout exploits the bridge configuration of the sensor by embedding it into a second-order continuous-time sigma delta modulator (RC CTΔΣM). By directly digitizing the output signal of a Wheatstone bridge in the current mode, the noise performance is dominated by the operational transconductance amplifier (OTA) in the first integrator. The proposed readout is designed in a 0.35 µm CMOS technology. Simulation results show that it achieves an input referred noise power spectral density (PSD) of 4.2 nV/√Hz with a current consumption of 860 µA from a 5 V voltage supply. This represents a noise efficiency factor (NEF) of 4.7.**

Keywords*— *Wheatstone bridge; Energy-efficient; Low noise power density; Continuous time sigma delta modulator.

I. Introduction

Thanks to simplicity and low manufacturing cost, resistive sensors are commonly embedded in Wheatstone bridges for many industial applications, e.g., to monitor pressure, humidity and temperature [1-3]. Fig. 1 shows an example of a MEMS piezoresistive differential pressure (MPDP) sensor, which senses pressure by measuring the deflection of a silicon membrane with high piezoresistivity [4]. With four piezoresistors connected in a full Wheatstone bridge, the sensitivity can be quadrupled.

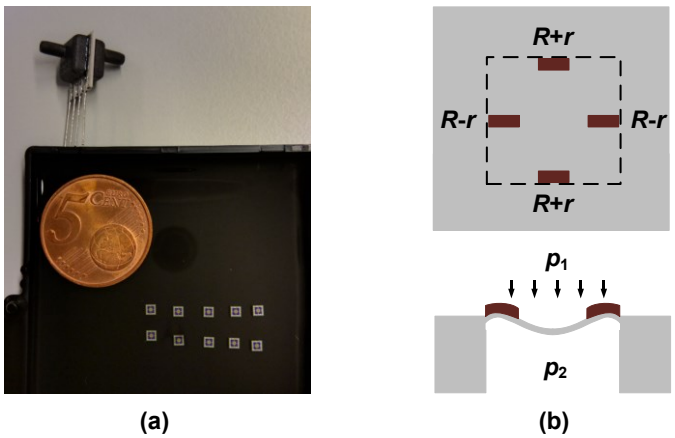

Fig. 1. MEMS piezoresistive differential pressure sensor (a); Piezoresistors that can be used in a full Wheatstone bridge configuration (b).

Conventional readout methods of bridge sensors consist of two main parts: instrumentation amplifiers (IAs) and analog to digital converters (ADCs) as shown in Fig. 2(a). An IA is typically designed with high input impedance and a large gain to boost the signal amplitude of the sensor's outputs (typically several mV) and drive the succeeding ADC stage, which converts the results into digital words. This results in a readout IC which involves two feedback loops with an overall open loop gain far exceeding the necessary closed loop gain. In addition to complexity [3, 5], such readouts have lower power efficiency. To address these issues, an alternative readout topology was proposed, as shown in Fig. 2(b). It embeds the IA into the ADC in one closed loop to improve energy efficiency and reduce complexity [6, 7]. In this architecture, two feedback loops are simplified into one loop by means of an indirect current feedback network. The high input impedance of the readout ICs is realized by using Gm-C integrators. However, additional design effort is needed to accommodate the poor linearity of the Gm-C integrators. This results in a large area or extra complexity.

Alternatively, bridge sensor can be read in current mode. In the design reported in [8], the bridge sensor is embedded into the first RC integrator of a continuous-time sigma delta (CTΣΔ) modulator. The output signals of the Wheatstone bridge are directly digitized in the current mode. However, the resolution of readout is limited by its 1/*f* noise. Consequently, it has a relatively low energy-efficiency.

In this paper, we describe a readout IC based on second order feedforward CTΣΔ with better performance compared to the prior art in terms of noise, power dissipation and design simplicity. The principle and topology are studied on high energy-efficient readout for bridge sensor. Moreover, the chopping technique is utilized to reduce the readout's 1/*f* noise and offset without fold-back of quantization noise to the signal band. Compared to state-of-the-art readout ICs for Wheatstone bridges [1, 3, 5-8], the proposed solution achieves a lower input referred noise PSD with higher power efficiency.

The rest of the paper is organized as follows. Background knowledge on and the principle of the proposed low power readout IC will be discussed in Section II. Section III discusses the implementation details of the proposed readout IC. The performance of the proposed readout IC is then verified with a simulation result in Section IV. The paper and the conclusions are drawn in Section V.

978-1-5386-1127-2/17/$31.00 ©2017 IEEE

II. Current Mode Operation Principle

Bridge sensors are usually read out in the voltage mode, which can, ideally, provide the best linearity performance. The output, V_{out}, of the Wheatstone bridge can be defined as

$$V_{out} = \frac{Vdd \times r}{R}, \quad (1)$$

where R is the bridge resistance and r is varying resistance. However, as shown in Fig. 2(a), two amplifiers A1 and A2 in a three-opamp IA are normally located close to the bridge sensors in the signal chain to provide high input impedance [3]. These two amplifiers usually dominate the noise contribution of the readout. To obtain better noise performance, more power needs to be consumed by these two amplifiers, which consequently increases the power consumption of the readout. The same statement is valid for indirect current-feedback IAs (CFIAs), since the input and the feedback Gm stages are the main noise sources of the readout [5]. In the single closed loop readout solution, as shown in Fig. 2(b), the power dissipation of the readout is thus dominated by two identical Gm stages G1 and G2. Although single-loop readouts have better energy efficiency, the improvement is rather limited [6, 7]. Capacitively coupled IAs (CCIAs) have even better energy efficiency because they only have a single opamp which dominates the noise in the readout circuit of the bridge sensors [9]. However, it is difficult to combine a CCIA and an ADC into a single loop with proper linearity and simplicity [10].

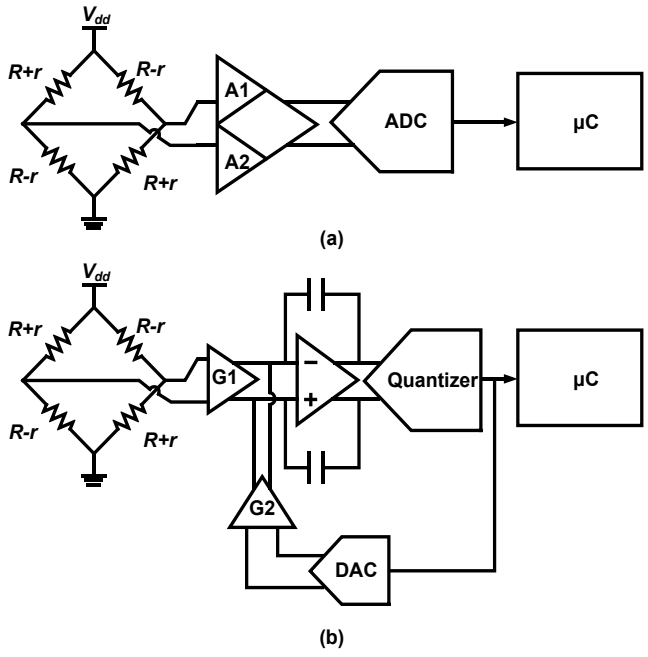

Fig. 2. Typical readout solution for bridge sensor: (a) Two-loop topology; (b) Single-loop topology.

Instead of reading the Wheatstone bridge in the voltage mode, an alternative interfacing strategy, which avoids the shortcomings of IAs, is to read out the output current of the Wheatstone bridge with a transimpedance amplifier (TIA), as shown in Fig. 3. The main noise contribution of this circuit comes from the OTA because R_f is significantly larger than R. The output signal of the TIA can be defined as

$$V_{out} = \frac{2 \times Vdd \times r}{R^2 - r^2} R_f . \quad (2)$$

It can be found that the output is a non-linear function of r as the denominator of the Eq. 2. However, for MPDP sensors, the additional nonlinearity due to the variation of r is relatively small compared to their natural nonlinearity, since r is much smaller than the bridge resistance.

In addition, the feedback network can be realized digitally by using the charge balancing technique in a ΣΔ modulator loop. Figure 4 shows the readout which is realized by embedding the Wheatstone bridge into a first order CTΣΔ modulator. The input referred noise power, which includes the noise of the Wheatstone bridge, is given by [11]

$$P_{noise} = 8kTBW(R + \frac{R^2}{R_f} + \frac{\gamma}{4g_m}), \quad (3)$$

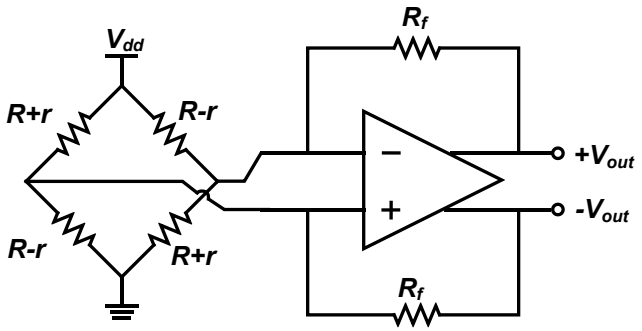

Fig. 3. Interfacing the Wheatstone bridge by a TIA.

with γ being the noise enhancement factor for short-channel transistors and g_m is the transconductance of the OTA. As shown in Eq. 3, the major noise source of this readout circuit is the OTA and the source resistance of the bridge. This suggests that the proposed architecture can be more power-efficient compared to traditional voltage mode readout ICs.

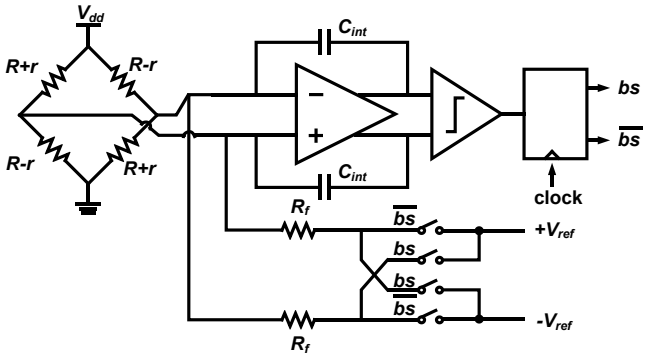

Fig. 4. Wheatstone bridge with a first-order CT sigma delta ADC.

III. Second-Order CT Readout IC for Bridge Sensors

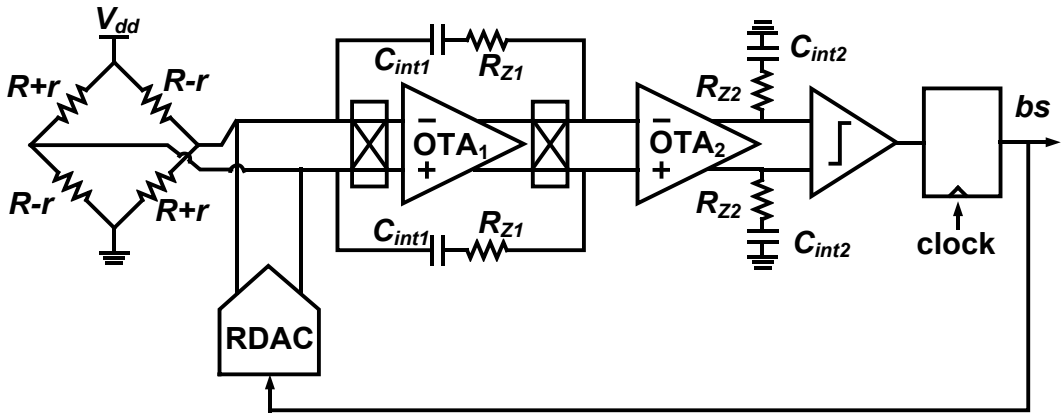

Fig. 5. Proposed readout IC for Wheatstone bridges.

A. Topology

In order to meet the resolution specification of the bridge sensors with fewer clock cycles, a higher-order ΣΔ modulator is preferable. The second order feedforward topology is adopted for energy efficiency. The oversampling ratio is set at 500 so that it can provide enough quantization noise suppression for the target resolution.

The circuit diagram is shown in Fig. 5. It consists of an RC as the first integrator and a Gm-C as the second integrator, a resistive feedback DAC, a 1-bit quantizer and a Wheatstone bridge. A Gm-C integrator is chosen to reduce the power consumption. In addition, the Gm-C integrator also helps to reduce the power consumption of the first integrator since it will not act as a resistive load to the first integrator. The offset and 1/*f* noise of the first integrator are modulated to high frequencies by means of chopping. As a result, the input referred noise spectrum will be flat and thermal noise limited at low frequencies.

The feedforward coefficient of the second-order sigma delta modulator is implemented by adding R_{Z2} to the Gm-C integrator. Thus, the transfer function *H(s)* from the input of OTA_2 to output of OTA_2 can be expressed as [12]

$$H(s) = g_{\mathrm{m}}(R_{Z2} + \frac{1}{sC_{\mathrm{int}\,2}}), \tag{4}$$

where g_m is the transconductance of OTA_2.

B. Implementation Details

In the proposed readout circuit, OTA_1 is realized in a simple folded cascade topology. It consumes 700 μA and provides a more than 80 dB open loop gain with a ± 400 mV output swing from a 5 V power supply.

As shown in Fig. 6, the OTA_2 in the second integrator is realized in the folded cascode topology with source degeneration to accommodate the output swing of the first integrator. The common mode feedback in OTA_2 is realized with two identical transistors M_{14} and M_{15}. These two transistors work in the deep triode region so that the output differential signal of OTA_2 will be canceled linearly. Since the noise of the second integrator is less significant compared to the first integrator, the power consumption of OTA_2 is only 100 μA. Moreover, it provides a more than 60 dB open loop gain with a ± 600 mV output swing.

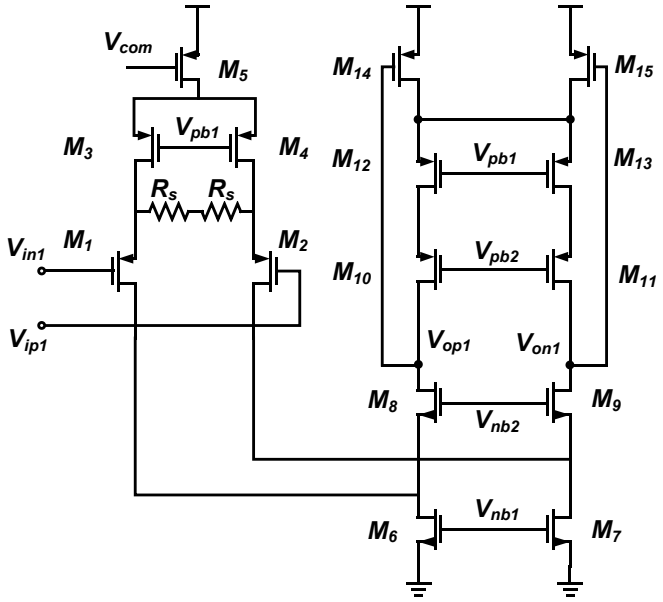

Fig. 6. Simplified schematic of OTA2 in the Gm-C integrator.

The readout consumes 860 μA from a 5 V voltage supply. The input referred noise PSD of the readout, excluding the noise of the Wheatstone bridge, can be given by

$$v_{i\mathrm{noise}} = \sqrt{8kT(\frac{\gamma}{4g_{\mathrm{m1}}} + \frac{R^2}{R_{\mathrm{DAC1}}})} \approx \sqrt{\frac{2kT\gamma}{g_{\mathrm{m1}}}}. \tag{5}$$

For 5 V transistors in 0.35 μm CMOS technology, γ is about 3.5. Since $\gamma/4g_{\mathrm{m1}} >> R_2/R_{\mathrm{DAC}}$, the noise that comes from the resistors of the DACs is negligible for this readout circuit.

Although chopping has been successfully implemented in instrumentation amplifiers and discrete-time ΣΔMs

(DTΣΔMs), it is known to cause undesirable artifacts when used in CTΣΔMs [13,14], namely fold-back of quantization noise to the signal band which is mainly due to the charging of the parasitic capacitors at the input of the OTA_1. This quantization noise fold-back can be avoided by chopping the first integrator at sampling frequency and its integer multiples.

IV. Simulation and Comparison

The proposed readout IC is designed in a 0.35µm CMOS technology. The key performance and power dissipation have been evaluated through simulation in Cadence. In the simulation, the bridge resistance is set to 3.5 kΩ and the Wheatstone bridge is modeled with 5 pF parasitic capacitance at each output node. In order to evaluate the signal-to-noise ratio (SNR), four sinusoidally time-varying resistances, which change from – 3.8 Ω to + 3.8 Ω at 503 Hz, are added to the Wheatstone bridge to model the small varying resistance *r*. A 2 mV voltage source, which is obtained from a Monte Carlo analysis, is added to the input node of the OTA_1 to model the input referred offset. The output swings of both integrators are limited to within ± 400 mV.

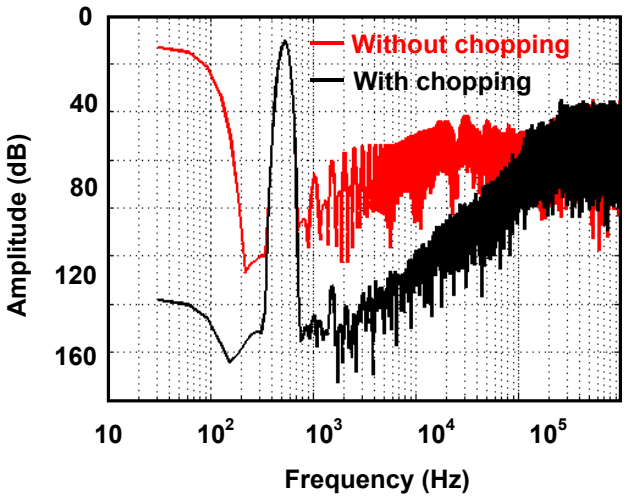

Fig. 7. FFT analysis of the bitstream of the proposed readout IC without chopping and with chopping.

As Fig. 7 shows, without chopping, the performance of readout ICs suffers from serious deterioration because the 2 mV offset does not only cause an error around the DC, but also makes the second-order modulator unstable due to the larger input signal. The performance improves significantly when chopping is enabled.

Figure 8 shows the FFT analysis with the transient noise of the readout IC. The readout achieves an SNR_{IC} of 88dB in a bandwidth of 2 kHz. The input referred noise PSD of the readout IC is 4.2 nV/√Hz since the equivalent input signal amplitude from the sensor is 5.4 mV. The overall SNR_{total} is 80dB, which takes into account the noise of the Wheatstone bridge. Together with the comparator and the biasing circuits, the readout IC consumes 860 µA from a 5 V voltage supply, which represents an NEF of 4.7 [15].

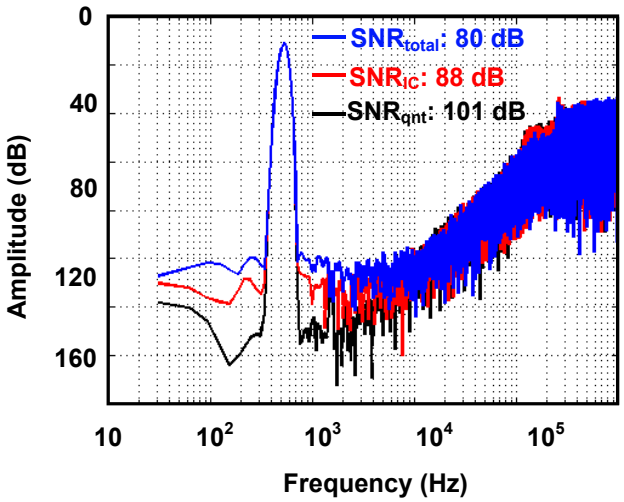

Fig. 8. FFT analysis of the bitstream of the readout IC with transient noise.

TABLE I. Performance of the Readout IC versus the State of the Art.

	This work	[1]	[5]	[7]	[10]
Architecture	RC CTΔΣM	IA + SAR	CFIA + DTΔΣM	RC CTΔΣM	CCIA + CTΔΣM
Technology	0.35µm	0.35µm	0.7µm	0.18µm	0.18µm
Year	2017	2015	2011	2015	2017
Supply Voltage (V)	5	3.3	5	1.5	1.8
Current Consumption (µA)	860[a]	61[b]	270[b]	35[b]	1200[b]
Bandwidth (Hz)	2000	50	10	5000	2000
Input Referred Noise PSD (nV/√Hz)	4.2[a]	191[b]	16.2[b]	256[b]	3.7[b]
NEF	4.7[a,c]	58[b]	10.4[b,c]	59[b]	5[b,c]

[a] Simulation Results; [b] Measured Results; [c] Folded Cascode

The key results of this work are summarized and compared in Table I to the state-of-the-art results published for Wheatstone bridge sensors.

V. Conclusion

Through this paper, an energy-efficient readout IC for MPDP sensors is presented. By digitizing the output signal of piezoresistive sensors in the current mode which are embedded in a continuous-time sigma delta converter, the noise performance is dominated by a single OTA in the first integrator. Compared to conventional voltage mode readout, the proposed readout IC requires fewer active stages and therefore consumes significantly less power. Its key performance and the power dissipation have been evaluated through simulation in Cadence. The proposed readout IC draws

860 µA from a 5 V power supply, achieving an input referred noise PSD of 4.2 nV/√Hz and an NEF of 4.

REFERENCES

[1] A. Donida, G.D. Dato, P. Cunzolo, M. Sala, F. Piffaretti, P. Orsatti and D. Barrettino, "A 0.036mbar circadian and cardiac intraocular pressure sensor for smart implantable lens," *ISSCC Dig. Tech. Papers*, pp. 392-393, Feb. 2015.

[2] M. Hämmerle and L. Pagel, "Pressure sensor in printed circuit board technology," 2010 IEEE International Conference on Industrial Technology, pp. 1553-1557, Mar. 2010.

[3] M. Maruyama, S. Taguchi, M. Yamanoue, and K. Iizuka, "An Analog Front-End for a Multifunction Sensor Employing a Weak-Inversion Biasing Technique With 26 nVrms, 25 aCrms, and 19 fArms Input-Referred Noise," IEEE Journal of Solid-State Circuits, vol. 51, no. 10, pp. 2252–2261, Oct. 2016.

[4] "Acuity Series AC401X 10 to 500 mbar Packaged Sensor Die." Acuity Incorporated, [Online]. Available: http://www.acuitymicro.com/PDF_Files/AC4010_low_pressure-1517.pdf, 2015.

[5] R. Wu, J. H. Huijsing and K.A.A. Makinwa, "A 21b ±40mV range read-out IC for bridge transducers," *ISSCC Dig. Tech. Papers*, pp. 110-112, Feb. 2011.

[6] N. Sarhangnejad, R. Wu, Y. Chae and K.A.A. Makinwa, "A continuous-time ΣΔ modulator with a Gm-C input stage, 120-dB CMRR and− 87 dB THD," *Proc. of A-SSCC*, pp. 245-248, Nov. 2011.

[7] G. Singh, R. Wu, Y. Chae and K.A.A. Makinwa, "A 20bit continuous-time sigma delta modulator with a Gm-C integrator, 120dB CMRR and 15 ppm INL," *Proc. of ESSCIRC*, pp. 385-388, Sept. 2012.

[8] C-H. Weng, C-K. Wu, and T-H. Lin, "A CMOS Thermistor-Embedded Continuous-Time Delta-Sigma Temperature Sensor With a Resolution FoM of 0.65 pJ $^{o}C^{2}$," IEEE J. Solid-State Circuits, vol. 50, no. 11, pp. 2491–2500, Nov. 2015.

[9] Q. Fan, J.H. Huijsing and K.A.A. Makinwa, "A capacitively coupled chopper instrumentation amplifier with a ±30V common-mode range 160dB CMRR and µV offset," *ISSCC Dig. Tech. Papers*, pp. 374-375, Feb. 2012.

[10] H. Jiang, K. A. A. Makinwa, and S. Nihtianov, "An energy-efficient 3.7nV/√Hz bridge-readout IC with a stable bridge offset compensation scheme," *ISSCC Dig. Tech. Papers*, pp. 172–173, 2017.

[11] M. Pertijs and J. Huijsing, *Precision Temperature Sensors in CMOS Technology*. Dordrecht, the Netherlands: Springer, 2006.

[12] C. Cai, Y. Jiang, S. Sin, Seng-Pan U, and R. P. Martins, "A Passive Excess-Loop-Delay Compensation Technique for Gm-C Based Continuous-Time Sigma-Delta Modulators," *IEEE Midwest Symposium on Circuits and Systems – MWSCAS*, pp. 1-4, Aug. 2011.

[13] F. Sebastiano, R. H. M. van Veldhoven, and S. Ersoy, "Modulator with high signal to noise ratio", European Patent EP2919388A1, Sep. 16, 2015.

[14] H. Jiang, B. Gönen, K. Makinwa, and S. Nihitanov, "Chopping in Continuous-Time Sigma-Delta Modulators," *the 50th International Symposium of Circuits and Systems – ISCAS*, Jun. 2017.

[15] M. Steyaert and W. Sansen, "A micropower low-noise monolithic instrumentation amplifier for medical purposes," *IEEE J. Solid-State Circuits*, vol. 22, issue 6, pp. 1163-1168, 1987.