Towards Scalable Qubit Arrays: Electrical Potential Landscape Control in Germanium Quantum Dot Devices

Dingshan Liu 5137993

Daily supervisor: Chien-An Wang
Supervisor: Menno Veldhorst

Abstract

Spin qubit in semiconductor quantum dot arrays offers a promising platform for future scalable quantum computing with its small size and compatibility with modern semiconductor industry. To scale up the quantum dot arrays, one of the major challenges is the wiring bottleneck, as a high density of control lines might need to be integrated into a small chip. A proposal to solve this problem is using the shared control protocol, in which multiple qubits could be controlled by a shared line. For this, the most critical requirement is to realize uniformity across the quantum dot array, such that a single control signal could lead to an identical response in all dots involved. However, such uniformity is hard to achieve due to the variation of the device fabrication, and tackling this problem via materials and fabrication optimization only appears to be a daunting challenge.

In this thesis, we propose a potential solution to achieve uniformity of threshold voltage in such share-controlled systems. This solution is based on the hysteresis behavior of turn-on voltage in the heterostructure field-effect transistor (HFET) devices hosting the quantum dot array. In the Ge/SiGe HFET devices with hole as carrier, we found that the drift of turn-on voltage can be caused by population of 2DHG under negative gate voltage and reversed by applying positive gate voltage. We attribute this effect to trapping and detrapping processes on the dielectric surface of the device. Following this discovery, an automatic feedback control program was designed, in which gate voltage pulses is applied to control the trap filling level such that potential landscape in the device corresponds to the desired turn-on voltage. Using this program, we performed deeper investigations of the turn-on voltage shift including its relaxation and history dependent stability. A hypothetical physical model for observations in these experiments is followed. For practical application of this effect, the feasibility to locally define and control the turn-on voltage is also demonstrated. Based on these results, we present a proposal for addressable manipulation of potential landscape in share-controlled quantum dot array, which might potentially realize the threshold voltage uniformity for scalable quantum dot array in the future.

Contents

1 Introduction

The intriguing property of quantum mechanics enables us to compute more efficiently in a quantum way. Early in the 1980s, physicists including Richard Feynman and David Deutsch suggested the possibility of making quantum mechanical-based computers, which could have better performance at specific computational tasks than classical computers [1]. Based on various mathematical ideas, it was soon demonstrated by proposals concerning different problems. In 1994, Peter Shor showed that quantum computers could achieve exponential speed-up in finding prime factorization [2] than the fastest classical algorithm. Further in Lov Grover's work in 1996, a quadratic speed-up is also realized in searching specific item(s) in unsorted database [3]. Nowadays, more than 200 algorithms have been proposed, serving as the evidence for the vast applicability of quantum computing [4].

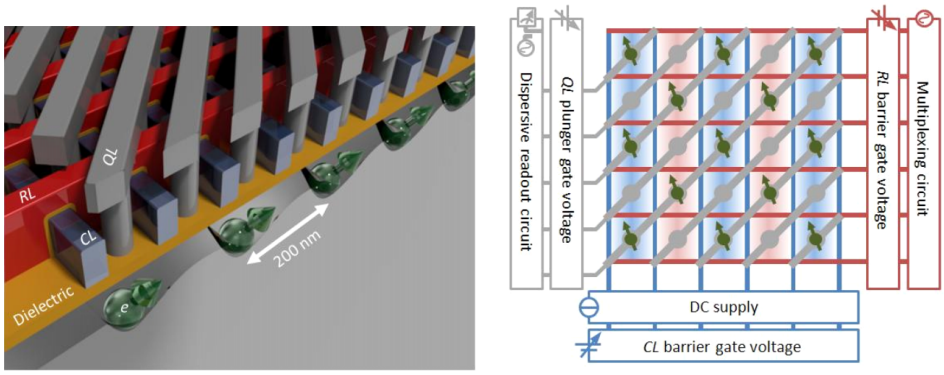
The quantum computing, however, cannot be easily realized with an arbitrary quantum mechanical two-level system. One of the major challenges is the scalability of the system. Due to the limited fidelity of current physical qubits, error correction codes are usually needed, which provides a tolerable qubit error rate up to 1% [5], but at the expense of a large number of physical qubits. Sometimes an order of 10^3 to 10^4 physical qubits are needed to perform a logical qubit, and even 10^6 to 10^4 are needed for a practical quantum computer [6].

Under this circumstance, the quantum dots in semiconductor heterostructures have became one of the most auspicious qubit platforms for their inherent scalability and compatibility with the modern semiconductor industry. In such heterostructures, several semiconductor materials are stacked in layers, forming effective 2-dimensional quantum well in their interface via the band structure offset. By tuning the voltage of the metallic gate on surface, we can control the electrical potential in the quantum well and locally confine one or few charges (electrons or holes) in small regions named quantum dots. [7]. Under magnetic field, the energy degeneracy of spin states can be lifted, and $|0\rangle$ and $|1\rangle$ state of the qubit can be encoded in these states. The gate voltage and pulse sequences can then be applied to control and readout the qubit.

The high scalability of semiconductor quantum dot systems is obvious. Due to the small size of the quantum dot structures, a large amount of qubits can be integrated into tiny chips. As example, the size required to host 2 billion qubits could be only $5 \times 5mm^2$ for quantum dots [8], but $5 \times 5m^2$ for superconducting circuits [9] and even $100 \times 100m^2$ for trapped ions [10]. Besides, the natural suitability to be arranged in two-dimensional arrays also makes it a promising platform for planar error correction codes like surface code [11], paving the way towards fault tolerance quantum computing. With these advantageous features, researchers have made a vast attempt to explore scalable quantum dot arrays. Recently, a 2×2 quantum dot array was demonstrated as germanium hole qubit platform [12], which have been used to realize a four-qubit quantum processor [13] and serves as an evidence for scalability of such platforms.

Along this path, one of the key challenges of further scaling up the quantum dot array is the wiring bottleneck, as high density of connection would be required for individual control for large qubit array [8]. To scale up a 2D quantum dot array, people need to achieve the interconnect management of extremely dense Input-Output (IO) lines, which is nearly impossible with present techniques. Under this circumstance, the shared-control quantum dot arrays are proposed as a solution for the wiring bottleneck [8,14,15]. In those shared-control arrays, control lines are crossing with each other, while each of them is coupled to multiple qubits. Thus, qubits can be uniquely addressed with

a specific combination of control lines. Fig.1.1 show a design of such share-controlled quantum dot array as an example [8].



(a) (b)

Figure 1.1: A schematic of a share-controlled quantum dot array. The Qubit lines (QL, grey) are used as plunger gates to control the electric potential of dots, while Column lines (CL, blue) and Row lines (RL, red) are used as barrier gates to control tunnel coupling between dots. A single dot can be uniquely addressed by specific combination of control lines. However, this requires high uniformity across the device. Figure from [8].

For all these shared control proposals, the most crucial requirement is the high level of uniformity across the whole layout, including uniform threshold voltage, charging energy, and tunnel coupling [8]. Only with these uniformities across the array can we control multiple qubits with a shared line, such that its control signal will result in the same effect, e.g., same charge occupancy in all dots involved. However, this turns out to be another severe challenge since the variation in the fabrication process usually induces different electrical characteristics between qubits and makes shared control hard to achieve. Tackling this problem via materials and fabrication optimization only appears to be a daunting challenge.

In this thesis, excitingly, we propose a potential solution to realize uniformity of threshold voltage in the future share-controlled quantum dot array. The idea starts from the discovery of hysteresis behavior of turn-on voltage in the HFET devices hosting the quantum dots. In such devices, we apply gate voltage to control the electric potential in the quantum well. When the gate voltage reach a threshold value, the charge carriers will start to be populated and form the conducting channel. The device is said to be turned on, and this threshold value is called the turn-on voltage. However, turning on the channel usually causes drift of the turn-on voltage, i.e., a higher voltage will be needed for turn-on in the next time. This is believed to originated from the trapping process induced by surface tunneling, which move charge carriers from the quantum well to the surface of heterostructure. These charge carriers will be captured by the surface traps and remain here, which will weaken the electric field acting on the quantum well and cause drift. As the drift usually result in instability of working condition of the device, it has always been an annoying problem that people want to avoid, and many measures are employed to prevent or bypass it.

However, in this research, we make this bug to become a feature. It is found that the drift is a hysteresis effect, as it can be reversed by the detrapping process under opposite gate voltage. Based on this discovery, an automatic feedback control program named *TurnonNavigator* is designed, which can harness the drift and adjust the turn-on voltage to any reasonable desired value. In this program, voltage pulses are applied

to control the trap's filling level, such that the resulting potential landscape gives the desired turn-on voltage for the channel. A nearly non-demolition detection of turn-on voltage is also presented. Using these tools, deeper investigations of the turn-on voltage shift are conducted in experiments with well-controlled initial conditions. This includes the relaxation of adjusted turn-on voltage after waiting at off-state voltage, and the stability of turn-on votlage adjusted from different historical paths. Based on the observations from these experiments, a hypothetical physical model named *Coin Pusher Model* is then proposed.

For future application in actual quantum dot arrays, the locality of the turn-on voltage control is also explored. In the last part of the experiments, we demonstrated the feasibility of locally define and control the turn-on voltage for single gates without affecting the others. It was found that the threshold voltage for single gates can be locally defined as the voltage needed to support the 2DHG underneath, and can be measured by reducing the voltage of the measured gate to pinch off the channel.

The aforementioned discoveries are unprecedented in previous research on semiconductor quantum dots in HFET devices. They make the threshold voltage in such devices to be a new degree of freedom that is under our control, providing a novel and promising tool to better operate them. Based on these results, we present a proposal to achieve the threshold voltage uniformity in share-controlled quantum dot array by addressable manipulation of potential landscape. This proposal serves as a potential solution for the uniformity requirement of share-controlled quantum dot array, opening up the possibilities for future scalable semiconductor quantum computing platforms.

Thesis Organization. The outline of this thesis is as follows. Section 2 briefly reviews the basic concepts of the semiconductor quantum dots and the theoretical background of this research. Section 3 describes the experimental setup. In section 4.1, we mention the first experiment of charge sensing in an 2×2 quantum dot array, which was unsuccessful due to the malfunction of device. Later in section 4.2 - 4.5, the main result and discussion of this thesis are presented, which focus on the manipulation of potential landscape in the Ge/SiGe HFET devices based on the hysteresis turn-on behavior. Finally, the conclusion and the proposal for future application are included in section 5.

2 Background Theory

2.1 Qubits for quantum computation

The advantages of quantum computing mainly come from the parallelism of quantum information. Unlike classical information represented by bits in a certain state of 0 or 1, the quantum information is stored in qubits, which can be in the linear superposition of both of them. The status of a single qubit can be described as:

$$|\psi\rangle = \alpha\,|0\rangle + \beta\,|1\rangle\,, \tag{1}$$

Here, $|0\rangle$ and $|1\rangle$ are two orthogonal basis states spanning the Hilbert space of the qubit, and α, β are two complex number satisfying normalization condition $|\alpha|^2+|\beta|^2 = 1$. By measuring in computational basis, we have possibility of $|\alpha|^2$ and $|\beta|^2$ to get $|0\rangle$ and $|1\rangle$ respectively.

Without loss of generality, the single qubit state can be further rewritten by three real angle:

$$|\psi\rangle = e^{i\gamma}\left(cos\frac{\theta}{2}\,|0\rangle + e^{i\phi}sin\frac{\theta}{2}\,|1\rangle\right), \tag{2}$$

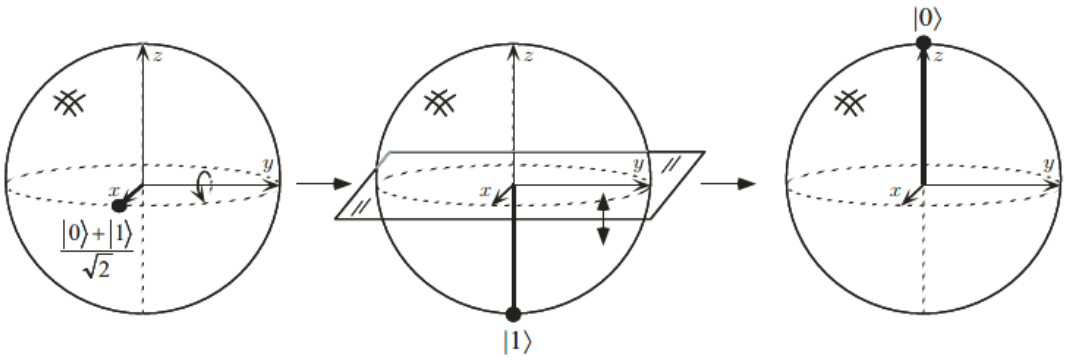


Figure 2.1: Visualization of single qubit gate as rotation in Bloch sphere. Here, the input state is $|+\rangle = (|0\rangle + |1\rangle)/\sqrt{2}$ and a Hadamard gate is applied to it, result in a $|0\rangle$ output. Figure from [16].

Which can be visualized as a vector on the Bloch sphere, as shown in Fig 2.1. A quantum gate applied to the qubit can then be represented by a unitary transformation, corresponding to a rotation in the Bloch sphere. That is, it preserves the superposition and only changes the relative coefficient of basis states.

In a quantum algorithm consisting of unitary operations, the superposition of the input state will be kept until the final measurement. This means that all possible input can be proceeded by the computer in parallel at the same time. When n qubits is involved, they can be entangled into the superposition of 2^n possible states that can be processed simultaneously, result in great computing advantage of quantum parallelism.

In the present age, enormous efforts have been made in search of the satisfactory systems for implementing quantum computation. Some promising platforms under

research includes superconducting circuits [17], single photon [18], cold trapped ions [19], cavity quantum electrodynamics [20], nitrogen-vacancy center in diamond [21] and Majorana zero modes in solid-state systems [22]. All these platforms have shown considerable potential for the future application of quantum computers, while each of them is also facing inevitable challenges and difficulties, respectively.

In this thesis, we focus on the spin qubit defined in semiconductor quantum dots. In the following sections, the theoretical background of defining and working with semiconductor quantum dot devices will be introduced, and the physical basis behind the work in this thesis will be demonstrated as well.

2.2 Semiconductor quantum dot as qubit

In a semiconductor heterostructure, quantum dots can be defined in the potential well in heterostructure field-effect transistor (HFET) devices. In Fig 2.2, the SEM image and device schematic of three examples are shown. In such devices, an active semiconducting layer (usually is Si/Ge, etc.) is stacking between barrier materials or below oxide, separated from the metallic top gate in the surface. Due to the band offset in the interface of the active layer, a shallow quantum potential well can be formed inside the layer, where charges are confined in the z-direction.

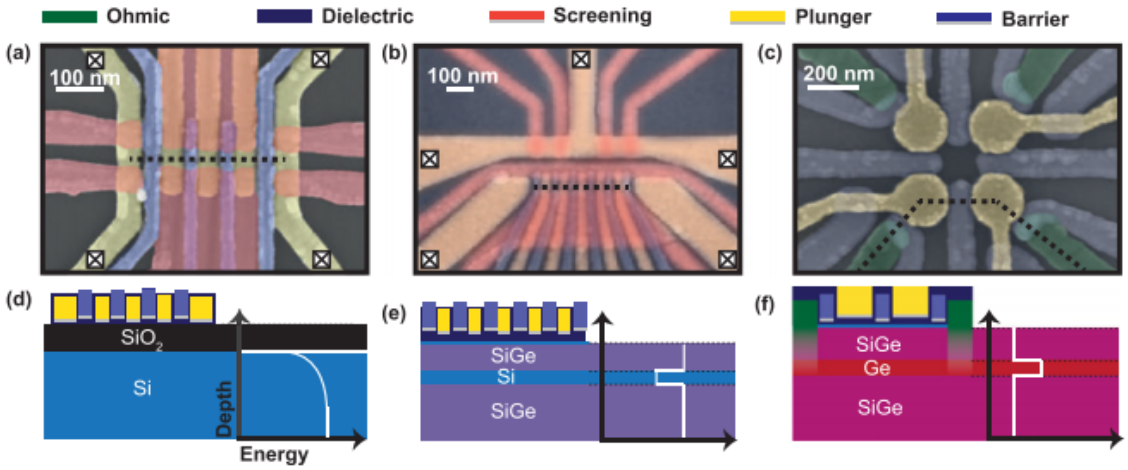


Figure 2.2: SEM images and device schematics of three examples of quantum dot systems defined in semiconductor heterostructure, including (a),(d) SiMOS QD linear array, (b),(e) Si/SiGe QD linear array and (c),(f) Ge/SiGe 2×2 array. In all those examples, the quantum dots are laterally confined in the two-dimensional channel by plunger gates on top of them. Figure from [23].

By applying an electric field from surface metallic gates, one can populate the charge carriers underneath, forming the two-dimensional electron/hole gas (2DEG/2DHG) on the surface of the quantum well. We can selectively populate and deplete the 2DEG/2DHG from top gates in a pre-designed pattern to form islands in the 2DEG/2DHG, where charges can be locally confined inside. Those islands are small enough that their sizes are comparable to the Fermi wavelength of electrons in all three dimensions, making them effective zero-dimensional systems, namely quantum dots. In a quantum dot, the energy spectrum of charge states is discrete and well-defined. When we tune the electric field from surface gates, we can control the electrostatic potential of its charge states and consequently load or remove a single charge to the dot.

To define a qubit, one can then apply a static magnetic field to the system, which lifts the energy degeneracy of spin-up state $|\uparrow\rangle$ and spin-down state $|\downarrow\rangle$ by introducing adjustable Zeeman splitting $\Delta E_Z = g\mu_B B$ between them, where μ_B is the Bohr magneton. A single spin qubit can then be encoded into these two states [24]. Besides, qubit encoding in singlet $|S\rangle = (|\uparrow\downarrow\rangle) - |\downarrow\uparrow\rangle)/\sqrt{2}$ and triplet state $|T_0\rangle = (|\uparrow\downarrow\rangle) + |\downarrow\uparrow\rangle)/\sqrt{2}$ in double quantum dot is also a favorable protocol [25]. Moreover, other encoding protocols including charge qubit [26], exchange qubit [27] and spin-charge hybrid qubit [28] were also demonstrated, serving as evidence for conveniences of quantum dot based qubit definition.

2.3 Charge transport in quantum dot system

In this section, we have a brief review of basic concepts of charge transport and sensing in quantum dot systems. Typical features in quantum dot systems like coulomb oscillation, coulomb diamonds and charge sensing are introduced. These features can serve as a characterization of quantum dot systems in our measurements.

As introduced before, a quantum dot is a conducting island that electrons are confined in all dimensions. The island can be modeled as a capacitor weakly coupled to the environment via tunnel barriers. Due to Coulomb interactions, the charging energy that a unit charge is needed to add to the island is:

$$E_C = \frac{e^2}{C} \tag{3}$$

Where C is the capacitance of the dot. However, to make the charging effect of a single electron observable and have quantized energy levels, two requirements are needed for the dot:

1. The charging energy should be much larger than thermal energy. That is, $E_C \gg k_B T$, where k_B is the Boltzmann constant. Therefore, the quantum dots measurements are required to be conducted under cryogenic temperature. Typically, the liquid helium temperature of 4.2 K corresponds to the thermal energy of 0.36 meV, which is much smaller than the 25 meV charging energy of a 10 nm metallic island [29].

2. The dot should be well isolated from the environment. From Heisenberg's uncertainty relation, the uncertainty of energy is $\delta E = h/\tau$. Here $\tau = RC$ is the charging lifetime estimated from the RC circuit model, and R is the tunneling resistance to the environment. To have a well-defined energy level, we need $E_C > \delta E$. This leads to $R > h/e^2 \approx 25k\Omega$, meaning that the dot should be weak coupled to the environment.

With these two requirements satisfied, Coulomb interaction dominates the total energy, and the quantum dot is in the Coulomb blockade regime. The constant interaction model can then be applied, and the system can be described as a single electron transistor (SET), as shown in Fig 2.3. In the SET, the dot is connected to the source and drain reservoir through barriers with constant resistance and capacitance, while a gate is capacitively coupled to the island to control its electrical potential. In our devices, the potential in the island can be tuned by the voltage of the plunger gate above the dot, and the tunnel coupling of the barrier can be tuned by the barrier gate voltage.

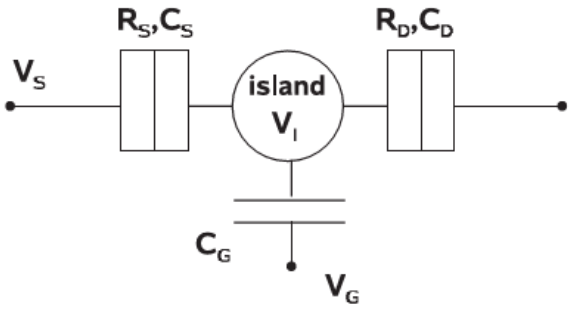


Figure 2.3: A circuit model of single electron transistor. Figure from [29]

From the capacitance model, the number of charges in the dot can then be written as:

$$\begin{aligned} Q &= C_D(V_I - V_D) + C_S(V_I - V_S) + C_G(V_I - V_G) \\ &= CV_I - C_DV_D - C_SV_S - C_GV_G \end{aligned} \tag{4}$$

Where $C = C_I + C_D + C_S$ is the total capacitance of the system. The ground state energy of the quantum dot with N electron on the dot is given by:

$$U(N) = \frac{(-eN + C_DV_D + C_SV_S + C_GV_G)^2}{2C} + \sum_{n=1}^{N} \epsilon_n \tag{5}$$

Where ϵ_n is the single-particle energy level that is related to characteristics of confinement potential. The potential with different N appears as a series of shifted parabola with respect to the gate voltage. For different gate voltage, the potential with different N take the energy minimum and becomes energetically favored. In this way, the electron number in the ground state can be tuned by the gate voltage. For the shift of electron number from $N-1$ to N, we consider the chemical potential of N th electron:

$$\mu(N) = U(N) - U(N-1) = (N - \frac{1}{2})E_C - \frac{e(C_DV_D + C_SV_S + C_GV_G)}{C} + \epsilon_n \tag{6}$$

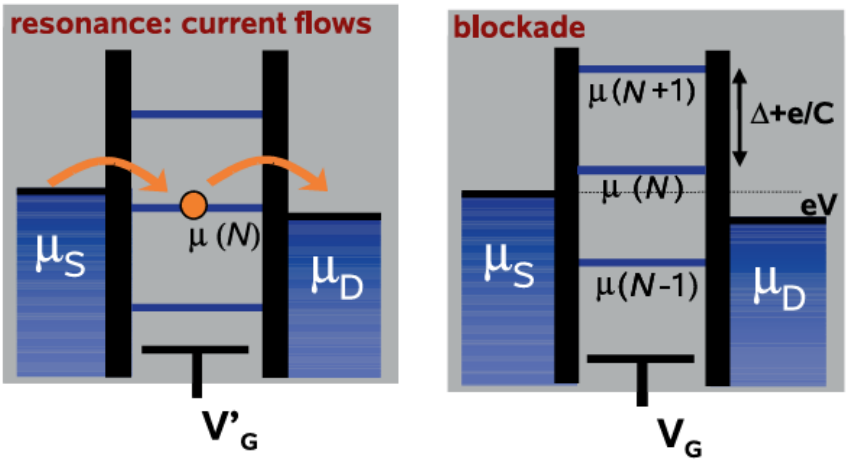
The addition energy can then be defined as the spacing between two adjacent chemical potential levels:

$$E_{add}(N) = \mu(N+1) - \mu(N) = E_C + \epsilon_{n+1} - \epsilon_n \tag{7}$$

Which describes the energy needed to add an electron to the dot with N electron occupied. Typically, the last two terms in negligible compared to the charging energy for large semiconductor quantum dots [29], so they are ignored for the following demonstration.

To allow transport through the quantum dot, the chemical potential of the dot should lie between the fermi level of source and drain, which is required from the energy conservation. As depicted in Fig 2.4(a), this condition can be achieved by applying a source-drain bias to open a bias window and tune the chemical potential of the dot within the window by the gate voltage. In this case, electron from the source can tunnel to the dot and occupy the $\mu(N)$ state, and electron from $\mu(N)$ state in the dot can tunnel to the drain, bring the dot back to $\mu(N-1)$ state. The dot can therefore

mediate the transport from source and drain and current start to flow, as shown in Fig 2.4(a). Otherwise, if no state lies between the bias window of source and drain, the transport is blocked and the SET is in the Coulomb blockade regime, as shown in Fig 2.4(b).



(a) (b)

Figure 2.4: The chemical potential configuration of a single electron transistor with (a) electron transport and (b) Coulomb blockade. Figure from [29].

In Fig 2.5, four critical configurations for transport to exist in the low bias regime are depicted. Assuming $V_D = 0$ and $V_C(N) = e(N - 1/2)/C_G$ is the reference gate voltage when $\mu(N)$ align with both μ_S and μ_D, those four critical configurations are then given by:

① $\mu(N) = \mu_S$, as depicted in left top panel in Fig 2.5. This gives:

$$\begin{aligned} \mu_S = -eV_S = (N - \frac{1}{2})\frac{e^2}{C} - (C_S V_S + C_G V_G)\frac{e}{C} \\ \therefore V_S = \frac{C_G}{C_G + C_D}(V_G - V_C(N)) = \beta(V_G - V_C(N)) \end{aligned} \tag{8}$$

② $\mu(N+1) = \mu_D = 0$, as depicted in right top panel in Fig 2.5. This gives:

$$\begin{aligned} 0 = (N - \frac{1}{2})\frac{e^2}{C} - (C_S V_S + C_G V_G)\frac{e}{C} \\ \therefore V_S = \frac{C_G}{C_S}(V_C(N+1) - V_G) = -\gamma(V_G - V_C(N+1)) \end{aligned} \tag{9}$$

③ $\mu(N) = \mu_D = 0$, as depicted in left bottom panel in Fig 2.5. This gives:

$$\begin{aligned} 0 = (N - \frac{1}{2})\frac{e^2}{C} - (C_S V_S + C_G V_G)\frac{e}{C} \\ \therefore V_S = \frac{C_G}{C_S}(V_C(N) - V_G) = -\gamma(V_G - V_C(N)) \end{aligned} \tag{10}$$

④ $\mu(N+1) = \mu_S$, as depicted in right bottom panel in Fig 2.5. This gives:

$$\begin{aligned} \mu_S = -eV_S &= (N + \frac{1}{2})\frac{e^2}{C} - (C_S V_S + C_G V_G)\frac{e}{C} \\ \therefore V_S &= \frac{C_G}{C_G + C_D}(V_G - V_C(N+1)) = \beta(V_G - V_C(N+1)) \end{aligned} \tag{11}$$

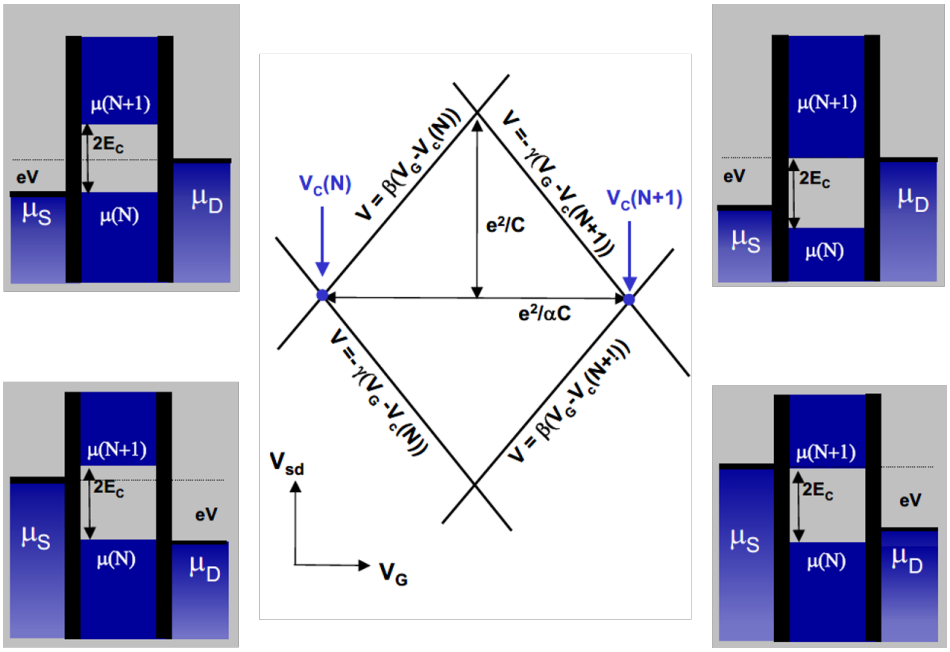


Figure 2.5: Four critical conditions of transport to exist in the low bias regime (Surrounding). When depicted in the map of gate voltage and source-drain bias, those conditions forms the Coulomb diamond region where current is forbidden (Centre). Figure modified from [30]. Note: This figure uses different definition that $E_C = e^2/2C$.

As shown in the center of Fig 2.5, those conditions form a diamond-shaped region in the map of source-drain bias and gate voltage, namely *Coulomb Diamond*. Within the coulomb diamond, the transport is blocked and the current is zero. From the coulomb diamond, much information about the system can be read. The slope of boundary of diamond gives $\beta = C_G/(C_G + C_D)$ and $\gamma = C_G/C_S$ gives capacitance relation in the system. More importantly, the lever arm $\alpha = \Delta V_G/\Delta V_I$ can be found via the length-width ratio of the diamond, serve as a measure for the efficiency of the plunger gate, i.e., how the applied voltage in plunger gate can shift the chemical potential of the dot.

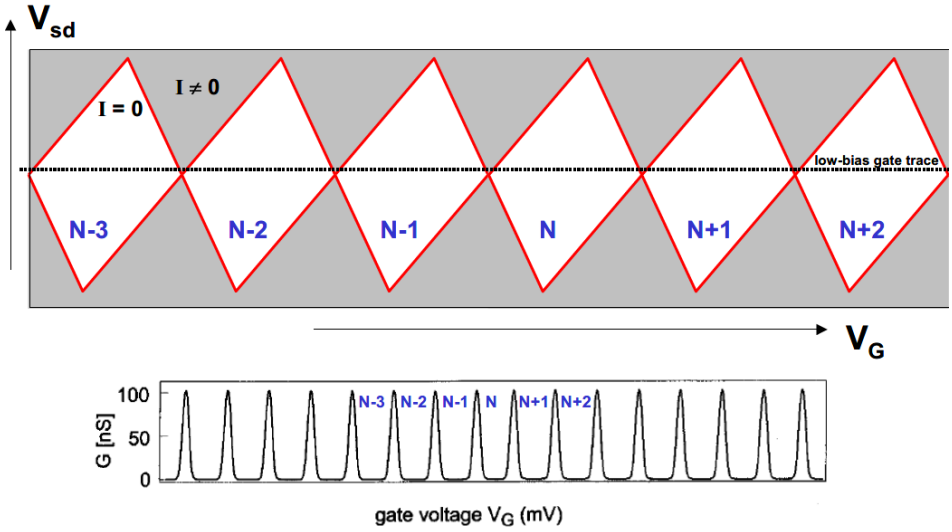


Figure 2.6: Coulomb diamonds in the map of gate voltage and bias voltage. Coulomb peaks from the low-bias gate trace are shown in the bottom figure. Figure from [30].

The full map of gate voltage and source-drain bias is shown in Fig 2.6. A series of diamonds are formed with different electron occupations N. Current is allowed to flow outside the diamonds (shown in grey) and is forbidden within the diamonds (shown in white). When sweeping the gate voltage in the low bias regime, Coulomb peaks will be observed, as shown in the bottom diagram of Fig 2.6. These Coulomb peaks indicate charge loading or unloading events in the dot.

2.4 Charge sensing in quantum dot system

In the previous subsection, we have shown that sharp Coulomb peaks appear when sweeping the gate voltage of a single charge transistor in the low-bias regime. In this regime, the bias window is small and the condition for transport is strict, which makes it sensitive to potential in the dot. Besides, when we make a larger dot for the single charge transistor, it's capacitive coupling to the environment potential is also larger.

Utilizing these effects, we can use the single charge transistor to realize the non-invasive sensing of the charge transport. To do this, we attach the sensor near to the quantum dot we want to monitor. Then we tune the sensor to the edge of a Coulomb peak in the low-bias regime in order to obtain the highest transconductance dI_{SD}/dV_G, where I_{SD} is the current through the sensor. When the gate voltage of the monitored dot is being tuned, two effects will be observed by the sensor:

1. **Capacitive coupling from other gates.** Since the gate of the monitored dot is also capacitively coupled to the sensor dot, its voltage change will also result in the potential shift of the sensor. Therefore, the position of coulomb peaks with respect to the gate voltage of the sensor will also be shifted. If the gate voltage of the sensor stays constant, this shift will be transformed to a slow and continuous change in current through the sensor.

2. **Charging Events.** When a charge is loaded or unloaded in the monitored dot, an abrupt electrostatic potential offset will be observed by the sensor. Different from the potential shift induced by capacitively coupling from the gate voltage,

these charging events will result in a discontinuous current change through the sensor.

The performance of the simple sensing method mentioned above, however, is not satisfactory. As a drawback, the signal from current in the sensor reflects both two effects, while only the charging events are of interest. Besides, the region of high sensitivity is finite with respect to gate voltage of the sensor. It would be hard to maintain desired high sensing transconductance with the same gate voltage if the potential is shifted far away.

To address these problems, a compensated charge sensing protocol is proposed [31]. In this protocol, a target value of I_{SD} in the coulomb peak is chosen. When the potential of the sensor is shifted, the resulting current change will be detected as feedback. Then the sensor gate will be adjusted to compensate the potential shift, bring back the sensor current to the target value. As a result, the sensor is always working at the same position of the Coulomb peak with the highest sensitivity. Effect from the capacitive coupling can also be suppressed and the effect from charging events can stand out.

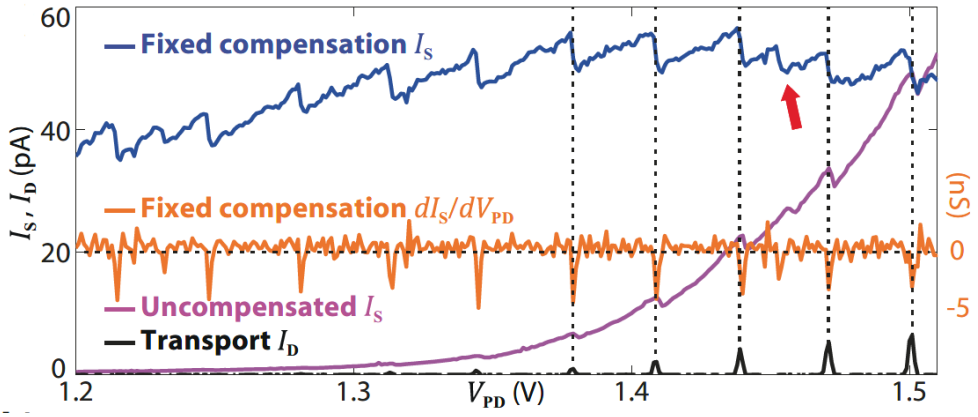


Figure 2.7: Current detected in the compensated (blue) and uncompensated (magenta) sensing experiment. The transconductance of compensated sensing (orange) and the transport current in the monitored dot (black) are also shown. [31]

A comparison of compensated and uncompensated measurement are shown in Fig 2.7. It is shown that more stable and sensitive sensing can be achieved with the compensation method.

Besides applying direct current (DC) for sensing dot, an alternative method for charge sensing is using radio-frequency (RF) reflectometry technique [32,33]. The idea of this technique is based on the impedance matching principle: Consider an input wave with amplitude A_{in}, when it transmit through a cable with characteristic impedance Z_0 into a load with characteristic impedance Z_L, a wave will be reflected back. The amplitude of reflective wave A_r is given by:

$$A_r = A_{in} \times \Gamma \tag{12}$$

With the reflection coefficient:

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{13}$$

The circuit schematic utilizing impedance match for charge sensing is shown in Fig 2.8. Here, we first build an on-resonant impedance matching network to transform the

characteristic impedance of the sensor to $Z = Z_0$. The reflection coefficient is then minimized and the highest sensitivity is achieved [33]. With this setup, an impedance change in the sensor will be directly converted into the change of reflection coefficient, and thus the detected reflected signal.

Due to the immunity from low frequency noise, higher measurement speed and broader bandwidth, the RF sensing technique is being widely used in quantum dot measurements [32–36].

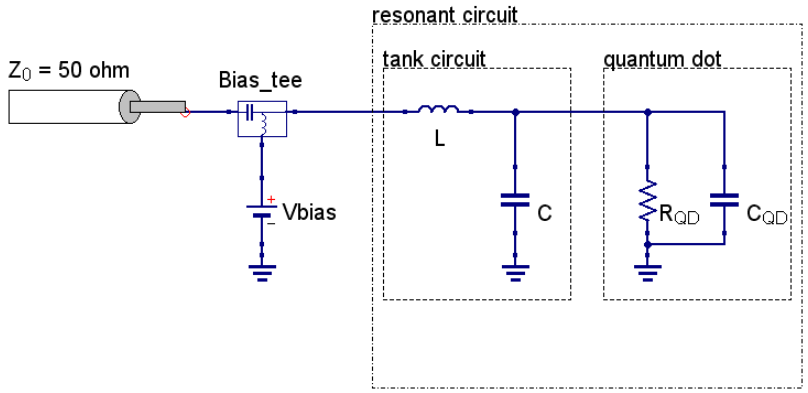


Figure 2.8: A schematic setup for RF sensing of quantum dot device. Figure from [37].

2.5 Surface tunneling in HFET devices

One of the most important physical models involved in this research is the surface tunneling model in the semiconductor HFET devices. Many interesting phenomena in the HFET system under study, including turn-on behavior, hysteretic drift of turn-on voltage and saturation of turn-on current, are believed to be well explained by it. In this section, a step-by-step physical description of surface tunneling model is shown, integrating related literature studies on such model [38–42].

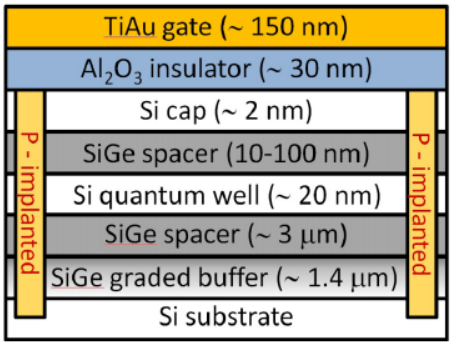


Figure 2.9: Device under study of [40]. The Si quantum well is stacked between two SiGe barriers and serve as the active layer. An oxide-insulated surface gate control the applied gate voltage. A Si cap separates the oxide and SiGe barrier

Here, we take the device studied in [40] as an example, as shown In Fig 2.9. In this device, a Si active layer is stacked between two SiGe barriers to form a buried quantum well. The metallic gates are attached on top of the device and insulated by the oxide

layer. From these gates, one can apply electrical field to tune the potential in the active layer. A thin Si cap is grown between the oxide and SiGe barrier because of its better Si-insulator interface performance than that of SiGe [43].

The Si cap is the major cause of surface tunneling. When high gate voltage is applied, charges in the buried quantum well will tunnel to the Si cap and are captured by charge traps, forming a screening layer and suppress the further tunneling process. If we keep increasing gate voltage, the speed of tunneling and population of charges in the quantum well will reach a balance, lead to saturation of carrier density. Finally, equilibrium is established between the layer and the buried quantum well. Specifically, its mechanism can be described sequentially in the following process:

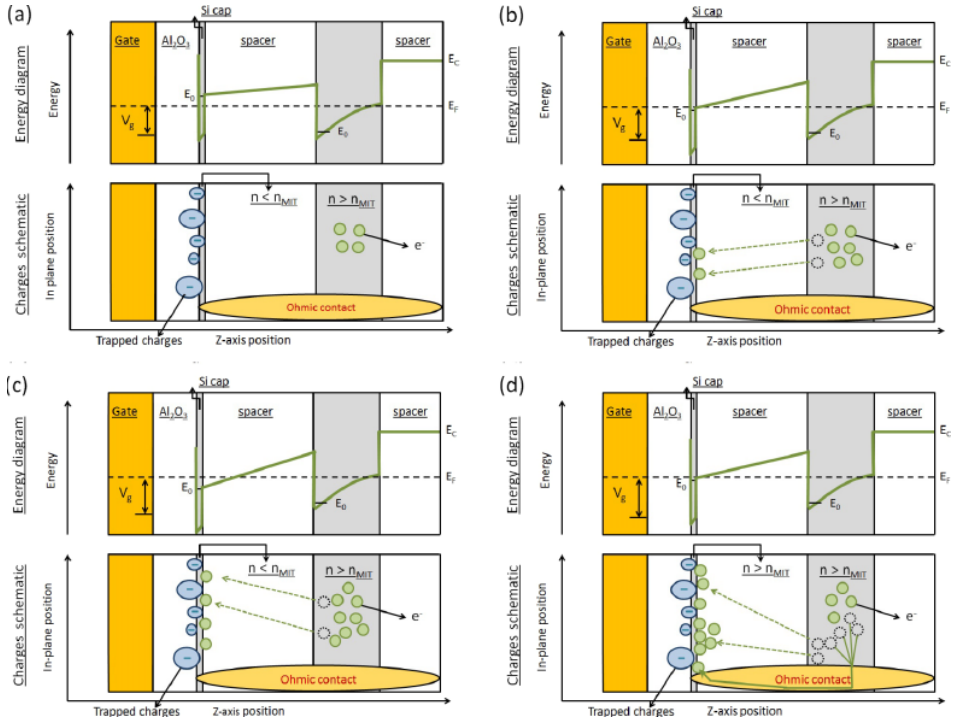


Figure 2.10: Three stages in surface tunneling model demonstrated in [40]. (a) Accumulation of charges in the active layer. (b),(c) Metastable state with slow surface tunneling from buried quantum well. (d) Equilibrium established when surface channel is conducting with ohmic contact.

2.5.1 Capacitive charge accumulation in active layer

When electrical field is applied from the gate, the conduction band (CB) energy in the device is shifted with respect to the Fermi energy level. When the ground state energy in CB aligns with the Fermi level, electron starts to populate capacitively in the buried quantum well and the carrier density increase linearly with the gate voltage, as shown in Fig 2.10(a).

This population, however, does not immediately lead to the formation of 2DEG or a conduction channel. This is because of the scattering-induced fluctuation in the potential landscape. For an actual device, disorders are randomly distributed in the interface, leading to non-uniform minima in the CB [44]. In the beginning of the population process, electrons firstly occupy these minima and are localized inside. When further increases the gate voltage, the carrier density reaches the threshold value and

produces a channel "percolate" through the potential landscape [45]. This threshold, namely percolation density, is also a metric to characterize disorder in the system. At this moment, a Metal-Insulator translation (MIT) occurs in the buried quantum well and the 2DEG is formed [46, 47]. This allows its metallic conduction with the ohmic contact.

The condition for Si cap is different. Because of smaller thickness and more disorder on the oxide interface, both the ground state energy and the percolation density of Si cap are higher than that of buried quantum well. Also the low temperature strongly suppress the thermal excitation of electron in the cap. Therefore, the population of electrons in the surface quantum well is later than that in the buried quantum well.

2.5.2 Metastable tunneling towards surface

When the gate voltage further increases, the ground state of surface quantum well also across the Fermi level and becomes energetically available. Under the electric field through barrier, electrons in buried quantum well tend to tunnel into the surface via Fowler-Nordheim process [6], as shown in Fig 2.10(b)(c). Two processes take place in this stage: On one hand, as gate voltage increasing, new electrons are populated in the buried quantum well and accelerate the tunneling. On the other hand, the tunneled electrons will weaken the electric field inside the barrier by screening effect, provide a negative feedback for this process. As a consequence, during the increase of applied voltage, the surface tunneling proceeds at a slow rate, and the carrier density in the buried quantum well nearly saturates. The system is therefore in the metastable state.

An interesting phenomenon in this stage is the surface passivation. On the cap layer, there are a large amount of charge traps, which could be attributed to many possible origins but are hard to distinguish due to small thickness of the cap [40]. Those traps are not homogeneous with respect to the location, lifetime, and corresponding potential, thus each point on the cap has a different effective barrier length between the quantum well. Since the tunneling rate of Fowler-Nordheim process exponentially depends on the barrier length and the electric field, the tunneling rate can be remarkably varied among the surface. During the tunneling, surface traps with effectively shorter barrier length are quickly occupied first, followed by slow filling of traps with longer barrier length. This process will smoothen the potential landscape in the surface, as refer as surface passivation [39].

2.5.3 Establishment of equilibrium state

As the gate voltage continues to increase, the carrier density in the surface will eventually reach the percolation threshold. Hense, MIT also takes place and the second layer of 2DEG is formed in the Si cap. This will enable the conduction between Si cap and the ohmic, thus electrons in buried quantum well can directly inject to the surface. This injection begins with a positive feedback process since the addition of electrons will enhance the conductivity of surface channel, making the injection faster. As a result, the carrier density suddenly collapses in the buried quantum well and rises in the surface, bring the system to equilibrium (Fig 2.10(d)). The screening effect in the surface then becomes much stronger, so increasing the gate voltage will mainly contribute to the density in the surface layer. In this stage, the carrier density cannot increase with gate voltage anymore.

In some works, a further stage of parallel conduction is also proposed [39], which is much more complicated and out of the range of our study, therefore is not shown here.

2.5.4 Effect on turn-on behaviors of HFET devices

The aforementioned mechanism is believed to be the origin of many effects in turn-on behaviors of HFET devices under our study. However, there are also some noticeable differences between the described model and our devices.

The first difference is the type of charge carriers. In our device, we use holes in germanium as our charge carriers instead of electrons for the review shown above. Secondly, for devices under this study we use germanium quantum well as the active layer with silicon cap on the top. Since the valance band of silicon is much lower in energy than that of germanium, the in-gap traps instead of surface quantum well will dominate the surface tunneling process. Also because of the relatively low valence band in Si cap, the last regime described in Section 2.5.3 (MIT in Si cap) does not involve in this research.

Despite these differences, all effects observed from the germanium HFET device in this research can still be addressed in this model and listed below:

- **Turn-on behavior.** When negative voltage is applied to the gate, holes are populated in the Germanium quantum well. As the hole density reaches the percolation threshold, the MIT process occurs in the buried quantum well, forming 2DHG underneath the gates. The 2DHG under each gate can be connected with each other. When the ohmic contact of source and drain is connected by 2DHG, a channel is turned on and current start to flow between them.

- **Saturation of turn-on current.** As the applied gate voltage keep increasing after turn-on, the growth of hole density in the quantum well will be slowed down by the surface tunneling. Then as described in Section 2.5.2, balance will be eventually reached between population and tunneling process. Therefore, the hole density in quantum well stop increases, and current in the channel saturates. This will result in an S-shaped curve in the I-V characteristic, where the current first grow quickly with voltage, then gradually slow down, and finally saturates at a constant value.

- **Decay of turn-on current.** If we stop increasing gate voltage after turn-on, surface tunneling still continues slowly due to the disequilibrium between surface and buried quantum well. However, no new charge being populated in this case, so the hole density slowly drops down. As a consequence, we observe the current decay on time because the decreasing hole density in the quantum well and increasing occupied traps in the surface. Eventually, the carrier density drop below the percolation threshold and the 2DHG is depleted, which also stops the surface tunneling and thus the drift.

- **Drift of turn-on voltage.** When the channel is turned on in the buried quantum well, charges start to migrate via slow surface tunneling. Those charges will remain in trap states on the surface, serve as a virtual floating gate and weaken the electric field act on the buried quantum well. With those trapped charges, a higher voltage will be required to apply in order to achieve the same electric field in buried quantum well the next time. Therefore, the turn-on voltage drift to more negative value.

A more detailed physical explanation and reasoning process for those effects, based on the experimental result, can be found in Section 4.

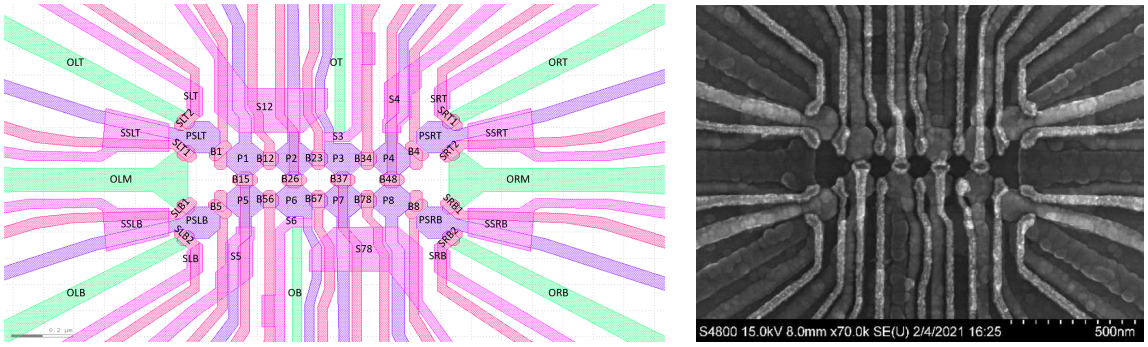
3 Experimental setup

In this chapter, we will briefly describe the experimental setup used in this research.

3.1 Schematic of the device

The sample fabrication can be described from three aspects: (1) The planar layout of the top gates and ohmic contacts; (2) The material stacking of heterostructure. (3) Deposition of gate layers.

Planar layout of the device. In Fig 3.1(a), we show the planar layout of top gates and ohmic contacts in the measured devices. The devices are composed of 12 dots, each defined by a plunger gate correspondingly. 8 dots in the central (defined by P1-P8) forms a 2×4 array to host spin qubit. 4 dots in the corner (defined by PSLT, PSLB, PSRT, PSRB) work as single hole transistors for charge sensing. Around each dot, there are barrier gates to produce potential barriers between the dots to other dots or ohmic contacts. In the peripheral of the layout, the screening gates are deposited to suppress the undesired turn-on from the fanout of plunger gates and barrier gates. The ohmic contacts connected to the device are used to supply DC or RF signals and act as a hole reservoir. The scanning electron microscope (SEM) image of the device is also shown in Fig 3.1(b).



(a) (b)

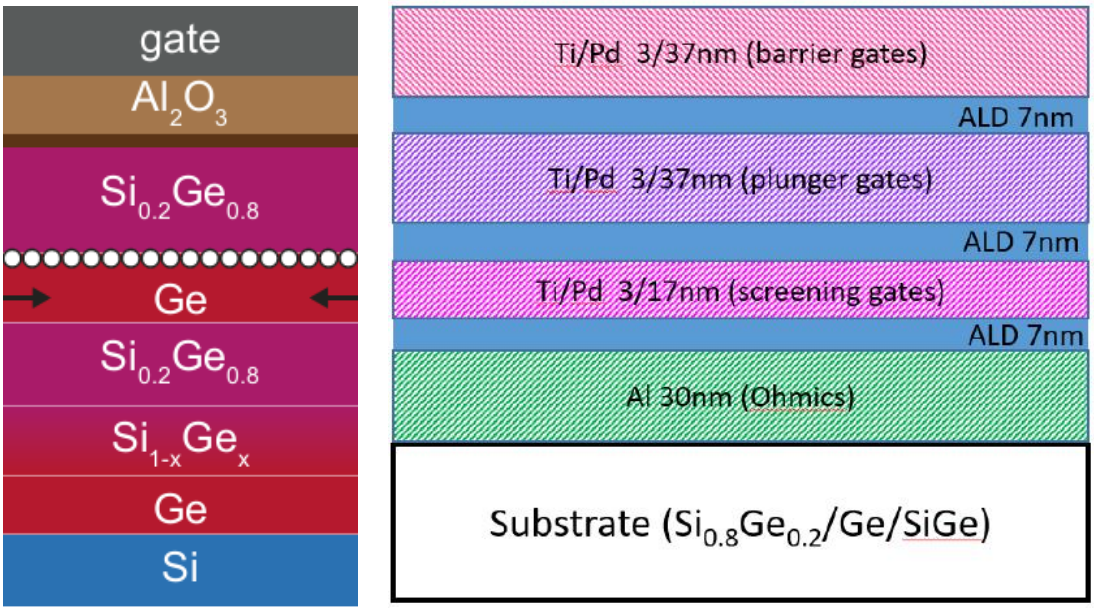
Figure 3.1: (a) The planar layout of the measured devices. The plunger gates (purple), barrier gates (red), screening gates (pink) and ohmic contacts (green) are depicted and labeled. (b) The scanning electron microscope (SEM) image of the device.

Material stacking of heterostructure. Fig 3.2(a) show the vertical cross-section profile of material stacking. The heterostructure start from a strain-relaxed Ge layer grown on the 100 mm Si substrate. A reverse graded $Si_{1-x}Ge_x$ alloy layer is then deposited to accommodate the Si-Ge lattice mismatch. In this layer, the Ge concentration decreases gradually from 1 to 0.8 and finally a $Si_{0.2}Ge_{0.8}$ buffer layer is obtained as a barrier.

Between two SiGe barriers, a 16 nm thick Ge quantum well is grown to host 2DHG in its upper interface. The quantum well is compressively strained to lift the valence band degeneracy of heavy and light hole states, result in a single band structure with heavy holes in 2DHG. The top barrier is chosen to be 55 nm-thick to moderate the tunneling between the quantum well to the semiconductor-oxide interface. Finally, a

2-nm sacrificial Si cap and Al_2O_3 dielectric is attached on top of the heterostructure, followed by metallic gates. The purpose of using Si cap is to provide a better interface with oxide and also protect the SiGe barrier from oxidization, while it will be partly oxide in air [40, 48].

Deposition of gate layers. Another cross-section schematic of heterostructure is depicted in Fig 3.2(b), which emphasis the gate layers. For the region with ohmic contacts, the Si cap is replaced by a 30 nm Al layer. The metallic gates are made from Ti/Pd with 3/37 nm (3/17 nm for screening gates) thickness respectively and their locations are depicted. Between each gate layer, the 7-nm thick AlO_x is deposited by atomic layer deposition (ALD).



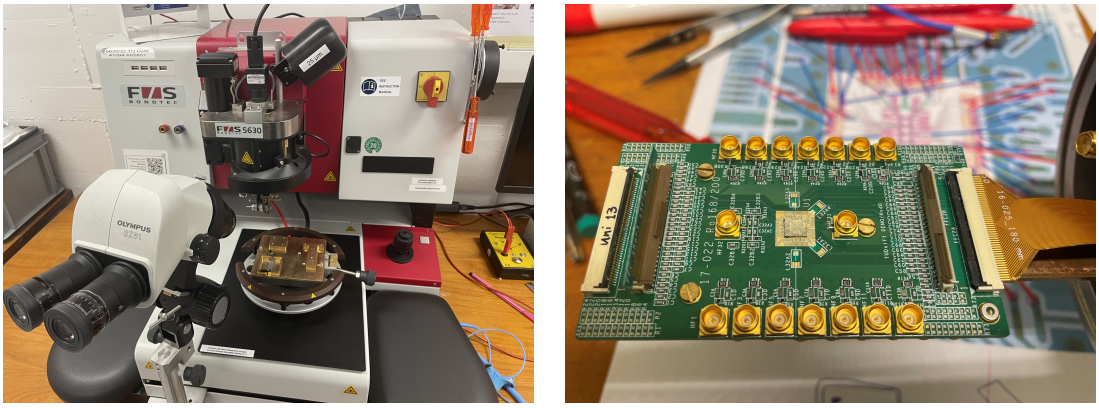
(a) (b)

Figure 3.2: The vertical cross-section schematic of the heterostructure. (a) The material stacking of heterostructure. The 2 nm Si cap between Al_2O_3 and SiGe is drown in brown. Figure from [49]. (b) Schematic of gate layers on top of the heterostructure. The Si cap was replaced by Al ohmic contact where ohmic contact is present.

3.2 Electronic preparation

Before conducting measurement in the sample, it needs to be first connected to the electronic setup. In this section, a series of preparation steps from a bare sample to complete measurement is introduced.

PCB and Bonding. After fabrication, the chip holding the bare sample is glued on the printed circuit board (PCB). To connect the chip and the PCB, we need to bond wire between bondpads on the chip and PCB with wirebonder. Fig 3.3 shows the BONDTEC 5630 Semi-Automatic wedge bonder used in our experiment and a bonded sample on PCB. After bonding, the gates can be accessed by matrix module via a stripline plugged in the PCB connector, as shown in Fig 3.3(b).



(a) (b)

Figure 3.3: Pictures for (a) BONDTEC 5630 Semi-Automatic wedge bonder (b) A bonded sample on PCB connected to the stripline.

Device storage. When the device is not being tested, its connectors need to be shorted by a grounding piece. Then it is put into the electrostatic discharge (ESD) safe box and stored in the vacuum desiccator, as shown in Fig 3.4.

(a) (b)

Figure 3.4: Pictures for (a) A device in the box (b) Vacuum desiccator.

Electronic connection. To conduct a computer-controlled experiment, the SPI rack platform [50] is used, as shown in Fig 3.5. In such platform, modules with various functions can be integrated and connected, provide us with full electronic input and output setup. Here, we introduce each part of the setup following order of connection:

- **DAC.** The digital control signal from computer is first transmitted to the digital-analog converter (DAC) through the USB cable. The DAC can convert the digital control signal to analog voltage output. From the connected wire, the output voltage signal can be sent to the modules.
- **Matrix Module.** The matrix module is a connection box with its ports connected to PCB through Fischer cables. From corresponding ports in its panel, we can apply analog voltage to each gate in the device. A switch is attached to each port to control its connection state (on/open/ground). In the matrix module, there are also some "ground" ports that ground the connected wire and "link" ports that link the connected wire together.

- **Source and Measurement Modules.** To conduct electrical measurements, we commonly use the voltage source and current measurement modules. The voltage source module can be controlled by signal voltage from DAC. It then converts it into the desired DC voltage and feeds it to the device through matrix module. The current measurement module is connected with a Keithley 2000 multimeter and the measured value is recorded by computer.

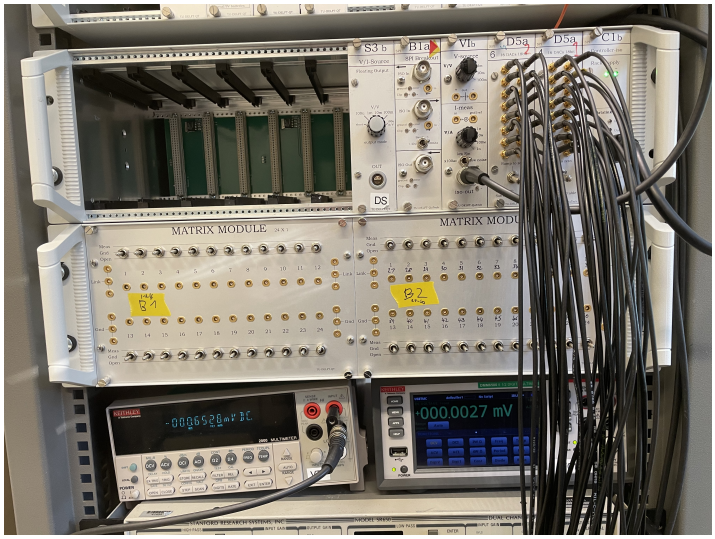
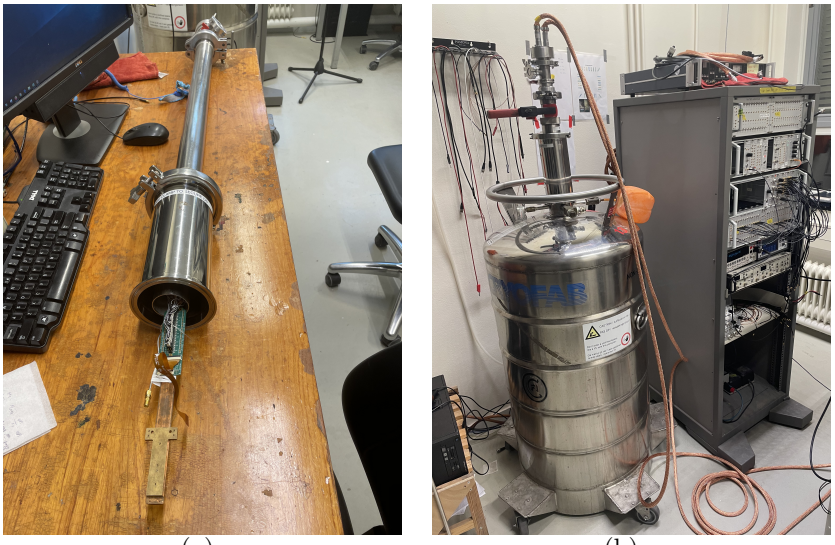


Figure 3.5: A picture of the measurement modules used in the experiment.

3.3 Cryogenic environment

To conduct quantum dot experiments, cryogenic temperatures are usually needed. Experimentally, we have two common setups for this: dipstick setup and dilution refrigerator setup.



(a) (b)

Figure 3.6: Picture for the dipstick measurement setup. The sample is mounted in the stick shown in (a) and dipped into the dewar as shown in (b).

Dipstick setup. In practice, the most convenient way to prepare a cryogenic environment is the dipstick measurement. As shown in Fig 3.6, in dipstick measurements the sample is mounted in a stick and dipped into the liquid helium dewar. The wires connected with matrix module are plugged into the stick. These wires are connected to each gate in the sample. Using the dipstick setup, we can cool down the device to $\sim$ 4K quickly and warm it up in around 30 minutes. Therefore, it is commonly used as the preliminary measurement or quick checking of new devices.

Dilution refrigerator. To obtain lower temperature (below 20 mK), we need to use the ^{3}He/^{4}He dilution refrigerator. In the dilution refrigerator, the device to measure is attached to a mixing chamber. The mixing chamber contains two phases of mixture of ^{3}He and ^{4}He: the concentrated phase (100% ^{3}He) and the dilute phase (6.6% ^{3}He). The heavier dilute phase lies in the bottom and its ^{3}He is being pumped out. Consequently, the ^{3}He in the concentrated phase is diluted and flows into the dilute phase. This is an endothermic process that can be used to cool down the sample. Finally, the pumped ^{3}He is purified and replenished to the concentrated phase of the mixture, finishing the cycle.

4 Results and discussions

In this chapter, the experiment results of this thesis in presented. The experiments are mainly divided into two parts:

Part 1: Single hole transistor as sensor (Section 4.1)

In the first part of the experiment, a device with 2×4 quantum dot array was measured in the dilution refrigerator ($T \sim 10$ mK). The original goal of this experiment was to characterize this device as a quantum information processor and conduct qubit measurements. However, this experiment is shown unsuccessful due to the dissatisfactory performance of the sensor. Therefore, further tests were not performed and only the basic sensing experiments are presented in Section 4.1. This part is only used to demonstrate how the devices are supposed to be functioned.

Part 2: Manipulating potential landscape in HFET devices (Section 4.2 - 4.5)

The second part of the experiments gives the main results in this thesis. In this part, we focus on the hysteresis behavior of turn-on voltage in the device. This direction is, fortunately, inspired by the occasional discovery of reversible drift of turn-on voltage in the HFET. Following this discovery, an automatic feedback control of the turn-on voltage is proposed and the physical mechanism behind the turn-on behaviors is studied. Finally, the locality of the observed effect is explored. This part of experiments is done with three sensors in 2×4 quantum dot devices in dipstick setup ($T \sim 4$ K).

4.1 Single hole transistor as sensor

As introduced in Section 2.4, a single hole transistor can be used as a sensor for charge transport in the quantum dot array. Because of this role, the first step to test a quantum dot device is usually the test of the sensor dot. In this section, the measurement of a 2×4 quantum dot device (SQ20-243-C5) in the LD 400 dilution refrigerator is presented. Fig 4.1 re-display the layout of the measured device from Section 3.

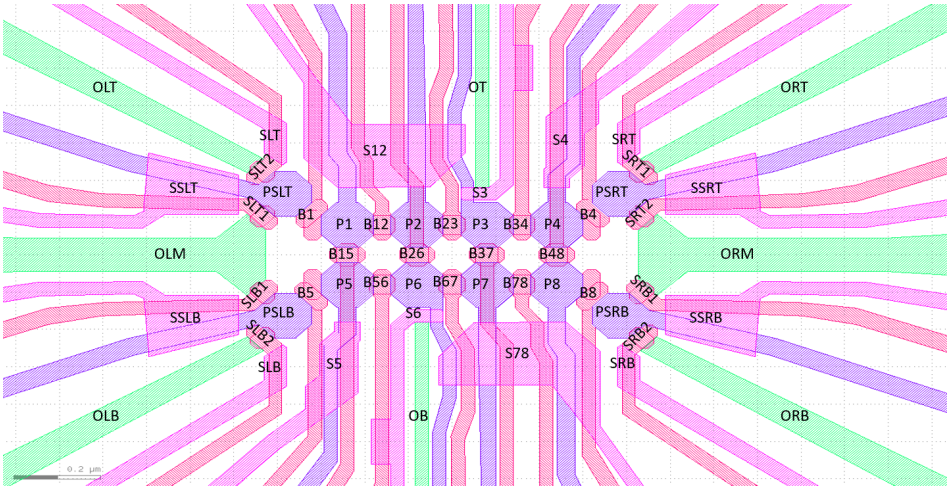


Figure 4.1: The schematic of measured 2×4 quantum dot device.

4.1.1 Coulomb peaks and Coulomb diamonds

The test of the sensor starts with the formation of the sensor dot. For a single hole transistor, this can be done by applying negative voltage in the plunger gate to populate the 2DHG underneath and using barrier gates to create barrier on edge of the dot. In such a configuration, the sensor dot is weak coupled to the surrounding and near the Coulomb blockade regime.

In our device, however, it was shown that the formation of sensor dots is not that easy. The sensor dot can only be defined in Left Top (LT) and Left Bottom (LB) single hole transistor, as the others are not functioning well: the Right Top sensor has leakage, and the Right bottom sensor cannot be turned on. Therefore, in this device only LT and LB sensors are tested.

To verify the formation of a quantum dot, the most common way is to measure the Coulomb peaks and Coulomb diamonds in the dot. In these tests, we first search for the Coulomb peaks by sweeping the sensor gate (e.g., PSLT) in a negative voltage range with barrier gate (e.g., SLT1 and SLT2) in positive voltage. Source-drain bias is supplied through Ohmic contacts connected to the sensor and the resulting DC current is measured. After Coulomb peaks are found, the corresponding Coulomb diamonds are measured in the gate-bias spectroscopy.

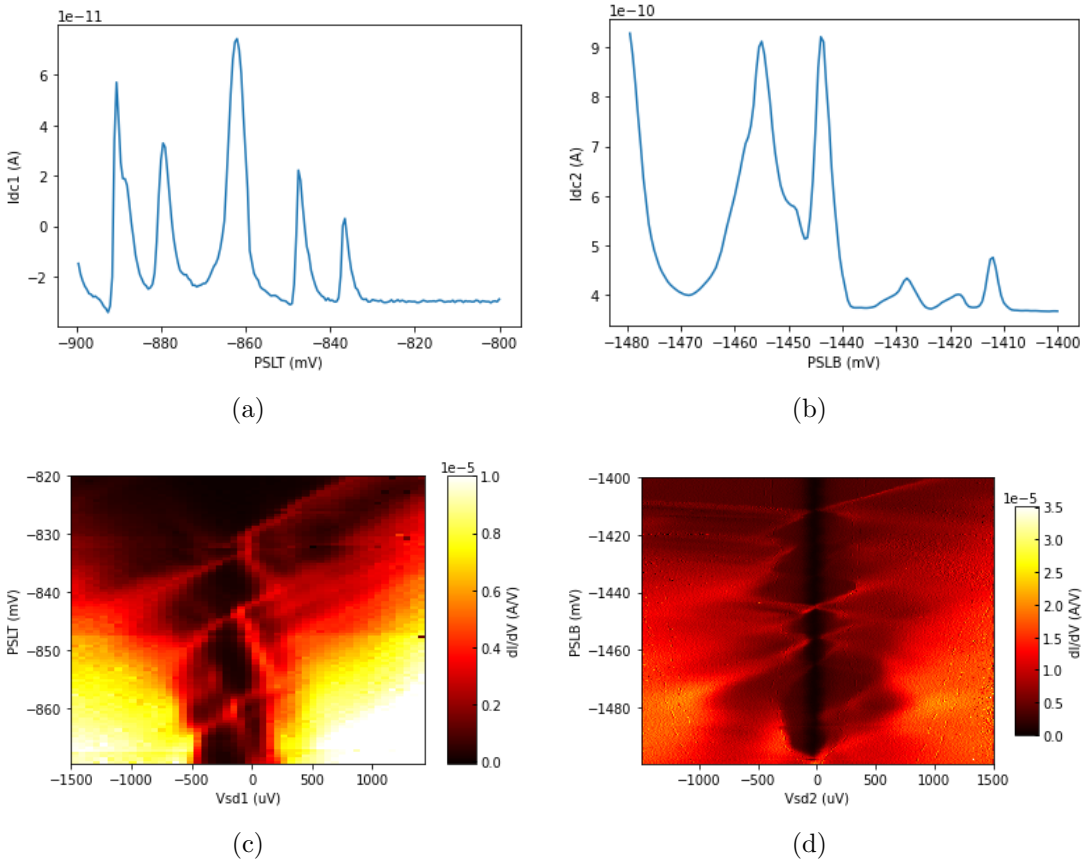


Figure 4.2: The Coulomb peaks and Coulomb diamonds measured in (a),(c) LT sensor and (b),(d) LB sensor. Here Idc1 (Idc2) is the DC current through LT (LB) sensor under bias. These measurements can be used to verify the formation of quantum dot.

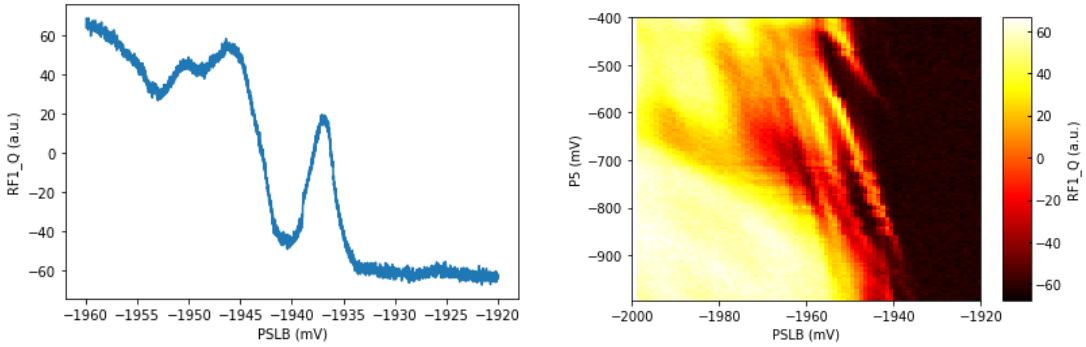
As shown in Fig 4.2, irregular Coulomb peaks and diamonds are found in both sensors. These results indicate the formation of sensor dots, however, not with high

quality. Firstly, regular and sharp Coulomb oscillations with a well-blockaded current in between are expected for a sensor, which are absent in the measurement. Secondly, behavior of these coulomb peaks is shown unstable in later experiments. In the later sweeps, the distribution of these peaks change between experiments and drift to more negative voltage as experiment goes. (At this time, the effect discussed in Section 4.2.1 is not discovered) After thermal cycling, the Coulomb peaks cannot be found in the LB sensor any longer, and are only detected in the LT sensor below -2100 mV. Therefore, further measurements with DC current were not performed.

4.1.2 RF charge sensing with compensation and "skiing" trick

An alternative way of charge sensing, as introduced in Section 2.4, is using the RF reflectometry technique. With this method, each sensor is associated with a resonant frequency by a tank circuit, and can be operated separately with the corresponding frequency. As an unexpected result, the RF measurement only shows a simple turn-on curve with a single peak, different from Coulomb peaks in the DC measurement. Besides, this peak is also unstable when the gate of nearby dot is varied.

Fig 4.3 shows an example for this in LB sensor. We can see the turn-on curve of voltage in PSLB with a single peak before the turn-on. However, as depicted in Fig 4.3(b), this peak is unstable when tuning P5, a plunger gate of the nearby dot. This behavior is believed to be caused by some fine structures close to the sensor rather than the transition in P5, since it strongly depends on PSLB but weakly depends on P5. These fine structures might be originated from undesired quantum dots formed in other gates, i.e., screening gates. If these undesired dots are coupled to the sensor, a similar sawtooth line might be observed.



(a) (b)

Figure 4.3: (a) The RF response of LB sensor in 1D sweep of PSLB. It appears as the turn-on curve with a single peak. (b) Effect of P5 on this turn-on curve. When P5 is tuned, the turn-on curve appears unstable.

In this situation, we use a trick before we employ the sensor dot for charge sensing. Before introducing it, we first need to recap the concept of compensated sensing. As discussed in Section 2.4, the operation of sensing dot relies on the peak or a steep slope in the response of sensing gates. By placing the sensing gate at the slope, the shift of nearby electrostatic potential will be transferred into the shift the sensor response due to the high gradient on the slope. When the compensation technique is applied, the shift can be compensated by moving the sensor gate voltage such that the same response is retrieved.

However, the compensation breakdowns when the slope to use is unstable. To understand this, we can look at an example demonstrated in Fig 4.4. Fig 4.4(a) shows a choice of slope in the response curve of PSLT. Here the target response is set to be -70, corresponding to the starting gate voltage about -1928 mV in the slope. During the compensated sweep, the voltage of P1 is swept (starting from the value used in Fig 4.4(a)) and the voltage of PSLT is automatically adjusted to retrieve the target response, based on the pre-set slope direction.

In the 2D map of PSLT and P1 (Fig 4.4(b)), the route of this compensated sweep is visualized by the yellow arrows. The map is depicted to show the contour with target response. Under compensation, the sweep goes along the contour - when the target position at slope is shifted to less negative, voltage of PSLT is corrected to less negative value to compensate for it.

In this example, the chosen slope is unstable and disappears after P1 $\sim -555mV$. When the sweep reaches this point, it pumps into the contour line and the compensation breakdowns. At this point, the program detects an increase of the response as P1 sweeps down, then the PSLT is swept more negative according to the pre-set slope. However, the actual slope is disappeared and this correction cannot retrieve the target value, so both the PSLT and response diverge. The trajectory of response and compensated PSLT is shown in Fig 4.4(c) and Fig 4.4(d) respectively.

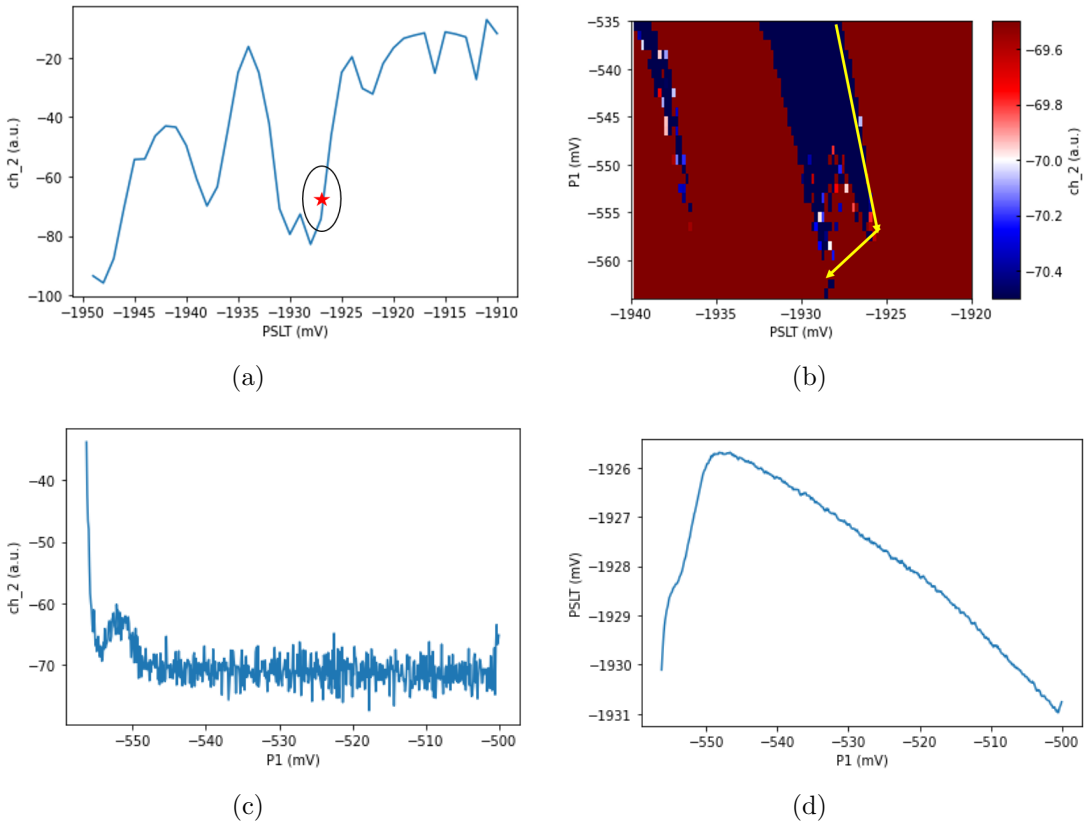
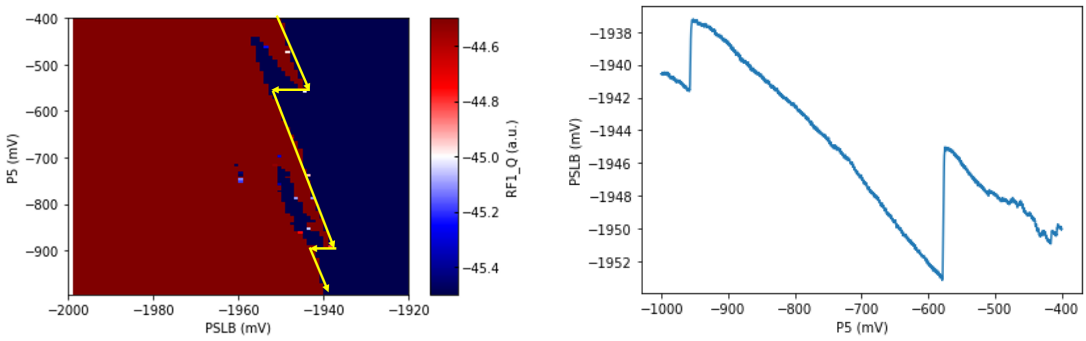


Figure 4.4: An example of compensation breakdown. (a) The chosen slope and target value of response from a response curve of sensor gate. The starting point of compensated sweeping is chosen as nearly -1928 mV and target response is nearly -70 (marked with a red star). (b) The 2D map on PSLT and P1. The color map is set that contour of the target response is shown. The yellow arrows show the route of compensated sweep. At nearly P1 = -555 mV, the chosen slope disappears and the compensation breakdown. (c) The response during compensated sweep. (d) PSLT voltage under compensation during the sweep.

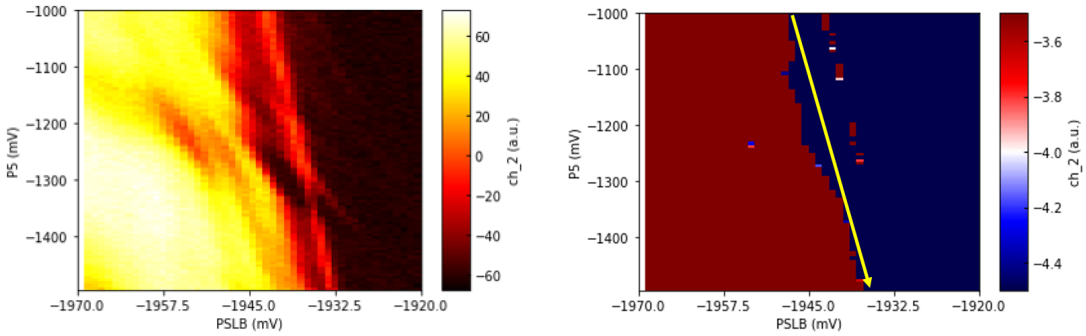
To avoid this problem, we can use a "skiing" trick to pre-design the route of compensation. An example of this is shown in Fig 4.5, using the same map in Fig 4.3(b). By pre-measuring a 2D map of the sensor and nearby plunger gate, we can predict the trajectory of the compensated sweep and choose a target value such that its contour is desired. To visualize the contour line, we can move the indicator in the color bar of 2D map. In Fig 4.5(a), a contour with target value -45 is shown, together with the predicted trajectory of compensated sweep. This prediction agree with the actual compensated sweep shown in Fig 4.5(b).



(a) (b)

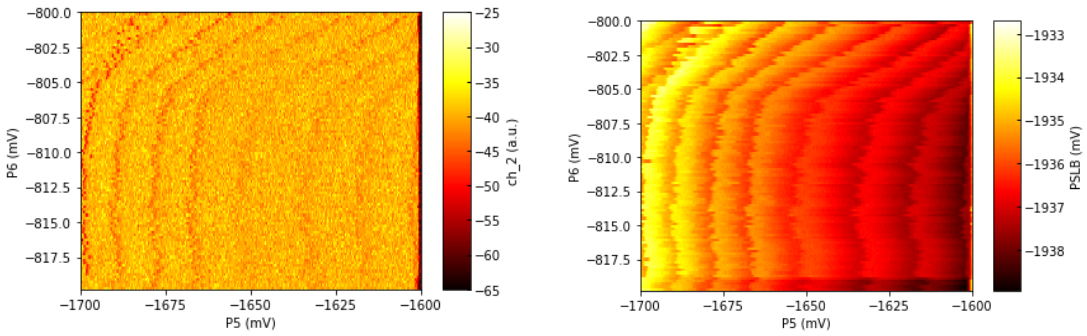
Figure 4.5: An example of pre-designed compensated sweep. (a) The contour with target value -45, chosen by moving the indicator of color bar. The predicted trajectory of compensated sweep is shown as yellow arrows. (b) The compensated PSLB voltage when sweeping P5. It agree with the trajectory predicted in (a).

The trajectory depicted in Fig 4.5, however, is not desired since it looks like a charge transition and might give us fake signal for sensing. To avoid this problem, the related gates were adjusted such that a continuous trajectory can be found for the compensated sweep, as shown in Fig 4.6.



(a) (b)

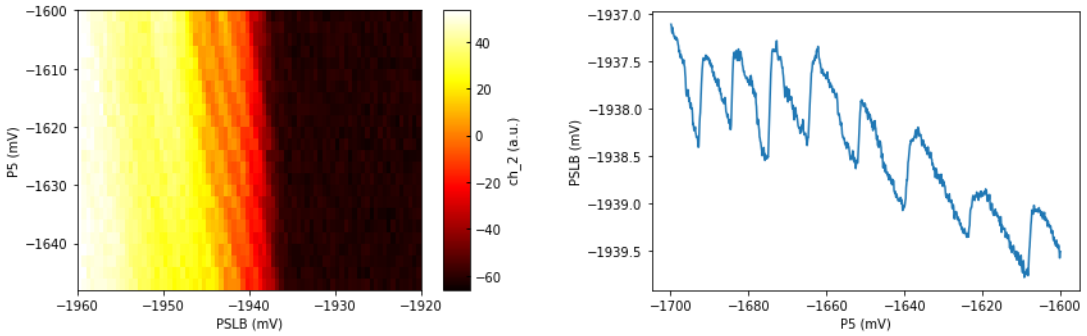
Figure 4.6: A compensated sweep trajectory can be designed to be continuous by choosing a proper range of gate and target response value. (a) The 2D map of PSLB and P5. (b) Contour for the chosen target response value (-4) and the designed trajectory for compensated sweep.



(a) (b)

Figure 4.7: The sensing result of sweeping P5 and P6. (a) The RF sensing response.(b) The compensated PSLB voltage. It seems to be the signal of merged dot between P5 and P6.

With the sensor prepared, a 2D measurement for dots in P5 and P6 is made. The result is shown in Fig 4.7. It seems to indicate the existence of merged dot between P5 and P6. To confirm this result, we double-check the sweeping trajectory in higher measurement precision. Unfortunately, the result in Fig 4.8 shows that fine structures are still unavoidable on small voltage scale and will cause fake transition signals. When P5 is being swept, these signals appear with spacing about 10 mV, which agrees with the behavior in Fig 4.7. We thus believe that this result is caused by the fine structures near the sensor instead of charge transition.



(a) (b)

Figure 4.8: Double-check of the sweeping trajectory in higher measurement precision. (a) The 2D map of RF sensing response from PSLB and P5. (b) The compensated PSLB voltage when sweeping P5. Saw-tooth lines are observed in this measurement, indicating the fine structures near the sensor.

In this section, we presented a trick to preparing a stable sensing route which is free from fake signals. This effort was shown not successful, however, it can also serve as a method to double-check the sensing result by tracing the trajectory of compensated sensing sweeps.

Due to the unsatisfactory performance of the device, further experiment is not carried out. This is attributed to the following problems:

1. The response from RF measurement does not agree with the DC one. The former shows turn-on behavior, but the latter shows irregular Coulomb peaks.

2. The response curve of sensor gates is noisy when plunger gates nearby are varied. As shown in this section, this might cause fake signal of charge transition. This problem was then shown to be hard to avoid.

3. The sensors in this device are not functioning well. The RB sensor cannot be turned on, and leakage was found in the barrier of RT sensor.

4. Hysteresis behavior is found in the barrier gates of sensor. To tune the channel from on-state to off-state, the barrier gates need to sweep down for around 1 V. For example, if they were pinch off at -800 mV, they need to be swept to -1700 mV in order to turn on, vice versa. However, this was later shown to be caused by the filter in the fridge by my colleague, which is different from the effect introduced in later subsections.

4.2 Hysteresis behavior of V_{on} in the HFET devices

In this section, the hysteresis properties of the turn-on voltage (V_{on}) are investigated as the most important phenomenon in this thesis. As introduced in Section 2.5, when we apply negative gate voltage to turn on the channel in an HFET device, 2DHG is formed and surface tunneling begins. Consequently, surface traps in the device are occupied and higher turn-on voltage will be needed to turn on the channel the next time.

This phenomenon, also known as *Drift*, is one of the most annoying problems in the cryogenic experiments of HFET. This is because the drift is usually a one-way process and reversing it is inconvenient. Under this circumstance, the working window of the gate voltage is unstable and the measurements can hardly be done in automatic and repeatable manner. Typically, there are two available methods to reverse the drift:

1. **Thermal Cycle.** Warm up the device to induce thermal excitation to the system. As a consequence, the whole device will then be reset.

2. **LED Exposure.** Connect all gates to the ground and apply LED light to the device. The device will also be reset by absorbing photons and heat from LED.

These two methods, however, cannot provide a satisfactory solution for the drift problem. One of the reasons is the interruption of the experiment, as both methods involve resetting the whole device and will erase all the preset conditions. Also the time cost is considerable: to apply a thermal cycle in the 4K dipstick experiment, one needs to pull up the device and warm it up naturally for half an hour; For dilution refrigerator it's even more time-consuming, since more than one day is usually needed.

Therefore, in practice these two methods are only used as the final reset step after a series of experiments. In most of the time, people still need to operate carefully to avoid the drift. This lead to the limited number of measurements we can apply, and also it is difficult to conduct experiment with identical initial condition.

As an exciting result, in the following sections we introduce a new method to reverse the drift in a convenient and reliable way. It is shown that by applying a positive voltage to the gate, we can reverse the turn-on voltage drift for all three HFETs tested in the experiment. Focus on this discovery, deeper investigations were made and introduced in this section. The list of relevant experiments and the devices involved is shown Table 4.1.

Regrettably, this phenomenon was found in the last month of the project, thus the time for the following experiments is highly limited and repeating experiments in all tested devices is unpractical. However, the universality of this phenomenon is still required. Therefore, the experiments shown in this section were carried out in the following way: When a new batch of experimental ideas was proposed, it will be tested for different HFET devices. At the end of the research, all these tests were repeated in the first device and demonstrated in the following sections to keep the consistency of the experiments. The test result from other devices will also be briefly mentioned.

Device under test		SQ20-8Dot		
		Batch 4 Dev5	Batch 4 Dev7	
Section	Experiments	RT sensor	RT sensor	RB sensor
4.2	Reversible Drift of V_{on}	✓	✓	✓
	Effect of Sweeping Range	✓	✓	✓
	Effect of Waiting Time	✓		
4.3	Touch-and-Back Sweeps	✓		
	Automatic Feedback Control of V_{on}	✓	✓	✓
	Relaxation of Adjusted V_{on}	✓	✓	
	History Dependent Stability of V_{on}	✓		
4.4	Decay Suspension Test	✓		✓
	"Swing" Experiment	✓		

Table 4.1: Summary of devices tested in the experiments of section 4.2 - 4.4. All these devices come from the same batch, so they have the same design and fabrication process. In this chapter, the results from the same HFET (RT sensor of SQ20-8Dot, Batch 4, Device 5) are presented, while test results for other HFET will also be briefly mentioned.

Based on the focusing topic, these experiments are sorted in section 4.2 - 4.5 with following topics:

- In section 4.2, we explore the basic characteristics and affecting factors of the reversible drift in HFET. The effect of the voltage range of sweep and waiting time at positive voltage are investigated.
- In section 4.3, we utilize the reversal of drift to design an automatic feedback control program, which can control the turn-on voltage precisely to any desired voltage in the common operation range. This program enables tests with well-controlled initial condition of the device, therefore deeper investigations of turn-on behavior are made. These include the relaxation of the adjusted turn-on voltage and the history dependent stability of turn-on voltage.
- In section 4.4, based on several assumptions, a hypothetical physical model is proposed as a possible explanation for turn-on voltage behaviors in all experiments above. Each phenomenon observed in section 4.2 and section 4.3 is explained correspondingly.
- Finally in section 4.5, we investigate the locality of this effect and explore the possibility of separately define and control the turn-on voltage of a single gate. This is crucial for local control in the future application of tuning quantum dot arrays.

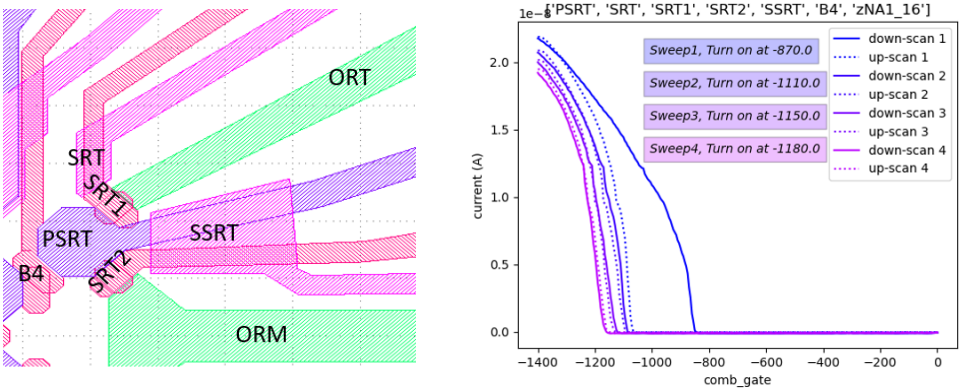
4.2.1 Reversible drift of V_{on}

To have a better introduction to the experiment condition and method in this research, we start with a simple demonstration of the drift of turn-on voltage. Fig 4.9(a) show the gates involved in measured HFET of the experiment. In the following tests, the dc voltage is applied to the ORT contact in series with the current measurement module, and ORM was grounded as the drain. Then PSRT, SRT1, SRT2, SRT, SSRT and B4 are swept together as a combined virtual gate. By applying negative voltage to these gates, 2DHG can be populated in the quantum well. When the 2DHG connect between source and drain, the channel is turned on and current can be detected.

In our research, we define the turn-on voltage to be the gate voltage when I_{SD} reaching a certain threshold current (3 nA for following measurement). Once the current reach this value in a down-scan, the corresponding voltage is recorded as the Turn-on Voltage (V_{on}) of that sweep.

Note that there are two differences from the common experimental condition. Firstly, in common experiments for quantum dot array we usually do not sweep all gates together, especially the screening gates. However, at the first stage of the experiment we mostly focus on the hysteresis phenomenon itself, so those gates are combined for convenience.

Besides, the definition of turn-on voltage is different from the typical definition with the x-axis intercept of turn-on IV curve's linear fit. It is also for the sake of convenience: For many experiments in this research, sweeping of gate voltage needs to stop at a threshold current, e.g.detection sweeps, so a full turn-on curve is hard to obtain. This definition will only cause a limited difference in turn-on voltage (tens of mV) from the typical method, and doesn't lead to meaningful effect.



(a) (b)

Figure 4.9: (a) The layout of the involved gates. (b) A demonstration measurement of drift of turn-on voltage. Here, the combined gates in the sensor were swept from 0 mV to −1400 mV, back and forth for 4 times. Each sweep are composed of a down-scan towards negative (solid line) at first, and an up-scan towards positive (dotted line) later. By repeating the sweep, the V_{on} were gradually pushed more negative. (unit of combined gate: mV)

Before the measurement shown in Fig 4.9(b), the turn-on voltage of combined gates is initialized at -880 mV. Then the combined gates are swept from $V_{max} = 0$ mV to $V_{min} = -1400$ mV (down-scan) and back (up-scan), repeated for 4 times. As result, in each sweep the channel can be turned on in the down-sweep, but as the sweeps repeating, the turn-on voltage drifts towards negative.

Voltage Range	V_{max}	0	0	0	0
	V_{min}	-1000	-1200	-1500	-1600
V_{on}	1	-670	-1010	-1185	-1350
	2	-940	-1120	-1300	-1360
	3	-975	-1150	-1330	-1390
	4	-980	-1170	-1350	-1370
	5	-990	-1170	-1350	-1390
	6	<-1000	-1180	-1360	-1400

Table 4.2: Drift of V_{on} with sweeping from 0 to different choice of V_{min}. For each V_{min}, result from 6 sweeps are shown. The tests went in a column-major order. (Voltage unit in mV)

The experiment in Table 4.2 further shows the effect of varying V_{min}. This experiment started right after the dipping and followed the same procedure as Fig 4.9(b). For each choice of V_{min}, sweeps are done 6 times and their turn-on voltage are recorded in columns of the table. After that, the measurement with next choice of V_{min} is conducted. As result, the turn-on voltage naturally initialized at -670 mV (The first measurement right after dipping), and during the sweeps the turn-on voltage clearly drift toward negative and getting closer to V_{min}.

Voltage Range	V_{max}	500	500	1000	1500	1550	1600	1600
	V_{min}	-1600	-1500	-1500	-1500	-1500	-1500	-1200
V_{on}	1	-1330	-1330	-1240	-1100	-1090	-1060	-1060
	2	-1330	-1330	-1240	-1110	-1080	-1060	-1040

Table 4.3: Reversing the drift of V_{on} by positive choice of V_{max}. Test order are same as above. (Voltage unit in mV)

As shown in Table 4.3, positive choices of V_{max} were also tried. Two observations can be found in these results: Firstly, the drift can be reversed by sweeping the gate voltage to positive V_{max}. With same V_{min}, higher V_{max} can bring back the turn-on voltage to less negative value. Secondly, the turn-on voltage stay nearly unchanged when repeat the sweeps. This is different from the results in Table 4.2, as the turn-on voltage drift to more negative value as the sweep repeated.

These results can be easily understood by the trapping and detrapping process in the device: When negative gate voltage is applied and 2DHG is populated, traps in the surface will be filled under surface tunneling. When positive gate voltage is applied, the detrapping process will be induced and the turn-on voltage recovered to a less negative value. When we repeat the sweeps with positive V_{max}, there is a competition between the trapping process under on-state negative voltage and detrapping process under positive voltage. A balance is struck between these two processes, result in a fixed turn-on voltage.

Measurement in other devices

In all three tested devices, similar results of the reversible drift were observed. For different devices, different threshold current were assigned from observation to define the turn-on voltage.

4.2.2 "Balance Table": V_{on} as function of sweeping range

To further characterize and compare the effect of positive and negative sweeping in a more comprehensive way, we measured the turn-on voltage as a function of voltage range of sweeps. In this experiment, turn-on voltages with different combinations of V_{max} and V_{min} were measured.

Since hysteresis effect is a significant factor for this experiment, order of the measurements should be carefully designed to ensure the reliability of the results. Hence, for each combination of V_{max} and V_{min}, the sweep was repeated 3 times. All the 3 turn-on voltages from the same range were recorded together in one cell of the table. In this way, the results are more depend on the present voltage range instead of the previous voltage range. The stability of the results can also be observed by comparing different sweeps with the same range. At the end of the experiment, V_{min} was switched back to -1300 mV to observe if there is history dependence in this effect.

$V_{min} \backslash V_{max}$	-500	0	300	600	900	1200	1500	1800	2100
-800	-	-	-	-	-	-	-	-	-
	-	-	-	-	-	-	-	-	-
	-	-	-	-	-	-	-	-	-
-1000	-1000	-	-	-	-	-	-1000	-1000	-990
	-1000	-	-	-	-	-	-1000	-1000	-990
	-	-	-	-	-	-	-1000	-1000	-990
-1200	-1010	-1170	-1180	-1160	-1100	-1060	-1030	-1020	-990
	-1120	-1180	-1180	-1150	-1100	-1050	-1030	-1010	-990
	-1160	-1190	-1190	-1150	-1100	-1050	-1030	-1010	-990
-1400	-1110	-1320	-1290	-1240	-1210	-1160	-1090	-1040	-1010
	-1270	-1330	-1290	-1230	-1210	-1160	-1080	-1040	-1000
	-1310	-1340	-1290	-1240	-1210	-1160	-1090	-1050	-1000
-1600	-1260	-1420	-1410	-1390	-1350	-1270	-1170	-1120	-1060
	-1380	-1430	-1420	-1400	-1360	-1270	-1170	-1120	-1060
	-1400	-1440	-1420	-1410	-1360	-1270	-1180	-1120	-1050
-1800	-1390	-1590	-1590	-1560	-1470	-1360	-1270	-1200	-1140
	-1510	-1620	-1600	-1560	-1470	-1380	-1270	-1200	-1150
	-1560	-1630	-1620	-1560	-1460	-1370	-1270	-1200	-1140
-2000	-1530	-1780	-1730	-1680	-1560	-1480	-1360	-1310	-1260
	-1730	-1780	-1740	-1660	-1560	-1470	-1370	-1310	-1250
	-1760	-1790	-1740	-1670	-1580	-1460	-1370	-1310	-1250
Back to -1300									
-1300	-1220	-1280	-1300	-1300	-1290	-1270	-1250	-1230	-1200
	-1250	-1290	-1300	-1300	-1290	-1270	-1250	-1230	-1190
	-1270	-1300	-1300	-1300	-1290	-1260	-1240	-1220	-1180

Table 4.4: The turn-on voltages measured as a function of sweeping range in the experiment. For each combination of V_{min} and V_{max}, sweeps were repeated 3 times to obtain the stable result. 3 results of the same voltage range were listed from up to down in one cell of the table. For the whole table, V_{max} was first varied along each row direction. Except for the grey region that indicates no turn-on in the sweep, three regimes were identified in the table. Red: Negative Dominated Regime; Yellow: Balanced Regime; Green: Positive dominated regime. A test back to $V_{min} = -1300mV$ is presented at the end of experiment. Its last cell is in Balance Regime by default, since it's hard to be compared with other ranges. (Voltage unit in mV)

The measurement results in Table 4.4 clearly shown that both V_{max} and V_{min} of sweeps can affect the turn-on voltage. Except for the grey region on top of table (No turn-on observed in the sweep), three regimes can be distinguished in the table:

- **Negative-Dominated Regime.** The value of turn-on voltage is dominated by effect from negative voltage experienced by device. As displayed in red region in the table, the turn-on voltage lose balance and keeps drifting negative even in different sweeps of a single cell (same range of sweep).

- **Balanced Regime.** The value of turn-on voltage is both affected by positive and negative voltage experienced by device and balance can be struck between these two processes. As displayed as yellow region in the table, the turn-on voltages are stable with the same range and show expected difference with neighboring cells. The turn-on voltage are more negative with more negative V_{min}, or less positive V_{max}, vise versa.

- **Positive-Dominated Regime.** The value of turn-on voltage is dominated by effect of positive voltage experienced by device. As shown in green region in the table, the turn-on voltage is pulled back to similar value even if it went to more negative V_{min}.

This measurement, namely "balance table" measurement, provides us with a very direct angle to understand how turn-on voltage can be affected by choice of voltage range. The first observation is the high regularity and stability of the result. It is shown that even a positive sweep with a very small voltage (+300 mV) can start to have an effect and strike a balance with that of negative experience.

Besides, clear gradient can be shown between different choices of sweep range, which implies that manipulating the turn-on point by control the sweep range is highly feasible in this device. This feature also makes the balance table measurement a direct characterization of the tunability of the turn-on voltage of a device.

Moreover, a subtle point worth to be noticed is that stable turn-on voltage can be achieved just by the first sweep of a cell (3 measurements with same range) in the balanced regime. For each cell of results, the first sweep usually starts with a more negative turn-on voltage remain from the past sweeps, compared with the other two later sweeps. Surprisingly, once switch to a more positive V_{max}, the turn-on voltage gets to the stabilized value early in the first sweep. Stable control of turn-on voltage is therefore possible.

However, the special test in the last row of the table shows that history-dependent factor exists in the mechanism behind turn-on voltage. After all these experiments above, the V_{min} was set back to -1300 mV, but the turn-on voltages didn't recover immediately. As shown in the last row of Table 4.4, its turn-on voltage with same V_{max} appears even higher than the row with $V_{min} = -1400$ mV, serving as an indicator of history-dependence behavior. In section 4.3.3 and 4.3.4 we will investigate the mechanism behind this phenomenon.

Measurement in other devices

As balance table measurement can be used to characterize the tunability of the turn-on voltage of the channel, it was done in all three tested HFETs. Although general patterns are similar for all devices, minor differences were still found. For RB and RT sensor in Batch 4 Dev 7, the Negative-Dominated regime is broader and even includes some sweeps with small positive V_{max}. Especially for the RB sensor, the gradient along a row is small: different V_{max} can only make a small difference for turn-on voltage. Compared to RT sensor of Batch 4 Dev 5, their tunability is therefore weaker. Fortunately, this difference doesn't hinder the manipulation of turn-on voltage. Thanks

to the feedback control, the weak tunability can be compensated by just automatically applying more positive V_{max}. More detail for this will be discussed in Section 4.3.

4.2.3 V_{on} as function of waiting time at positive voltage

Besides the voltage range of sweeping, another variable we can control is the duration time of applied voltage. Following the same measurement procedure as before, sweeps with the same voltage range but different waiting times at V_{max} are also made.

It's worth noting that these results come in a series of measurements that the waiting time increased in one way. Similar to the balance table experiment, different order of measurements also shows history dependence: Coming back from longer t_{max} to shorter t_{max} will result in less negative turn-on voltage than before. Therefore, uniquely calibration of the effect of waiting time is impossible and this test only made to show a general trend.

V_{max}	1600	1600	1600	1600	1600	1600	1600
t_{max}	30	60	120	180	300	900	1800
V_{min}	-1200	-1200	-1200	-1200	-1200	-1200	-1200
t_{min}	0	0	0	0	0	0	0
V_{on}	-850	-820	-780	-760	-730	-680	-650

Table 4.5: Turn-on voltage in sweeps with same voltage range but varied waiting time at V_{max}. (Voltage unit in mV, time unit in seconds)

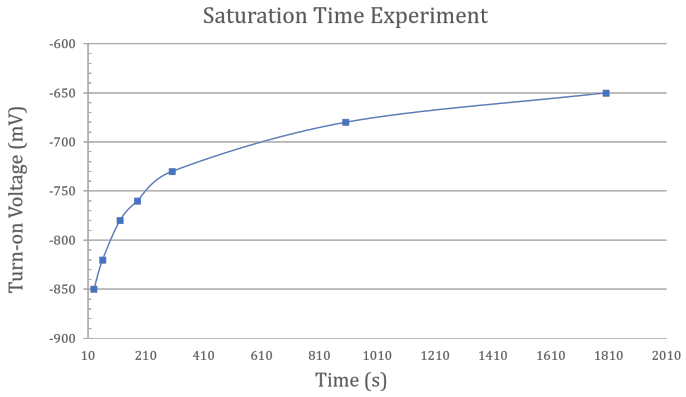


Figure 4.10: Turn-on voltage versus waiting time at V_{max} with fix range of sweep. The result show a clear exponential behavior.

The measurement results are shown in Table 4.5 and Fig 4.10. The first observation is the clear exponential dependence on waiting time, as the exponential fit gives $V_{on} = -1019.2 + 49.755ln(t_{max})$ mV with $R = 0.9979$, indicating the exponential behavior of the detrapping process. Besides, we notice that the saturated turn-on voltage with enough length of t_{max} is very close to the first turn-on voltage measured right after dipping (670 mV), also indicates a thorough detrapping by staying at the positive voltage for enough time. However, as this time scale is too long for practical use, we mainly prefer higher voltage for faster reversal of drift and waiting time is only used as a secondary variable.

4.3 Automatic feedback control of V_{on}

Based on the reversibility of drift demonstrated in Section 4.2, a natural idea could be utilizing this reversibility to control the turn-on voltage of a channel. The significance of doing this, however, is more than turning on a channel itself.

Firstly, it can free us from tedious resetting operations like thermal cycling. The duration time of experiments can thus be almost infinitely extended without being interrupted. Consequently, every experiment can be done in an automatic and efficient manner. The controlling method is describe in Section 4.3.1 and 4.3.2.

Secondly, the control of turn-on voltage will provide us with a powerful and convenient platform to investigate the electrical characteristics of the device with desired and well-controlled initial conditions. Therefore, lots of interesting experiments that sensitive to initial conditions then become possible and repeatable. The experiments demonstrated in Section 4.3.3 and Section 4.3.4 benefit from this advantages.

Most important of all, from these controlled-variable experiments, we can get a deeper insight into the physical mechanism behind the behaviors of turn-on voltage shift. A hypothetical physical model, namely the "Coin Pusher Model", is proposed as a possible explanation for the observed results, as shown in Section 4.4.

4.3.1 "Touch and back" sweeps: Nearly non-demolition detection of V_{on}

Reliable control always needs reliable input. Before we go to the control of turn-on voltage, there is one more step to go: to have a trustworthy detection of the turn-on voltage. It is not unreasonable to worry about detection. As demonstrated in Section 4.2, we cannot detect a turn-on voltage until we actually turn it on. However, once the channel is turned on, drift takes place and the turn-on voltage is changed. Therefore, a non-demolition detection of turn-on voltage is needed.

In order to figure out the minimum effect of measuring the turn-on voltage, the "Touch-and-back" sweeps are designed. In such sweeps, the sweeping of gate voltage stop immediately when turn-on is detected and then swept back to 0. By making this sweep successively for many rounds, the influence from the last sweep can thus be determined by the next sweep. In our experiment, 2 series of successive "Touch-and-back" sweeps with initial turn-on voltage at -1010 mV and -1220 mV are made, each contains 30 rounds of sweep.

Attempt	1	2	3	4	5	6	7	8	9	10
V_{on}	-1010	-1020	-1030	-1040	-1060	-1070	-1090	-1100	-1120	-1120
Attempt	11	12	13	14	15	16	17	18	19	20
V_{on}	-1130	-1150	-1150	-1160	-1170	-1180	-1190	-1200	-1210	-1210
Attempt	21	22	23	24	25	26	27	28	29	30
V_{on}	-1220	-1230	-1230	-1230	-1240	-1240	-1250	-1250	-1260	-1270

Table 4.6: To test the minimum effect of measuring the turn-on voltage, the successive "Touch-and-back" sweeps was conducted. Here the turn-on voltage detected in one series of the successive "Touch-and-back" sweeps is shown. The experiment started from initial turn-on voltage -1010 mV. For each sweep in the series, the gate voltage was swept towards negative until turn-on event is detected. Then gate voltage was immediately swept back to zero.

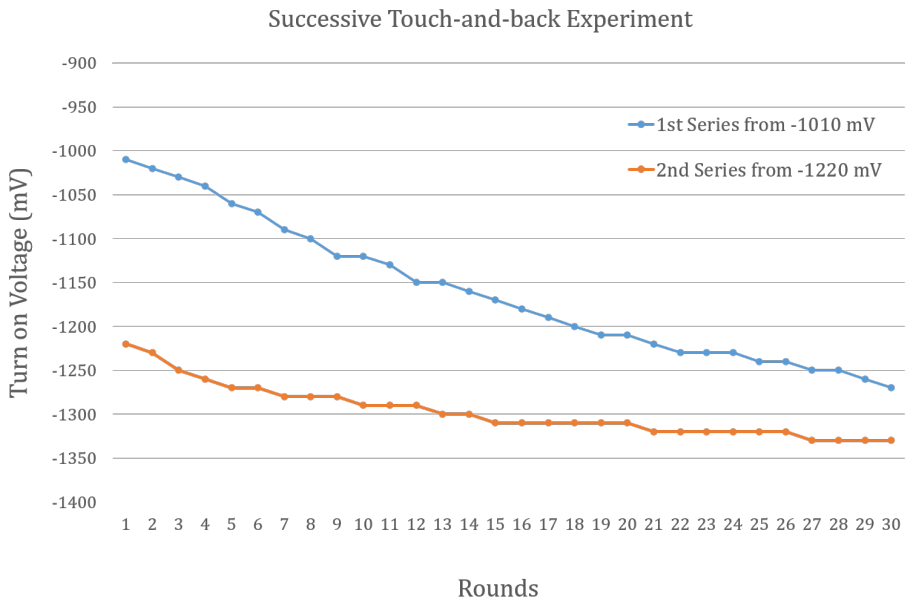


Figure 4.11: To further measure the effect of "Touch-and-back" sweeps on turn-on voltage for different initial value, two successive "Touch-and-back" sweeps as in Table 4.6 were made. It was shown that the successive "Touch-and-back" sweeps only cause small drift of the turn-on voltage, and the drift appears slower for more negative turn-on voltage.

The results from these two series of sweeps were depicted in Fig 4.11 and data from one of the series is also shown in Table 4.6. In this experiment, it was found that the successive "Touch-and-back" sweeps only cause little drift in the turn-on voltage (on average $\leq 10mV$ for one sweep). This can be well understood from the surface tunneling model introduced in Section 2.5. As described in this model, the drift only takes place after charges start to populate in the quantum well and tunnel to the surface. Therefore, in each "Touch-and-back" sweeps the period of formation of 2DHG is very short, thus only little drift of turn-on voltage will be induced in each round. With this property, the "Touch-and-back" sweep provides an approach of nearly non-demolition detection of turn-on voltage. We thus use it as the detection step in the automatic feedback control program in the experiments afterward.

Besides, another interesting observation is the different speeds of drift under successive "Touch-and-back" sweeps. When the turn-on voltage drift to more negative value, the drift under successive "Touch-and-back" sweeps slows down. In section 4.4, this phenomenon will be modelled and explained.

4.3.2 "Turn-on Navigator": Automatic feedback control of V_{on}

Based on all the aforementioned observations, we are now prepared for the control of turn-on characteristics. For this, an automatic feedback control program for turn-on voltage was designed, namely *TurnonNavigator*. Using this program, we can conveniently control the turn-on voltage of the tested HFET devices to almost any desired voltage in the common operation range (roughly -800 mV to -1700 mV for our device).

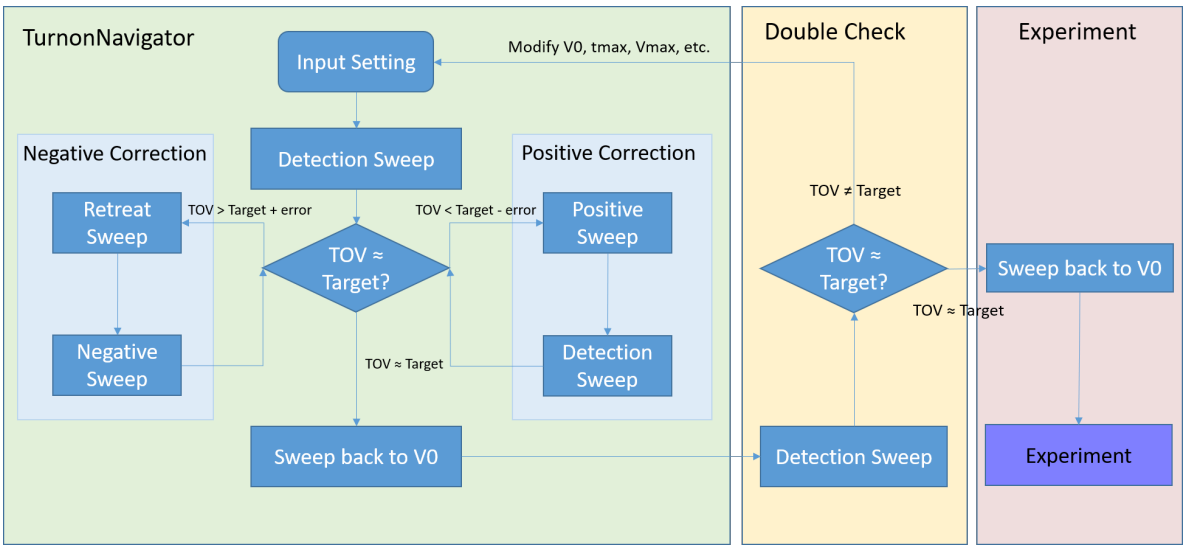


Figure 4.12: A flow chart describing the automatic feedback control program of turn-on voltage. Here, "TOV" stands for the turn-on voltage. The "Double Check" step is optional and mainly used for tests that are sensitive to initial conditions.

Fig 4.12 shows the flow chart of the algorithm of *TurnonNavigator*. Particularly, its full working strategy can be described as follows:

1. **Input Setting.** Firstly, all control parameters were taken as input. These parameters are listed in Table 4.7.

2. **Detection Sweep.** A detection sweep modified from "Touch-and-Back" sweep described at section 4.3.1 is made. In such detection sweeps, the gate voltage is swept towards negative value until detection of turn-on event (current reach $I_{threshold}$) or reaching minimum voltage of detection ($V_{min} = V_{target} - V_{-}$). If turn-on occurs, the difference $V_{target} - V_{on}$ is recorded as correction value. After reaching the turn-on point or minimum voltage, the following conditional correction loop is executed:

   2.1. **No Correction Needed.** When detected correction $|V_{target} - V_{on}| \leq V_{error}$, no correction is needed, sweep gate voltage back to V_0 and end the correction loop.

   2.2. **Positive Correction.** While no turn-on detected or detected $V_{on} < V_{target} - V_{error}$, positive correction is needed.

      2.2.1. **Positive Sweep.** Sweep from where detection stop to a positive voltage V_{max}. This positive voltage is assigned with feedback from accumulative correction: $V_{max} = min[V_{ceiling}, V_{on} + V_{+} + \sum_i \beta(V_{target} - V_{on})_i]$ and wait for t_{max}. Here, i is the times that positive sweep is triggered. Therefore, all correction from previous sweep $\beta(V_{target} - V_{on})$ will add to the feedback, until $V_{on} \geq V_{target} - V_{error}$ is detected.

      2.2.2. **Detection Sweep.** Make detection sweep again to obtain new V_{on}. It will be compared with V_{target} and lead to new conditional operation. If no turn-on was detected for 3 times, return to V_0 and report error.

   2.3. **Negative Correction.** While detected $V_{on} > V_{target} + V_{error}$, negative correction is needed.

2.3.1. **Retreat Sweep.** Sweep from where detection stop to a slightly less negative voltage $V_{on} - V_{retreat}$. (So it can make detection of V_{on} frequently and improve the efficiency of the correction.)

2.3.2. **Negative Sweep.** Sweep towards negative again. When turn-on detected, record the V_{on} and correction. Continue sweep for $V_{penetrate}$ and then wait for t_{min}.

3. **Double Check (Optional).** If $doublecheck = True$, do another detection sweep to ensure the turn-on voltage is still at the desired value. If not, repeat the process above with automatic modified input. Inspired by effects introduced in Section 4.3.3, in the future this step could be replaced by the "Stabilization" step, which parks the gate voltage at a negative off-state value.

Parameter	Explanation
V_{target}	Desired Turn-on voltage
V_{error}	Maximum permissible error of V_{on}
V_0	Original voltage the program start and end at
β	Feedback coefficient for positive correction
$V_{retreat}$	Voltage to retreat in negative correction
t_{max}	Waiting time at V_{max}
t_{min}	Waiting time at V_{min}
V_+	Initial difference from detected V_{on} to next V_{max} (Positive correction)
V_-	Maximum range to detect below V_{target}
$step$	Voltage step for sweeping
$V_{penetrate}$	Voltage continued to sweep after turn-on in negative correction
$V_{ceiling}$	Maximum limit of V_{max}
$I_{threshold}$	Threshold current to define turn-on event
$doublecheck$	Do doublecheck step or not

Table 4.7: Control parameters of the program and corresponding definition of them.

In all three tested devices, the *TurnonNavigator* is shown functioning well and can tune the turn-on voltage to any desired value within common range of operation (-800 mV to -1700 mV). In Section 4.2.2, we have shown that the tunability can be represented by the gradient between neighboring cells in the balance table measurement. Knowing the tunability, one can adjust the control parameters listed in Table 4.7 correspondingly and achieve highly customized and flexible control for certain devices. For example, if the tunability appears low, we can set higher β and t_{max} to compensate, vise versa. By properly choosing those parameters, we can precisely obtain the desired turn-on voltage efficiently, sometimes the correction can even finish with only one or two sweeps.

Making use of this program, we are then able to further conduct lots of interesting experiments on the turn-on characteristics with their initial turn-on voltage well-controlled. For some experiments sensitive to the initial turn-on voltage, a double-check or stabilization step can be added that even the history dependence effect is weakened.

4.3.3 Relaxation and stabilization of adjusted V_{on}

To apply the turn-on manipulation technique, an important question is how stable the result we can get. That is, after adjusting the turn-on voltage, we wonder if the

turn-on voltage will relax to a different value if the voltage is rest at an off-state value for some time. Therefore, it's necessary to monitor the relaxation of turn-on voltage after adjustment. Here, a relaxation characterization experiment is conducted to answer this question.

$V_{on,before}$	-1090	-1100	-1100	-1090	-1090	-1090	-1090
V_{rest}	0	0	0	0	0	0	0
t_{rest}	10	30	60	120	300	1800	7200
$V_{on,after}$	-1110	-1120	-1110	-1120	-1120	-1120	-1120
$V_{on,before}$	-1390	-1380	-1380	-1380	-1400	-1380	-1380
V_{rest}	0	0	0	0	0	0	0
t_{rest}	10	30	60	120	300	1800	7200
$V_{on,after}$	-1370	-1380	-1370	-1360	-1360	-1350	-1340
$V_{on,before}$	-1590	-1580	-1580	-1580	-1580	-1580	-1580
V_{rest}	0	0	0	0	0	0	0
t_{rest}	10	30	60	120	300	1800	7200
$V_{on,after}$	-1440	-1450	-1460	-1480	-1480	-1470	-1460

Table 4.8: Relaxation of turn-on voltage tested from 3 choices of initial V_{on}, each for a series of rest time. The test was executed from left to right in the table. In each test, we choose a combination of t_{rest} and initial value $V_{on,before}$. Firstly, the V_{on} was initialized to $V_{on,before}$. After the initialization, the gate voltage was grounded ($V_{rest} = 0$) for variable time t_{rest}, then the turn-on votlage was measured again to obtain $V_{on,after}$. In this experiment, error of 20 mV is permitted for initialization. (Voltage unit in mV)

Table 4.8 show the result of the relaxation characteristic test. For each combination of initial turn-on voltage $V_{on,before}$ and t_{rest}, we first initialized the turn-on voltage to a target value using *TurnonNavigator* with ±20 mV error permitted. The gate voltage was then swept back to $V_{rest} = 0$, wait for t_{rest} and finally make a detection sweep to obtain $V_{on,after}$.

Counterintuitively, it seems that t_{rest} doesn't make perceptible influence on the $V_{on,after}$. Besides, when we tune the turn-on voltage to a very negative value (For example, -1600 mV), the turn-on voltage after relaxation is significantly less negative, however, it doesn't depend on waiting time either.

These counter-intuitive results, however, provide us with valuable insight into the physical mechanism behind the behavior of turn-on voltage. Provided that the turn-on voltage shift is explained by charge trapping process, two conclusions can be proposed inductively from these observations:

1. For different turn-on voltages after adjustment, different relaxation is observed. This indicates that the amount of occupied traps affects the trapping and detrapping processes. When a large amount of traps are already occupied, the newly filled traps appear more unstable.

2. In certain conditions, at least a part of traps are so unstable that its corresponding detrapping can be completed thoroughly when we sweep back to 0. As a result, turn-on voltage relaxes quickly to less negative voltage right after the adjustment. (e.g. from -1590 mV to -1440 mV) After this, the amount of trapped charges is no longer depends on time, at least within the timescale of 2 hours.

To further explore the mechanism of fast detrapping process mentioned at point 2, a modified version of relaxation test was designed. As shown in Table 4.9.

$V_{on,before}$	-1630	-1630	-1630	-1640	-1640	-1630	-1640	-1640	-1630	-1640	-1630	-1640
V_{rest}	0	0	0	0	-800	-800	-800	-800	0	0	0	0
t_{rest}	10	30	60	120	10	30	60	120	10	30	60	120
$V_{on,after}$	-1510	-1530	-1540	-1530	-1620	-1620	-1620	-1630	-1590	-1590	-1580	-1580
$V_{on,before}$	-1680	-1680	-1680	-1680	-1680	-1690	-1690	-1680	-1680	-1690	-1680	-1690
V_{rest}	0	0	0	0	-850	-850	-850	-850	0	0	0	0
t_{rest}	10	30	60	120	10	30	60	120	10	30	60	120
$V_{on,after}$	-1550	-1570	-1580	-1580	-1670	-1660	-1670	-1670	-1630	-1630	-1620	-1600

Table 4.9: Modified version of relaxation test. The measurement procedure is similar to that described in Table 4.8. However, in the middle of test series we let the gate voltage rest at an off-state negative value instead of zero. It was shown that the stability of the turn-on voltage can be clearly improved after resting at the off-state negative value. (Voltage unit in mV)

In the modified test, we apply the same measurement procedure for very negative initial turn-on voltage and observe similar results of fast relaxation. However, in the middle of the test series, we change the V_{rest} to an off-state negative value between zero and V_{on}. Surprisingly, the stability can be clearly improved in this condition. More surprisingly, even when we switch back the condition to $V_{rest} = 0$, the relaxation is weaken compared to the first test. We thus stabilized the turn-on voltage by resting at negative voltage for a certain period of time.

Similar as before, some conclusions from this result can be deduced:

1. Even without turning on the channel, keeping the applied voltage at a negative value can stabilize the high-negative adjusted turn-on voltage. This indicates that turning on the channel is not the only way of affecting turn-on voltage. As long as negative voltage is applied, the properties (e.g. distribution) of the trapped charges can also be affected.

2. However, after the stabilization, turn-on voltage still relax to slightly less negative value if the V_{rest} changed from low negative voltage back to zero. That indicates at least a part of the traps are stable under low negative voltage but unstable under zero voltage, i.e., they can be naturally detrapped. To keep these traps being filled, a negative voltage might be needed.

3. For 3 choices of initial voltage that shows behavior of fast relaxation (-1600 mV, -1650 mV, -1700 mV), interestingly, the difference between initial turn-on voltage and turn-on voltage after relaxation is similar, i.e. around 120 mV. This can be an estimation of capacity of the traps in the measured structure which is unstable under zero gate voltage.

Measurement in other devices

In RT sensor of Batch 4 Dev 7, similar experiments were done, yielding similar results: when the channel enters high negative turn-on voltage, relaxation occurs and resting at lower negative voltage can stabilize it.

4.3.4 History dependent stability of V_{on}

To further investigate the mechanism behind turn-on voltage, the history dependence test was designed. The idea of this experiment is to initialize the turn-on voltage to the same value but went through different historical paths, i.e., previous turn-on voltage it had. Here, we prepared the same turn-on voltage from three different historical paths and tested their evolution trend under successive "Torch-and-Back" sweeps.

Historical Path			Turn-on Voltage under successive "Touch-and-back" sweeps									
3rd Recent V_{on}	2nd Recent V_{on}	1st Recent V_{on}	1	2	3	4	5	6	7	8	9	10
-1700	-1560	-1240	-1270	-1290	-1300	-1320	-1330	-1340	-1360	-1360	-1370	-1380
-1250	-1500	-1240	-1240	-1250	-1260	-1270	-1270	-1280	-1280	-1290	-1290	-1300
-1400	-1000	-1240	-1230	-1230	-1240	-1240	-1250	-1240	-1250	-1260	-1260	-1260

Table 4.10: The turn-on voltage evolution under successive "Touch-and-Back" sweeps with three different initialization paths. In experiment of each historical path, the turn-on voltage was adjusted with *TurnonNavigator* to different sequences of value, and finally reach the same initial value (-1240 mV). Then the successive "Touch-and-Back" sweeps is applied to measure the stability of the turn-on voltage. The result clearly show its history dependence behavior.

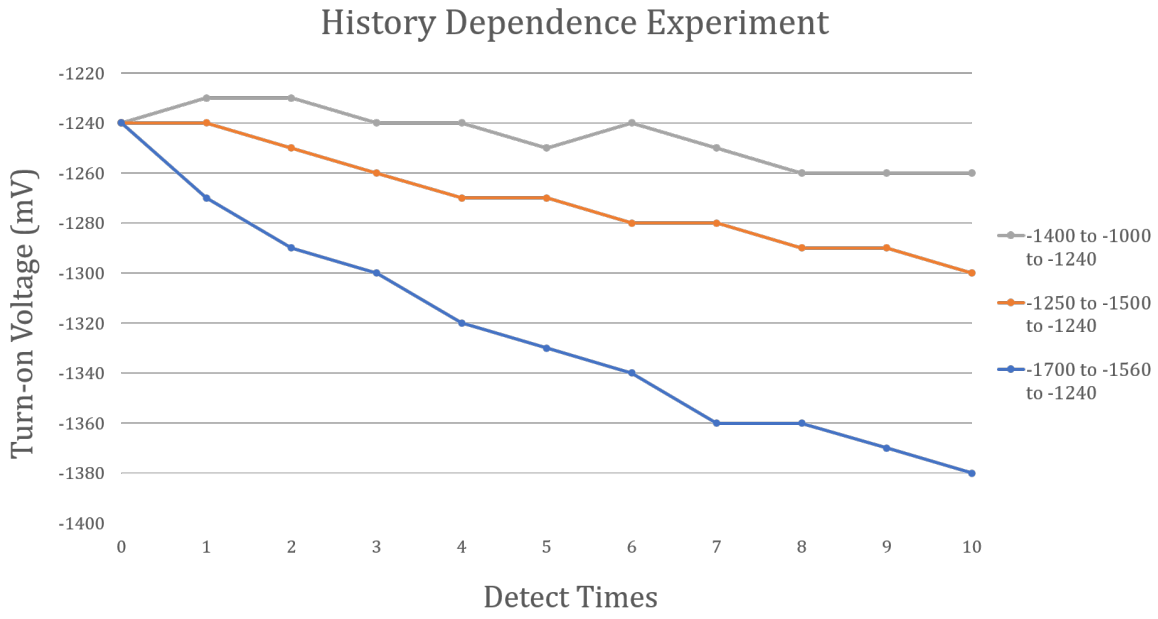


Figure 4.13: Visualization of result in Table 4.10. The turn-on voltage was initialized to -1240 mV from different historical paths (marked as detect time "0"). All these paths are followed by a series of successive "Touch-and-back" sweeps. This chart depicts the evolution of turn-on voltage under such sweeps series as three curves. The result clearly show that different historical path lead to different stability under successive "Touch-and-back" sweeps.

As shown in Fig.4.13, interestingly, even starts from the same initial turn-on voltage, different history paths still lead to clear different evolution under successive Touch-and-Back sweeps. This result indicates the turn-on voltage on its own cannot represent full information of the system.

A possible explanation for this can be the different distribution of trapped charges caused by the different history values of turn-on voltage. These different distributions might lead to different stability under successive Touch-and-Back sweeps.

4.4 "Coin Pusher Model": Hypothetical physical model for reversible drift

4.4.1 Assumptions for the model

Inspired by the aforementioned results in Section 4.3.1 - Section 4.3.4 and related research works [51–62], a hypothetical physical model namely **"Coin Pusher" model**, is proposed as a possible explanation for the observed behavior of turn-on voltage shifts. This model is based on three assumptions:

- **Assumption 1:** Traps are distributed with different trapping time constant in the device.

  Motivation: This assumption can be attributed to different physical origins or properties of traps in the device. For example, traps can be distributed with different spatial locations of the surface like interface and border [51, 52, 55, 57, 61], or different capture cross-sections due to the disordered oxide states [52, 60]. All these factors might effectively result in different time constant of the trap. Especially for the Si cap in our device, traps might be originated from multiple location, including Si/SiO_2 interface, $SiO_2/SiGe$ interface or SiO_2/Al_2O_3 interface [40], acting as a possible origin of traps with different time constant.

  Besides, it is worth to notice that enormous research works have been made to investigate the existence of traps with different trapping and emission time constants [52, 54, 55, 58, 59, 62], or even reversible and irreversible traps [56] to explain the instability of threshold voltage in the MOSFET devices. Under this circumstance, it is reasonable to assume traps with different time constant also in our research. For simplicity, we assume a correlation between trapping and detrapping time constant.

- **Assumption 2:** The amount of traps with a certain range of time constant can be considered finite in our experiment.

  Motivation: When traps have distribution with respect to time constant, it is very natural to make this assumption. It means that traps with a range of time constant are possible to be mostly or completely filled in the experiment and become unavailable. Also this is assumed in most mentioned research works above. With this assumption, we draw traps with different range of time constant as columns of the same size in the schematics of the model (Fig.4.14). Note that this is not accurate and only for simplicity of demonstration.

- **Assumption 3:** At least a part of traps are very unstable, such that charges cannot be kept inside without enough negative voltage and emission occurs within the timescale of the sweeping.

  (*Strong assumption*): These traps are distinctly different from others. A possible reason is that they are located at the interface of oxide while others are inside. This will lead to their differences in stability and time constant.

  (*Weak assumption*): These traps are not distinctly different from others, i.e., their instability just originate from distribution of energy or time constant.

  Motivation: The traps in the assumption are supposed to have two properties: unstable without enough negative voltage and quick emission. From assumption 1, the distribution of time constant is assumed, which also naturally includes traps

with very short time constant. Besides, the instability without enough negative voltage might be associated with the in-gap traps with energy lower than quantum well at zero gate voltage. They can be filled when a negative voltage is applied, but emit quickly when the negative voltage is removed. In the schematic below, this part of traps is depicted with green color. A possible origin for these traps might be the interface states in the semiconductor-oxide interface [55], which is distinctly different from the border traps inside the oxide layer. However, to be careful, in this model we take the weak assumption and keep reservation about whether two essentially different categories of traps are distinguished or not. Both two assumptions can lead to observed results in this research. In the future, more experiments could be done to improve this model.

4.4.2 Model for drift and decay

Based on these assumptions, we can now start to introduce the model, following the observations of the aforementioned experiments. A schematic of trap distribution of initial state of the device is depicted in Fig 4.14, with all traps are empty and $V_{on} = -650$ mV. In this schematic, traps with a longer time constant ("Slow" Traps) are depicted on the left side. The unstable traps mentioned in Assumption 3 are colored with green on the right side. Note that this schematic is only depicted for simplicity, and we don't assume neither same amount of traps with different time constant nor essential difference between fast and slow traps.

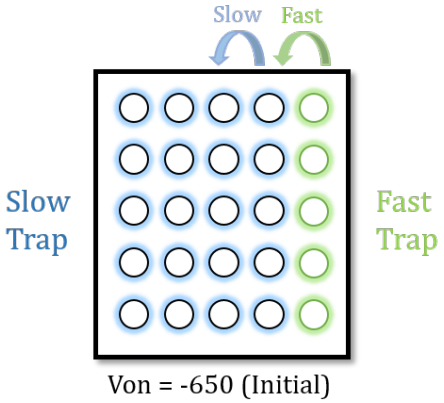


Figure 4.14: Simplified schematic of traps in the device. Traps on left side have higher time constant. The unstable traps mentioned in assumption 3 are colored with green on the right side. As reference, this diagram show the initial condition with no trap filled and $V_{on} = -650$ mV.

To better introduce this model, an example process of drift from $V_{on} = -800$ mV to $V_{on} = -1150$ mV and a decay process afterwards, are demonstrated in Fig 4.15. In step-by-step, they can be described as follows:

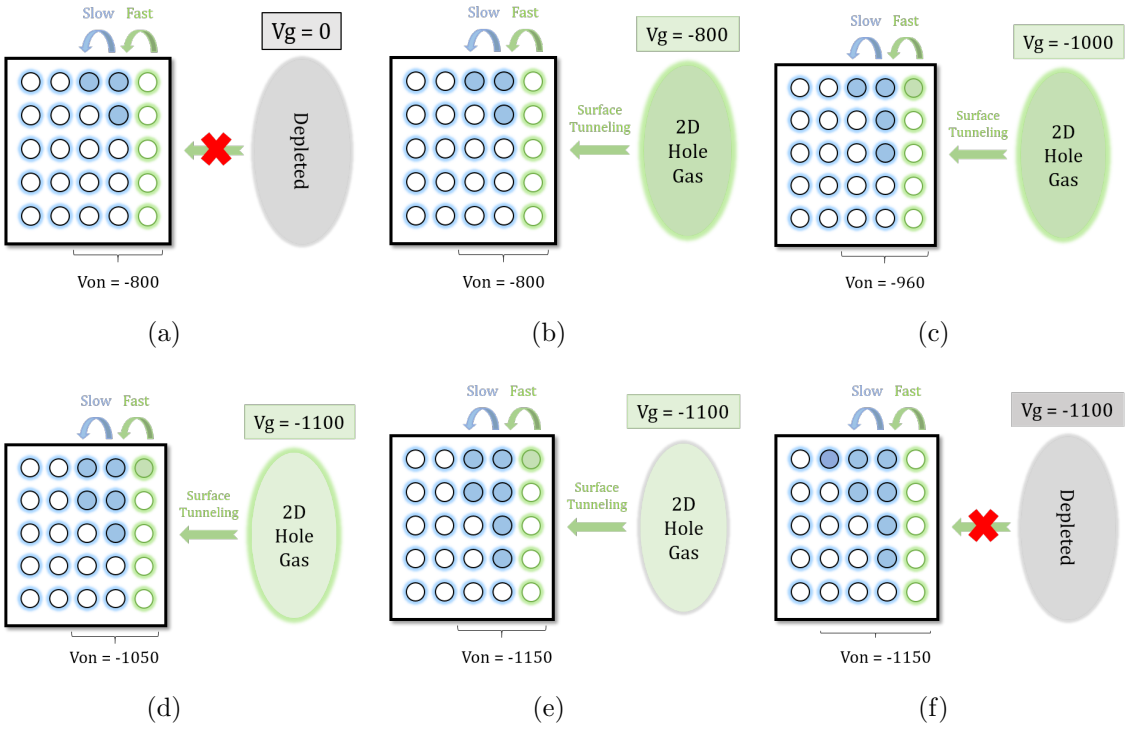


Figure 4.15: A demonstration of drift and decay process in the model. Physical process of each sub-figure is described below. (Voltage unit in mV)

1. Initially, some traps are occupied and the gates are grounded. These trapped charges will screen the electric field from the gate and the turn-on voltage is more negative than that of fresh device. Here the device has V_{on} = -800 mV. (Fig 15(a))

2. When we sweep the gate voltage below turn-on voltage, the 2DHG starts to be populated under the process described in section 2.5.1. (Fig 15(b))

3. Once 2DHG exist, its disequilibrium with the surface will cause surface tunneling. Traps are being slowly filled in process with negative feedback, as described in section 2.5.2. Traps with shorter time constant have higher priority to be filled. However, the time constant of the fast traps is too short that their charges quickly transfers into slower traps. (Fig 15(c))

4. As surface tunneling continues, more traps are being filled. Meanwhile, charges detrapped from faster traps and re-trapped into slower traps. The turn-on voltage of channel drifts toward negative when traps being filled. (Fig 15(d))

5. If we stop sweeping gate voltage and fix it at on-state (e.g. -1100 mV in the figure), the surface tunneling will temporally continue since 2DHG still exist. In this case, the surface tunneling gradually depletes the 2DHG and also increases the turn-on voltage. A current decay can be observed in the channel. The 2DHG doesn't immediately disappear, as we define the turn-on voltage will a threshold current, so the point of complete depletion is actually slightly below that current. (Fig 15(e))

6. Finally, the 2DHG is depleted as current decay to zero. Surface tunneling therefore stops and no new trap is being filled. (Fig 15(f))

Note: It seems that the time constant of "green" traps are essentially different from the rightmost "blue" traps as charges can accumulate in the latter. However, this is a simplified schematic, and under the weak assumption we don't assume a distinct difference between them.

4.4.3 Model for relaxation and stabilization of adjusted V_{on}

Under this model, the different relaxation effect observed after adjusting turn-on voltage to different values (Section 4.3.3) can be understood. The model of it is demonstrated in Fig 4.16, with the distribution of trapped charge corresponding to different turn-on voltage. Again, here we analyze the model following each figure:

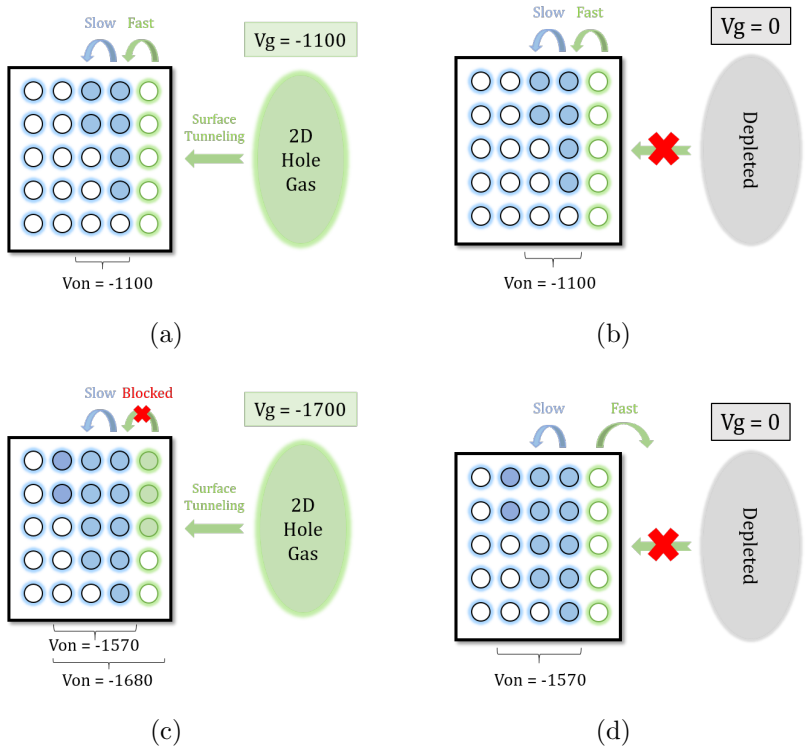


Figure 4.16: A demonstration for different relaxation of low (-1100 mV) and high (-1680 mV) adjusted turn-on voltage in the model. Physical process of each sub-figure is described below. (Voltage unit in mV)

1. For low negative turn-on voltage (-1100 mV), a small amount of traps are occupied. If this turn-on voltage was tuned from a less negative value, deeper traps are rarely filled. (Fig 4.16(a))

2. Consequently, the occupied traps are more stable when the gate voltage back to zero. No detrapping take place in this process. (Fig 4.16(b))

3. For high negative turn-on voltage (-1680 mV), relatively more traps are occupied. If this turn-on voltage was being tuned from less negative value, charges fully occupy from fast to slow traps. Under negative gate voltage, large amount of slow traps are full and "traffic jam" happens. As a consequence, some charges are stuck in fast traps and cannot move to slow traps on time. (Fig 4.16(c))

4. Once the gate voltage back to zero, the detrapping of fast traps occurs quickly. In contrast, the deeper traps can survive for very long time in this case. Therefore, turn-on voltage is immediately recovered to a less negative value. (Fig 4.16(d))

Within this context, another interesting result in section 4.3.3 is that parking the gate at a less negative "off" state voltage can stabilize the adjusted turn-on voltage, even if it's highly negative. To explain this effect, the corresponding physical process is demonstrated in Fig 4.17:

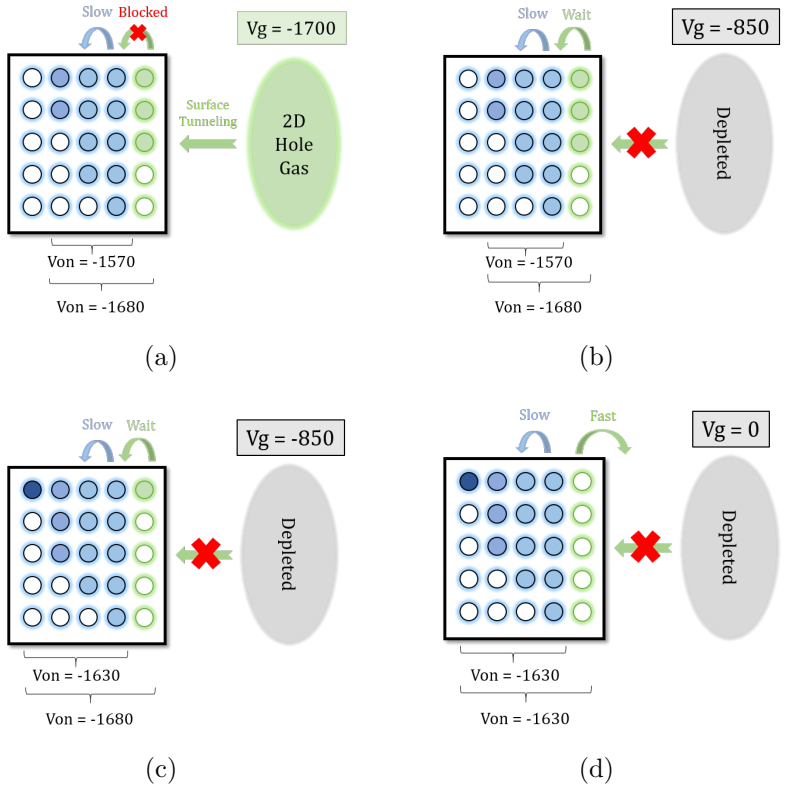


Figure 4.17: A demonstration of stabilization of adjusted high turn-on voltage (-1680 mV) in the model. Physical process of each sub-figure is described below. (Voltage unit in mV)

1. We consider the same starting point as before: the turn-on voltage is adjusted to -1680 mV. (Fig 4.17(a))

2. Different from Fig 4.16(d), after the turn-on voltage was adjusted to -1680 mV, we park the gate voltage at -850 mV instead of zero. In this case, the 2DHG is not formed, so no surface tunneling and no new charge come in. (Fig 4.17(b))

3. Although the 2DHG is not populated, in this case there is still an electric field towards the surface. Therefore, the emission of the fast trap is also suppressed and charges at the fast traps can "wait in line". After waiting for some time, they can eventually move to slower traps. As another possible interpretation, the applied electric field could force charges to migrate deeper if the distribution of time constant is attributed to the spatial location of traps [55]. (Fig 4.17(c))

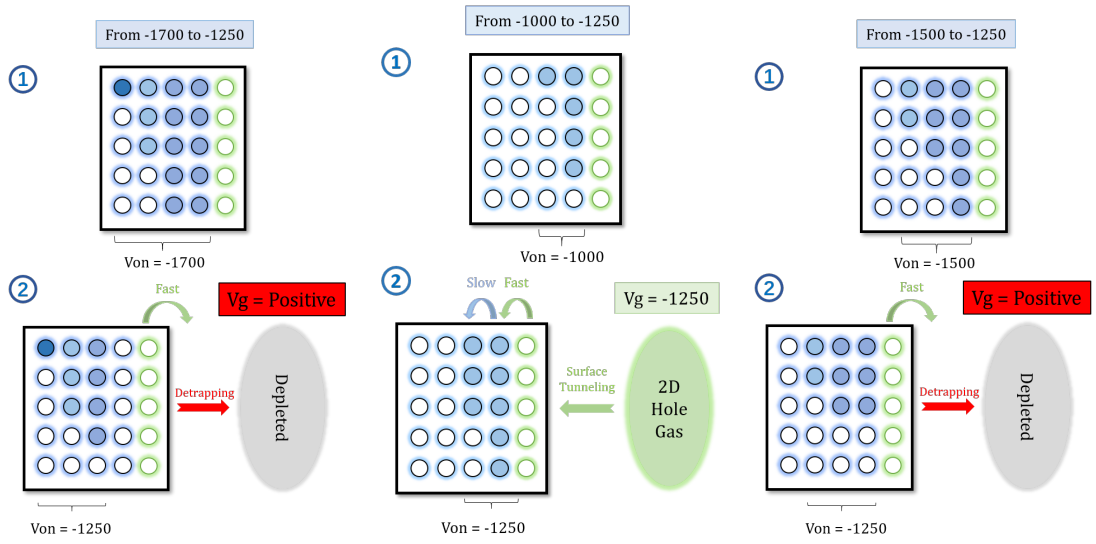
4. As charges in fast traps got into the slower traps, the turn-on voltage appears more stable when gate voltage back to zero. However, some charges are still in the fast traps as it might need more time to find a vacancy. At zero gate voltage,

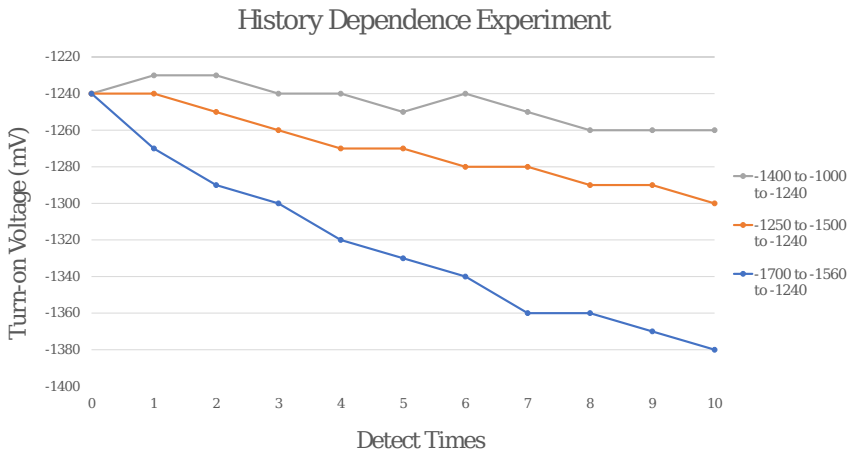
these charges are cleaned, result in a slight recovery to less negative turn-on voltage.(Fig 4.17(d))

As a recap, we mentioned in section 4.3.2 that for negative correction sweeps, the gate voltage is retreated to a slightly less negative value instead of going back to zero. Its motivation can be understood in effect shown above: if we go back to zero after every negative pushing, charges in fast traps are lost, without enough time for them to get into slower traps. In this case, negative correction would turn out to be very hard.

4.4.4 Model for history dependent stability of V_{on}

Another interesting phenomenon is the history dependence effect found in section 4.3.4. This effect is one of the strongest evidence of the distribution of time constant of traps. Similarly, its physical model is depicted in Fig 4.18 and analyzed as follows:





(d)

Figure 4.18: (a-c) A demonstration of history dependence effect in the model. Physical process of each sub-figure is described below. (d) Recap of the result in section 4.3.4. Different turn-on voltage stability is shown under successive "Touch-and-back" sweeps with different initialization paths in (a-c). (Voltage unit in mV)

1. When the turn-on voltage is highly negative (-1700 mV), massive charges filled from slow to fast traps. Then during the positive correction of turn-on voltage (-1700 mV to -1250 mV) the faster traps are first cleaned, until the remnant charges in slow traps exactly support corresponds to the target turn-on voltage (-1250 mV). Consequently, large amount of fast traps are free and more charges can be gradually added to stable traps from Touch-and-Back sweeps. This results in faster drift in successive Touch-and-back sweeps. (Fig 4.18(a))

2. When the turn-on voltage is less negative (-1000 mV), only few traps are filled and they are mostly faster traps. Then during the negative correction (-1000 mV to -1250 mV), charges gradually move to slower traps until charge density is enough for target turn-on voltage. Consequently, trapped charges are mainly contributed by faster component, and less space will be accessible for new charges. This results in slower drift in successive Touch-and-back sweeps. (Fig 4.18(c))

3. For the medium path (-1500 mV to -1250 mV), the condition is similar to the path from higher turn-on voltage. However, as the turn-on voltage has been to -1500 mV, medium amount of slow traps are filled. Therefore, when the charge density supporting target turn-on value is reached, the amount of free fast/slow traps is between the above two cases, result in an intermediate evolution trend. (Fig 4.18(b))

With this model, it is also easy to understand the non-uniform drift observed in successive "Touch-and-back" experiment. Remember that in section 4.3.1, we observed that the turn-on voltage drift under successive "Touch-and-back" sweeps is faster with small turn-on voltage, but gradually slow down with high turn-on voltage, as shown in Fig 4.19:

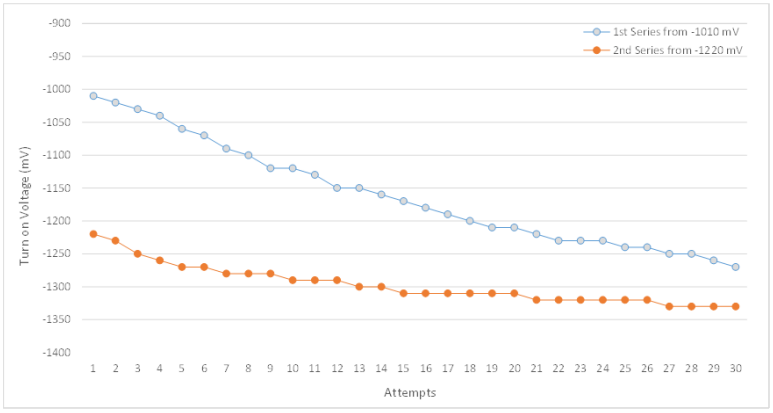
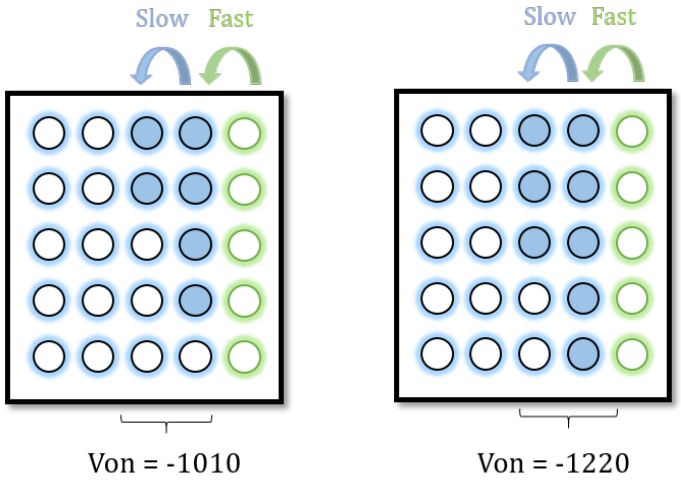


Figure 4.19: A recap of non-uniform drift shown in section 4.3.1.

This can be explained by the distribution-dependent accessibility of new coming charges. Fig 4.20 gives a simple model of the observation. During the successive "Touch-and-back" sweeps, traps are keep being filled and becoming less accessible to new coming charges. When turn-on voltage drift to more negative, new coming charges are more likely wait in the fast traps in the on-state, and escape when the gate voltage is swept back. Therefore, less charges can be actually kept in the traps, so the drift is slower.



(a) (b)

Figure 4.20: (a) For lower negative turn-on voltage, more vacancies are available in fast traps, making it more accessible for new tunneled charges. (b) For higher negative turn-on voltage, fewer vacancies are available in fast traps, making it less accessible for new tunneled charges. (Voltage unit in mV)

4.5 Local manipulation of the threshold voltage

From the experiment shown above, we have discovered the hysteresis behavior of turn-on voltage in HFET and utilized it to control the turn-on voltage in such devices. Further, we also proposed a physical model to understand the observed effects.

To employ this effect to real application scenarios, there is still one step to go. In the aforementioned experiments, all the gates involved were combined and swept together. This manner, however, is only used to investigate the properties of the hysteresis effect itself. In actual quantum dot experiments, separate and finely control of gates are usually required in order to produce a well-defined quantum dots. Besides, due to the capacitance coupling between gates and shared barriers between dots, cross-talk is very common in multi-dot devices, making them much more complicated than the structure under our study.

Within this context, local control of the turn-on voltage is desired for application. For this, we need to define and control the turn-on character not only for combined gates but also for single gates. However, the turn-on voltage can only be defined when the channel is turned on by multiple gates. Therefore, in this subsection we define "threshold voltage" for single gates based on the local formation of 2DHG instead of the whole conductive channel. Their difference can be distinguished as below:

- **Threshold voltage**: The voltage needed for a gate to locally support the 2DHG underneath. It can be defined specifically for a single gate. To measure it, we set other gates to the on-state voltage to prepare a conducting channel. Then the voltage of measured gate can be reduced to pinch off the channel, or then increased to recover the channel. The threshold voltage for the single gate is therefore obtained at the pinch-off or recovery event.

- **Turn-on voltage**: The collective voltage needed for a set of gates to populate 2DHG underneath and form the conducting channel connecting source and drain. As the experiments shown above, it can be measured by sweeping these gates together to turn on the channel. It can be regarded as the threshold voltage for a combined set of gates.

4.5.1 Decay suspension test: Verifying locality of surface tunneling effect

To make separate control of the turn-on character possible, we first need a separate definition of it. For this, we have to confirm if the effects studied above are local, i.e., they depend on specific gate we use and no need to involve the whole channel. Unfortunately, we can only turn on a channel as a whole, which need to populate 2DHG under all gates and connect them to form the conducting channel. It is therefore hard to check the locality of turn-on character straightforwardly by turning-on the channel as all gates must be involved. However, there is an interesting idea to verify the locality indirectly: by measuring the locality of current decay.

To understand why this works, let's review the physical mechanism behind current decay again. As introduced in Section 2.5.4, the current decay also origin from the surface tunneling. In particular, when we turn on the channel and 2DHG is formed in the active layer, the buried quantum well is in disequilibrium with the surface and surface tunneling starts to take place.

In this process, the charges in the quantum well are being depleted and the surface-well field also being weaken. Therefore, if we continue increasing the gate voltage, balance will be reached between the populating and tunneling process at some point,

then the carrier density saturate at a constant value. This results in the S-curve in I-V characteristic, followed by the saturation of current. If we stop sweeping the gate and stay in the on-state value after turn-on, the population also stops. However, the tunneling still continues with existence of 2DHG. Consequently, traps are being filled and the effective field applied to the quantum well is keep being weaken. The 2DHG is thus being slowly depleted, result in the current decay in the channel.

From the previous results, we know that the drift of turn-on voltage depends essentially on the amount of occupied traps in the surface. Inspired by this, we can therefore check if the drift is local by checking if the decay can happen locally. Here, we can monitor the decay when applying a high negative voltage locally to single gates but not turn on the whole channel. If the result indicates the decay can be induced solely by 2DHG underneath single gates without full conducting channel, we can confirm the locality of the surface tunneling.

For this, we designed a "decay suspension experiment" as follows:

1. Initialize the system with a certain collective turn-on voltage using method described at section 4.3.2. In experiment shown in Fig 4.21, it was set to -1150 mV.

2. Turn on the whole channel by collectively sweep all gates from zero to a voltage lower than the collective turn-on voltage, here we use V_{min} = -1350 mV. The channel is therefore turned on.

3. Pinch off the channel by reducing the voltage of the chosen single gate to a less negative value , here we set it to -600 mV. Wait for 30s. Although the channel is pinched off, other gates are still applied with V_{min} in th is step, and 2DHG exist underneath them.

4. Sweep back this gate voltage to V_{min} to recover the channel. The current decay is calculated as difference between current before pinch-off and after recovery. If the effect of surface tunneling is local, we can get different decay when different gates is pinched off, based on their influence on the channel.

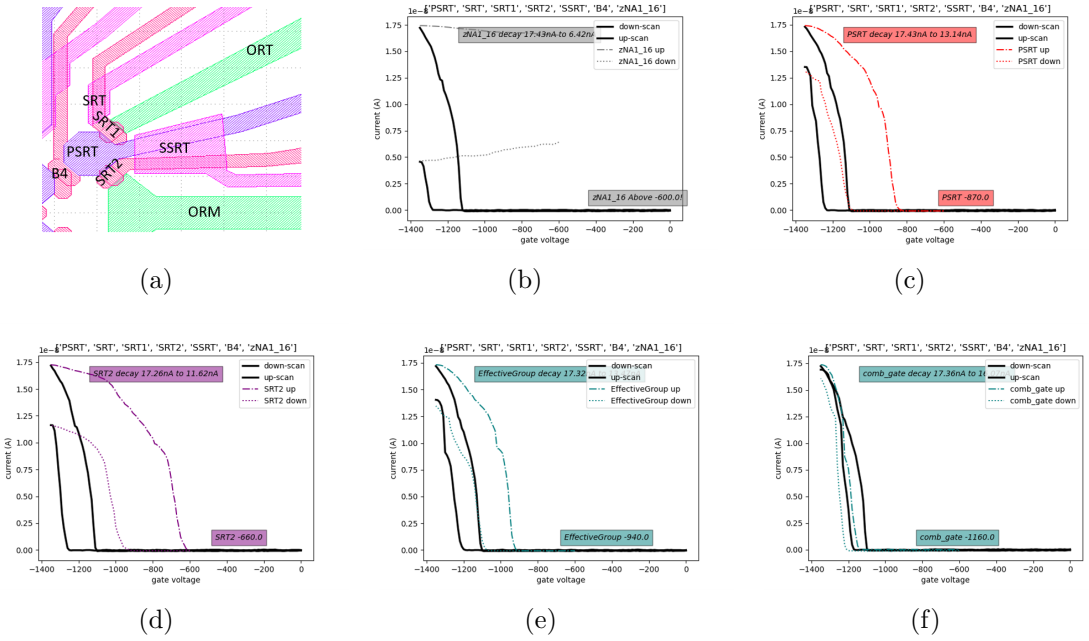
5. Finally, sweep all gates from V_{min} back to zero.

In Fig 4.21 the result with different choices of gate to pinch off is shown. Interestingly, When gates with bigger influence are pinched off, the decay during pinch-off is smaller. The results can be understood as follows:

- When we "pinch-off" the auxiliary gate, which is actually disconnected and has no influence on the channel, we have the largest decay. It's because other gates with full influence are still at V_{min} during the "pinch off", and 2DHG still exists under all of those gates. Therefore, surface tunneling fully continues and largest amount of charges tunnels to the surface during this period. So we observe the largest decay.

- When we pinch off PSRT, which has some influence on the channel, we have medium decay. In this case, other gates besides PSRT are still at V_{min} during its pinch-off. Therefore, 2DHG exists under all gates except PSRT. The surface tunneling thus continues in those regions and some charges tunnels to the surface during this period, which is less than the former case. So we observe medium decay.

- When we pinch off the combined gate (PSRT+SRT2 or all gates combined), we have much smaller decay. In this case, no gates or only a few gates still at V_{min} during the pinch-off. Therefore, regions where 2DHG exist are much smaller and little charges tunnels to the surface during this period. So we observe the smallest decay.



(a) (b) (c)

(d) (e) (f)

Figure 4.21: (a) The layout of gates in RT sensors. (b) - (f) Result of decay suspension test. In each measurement, the combined gate voltage is first swept to a minimum value to turn on the channel (Black solid curve on right). Then a chosen gate is swept to a less negative value to pinch off the channel and wait for 30s (Colored dash-dot curves). After waiting, this gate is swept back to the minimum voltage to recover the channel (Colored dotted curves). The difference between current before pinch-off and after recovery is recorded as current decay in this process. The result of choosing auxiliary gate (b), PSRT (c), SRT2 (d), combination of PSRT and SRT2, (e) and all the involved gates (f) to pinch off are shown.

Current\Gate	Auxiliary	PSRT	SRT2	SRT2+PSRT	Combined Gate
I_{before} (nA)	17.43	17.43	17.28	17.32	17.36
I_{after} (nA)	6.42	13.14	11.62	13.47	16.07
I_{decay} (nA)	11.01	4.29	5.66	3.85	1.29

Table 4.11: Result from decay suspension test. The table show current in channel before the pinch off of the selected gate, and the current after the selected gate is swept back again. Their difference are calculated as decay during the pinch off of selected gate.

From these results, we can clearly confirm the locality of surface tunneling. It shows that decay can take place without existence of conducting channel and is depend on the local gate voltage applied. Also it gives us an approach to evaluate the influence of each gate: the bigger influence a gate has, the smaller decay it will give when we do not pinch it off in the decay suspension test.

Measurement in other devices

This experiment was also done for RB sensor in Batch 4 Dev 7. Similar results was observed.

4.5.2 "Swing" experiment: Reversing threshold voltage of single gates

After verifying the locality of the surface tunneling effect, the next step is to realize local control of single gates, such that each gate has desired trap occupation level. This was found to be difficult, as many methods were attempted but didn't give satisfactory outcome. There are several main challenges for this:

1. **It is hard to define the threshold voltage of single gates by turn-on sweeps.** To define the threshold voltage, we usually need to turn on the channel. However, we cannot turn on the channel by single gates without support from others. A solution might be preparing the other gate slightly under the collective turn-on voltage then turn on with the single gate - by forcing the 2DHG population nearby via capacitance coupling. Unfortunately, it doesn't solve the problem since it's not truly local and depends on too many factors, such as the prepared voltage of other gates.

2. **It is hard to control the threshold voltage of single gates based on pinch-off voltages.** On one hand, to detect a pinch-off voltage (defined as gate voltage when current drops to a small threshold value), one must first turn on the channel, which requires sweeping multiple gate to negative voltage. On the other hand, to utilize the hysteresis effect for a single gate to control the threshold voltage, we must sweep it to positive voltage. Within this context, the detection step conflicts with the control step, as the turn-on process will erase the effect from positive voltage applied to the single gate. Therefore, a reliable control the threshold voltage based on pinch-off voltages is hard to achieve.

3. **Cross-talk between neighboring gates could lead to side effects.** Due to the existence of capacitive coupling between gates, when we apply the positive voltage to single gates, it will affect other gates nearby. In one attempt, we tried to sweep single gates to positive voltage and detect its effect on collective turn-on voltage. It was found that the collective turn-on voltage became less negative afterward, probably because traps under other gates were also cleaned in this process via cross-talk. Therefore, controlling the threshold voltage by applying positive voltage might causes side effect on other gates.

Under this circumstance, the "swing" experiment was designed to overcome these problems. In this experiment, we first turn on the channel with all gate combined, then "swing" one of a single gate voltage to positive value. Then the single gate voltage is swept back to recover the channel, and the re-turn-on voltage in this process can be used to characterized its threshold voltage. This experiment can be described as follows:

1. At first, the collective turn-on voltage was initialized to an assigned value. In experiment shown in Fig 4.22, we set the collective turn-on voltage to be -1150 mV.

2. Turn on the channel by sweeping all gates to V_{min}, which is more negative than collective turn-on voltage.

3. Sweep the single gate to positive voltage V_{max} and wait for 30s, while other gates still stay at V_{min}. It is called "swing" operation.

4. Sweep the single gate back to V_{min} to recover the channel. The re-turn-on voltage of this sweep will be used to characterize the threshold voltage of the single gate.

5. Finally, sweep all gates from V_{min} back to zero.

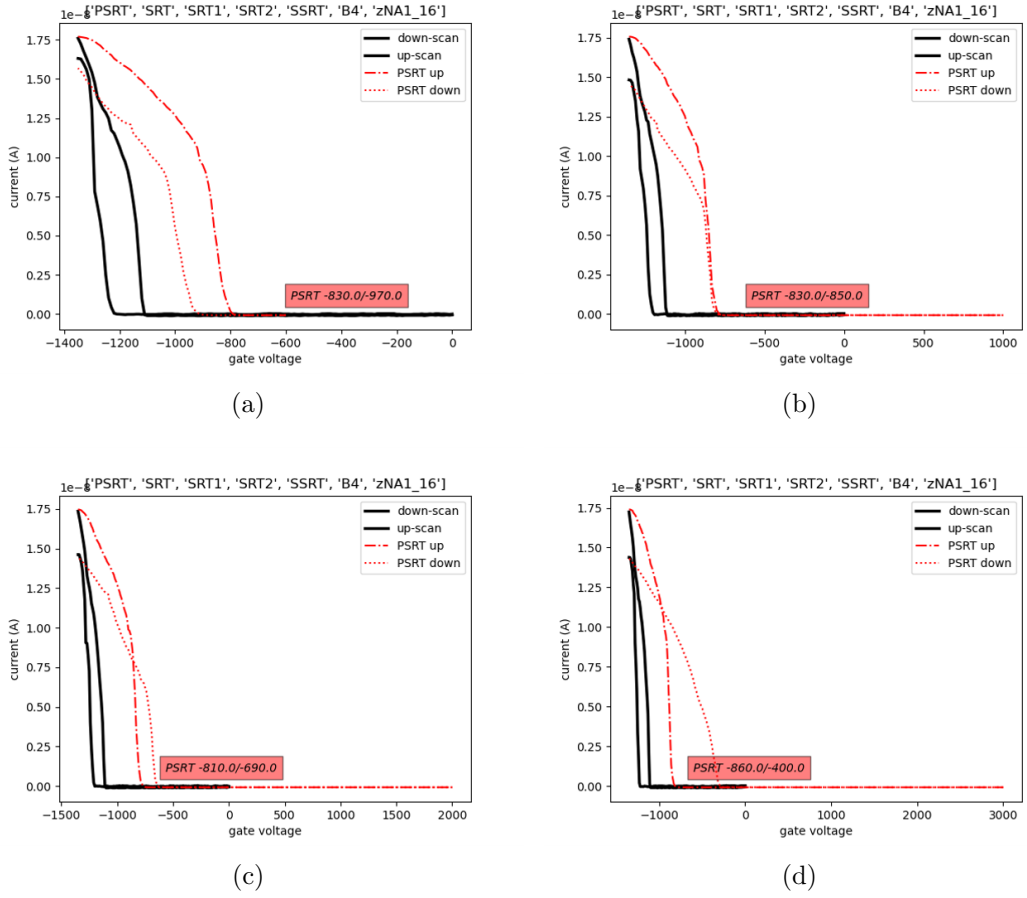


Figure 4.22: Pinch off and re-turn-on curve of PSRT under the "swing" operation. After turn-on the channel by sweeping combined gate to V_{min} (Black solid curve at right), PSRT was swept to (a) -600 mV, (b) 1000 mV, (c) 2000 mV and (d) 3000 mV and wait for 30s (Red dash-dotted curve). Then it was swept back to recover the channel (Red dotted curve). In this experiment, the collective turn-on voltage was initialized at -1150 mV and minimum voltage was set at -1350 mV.

Fig 4.22 show an example for "swing" experiment. Here we tried using it to adjust the turn-on position of PSRT. The collective turn-on voltage was initialized at -1150 mV and all gates were swept to V_{min} = -1350 mV in each test. Four choices of V_{max} from -600 mV to 3000 mV were tested. As we expected, the re-turn-on voltage of PSRT is significantly modified by the positive sweep, showing a positive outcome for this method.

To further check if the other gates could be affected by the "swing" operations, we further apply it in an one-by-one manner. In the experiment shown in Figure.4.23, we choose PSRT, SRT2, SRT and SSRT and the "swing" operation was repeated one-by-one for them in each test.

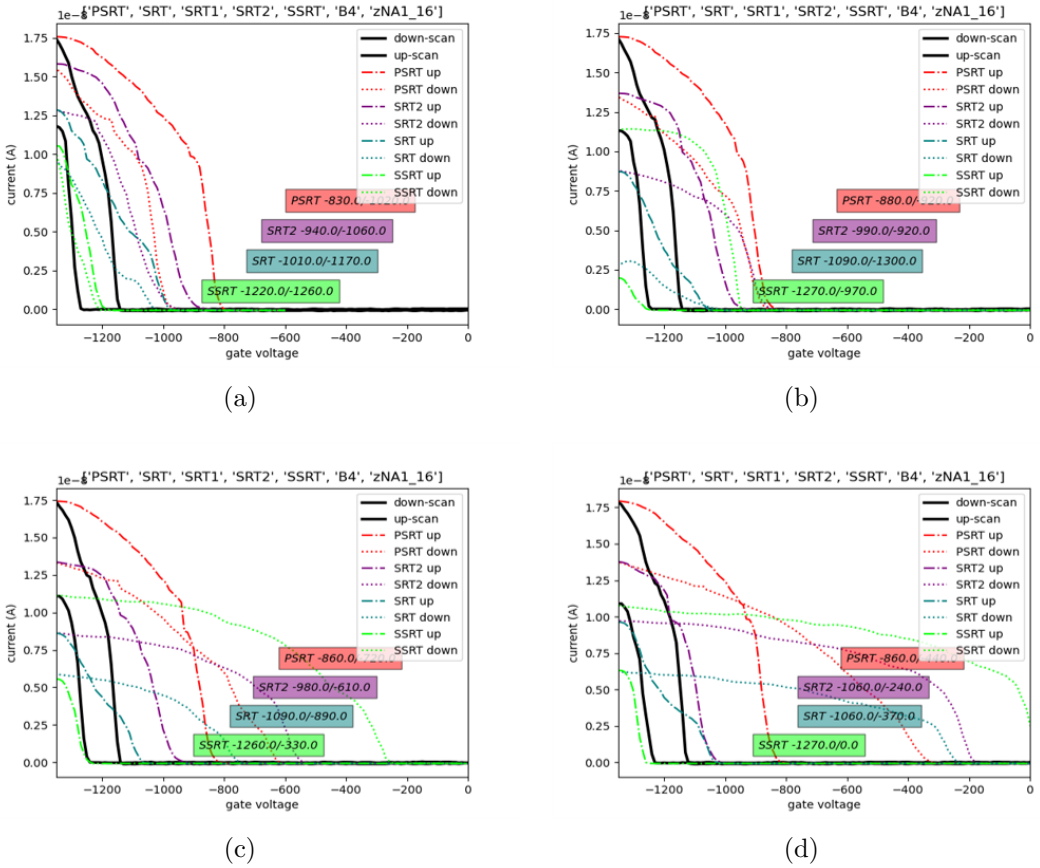


Figure 4.23: Pinch off and re-turn-on curve of PSRT,SRT1,SRT and SSRT under one-by-one "swing" operation. After turn-on the channel by sweeping combined gate to V_{min} (Black solid curve on right), the single gate was swept to (a) -600 mV, (b) 1000 mV, (c) 2000 mV and (d) 3000 mV and wait for 30s (Colored dash-dotted curves). Then it was swept back to recover the channel (Colored dotted curves). This process was ran sequentially for PSRT, SRT2, SRT and SSRT. The collective turn-on voltage was initialized at -1150 mV and the minimum voltage was set at -1350 mV. Positive part of the sweeps is not depicted.

As shown in Fig 4.23, the result indicates the realization of local control for turn-on position in each gate. The observations can be summarized as follows, solving the challenges listed at the beginning of this section:

- **The threshold voltage of single gates can be locally defined and controlled with "swing" operation.**

  From the result, it is clearly shown that the re-turn-on voltage of a single gate can be controlled by applying a positive voltage to it. With more positive voltage applied, we observe less negative re-turn on voltage.

  Physically speaking, this can be clearly attributed to the detrapping process under the single gate. The turn-on position of a single gate is therefore defined and controlled.

- **The cross-talk is suppressed in "swing" operation.**

  In Fig 4.23(a), a swing operation to a negative voltage is made as a control experiment. For experiments with all three positive voltages, the pinch-off voltage of gates swung later (SRT2, SRT, SSRT) appears slightly more negative than the

control experiment. This is believed to be caused by decay instead of cross-talk. If cross-talk happened, sweeping a single gate to positive would have made pinch-off voltage of other gates less negative due to detrapping. Therefore, this can only be explained by decay: sweeping single gates to more positive voltage will take more time, and decay will appear higher as in section 4.5.1.

Physically speaking, the absence of cross-talk can be explained by blocking effect by negative voltage of neighboring gates. If other gates stay at zero voltage when the single gate is swept to positive, detrapping might occur in its neighbors via cross-talk. However, when other gates stay at a negative voltage, the positive voltage applied to the single gate is harder to induce cross-talk, since its effect will be counteracted by the negative voltage applied to the neighbors. These negative voltages narrow the potential landscape around the single gate, so its neighbor stays unaffected.

In practice, the "swing" operation is also more close to the actual application scenarios in the experiment of quantum dot array - we more often want to adjust the characteristic of a single gate, i.e., loading or unloading threshold of a dot, rather than the collective turn-on voltage of the whole channel. During the adjustment, the other gates can stay in the negative voltage as usual and don't need to be swept to positive together. Besides, this also naturally help suppress the cross-talk. Within this context, locally sweeping a single gate with other gates unchanged is desired as this can make our control simpler.

More importantly, the blocking effect shown in the "swing" experiment provides us with a third possible operation other than negative or positive correction: the blocking operation. As we will demonstrate in section 5.2, this operation will be the key ingredient of local threshold voltage manipulation in future share-control arrays.

5 Conclusion and Outlook

5.1 Conclusion

In this research, measurements were conducted for single hole transistors in germanium HFET devices. The experiments are divided into two parts.

In the first part of the experiments (section 4.1), we demonstrated the application of SHT as a sensor for quantum dots arrays. As basic characterizations of the SHT, Coulomb peaks and Coulomb diamonds were measured in two sensors of the device. Unfortunately, the results appear irregular and unstable, indicates the unsatisfactory quality of the device. The RF compensated charge sensing measurements were also attempted. As a remedy for the instability of sensors, we demonstrated a "skiing trick" to improve the stability of these measurements, for which we measure and select the compensated sweep route in advance. However, the sensing still turns out to be unsuccessful due to the noisy behavior from fine structure near the sensor. Further experiment is therefore not conducted in this device.

The second part of experiments (section 4.2 - section 4.5) is the main part of the research. It was discovered that the drift of turn-on voltage could be reversed by sweeping the gate to positive voltage. The affecting factors of this effect were then investigated. As a result, the turn-on voltage is clearly depend on both the strength and duration of applied voltage. Utilizing this discovery, the manipulation of turn-on voltage of the devices is possible. Firstly, a "Touch-and-Back" sweep is proposed, providing us with a nearly non-demolition detection of turn-on voltage. Then an automatic feedback control program, namely *TurnonNavigator* is made, which can control the turn-on voltage of the channel to any desired values in usual range of operation. The program is flexible and customized adjustment for specific devices can be achieved by changing the control parameters of input.

Making use of the *TurnonNavigator*, deeper investigations of turn-on voltage behaviors with well-controlled initial conditions are made. These mainly include relaxation characterization experiments and history dependence experiments. In the relaxation characterization experiment, interestingly, different relaxation is observed after adjusting turn-on voltage to a different value. When the turn-on voltage is adjusted to highly negative value, it appears very unstable and relax to less negative value after removing the negative gate voltage. However, staying in a less negative off-state voltage can suppress the relaxation and stabilize the adjusted turn-on voltage. In the history dependence experiment, it was found that even if we adjust turn-on voltage to the same value, its different history value will result in different stability under successive touch-and-back sweeps.

To explain all these results, a hypothetical physical model, namely *"Coin Pusher Model"* is proposed. In this model, we assume the surface traps have a distribution of different time constant. Based on this model, all observed phenomena of turn-on voltage are modeled and explained. These phenomena include the drift and its reversal, different relaxation of adjusted turn-on values, stabilization with negative rest voltage, history dependence of stability and non-uniform drift under successive touch-and-back sweeps.

Finally, for future application of threshold voltage manipulation, we investigated the locality of these effects. For this, two experiments were designed. In the decay suspension experiment, we have shown that surface tunneling can happen locally under single gates, even without formation of full conducting channel. The locality of threshold voltage drift is thus concluded. In the "swing" experiment, we proposed a

method to locally define and reverse the threshold voltage by "swinging" single gate to positive voltage while the others are kept negative. The re-turn-on voltage after this swing operation is defined as the threshold voltage of this single gate. It was shown that the swing operation could locally reverse the drift while other gates stay unaffected.

The exciting results of these experiments provide us with powerful tools in the future operations on quantum dot arrays. Firstly, the manipulation of threshold voltage solves the problem of drift in a very convenient and reliable manner. We thus no longer need to suffer from tedious and interruptive resetting operations. Experiments can therefore be conducted efficiently and automatically in the future. Secondly, it opens up the possibilities of controlling initial condition of threshold voltage in the experiment. The threshold voltage then becomes a new degree of freedom that is under our control in quantum dot experiments.

Most important of all, controlling the turn-on characteristic of a channel might be the first step towards the uniformization of quantum dots arrays. Based on the tunability of the threshold voltage, we might be able to initialize the array with uniform conditions and apply shared control to the array, as proposed in [8]. This will pave the way towards future scalable semiconductor quantum computers. In the next subsection, we will introduce a proposal to realize addressable shared control for charge uniformity in the future quantum dot array.

5.2 Outlook: Proposal for addressable shared control for charge uniformity in future quantum dot array

In this subsection, we briefly introduce a proposal to improve the uniformity in the share-controlled quantum dot array by addressable manipulation of potential landscape in such systems. Here, we consider a 4×4 share-controlled quantum dot array as an example. Its schematic is shown in Fig 5.1. In this array, plunger gates of qubits are connected in diagonal lines across the layout. Barrier gates are defined by winding lines in a ladder-shaped pattern. With this layout, all qubits are share-controlled by both plunger gates and barrier gates.

(Note: Since the barrier gates interlace with each other, they are distinctively plotted in different colors in Fig 5.1 for clarity. In the following demonstration of strategy, we use another version of this schematic to better present different operation modes.)

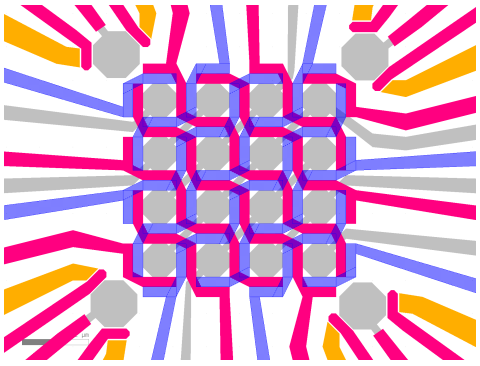


Figure 5.1: The schematic of the 4×4 share-controlled quantum dot array. Barrier gates are depicted as winding lines in blue and red, plunger gates are depicted as diagonal lines in grey.

The idea of this proposal comes from four observations from this research:

1. If voltage applied to the gate is negative enough to induce 2DHG underneath, traps will be filled via surface tunneling and threshold voltage for the next time will drift to more negative value. (section 4.2.1)

2. If voltage applied to the gate is negative, but smaller than threshold voltage, 2DHG will not be populated. In this case, drift will not happen and threshold voltage can only be stabilized. (section 4.3.3)

3. If voltage applied to the gate is positive, detrapping process will be induced under this gate, and threshold voltage can be recovered to less negative value. (section 4.2.1)

4. If voltage applied to a single gate is positive, while negative voltage is not applied to its neighbor gates, detrapping might be induced not only under the single gate but also under its neighboring gates via cross-talk. As result, the threshold voltage of both of them will recover to less negative value. (section 4.5.2)

5. However, if voltage applied to a single gate is positive, while its neighboring gates are applied with negative voltage, cross-talk will be suppressed and only the threshold voltage of the single gate will recover to less negative value. This is because the negative voltage in neighboring gates will counteract the effect from

positive in the single gate, narrowing the potential landscape nearby. (section 4.5.2)

Based on these four observations, we can therefore define three operation modes for gate in shared control layout and predict their effect as follows:

- **Negative Correction Mode.** Applying more negative voltage than the threshold voltage to the gate. This will populate 2DHG and make threshold voltage drift to a more negative value.
- **Blocking Mode.** Applying negative voltage but smaller than threshold voltage to the gate. This will not change the threshold voltage, but can block the effect from the positive voltage in neighboring gates, and can make the threshold voltage more stable.
- **Positive Correction Mode.** Applying positive voltage to the gate, this will cause detrapping process on the surface below this gate and threshold voltage will recover to a less negative value. If negative voltage is not applied to its neighboring gates, detrapping will also induced in its neighbor via cross-talk.

With these three operation modes, we can propose the strategy to tune the threshold voltage of single gates without affecting others. The strategy of positive correction (make the threshold voltage of specific gate less negative) is shown in Fig 5.2. Here, we only consider correction of plunger gates. Three positions of plunger gate under correction are chosen, which can represent all positions in the array by symmetry.

In this strategy, the barrier gates around the target gate are working on positive correction mode and induce detrapping for the target by cross-talk. The undesired lines of plunger gates are working on blocking mode, such that they cannot be affected from positive correction. By choosing barrier gates perpendicular to plunger lines, the target gate can be affected uniquely. Fortunately, this is very compatible with the actual operation scenarios of the quantum dot arrays. As the gates are usually working at negative voltage, sweeping single gates voltage towards positive would have very limited undesired effect to the surrounding.

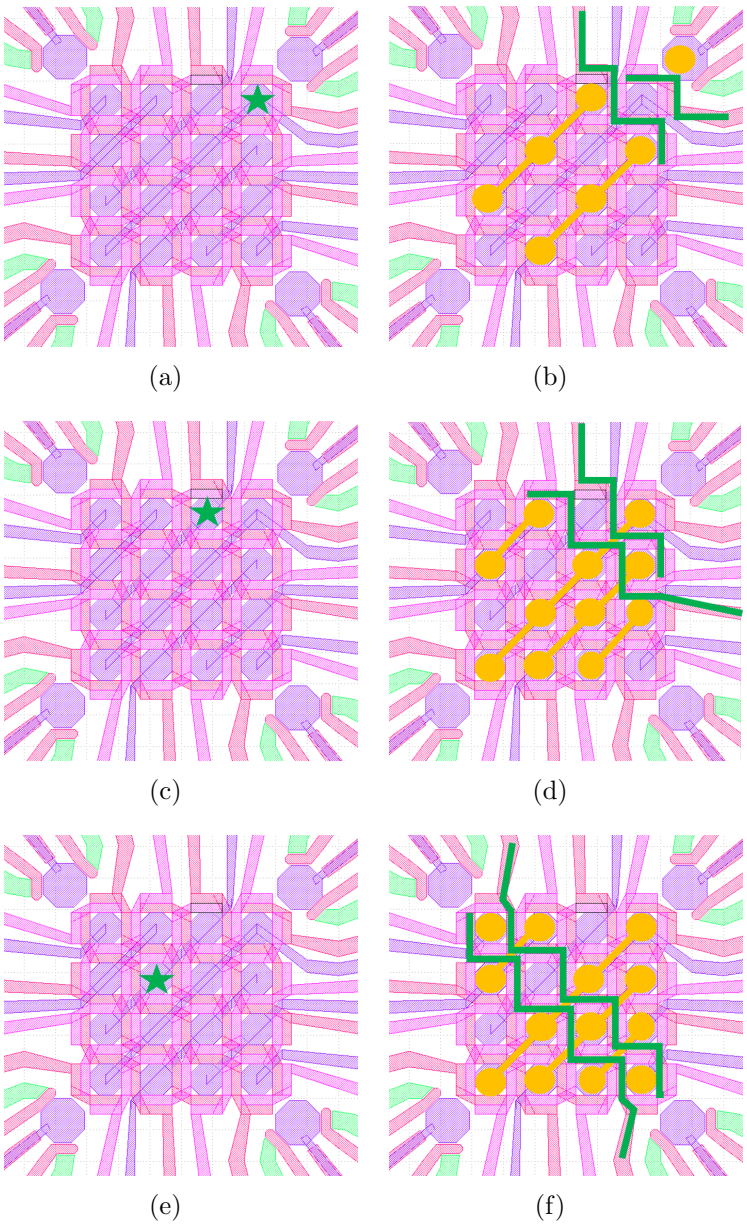
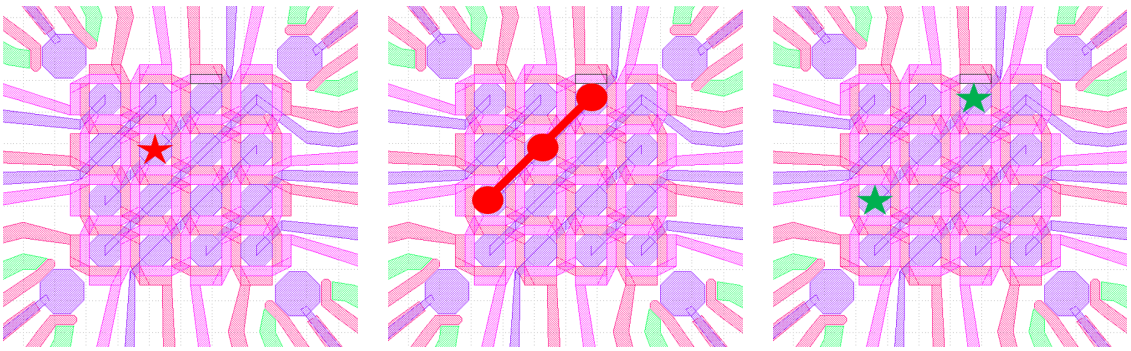


Figure 5.2: Strategy of positive correction of each single plunger gates with other plunger gates unaffected. The target plunger gate is indicated in the left diagram, and the corresponding strategy is shown in the right diagram. Green star: Target plunger gate for positive correction. Green line: Barrier gates working on positive correction mode. Yellow circle: Plunger gate working on blocking mode.

The strategy of negative correction (make the threshold voltage of specific gate more negative) is also shown in Fig.5.3, In this strategy, we first need to put the line of the target plunger gate to negative correction mode. Then, we recover the effect on undesired plunger gates in the line by applying a local positive correction to them in the way described in Fig 5.2. A negative correction of threshold voltage is therefore achieved.



(a) (b) (c)

Figure 5.3: Strategy of negative correction of each single plunger gates with other plunger gates unaffected. The target plunger gate is indicated in the left diagram, and the corresponding strategy is shown in the middle and right diagram. Red star: Target plunger gate for negative correction. Red circle: Plunger gate working on negative correction mode. Green star: Plunger gate under positive correction as in Fig 5.2.

This proposal, however, is still in the draft state and needs further improvements. These improvements includes feasibility check, proposal for detection and qubit operations. We believe that more ideas will be inspired for these topics in the future.

Starting from this kind of strategy, we can find a way to achieve threshold voltage uniformity in the share-controlled quantum dot arrays. With such uniformity, the variation of electrical characteristics induced by fabrication could be compensated by locally controlled potential landscape. This would be a very promising launchpad for future scalable semiconductor quantum computing platforms. To further go in this direction, we can also clearly locate many problems to solve in the future, as will be discussed in the next part.

5.3 Open questions for future research

Starting from the proposal of locally manipulating the threshold voltage in the share-controlled quantum dot array, there are also some clear directions to explore in our future research:

Question A: How to qualitatively describe the drift behavior of threshold voltage and its reversal?

In this research, we have explored the hysteresis behavior of threshold voltage in HFET devices. Based on the observations from the experiments, we have proposed a hypothetical physical model for the trapping and detrapping mechanisms behind the hysteresis behavior in our devices. The model can at least explain all the observations from the experiments included in this thesis.

However, it is still a quantitative model based on hand-waving description. To make it a good theory, qualitative or statistical analysis is needed. we notice that the qualitative or statistical methods are applied to analyze similar trapping and detrapping mechanisms [52, 55, 58]. It is therefore reasonable to conduct similar research for our study. If we can qualitatively model the behavior, the efficiency of the control could be greatly promoted. For this goal, a set of detailed and systematic tests are needed, which would be a direction to put effort into.

Question B: How is the actual performance of this proposal in the share-controlled quantum dot array?

As the reversibility of drift was found in the last month of my project, the time for detailed test is extremely limited and the experimental observations mentioned above are only found in simple structures shown in Fig.4.9(a). Further tests in more complex structures like the quantum dot arrays are desired. However, since the devices under study in our group are mainly new designs (e.g. the 2×4 and 4×4 quantum dot arrays), it will take time to have a device with good characterization and stable working status. Under this circumstance, conducting similar tests in these devices is the most obvious direction in the foreseeable future.

Question C: Can we make this strategy automatic and work as a standard initialization procedure of large-scale quantum dot arrays?

In this thesis, we have realized the automatic feedback control program for a simple transistor structure in HFET (Fig.4.9(a)), which can precisely control the collective turn-on voltage to any reasonable target value. It performs very well and can achieve highly customized and flexible control for different tested devices. However, when we go to more complex tasks like local threshold voltage manipulation of specific gates in large quantum dot arrays, the requirement for detection and feedback control design becomes much higher.

In the future, a possible idea to address this problem might be applying machine learning techniques to achieve an automatic standard initialization process for the quantum dot arrays. It's worth notice that the machine learning technique is already used for tuning the parameters of quantum dot arrays to desired charge states [63–65]. Within this context, it provides us with inspiration for the threshold voltage control in large-scale quantum dot arrays and could be another direction to explore.

Question D: Provided with uniformity, how far can we go for scalable share-controlled quantum information processing?

If we can realize the uniformity of threshold voltage, the uniformity of charge state control would follow. In this case, electrical characteristic variation induced by fabrication processes could be compensated, and share-control would be very feasible. Then we can try to actually realize the share-controlled quantum information processing in scalable quantum dot arrays, as proposed in [8]. This would be a very exciting milestone in semiconductor quantum computing route.

6 Acknowledgements

This Master thesis summarizes the results of the research project in the past six months. In this project, I confirmed my views on scientific research when I entered the campus of Delft University of Technology: This is the purest and happiest thing in the world. Most of this feeling stems from my participation in this exciting project. In this project, I experienced the process of realizing a very interesting idea: from learning this exciting idea at the beginning, to slowly figuring out the way to realize it, to designing a series of interesting experiments, to finding a breakthrough, and finally to proposing the corresponding physical model and future application plan for it. Every step far exceeded my expectations, and every step can bring me the happiest experience so far in my life.

First of all, I am extremely fortunate that in my master thesis project I have encountered an academic instructor who has benefited me a lot: Professor Menno Veldhorst. He is the supervisor in every Master student's dream: knowledgeable, experienced, open-minded, patient, friendly, and responsible towards students. He encourages students when they encounter difficulties, and can always give the most sensible insights and advice at the fork in the road. I still remember that when there was almost no progress in the fourth month of the project, he comforted me and encouraged me by telling me that the difficulty I was having is very common, and maybe there will be a breakthrough in a while and all the problems will be solved quickly.

Things came as he expected-on April 21st, when I discovered the phenomenon of reversible drift, and the research has progressed rapidly since then. Inspired by his idea, I can make new discoveries and progress every week: I realized the control of the turn-on voltage this week, and its stability was tested next week, and a physical model was proposed next week... This process has become the most exciting and happiest experience in my research life. I can't imagine what my thesis project would look like without his encouragement and advice.

I am also very fortunate to be able to meet such a skillful and kindhearted daily supervisor like Chien-an Wang. His understanding of physics always provides me with inspiration in every discussion. What moved me even more was that he often took the trouble to help me solve basic and trivial problems like program bugs and wiring problems. In the process of helping me review the thesis, he made very detailed and helpful suggestions, which played a huge role in the improvement of my thesis.

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completely given me the freedom to choose the path of life. I hope I will be able to repay them through hard work in the future.

Looking back, as a graduate student who is interested in academic research, how honored I am to meet such kind, responsible, and enthusiastic partners at the beginning of scientific research? How honored is it for me to finally have a good start on the academic road under their influence, guidance and help? Although in this beginning, the things I have done are so small: for example, in my master's project, what I did was research on the physical characteristics of one aspect of semiconductor quantum computing systems, and this characteristic is explored to realize the uniformity of the quantum dot array; and this kind of array is only an attempt by humans to explore scalable quantum computing, and quantum computing is only an attempt to achieve higher computation efficiency...

Whether it is now or in the future, it is very likely that the work I have paid countless hours and painstaking time for will only be a "part of part of part of part of part" of the whole picture of the scientific progress. However, it is such a small and real achievement that can bring our motivation and thirst throughout, and can also indelibly accumulate the development of human knowledge. Let's end with one of my favorite sayings: "It is not necessary for me to draw the final success, by my effort will not be paid in vain." The spirit of it should be the faith in my future academic life.

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