A High-Temperature Electronic System for Pressure-Transducers

Paul C. de Jong and Gerard C. M. Meijer, *Member, IEEE*

***Abstract*—This paper describes a high-temperature pressure-transducer interface for resistive Wheatstone bridges. The long-term drift of the smart sensor, i.e., the (pressure) sensor plus its interface electronics, will be determined by the drift of the sensor element only. A three-signal auto-calibration sequence of the interface electronics keeps the transducer interface virtually free of long-term drift. A novel low-drift pre-amplifier forms an essential element in this system. The high-temperature operation of the transducer interface has been investigated from both an electronic and a packaging point of view. The system has been realized by combining CMOS ASIC's with a thick-film packaging technology. The pressure-transducer interface works up to 250–275 °C with 15–16 bits accuracy.**

***Index Terms*—Dynamic element matching, high-temperature electronics, intelligent sensors, pressure transducers, transducer interfaces.**

I. Introduction

In the oil industry, downhole-pressure measurements are important parameters for oil-reservoir prognosis. The conditions downhole are harsh. The electronic systems have to cope with high temperatures, high pressures, vibration, shock, confined space, etc. Permanent-installed pressure gauges provide on-line data, which allow for direct monitoring of the downhole conditions. The long-term stability of these pressure sensors forms their key parameter. Ideally, these sensors should be free of drift because, once installed, maintenance and re-calibration are impossible or extremely expensive. High-temperature piezo-resistive pressure sensors have been developed that specify a long-term drift of less than 0.15% per year below 300 °C [1]. Currently, there is hardly any analog electronic circuitry available that works well at temperatures above 150 °C. Leakage currents and latch-up disturb the biasing conditions. Moreover, when following the traditional design approaches, the long-term stability of any electronics that would survive at such temperatures would be much worse than the stability specified by the sensor. Recently, the present authors described a novel instrumentation amplifier, which is fabricated in conventional CMOS technology and features a high accuracy up to 275 °C [2]. In this paper, the design of a complete high-temperature pressure transducer interface will be described that is able to keep up with the specifications of the sensor.

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The authors are with Delft University of Technology, Faculty of Electrical Engineering, Electronics Research Laboratory, 2628 CD Delft, The Netherlands (e-mail: g.c.m.meijer@et.tudelft.n).

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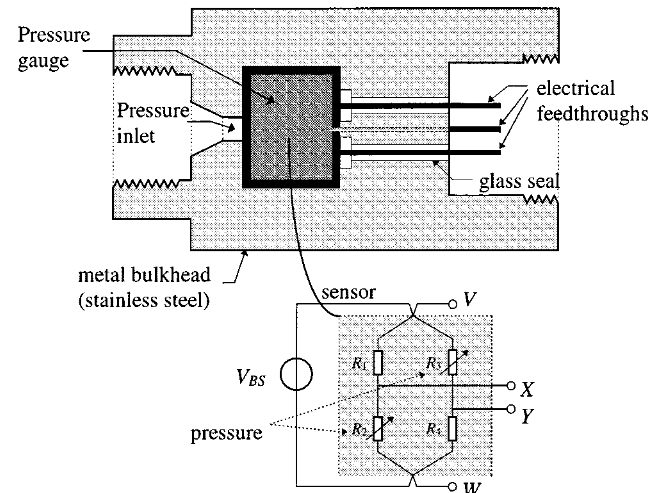

Fig. 1. Cross-sectional view of a pressure-transducer bulkhead. The well fluid compresses a pressure gauge, which changes the imbalance of a Wheatstone bridge. The voltage across the bridge is measured using the four-wire measurement technique.

The design of a high-temperature electronic system not only involves the design of the electronics, but also their packaging. Traditionally employed materials such as polyamide, plastics and epoxies are causing long-term reliability problems because they melt, are chemically reacting, or produce aggressive outgassing products. The combination of confined space and sealed environment demands for a reviewing of the currently available packaging technologies. Both the interfacing and packaging related design aspects are considered in this paper.

II. The Measurement Principles

Mechanical structures are available that cause changes to the sensor in response to the applied pressure. Fig. 1 shows a cross-sectional view of a pressure-transducer bulkhead. Pressurized well-fluid causes a mechanical force to be applied to a resistive pressure gauge. This changes the imbalance of a Wheatstone bridge, where its imbalance ξ is defined as

$$\xi = \frac{V_{XY}}{V_{VW}} = \frac{R_2}{R_1 + R_2} - \frac{R_4}{R_3 + R_4} \tag{1}$$

Two different types of gauges are available: strain gauges and piezo-resistive gauges. The maximum imbalance of strain gauges is small, i.e., in the order of 0.5% only, while the maximum imbalance of piezo-resistive gauges can be in the order of 6%. The imbalance of the Wheatstone bridge can be measured by forcing a supply voltage $V_{\rm BS}$ across the bridge,

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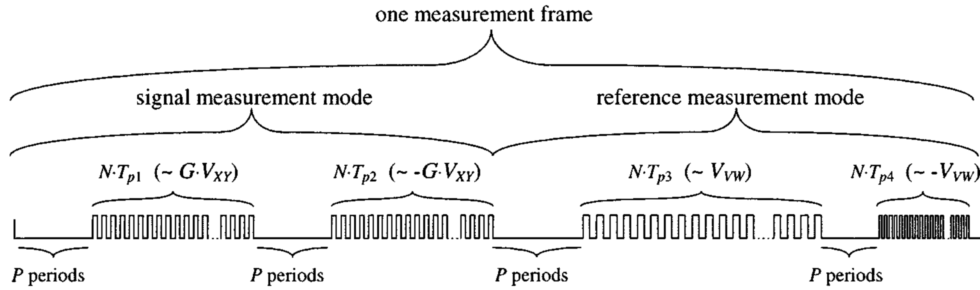

Fig. 2. Proposed output protocol of the SSP. One measurement frame consists of four successive measurement phases, each M $(=P+N)$ periods long. During the first P periods, the output of the SSP will be held low.

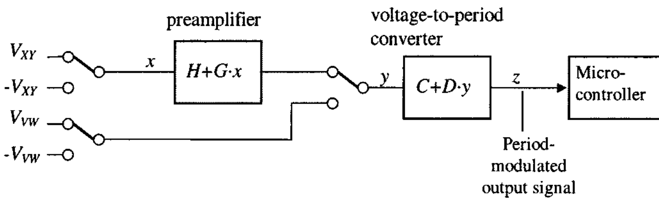

Fig. 3. The four-signal auto-calibration applied to the pressure-transducer interface. The microcontroller selects the successive measurement phases.

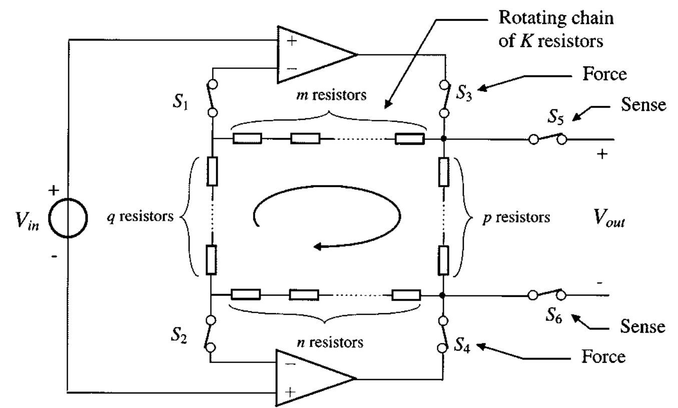

Fig. 4. The principle of a dynamic-feedback instrumentation amplifier. The gain is independent of the ON-resistance of the switches.

while sensing the voltages V_{XY} and V_{VW}, respectively. Separate force and sense wires are necessary to eliminate the effects of parasitic wire resistances. The measured imbalance x will be obtained digitally in the microcontroller after processing the voltages V_{XY} (the pressure-dependent signal) and V_{VW} (the reference signal) separately. The bridge signals are converted into a period-modulated output signal by means of a smart signal processor (SSP). Fig. 2 shows a typical example of such an output signal, which consists of several groups of periods for the various measurement modes within a measurement frame. The duration of each period represents an analogue sample of the electrical input signal. Afterwards the period-modulated signal can easily be digitized using the timer of a microcontroller (Fig. 3). Continuous auto-calibration, i.e., periodically measuring the three input signals, is applied to eliminate the effects of long-term drift of the additive and multiplicative errors introduced by the SSP [3], [4]. Obviously, the major requirement of the SSP is that of linearity. The long-term stability of the SSP will then only be determined by the sensor and by the long-term stability of the offset and reference signals.

The auto-calibrated conversion of the imbalance ξ of the Wheatstone bridge introduces a dynamic-range problem when both V_{XY} and V_{VW} have to be processed by the same SSP converter. Since the output level of V_{XY} is only a small fraction of V_{VW}, the demands for linearity become hard to be accomplished. Using a pre-amplifier can solve this problem. The bridge-output voltage V_{XY} must be amplified to a level where its dynamic range is in the range of V_{VW}. This however, shifts the dynamic-range problem to a stringent demand for (long-term) stability of the amplifier gain because the amplifier gain falls outside the auto-calibration sequence. This can be explained with the aid of Fig. 3. The amplifier gain has been represented by a linear function with offset H and a gain factor G. The transfer function of the voltage-to-period converter has also been represented by a linear function with an additive component C and a multiplicative component D, respectively.

Since the signal V_{XY} and the reference V_{VW} follow different paths, separate zero measurements are necessary to eliminate the additive components from both the amplifier and the A/D converter. For this reason, the three-signal auto-calibration turns into a four-signal auto-calibration. The zero measurements can be realized by processing the inverted values of the signal and the reference voltages. This can conveniently be implemented with a multiplexer circuit, which causes the bridge-supply voltage V_{BS} to be alternating. The microcontroller can be used to control this multiplexer. So, the digital result M after these four successive measurements becomes

$$M=\frac{Z(V_{XY})-Z(-V_{XY})}{Z(V_{VW})-Z(-V_{VW})}=G\frac{V_{XY}}{V_{VW}}. \tag{2}$$

This result evidently shows the dependency on the amplifier gain. Consequently, the long-term stability of the SSP is determined by the drift of the sensor as well as by the drift of the instrumentation amplifier. This problem can be overcome by the use of dynamic feedback.

Dynamic-feedback amplifier: The principle schematic of the dynamic-feedback pre-amplifier is shown in Fig. 4. The resistive feedback consists of a chain of K matched resistors. The chain will be made rotating by addressing of the appropriate switches. The feedback is realized by m, n and q resistors, respectively.

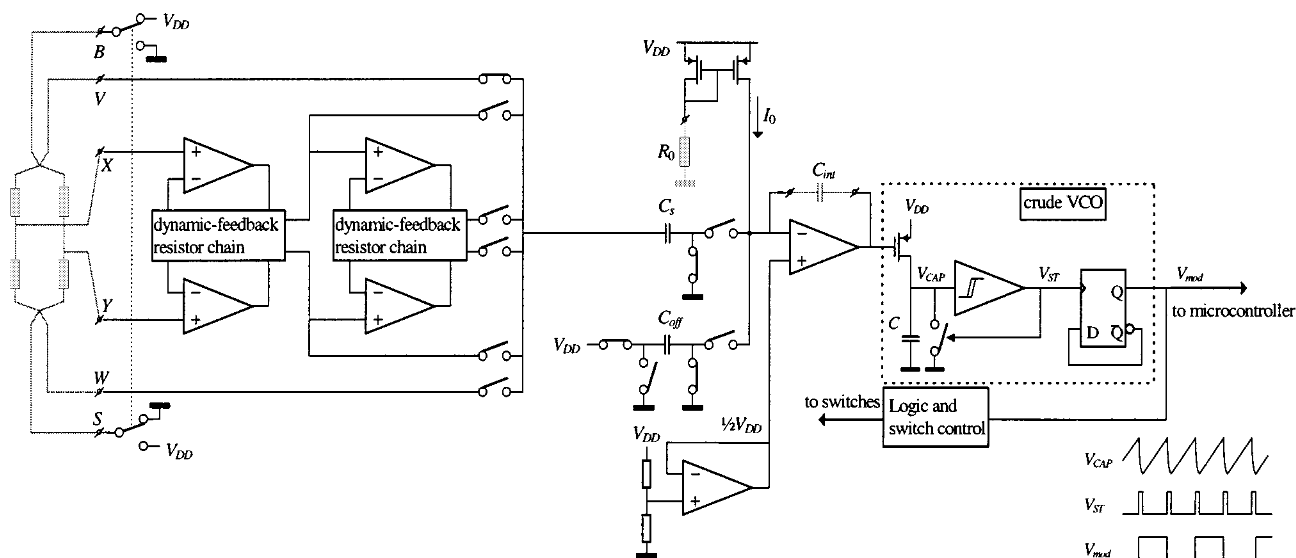

Fig. 5. Block diagram of the ASIC; the switch positions concern an arbitrary chosen moment.

Since the resistors are connected as a chain, a resistive load will be present which consists of p resistors. Therefore, it holds that

$$K \equiv q + m + n + p. \tag{3}$$

By applying force and sense wires the effect of the ON resistances of the switches S_1–S_6 is completely eliminated [2], [6]. The feedback is made dynamic by rotating the resistor chain between the two opamps. Therefore, the feedback has K states. Therefore, a resistor that is part of the load will become part of the feedback later. For this reason, this load resistor is of vital importance for the functionality of the dynamic feedback. The average gain $\overline{G}$ of this amplifier over K successive states is equal to

$$\overline{G} = 1 + \frac{m+n}{q}. \tag{4}$$

Any mismatch between the resistors hardly affects the average gain because there is a compensating effect when the resistors move along the chain. By this compensation resistor mismatches appear as second-order effects in the average gain. The drift of the resistors does not affect the average gain at all, because rotational speed of the resistor chain is relatively fast, i.e., several kilohertz.

The resistor chain is controlled by a digital-state machine, which addresses the appropriate switches. Every successive state, the chain rotates one position. So, the number of states is equal to the number of resistors in the chain. The control of the resistor chain requires that there are six switches connected to a single point between every two resistors. Two of these switches are necessary to connect to the negative-input nodes of the opamps and two switches are necessary to connect to the output nodes of the opamps. The remaining two switches are necessary to sense the output voltage across the load resistor(s). Consequently, a total of $6K$ switches is required to realize the dynamic feedback circuit.

III. High-Temperature ASIC Design

A. The Circuit

The pressure-transducer SSP has been realized as an ASIC [6], [7]. A block diagram of the circuit is shown in Fig. 5. The interface consists of two dynamic-feedback amplifiers to handle signals from strain gauges and piezo-resistive gauges. When handling the signals from piezo-resistive gauges, the second dynamic-feedback amplifier will be bypassed and powered-down. The ASIC also contains a linear VCO to convert the signal, the reference signal, the inverted signal and the inverted reference signal, according to (2), into period-modulated output signals that will be handled by the microcontroller. The ASIC also contains logic circuitry to control the successive measurement phases.

The circuit design also accounts for degradation mechanisms that may impede the ASIC's reliability at high ambient temperatures. These are, among others, corrosion, electromigration, diffusion, mechanical stresses, leakage currents, and latch-up. These degrading mechanisms are discussed now:

B. Technology, Leakage Currents and Latch-Up

For high-temperature applications, a CMOS technology is preferred to the bipolar technology. There are three main reasons for this:

1) In contrast with the bipolar devices, the operation of CMOS devices relies on the behavior of *majority* carriers instead of *minority* carriers. Therefore, the overshadowing of these respective concentrations by thermally generated carriers occurs for the CMOS devices at much higher temperatures than for the bipolar devices.
2) The number of pn-junctions is for analog CMOS circuits much less than that of their bipolar equivalents.
3) The leakage currents are proportional to the pn-juncton areas. Usually, for CMOS components these areas are much smaller than for bipolar ones.

As a consequence, MOS devices have shown to be functional up to 350 °C, whereas bipolar transistors are hardly useful above 225 °C. Moreover, the implementation of the required logic circuitry and switches is much simpler in a CMOS technology.

Latch-up is a general term to indicate undesired states of biasing caused by the action of parasitic transistors, which amplify the currents caused by leakage and interference. It concerns a serious problem, which can cause a complete failure or even burn-out of the circuit. To avoid latch-up it is advised to take the following measures [7]:

1) apply high-threshold technology, which reduces the magnitude of the sub-threshold currents.
2) apply reverse biasing of all pn-junctions, which has the same effect as using high-threshold technology.
3) avoid the use of short-channel devices, in order to avoid punch-through effects.
4) keep sufficient distance between the NMOS and PMOS section.
5) apply double guard rings to collect the thermally generated minority and majority carriers.

C. Electromigration and Corrosion of Aluminum

Electromigration problems have been solved by increasing the widths of the aluminum interconnection patterns, while the use of redundant contacts and vias further reduces this problem. In addition, the circuit has been designed to be low-power; the ASIC current consumption stays below 5 mA. On the other hand, the biasing currents are still large enough to overshadow high-temperature leakage currents. Otherwise, these leakage currents would cause total runaway of the biasing. Corrosion of aluminum can easily be avoided by removing all oxygen during packaging of the ASIC. The package should be hermetically sealed under a chemically inert gas, e.g., nitrogen. Electromigration becomes a serious problem when the current densities in the aluminum conductor patterns are roughly exceeding 0.1 mA/mm^2. Altering the metal system for, for instance, tungsten can develop an electromigration-hardened process. This adds costs plus that such processes are not widely available. Therefore, for the pressure-transducer interface, it was chosen to trade silicon area to allow for increased widths of the aluminum interconnection patterns. Moreover, using multiple contacts and vias further reduces this problem as it adds redundancy. Another problem is that silicon tends to diffuse into pure aluminum. This process is accelerated at higher temperatures. Therefore, a diffusion barrier would be required at the interfaces where the on-chip devices, e.g., transistors, diffused resistors and junction capacitors, are contacted with the aluminum conductor pattern. A very simple, though effective, solution to eliminate these diffusion problems is to add 1% silicon to the aluminum on beforehand. The alloy aluminum-silicon (1%-Si, 99%-Al), in fact, does not use up any silicon before 500 °C. At 300 °C, the chemical equilibrium lies around 0.5% silicon, so sufficient overkill is present to avoid any detrimental diffusion effects. This technique is commonly applied in commercially available CMOS processes. Also note that even aluminum for wire bonding contains 1% silicon in order to obtain wire strengths comparable to gold. In conclusion, it is possible to obtain reliable high-temperature electronics from standard CMOS technologies using aluminum as a metal system.

D. Mechanical Stresses

Mechanical stresses can arise from differences of thermal expansion of the different materials, which may lead to fractures. Shocks and vibration have their impact on devices, especially when their connection area is small with respect to their mass.

The thermal expansion coefficients of the ceramic substrates and packages must be matched to the one of silicon (2.6×10^{-6}°C^{-1}) to avoid ASIC fracture. The ASIC-bonding will have to be elastic to cope with thermal strain. For this reason, it is to be avoided to use polyamide as a carrier material because it expands much faster with temperature than ceramics. Metal packages must be Kovar-based because the temperature-coefficient of Kovar is matched to the one of silicon.

E. Chemical Considerations

Often, reliability problems arise from outgassing of components. The resulting chemical attack causes corrosion or causes formation of compounds. Eventually, this leads to reliability problems. Corrosion is accelerated by temperature while moisture acts as a catalyst. Therefore, when sealing an electrical component package, this should be done in an environment filled with a chemically inert gas, e.g., nitrogen (N_2). Making all components more robust against chemical attack does not solve the problem of outgassing at all. Such outgassing materials must be avoided completely. Due to the sealed environment, some reactive gasses may cause failures otherwise. Moreover, it is always recommended to place any circuitry in a high temperature vacuum to remove all outgassing prior to filling the package with nitrogen or helium. This "vacuum-baking" step covers a main part of the burn-in of the tool.

IV. High-Temperature Packaging of the Pressure-Transducer Interface

In order to design a temperature-resistant package, it is necessary to identify the different components inside these packaged modules. It will be assumed to package a hybrid circuit according to the thick-film technology [8]. The packaging of single ASIC's then follows from simplifications of this technique. Five levels can be distinguished:

1) die bonding;
2) wire bonding;
3) conductor pattern to substrate;
4) the printing of interconnections;
5) substrate to package cavity.

The following levels will be more closely analyzed now.

A. Die Bonding

The ASIC must be bonded to a substrate, which usually is, e.g., for high-temperature purposes, a gold-plated area on top of a ceramic substrate. Elastic bonds are a prerequisite to avoid

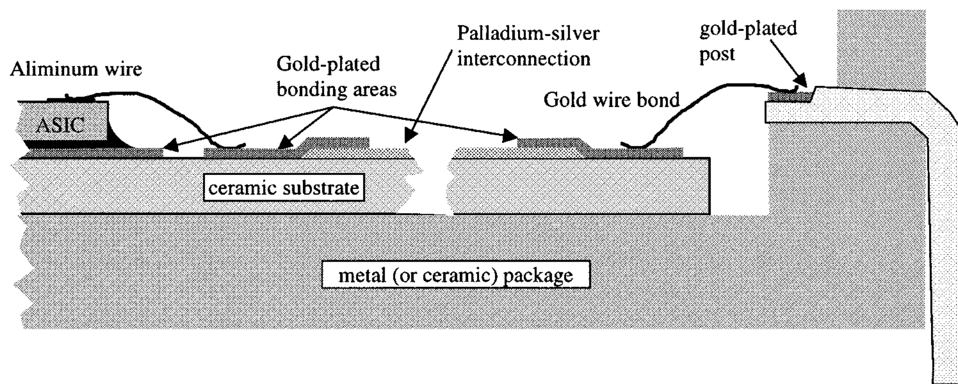

Fig. 6. Cross-sectional view (not to scale) of a high-temperature package. Both aluminum and gold wire bonds will be present throughout the package.

mechanical stresses between the substrate and the silicon. Two types of die-bonds are suitable for high-temperature applications: eutectic bonds and high-temperature epoxy bonds: The well-known silicon-gold eutectic bond [9], which consists of 6%–94% Si-Au, has a melting temperature of 370 °C. The resulting bond has a high elastic modulus and provides a good electrical contact to the backside of the ASIC. As compared to other bonds, the eutectic bond is favorable as it forms an excellent medium between the silicon ASIC and the gold-plated carrier material. Latch-up susceptibility will be greatly reduced by electrically contacting the backside of the ASIC. Furthermore, the eutectic bond provides an excellent thermal contact to the on-chip devices, which results in junction temperatures that are close to the ambient temperature.

B. Wire Bonding

Thin wires are used to form connections between ASIC's, substrates and package posts. Long bonding wires show wire sweep due to shocks and vibration. They can cause shorts to neighboring wires or even come off. Therefore, short bonding wires are necessary. Commonly used bonding wires are made from gold or aluminum. Wire bonding with gold will cause problems at high temperatures because aluminum of the ASIC's bondpads diffuses into the gold wire (purple plague). This process is further accelerated due to the presence of silicon, which acts as a catalyst. This causes the bond wire to be torn loose. To prevent the occurrence of purple plague, aluminum bonding is recommended [10]. Aluminum is more susceptible to corrosion, but when the atmosphere consists of dry nitrogen then it is not expected to give any problems.

Ceramic packages and substrates make use of gold-plated bonding areas. The Kovar posts, i.e., the connection to the inner leads of the package are also gold-plated. When using aluminum wires instead of gold, it may be expected that the purple-plague problem will be transferred from the ASIC to the gold-plated bonding areas. Fortunately, this is hardly the case. The aluminum film on the ASIC is only 1–2 µm thick while the bonding wire has 25 μm–50 μm diameter. Therefore, a gold wire would consume this thin aluminum film easily. On the contrary, an aluminum wire will not be consumed by the gold film (of approximately 10 μm thickness) at the posts or bonding areas so easily because the gold film does not have enough volume to consume a significant part of the aluminum wire. Nevertheless, due to the presence of both gold and aluminum, it is expected to see some purple-plague formation. This has been verified by measurements. It was found from aluminum wires (32 μm-diameter) bonded to gold-plated conductor patterns of 10 μm thickness that there was light-brown coloration around the bond after 528 h at 300 °C. Wire-pull tests showed approximately 50% loss of strength. After 528 h, the average measured pull-strength equals 4.36 g, which is still above the military specified value of 3 g. Therefore, all ASIC bondpads must be bonded by using aluminum wires. All remaining bonds have to be completed by gold wires, i.e., the connections between the posts and the substrates. A cross-sectional view of a package where these techniques have been applied is shown in Fig. 6.

C. Substrates

The choice of the substrate depends on the thermal expansion coefficient between silicon and substrate. A value close to the one of silicon ($2.6 \times 10^{-6}{}^{\circ}\mathrm{C}^{-1}$) is mandatory to avoid chip fracture. A commonly used material is the ceramic material alumina (Al_2O_3), which is a very good electrical insulator and well suited for high-temperature applications.

D. Interconnection and Wiring

The interconnection patterns on alumina substrates are made of precious metal palladium-silver. Wire bonding to the palladium-silver tracks is difficult. Therefore, as shown in Fig. 6, gold-plated bonding areas are necessary. These areas generally are 0.5 mm × 2 mm × 10 mm gold areas with 1 mm overlap over the palladium-silver tracks.

E. Hybrid and ASIC Packaging

Two types of material for high-temperature packages can be distinguished: metal and ceramics. The electrical feedthroughs of metal (Kovar-based) packages are isolated from each other by glass encapsulations. The Kovar-based feedthroughs have gold-plated connection are as shown in Fig. 6. Hybrid circuits use an alumina substrate that will be attached in a similar way to the cavity of a metal flat-pack. The substrate is pressed into an epoxy paste and cured at a temperature below 300 °C in order not to impair the bonding quality of the ASIC's, chip resistors, capacitors, etc. Ceramic packages are merely used to package individual ASIC's. ASIC's can be directly attached to the cavity using an epoxy paste or by means of an eutectic bond because

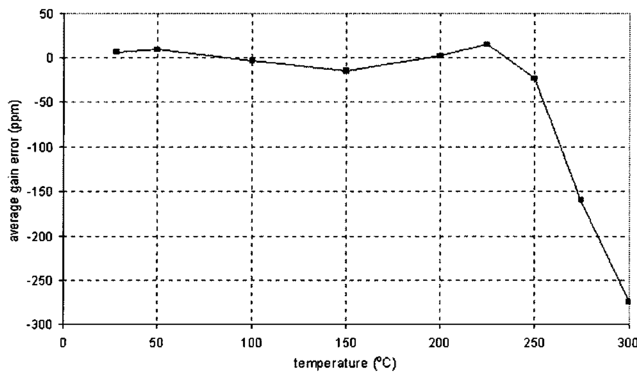

Fig. 7. The average gain of the instrumentation amplifier over the temperature range.

the cavity is gold-plated. Care should be taken to use fritless feedthroughs as side-brazed pins might fall apart at high temperatures.

F. Printed-Circuit Boards

At present, PCB's are usually made of epoxy or polyamide. Both are synthetic materials. Epoxy cannot be used at high ambient temperatures because it simply burns away above 175 °C. Polyamide is more temperature resistant, but will be abandoned because of its large thermal-expansion coefficient, i.e. approximately 45×10^{-6}°C^{-1}, which results in mechanical stresses. For example, there will be friction at the solder joints when the temperature is cycled. Moreover, the conductive interconnection patterns adhere much more firmly to alumina than to polyamide. Therefore, the highest reliability is to be expected from using alumina printed-circuit boards, which thermal-expansion coefficient is about 8×10^{-6}°C^{-1}.

G. Test Results

The ASIC has been fabricated and tested, following the above indicated criteria. The die bonding of the prototype has been realized by means of an epoxy paste because a thick oxide at the ASIC's backside did not allow for eutectic bonding. The wire bonding at the ASIC has been realized by means of aluminum wires, while the posts are connected to the substrate by means of gold wires. This circuit has been successfully tested for three weeks at 225 °C where other components in the system limited the maximum testing temperature. Brief tests [11] proved that the circuits are functional up to 275 °C. Fig. 7 shows the measured average gain variations of the dynamic-feedback instrumentation amplifier [2], plotted versus the temperature.

V. CONCLUSION

An accurate pressure-transducer interface, for high temperature operation, has been designed, using a systematic approach to solve the problems related to the electronic circuitry and the packaging. With respect to the electronic circuitry it has been shown that CMOS technology is more suited than bipolar technology. At the chip level, measures such as guarding have been taken to obviate latch-up phenomena. Usually, biasing currents of about 10 μA per component are large enough to overshadow the effects of leakage currents, for temperatures up to 250 °C.

An excellent long-term stability of the interface is guaranteed by applying the concepts of continuous auto-calibration and dynamic feedback of the pre-amplifiers. The packaging related problems have been discussed and recommendations have been given regarding the die-bond, the wire bonding, the ASIC packaging and the applied printed circuit boards. A complete interface has been built and shows good test results for temperatures up to 275 °C.

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Paul C. de Jong was born in Nieuwkoop, The Netherlands, on May 13, 1967. He received the M.Sc. and Ph.D. degrees in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 1990 and 1998, respectively.

From 1990 to 1991, he was with Schlumberger in Clamart, France and Houston, TX, where he designed high-temperature electronics for down-hole oilfield applications. Next, he was with the Laboratory of Electronics, Delft University of Technology, from 1991 to 1998, where he was involved successively in the design of Δ-σ A/D converters and smart sensor systems for high-temperature applications. He is currently a Senior Design Engineer at the Netherlands Organization for Applied Scientific Research (TNO) in The Hague, The Netherlands, where he is designing analog and mixed-signal Ics.

Gerard C. M. Meijer (M'94) was born in Wateringen, The Netherlands, on June 28, 1945. He received the ingenieurs (M.S.) and Ph.D. degrees in electrical engineering from the Delft University of Technology, Delft, The Netherlands, in 1972 and 1982, respectively.

Since 1972, he has been part of the Laboratory of Electronics, Delft University of Technology, where he is an Associate Professor, engaged in research and teaching on analog IC's. In 1984 and part-time during 1985–1987, he was seconded to the Delft Instruments Company in Delft, where he was involved in the development of industrial level gauges and temperature transducers. In 1996, he was one of the founders of the company Sensart, where he is a consultant in the field of sensor systems.

Dr. Meijer is a member of the Netherlands Society for Radio and Electronics.