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Sub-Orbital Flight Demonstration of a 183/540–600 GHz Hybrid CMOS-InP and CMOS-Schottky-MEMS Limb-Sounder

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(Invited Paper)

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ABSTRACT This paper presents an overview of a sub-orbital flight demonstration with a 183 GHz and 540–600 GHz limb-sounding instrument aboard a stratospheric balloon craft. The 183 GHz band provides soundings of stratospheric H_2O and is implemented with a hybrid CMOS-InP receiver architecture which provides excellent sensitivity while remaining compact (162 g) and offering an extremely low DC power consumption (0.62 W). The 540–600 GHz channel sounds stratospheric O_3 and uses a combination of a CMOS local oscillator, GaAs Schottky mixer and micro-electro-mechanical-system (MEMS) RF switch for calibration, again offering competitive form factor (1.4 Kg) and low DC power consumption (6.6 W) compared to prior instruments. The instrument was flown on the NASA Reck-Tang Limb-sounding Experiment (ReckTangLE) balloon craft and performed atmospheric soundings across New Mexico and Northwestern Texas on Oct. 17 2019.

INDEX TERMS CMOS, InP, hybrid, Schottky, MEMS, limb-sounder, ReckTangLE.

I. INTRODUCTION

Millimeter & Sub-millimeter wave rotational spectroscopy has played an important role in exploring the solar system and contributed several major results to the planetary science field. One major example of this is the Microwave Instrument for the Rosetta Orbiter (MIRO) which studied H_2O isotopes of Jovian family comet 67/P [1] and demonstrated that the Deuterium to Hydrogen (D/H) isotope ratio was far from what conventional models of solar system evolution predicted [2]. This study of D/H ratio is important in understanding the mechanisms with which the solar system formed as well as how water resources were delivered to Earth and other planetary boides. While the D/H of the inner solar system (Mars, Earth, Venus) is better understood, there have been limited opportunities to send millimeter/sub-millimeter wave spectrometer instruments to the outer solar system with only limited measurements at Jupiter and none conducted at Saturn or other outer solar system targets. Beyond the D/H ratio focus of MIRO, sub-mm-wave offers the possibility of investigating other exciting phenomenon in the outer solar system including studying the structure and composition of water jets or plumes shooting out of icy world moons like Enceladus and Europa. Beyond jet structure, sub-mm-wave can detect if organic molecules are present within these jets, providing evidence for microbial life being harbored within their originating subsurface oceans [3]. The primary reason that millimeter/sub-millimeter instruments struggle for opportunities in the outer solar system, is the matter of payload requirements. Existing

planetary science mm/sub-mm spectrometer instruments have required on the order of 50–100 W of DC power and weigh 15–25 Kg [5], [6], demanding a significant portion of a science payloads resources, making them unattractive for outer solar system missions where the available payload power and mass are so limited. Beyond the continued large flagship missions like the Rosetta Orbiter, NASA also envisions a whole other class of much smaller spacecraft exploring the outer solar system like the interplanetary cube-satellite (cubesat) proposed in [4] as a part of a recent NASA mission concept study. In this example, an extremely compact 20 cm x 20 cm x 30 cm spacecraft is sent to explore planetary objects as far away as Neptune. These and other similar small platforms are expected to have a much lower associated mission cost and therefore create many new opportunities for outer solar system exploration. However, their payload capacity is limited to under 5 Kg of mass with DC power consumption under 15W [4]. For mm/sub-mm spectroscopy to take advantage of these new small platform opportunities, much technical progress is needed to reduce the mass and power consumption of these instruments from the scales of the MIRO-like implementations, while still maintaining the level of sensitivity and measurement fidelity required to conduct meaningful scientific investigations.

Towards this goal, we have proposed, developed, and demonstrated in sub-orbital flight, a next generation spectrometer instrument capable of meeting the strict payload mass and power requirements of these future small-platform deep space missions. The instrument leverages the latest advances in mm/sub-mm electronics technology, exploiting recent advances in commercial mm-wave complimentary metal-oxide semiconductor (CMOS) electronics [7], advances in CMOS high-speed signal processing technology [8], advances in InP-monolithic microwave integrated circuit (MMIC) based amplifier technology [9], and advances in micro electro mechanical system (MEMS) based THz switching technology [10]. From a top-level perspective, the instrument demonstrates the same two frequency bands as the MIRO instrument on the Rosetta Orbiter [5], A 183 GHz spectrometer targeting the H_2O spectral line at 183.310 GHz, and a tunable 540–600 GHz spectrometer which provides spectral coverage for detecting several isotopes of water (H_2O^{16}, H_2O^{18}, D_2O) as well as a wide range of gas species (O_3,NH_3, NO_2, N_2O, CH_3OH, …) that are important planetary science targets.

This paper details the design of both the 183 GHz and 540–600 GHz spectrometers including their receiver systems, their back-end processing systems, their integration into sub-orbital payload, and their operation conducting measurements during a sub-orbital near-space flight.

II. SUB-ORBITAL VALIDATION OF MM/SUB-MM SPECTROSCOPIC INSTRUMENTATION

Validating mm-wave and sub-mm-wave spectroscopic systems with a lab or ground based test is difficult as it requires the beam to have a path length of several hundred meters within the gas being sensed to have an accurate representation of the signal-to-noise (SNR) encountered in real planetary exploration conditions. Additionally, this gas path must be held at representatively low pressures (1-100 millitorr range) meaning a pressure vessel must be used. Coupling the mm/sub-mm wave radiation in and out of the pressure vessel will incur losses, again limiting the applicability of ground measurements towards predicting actual planetary exploration conditions. Beyond just the target gas, sub-mm-wave spectroscopic measurements need to be made with a background representative of the cold space in actual exploration conditions so cryogenics must be used to simulate the backdrop of the experiment. At hundreds of meters of path length, the beam diameter from a reasonable antenna becomes prohibitively large to fully occupy with a cryogenic load. Given these considerations, conducting a laboratory test of our sub-mm instrument provides limited insight towards predicting its performance in exploration conditions, and so we instead elect to characterize the system in a sub-orbital flight demo.

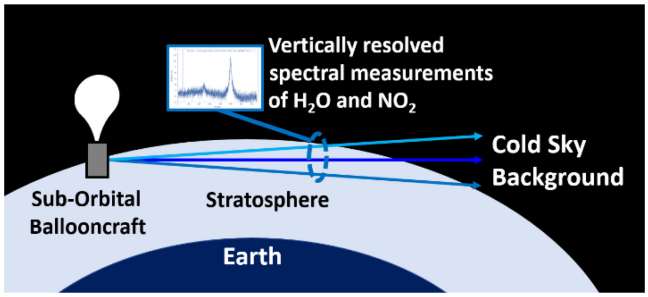

FIGURE 1. Limb-sounding from a sub-orbital balloncraft that produces vertically resolved measurements of gas species within Earth's stratosphere.

Sub-orbital flights aboard high-altitude balloncraft (HABs) can access the upper limits of Earth's stratosphere (30 km–40 km) where space-like conditions exist in terms of atmospheric pressures and temperatures, but unlike full sized missions, HABs are modest in associated cost. For this reason, the environment these balloncraft operate in is often referred to as "near-space". The upper stratosphere contains a wide range of trace gasses and an abundance of water vapor, which is continuously tracked by several Earth orbiting mm/sub-mm instruments for Earth science and climate studies, including the Microwave Limb Sounder (MLS) instrument on the Aura spacecraft [11] and recently launched Tempest radiometer demonstration [12]. From this position in the upper stratosphere, a process called limb-sounding can be performed where the stratosphere is observed horizontally from the balloncraft against the cold background of space to detect trace gases and water vapor. The angle of the observation relative to the plane of the Earth's surface can be swept to produce vertically resolved measurements as depicted by Fig. 1. By performing these limb-sounding measurements the spectroscopic system can be characterized and validated in an environment representative of a planetary exploration mission. For the demonstration flight the 183 GHz

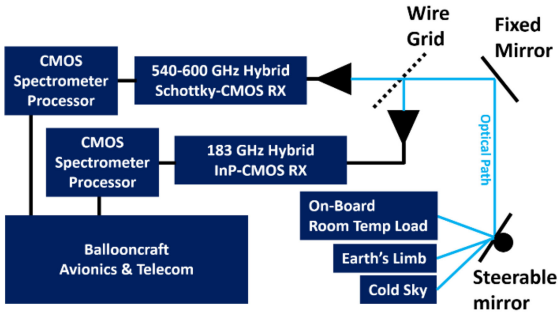

FIGURE 2. Block diagram of the compact 180 GHz and 540–600 GHz spectrometer instrument showing optical coupling path and major electronic sub-systems.

channel targets the H_2O rotational emission spectral line at 183.31 GHz while the 540–600 GHz channel sounds the O_3 rotational emission spectral line at 570.99 GHz.

III. INSTRUMENT ARCHITECTURE

Fig. 2 shows a block diagram of the overall instrument highlighting the optical beam path and key electronic sub-systems. The instrument's optical path begins with a 15 cm primary mirror mounted on the balloon craft which can steer the beam towards Earth's limb at varying degrees of elevation to produce the vertically resolved measurements described in the previous section. Beyond Earth's limb, the mirror can also steer the beam towards cold sky at a +45 degree angle above Earth's horizon, and towards an on-board load that is closed-loop heated to room temperature. This combination of viewing the 2 °K cold sky and 293 °K on-board load provide the two reference points required to calibrate the radiometric brightness of the receiver by de-embedding the frequency response of the receiver and characterizing any drift in receiver gain that occurs during the observations. The input beam is split via a wire-grid allowing both receivers to share the same optical path. In this configuration the 540–600 GHz receiver captures the horizonal polarization while the 183 GHz receiver captures the vertical polarization.

The 183 GHz receiver is implemented with a combination of a 183 GHz MMIC LNA and CMOS system-on-chip (SoC) that provides an integrated local oscillator (LO), down-conversion mixer and intermediate frequency (IF) amplification chain. The 540–600 GHz channel is implemented with a GaAs Schottky mixer receiver driven with a CMOS SoC based LO. Additionally, the 540–600 GHz channel carries a MEMS based single-pole double throw (SPDT) Dicke switch that provides an alternative to using the optically steered hot load for calibration. The MEMS Dicke switch offers the advantage of being able to switch to a room-temperature calibration load much faster than the large 15 cm mirror can steer optically and could potentially eliminate the need for a motorized mirror all-together in future instruments. Note: In this demonstration we still require the steerable mirror to calibrate the 183 GHz channel as it does not have a similar MEMs Dicke switch. This configuration affords us the opportunity to calibrate some

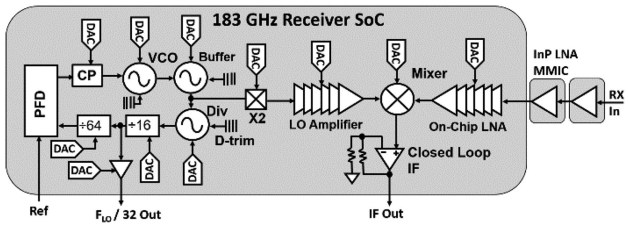

FIGURE 3. Block diagram of the 183 GHz receiver system showing key elements within the CMOS SoC and external MMIC LNA amplifiers [13], [14].

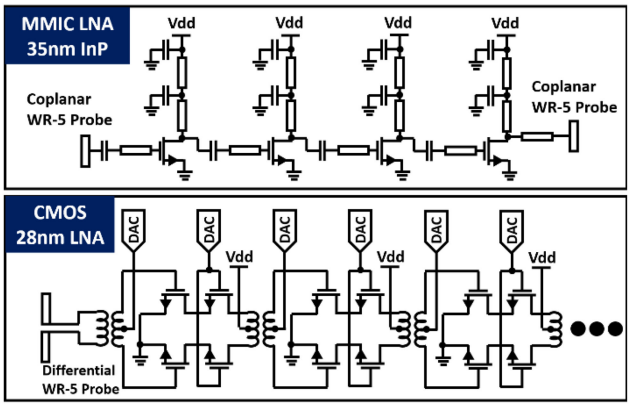

FIGURE 4. Schematics diagram of the MMIC and CMOS mm-wave front-end 183 GHz low noise amplifiers [13], [14].

of the 540–600 GHz limb-sounding measurements with the MEMs Dicke switch, while calibrating others with the steerable mirror only, and allows us to directly compare the quality of calibration between the two methods. Back-end processing (digitization and computing the power spectral density of each receiver output) is accomplished via a pair of CMOS-SoC based spectrometer processors which contain an integrated digitizer, and all the needed digital signal processing (DSP), which allows for a compact and low power solution compared with FPGA-based solutions (see comparisons in [8]). The baseband processors for both the 183 GHz and 500-600 GHz channels are identical.

IV. CMOS-INP 183 GHZ RECEIVER

Fig. 3 shows a block diagram of the 183 GHz spectrometer receiver system which consists of a set of InP HEMT MMIC pre-amplifiers followed by a CMOS SoC containing more amplification, a down conversion stage, and an integrated LO. InP MMIC technology offers much lower noise temperatures than CMOS mm-wave circuitry, so two InP stages are placed in front of the CMOS receiver to suppress its noise contributions. Design of the MMIC LNA is reported in detail in [13] while detailed design of the CMOS SoC is reported in [14]. For the purposes of this article, we just report an overview of the key details for each of the chips. Fig. 4 shows circuit schematics of the front-end amplifiers in the 183 GHz receiver

chain. The InP MMIC pre-amplifiers (two chips/modules cascaded) are implemented as a traditional common source amplifier (4 stages per chip) with traditional distributed matching elements (series and shunt stubs). The 183 GHz amplifier on the CMOS chip is implemented as a differential transformer coupled structure, with each stage in a cascode configuration. The transformer coupling allows DC biases to be fed at the center point of each transformer without the bias circuitry being in the RF pathway.

As the transformer matching networks have almost no coupling near DC, low frequency stability of the amplifier is essentially guaranteed without needing to apply additional stabilization elements. For the CMOS chip the bias of each stage is controlled by an independent DC digital to analog converter (DAC) which allows software to program and optimize the bias voltage at each stage to achieve the best receiver noise temperature. The DAC bias settings are selected with a software algorithm during bench testing that searches for the bias settings that give the lowest noise temperature. In-flight we just use the static values selected by this bench test. Conceptually, the bias calibration could be run in flight by extracting the Y-factor using the cold sky and room temperature load, although we have not implemented that approach in this flight demonstration. The circuit schematics for the CMOS downconverter and IF stages are shown in Fig. 5. The down converter itself is a traditional double-balanced Gilbert-cell type mixer, except that it is again transformer coupled with DAC at the center-taps to provide the bias conditions. Similar to the CMOS amplifier biases, the biases for the downconverter are bench optimized with software to find the settings with the lowest noise temperature.

One interesting aspect of the CMOS receiver not covered in reference [14] is the configuration of the IF circuitry and its effects on both receiver bandwidth and receiver drift. Fig. 5 shows two IF structures, one open-loop and one closed-loop. We fabricated two variants of the CMOS receiver, one with 3 stages of the open-loop variant of the IF amplifier and one with 3 stages of the closed-loop variant of the IF amplifier. The open-loop variant is a simple differential pair with a resistive load, so the gain of the stage depends heavily on the transistor parameters

$$V_{out} = gmR\,V_{in} \tag{1}$$

Where R is the load and gm is the transconductance of the input differential transistor pair. Since gm is dependent on device temperature and supply conditions, we would expect the gain of the amplifier to drift continuously making calibration more difficult. Alternatively, the closed-loop variant's gain expression depends only on the ratio of the two resistors for frequencies within the amplifier's loop bandwidth

$$V_{out} = \frac{R_o}{R}\,V_{in} \tag{2}$$

Where Ro/R is the ratio of the feedback network. Since the gain depends only on the ratio of resistors, the gain of the structure should be much less sensitive to drift arising from

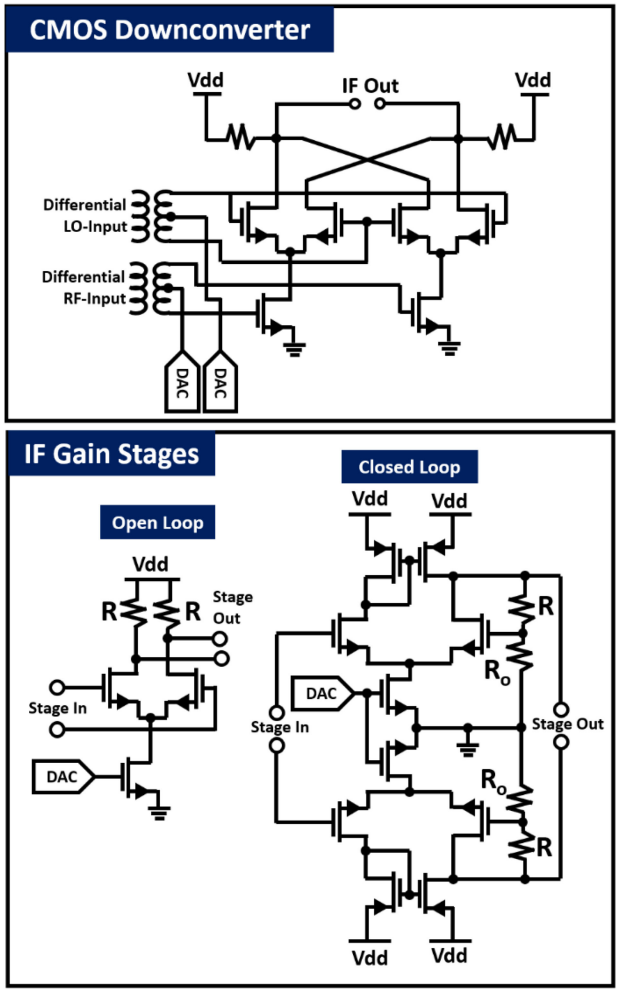

FIGURE 5. Schematic diagrams of the CMOS downconverter stages and IF amplifier stages for open and closed loop variants [13], [14].

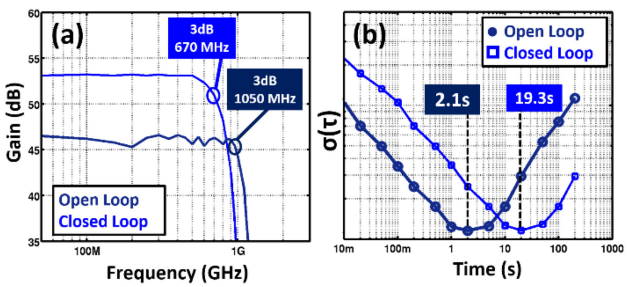

FIGURE 6. (a) Measured gain behavior of the IF with open and closed-loop IF configurations. (b) Measured Allan time behavior of open and closed-loop IF configurations.

supply and temperature variations. This is confirmed in the measurements shown in Fig. 6 where the IF bandwidth and Allan deviation was measured for the overall CMOS receiver with each IF amplifier variant. As seen in Fig 6(a) the simpler open-loop structure with less parasitic capacitance has almost a factor of 2 more bandwidth than the closed-loop variant. However, the Allan time (quantifies how long in time the gain remains invariant) measurements shown in Fig. 6(b)

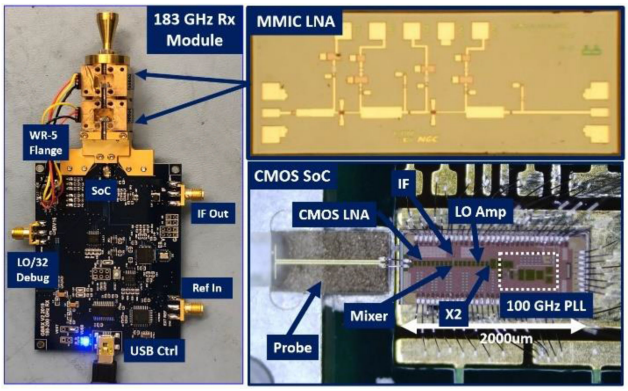

FIGURE 7. **Photographs of the 183 GHz receiver module with close up images of CMOS SoC assembly and MMIC LNA chip.**

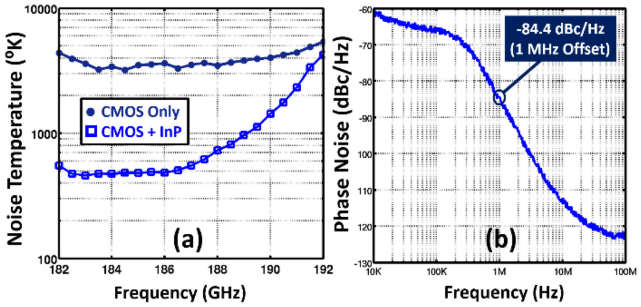

FIGURE 8. **(a) Measured noise temperature performance of the 183 GHz receiver showing the CMOS SoC only performance, and performance with the InP MMIC LNA pre-amplifier present. (b) Measured phase noise of the 183 GHz LO used for down-conversion.**

TABLE 1. **Summary of the 183 GHz Receiver**

Receiver Characteristic	Value
Noise Temperature at 183.31 GHz (H_2O)	505 °K
Phase Noise (at 1 MHz from carrier)	-84.4 dBc/Hz
Total Receiver Allan Time	19.3 sec
IF Bandwidth	670 MHz
CMOS LO Coverage	182-192 GHz
CMOS Power Consumption	515 mW
MMIC Power Consumption	103 mW
Total 183 GHz Receiver Mass	162 g

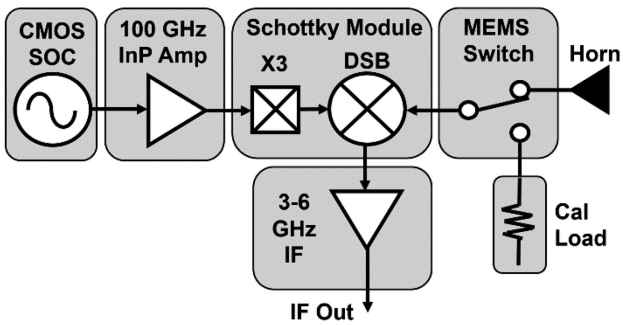

FIGURE 9. **Block diagram of the 540–600 GHz receiver system showing key components.**

demonstrates a substantial advantage in the closed-loop variant's gain drift over the open loop variant (19.3 seconds as oppose to only 2.1 seconds). For a radiometer or spectrometer application, a long Allan time is extremely critical as it constrains how often you need to calibrate the receiver chain. For our steerable mirror, having to steer to the room-temperature load and cold sky every 2.1 seconds would place demanding mechanical requirements on the mirror and greatly limit observation time as the mirror would be in motion during the majority of the 2.1 second cycle. For this reason, the closed-loop variant with its 19.3 second Allan time was selected for the sub-orbital demonstration (and would be the likely choice for a full-sized mission). It allows for reasonable observation times, and for the steering mirror to operate at reasonable mechanical speeds while still meeting the calibration time constraints.

Again, referring back to Fig. 3, the LO for the receiver is an integrated integer-n phase-locked loop (PLL) operating at 90-100 GHz that is ultimately doubled with an on-chip doubler to the 183 GHz band. The PLL loop uses an injection locked frequency divider, and inductively peaked current-mode divider to provide the high frequency phase feedback to the phase detector comparing to the input reference clock. The detailed design of the PLL is considerably more complex compared to the other circuitry, and the authors refer the reader to reference [14] which presents the full set of PLL design details.

Fig. 7 shows photographs of the MMIC amplifier chip, the 183 GHz CMOS SoC receiver, and the overall packaged module with a PCB containing the support control and power electronics. The input to the CMOS SoC is coupled to a WR-5 waveguide flange via a quartz probe similar to the package reported in [15]. The MMICs are packaged in traditional waveguide blocks which provide bias connections and WR-5 input and output flanges. The PCB that supports the CMOS chip has inputs for an ultra-stable-reference oscillator (USO) that the LO-PLL is referenced against, as well as a USB port to control all the DAC bias settings throughout the chip. Fig. 8a shows the overall noise temperature performance of the module where a T_{sys} of 505 °K was measured at the 183.310 GHz H_2O line frequency. For comparison, the noise temperature of the CMOS receiver only without the MMIC preamplifiers is also shown and remains in the 3000 °K range across the entire 182-192 GHz band (the frequency range over which the PLL remains phase-locked). Also shown in Fig. 8b, is the measured phase noise of the LO at the input to the mixer as measured by a stand-alone PLL chip. Finally, Table 1 summarizes the key performance and payload characteristics of the overall 183 GHz receiver system.

V. CMOS-MEMS-SCHOTTKY 540–600 GHZ RECEIVER

Fig. 9 shows the block diagram of the 540–600 GHz receiver system. The primary receiver component is a combination

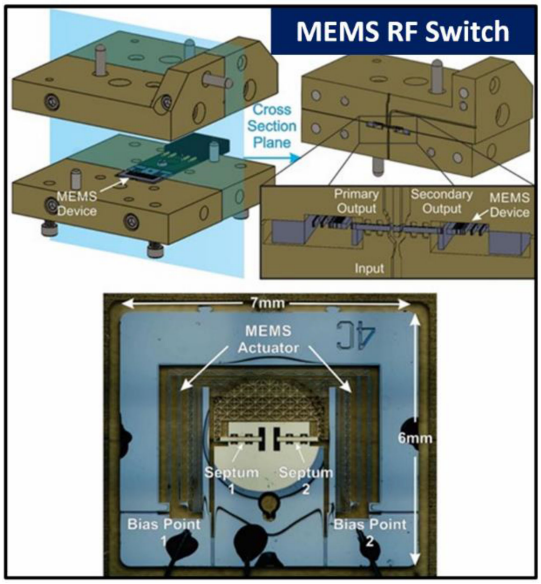

FIGURE 10. Construction diagram and photograph of 500–600 GHz waveguide-MEMS Dicke switch [10].

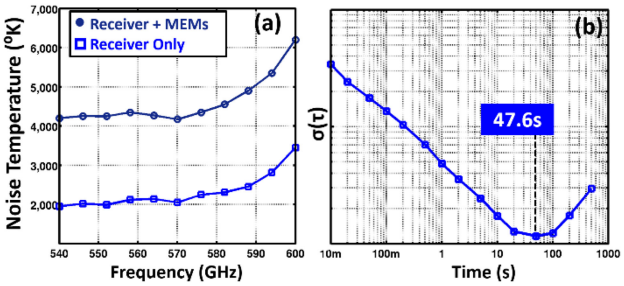

FIGURE 11. (a) Noise temperature measurements of the 540–600 GHz receiver system with and without the demo-flight version of the MEMS switch present between the feed horn and receiver input. (b) Allan time measurement of the 540–600 GHz receiver including the MEMS switch.

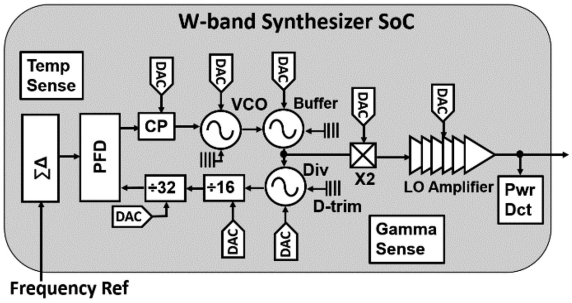

FIGURE 12. Block diagram of the CMOS 90–102 GHz (W-band) synthesizer SoC showing key circuit blocks [16].

LO tripler and 540–600 GHz sub-harmonic mixer chip implemented in JPL's GaAs Schottky technology and packaged in a WR1.5 waveguide block. The mixer/receiver input is fed from the 540–600 GHz waveguide MEMs switch which can toggle between connecting the receiver to the feed horn out to the optical path or connecting it to WR1.5 waveguide calibration load. The load itself is a purchased catalog component from VDI. The complete design details and characterization of the MEMS switch are presented in [10], and a summary of its construction is shown in Fig. 10.

While the variant of the Dicke switch in [10] was carefully characterized for insertion loss and isolation on a network analyzer, the variant flown in the sub-orbital demonstration (modified only for geometry constraints) was assessed indirectly by measuring the receiver noise temperature with a Y-factor measurement. This used a LN2 soaked free-space absorber placed in front of the horn with and without the switch inserted between the feed horn and receiver input. For the hot-load in this measurement we used both the waveguide load and a room temperature free-space absorber placed in front of the horn finding no significant difference between the two measurements. The T_{sys} taken with the VDI load shown in Fig. 11 where it can be seen the noise temperature is inflated by a factor of $\sim$2 when the MEMS Dicke switch is inserted versus the receiver and free-space absorbers alone. This leads us to an estimated insertion loss of 3.0 to 3.2 dB. For completeness we also measured the Allan time of the receiver with the MEMS switch to ensure that mechanical vibration or temperature changes were not modulating the insertion loss.

The IF path of the receiver is constructed out of commercially purchased catalog amplifiers from mini-circuits as well as several catalog bandpass filters from K&L microwave. The LO pathway has two components, a custom CMOS synthesizer SoC that provides a phase-locked LO from 90-102 GHz, and an LO amplifier implemented with commercially available W-band InP amplifier MMICs from Teledyne.

A block diagram of the CMOS 90-102 GHz synthesizer SoC which drives the 540–600 GHz receiver system is shown in Fig. 12 with the complete design details presented in reference [16]. The chip uses a 50 GHz fundamental PLL with an injection locked buffer and injection locked frequency divider to close the phase feedback loop. After the initial 50-to-25 GHz stage the remaining stages of the feedback divider path are implemented as current mode logic circuits. The charge pump and phase detector are traditional topologies, while a Multi-stAge noise Shaped (MASH-1-1-1) delta-sigma modulator pre-scales the reference pathway of the PLL, providing fractional operation (forming a fractional-N PLL). Clocking of the chip is provided by an external ultra-stable oscillator (USO) which provides a common temperature independent 50 MHz reference signal throughout the entire payload. The chip then doubles the 50 GHz PLL and amplifies it with a CMOS on-chip mm-wave amplifier to provide a final chip output across 90-102 GHz. Similar to the 183 GHz SoC, each mm-wave amplifier stage is transformer coupled and contains a DAC at the winding center taps to provide digital bias control for optimization purposes. Unlike the 183 GHz SoC, the 100 GHz SoC also has small tuning devices called

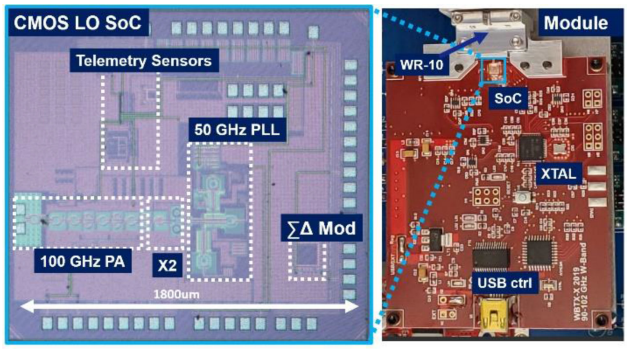

FIGURE 13. Photograph of CMOS synthesizer chip and LO module assembly showing key inputs and outputs.

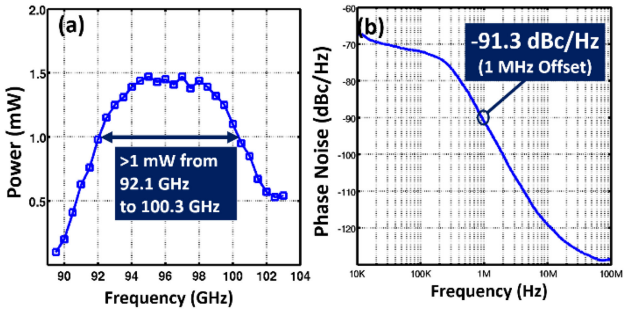

FIGURE 14. (a) Measured output power of the CMOS synthesizer chip across the locking range. (b) Phase noise of the CMOS synthesizer at 95 GHz (mid-band).

digitally controlled artificial dielectrics (DiCADs) [16] which are loaded transmission line structures that allow the reactive tuning and impedance matching of each stage in the doubler and amplifier chain to be optimized. Beyond the core mm-wave circuitry the SoC chip also contains several telemetry functions including a temperature sensor, output power sensing feedback and even a radiation sensor that monitors the total ionized dose the chip receives in the near-space environment [17]. Fig. 13 shows a die photograph the CMOS chip with the major circuit blocks identified as well as a photograph of the overall LO module with WR-10 waveguide flange and supporting PCB. For the sub-orbital demonstration flight, the SoC was identical to the one reported in [16] but repackaged to improve the mechanical robustness of the module. Fig. 14 shows the measured output power and phase noise of the LO module. The LO module is controlled via a USB interface.

Fig. 15 shows a photograph of the entire 540–600 GHz receiver system identifying the key components, while Table 2 lists the performance and characteristics of the entire receiver.

VI. CMOS SPECTROMETER PROCESSORS

Both the 183 GHz and 540–600 GHz spectrometers in the demonstration use identical back-end processing systems based on the "SVII" spectrometer processor SoC chip with design and architecture details fully presented in [18] and [19] (SVII denotes the 7'th gen). Although identical, the two

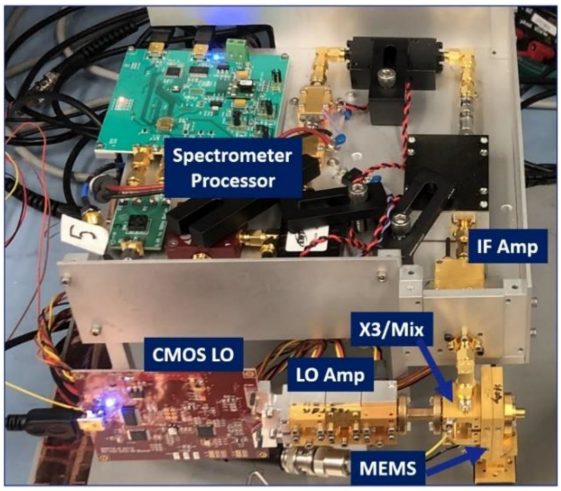

FIGURE 15. Photograph of the full 540–600 GHz receiver system with key components identified.

TABLE 2. Summary of the 540–600 GHz Receiver

Receiver Characteristic	Value
Noise Temperature at 570.99 GHz (O_3)	4300 °K
Phase Noise (at 1 MHz from carrier)*	-75.7 dBc/Hz
Total Receiver Allan Time	47.6 sec
IF Bandwidth	3000 MHz
LO Coverage	500-600 GHz
CMOS LO Power Consumption	670 mW
IF Amplification	2900 mW
LO Amplification	3700 mW
MEMS / X3 / Mixer Bias	50 mW
Total 540-600 GHz Receiver Mass	1.4 Kg

*referred to 570 GHz (mid-band)

back-ends are operated at a different clock frequencies so different Nyquist bandwidths are processed that match each receiver system. The 183 GHz channel is clocked at 1.5 GS/s to provide 750 MHz of bandwidth, while the 540–600 GHz channel is clocked at the chip's maximum speed of 6 GS/s to provide 3 GHz of Nyquist processing bandwidth. Fig. 16 shows a block diagram of the "SVII" back-end processor chip with key sub-systems identified.

The chip has two interleaved 3-bit input analog to digital converters (ADCs) that operate up to 6 GS/s and sample the input IF signal. A third "replica" ADC is also included for track how fabrication process, supply and temperature conditions are affecting the ADC system without needing to take it offline for calibration. The ADC output is demultiplexed by 2 prior to the decoder which converts thermometer code to binary code. Following decoding the signal is further demultiplexed by 8 into 32 parallel data streams. A time domain windowing function is applied prior to FFT processing to prevent leakage between FFT bins. The FFT computation itself is an

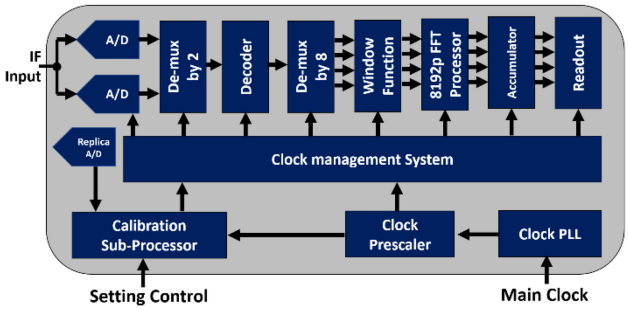

FIGURE 16. Block diagram of the "SVII" Spectrometer processor used as the back end for both the 180 GHz and 540–600 GHz spectrometer channels.

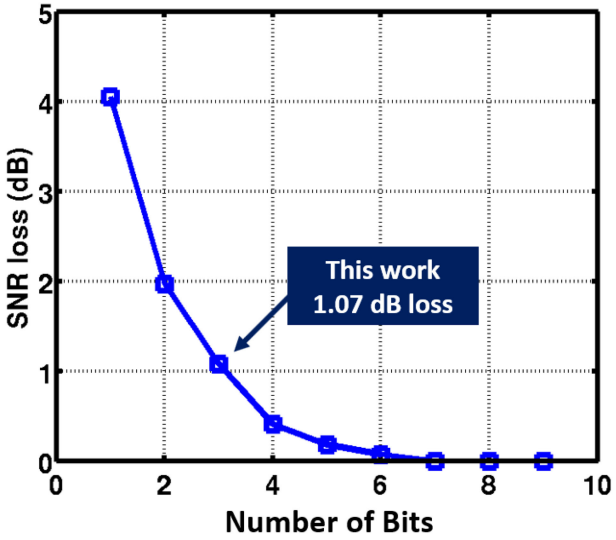

FIGURE 17. SNR loss due to quantization noise as a function of ADC bit depth for back-end spectrometer processors.

8192-point complex radix-2 FFT processor using serial-delay feedback (SDF) units and pipeline units to implement transform operations. After the FFT, the power spectral density (PSD) is computed and averaged in an on-chip high-speed SRAM based accumulator prior to readout to the payload host computer via a USB link. The main clock for the processor is generated from an on-chip PLL that is phase-locked onto the same USO references used for the two receivers' LO systems. A clock pre-scaler allows this synthesized clock from the on-board PLL to be sub-divided by factors of 24,816 or 32 to set the Nyquist bandwidth of the processor. Each setting results in a different chip power-consumption since the processor core's dynamic power is highly dependent on clock speed. Operating digital and mixed-signal circuitry at such high-speed clocks (up to 6 GHz) creates problems closing static timing (setup/hold constraints) across all temperatures and process conditions so instead of static clocking, we employ an integrated clock management system (CMS) which monitors and adjust clock timings and phases throughout the chip to ensure timing operations are met. To oversee all the calibration operations of the analog portion of the processor chip, as well as management of the CMS and clocking sub-systems the chip contains a dedicated calibration sub-processor. This sub-processor runs firmware for calibration tasks related to trimming the ADCs analog settings (about 125 I and V biases total) and the over 100 different clock control knobs within the CMS system. Interfacing to the calibration sub-processor from the payload computer is again accomplished through use of a USB interface.

One of the most important considerations for back-end processor processing is the bit resolution of the digitizer. As the bit resolution or "bit depth" increases, the power consumption of the processor grows exponentially as multipliers become exponentially larger in terms of logic implementation. At the same time the logic requires more physical area, so die size and overall cost also increases exponentially. However, if the bit resolution is too coarse, the added quantization noise of the digitization process will degrade the SNR of the spectral signal substantially. If we assume the input signal is a Gaussian distribution (typically true in spectrometer signals) with a variance of σ that is quantized to N levels (N being even, $N = 2n$), and with spacing ε (in units of σ), the quantization efficiency η_Q, defined as the loss in SNR due to digitization and added quantization noise, can be expressed as [18]:

$$\eta_{Q(N=2n)} = \frac{\frac{2}{\pi}\left(\frac{1}{2} + \sum_{m=1}^{n-1} e^{-m^2\varepsilon^2/2}\right)^2}{\left(n-\frac{1}{2}\right)^2 - 2\sum_{m=1}^{n-1} m\,\mathrm{erf}\left(\frac{m\varepsilon}{\sqrt{2}}\right)} \tag{3}$$

If we further assume the IF gain is well designed to excite the full input scale of the ADC (easily accomplished through programmable attenuation or gain control), the expression in (3) can be evaluated versus the number of bits to produce the plot shown in Fig. 17. As discussed in [18] the selected 3-bit resolution provides a reasonable tradeoff between total digital processor power (on the order of 1.3 W) and an SNR loss of only 1.07 dB. Practically, some margin needs to be left between the IF signal power and the ADC full scale to avoid saturation, so we expect SNR loss due to digitization to be slightly larger, in the 1.3 to 1.4 dB range. The ADC subsystem is depicted in Fig. 18 showing the main architecture of each of the two interleaved flash ADCs, the reference generation circuitry, and the calibration scheme using the replica ADC.

The reference voltage levels for the flash ADCs are generated by 8-bit DAC units so that any gradients or errors in fabrication can be calibrated out from software (this is described in the later section). An anti-kickback protection buffer (2-stage opamp) is placed between the reference generator and comparator array to prevent switching noises from coupling into the voltage reference system. The ADC itself is a typical flash ADC with 7 level comparators and traditional track and hold (THA) and distribution amplifier (DA) circuitry.

The biases throughout the ADC are established with current and voltage DACs using a technique called replica biasing. Placing bias and signal monitoring circuitry within the high-speed ADCs would add considerable parasitic capacitance,

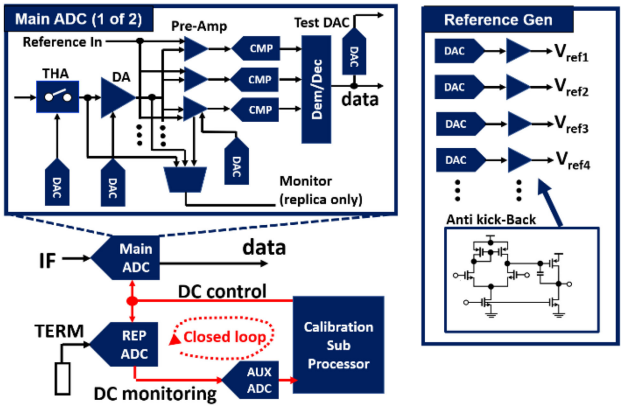

FIGURE 18. ADC sub-system of the "SVII" spectrometer processor showing the closed loop replica calibration [19].

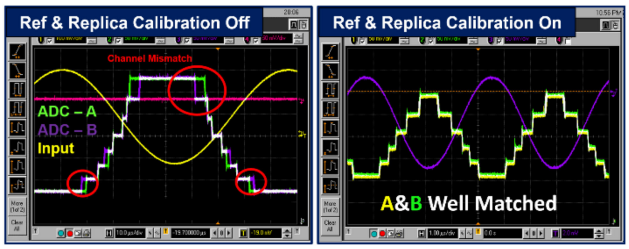

FIGURE 19. Waveforms from the two interleaved ADCs with the full calibration system disengaged and activated showing how the variation between the two ADCs are calibrated.

limiting the high-speed operation, so instead we build an exact duplicate called a "replica ADC" which has the same knobs and bias conditions as the main signal ADCs. We then monitor the replica ADC in closed loop to compensate for supply, fabrication variation, and temperature effects while commanding the settings to both the replica and main ADCs in parallel, allowing calibration to occur in the background while the spectrometer processor is running. Fig. 19 demonstrates how the mismatches between the two main interleaved ADCs are calibrated out through both the replica and reference calibration process (the software approach is described later in this section).

The CMS system that drives the ADC, demultiplexing, decoding and digital signal processor within the SVII SoC is shown in Fig. 20 where a PLL first synthesizes a 3 GHz signal from an external reference. Note 3 GHz corresponds to 6 GS/s since the two main ADCs are configured to operate on opposite clock edges. The PLL output is pre-scaled to either pass div by 12,48,16 or 32 versions of the clock allowing for programmable operating bandwidth (allowing the spectral resolution to be varied by software). Next, a combination of a coarse and a fine phase shifter is placed in each clock signal that is distributed to each sub-system within the SoC. Each phase shifter allows full 360-degree rotation at either the full or sub-divided clock frequency it operates on. This allows the timing relation between any two sub-systems to be advanced or retarded, allowing inter-stage timing to be met under all

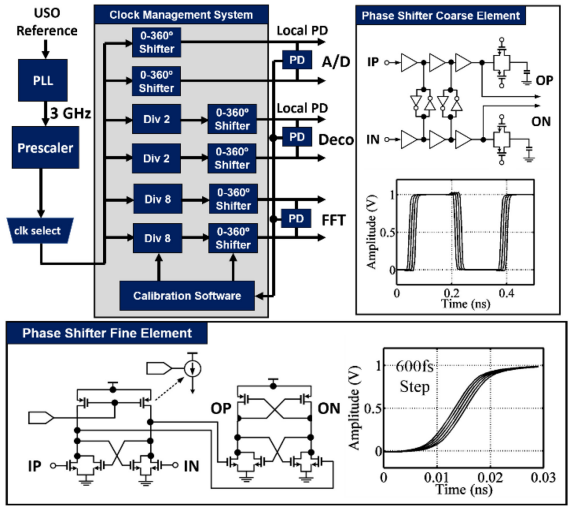

FIGURE 20. Clock management system (CMS) showing block diagram with local phase detectors and circuit schematics for both coarse and fine phase shifters [18].

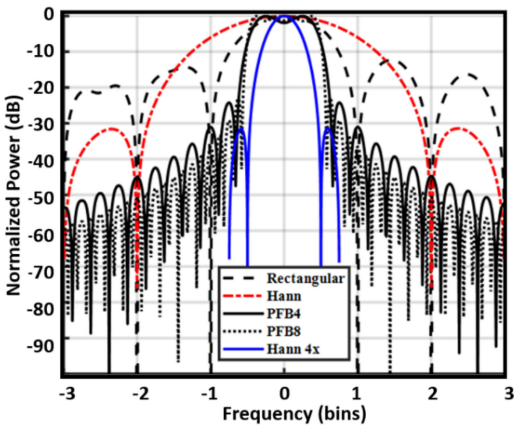

FIGURE 21. Spectrometer channel shapes for various Nyquist length, and super-Nyquist length windowing functions.

temperature, process, or supply conditions. To establish the clock phase relationships required for the processing, local phase detectors are embedded within each block that compares the phase of the received clock to the phase of the clock from neighboring or subsequent processing blocks and read back to the calibration sub-processor.

A second critical concern for spectrometer processors is the effect of windowing distortion. If an FFT is computed on a time-domain series without a windowing function applied first, energy from each spectral bin will leak into adjacent bins. Beyond this, energy at concentrated frequencies within an FFT bin will contribute to bin's overall amplitude differently depending on where they lie within the bin's boundaries. This effect is often referred to as spectrometer "channel shape" and is illustrated in Fig. 21.

The plot in Fig. 21 demonstrates the channel shape for both Nyquist-length and longer windowing functions. The worst case is a rectangular function which has high leakage to adjacent changes and substantial amplitude distortion within the

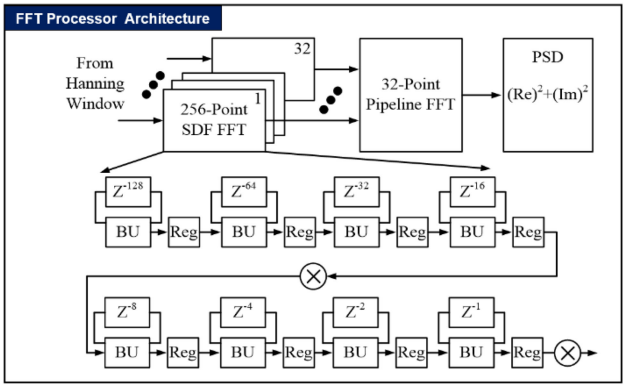

FIGURE 22. Block diagram of the "SVII" spectrometer SoC's FFT processor architecture using a 256-point SDF FFT followed by a 32-point pipeline FFT.

channel. The Hanning window is a Nyquist-length window which improves both the amplitude distortion and leakage to adjacent channels. Polyphase Filter Bank (PFB) windows are longer than Nyquist-length (meaning the window function contains more points than the time-domain sequence) offer superior channel shapes at the cost of much increased hardware complexity. Given the added complexity a PFB would entail, we elected to use the simpler Nyquist-length Hanning window for this version of the spectrometer processor.

The FFT processor itself is structured as a 256-point SDF coarse stage followed by a 32-point pipeline FFT fine stage using traditional butterfly processing units (BUs) as shown in Fig. 22. The FFT architecture is traditional except as described in [18], the twiddle rotation factors for each multiplier stage are computed "on-the-fly" using a coordinate rotation digital computer (CORDIC) processor to perform the trigonometry computations instead of a look-up table to allow for higher operating clock speeds.

Fig. 23 shows a photograph of the "SVII" spectrometer chip's micro-assembly with key blocks identified as well as the overall PCB module. To support the high impulse current of the processor 5-mil wide ribbon bonds were used for the supply connections while wire-bonds were used for the signal connections. The PCB itself has several components including two parallel USB interfaces, one sending captured spectral data to the host computer and a second separate USB interface to interact with the calibration sub-processor. Beyond that the PCB board has a microcontroller equipped with 8 kB of flash memory to store calibration settings for the chip.

Calibration of the "SVII" spectrometer processor chip is accomplished by connecting the module in a closed loop system with additional calibration software run on a host computer (either a benchtop computer, or the payload computer of the balloon craft) as shown in Fig 24. The calibration process can be run in flight provided the spectrometer can be interrupted from acquiring data. When the spectrometer chip has incorrect analog settings for the ADC, or has a timing violation in the CMS system, it results in the presence of timing/code mismatch spurs like those highlighted in the spectrum shown in Fig. 25a. These mismatch spurs provide an elegant avenue

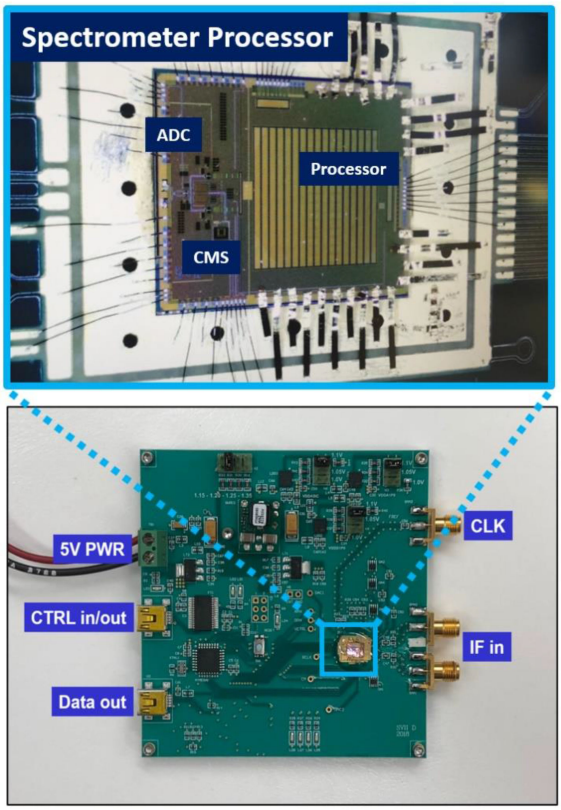

FIGURE 23. Photograph of the "SVII" Spectrometer SoC chip and PCB module highlighting the micro-assembly.

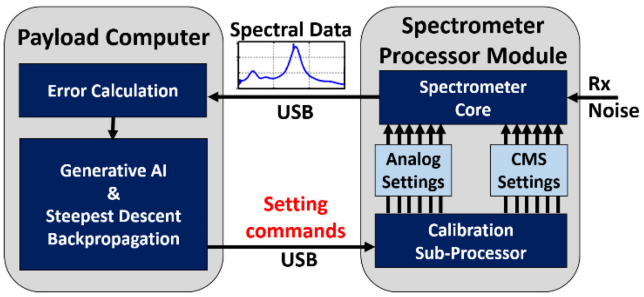

FIGURE 24. "SVII" Spectrometer SoC calibration using external generative AI software on the payload computer.

for performing calibration using their total energy as an error function E

$$E = \left(\sum_{k=1}^{N} (X_{k+1} - X_k) \right)^2 \tag{4}$$

where X_n is the amplitude of the n'th PSD bin and N is the total number of PSB bins. An artificial intelligence engine running on the host computer iteratively tunes the CMS and analog calibration settings of the chip. While we have experimented with several different generative AI engines freely available within the tensorflow^{tm} development environment from google, we have found that simple genetic algorithms using steepest descent backpropagation provide reasonable

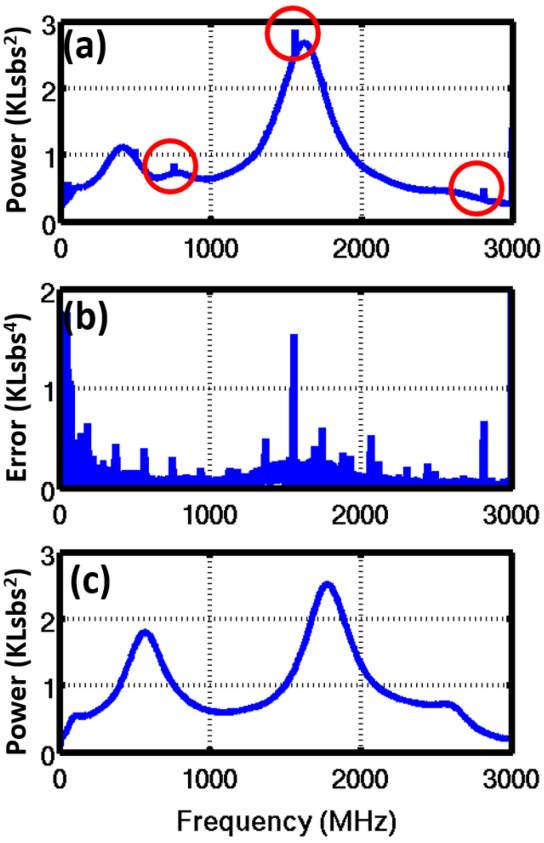

FIGURE 25. **(a) Spectrometer output without calibration performed showing error spurs. (b) Calibration error signal the generative AI engine is trained to optimize. (c) Spectrometer output spectrum after calibration is applied.**

calibration times of only a few minutes. Fig. 25(c) shows the spectrum for the same receiver IF input signal as Fig. 25(a) after the calibration has been applied. Note that the overall spectral shape has also changed from correcting the calibration parameters. This overall change in spectral shape is a result of the sampling instant of the two interleaved ADCs initially being spaced incorrectly in time and then being corrected. The correct alignment is confirmed not only by the absence of spurs, but more importantly by the phase detector within the CMS system placed between the two ADC clocks that confirm the two ADC sampling phases are indeed 180 ° apart. It is this dual-check of the phase detectors plus the spurs from the AI-based calibration loop, that resolve any ambiguity exiting between possible correct settings. Once calibration is completed the settings are stored within the non-volatile flash memory of a microcontroller on the spectrometer processor's PCB module. The characteristics of the spectrometer processor are summarized in Table 3.

VII. SUB-ORBITAL FLIGHT ACTIVITY

The entire instrument including the 183 GHz receiver, 540–600 GHz receiver, both spectrometer processors and optical components were integrated into a compact high altitude stratospheric balloon craft along with a host computer, and a

TABLE 3. **Summary of "SVII" Spectrometer Processor**

Spectrometer Characteristic	183 GHz Config	540-600 GHz Config
Bandwidth	750 MHz	3000 MHz
Bit Depth	3 bits	3 bits
Window Function	Hanning	Hanning
Calibration Scheme	Steepest Des.	Steepest Des.
Module DC Power Consumption	730 mW	2305 mW
Spectrometer Mass	155g	155g

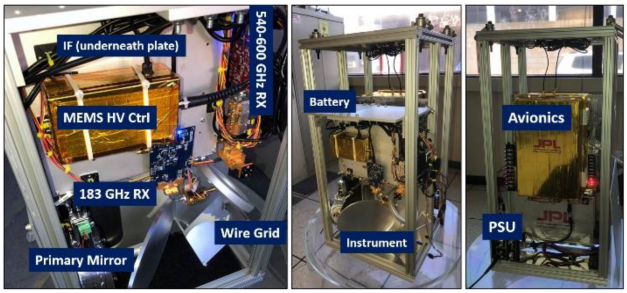

FIGURE 26. **Integration of the spectrometer instrument into the "ReckTangLE" high-altitude stratospheric balloon craft.**

variety of other near-space flight related modules: power supplies and power monitoring systems, a thermal management system consisting of temperature sensors and heaters placed throughout the payload to make sure various systems don't freeze below their operating temperature ranges, an L-band transmitter for transmitting measurement and payload health telemetry data (DC conditions, temps, …) back to the ground station, an FAA transponder system for safety purposes, a GPS, gyroscope and compass for tracking and navigation, and a termination system consisting of a parachute and pyrotechnic explosives for its deployment. The thermal system maintains the spectrometer payload to a temperature of 16 °C +/− 1 °C eliminating the need for specialized packaging or materials. The full balloon craft was designated the Reck-Tang Limb-sounding Experiment or "ReckTangLE" after the two investigators (both authors on this article). Fig. 26 shows photographs of the integration of the instrument into the balloon craft highlighting the key systems and optical components.

Launch of the balloon craft occurred on Oct 17, 2019, from Ft Sumner, New Mexico and was supported by the NASA Columbia Scientific Balloon Facility (CSBF).

The balloon itself was a 1.128 million cubic feet polymer balloon. Fig. 27 provides several photographs of the launch setup, payload, and a capture from the in-flight camera, providing a sense of scale of the overall balloon and flight train compared to the balloon craft platform itself. Fig. 28 provides a map of the sub-orbital flight from its launch in NM to its termination in the eastern Texas panhandle, and a plot of all the telemetry exchanges that occurred during the 5-hour flight, and altitudes at which the telemetry exchanges were made. The balloon operated at a float altitude of 38000 m (124600 ft)

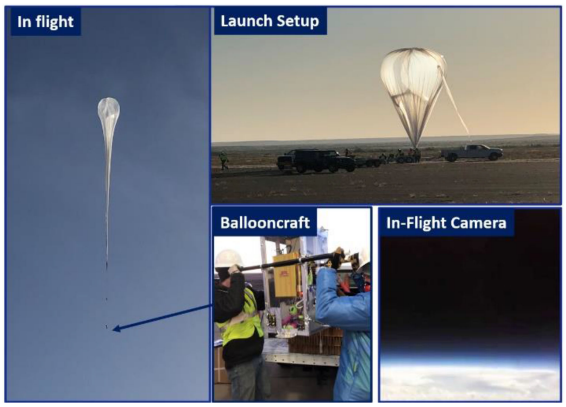

FIGURE 27. Photographs of the launch setup and balloncraft in flight (immediately after launch), as well as a capture from the in-flight camera.

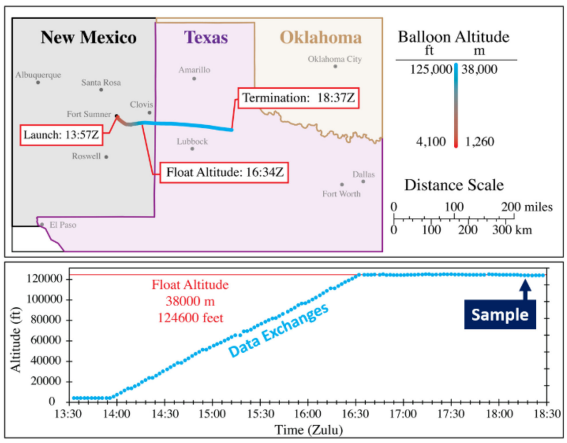

FIGURE 28. Flight profile showing map of flight path, balloncraft altitude and telemetry data exchanges [20]. .

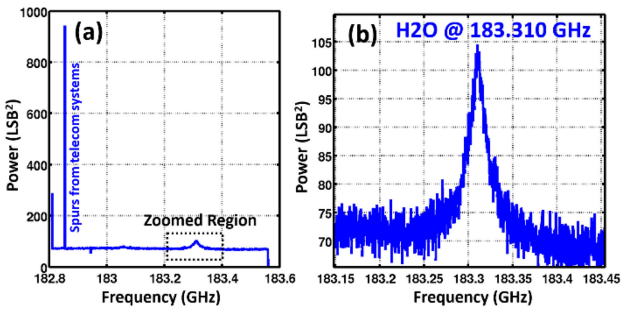

FIGURE 29. (a) Captured detection of stratospheric water vapor during the float phase of the flight from the 183 GHz spectrometer using the calibration scheme described in [21]. (b) Zoom in view around the H_2O signal.

during the observation phase of the flight. The flight tracking data is publicly available on the NASA-CSBF website [20].

Fig. 29 shows one captured 183 GHz spectrum from Earth's limb during the float (stable altitude) phase of the flight in both (a) full bandwidth and (b) zoomed in formats. The background receiver noise shape was calibrated using the room temperature load and cold sky calibration data following

TABLE 4. Comparison of This Work to the Previously Flown MIRO Planetary Sub-mm-Wave Spectrometer [1], [5]

Channel	183 GHz	540-600 GHz
Receiver DC Power	**0.62 W**	**6.6 W**
Spectrometer DC Power	**0.73 W**	**2.3 W**
Steerable Mirror DC Power	**2.2 W** (shared)	
Total Instrument Power	**12.45 W**	
Spectrometer Total Mass	**155g**	**155g**
Receiver total Mass	**162g**	**1.4 Kg**
Optical Components Mass	**1.2 Kg** (shared)	
Total Instrument Mass	**3.1 Kg**	
Receiver Sensitivity	**505°K**	**4300°K**

Comparison to MIRO Instrument [1],[5]	
Total Instrument Power	**68 W**
Total Instrument Mass	**20.32 Kg**
183 GHz Receiver Sensitivity	**807°K**
500-600 GHz Receiver Sensitivity	**3580°K**

the post-processing method employed in [21], and reveals a sensitive detection of stratospheric H_2O.

Unfortunately the 540–600 GHz receiver did not operate correctly in flight. Although the authors cannot offer a definitive explanation for the failure, the explanation most consistent with the DC, control, and other control telemetry logs suggests that the sudden vibration of launch may have dislodged the signal cable that controls the MEMs switch rendering it stuck pointing towards the calibration load, not the antenna port. This explanation is supported in that we see no radiometric contrast in the 540–600 GHz data as the mirror was steered between the various limb angles, room-temperature load and cold sky. We know the mirror must have steered correctly as the 183 GHz receiver that shares the same mirror and optical path produced correct stratospheric H_2O detections. Additionally, although many of the components were damaged during the landing impact, the authors were able to successfully re-test several surviving components including the LO amplifiers, mixer, IF amplifier further providing evidence towards the envisioned scenario of the MEMS Dicke switch being stuck connected to the calibration load. The MEMs switch itself had undergone a lifetime test of over 1 million cycles and vibration testing prior to the flight [10], leading us to believe it was the control cable that came lose not a malfunction of the switch itself.

VIII. CONCLUSION

In this paper we have described the development of a 183 GHz and 540–600 GHz spectrometer instrument and back-end spectrometer processor for future planetary exploration missions. By leveraging advances in CMOS SoC technology, InP MMIC technology, and MEMS THz technology we have demonstrated a considerable reduction in mass (6.5X) and power (5.5X) when compared with the most recently flown

sub-millimeter-wave spectrometer (the MIRO instrument on the Rosetta orbiter).

A top-level comparison of this work to the MIRO instrument is provided in Table 4 which shows the reduction in power and mass while providing improved sensitivity in the 183 GHz band, and comparable sensitivity in the 540–600 GHz band. The developed 183 GHz & 540–600 GHz spectrometer was flown aboard the NASA-CSBF ReckTangLE sub-orbital balloocraft and the 183 GHz spectrometer instrument successfully sounded stratospheric water vapor to yield the expected detections. The 540–600 GHz channel failed in flight due to a suspected problem with cabling related to the MEMS Dicke switch. At the time this article was prepared, a repeat sub-orbital flight of the 540–600 GHz spectrometer is planned for late 2021 although exact payload details are not yet decided.

ACKNOWLEDGMENT

The authors are grateful to NASA WFF & CSBF for supporting the launch operations and sub-orbital flight of the ReckTangLE balloocraft. The authors are also grateful to their collaborators at TSMC for their excellent 65nm and 28nm foundry support. Part of this work was carried out at the Jet Propulsion Laboratory, California Institute of Technology under contract to the National Aeronautics and Space Administration.

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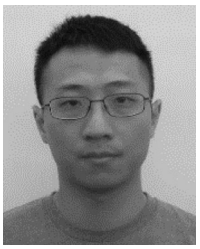

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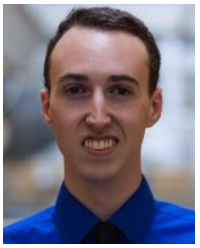

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