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Investigation on Short-Circuit Characteristics and Failure Modes of SiC Planar MOSFETs With Linear and Hexagonal Topologies

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***Abstract*— This article compares and evaluates the single pulse short-circuit robustness of silicon carbide (SiC) MOSFETs with linear and hexagonal cell topologies under different gate voltages, bus voltages, and case temperatures. The short-circuit failure mechanisms of the linear and hexagonal cell topologies are studied. A new switching model for gate failure and thermal runaway short-circuit failure modes is proposed and analyzed. The robustness performance of the linear and hexagonal cell topologies is compared and evaluated under the same short-circuit power for the first time, fully revealing the comprehensive impact mechanism of cell topologies on the short-circuit robustness for SiC MOSFETs.**

***Index Terms*— Cell topology, failure mechanism, gate failure, MOSFETs, short-circuit, silicon carbide (SiC), thermal runaway.**

I. Introduction

BASED on the advantages of high bandgap width, high critical breakdown electric field, and high thermal conductivity for silicon carbide (SiC), SiC MOSFETs have been widely used in medium- and high-voltage power electronic fields, making them the best choice for high operating temperature, high frequency, and high-efficiency applications [1], [2], [3]. Since the commercialization of SiC MOSFETs, with the progress of process technology, the power density of SiC MOSFETs has been continuously increasing. Higher power density brings miniaturization and low-cost advantages but also leads to a significant decrease in short-circuit capability [4], [5].

Many studies have been conducted on the robustness and failure modes of single pulse short-circuits for SiC MOSFETs. For SiC trench MOSFETs, it is found that the asymmetric trench has two short-circuit failure modes, gate failure, and thermal runaway, depending on the bus voltage level, while the double trench exhibits thermal runaway at all bus voltages [6]. In terms of SiC planar MOSFETs, there are two independent short-circuit failure modes, namely thermal runaway and gate failure [7], [8], [9]. Typical failure points and waveforms for two short-circuit failure modes are shown in Fig. 1(a) and (b). The thermal runaway mode is caused by the positive feedback between the high lattice temperature and parasitic bipolar junction transistor (BJT) conduction during the short-circuit process, resulting in device burnout [10], [11]. Gate failure is a unique mode of SiC MOSFETs, which may be due to cracking of the interlayer dielectric (ILD) between gate and source under high-temperature stress [12], [13], [14], [15], [16], [17]. The molten Al infiltrates these cracks, resulting in a short circuit between the gate and the source. Different gate and bus voltages can lead to different failure modes [8], [14], [18]. The occurrence conditions of two short-circuit failure modes have been distinguished from a thermodynamic perspective in [8], but there is a lack of detailed mechanism analysis and experimental comparison. The specific switching mechanism between the two failure modes still needs further detailed research.

Commercial SiC planar MOSFETs typically use linear or hexagonal cell topologies. Previous studies [19], [20] have conducted detailed comparative evaluations of the static and dynamic electrical characteristics of SiC MOSFETs with different cell topologies. The results show that hexagonal cell topologies have lower specific ON resistance due to their higher channel density, while linear cell topologies have better-blocking characteristics and high-frequency advantages. Up to now, there is still a lack of detailed comparative research on the short-circuit robustness of SiC MOSFETs with linear and hexagonal cell topologies. The vast majority of studies on short-circuit robustness and failure mechanism are based on SiC MOSFETs with linear cell topology, while there is relatively little research on hexagonal cell topology devices. In addition, due to the interference of power density differences, the potential short-circuit robustness impact mechanism of linear and hexagonal cell topologies is difficult to further explore. This article provides a detailed research on the short-circuit robustness differences and failure mechanisms

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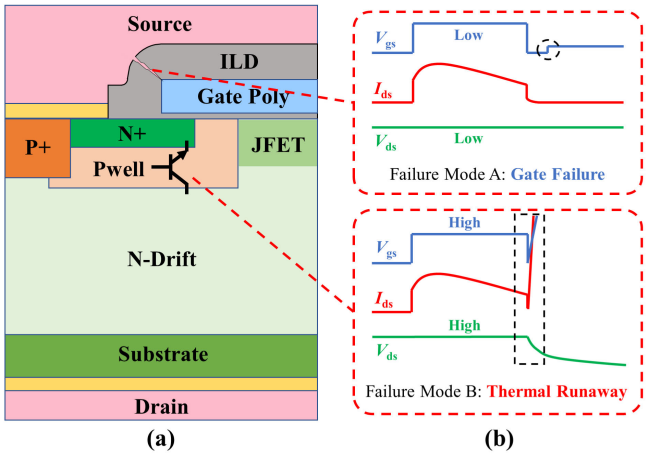

Fig. 1. Two short-circuit failure modes of SiC MOSFETs: gate failure and thermal runaway. (a) Cell failure points. (b) Typical failure waveforms.

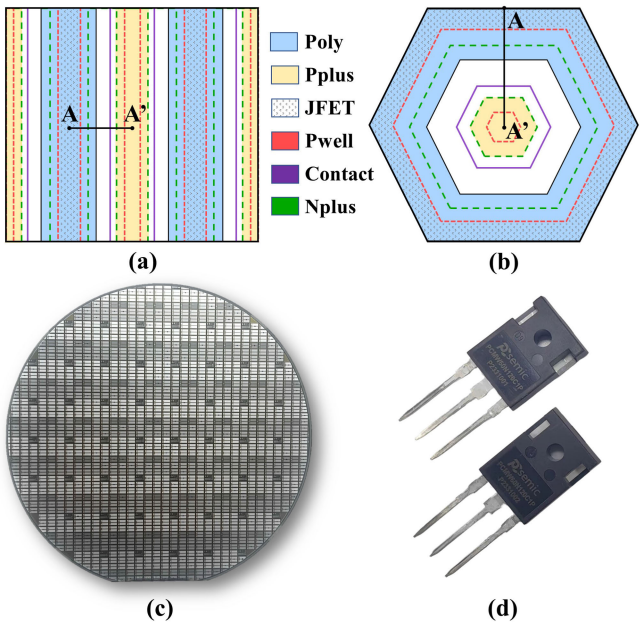

Fig. 2. Cell topologies for SiC MOSFETs. (a) Linear. (b) Hexagon. (c) Fabricated 1.2-kV SiC MOSFET MPW wafer. (d) SiC MOSFETs packaged in TO-247-3.

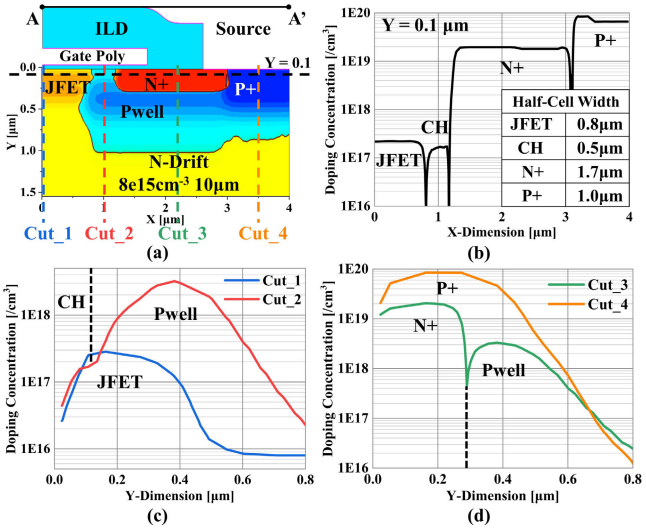

Fig. 3. (a) Developed SiC MOSFETs half-cell cross section at A–A′. Doping concentration distribution in the X-direction at (b) $Y = 0.1$ μm and in the Y-direction at (c) Cut_1 and Cut_2 and (d) Cut_3 and Cut_4.

of self-developed SiC MOSFETs with linear and hexagonal cell topologies under specific operating conditions, which has guiding significance for cell topology selection in different application scenarios.

The rest of this article is organized as follows. In Section II, the single pulse short-circuit robustness differences of the linear and hexagonal cell topologies are tested and compared under different gate voltages, bus voltages, and case temperatures. Based on failure analysis, Section III studies the short-circuit failure mechanisms of the linear and hexagonal cell topologies. Combining simulation analysis with test results, Section IV proposes a detailed switching model for two short-circuit failure modes. In Section V, under the designed equal power short-circuit test, the differences in short-circuit robustness are compared and evaluated for the first time, and the potential impact mechanism of cell topology on short-circuit robustness is revealed through 3-D cell temperature and stress simulation.

II. Short-Circuit Robustness Comparison

Based on a 6-in SiC MOSFET foundry, 1200 V SiC planar MOSFETs with linear and hexagonal cell topologies were manufactured. Fig. 2(a) and (b) show the linear and hexagonal cell topologies, respectively. The concentration of the epitaxial layer is $8e^{15}$ cm^{-3}, with a thickness of 10 μm. The concentration of N-substrate is $1e^{19}$ cm^{-3}, and the thickness is thinned to 180 μm. Taking the linear cell topology as an example, Fig. 3(a) shows the cell cross-sectional structure diagram at A–A′. The concentration distribution in the surface doping region is shown in Fig. 3(b), and the width of the key ion implantation region in the half-cell is presented. Fig. 3(c) and (d) show the corresponding doping concentration distributions of the Y-direction cutting lines in the JFET region, channel region, N+ source region, and P+ source region in detail. The fabricated multiproject wafer (MPW) of SiC MOSFETs with linear and hexagonal cell topologies is shown in Fig. 2(c). Based on the same packaging process, SiC MOSFETs with TO-247-3 package were completed as shown in Fig. 2(d). All devices under test (DUTs) adopt the same ion implantation parameters and chip manufacturing process to reduce interference in short-circuit robustness comparison. The same die size and standard packaging process ensure that the DUTs with two cell topologies have the same thermal resistance.

Linear and Hexagon are used to represent SiC MOSFETs with linear and hexagonal cell topologies, respectively. The difference in cell pitch is due to the process size limitation of the P+ region in Hexagon. We have conducted a detailed comparative study on the static and dynamic characteristics of Linear and Hexagon in [19]. Table I summarizes the relevant structural and characteristic parameters of Linear and Hexagon. The electric field concentration at the cell topology corners results in Hexagon having a lower breakdown voltage

TABLE I
KEY STRUCTURAL AND CHARACTERISTIC PARAMETERS OF SiC MOSFETs WITH LINEAR AND HEXAGONAL CELL TOPOLOGIES

Cell Topology	Pitch [μm]	S_{ACT} [cm^2]	Channel Density	JFET Density	BV [V]	V_{th} [V]	$R_{ds,on}$ [mΩ]
Linear	8.0	0.0973	0.125	0.200	1573	3.27	63
Hexagon	8.7	0.1023	0.174	0.334	1319	3.08	41

* BV @ V_{gs} = 0 V, I_d = 100 μA;
* $R_{ds,on}$ @ V_{gs} = 20 V, I_d = 20 A;
* V_{th} @ V_{ds} = V_{gs}, I_d = 0.4 mV/ $R_{ds,on}$.

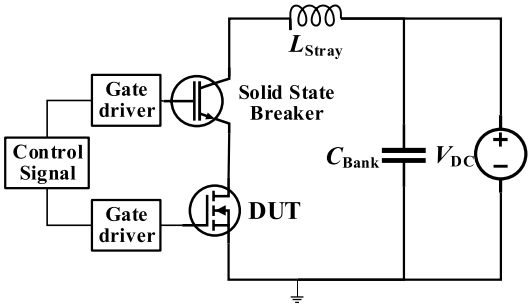

Fig. 4. Schematic of short-circuit testing platform.

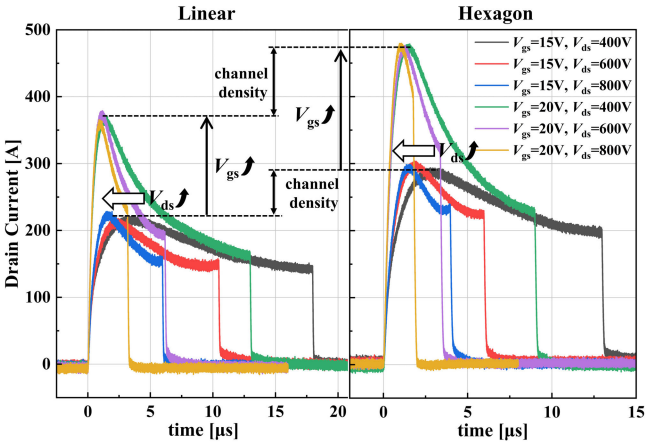

Fig. 5. Typical short-circuit current waveforms of Linear and Hexagon under different gate and bus voltages.

(BV). Due to the differences in channel and JFET density, the ON-resistance ($R_{ds,on}$) of Linear and Hexagon under V_{gs} = 20 V, I_d = 20 A are 63 and 41 mΩ, with corresponding specific ON-resistance ($R_{on,sp}$) of 6.1 and 4.2 mΩ cm^2, respectively.

The equivalent circuit diagram of the short-circuit test platform is shown in Fig. 4. The capacitor bank is 1800 V 400 μF to maintain the stability of the bus voltage during the short-circuit process. Before starting the test, use a high-voltage power supply to charge the capacitor bank to the specified bus voltage. Adjusting the width of the gate drive pulse to control the short-circuit pulse time, which gradually increases until the DUT reaches the short-circuit tolerance limit. Using a 1200 V 150 A insulated gate bipolar transistor (IGBT) as a solid state breaker, when the DUT reaches the short-circuit withstand limit and thermal runaway occurs, the circuit is quickly shut off by desaturation of the IGBT to ensure that the DUT does not explode and affect failure analysis. At least 3 min should be left between each short-circuit test to ensure that the heat generated by the previous test is fully dissipated.

The short-circuit characteristics of Linear and Hexagon were tested at room temperature under gate voltages of 15 and 20 V, and bus voltages of 400, 600, and 800 V, respectively. Fig. 5 shows the typical short-circuit current waveforms of Linear and Hexagon under different gate and bus voltages, taken from the latest test before short-circuit failure. The high V_{ds} during the short-circuit process causes DUT to operate in the saturation region, and the short-circuit current is mainly affected by V_{gs}. In addition, during the short-circuit process, it can be observed that I_{sc} gradually decreases after rising to peak short-circuit current (I_{peek}). This is because as the lattice temperature gradually increases during the short-circuit process, although the channel electron mobility of the DUT increases, the drift region resistance also increases (the bulk electron mobility decreases), and its proportion in the total ON-resistance increases accordingly [21], [22], resulting in a gradual decrease in I_{sc} after reaching I_{peek}. By changing the short-circuit heating power, V_{ds} affects the corresponding time of I_{peek} and the decreasing rate of I_{sc}. By horizontal comparison, it can be seen that Hexagon has a higher short-circuit current than Linear due to its higher channel density.

The short-circuit withstand time (SCWT), I_{peek}, ultimate short-circuit energy (E_{sc}), and short-circuit failure modes of DUTs are summarized in Table II. To compare the differences and trends in short-circuit robustness more intuitively, the SCWT, E_{sc}, and failure modes of Linear and Hexagon in Table II are graphically displayed based on different gate and bus voltages, as shown in Fig. 6. The short-circuit heating power rises with the increase of V_{gs} and V_{ds}, resulting in a significant decrease in SCWT and E_{sc} of both Linear and Hexagon. As shown in Fig. 6, under the same V_{gs} and V_{ds}, a Linear always exhibits higher SCWT and E_{sc} than Hexagon. This is mainly because, under the same short-circuit condition, a hexagon has a higher saturation current due to its higher channel density, resulting in a higher short-circuit power and poorer short-circuit robustness than Linear. Although Hexagon has a lower $R_{on,sp}$, its short-circuit robustness is worse than Linear under the same operating conditions, which requires a compromise between output characteristics and short-circuit capability according to application requirements.

In terms of short-circuit failure modes, multiple sets of DUTs were tested for each condition to eliminate the randomness of experimental results. For Linear, the short-circuit failure mode is always gate failure under the conditions of V_{gs} = 15/20 V, V_{ds} = 400 V and V_{gs} = 15 V, V_{ds} = 600 V. And the short-circuit failure mode is always thermal runaway under the conditions of V_{gs} = 15/20 V, V_{ds} = 800 V. For Hexagon, the short-circuit failure mode is always gate failure under the conditions of V_{gs} = 15/20 V, V_{ds} = 400 V. And the short-circuit failure mode is always thermal runaway under the conditions of V_{gs} = 15/20 V, V_{ds} = 800 V, and V_{gs} = 20 V, V_{ds} = 600 V. For the remaining conditions, the short-circuit failure mode appears to be in a critical state, as both gate

TABLE II
SHORT-CIRCUIT ROBUSTNESS TEST DATA OF LINEAR AND HEXAGON UNDER DIFFERENT GATE AND BUS VOLTAGES

Cell Topology	V_{gs} [V]	V_{ds} [V]	SCWT [μs]	I_{peek} [A]	E_{sc} [mJ]	Failure Mode*
Linear	15	400	20	218	1267	A
		600	11.5	218	1093	A
		800	6.4	224	874	B
	20	400	14	362	1155	A
		600	6.4	374	968	A
		800	3.2	361	686	B
Hexagon	15	400	14.5	285	1248	A
		600	6.8	297	926	A
		800	4.2	286	787	B
	20	400	10	468	1112	A
		600	4	465	821	B
		800	2	472	581	B

* Failure Mode A: **Gate Failure**;
* Failure Mode B: **Thermal Runaway**

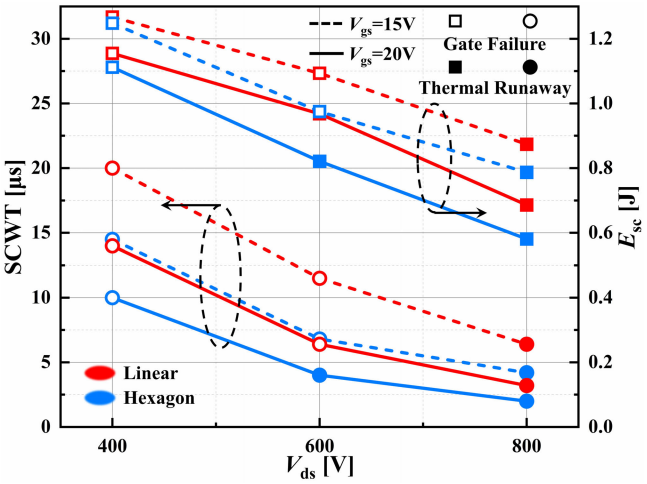

Fig. 6. Distribution plot of SCWT, E_{sc}, and failure modes of Linear and Hexagon under different gate and bus voltages (at T_C = 25 °C).

failure and thermal runaway modes have been observed in multiple DUT tests.

Further comparative studies were conducted on the short-circuit robustness of Linear and Hexagon at different case temperatures (T_C). The short-circuit robustness of DUTs was tested and evaluated at case temperatures of 100 °C and 150 °C with a fixed bus voltage V_{ds} = 600 V. The corresponding distribution of SCWT, E_{sc}, and failure modes is shown in Fig. 7. It can be seen that Linear still has better short-circuit robustness than Hexagon at high case temperatures. The SCWT and E_{sc} of Linear and Hexagon both show a decreasing trend with the increase of case temperature. This can be simply understood as a higher case temperature reducing the short-circuit energy required for the DUT to reach the critical failure temperature [9], [16], resulting in a decrease in the measured short-circuit robustness. In terms of short-circuit failure modes, multiple sets of DUT tests are also conducted to eliminate randomness. The results show that Linear with V_{gs} = 15 V always exhibits gate failure at T_C =

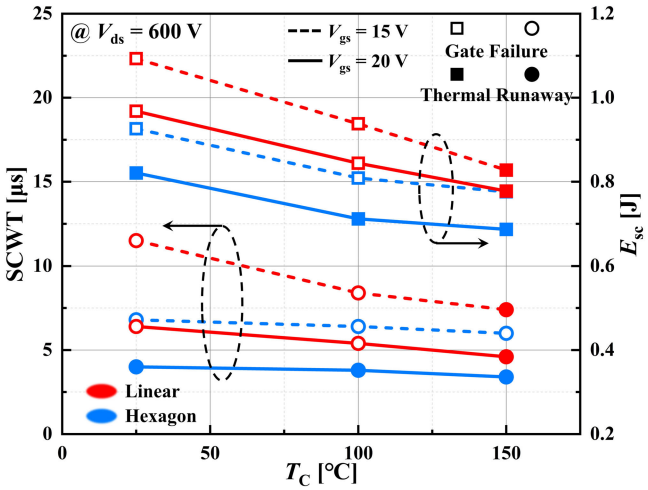

Fig. 7. Distribution plot of SCWT, E_{sc}, and failure modes of Linear and Hexagon under different case temperatures.

25 °C and 100 °C, while Hexagon with V_{gs} = 20 V always exhibits thermal runaway at different case temperatures. The remaining conditions are in a critical state where the failure mode is not fixed. It is worth noting that the Linear with V_{gs} = 15 V and V_{ds} = 600 V, which always exhibits gate failure at room temperature, also began to experience thermal runaway when the case temperature rises to 150 °C. This indicates that the probability of thermal runaway failure mode gradually increases with the increase of case temperature.

III. SHORT-CIRCUIT FAILURE MECHANISMS

Due to the protection of the solid-state breaker, the DUTs did not explode even in thermal runaway mode. Therefore, from the appearance of the package, there is no difference between the short-circuit failure DUTs and normal devices. The optical microscope (OM) images of chemical decap for Linear and Hexagon with different short-circuit failure modes are shown in Fig. 8. For thermal runaway mode, obvious thermal burnout points can be observed on the die surface of both Linear and Hexagon, randomly distributed in the active region. For gate failure mode, there are no obvious failure points on the die surface.

Using optical beam-induced resistance change (OBIRCH) to observe the failure points of Linear and Hexagon with gate failure modes. To capture a clear and accurate failure point location, partial Al removal is performed on the die surface of Linear. As shown in Fig. 9(a), two randomly distributed gate failure points were observed in the active region of Linear under V_{gs} = 2.0 V, I_{gs} = 2.6 mA.

Using a focused ion beam (FIB) to further accurately locate the gate failure point of Linear cell structure, the FIB observation region is marked in Fig. 9(a). During the process of gradually advancing toward the failure point, an obvious crack was found in the ILD layer between the gate and source, as shown in Fig. 9(b) and (c). In addition, tiny cracks were also observed in the Ti/TiN layer. This indicates that due to the difference in thermal expansion coefficient, the thermal stress caused by short-circuit high temperature exceeds the stress tolerance limit of the ILD and Ti/TiN layer, resulting in

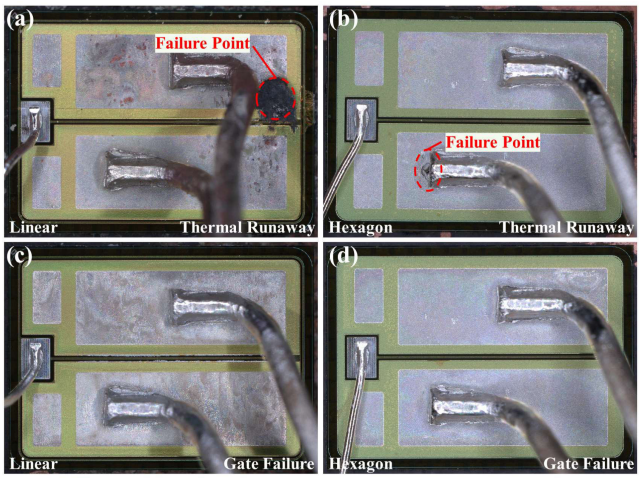

Fig. 8. OM images of chemical decap for DUTs under (a) thermal runaway mode of Linear, (b) thermal runaway mode of Hexagon, (c) gate failure mode of Linear, and (d) gate failure mode of Hexagon.

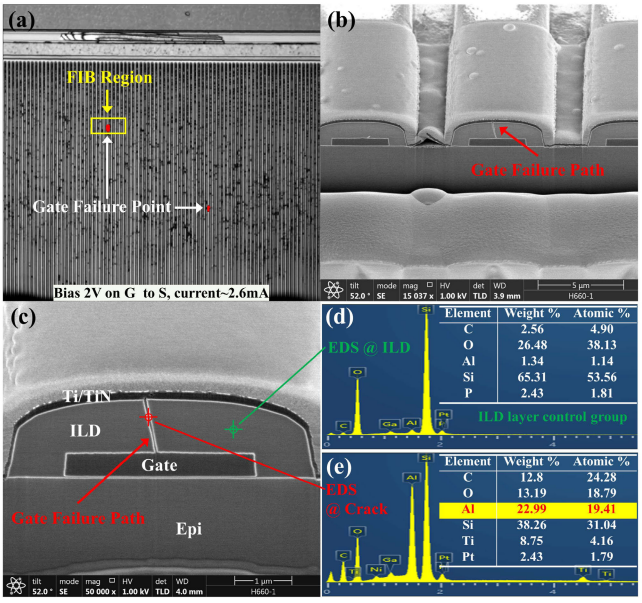

Fig. 9. (a) Short-circuit gate failure points of Linear. (b) and (c) FIB results of gate failure path in linear cell. EDS element analysis results of (d) normal ILD layer and (e) gate failure path for Linear.

cracking. The gate failure path of this Linear is located in the center of the ILD layer.

Using energy dispersive spectroscopy (EDS), element analysis was performed on the normal point and the crack point in the ILD region for Linear, and the corresponding element weight percentage and atomic percentage results are shown in Fig. 9(d) and (e), respectively. Comparing the elemental analysis results of these two points, it can be clearly observed that the Al element content at the crack point is significantly higher, indicating that molten Al infiltrated the ILD crack during the short-circuit gate failure process. In addition, during the FIB advancement process of Linear, some shorter ILD layer cracks were also observed at other cells, but no gate-to-source path was formed. This indicates that cracks are forming in the ILD layer at this short-circuit temperature, while Al has already melted. It can be seen that cracks are formed after the

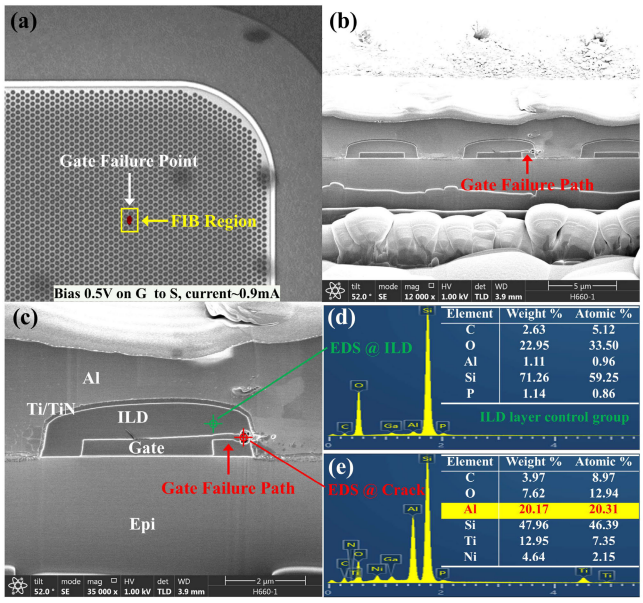

Fig. 10. (a) Short-circuit gate failure point of Hexagon. (b) and (c) FIB results of gate failure path in hexagonal cells. EDS element analysis results of (d) normal ILD layer and (e) gate failure path for Hexagon.

Al melting, and the ILD layer temperature of crack formation is higher than the Al melting temperature.

In terms of Hexagon, as shown in Fig. 10(a), a randomly distributed gate failure point was observed in the active region under $V_{gs} = 0.5$ V, $I_{gs} = 0.9$ mA. Similarly, FIB is used to further locate the gate failure point in the cell structure, and the corresponding observation region is marked in Fig. 10(a). During the process of gradually advancing toward the failure point, an obvious crack was found in the ILD layer between the gate and source, as shown in Fig. 10(b) and (c). There are also obvious cracks in the Ti/TiN layer here. This indicates that, similar to Linear, Hexagon also experienced cracking in the ILD and Ti/TiN layers during the gate failure process due to the high short-circuit thermal stress. Unlike Linear, the gate failure point of this Hexagon is located on the corner of the ILD layer.

Using EDS to perform element analysis on the normal point and the crack point in the ILD region for Hexagon, and the corresponding element weight percentage and atomic percentage results are shown in Fig. 10(d) and (e), respectively. By comparison, a significantly higher proportion of Al element was observed at the crack point, indicating that molten Al had infiltrated the crack and formed a short-circuit path between the gate and source. Unlike Linear, during the FIB advancement observation of Hexagon, no other unpenetrated cracks were observed except for this gate failure point.

Overall, the gate failure mechanisms of Linear and Hexagon are all due to the cracks in the ILD layer caused by short-circuit thermal stress, and the molten Al infiltrates into the cracks to form a short-circuit path between the gate and source. For the location of failure points and crack occurrence rates in the ILD layer, there is a slight difference between the analyzed Linear and Hexagon, which may be related to differences in cell topology or DUT randomness.

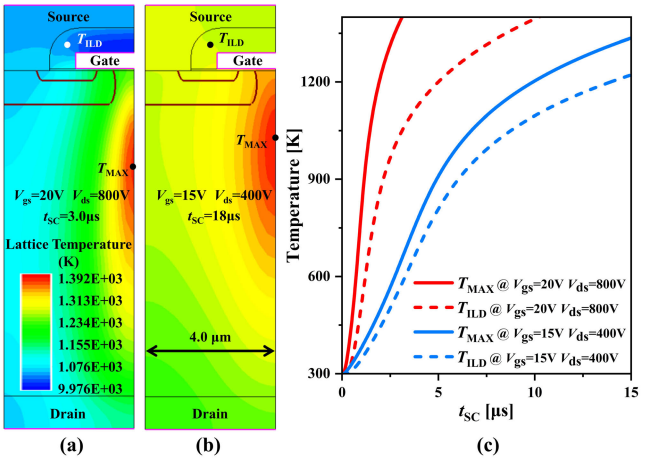

Fig. 11. Lattice temperature distribution of SiC MOSFETs in short-circuit mode: (a) V_{gs} = 20 V, V_{ds} = 800 V; (b) V_{gs} = 15 V, V_{ds} = 400 V; and (c) lattice temperature variation curve during short-circuit process.

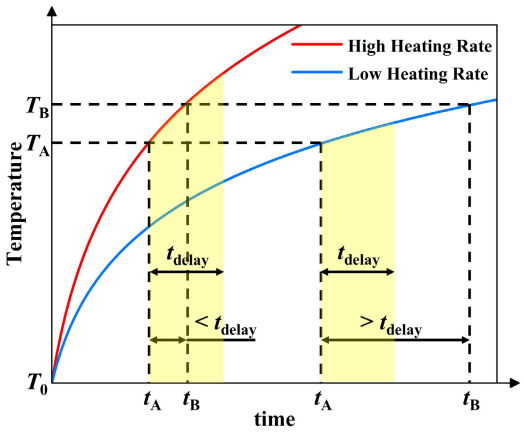

Fig. 12. Diagram of short-circuit failure mode switching model.

IV. Switching Model of Two Failure Modes

According to the mechanism of short-circuit gate failure and thermal runaway, the short-circuit failure mode of SiC MOSFET is closely related to the changes in the thermal distribution of the cell during the short-circuit process. The short-circuit characteristics of SiC MOSFETs were simulated using TCAD software, and the structural dimensions of the 2-D half-cell simulation model were referenced to Linear. The simulation physical models applied include impact ionization, high field saturation, temperature-dependent bandgap, and mobility, as well as thermodynamic-related models. Fig. 11(a) and (b) show the lattice temperature distribution at the corresponding short-circuit times under V_{gs} = 20 V, V_{ds} = 800 V and V_{gs} = 15 V, V_{ds} = 400 V, respectively. Fig. 11(c) records the changes in the maximum lattice temperature (T_{MAX}) and the ILD layer temperature (T_{ILD}). Under high gate and bus voltages, the heating rate of SiC MOSFETs is faster. Use T_A and T_B to represent the critical maximum lattice temperature for gate failure and thermal runaway, respectively. The presence of gate failure short-circuit mode indicates that T_A is lower than T_B. In theory, the temperature in short-circuit mode always rises to T_A first, but the failure mode is not entirely gate failure.

To provide a clearer explanation of the switching mechanism between short-circuit gate failure and thermal runaway mode, a delay time (t_{delay}) is introduced. From Fig. 11, it can be seen that the core heating position during the short-circuit process is below the JFET region, which is close to the thermal runaway failure point caused by parasitic BJT conduction. Considering the high thermal conductivity of SiC and the fast conduction of BJT, it can be considered that thermal runaway occurs when T_{MAX} rises to T_B. However, as mentioned in Section III, the failure point of gate failure mode is located in the ILD layer, far away from the T_{MAX} point. The critical ILD layer temperature at which cracking occurs is defined as T_{crack}. In terms of the gate failure mode, there is a delay time t_{delay} between T_{MAX} reaching T_A and DUTs experiencing gate failure. The t_{delay} is shown as follows:

$$t_{delay} = t_{transfer} + t_{degradation} \quad (1)$$

where $t_{transfer}$ is the time required for T_{ILD} to rise to T_{crack}, based on the heat transferred from the short-circuit core heating region. The $t_{degradation}$ is the time required for the ILD layer at the corner to form cracks due to thermal stress and for molten Al to penetrate into the cracks. Even if the short-circuit temperature rises to T_A, it still takes t_{delay} before gate failure occurs. For the convenience of subsequent model comparisons, the t_{delay} under different short-circuit conditions is simply treated as a fixed value.

For a more intuitive explanation, Fig. 12 simulates the temperature change curves of the device under different heating rates during the short-circuit test. Among them, the high heating rate corresponds to high bus voltage and high gate voltage, while the low heating rate corresponds to low bus voltage and low gate voltage. The t_A and t_B are the short-circuit times required for T_{MAX} to reach T_A and T_B, respectively. At the low heating rate, $t_B - t_A > t_{delay}$, meaning that when the T_{MAX} rises to T_A, after a delay of t_{delay}, the T_{ILD} rises to T_{crack} and device experiences gate failure. At the high heating rate, $t_B - t_A < t_{delay}$, meaning that before the T_{ILD} rises to T_{crack}, the T_{MAX} has already reached T_B within the t_{delay}, leading to direct thermal runaway.

Due to the step-like increase in short-circuit time when testing the short-circuit capability of SiC MOSFETs, the measurement time point also significantly affects the actual test waveform. This leads to unfixed failure modes in the short-circuit failure waveforms of different test groups under some critical short-circuit conditions, e.g., V_{gs} = 20 V, V_{ds} = 600 V. Introducing the measurement time point (t_M) and combining the proposed theoretical model with actual short-circuit test data, several typical failure waveforms of Linear were compared and explained, as shown in Fig. 13.

Using a simplified short-circuit failure mode switching model, t_A and t_B are the short-circuit times required for T_{MAX} to reach T_A and T_B, respectively. The t_{AF} and t_{BF} are the actual time points at which gate failure and thermal runaway occur, respectively. The t_{delay} is the delay time, and t_M is the time point of short-circuit measurement.

Fig. 13(a) is a typical waveform of gate failure. After a short-circuit of 11.5 μs, the DUT was turned off. But 3.5 μs later, a short circuit occurred between the gate and source.

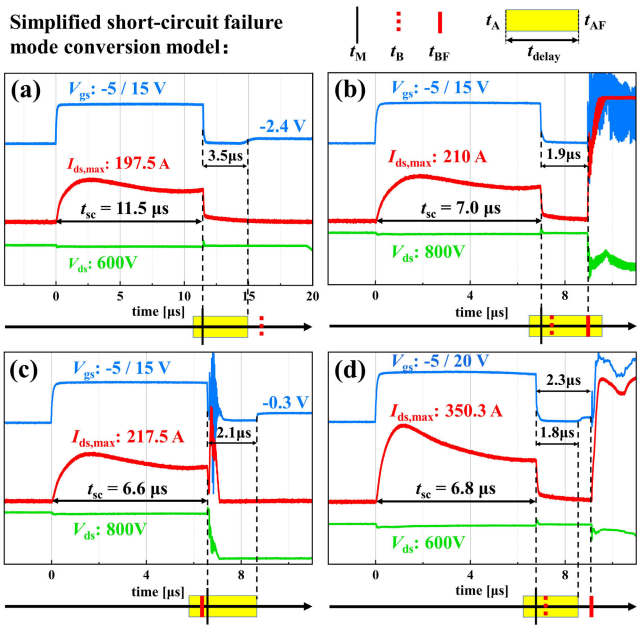

Fig. 13. Comparison diagram of short-circuit test failure waveforms and simplified models of Linear under different short-circuit conditions: (a) $V_{gs} = -5/15$ V, $V_{ds} = 600$ V; (b) and (c) $V_{gs} = -5/15$ V, $V_{ds} = 800$ V; and (d) $V_{gs} = -5/20$ V, $V_{ds} = 600$ V.

As shown in the simplified model in Fig. 13(a), under the short-circuit condition of $V_{gs} = 15$ V and $V_{ds} = 600$ V, t_A and t_B are far apart, satisfying $t_B - t_A > t_{delay}$. The short-circuit test time point t_M has reached t_A, but has not reached t_B. Therefore, due to the influence of t_{delay}, after a brief delay, cracks are generated in the ILD layer due to thermal stress, leading to gate failure.

Fig. 13(b) is a typical waveform of thermal runaway. After a short circuit of 7.0 μs, the DUT was turned off. But 1.9 μs later, the DUT experienced a thermal runaway. As shown in the simplified model in Fig. 13(b), under the short-circuit condition of $V_{gs} = 15$ V and $V_{ds} = 800$ V, t_A and t_B are relatively close and t_M is between t_A and t_B. However, due to the hole trailing current caused by high temperature during the short-circuit shutdown period [8], [23], the temperature will continue to rise under high bus voltage, reaching T_B. However, compared to the short-circuit period, the heating rate caused by the leakage current is lower, so the actual time to reach T_B is delayed to t_{BF}, which is still less than t_{AF}. Therefore, after the DUT is turned off, there is a delay time before thermal runaway occurs, and gate failure will not occur.

Fig. 13(c) is another typical waveform of thermal runaway. At the moment when the short-circuit pulse was turned off, the device reached the short-circuit withstand limit, and the drain current rapidly increased. As shown in the simplified model in Fig. 13(c), under the short-circuit condition of $V_{gs} = 15$ V and $V_{ds} = 800$ V, t_A and t_B are relatively close, satisfying $t_B - t_A < t_{delay}$. In this case, the short-circuit test time point t_M exceeds both t_A and t_B. Due to the t_{delay} required for gate failure to occur, thermal runaway will directly occur in this case. Subsequently, the solid-state breaker quickly intervened to shut off the circuit. After a delay time of 2.1 μs, a current path was formed between the gate and source, resulting in an obvious gate failure.

Fig. 13(d) shows a rare short-circuit failure waveform. After the 6.8 μs gate pulse was turned off, the DUT first experienced gate failure, followed by thermal runaway. This case is similar to Fig. 13(b), except t_{BF} is larger than t_{AF}. Therefore, after the DUT is turned off, gate failure first occurs, and then due to the heating of the trailing current, the DUT temperature reaches T_B, leading to thermal runaway. It is worth noting that the occurrence of this failure waveform is related to both the heating rate and the test time point, which is accidental.

This model combines the differences in heating rate under multiple short-circuit conditions, the distribution of short-circuit temperature inside the cell, and the test time points to reveal the switching mechanism of two short-circuit failure modes for SiC MOSFETs. This short-circuit failure mode switching model is applicable to both Linear and Hexagon. The simplified model effectively explains the occurrence principles of various short-circuit waveforms under different failure modes, as shown in Fig. 13, further confirming the correctness of this model.

V. Comparison of Robustness for Equal Power Short-Circuit

As shown in Section II, under the same gate and bus voltage, Linear always exhibits better short-circuit robustness than hexagon due to its lower short-circuit power density. It is difficult to evaluate whether cell topology has other potential effects on the short-circuit robustness of SiC MOSFETs besides short-circuit power. It is necessary to design equal power short-circuit tests to eliminate the interference of short-circuit power differences and further explore the influence mechanism of cell topology on the short-circuit robustness of SiC MOSFETs.

How to achieve equal power short-circuit tests for Linear and Hexagon? The condition of ensuring the same chip size and manufacturing process can be achieved by adjusting key ion implantation parameters or changing the cell pitch of Linear and Hexagon. However, both methods require high process and layout adjustment costs to explore suitable parameters, resulting in poor flexibility. Adjusting the short-circuit gate and bus voltages can significantly change the short-circuit power, which does not require additional manufacturing costs and has higher adjustment flexibility. As shown in Fig. 5, by adjusting V_{gs}, similar I_{peek} of Linear and Hexagon can be achieved. However, experimental results indicate that even if I_{peek} is adjusted to be similar, the subsequent short-circuit current of Hexagon is still higher than that of Linear. Through experimental verification, directly adjusting the short-circuit bus voltage V_{ds} is a good test method, which can ensure excellent short-circuit power matching throughout the entire duration of the short-circuit pulse.

For gate failure mode, three sets of equal power short-circuit comparison tests were conducted between Linear and Hexagon under different gate and bus voltages, namely set_1, set_2, and set_3. Combine cell topology with a set number to distinguish different DUTs, for example, using Lin1 and Hex1 to represent the comparative DUTs in set_1. Fig. 14 shows the waveforms of equal power short-circuit tests for each set and summarizes the relevant short-circuit parameters in the table.

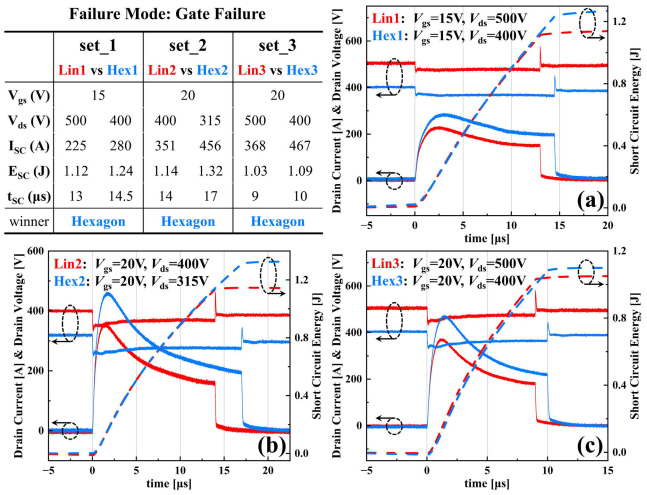

Fig. 14. Comparison of waveforms for equal power short-circuit test under gate failure mode: (a) set_1, (b) set_2, and (c) set_3.

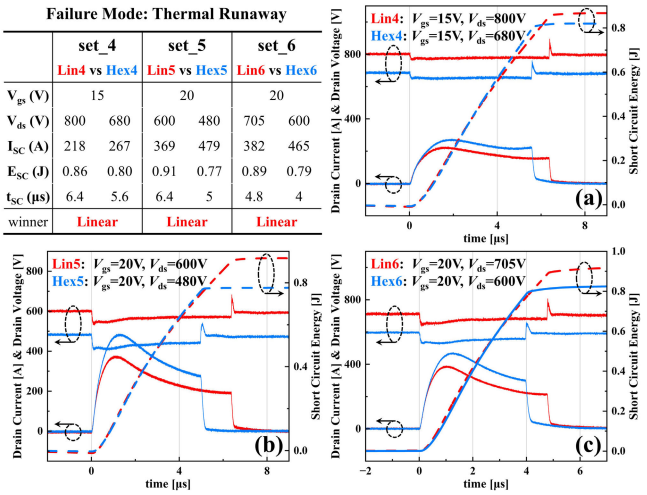

Fig. 15. Comparison of waveforms for equal power short-circuit test under thermal runaway mode: (a) set_4, (b) set_5, and (c) set_6.

The corresponding short-circuit waveforms are all taken from the latest tests before the occurrence of gate failure. Taking set_1 as an example, Fig. 14(a) shows the short-circuit waveforms and energy curves of Lin1 under V_{gs} = 15 V, V_{ds} = 500 V and Hex1 under V_{gs} = 15 V, V_{ds} = 400 V, respectively. Lin1 reaches the gate failure short-circuit limit at 13 μs, while Hex1 persists to 14.5 μs. Before 13 μs, the short-circuit energy curves of Lin1 and Hex1 were highly overlapping, indicating that the short-circuit power during this process is similar. Subsequently, Hex1 was still able to withstand 1.5 μs and the short-circuit energy continued to rise, while Lin1 had reached its limit, indicating that Hex1 has higher short-circuit robustness under this equal power short-circuit condition. Similarly, for gate failure mode, the equal power short-circuit test results of set_2 and set_3 under different gate and bus voltages also show that Hexagon has better short-circuit robustness than Linear.

For thermal runaway mode, three sets of equal power short-circuit comparison tests were conducted between Linear and Hexagon under different gate and bus voltages, namely set_4, set_5, and set_6. Fig. 15 shows the waveforms of equal power short-circuit tests for each set, and summarizes the relevant short-circuit parameters in the table. Unlike the case of gate failure, for equal power short-circuit tests of thermal runaway, the results of all three sets indicate that Linear has higher short-circuit robustness than Hexagon. In summary, for the equal power short-circuit test, Hexagon has better short-circuit robustness in gate failure mode, while Linear performs better in thermal runaway mode.

First, the difference in the equal power short-circuit robustness between Linear and Hexagon for thermal runaway mode is briefly analyzed. Thermal runaway is mainly caused by the positive feedback between BJT conduction and short-circuit high temperatures. In these equal power short-circuit tests, the theoretical heating rates of Linear and Hexagon are similar, and the difference in cell temperature distribution is relatively small. However, during the short-circuit process, Hexagon has a higher short-circuit current than Linear. And after the gate voltage is turned off, the BJT hole tail current of Hexagon is also higher than that of Linear. Therefore, the temperature required for thermal runaway positive feedback to occur in Hexagon is lower than Linear, resulting in a lower thermal runaway SCWT for Hexagon.

Then, the mechanism of the equal power short-circuit robustness difference for Linear and Hexagon in gate failure mode was investigated in detail. Due to the 3-D structural differences in cell topology, 2D-TCAD simulation cannot be directly used to accurately reflect the temperature and thermal stress of Linear and Hexagon under short-circuit conditions. Combining macroscopic test data of equal power short-circuit with 3-D temperature and thermal stress simulations at the cell level can more intuitively demonstrate the performance difference between Linear and Hexagon during the short-circuit process for gate failure mode. Based on the ANSYS Workbench platform, the thermal and mechanical stress coupling performance of 3-D cell topology structures under equal power short-circuit conditions has been extensively studied. The 3-D cell models corresponding to Linear and Hexagon are shown in Figs. 16(a) and 17(a), respectively, and their structure dimensions are the same as the actual cell topology. Considering the limited heat transfer distance in microsecond level short-circuit process simulation, the thickness of epoxy molding compound (EMC) in the 3-D simulation model is set to 10 μm. The material characteristic parameters for 3-D cell temperature and thermal stress simulation of SiC MOSFET are shown in Table III.

Taking the short-circuit waveform of set_2 as a reference for 3-D temperature and thermal stress simulation, according to Fig. 14(b), the total short-circuit heating power during the 14 μs short-circuit process is calculated to be P_{total} = 82 kW. It is worth noting that due to the slight difference in S_{ACT}, the actual short-circuit power density of Linear and Hexagon is not equal. The active region short-circuit power densities of Linear and Hexagon are as follows:

$$P_{\text{Density.Lin}} = \frac{P_{\text{total}}}{S_{\text{ACT.Lin}}} = 0.00843\ \text{W}/\mu\text{m}^2 \tag{2}$$

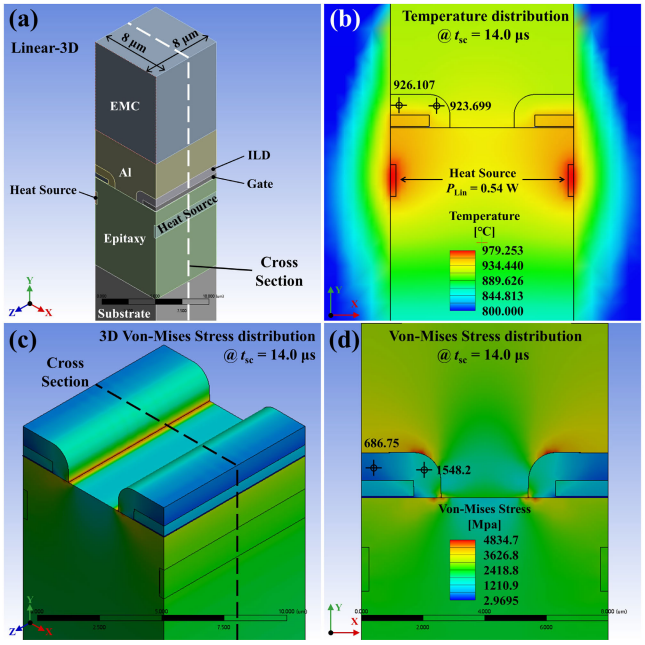

Fig. 16. Temperature and thermal stress simulation results of short-circuit gate failure under V_{gs} = 20 V, V_{ds} = 400 V, t_{sc} = 14 μs for Linear. (a) Three-dimensional simulation structure. (b) Temperature distribution within the cell cross section. (c) Three-dimensional Von-Mises stress distribution. (d) Von-Mises stress distribution within the cell cross section.

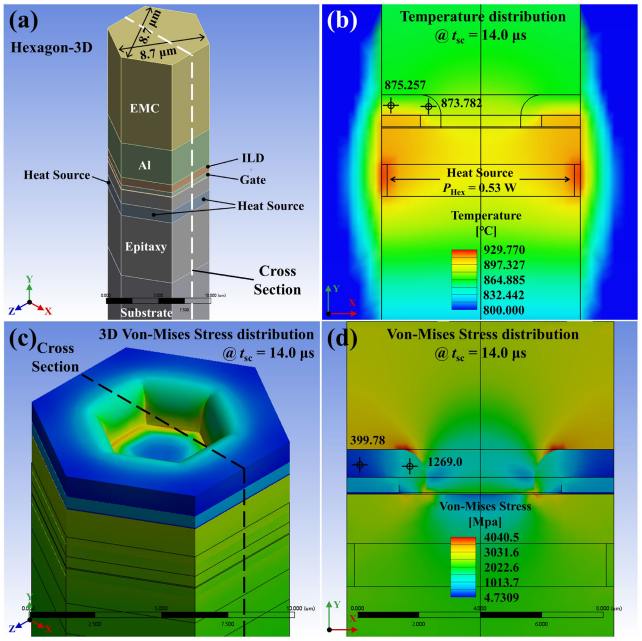

Fig. 17. Temperature and thermal stress simulation results of short-circuit gate failure under V_{gs} = 20 V, V_{ds} = 315 V, t_{sc} = 14 μs for Hexagon. (a) Three-dimensional simulation structure. (b) Temperature distribution within the cell cross section. (c) Three-dimensional Von-Mises stress distribution. (d) Von-Mises stress distribution within the cell cross section.

$$P_{\text{Density.Hex}} = \frac{P_{\text{total}}}{S_{\text{ACT.Hex}}} = 0.00802\ \text{W}/\mu\text{m}^2. \tag{3}$$

Figs. 16(a) and 17(a) show the 3-D simulation structures of Linear and Hexagon, respectively, with corresponding cell top areas of S_{Lin} = 64 μm^2 and S_{Hex} = 65.55 μm^2. The power of Linear and Hexagon 3-D simulation cell structures are as

TABLE III

MATERIAL CHARACTERISTIC PARAMETERS FOR 3-D CELL TEMPERATURE AND THERMAL STRESS SIMULATION OF SiC MOSFET

Material	Thermal Conductivity [W/(m·K)]	CTE [×10^{-6}/K]	Young's Modulus [GPa]	Poisson's Ratio
SiC	490	4.3	500	0.157
Polysilicon	34	2.6	169	0.22
SiO_2	1.4	0.5	75	0.17
Al	240	24	88.5	0.36
EMC	0.96	8 @ < 185 °C 30 @ > 185 °C	24.6	0.136

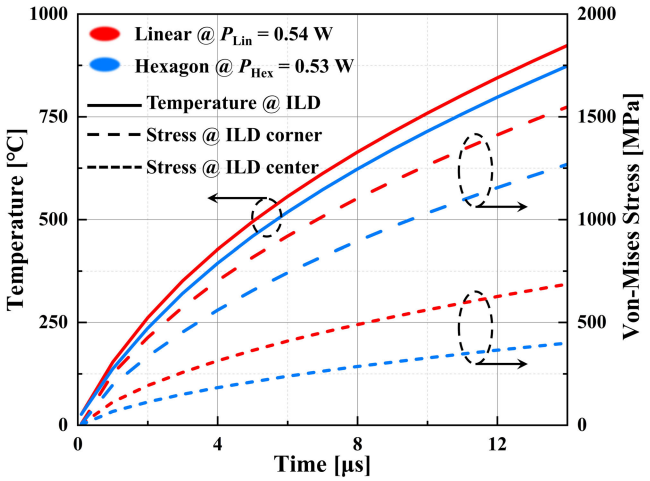

Fig. 18. Simulation curves of short-circuit temperature and stress at key points in the ILD layer for Linear and Hexagon of set_2.

follows:

$$P_{\text{Lin}} = P_{\text{Density.Lin}} \times S_{\text{Lin}} = 0.54\ \text{W} \tag{4}$$

$$P_{\text{Hex}} = P_{\text{Density.Hex}} \times S_{\text{Hex}} = 0.53\ \text{W}. \tag{5}$$

Under the above short-circuit power, transient thermal simulations on Linear and Hexagon were conducted using ANSYS Icepak to obtain detailed temperature distribution data in the 3-D cell topology structures. According to the temperature distribution inside the TCAD simulation cell shown in Fig. 11, it can be seen that the short-circuit heating core is located below the JFET region. To simplify the short-circuit heating process, the equivalent short-circuit heat source is set below the JFET region in the 3-D model, as shown in Figs. 16(a) and (b) and 17(a) and (b), with corresponding heating powers of P_{Lin} = 0.54 W and P_{Hex} = 0.53 W, respectively.

Figs. 16(b) and 17(b) show the temperature distribution of the cell cross section in the thermal simulations for Linear and Hexagon at t_{sc} = 14 μs, respectively. The temperature variation curves of Linear and Hexagon ILD layers are extracted, as shown in Fig. 18. It can be seen that the temperature distribution of Linear and Hexagon in the ILD layer is relatively uniform. At t_{sc} = 14 μs, the ILD temperature of Hexagon is approximately 50 °C lower than that of Linear.

It is also necessary to consider the distribution of 3-D cell thermal stress during the short-circuit process. The thermal

distribution data were imported into the ANSYS Mechanical APDL solver for further transient structural simulation to obtain stress distributions of 3-D cell topology structures. In terms of boundary constraint conditions, referring to the actual composition of active region cells, the bottom and all sides are set to frictionless constraints [24]. In addition, considering the melting of the Al layer under short-circuit high temperature, the top is set to be free. The 3-D Von-Mises stress distributions for Linear and Hexagon at $t_{sc} = 14\ \mu s$ are shown in Figs. 16(c) and 17(c), respectively, from which uniform and symmetric stress distributions can be observed. The corresponding Von-Mises stress distributions at the cell cross section are shown in Figs. 16(d) and 17(d), respectively. Referring to the failure points in Figs. 9 and 10, focus on the stress at the center and corner of the ILD. The extracted corresponding stress variation curves for Linear and Hexagon are shown in Fig. 18. It can be seen that during the entire short-circuit process, Linear has higher stress at both the ILD corner and ILD center. The simulated stress difference between the Linear and Hexagon ILD layers is about 280 MPa at $t_{sc} = 14\ \mu s$.

The above 3-D simulation reproduced the short-circuit heating situation of set_2 as much as possible, but there is still a small difference in short-circuit power density between Linear and Hexagon. For this purpose, the temperature and thermal stress distribution simulation studies of Linear and Hexagon were also conducted under the same short-circuit power density. When considering $P_{\text{Density.Hex}} = P_{\text{Density.Lin}} = 0.00843\ \text{W}/\mu\text{m}^2$, the power of Hexagon 3-D simulation cell structure is as follows:

$$P_{\text{Hex}} = P_{\text{Density.Hex}} \times S_{\text{Hex}} = 0.55\ \text{W}. \tag{6}$$

The same 3-D cell simulation was performed on Hexagon under the heat source power of $P_{\text{Hex}} = 0.55$ W, and the extracted ILD layer temperature and thermal stress variation curves are shown in Fig. 19. The specific ILD temperature and stress values at $t_{sc} = 14\ \mu s$ are also indicated in the figure. Although the temperature difference between the ILD layers of Linear and Hexagon is very small under the same short-circuit power density, there are still significant differences in thermal stress. The simulated stress of the ILD layer for Linear is about 200 MPa higher than for Hexagon at $t_{sc} = 14\ \mu s$. This fully demonstrates that the cell topology difference has a significant impact on the short-circuit thermal stress of the ILD layer in SiC MOSFETs. On the one hand, the polysilicon gates and ILD layers between adjacent cells of Hexagon are connected to each other through a hexagonal mesh structure. Compared with the separated array layout of Linear, this hexagonal layout may be able to relieve the thermal stress concentration in the ILD layer caused by short-circuit thermal expansion. On the other hand, due to differences in cell topology, Hexagon has a lower proportion of source metal contact holes compared to Linear, which may help reduce the ILD layer stress caused by source metal short-circuit thermal expansion.

The thermal stress simulation results in Figs. 18 and 19 are highly consistent with the actual results of equal power short-circuit tests under gate failure mode. In summary, due to the difference in cell topology, Hexagon always has lower ILD layer thermal stress than Linear during equal power short-circuit tests, resulting in higher SCWT for gate failure.

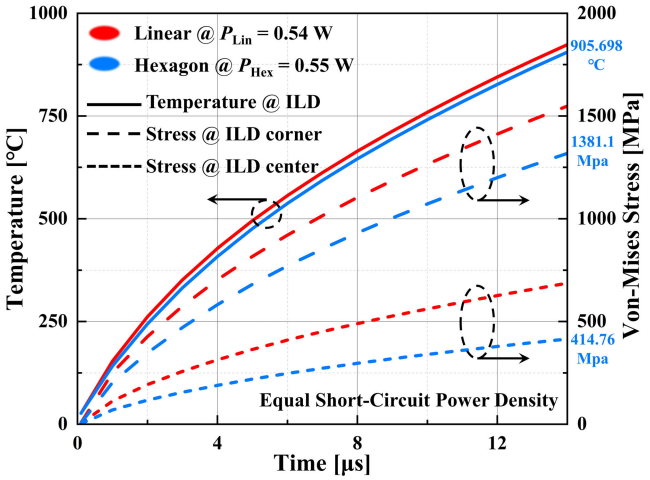

Fig. 19. Simulation curves of short-circuit temperature and stress at key points in the ILD layer for Linear and Hexagon under equal short-circuit power density.

VI. Conclusion

This article investigates the single pulse short-circuit robustness and failure modes of SiC MOSFETs with different cell topologies in detail. Based on self-developed SiC MOSFETs with linear and hexagonal topologies, the SCWT, ultimate short-circuit energy, and short-circuit failure modes were tested and evaluated under different gate voltages, bus voltages, and case temperatures. Under the same short-circuit conditions, Linear always has higher short-circuit robustness than Hexagon.

Through failure analysis, significant cracks were observed in the ILD layer of both Linear and Hexagon, and Al infiltration was detected. The gate failure mechanisms for both Linear and Hexagon are caused by short-circuit thermal stresses that lead to cracks in the ILD layer, where molten Al infiltrates into the cracks and forms a short-circuit path. This fills the gap in the research on the short-circuit gate failure mechanism of SiC MOSFETs with hexagonal topology.

A new switching model of short-circuiting two failure modes for SiC MOSFETs was proposed by combining the simulation and test results. Due to the delay time of gate failure mode, gate failure occurs at a low short-circuit heating rate, while thermal runaway occurs at a high short-circuit heating rate. Based on the simplified model and test time points, several typical short-circuit test waveforms have been well explained. This model reveals the unique short-circuit mode switching mechanism of SiC MOSFETs, which can provide an analytical reference for almost all short-circuit failure situations.

The short-circuit robustness of Linear and Hexagon was compared and evaluated under the same short-circuit power for the first time. The results showed that Hexagon has better short-circuit robustness in gate failure mode, while Linear performs better in thermal runaway mode. The simulation

comparison of 3-D cell temperature and thermal stress reveals that Hexagon has a lower ILD layer stress than Linear. This further reveals the comprehensive impact mechanism of cell topology on short-circuit robustness.

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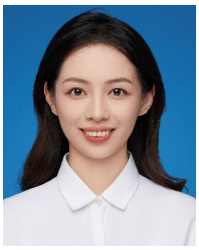

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