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An Aging-Robust 32-MHz RC Frequency Reference With 0.4-ppm Allan Deviation and ±1550-ppm Inaccuracy From –40 °C to 125 °C After a 1-Point Trim

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***Abstract*—This letter presents an aging-robust 32-MHz RC frequency reference based on a frequency-locked-loop (FLL). With a temperature compensation scheme that combines BJTs and aging-robust diffusion resistors, the FLL achieves ±1550-ppm inaccuracy from –40 °C to 125 °C after batch calibration and a low-cost 1-point trim, which increases to ±2350-ppm after accelerated aging. Due to the extensive use of dynamic error-correction techniques, the FLL also achieves a state-of-the-art Allan deviation floor of 0.4 ppm.**

***Index Terms*—Aging robust, frequency-locked-loop (FLL), RC frequency reference.**

I. Introduction

RC-based frequency references [1], [2], [3], [4], [5], [6] are commonly used as clock generation circuits in SoCs. Compared to LC oscillators, they are low power, compact, and can achieve medium frequency accuracy. With low-temperature-coefficient (low-TC) poly resistors and digital calibration, some designs can achieve inaccuracies of a few 100 ppm [1], [2], but the aging-induced drift can be as large as 5000 ppm [5], [6]. Designs based on via-metal [4] or silicided [7] resistors exhibit significantly better aging robustness, in the order of several 100 ppm. However, such resistors have larger TCs (∼3000 ppm/ °C), which then require a time-consuming 2-point trim to achieve inaccuracies of a few 100 ppm. In [6], a compact design (∼0.03 mm^2) is proposed that uses aging-robust diffusion resistors with a smaller (∼1500 ppm/ °C) TC. However, its temperature compensation relies on trimmed PTAT/CTAT current sources, whose mismatch still requires a 2-point trim.

This letter, an extension of [8], describes a compact, aging-robust, and easy-to-calibrate 32-MHz RC frequency reference. Its temperature compensation scheme relies on four unit current sources, whose mismatch can be mitigated by dynamic element matching (DEM). As a result, the proposed frequency reference achieves ±1550-ppm inaccuracy from –40 °C to 125 °C after a low-cost 1-point trim, which increases to ±2350 ppm after accelerated aging. It also achieves an Allan deviation floor of 0.4 ppm, corresponding to state-of-the-art stability.

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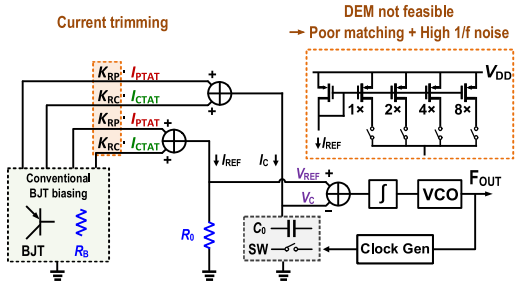


Fig. 1. Operating principle of the RC frequency reference in [6].

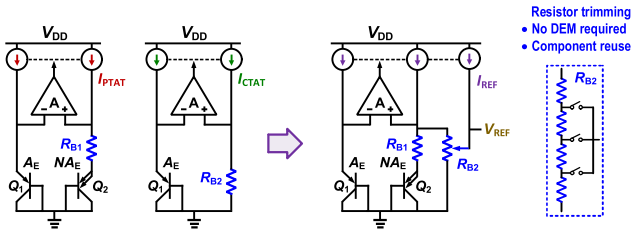


Fig. 2. Hybrid BJT biasing principle and its advantages.

II. Operation Principle

A. Previous Biasing Design and Its Limitations

Fig. 1 shows the operating principle of an RC frequency reference in [6]. It is built around a frequency-locked-loop (FLL), which locks the period of a VCO to the time an MIM capacitor (C_0) is charged to a reference voltage (V_{REF}) via a reference current (I_{REF}). Since the TC of C_0 is sufficiently small, the TC of the VCO's output frequency (F_{OUT}) can be minimized by forcing the same TC of V_{REF} as that of I_{REF}. In [6], this is achieved by a conventional BJT-based biasing circuit that generates PTAT ($I_{PTAT} = \Delta V_{BE}/R_B$) and CTAT ($I_{CTAT} = V_{BE}/R_B$) currents, as shown in Fig. 1. These currents are then scaled and combined to generate I_{REF} and V_{REF} (via a diffusion resistor R_0). In [6], the TCs of I_{REF} and V_{REF} are fine-tuned by trimming the scaling factors K_{RP}, K_{RC}, K_{CP}, and K_{CC} using binary-weighted current mirrors. However, the mismatch of the current mirrors leads to added TC error and necessitates 2-point trimming. Also, the residual 1/*f* noise of current mirror transistors results in a high Allan-deviation floor (18.8 ppm).

B. Hybrid BJT Biasing

The matching issue can be solved by using a set of unit current sources, whose mismatch can then be addressed by DEM. Fig. 2 shows how TC compensation for I_{REF} and V_{REF} is achieved under

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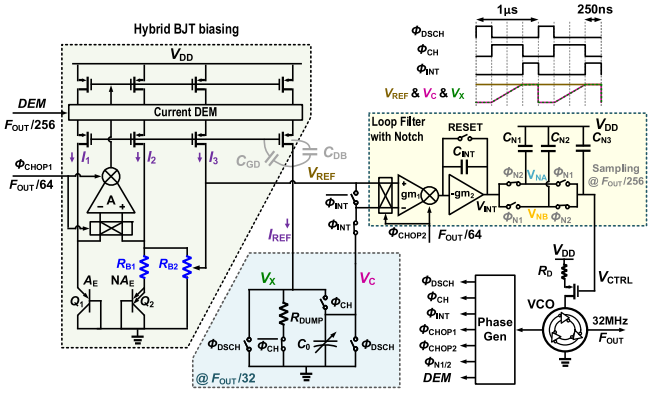


Fig. 3. System block diagram of the proposed frequency reference.

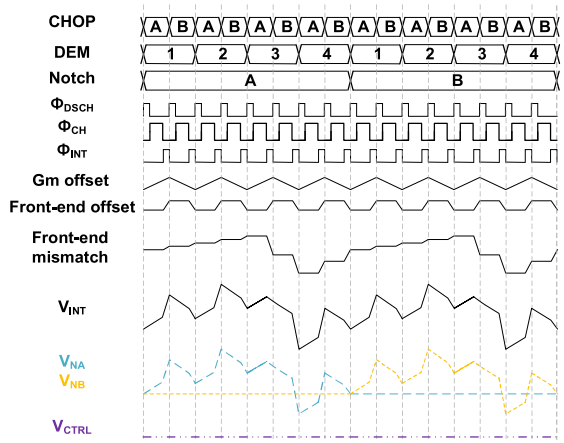


Fig. 4. FLL timing diagram showing control signals and the operation of the SC notch filter.

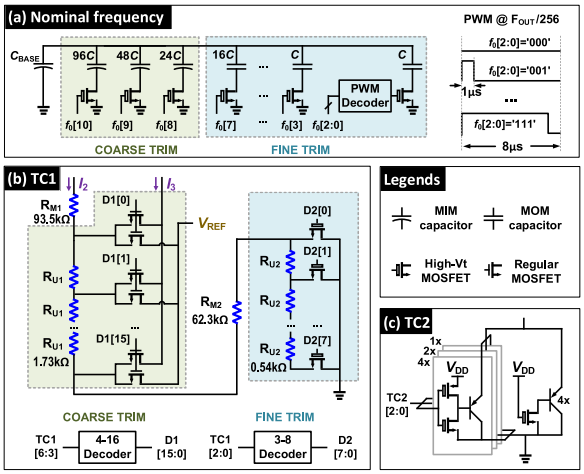


Fig. 5. Trimming circuits for (a) nominal frequency, (b) TC1, and (c) TC2.

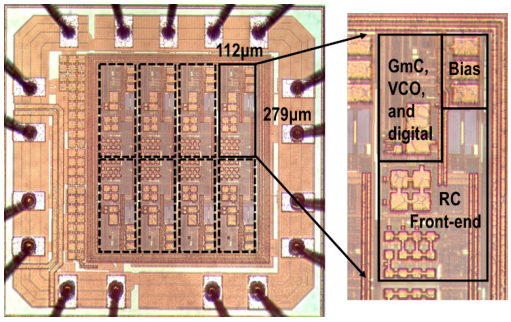


Fig. 6. Chip micrograph with eight identical FLLs and a zoomed-in view of one FLL.

this strategy. By properly combining the PTAT/CTAT current generation circuits and placing R_{B2} in parallel with the Q_2 branch, the TC of the biasing current will be a weighted average of the PTAT/CTAT TC characteristics [9], with the weighting factors determined by the resistor ratio.

To generate V_{REF} with a better TC tunability, a copy of I_{REF} is injected into a segmented version of R_{B2} using different tap ratios. This structure provides another degree of freedom that enables an adjustable second-order curvature compensation [6]. Compared to the biasing scheme in [6], this hybrid biasing reduces component count (saving one op-amp and one resistor), thereby improving stability. Furthermore, all the currents are now derived from a single unit current I_{REF}, and their mismatch and 1/*f* noise can be effectively mitigated by DEM [6].

III. Circuit Implementation

A. Frequency-Locked Loop and Its Timing

Fig. 3 illustrates the implementation of the proposed FLL, which has a 32-MHz output frequency, F_{OUT}. The hybrid biasing circuit employs two PNP transistors (Q_1, Q_2) with a fixed emitter area ratio N, and the biasing op-amp is implemented as a telescopic OTA (gain≈95 dB, gm≈20 μS), which forces V_{BE} across R_{B2} (185 kΩ) and ΔV_{BE} across R_{B1} (6 kΩ). The resulting reference current, I_{REF}, is mirrored by two additional pMOS sources to charge C_0 (5.3 pF) and generate V_{REF} (~0.7 V at room temperature). Following the approach in [6], the FLL operation is divided into three phases with a period of 1 μs (32/F_{OUT}). During the discharge phase Φ_{DSCH} (250 ns), C_0 is shorted to ground and thus resets V_C. In the next charging phase Φ_{CH} (500 ns), C_0 is charged by I_{REF} to generate V_C. At the end of this phase, the current source output, V_X, is connected to a resistive dummy load sized to ensure V_X~V_C, thereby minimizing the voltage transient at V_X. During the integration phase Φ_{INT} (250 ns), the error between V_C and V_{REF} is integrated by a two-stage Gm-C loop filter (gm_1=3.5 μS, gm_2=120 μS, and C_{INT}=3 pF). The first stage of the Gm-C consists of a telescopic OTA, while the second stage is a pMOS-input common-source amplifier. The Gm-C loop filter output is sent to a current-starved VCO controlled by a resistor-degenerated pMOS transistor. During the reset phase, the second stage of the Gm-C is diode-connected, establishing a voltage close to the VCO's steady-state control voltage, thereby reducing its settling time.

Fig. 4 details the FLL's timing diagram (1 μs/div) associated with dynamic matching techniques. To mitigate offset and 1/*f* noise, the biasing op-amp and the first stage of the Gm-C are chopped at F_{OUT}/64 (500 kHz). With a barrel shifter, the four current sources undergo DEM with a cycle frequency of F_{OUT}/256 (62.5 kHz). A switched-capacitor (SC) notch filter is implemented with C_{N1}=C_{N2}=C_{N3}=1.1 pF. As described in [10], the ping-pong operation reduces loop delay, enhancing stability and settling behavior. By setting the SC filter sampling rate to F_{OUT}/256 (the lowest DEM frequency), ripple generated by the effects of mismatch—the front-end biasing OTA offset, current source mismatch, and loop filter gm offset—are effectively suppressed, ensuring a stable frequency output.

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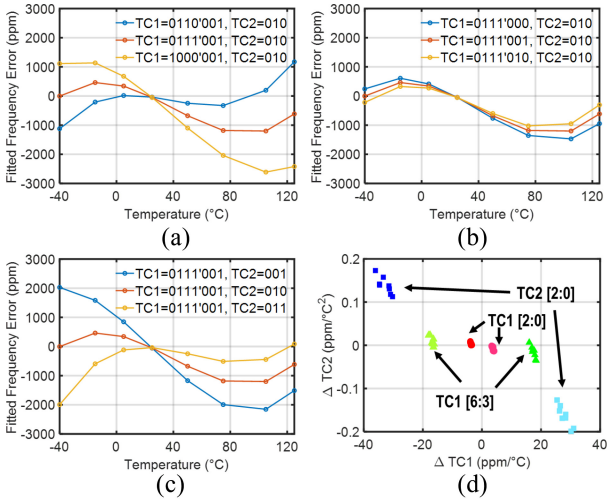


Fig. 7. Effect of ±1LSB changes in the (a) coarse TC1 code, (b) fine TC1 code, and (c) TC2 code (bottom-left). (d) ΔTC1 and ΔTC2 statistics from eight samples in one batch.

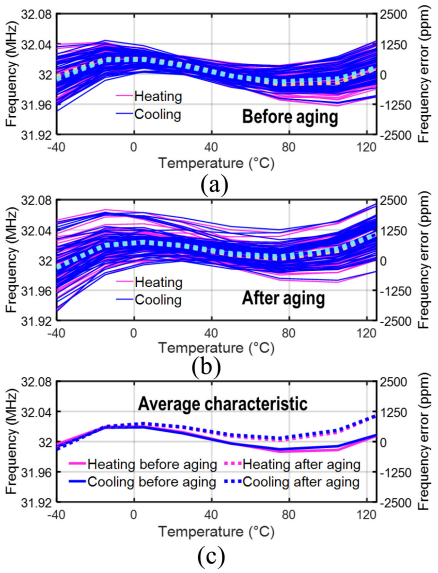


Fig. 8. Frequency error of Batch 1 samples: (a) after batch + 1-point calibration, (b) after 500 h of accelerated aging at 150 ° C with the same trimming codes, and (c) averaged results.

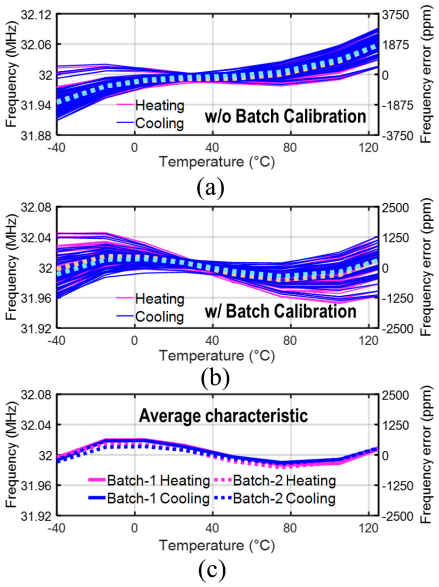


Fig. 9. Frequency error of Batch 2 samples. (a) 1-point trim + no batch calibration. (b) 1-point trim + batch calibration. (c) Averaged results compared to that of Batch 1 samples.

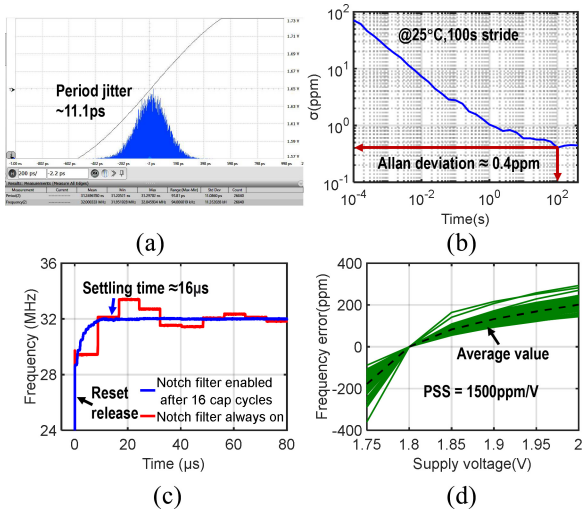


Fig. 10. (a) Measured jitter. (b) Allan deviation. (c) Start-up response. (d) Power supply sensitivity.

B. Trimming Circuits

To ensure an accurate and stable F_{OUT} despite process variations, both the nominal F_{OUT} and TC of the FLL should be trimmed. The trimming ranges were designed to cover the full range of process variations.

As shown in Fig. 5(a), the nominal F_{OUT} is adjusted by trimming C_0 via a CDAC, which consists of a coarse MIM and a fine MOM capacitor array to calibrate batch-to-batch/chip-to-chip variations of F_{OUT}, respectively. The former is implemented as a 3-bit DAC with 275fF LSB (∼5%), while the latter as a 5-bit thermomotor-coded DAC and a 3-bit pulse-width modulated (PWM) DAC operating at F_{OUT}/256, corresponding to an effective LSB of ∼1.45fF (∼250 ppm).

Fig. 5(b) illustrates the TC1 compensation circuit. A coarse 4-bit trim (∼18 ppm/ °C LSB) is realized by selecting the injection tap for I_{REF} on R_{B2}. With Kelvin connections, errors caused by voltage drops across the switches are eliminated. A fine 3-bit trim (∼3 ppm/ °C LSB) is achieved by shorting a portion of the lower segment of R_{B2}. By adjusting the effective emitter area and consequently V_{BE}, another degree of freedom is realized to perform TC2 trimming, as shown in Fig. 5(c). To minimize leakage current at high temperatures, switches in TC2 and fine TC1 trimming blocks are high-V_T devices.

IV. Measurement Results

The frequency reference was fabricated in a standard 0.18-μm CMOS process (Fig. 6). Each prototype chip contains eight identical frequency references, while each reference occupies 0.031 mm^2 and consumes 89 μA from a 1.8-V supply.

Samples from two typical-corner batches (56 from Batch 1 and 56 from Batch 2) were packaged in ceramic and characterized over the automotive temperature range (–40 °C to 125 °C). Fig. 7(a)–(c) illustrates the effect of tuning the trimming codes by ±1 LSB. Compared to the BJT ratio trimming that affects both TC1 and TC2, the resistive TC1 trimming primarily affects TC1 [Fig. 7(d)]. Consequently, both TC2 and TC1 tuning can be realized by combining the two mechanisms.

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TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART RC-BASED FREQUENCY REFERENCES

	JSSC 2022 [1]	ISSCC 2021 [2]	JSSC 2023 [3]	JSSC 2023 [4]	JSSC 2023 [5]	JSSC 2025 [6]	ESSCRC 2025 [7]	**This work**
Technology	180nm	180nm	65nm	65nm	180nm	180nm	180nm	**180nm**
Main resistor	P-Poly	P-Poly	N-Poly	P/N-Poly	P-Poly	N-Diff	SN-Poly	**N-Diff**
Compensation device	S-Poly	S-Poly	P+ Diff	VIA Res.	N-Poly	BJT	BJT	**BJT**
Area [mm^2]	0.3 [a]	0.14 [a]	0.15	0.22	0.01	0.028	0.22	**0.031**
Frequency [Hz]	16M	16M	400M	100M	10M	32M	16M	**32M**
Power [µW]	220	158.4	547	142	85.1	131	157	**160**
Energy [pJ/cycle]	13.8	9.9	1.4	1.4	8.51	4.1	9.8	**5**
Temp. range [°C]	-45~85	-40~85	-40~85	-40~85	-45~125	-45~125	-45~85	**-40~125**
Trimming points	2+batch	1+batch	2	2	1+batch	2+batch	2+batch	**1+batch**
Temp. coefficient [ppm/°C] [b]	1.3	5.2	6.8	12.3	31.5	10.6	4.9	**18.8**
Freq. error [ppm]	±90	±400	+450/-400	±770	±2800	±900	±350	**±1550**
Freq. error after aging [ppm]	-	-	-	±1030 [c]	-3200/-7300 [d]	+1600/-1400 [d]	±450	**±2350** [d]
Supply range [V]	1.6~2	1.6~2	0.9~1.1	1.1~1.3	1.5~1.8	1.7~2.0	1.6~2	**1.75~2.0**
Supply sensitivity [ppm/V]	1200	2000	1000	1400	9000	3000	1500	**1500**
Jitter [ps]	39.9	10.2	3.5	5.1	41.4	18.7	21	**11.1**
Allan Deviation Floor [ppm]	0.32	3	3	8.1	1	18.8	2	**0.4**
Number of samples	20	18	10	14	112	28	16	**112** [e]

[a] with high-order polynomial engine [b] box method [c] 500hours @125°C
[d] 168hours @150 °C [e] 2 batches, 56 samples per batch

After a batch calibration to determine the TC1/TC2 codes, an individual 1-point calibration is applied to adjust the nominal F_{OUT}. As shown in Fig. 8(a), samples from Batch 1 achieve a peak inaccuracy of ±1550 ppm.

After one week of un-powered accelerated aging at 150 °C [5], [6], the average frequency error increased to ±2350 ppm [Fig. 8(b)]. Applying the TC1/TC2 codes derived from Batch 1 to the Batch 2 samples results in an inaccuracy of ±2900 ppm, primarily due to shifts in TC1. After a batch calibration on TC1, their inaccuracy and the average characteristics become nearly identical to those of Batch 1 samples [Fig. 9], and the averaged curves. Fig. 10(a) shows the output period jitter. By employing DEM and chopping on all amplifiers and current sources, an Allan deviation floor of only ∼0.4 ppm can be achieved [Fig. 10(b)]. Fig. 10(c) demonstrates the start-up acceleration achieved by disabling the notch filter during the first 16 cycles, resulting in a 0.1% settling time of ∼16 μs (5× faster than [6]). Finally, Fig. 10(d) presents the supply sensitivity of the proposed frequency reference.

The performance of the proposed RC frequency reference is compared to the state-of-the-art in Table I. It achieves the best 1-point trimmed inaccuracy after accelerated aging, which is beneficial for cost-sensitive SoC applications. Also, its Allan deviation floor of 0.4 ppm is at par with the state-of-the-art [1].

V. CONCLUSION

This letter presents an aging-robust RC frequency reference based on an FLL. It uses a hybrid BJT biasing circuit to compensate for the temperature coefficients of diffusion resistors using one set of unit current sources. The FLL achieves ±1550-ppm inaccuracy from –40 °C to 125 °C after batch calibration and a 1-point trim, which increases to ±2350 ppm after accelerated aging. It also achieves a state-of-the-art Allan deviation floor of 0.4 ppm due to the extensive use of dynamic error-correction techniques.

REFERENCES

[1] Ç. Gürleyük, S. Pan, and K. A. A. Makinwa, "A 16 MHz CMOS RC frequency reference with ±90 ppm inaccuracy from –45 °C to 85 °C," *IEEE J. Solid-State Circuits*, vol. 57, no. 8, pp. 2429–2437, Aug. 2022, doi: 10.1109/JSSC.2022.3142662.

[2] H. Jiang, S. Pan, Ç. Gürleyük, and K. A. A. Makinwa, "31.3 A 0.14mm2 16MHz CMOS RC frequency reference with a 1-point trimmed inaccuracy of ±400ppm from –45 °C to 85 °C," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, 2021, pp. 436–438, doi: 10.1109/ISSCC42613.2021.9365795.

[3] Y. Li et al., "A 20-μs turn-on time, 24-kHz resolution, 1.5–100-MHz digitally programmable temperature-compensated clock generator," *IEEE J. Solid-State Circuits*, vol. 58, no. 3, pp. 785–795, Mar. 2023, doi: 10.1109/JSSC.2022.3227139.

[4] K.-S. Park et al., "A temperature- and aging-compensated RC oscillator with ±1030-ppm inaccuracy from 40 °C to 85 °C after accelerated aging for 500 h at 125 °C," *IEEE J. Solid-State Circuits*, vol. 58, no. 12, pp. 3459–3469, Dec. 2023, doi: 10.1109/JSSC.2023.3320709.

[5] S. Pan, X. An, Z. Yu, H. Jiang, and K. A. A. Makinwa, "A compact 10-MHz RC frequency reference with a versatile temperature compensation scheme," *IEEE J. Solid-State Circuits*, vol. 58, no. 12, pp. 3450–3458, Dec. 2023, doi: 10.1109/JSSC.2023.3322307.

[6] S. Pan, Y. Cheng, G. Wu, Z. Wang, K. A. A. Makinwa, and H. Wu, "A 0.028-mm2 32-MHz RC frequency reference with an inaccuracy of ±900 ppm from –40 °C to 125 °C and ±1600 ppm after accelerated aging," *IEEE J. Solid-State Circuits*, vol. 60, no. 9, pp. 3257–3267, Sep. 2025, doi: 10.1109/JSSC.2025.3530944.

[7] K. Mohamed, N. G. Toth, H. Jiang, Ç. Gürleyük, and K. A. A. Makinwa, "A 16 MHz RC frequency reference with ± 450 ppm inaccuracy from –45 °C to 85 ° C after accelerated aging," in *Proc. IEEE Eur. Solid-State Electron. Res. Conf. (ESSERC)*, 2025, pp. 81–84, doi: 10.1109/ESSERC66193.2025.11214134.

[8] S. Pan, J. Zeng, X. Liu, Y. Cheng, K. A. A. Makinwa, and H. Wu, " An aging-robust 32MHz RC frequency reference with 0.4ppm allan deviation and ±1550ppm from –40 °C to 125 °C inaccuracy after a 1-point trim," in *Proc. IEEE Asian Solid-State Circuits Conf. (ASSCC)*, 2025, pp. 1–3.

[9] H. Banba et al., "A CMOS bandgap reference circuit with sub-1-V operation," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 670–674, May 1999, doi: 10.1109/4.760378.

[10] P. Park, D. Ruffieux, and K. A. A. Makinwa, "A thermistor-based temperature sensor for a real-time clock with ± 2 ppm frequency stability," *IEEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1571–1580, Jul. 2015, doi: 10.1109/JSSC.2015.2417806.

[11] K. Allinger and M. Kuhi, "A closed-loop 12bit CMOS-integrated stress sensor system with 4bit adjustable sensitivity from 178 to 11 kPa/LSB at up to 22.5kS/s and 5bit dynamic range adjustment," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, 2023, pp. 1–3, doi: 10.1109/ISSCC42615.2023.10067788.

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