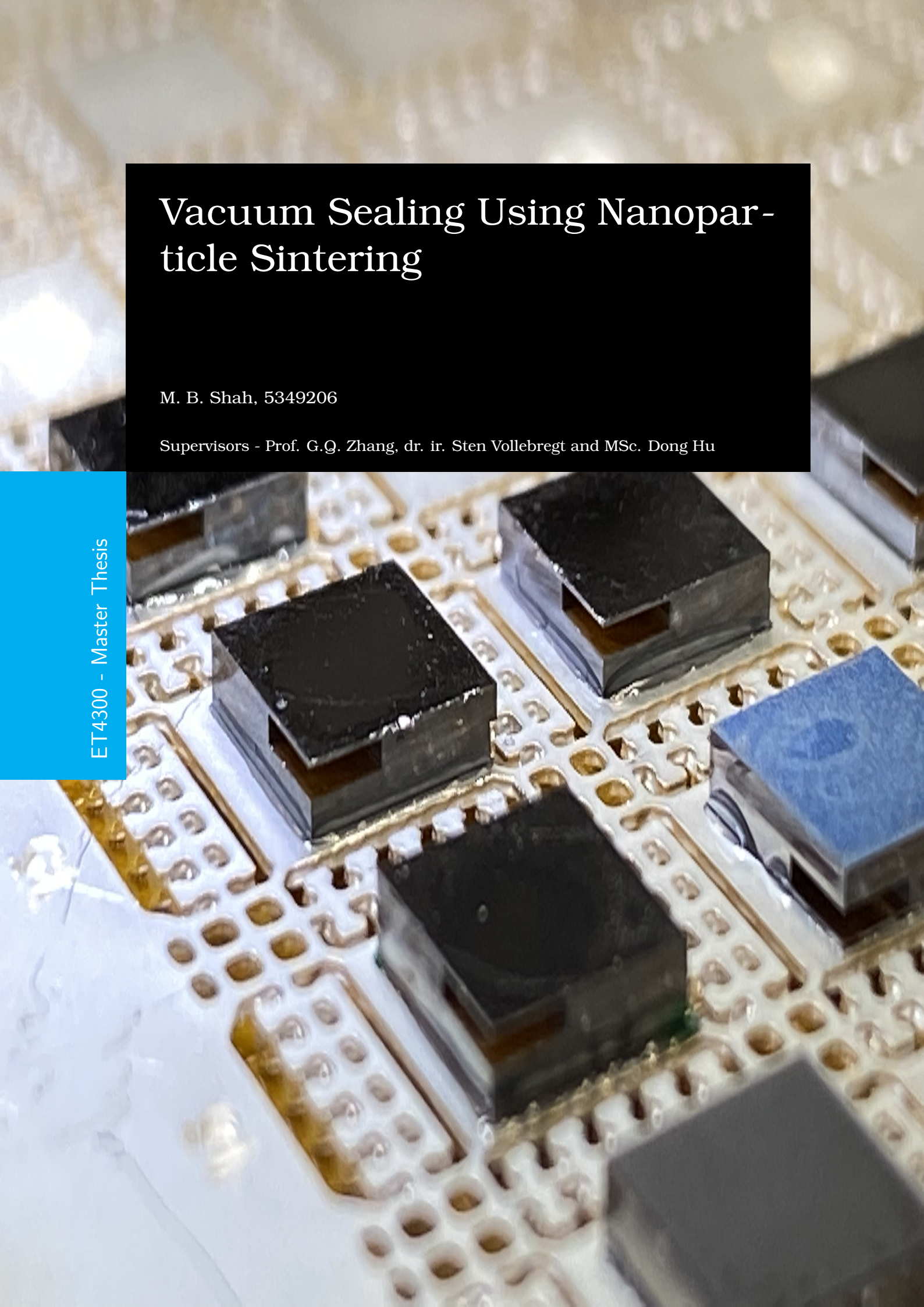
Vacuum Sealing Using Nanoparticle Sintering

M. B. Shah, 5349206

Supervisors - Prof. G.Q. Zhang, dr. ir. Sten Vollebregt and MSc. Dong Hu

ET4300 - Master Thesis



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November 30, 2022

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The undersigned hereby certify that they have read and recommend to the Faculty of Electronic Components, Technology and Materials (ECTM) for acceptance a thesis entitled

Vacuum Sealing Using Nanoparticle Sintering

by

M. B. Shah, 5349206

in partial fulfillment of the requirements for the degree of

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Abstract

Many semiconductor sensors, particularly MEMS sensors such as inertial, temperature, pressure, and resonance sensors need a vacuum environment for optimal performance and sensitivity in addition to the improvement in their long-term reliability. With the rise of heterogeneous integration with the MEMS and ICs being integrated together, process compatibility becomes a very big issue. Cu is a desirable bonding and sealing material for low-temperature vacuum packaging of next-generation microsystems, as it is compatible with modern CMOS circuits and 3-D IC fabrication. Cu thermocompression bonding has been reported to achieve vacuum sealing at low temperatures, but these approaches need extremely flat and clean Cu surfaces or additional capping layers, and the overall bonding areas are still rather large. To mitigate this, the use of copper nanoparticles as the sealing material has been proposed. In this study, the first successful demonstration of die and multi-die level hermetic sealing has been demonstrated using Copper nanoparticle paste as the sealing material for sealing ring widths as small as 8μ at a minimum temperature and pressure levels of 300°C and 10 MPa respectively with average encapsulated pressure of 54.18 mbar. Moreover, the leak rate evaluation was conducted which revealed no discernable leakage over a period of 48 days. Finally, the bond shear test and a subsequent failure analysis revealed high densification of the Copper nanoparticles at the bond interface.

Background and Motivation

1-1 Introduction

Moore's law has driven the primary stream of microelectronics innovation for the past 50 years, with two fundamental development arenas: IC reduction to the nanoscale and SoC-based system integration. The global microelectronics community continues to develop innovative approaches to maintain Moore's law. There is a growing awareness, R&D effort, and business motivation to push the development and application of "More than Moore" (MtM) technologies, which are based on or derived from silicon technologies but do not scale with Moore's law; examples include RF, Power, Sensor and actuator, SiP, heterogeneous integration, etc. Moore's law, which focuses mostly on digital operations, will be the focal point of future commercial prospects and technical improvements, which will emphasize innovation and successful integration. The "More than Moore" methodology prioritizes non-digital functions and heterogeneous integration. MtM refers to all technologies based on or built from silicon that do not simply scale with Moore's law. Figure 1-1 illustrates the critical significance of the More than Moore strategy for intelligent systems that require both computational and interface capabilities. [1] The shift from the internet of people to the internet of things

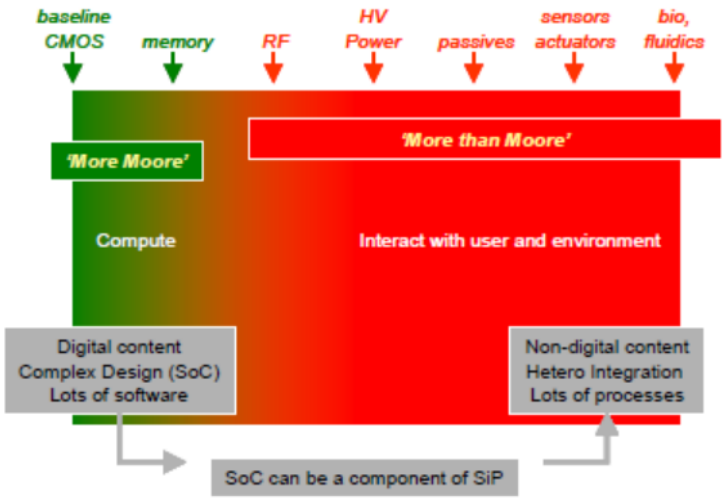


Figure 1-1: Intelligent Systems with More than More approach[1].

is key to the next wave of interconnectivity, with the More than Moore method at its core.

Despite the availability of a large number of discrete sensors, genuine IoT systems will not be feasible until miniaturized sensors are integrated with IC systems. The next generation of IC innovation will rely heavily on the lateral integration of extra system functions and the 3D heterogeneous integration of non-silicon devices with Si CMOS systems. [2] The use of 3D-Integration can result in a reduction in power consumption and an improvement in the chip's overall performance. The performance enhancement may be ascribed to the increase in integration density and the decrease in interconnect length as a consequence of the reduction in size and form factor of IC and MEMS devices, resulting in increased transmission speed and decreased power consumption.

In addition, for heterogeneous integration technology to reach its full potential, MEMS fabrication methods must continue decreasing the size, weight, power, and cost (SWaP-C) of MEMS components and systems. The similar tendency must be applied to MEMS packaging, which now accounts for up to 80% of the total cost and form factor [4]. To realize the full potential of heterogenous integration technology, it is necessary to adopt packaging approaches that result in low-cost, high-volume production. Many semiconductor sensors, notably microelectromechanical systems (MEMS), require a vacuum environment in order to achieve the appropriate sensitivity and performance. This category includes inertial sensors, thermal imagers, pressure sensors, and resonance devices. In addition, putting these MEMS sensors in a vacuum environment guarantees their reliability long-term [5]. On the path to low-cost, high-volume MEMS production, the vacuum packing of these MEMS sensors is a significant challenge. Typically, a vacuum environment is generated shortly after sensor fabrication to preserve the sensor during downstream assembly.

In order to minimize SWaP-C, vacuum packaging has shifted from serial, die-level techniques to massively parallel, wafer-level approaches, i.e. wafer-level vacuum packaging (WLVP). In a WLVP process, a semiconductor sensor die (device wafer) is bonded under vacuum to a passive lid wafer or another device wafer containing a portion of the sensor architecture. The principle

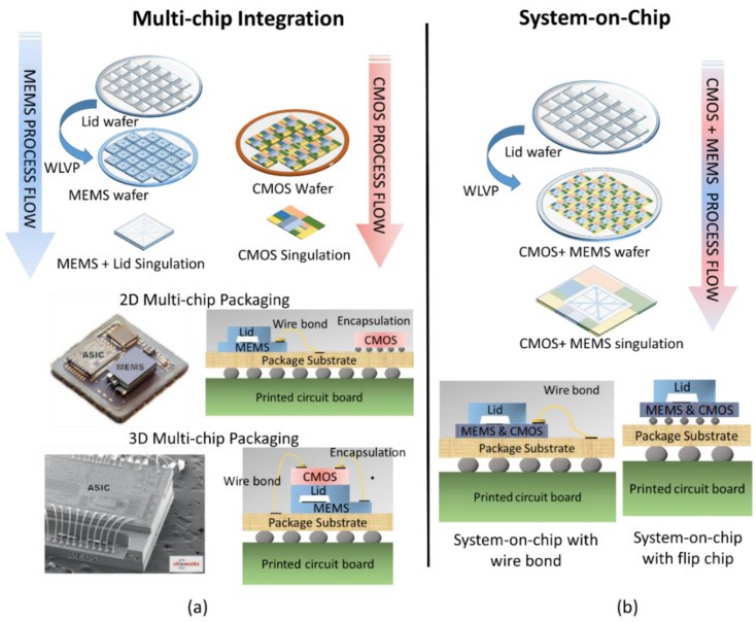


Figure 1-2: Multichip vs SoC approach [4].

behind a smart sensor is to integrate closely, sensor components with silicon integrated circuits (Si) (ICs). These readout ICs (ROICs) enable device bias, signal amplification, and other signal processing capabilities. WLVPs initially contained only discrete sensor devices, and smart sensors were accomplished by interconnecting discrete MEMS chips with ROIC chips via the package or board substrate. This technology, seen in Figure 1-2 (a), is known as multi-chip integration and is available in a variety of two-dimensional (2D) and three-dimensional (3D) configurations. Figure 1-2 (b) demonstrates the WLVP process flow for a system-on-chip architecture in which the complementary metal-oxide-semiconductor (CMOS) IC and sensor devices are integrated directly without needing routing layers in the package or board (SoC).

SoC is required for large-format pixelated devices such as micromirrors and image arrays. By integrating sensor arrays with CMOS ICs, it is possible to attain pixel-level connection density. Typically, SoC is more complex than discrete multi-chip packaging. Nonetheless, it has lower parasitics, smaller footprints, higher connection densities, and cheaper package costs than discrete multichip packaging. Several mature, high-volume microphones, pressure sensors, and inertial sensors are transitioning from multi-chip to SoC solutions in order to reduce SWaP-C [6].

1-2 Motivation and Problem Statement

When MEMS and CMOS ICs are merged on a single chip, the WLVP approach faces additional obstacles. The sensing element and the CMOS ICs must be thermally, chemically, and mechanically compatible for the WLVP method to work. To address these problems, several WLVP approaches have been developed. One of the approaches that may be employed for vacuum packaging of these integrated MEMS and CMOS devices is wafer bonding as a capping process. Various bonding techniques, such as Anodic Bonding, Glass Frit bonding, and Metal bonding, are described in the literature. Current WLVP approaches for packaging discrete MEMS devices, such as anodic, direct, or glass frit bonding, are incompatible with the temperature budget of the IC circuitry and/or require an excessive amount of valuable smart sensor space. As a result, device and process designers have been exploring alternate CMOS-compatible interconnect technologies for the WLVP of smart sensors. Typically, the relative maturity of a CMOS-compatible, metal-based WLVP solution corresponds to the relative maturity of the IC solution from which it emerged[4].

Mature metallic bonding techniques include solder bonding, eutectic bonding, solid liquid inter-diffusion bonding (SLID), surface activated bonding, and thermo-compression bonding. Nevertheless, each of these metallic bonding techniques has its own advantages and disadvantages and is ideally suited for applications that lie within the process parameters like temperature and pressure of the respective bonding strategy[7]. Solder bonding and eutectic bonding have disadvantages in that the melting of solder metals and alloys can cause reflow concerns, and sealing ring widths frequently exceed 100 μm to meet the required hermeticity and bond strength [8],[9],[10],[11]. Surface activated bonding permits sealing at room temperature [12],[13]; however, the surface planarity and surface roughness requirements for substrates are extremely stringent [12, 14]. SLID bonding can result in the formation of voids in the intermetallic compound layer; thus, special care must be taken in designing the sealing layer thickness and regulating the temperature ramping during bonding to achieve strong and

uniform bindings. [8], [21], [22]. Thermo-compression bonding utilises high temperatures of 300 – 450 °C [15]– [20], [26] and high bonding pressures, and has been demonstrated with metals like gold (Au) [15]– [17], aluminium (Al) [18], [19], and copper (Cu) [20], [26]. To prevent thermally-induced damage to MEMS devices and CMOS circuits, however, low bonding temperatures during vacuum packing are required.

Several low-temperature wafer-level sealing techniques using bonding layers such as Al [23], indium (In) [24], Au [27–32], and Cu [33, 34] have been developed to decrease the temperature threshold. Despite the fact that localised heating was utilised to seal Al-based MEMS cavities at room temperature, micro-heaters must be included into the package production [23], which considerably increases process complexity. In and Au were utilised to examine hermetic thermo-compression bonding at low temperatures. However, the reported sealing rings have extremely large widths ranging from 60μm to 200μm [24], [27], [32], and bonding layers with granular materials [28] or smoothed surfaces [32] need specialised processes to prepare. Due to Au's high ductility, vacuum sealing is possible by cold welding Au structures [29]–[31]. However, the recommended sealing procedures either rely on additional materials such as epoxy underfill [29] or solder patches [30] to strengthen the connection, or the procedure is based on wafer bonding combined with vent-hole sealing by plastic deformation of Au plugs [31].

Cu is increasingly used for metal interconnect layers in advanced CMOS circuits and electrical vias in advanced 3-D integrated circuit (IC) technologies [40] compared to the materials listed above. Cu is consequently a desirable bonding and sealing material for low-temperature vacuum packaging of next-generation microsystems, as it is compatible with modern CMOS circuits and 3-D IC fabrication. In addition, Cu's excellent mechanical strength may make it suitable for constructing extremely narrow sealing rings, resulting in compact package sizes.

Cu thermocompression bonding has been reported to achieve wafer-level vacuum sealing at low temperatures [33], [34], but these approaches need extremely flat and clean Cu surfaces [33] or additional capping layers [34], and the overall bonding areas are still rather large. Ultrasonic Cu bonding was utilized to seal MEMS cavities at room temperature in another investigation [39]. However, this approach has only been shown on a die level, and the bonding's mechanical and hermetic reliability has yet to be verified.
To overcome the aforementioned drawbacks, the use of nano Copper paste for wafer bonding has been proposed. This type of bonding can be performed at a CMOS Compatible low temperature enabled by low-temperature sintering due to the high surface-to-volume ratio of NPs, leading to a significant reduction of the bonding temperature [35]. Moreover, due to the usage of sub-micron nanoparticles, a surface-compliant bond can be formed, which compensates for the surface roughness of processed wafers which can degrade the hermetic properties of the bond [38]. The use of Cu NP for wafer-level bonding can be found in the literature at [36] and [37]. However, the hermeticity of these approaches has not been verified.

In this study, we aim to demonstrate hermeticity using Copper Nano-paste using Cu NP stencil printing technique as used in [37]. Thus, the research questions of this research work can be drafted as follows:

- **"Can Cu Nanoparticle-based be used reliably for vacuum sealing of MEMS cavities? "**
- "Can Cu Nanoparticle-based bonding approach be used for the Wafer Level Vacuum Packaging? "

1-3 Research Goals

The entire research work has been divided into separate research goals in order to achieve the problem statement. A dedicated chapter has been allotted to each research goal.

- Perform a literature review about the various works within the domain of wafer-level hermetic packaging.
- Build a valid device simulation model and decide on design parameters.
- Convert design parameters into mask designs, create a process flow, and manufacture the structure.
- Vacuum characterization of the device using cap deflection method and leak rate evaluation.
- Bond quality assessment of the structure using shear force test and imaging of the bond cross-section.

1-4 Organization of the Thesis Report

This work will investigate the usage of Copper Nanopaste for the sealing of MEMS cavities, The outlook of this thesis has been discussed as under.

- Chapter 2: Literature Overview: In this chapter, a background literature review about the various traditional and novel bonding approaches and the densification mechanism of nanoparticles.
- Chapter 3: Design and Methodology: In this chapter FEA simulations used for the finalization of the seal ring structure including the decision on the dimensions and choice of materials for the structure to be fabricated have been described. Moreover, hermeticity and bond quality assessment methods have also been discussed.
- Chapter 4: Mask design and the subsequent fabrication of the structures designed in chapter 3 with the discussion about the various processes done in the cleanroom.
- Chapter 5: Description of the bonding experiments and the results.
- Chapter 6: Conclusions and future work.

Literature Review

2-1 Introduction to WLVP

As illustrated in Figure 2-1, the manufacture of SoC smart sensors begins with the integration of CMOS and MEMS technologies, which can be done monolithically or heterogeneously. MEMS and CMOS devices are produced in a serial or parallel manner on the same substrate in the monolithic technique (Figure 2-1a). The device wafer is attached to a lid or cap wafer to create sealed packaging. The CMOS and MEMS devices are produced on different wafers in the heterogeneous approach (Figure 2-1b). The vacuum package can be manufactured by bonding the wafers together, or it can be created after the MEMS and CMOS are integrated [4].

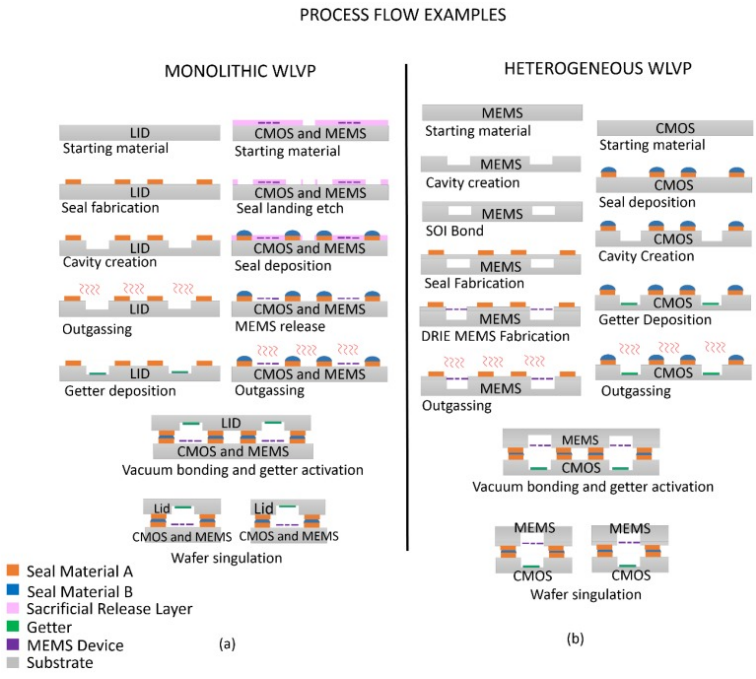


Figure 2-1: WLVP[4]

During the WLVP process, cavities are frequently created in one or both wafers; cavities provide an empty space in which the MEMS device can work. They also enhance the internal package volume, making it easier to achieve the desired ambient pressure. Metal-based seals

are often used in WLVP. The integration technique affects the generation order of seals and cavities. If the seal material is to be coated after cavity formation, the metal layer must be patterned using shadow masks, conformal resist deposition methods such as spray coating, or dry-film resist lamination. If traditional, less complex spin-coated resists can be used if the seal metal is applied prior to the formation of the cavity, then the seal metal must be compatible with the cavity etching procedure. Metal deposition processes will influence these integration options.

As shown in Figure 2-1, thin film getters are frequently inserted within the package to produce and maintain the required cavity pressure. These getters capture undesirable air and other gases emitted by activated electronic gadgets. Temperatures between 300°C and 400°C are necessary for getter activation [41]. Prior to deposition, wafers receiving getters should be degassed to prevent premature activation.

The final stage prior to bonding is the release of MEMS devices. For release, a sacrificial layer used in device fabrication is often etched dry or wet. If the getter is deposited on the wafer of the MEMS device, the release process must not impair the getter's functionality. The releasing procedure must also be compatible with the exposed seal materials. If at all possible, sealing surfaces that are sensitive to the release process should be included on a non-MEMS wafer. Once the seal metal has been deposited and patterned, the getter has been deposited, and the MEMS release has been performed, the wafers are ready for bonding. Wafers should be bonded in a vacuum bonder that can apply heat and mechanical force. The getter may be triggered before, during, or after bonding, depending on the bonding equipment and wafer temperature limits.

2-2 Bonding Technology

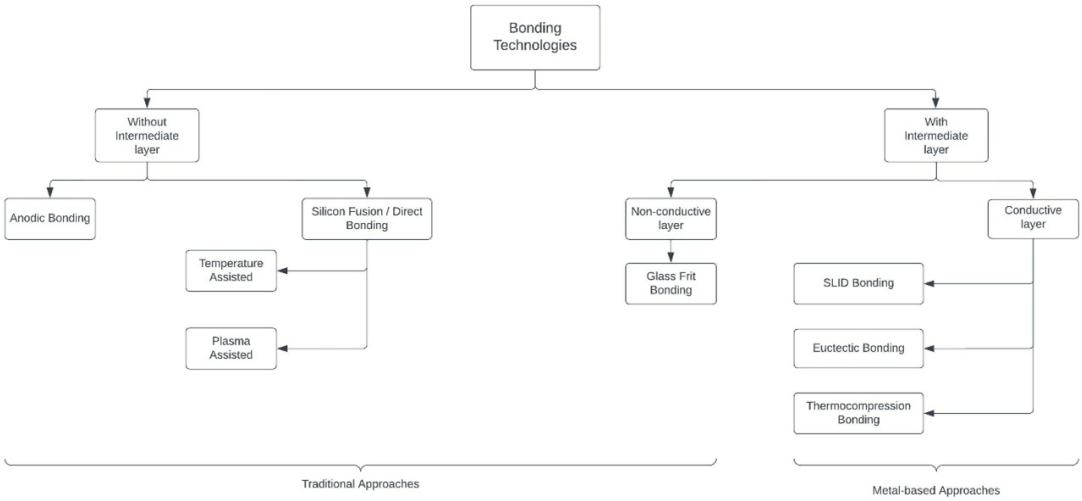


Figure 2-2: Bonding Technologies Classification

Bonding the cap wafer to the device wafer is a vital stage in the WLVP process. Wafer bonding techniques can be classified broadly into two categories based on the presence or

absence of an intermediate layer in the bonding technique as illustrated in figure 2-2. The intermediate layer may be conductive or non-conductive. Conductive seals may serve a dual purpose by acting as a sealant as well as providing electrical connections to the active devices within the sealed region [42].

2-2-1 Traditional Approaches

Traditional bonding methodologies involve the use of a non-conductive seal or directly bonding the two surfaces to be bonded without the use of an intermediate layer. Methods with no intermediate layers include approaches like Direct/ Silicon Fusion bonding and Anodic Bonding. These methods have been discussed in detail in the succeeding subsection.

Anodic Bonding

It involves the bonding of glass doped heavily with Sodium with Silicon under a high voltage (1000 V) at 400 °C. This leads to the formation of SiO_2 at the glass silicon interface, which forms a very strong bond with hermetic sealing. However, it has its drawbacks in

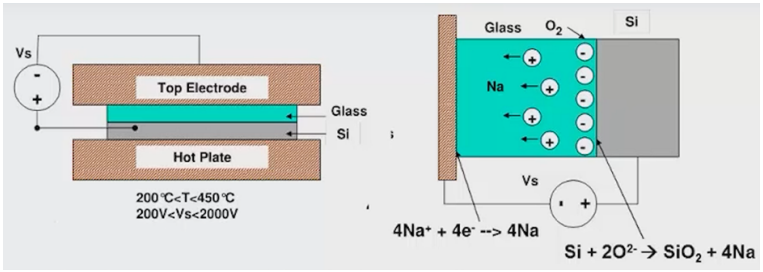


Figure 2-3: Anodic bonding [42]

the form of the high voltage involved, which can damage the devices fabricated on the wafer. Moreover, the presence of sodium dopant may degrade the functioning of the CMOS devices in addition to the outgassing of glass which leads to a degradation of the quality of the vacuum. The presence of a CTE mismatch between glass and Silicon and the surface smoothness requirements also add to the non-feasibility of this method for SoC-based applications.

Silicon Fusion/Direct Bonding

Silicon fusion bonding, on the other hand, eliminates the CTE mismatch problem in anodic bonding. It involves the formation of a Si-Si or a Si-O-Si bond at the interface of the two Si substrates depending on the surface activation method used. However, it requires very high temperatures (>1000°C), which is not conducive for CMOS, thus limiting its application range. The usage of plasma instead of heat can be used for surface activation, reducing the bonding temperature to 400 °C. However, the surfaces that need to be bonded must be extremely smooth, with roughness values below 0.3-0.5 nm, as direct bonding depends on weak Van der Waal's forces that disappear at distances of just a few nanometers (nm) [43-45], thereby making this bonding process unusable for surfaces with a high degree of varying topography.

Glass Frit Bonding

One of the most traditional ways of bonding with an intermediate layer is the glass frit bonding approach. This method is based on the usage of a low melting point lead silicate glass with added inorganic and organic fillers to alter the CTE and form a paste that can be later deposited on the surface to be bonded. This method involves screen printing of this paste in a definite pattern onto the substrate to be bonded, followed by heating up to 450 °C and compression of the surfaces to be bonded. The heating ensures that the organic fillers are evaporated, and the glass melts to wet the surface, followed by the cool down to form a strong bond.

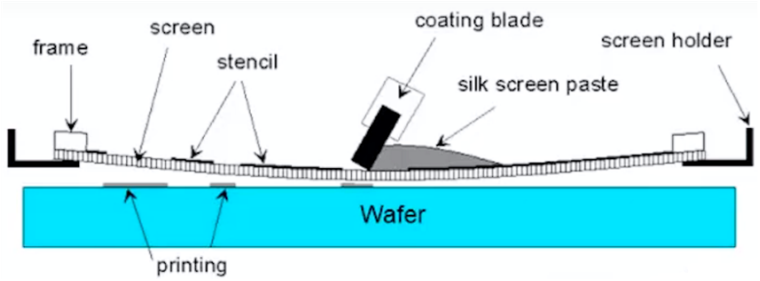


Figure 2-4: Glass Frit bonding using Screen Printing

This method does away with the drawbacks of high temperature, CTE mismatch, and low surface topography tolerance, as seen with the bonding approaches with no intermediate layers, all the while providing a hermetic seal which is suitable for WLVP applications. However, this method suffers from the drawbacks of outgassing, leading to the degradation in vacuum level and the presence of lead which is banned by some regulations. In addition, a large material squeeze-out occurs, which restricts the reduction of the width of the sealing ring below 75um, which translates to the sealing ring taking up valuable real estate area of the chip, reducing the number of dies per wafer and hence, the overall area of the chip[4]. Moreover, there is also the risk of glass material flowing into the movable structures of a MEMS device which poses severely detrimental consequences for the functioning of the device [4] [42].

2-2-2 Metal-based Bonding

Metal-based bonding techniques were developed to solve the deficiencies of conventional bonding techniques, which are primarily utilised for bonding discrete MEMS devices and are unsuitable for WLVP. The metal-based bonding techniques use IC- and MEMS-developed deposition and patterning techniques. Due to advanced manufacturing processes and the relatively low gas permeability of metals, hermetic sealing techniques may be achieved with as little as a few micrometres of the seal material. By reducing the amount of chip area required for bonding, these microscopic seals also reduce the cost of the component. Due to the fact that the seals are produced prior to being connected, the seal material may outgas, preventing any negative impact on the vacuum level. Because they can be utilised at temperatures acceptable for CMOS circuitry and may be paired with a range of substrate materials, metal-based bonding methods are perfect for packaging intelligent sensors. Metal-based techniques fall into three

basic categories: SLID, Eutectic, and Thermo-compression bonding. Each of these methods is explained in the sections that follow.

SLID Bonding

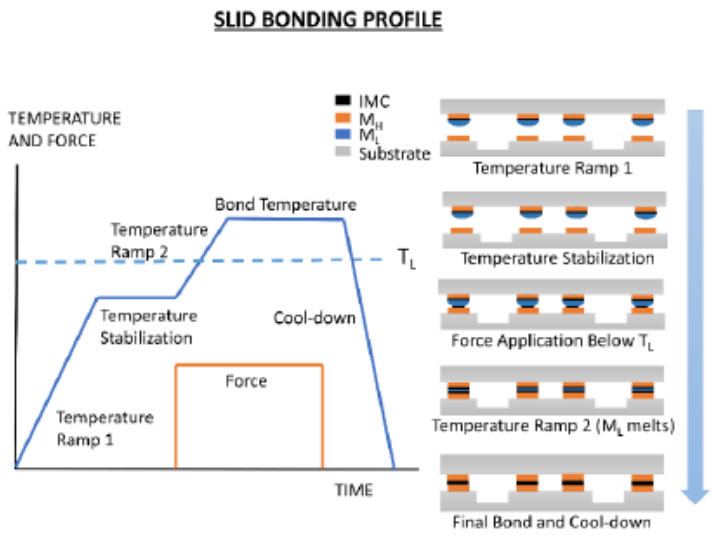
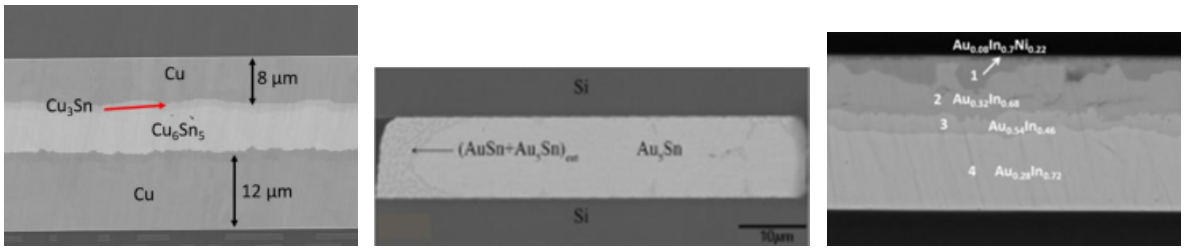


Figure 2-5: Typical SLID bonding process flow [47].

As shown in figure 2-5, SLID bonding—also known as transient liquid-phase (TLP), off-eutectic, and isothermal bonding—involves sandwiching a metal with a low melting temperature (ML) between a metal with a higher melting temperature (MH). These metals' melting points are indicated by the letters TH and TL, respectively. ML melts and wets to MH when the applied temperature surpasses the threshold limit. Although solid-state diffusion takes place below the melting point, the diffusion rates between ML and MH can rise by up to three orders of magnitude once ML melts [46]. Intermetallic compounds (IMCs) composed of MH and ML are created as a result of solid-liquid diffusion. The melting temperatures of these IMCs are significantly above TL. When bonding is complete, all of the ML should ideally be converted into IMCs, with layers of MH remaining on either side. The presence of excess MH prevents a reaction between the Under-seal metal (USM) layer and the seal. Excess MH absorbs mechanical stress and ensures that all of ML can be converted, creating a thermodynamically stable seal [47].



(a) SEM Image of Cu-Sn SLID Bonding.

(b) SEM Image of Au-Sn SLID Bonding.

(c) SEM Image of Au-In SLID Bonding.

Figure 2-6: SEM Imaging of SLID Bonding[4,62-63].

Pure elemental phase deposition, which is necessary for SLID bonding, is often significantly less difficult than alloy deposition, which is necessary for eutectic bonding [4]. Additionally, this method is particularly suited for smart sensors that need downstream elevated-temperature procedures like post-bond getter activation and/or assembly because of the IMC layers' high remelting temperature. Given that it enables the reuse of the same bonding temperatures and materials over and over again, it is also the perfect bonding technique for sensor production schemes that call for further wafer or chip stacking. The packaging of IC, MEMS, and smart sensing devices has been successfully demonstrated using three distinct SLID material sets, viz a viz, Copper – Tin (Cu-Sn) [48-54], Gold-Tin (Au-Sn) [55-59], and Gold-Indium (Au-In) [60,61].

This bonding technique is a promising technique for bonding MEMS cavities, Cu-Sn bonding can be achieved at a bonding temperature of greater than 230 °C with a yield strength of about 180MPa, while the AuSn SLID bonding has been demonstrated at temperatures around 280 °C having IMCs with high melting points and low stiffness can be ideal for high temperature automotive and space applications. However, Cu-Sn bonds form IMCs like Cu6Sn5, which tend to be scalloped (Figure 2-7) and can form voids due to the elemental consumption of Sn prior to the application of mechanical force. [51] This can be solved by providing excess Sn, but it leads to higher squeeze-out, thereby increasing the sealing ring width. In addition to these voids, void formation due to the Kirkendall effect is also a common occurrence in Cu-Sn IMCs [64,65]. Moreover, this bonding also has the drawback of having a high young's Modulus, thereby making them stiffer, leading to a higher CTE mismatch and thus reliability issues.

On the other hand, the high diffusivities of the Au-Sn couple and the wide range of potential IMC phases are the main obstacles to the Au-Sn SLID bonding [66]. The Au-In couple SLID bonding has been demonstrated at temperatures as low as 165 °C, making it attractive for temperature-sensitive devices. However, the native In oxide can be quite difficult to remove. Moreover, it also suffers from the same drawback as Au-Sn bonding with a multitude of IMCs formed [67], which lack elemental Au, which can cause a selection issue with the Under-seal metal (USM) as a wettable USM needs to be selected.

Eutectic Bonding

Wafer bonding methods based on eutectic metals are described by the term "eutectic bonding." These substances have the unique ability to transition from a solid to a liquid form at a certain

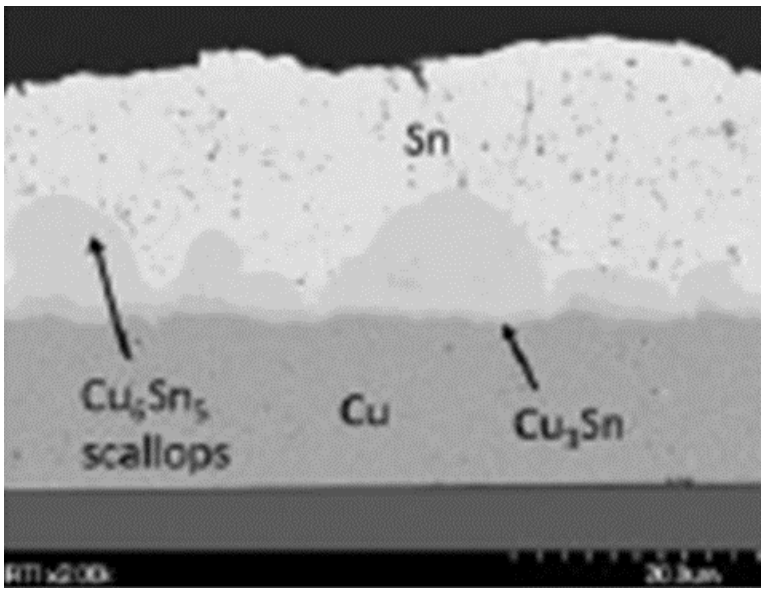


Figure 2-7: Scanning electron microscope (SEM) micrograph of a Cu-Sn layer [4].

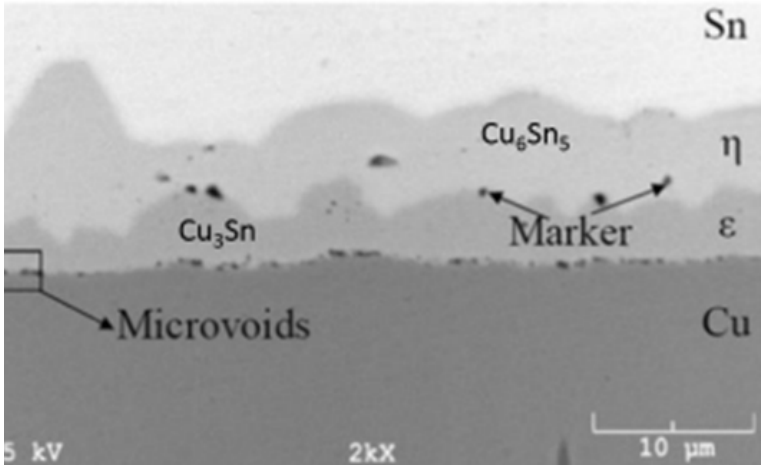


Figure 2-8: SEM image of Kirkendall void formation in Cu-Sn SLID bonding. [68]

temperature and composition without undergoing a two-phase equilibrium. The eutectic point of the alloy is defined by these precise temperature and composition characteristics. Once the eutectic melting temperature is surpassed during bonding, the alloy changes phases from solid to liquid. The intermediate bonding layer collapses after the liquid layer develops, accommodating surface roughness, particles, and other causes of non-uniformity between the two wafers. All surfaces that are wettable are coated by the liquid, which forms a continuous sealing layer that solidifies as it cools. The fundamental benefit of this method is that the melting point of one or both constituent metals in their pure condition is substantially lower than the eutectic temperature of the metal alloy, thereby allowing bonding at much lower temperatures.

A list of the most commonly used eutectic alloys and their pros and cons have been tabulated in Table 2-1. Alloys having eutectic temperatures at or below 400 °C are preferred for WLVP of smart sensors. Due to this, bonding temperatures—which are normally 20 °C - 50 °C above the eutectic temperature can be maintained for a few minutes below the CMOS thermal budget restrictions of 450 °C. It is also useful to outgas the wafers above the bonding temperature before bonding, which further restricts the bonding temperature for devices that need low package pressures to function.

Au0.8Sn0.2 eutectic bonding has been extensively studied for WLVP packaging due to a variety of intrinsic benefits, and it has been shown utilizing surrogate proxy wafers [69–74], RF MEMS switches [75,76], MEMS resonators [77], and infrared imaging smart sensors [78]. In this method, a wettable layer, usually Au, is placed on one of the wafers—the lid or the device wafer—and $Au_{0.8}$ $Sn_{0.2}$ is put on the other wafer. It is not necessary to clean the surface with flux or other chemicals that might not be suitable for released MEMS devices since $Au_{0.8}$ $Sn_{0.2}$ bonding layers do not oxidize. The $Au_{0.8}$ $Sn_{0.2}$ eutectic is a perfect choice for devices utilized in corrosive conditions (such as in medical applications) due to Au's inertness [79]. However, the steep liquidus lines, especially on the Au side of the target eutectic composition, are the biggest challenges to $Au_{0.8}$ $Sn_{0.2}$ eutectic bonding. The melting point is equal to 340 °C and 333 °C, respectively, with 81% and 75% Au by weight [72]. Process control issues arise during deposition and bonding because precise alloy composition control is necessary to achieve the 280 °C melting temperature.

More recently, it has been shown that the $Au_{0.82}$ $Si_{0.18}$ eutectic bonding technique, which was first developed and used as a die attach method [80], can be used to bond wafers for absolute pressure sensors [82], a MEMS Pirani vacuum gauge with CMOS elements [56-58], and other MEMS and smart sensors using surrogate wafers [83-93]. In this method, Au is deposited using electroplating, sputtering, or evaporation. The Si substrate itself or a deposited Si layer serves as the source of the element. Diffusion barriers are incorporated for smart sensor applications to stop Au from diffusing into the CMOS device layers. The wafers are heated to a temperature of around 400 °C during bonding, and the Au and Si undergo solid-state diffusion until the eutectic composition is attained. The Au and Si layers are often produced on the same wafer because solid-state diffusion is necessary, guaranteeing close contact between the layers. As seen in Figure 2-9, bonding takes place between the liquid on the cap wafer and the matching Si or Au surfaces on the device wafer after the $Au_{0.82}$ $Si_{0.18}$ liquid, in this example, develops on the cap wafer.

This method has a number of advantages, including a material selection that is easily accessible, simple deposition, compatibility with MEMS release and cavity etch operations and the

Table 2-1: Eutectic Bonding Alloys and the corresponding Eutectic temperatures.

Alloy	Eutectic Temperature (°C)	Advantages	Disadvantages
$\mathbf{Au_{0.8}\ Sn_{0.2}}$	280	• Relative Maturity • Fluxless bonding • Deposition options	• Steep Eutectic liquidus lines • Under-seal metal (USM) integration challenges
$\mathbf{Au_{0.82}\ Si_{0.18}}$	363	• Ease of deposition	• Long bonding times • Under-seal metal (USM) integration challenges
$\mathbf{Al_{0.72}\ Ge_{0.28}}$	423	• Seal materials compatible with legacy CMOS processes	• Bonding temperatures at or near CMOS limits • Difficult to remove native oxide

absence of a native oxide on the Au surface. However, in addition to the diffusion barrier, an additional diffusion barrier is needed between Au and Si layers to prevent Si migration into Au, which may lead to SiO_2 formation or Si-rich alloys, which are not conducive to bonding. [80] The premature mixing can also be prevented by placing Au and Si on separate wafers prior to bonding [81,94]. However, in this case, very good control over the wafer planarity has to be implemented to ensure intimate contact between the bonding surfaces for the eutectic to form.

For 3D ICs [95], LEDs [96], passive test vehicles [97–104], and smart gyroscopes [105,106,110], the $Al_{0.72}Ge_{0.28}$ eutectic bonding method has been demonstrated. This sealing technique uses solid-state diffusion to generate the eutectic solution, just as the Au-Si method. On one or both wafers, layers of Al and Ge are placed, brought into contact with one another, and heated above the eutectic temperature of 423 °C. One of the drawbacks of this method is the formation of Al oxide, which is very difficult to remove effectively. To mitigate this, Ge is deposited on top of Al in a vacuum on the same wafer. This also ensures intimate contact between the two materials, thus facilitating solid-state diffusion and eutectic formation during heating. Diffusion barriers like Si, SiO_2 or tantalum nitride (TaN) can be used to prevent the mixing of the seal materials with Si substrate. The manufacturing and bonding of MEMS and CMOS components take place in the same foundry, as shown in figure 2-10 [105].

In this heterogeneous SoC technique, the vacuum package is formed by the wafer-to-wafer bond with the $Al_{0.72}Ge_{0.28}$ seal, and interconnects between CMOS and MEMS circuits are

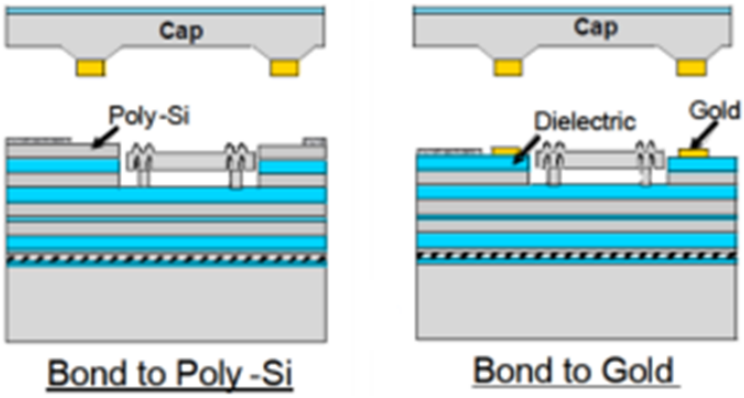


Figure 2-9: Bond directly to Poly-Si (left) or to gold (right)

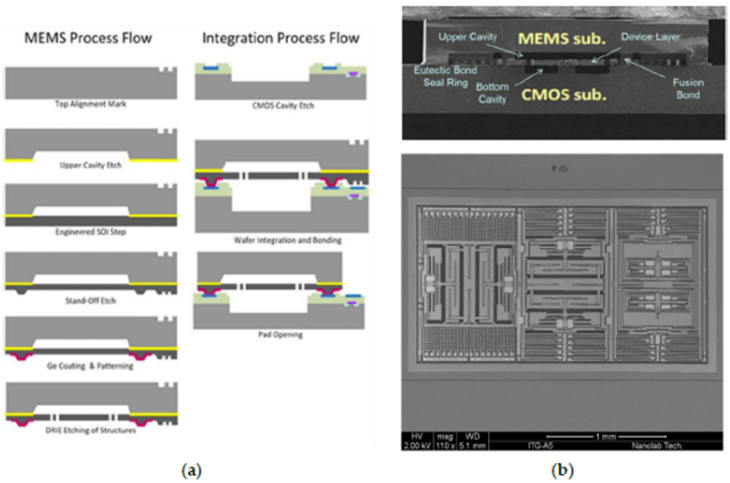


Figure 2-10: (a) Heterogenous process flow of MEMS wafer joined to Al pads and seal ring on CMOS wafer. (b) SEM image of gyroscope fabricated using the process flow.

created to build a MEMS gyroscope [106]. Several CMOS foundries now provide the process [107]. One of the main drawbacks of this approach is how close the bonding temperature is to the thermal limitations of the CMOS technology. It has been demonstrated that solid-state bonding below the eutectic temperature can lower bonding temperatures, albeit at the cost of substantial increases in bonding time and force [108].

Metal-Metal Thermo-compression Bonding

Diffusion bonding commonly referred to as metal-to-metal bonding, is based on the solid-state diffusion of metals at high temperatures and pressures. Typically, the same metal is put on each wafer, and self-diffusion creates a uniform metal seal (e.g., Al-Al, Cu-Cu, and Au-Au). The metal-to-metal approach has also been studied for IC interconnects [111,125] and WLVP on proxy surrogates [112], MEMS accelerometers [113], and infrared imagers [114], just like the previously described sealing techniques. On surrogate wafers, embodiments that produce IC interconnects and hermetic seals concurrently have been shown [115-119]. Examples of metal-to-metal bonding that are utilized for hermetic sealing and interconnects are shown in Figure 2-11.

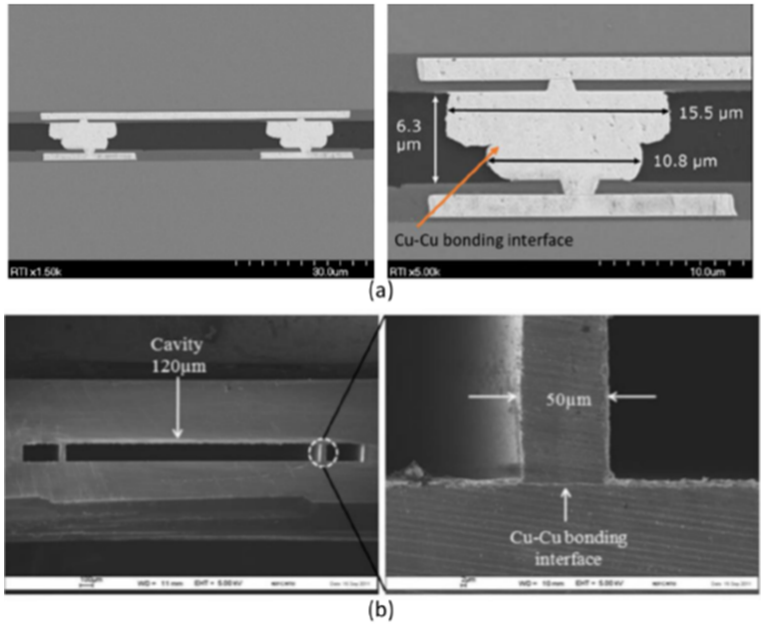


Figure 2-11: . (a) SEM image of Cu-Cu bonded interconnect. (b) SEM image of Cu-Cu thermal compression bonded hermetic seal [117]

This approach is less complicated and more adaptable with regard to upstream and downstream WLVP processes than the eutectic and SLID sealing techniques, which entail phase changes and generate different alloys. Wetting is not an issue since no liquid layer formed during bonding, which makes choosing an under seal metal (USM) material easier. The seal material is often deposited using evaporation, electroplating, and/or sputtering processes, which is also a simple process.

The mechanical pressure and temperature ramps and dwells are important bonding variables. Mechanical scrubbing and/or ultrasonic vibration are occasionally utilized to help

the self-diffusion. Pre-bond thermal treatments often have no effect on the metal-to-metal seal material, in contrast to the eutectic and SLID methods, which depend on interdiffusion. Kirkendall voiding is not a possibility since there is no interdiffusion.

The absence of a liquid layer makes this method more susceptible to oxide development and nonplanarity. A greater level of planarity is necessary to guarantee that the sealing surfaces are in contact throughout the whole wafer. Thermocompression bonding is frequently employed in combination with chemical mechanical planarization (CMP) and/or uniform deposition techniques (such as sputtering and evaporation) to guarantee consistent contact of the sealing surfaces. Additionally, soft metals with low melting points and generally low yield strengths need to be employed. As a result, the metals may deform plastically at pressures and temperatures that are suitable for CMOS and MEMS. If the sealing surfaces are somewhat out of plane, this deformation can make up for it. The three metals that are most frequently examined for this method are Al-Al, Cu-Cu, and Au-Au.

The existence of the native oxide is another hurdle for the metal-to-metal sealing of smart sensors, in addition to the requirements for planarity. The native oxides can be broken up and absorbed by the collapse of the underlying liquid layer in the eutectic and SLID methods. The oxides must, however, be completely eliminated before bonding in thermocompression bonding. The absence of a native oxide is one of the main benefits of the Au-Au solution. Cu does contain a native oxide, but it can be easily eliminated in the bonding process by using diluted acids either in situ or ex-situ. Cu-Cu thermocompression bonding has also been established using self-assembled monolayer (SAM) technology, which inhibits oxide development [118,120-122]. Al is a popularly utilized soft metal for contact pads in CMOS processing, making it a desirable option as well. Higher bonding temperatures and pressures are, however, necessary [113] because the native Al oxide is difficult to remove. Furthermore, larger degrees of the CTE mismatch brought on by Al's comparatively high CTE might cause additional stress in Si packages.

Table 2-2: Relevant properties of commonly used metals in Thermo-compression bonding [123,124].

Metal	**Bonding Temperature (°C)**	**Self-Diffusivity** (m^2/s)	**Activation Energy (eV)**	**CTE** ($\mu m/m.K$ **at 25 °C)**	**Melting Temperature (°C)**
Aluminum (Al)	> 400	4.2×10^{-19} (at 500 °C)	1.49	23.1	660
Copper (Cu)	> 350	4.2×10^{-14} (at 500 °C)	2.19	16.5	1084
Gold (Au)	> 350	1.0×10^{-18} to 1.0×10^{-19} (at 400 °C)	1.81	14.2	1064

The metal used, the pressure, the planarity, and the cleanliness of the surface together deter-

mine the bonding temperatures. Typically, bonding pressures range from 0.2 to 10.0 MPa, while bonding times range from 30 to 120 minutes. A robust seal and post-bond anneal are frequently utilized to prolong the solid-state diffusion process and create a hermetic seal. The additional bonding and anneal time may raise gas pressure inside the package; therefore, it must be adjusted properly. Metals with relatively high self-diffusivities and low activation energies should be used to reduce bonding time and temperature. The seal materials' characteristics and typical bonding temperatures are shown in Table 2-2.

Table 2-3: Comparison of Metal-Based Bonding approaches [4].

Bonding Approach	Main Advantages	Main Disadvantages
Eutectic alloy	• Ductile seal	• Complex deposition • Bonding temperature dependent on alloy stoichiometry • Under-seal metal (USM) can react with eutectic alloy
SLID	• Mature deposition and bonding processes • Re-melting temperature is greater than bonding temperature	• Lack of ductility in seal • Possible formation of Kirkendall voids and scallops.
Metal-to-metal	• Mature deposition and bonding processes • Relatively simple deposition and metallurgy	• No collapse layer to absorb topography • Oxide removal more critical • Generally requires higher force and temperature during bonding

2-2-3 Novel bonding Approaches

So far, the standard metal bonding approaches used in the industry have been discussed. However, all of these approaches have their merits and drawbacks. Thus, a trade-off is always required in selecting bonding methods based on the requirements of a particular application. These trade-offs have been summarized in table 2-3. Several novel metal bonding techniques have been proposed in research to overcome the drawbacks of standard metal-based bonding approaches. These approaches are focused on making the metal-based bonding more com-

patible with the CMOS processes and improving the bond quality in terms of bond strength, surface topography tolerance, better vacuum, etc., with a smaller seal ring footprint for continued miniaturization of MEMS devices for reduced costs. Some of these novel approaches provide valuable insights into the method of sealing used in this study of vacuum sealing using nanoparticle sintering. These novel approaches have been discussed in the next section.

Wafer Bonding using Plastic Deformation

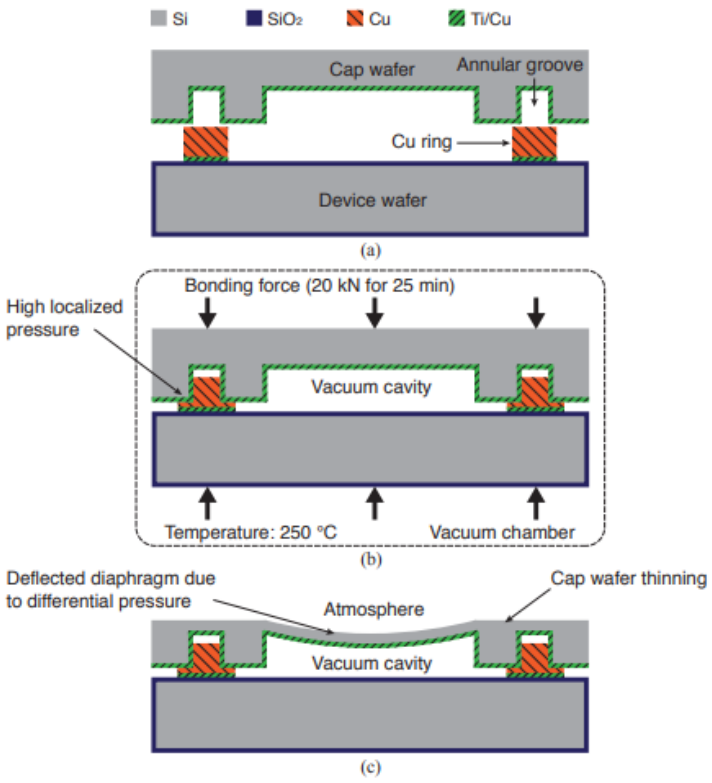


Figure 2-12: A cross-sectional overview of the vacuum sealing method's process flow. (A) Electroplating of Cu rings on the device wafer according to a mould. (b) Cu deposition on the cap wafer and Si DRIE of the grooves and cavities, followed by alignment of the two wafers. (c) Wafers are joined and bonded at a temperature of 250 °C inside a vacuum chamber, closing the enclosed cavities.

Xiaojing et al. proposed a low-temperature wafer-level vacuum sealing approach using narrow Cu seal rings (below 10um) without adding any bond enhancements [7]. Fig. 2-13 shows the proposed sealing structure based on low-temperature Cu welding.

At a low temperature of 250 °C, electroplated Cu rings fabricated on the device wafer are pressed against matching grooves (covered by 300 nm-thick Cu) in the cap wafer. High localized pressures are present at the bond interfaces because of the tiny contact area between the wafers, which causes plastic deformation of the Cu rings and makes it easier to accomplish the subsequent solid-state Cu-Cu diffusion bonding processes. This process culminates in forming a hermetic seal, with the bonding temperature decreasing to 250 °C as opposed to the traditional Cu-Cu thermo-compression bonding temperature range of 300-450 °C.

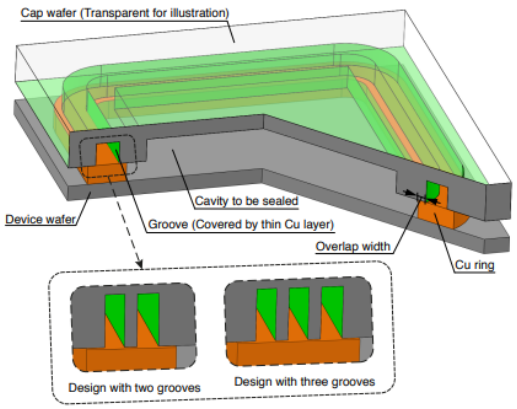


Figure 2-13: Schematic of the thin Cu ring sealing structures. There are three designs, each with a different number of grooves from 1-3.

In fig. 2-12, the wafer bonding process flow is shown. Following the two wafers' alignment, a wafer bonder was used to carry out the bonding. 20 kN of bonding pressure force was applied for 25 minutes. During the bonding and sealing, the bonder chamber was pumped to a vacuum of 7 x 10-5 mbar. The Cu sealing rings would deform plastically due to the predicted localized pressure of 550 MPa, which is 2.4 times the documented yield strength of electroplated Cu [126] at the beginning of the bonding process. The cap wafer was thinned down by Si reactive ion etching after bonding.

Bond Analysis and sealing yield analysis were done on the various designs. The design with a 13.5um seal width with two grooves achieved a 100% sealing yield after three months of storage.

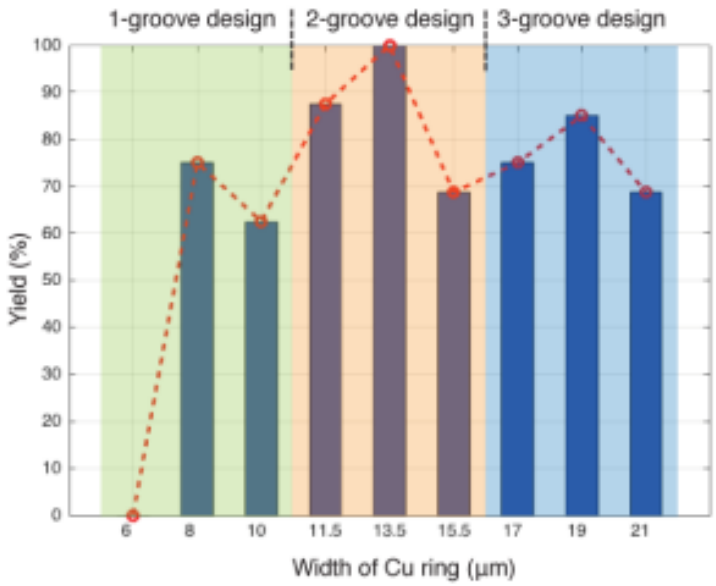


Figure 2-14: Sealing yield after three months of atmospheric pressure storage as a function of the Cu sealing ring width.

SEM imaging of the three bond interfaces indicates the occurrence of large-scale plastic deformation of Cu rings due to very high localized pressures, as illustrated in figure 2-15.

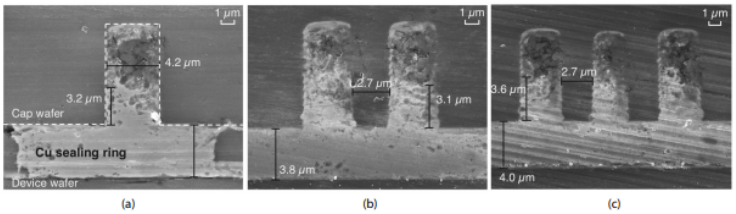


Figure 2-15: Cross-sectional SEM images of (a) 1-groove design (b) 2-groove design (c) 3-groove design

For hermeticity evaluation of the designs, a leak rate test was carried out by observing the cap deflection for 97 days. A conservative estimate of the leak rate was found to be 1.3×10^{-12} mbarL/s. For the measurement of absolute pressures inside the cavities, residual gas analysis (RGA) was conducted, and the highest pressure detected was 10^{-2} mbar 146 days after bonding. The bond shear strength test was also carried out, revealing a strength above 90MPa for all the designs.

Nanoparticle-Based Bonding Methods

Process simplicity and thermal compatibility with CMOS devices are the most critical factors for a better wafer bonding approach. Within the various metal-based approaches, thermo-compression bonding was the simplest of approaches in terms of process complexity. However, it suffered from the drawback of higher bonding temperatures and lower tolerance for highly varying surface topography. By using metal nanoparticles instead of their bulk counterparts, the surface topography can be accounted for because of their tiny size. Moreover, because of their increased surface area, the reactivity of these particles is also higher than in the bulk state, which translates to lower fusing and bonding temperature [28]. There have been several attempts at realizing metal nano-particle-based wafer bonding in recent literature. In the next section, the studies relevant to the study performed in this thesis have been elucidated briefly.

- **Wafer Bonding using Sub-Micron Gold Particles**

  By adopting a narrow-width rim structure and utilizing sub-micron-size gold particles (0.3μm mean diameter), H. Ishida et al. [28] successfully accomplished wafer-level hermetic seal bonding within the range of commercial wafer bonders. A practical fabrication technique was used to create sealing lines over the rim structure: conventional stencil printing in conjunction with a newly created suspended metal mask. Au-Au thermo-compression bonding was carried out at 200 C for 30 minutes with a bonding pressure of 200 MPa using a ten μm-wide rim structure. Excellent hermeticity was attained, and the sealed cavity's encapsulated pressure was calculated to be roughly 100 Pa.
  Wet chemical processing was used to synthesize the spherical, sub-micron-sized, 99.95wt% pure Au particles by combining a reducing agent with a chloroauric acid solution. Individual gold particles with mean diameters of 0.3μm and a range of 0.2μm to 0.5μm were

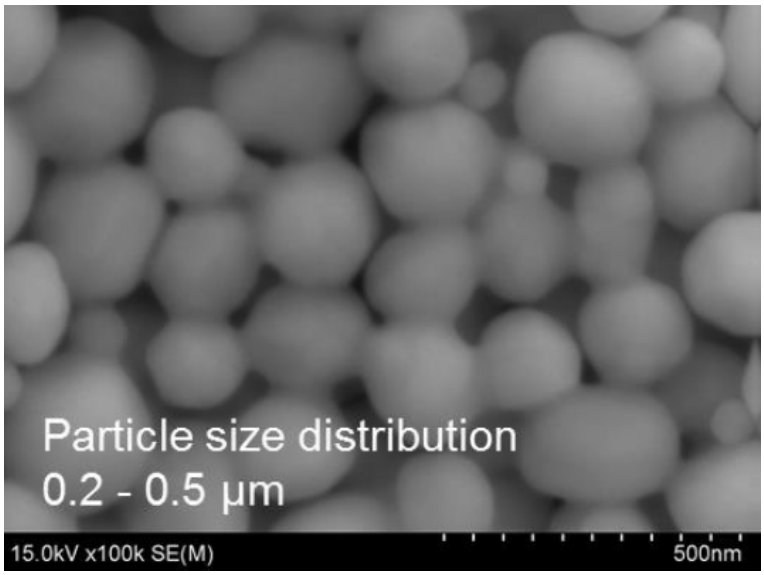


Figure 2-16: SEM image of Sub-micron Au particles without compression at 150°C [28].

obtained. The particle size significantly impacts the reactivity of the Au particles. Even at 200°C, these sub-μm Au particles are capable of connecting and reacting with one another. Figure 2-16 depicts the sintering behaviour of sub-μm Au particles at 150°C for 5 minutes in the air without compressive force, showing that the necking reaction occurs even at such a low temperature.
The test sample wafer-level manufacturing process is depicted in Figure 2-17. On a 100 mm Si wafer, ten μm tall and ten μm wide rim structures were created using deep RIE, and an Au/Pt/Cr (0.2/0.03/0.03 μm thick) metallization layer was created using sputtering. By employing a high-precision screen printer and a suspended Ni-metal mask in conjunction with a traditional stencil printing technique, sub-μm Au particles paste (AuRoFUSETM, Tanaka Kikinzoku Kogyo KK) was used to cover the rims.

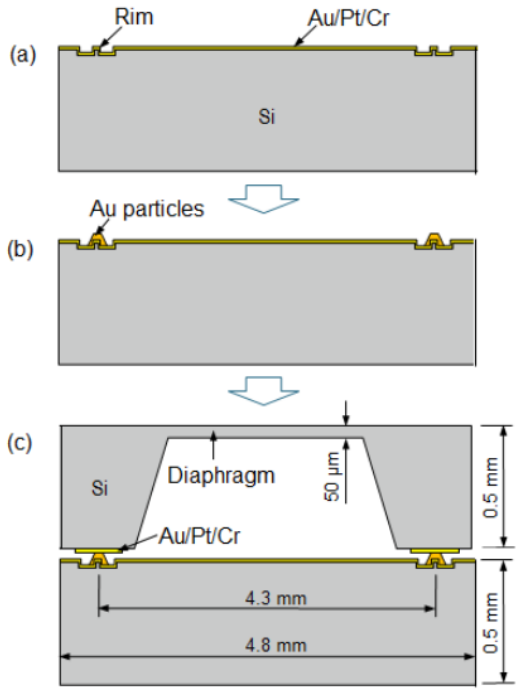
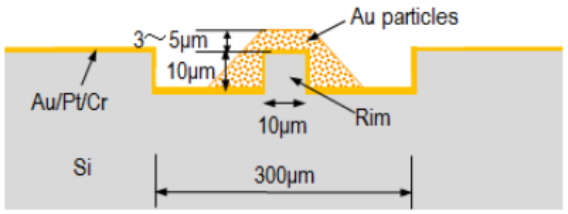
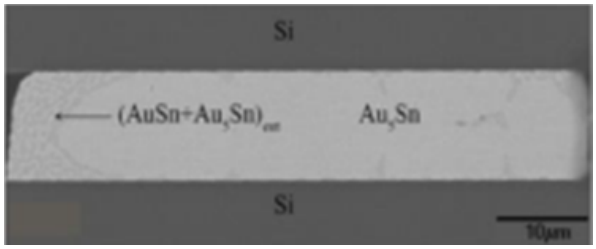


Figure 2-17: Schematic of the process flow [28].



(a) Schematic of the rim with Au paste.



(b) SEM image of the rim with Au paste on top.

Figure 2-18: A rim structure covered with sub-micron Au particles [28].

Figure 2-18a depicts a cross-sectional view of the sub-μm Au particle paste-coated rim pattern, and figure 2-18b depicts an SEM top view of the coated rim structure. The bond aligner (BA8, SUSS MicroTec AG) was used to precisely align the rim wafer and the diaphragm wafer after the rim wafer had been annealed at 200°C for two hours. The aligned wafer pair was subsequently bonded using a commercial wafer bonder (SB8e, SUSS MicroTec AG) for 30 minutes at 200°C with 200 MPa of applied pressure to

create the structure seen in figure 2-17(c). To evaluate the bond's strength and hermetic properties, the bonded wafer pair was cut into individual chips.
Die shear testing of the test chip with a 4.3mm-square sealing line revealed a shear strength for a ten-μm-wide rim was 44N. Concerning the hermeticity of the package, the cap deflection method was used, and a pressure of 100 Pa was estimated within the cavity. Moreover, the helium fine leak test revealed the leak rate to be in the range of 10^{-14} Pa m^3/s.

- **Wafer Bonding using Cu Nanoparticles**
  Over recent years, there have been a few attempts to realize Wafer Level bonding and 3D interconnect technology using Cu nanoparticles in literature.

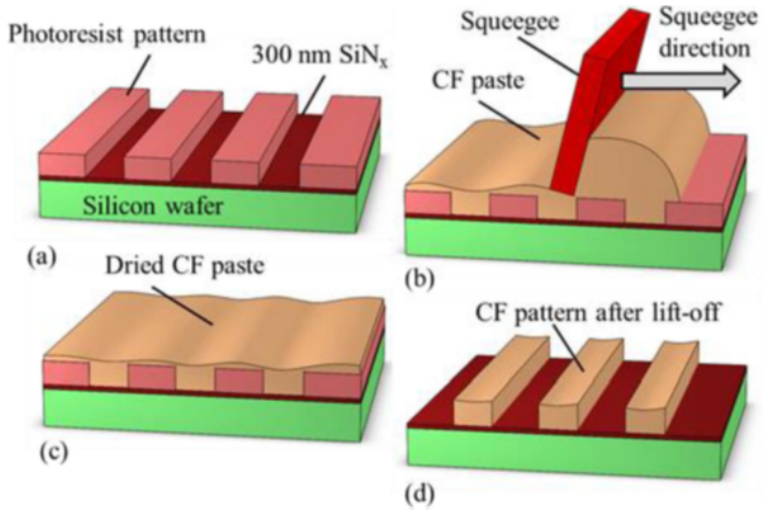


Figure 2-19: Process flow of Lithographic screen printing of Nano copper paste.

For 3D interconnect applications in wafer-to-wafer (W2W) bonding, B. Zhang et al. at [36] investigated a technique for patterned copper nanoparticle paste. Using coated copper nanoparticle paste, a revolutionary fine pitch thermal compression bonding (sintering) technology has been created. The majority of the particles range in size from 10 to 30 nm. The paste was applied and patterned utilizing lift-off and lithographically defined stencil printing (figure 2-19).
The bottom wafer with patterned Nano-Cu paste on top was bonded with a cap wafer with a process flow illustrated in Figure 2-20 at 260 °C.
A low electrical resistivity at 7.84 $\pm$ 1.45 $\mu\Omega$.cm was obtained, which is about 4.6 times that of bulk copper after sintering at 260°C for 10 min, in a 700 mBar forming gas(H_2/N_2) environment. A FEM analysis was also done for the effect of porosity on Electrical resistivity, indicating that the conductivity increased with decreasing porosity. These results suggest that changing the sintering parameters can affect the sintered nano-Cu's electrical properties and hence the nanoparticles' porosity.
In another study by J. Li et al. [127], a wafer bonding experiment was carried out at 300 °C under a low sintering pressure of 0.98 MPa. The cross-sectional microstructure of Cu-Cu bonding joints is depicted in SEM pictures in Fig. 2-21. The Cu-Cu joint exhibits an unconsolidated bonding morphology when the bonding temperature is less than 200

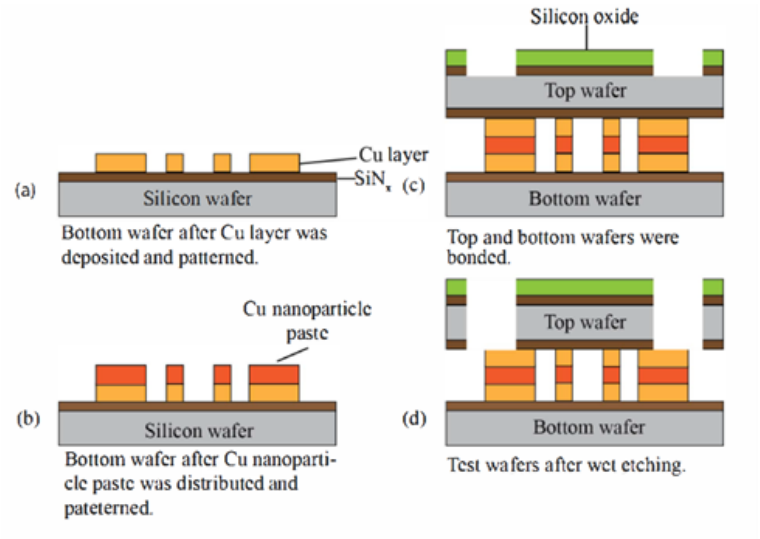


Figure 2-20: Process flow of wafer bonding process using lithographically patterned Cu-NP paste.

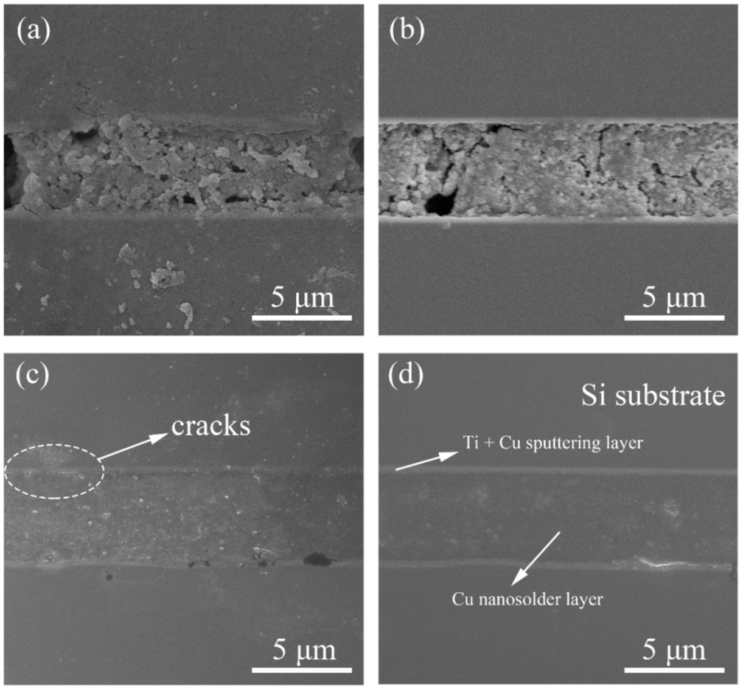


Figure 2-21: Cu-Cu bonding joints' cross-sectional microstructure as shown in SEM images taken at (a) 150 °C, (b) 200 °C, (c) 250 °C, and (d) 300 °C

°C. Cu nanoparticles' insufficient sintering is the primary cause of the defects, and the morphology of the particles can be clearly seen. The Cu-Cu bonding connection exhibits a compact microstructure when the bonding temperature is raised to 250 °C; however, some fractures and flaws can also be seen at the nano solder layer/substrate contact. The Cu-Cu junction is filled with well-sintered Cu nano solder paste at a bonding temperature of 300 °C. The substrate is tightly integrated with the sintered nano solder layer, and there are no evident defects, indicating a stable structure. Moreover, a study of bond strength vs Sintering temperature was also carried out. The results indicate that a higher sintering temperature corresponded to a better bond shear strength, as seen in figure 2-22.

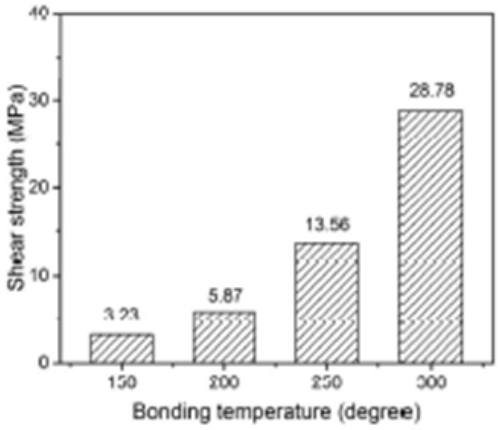


Figure 2-22: Shear strength of Cu-Cu bonding joint at different bonding temperatures.

2-3 Effect of sintering parameters on NP Sintering : Temperature and Pressure

Sintering is a thermal process for connecting particles into a coherent, mainly solid structure by atomic-scale mass transfer events, resulting in improved strength and decreased total system energy. The sintering of NPs starts with the formation of sintering necks, followed by the coalescence or fusion of the nanoparticles, as indicated in Figure 2-23. Typically, the contacting neck is where the majority of the coalescence for Cu NPs at a low temperature (573 K) takes place. The area distant from the neck has little impact on how well Cu NPs sinter [128].

In general, at least five mass transport processes are involved in the coalescence of NPs during sintering, including grain boundary diffusion, surface diffusion, volume diffusion, dislocation activity, and surface evaporation-condensation [129]. Surface diffusion, also known as atomic diffusion, is the term used to describe how atoms travel from one surface to another to liberate energy. The bonding parameters, primarily the process temperature and applied pressure, impact the diffusion rate. The free movement of metal atoms in vacant atomic lattice positions forms the basis of grain boundary diffusion. It is based on the movement of atoms along the boundaries of atomic lattice mismatches and grains and takes place in polycrystalline layers.

Bulk or volume diffusion is based on the movement of atoms inside the lattice by exchanging positions with vacancies. The study by D. Hu et al. [128] provides some valuable insights into the coalesce process of Cu NPs, which is relevant for this thesis.

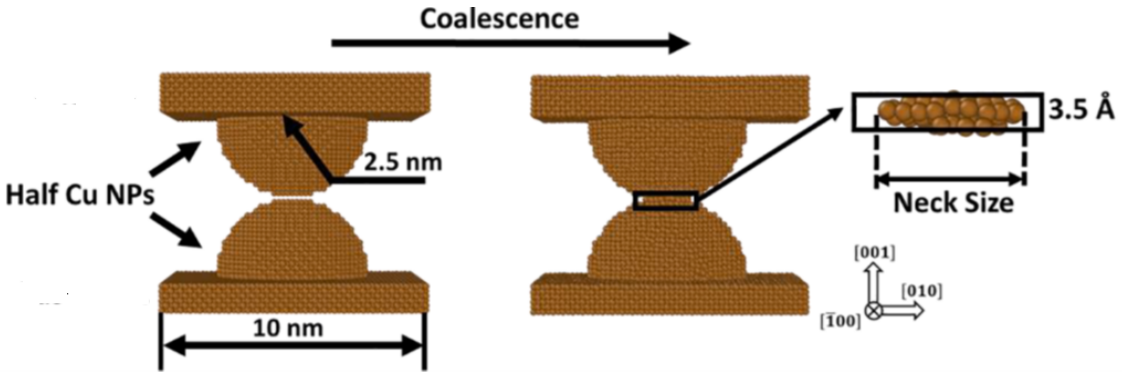


Figure 2-23: Two-half Cu NPs model and geometric parameters for the coalescence simulation. [128]

A molecular dynamics simulation was used in this work to analyze the impact of pressure and temperature on the coalescence of Cu nanoparticles. There are two ways that pressure might affect sintering:

- It increases atomic diffusion both at the surface and in the volume during Cu NPs and causes plastic deformation.
- As soon as adequate pressure is applied, defects are generated, and the microstructure is stimulated to evolve, increasing dislocation density and facilitating mass transport.

Thus, successfully sintered Cu NPs can be produced even at low temperatures (573 K), as atoms can move along high-density dislocations and grain boundaries with low energy.

In contrast, the influence of temperature varies with the microstructure of Cu NPs. With fewer defects, NPs agglomerate mostly through surface diffusion, which is minimally influenced by an increase in temperature. Temperature has a key influence in sintering with a greater defect density due to the fact that atomic migration around defects can be greatly enhanced at higher temperatures for structures with a high defect density. In addition, a higher pressure will also result in an increase in flaws; hence, the effect of temperature will be compounded.

In addition, the elastic modulus and tensile strength of sintered Cu NPs were discovered to be affected by the sintering pressure and temperature. On the one hand, the structure sintered at a higher pressure and temperature exhibited superior mechanical properties, such as a greater elastic modulus and tensile strength. In contrast, between 300 K and 500 K, the sintering pressure increased from a pressure-free condition to 300 MPa, influencing the mechanical characteristics of Cu NPs in a manner comparable with its influence on the coalescence degree of Cu NPs.

2-4 Conclusion

This chapter provided a background to the various bonding technologies in the current Wafer Level Vacuum Packaging (WLVP) scenario while discussing the pros and cons of each ap-

proach. It can be concluded that metal-based approaches, especially the metal-based thermo-compression approach, are the most suitable because of the less complex process. Furthermore, introducing metal nanoparticles instead of the bulk counterpart also ensures good thermal compatibility with CMOS processing by lowering the bonding temperature and a good surface topography tolerance due to the small size of NPs.

A survey was also done on the recent attempts at bonding using Cu NPs. All the studies indicated a good bond shear strength. However, there was no report on the hermeticity of the bond. The NP coalescence process's kinetics depicts pressure's increased role in the sintering of Cu NPs [128]. Thus, to lower the temperature, pressure-assisted sintering can be implemented to lower the porosity of the coalesced NPs, thereby promoting an excellent hermetic seal.

Based on the insights gained from this literature survey in this chapter, a design of the test microstructure will be devised in the next chapter.

Design and Methodology

3-1 Introduction

From the extensive literature survey in the previous chapter, pressure-assisted Cu NP was found to be the best approach to reduce the porosity of the coalesced Cu NPs as much as possible, which can ensure a hermetic sealing environment inside the cavity. Therefore, our design maximizes localized pressures on the seal for a given seal width. The following section will focus on ideas taken from the literature to formulate such a design. Moreover, the choice of materials for the layer stack-up will also be selected. Finally, simulations will follow this to consolidate further on the theory established.

3-2 Choice of materials

Choosing the right material for the layer stack-up is crucial for achieving high-quality bonding. It was decided to employ a Ti/Au layer stack up for the top (cap) wafer and a $SiO_2/Ti/Au$ layer stack up as the intermediary layer between the Device substrate (Si) and the nano-Copper layer for the bottom (device) wafer. The following factors were taken into account when making these decisions:

- The SiO_2 layer was chosen as the bottom wafer's first layer to insulate the device wafer substrate from the fused nano-Cu sealing rings and thus prevent shorting of the encapsulated devices.
- The titanium (Ti) layer acts as a very excellent adhesion layer because it bonds well with SiO_2 and forms alloys with gold (Au), providing good adhesion to the continuing thickness build-up of the gold (Au) layer[140].
- Titanium (Ti) also acts as an effective diffusion barrier, preventing copper (Cu) from diffusing into the Silicon (Si) Substrate [141].
- The Au/Ti bi-layer stack has also been reported to have low-temperature activation getter material properties, allowing it to absorb gases emitted by outgassing or leaks, hence enhancing the package's vacuum level [142].

3-3 Design for high localized pressure

Pressure on any region is defined as the force per unit area on that region. Therefore, for a constant force applied, in order to increase the pressure, the area of the region has to be minimized. This can be accomplished for a given area using a groove or rim-type structure.

In the study by H. Ishida et al. [28], a rim-type structure was used under the Au nanoparticles to increase the local pressure on Au particles on top of the rim. This can be clearly seen in the FIB-SEM images of the rim joint after the tear-off of the diaphragm chip (figure 3-1). It is evident from the images that the Au particles on top of the rim have densified to a much higher degree as compared to the region around the rim. This can be attributed to higher localized pressure on top of the rim. This localized densification ensures that the voids are reduced as well as isolated at the same time, thus ensuring a hermetic seal.

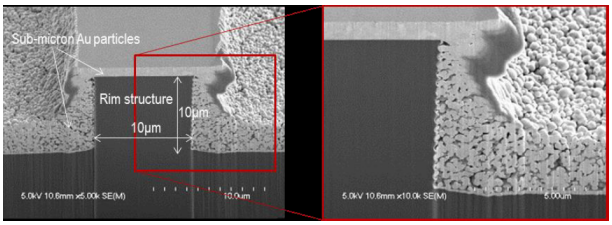


Figure 3-1: SEM image of sintered Au particles in WLVP[28].

On the other hand, a groove-based design was used in the study with the WLVP using plastic deformation of Cu, as illustrated in the previous chapter. In this design, the device wafer with the Cu sealing rings is aligned to the cap wafer with the corresponding annular grooves. Next, the wafers are pressed together at a temperature of 250 °C. The Cu rings are slightly wider than the grooves, resulting in small overlapping areas of the rings and grooves experiencing very high localized pressures that exceed the yield strength of Cu (≈233 MPa) [44] and, thus, inducing plastic deformation of the Cu rings. It is visible from the SEM imaging (figure 3-2) of the bonded wafers after cleaving that the Cu from the sealing ring on the device wafer is wedged into the grooves in the cap wafer, verifying that the plastic deformation of Cu has occurred as expected.

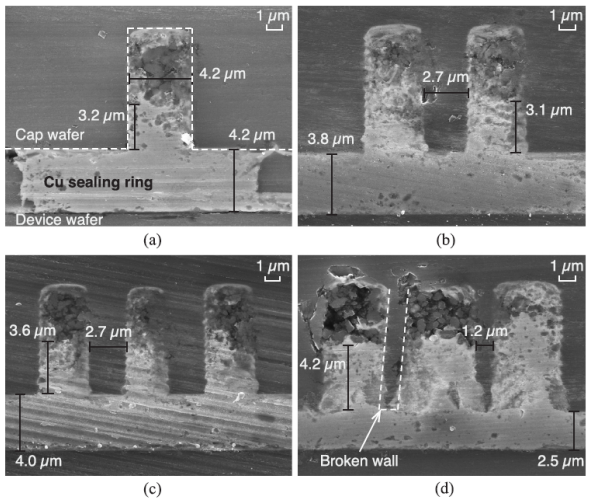


Figure 3-2: Different sealing rings and the corresponding grooves at the bond interface are shown in cross-sectional SEM pictures. The dashed line shows the interface between the cap wafer and the device wafer[28].

A groove-based design was chosen, with the goal of reducing the number of process steps

and, consequently, process complexity. Figure 3-3 shows an illustration of this. The nano-Cu sealing rings on the device wafer are aligned with the corresponding annular grooves on the bottom wafer. The bottom wafer and the top wafer with the cavity are then pressed together at various temperatures and pressures. The nano-Cu rings are slightly wider than the grooves, resulting in very high localized pressures in the narrow overlapping regions of the rings and grooves.

Varying design variants of the sealing structures with different dimensions are included on the same wafer (shown in the close-up drawings in Fig. 3-4) to study the bonding and sealing capabilities of different designs. The simplest instance simply involves one annular groove in the device wafer. The design variables for the designs that were chosen for this study are the overlap width (t_{ov}) at the edge of the nano-Cu rings on the device wafer, the number of annular grooves (N_g) in the device wafer, and the distance between the grooves (d_g). The reason for this is that these design variables have a direct impact on the available surface area for the nano-Cu sintering process. In all cases, only one nano-Cu sealing ring surrounds each cavity on the device wafer.

The smallest overlap width of 2μm was chosen to account for the alignment accuracy of the manual mask alignment process in the cleanroom. The relationship between the various design variables and the total sealing width can be devised from the following relation:

$$S_W = N_g w_g + (N_g - 1)d_g + 2t_{ov} \tag{3-1}$$

Where is the sealing width, is the number of annular grooves, is the distance between the grooves, and is the width of the overlap region between the nano-Cu ring and the grooves. Table 3-2 lists the essential design characteristics and Table 3-1 describes the details of each of the 15 distinct designs. Moreover, the corners of the ring were decided to be kept rounded to avoid higher stress values in the case of sharp corners [146] with the radius of the rounded corners based on the figures obtained from the literature [7,28].

For confirming the hermeticity of the package, the thin membrane deflection method, as described later in section 3-5-1 was used. Therefore, a cavity was incorporated into the design to have a thin membrane on top. The membrane dimensions were decided based on the structures already used in the literature [7,28] for attaining a good sensitivity of leak rate detection.

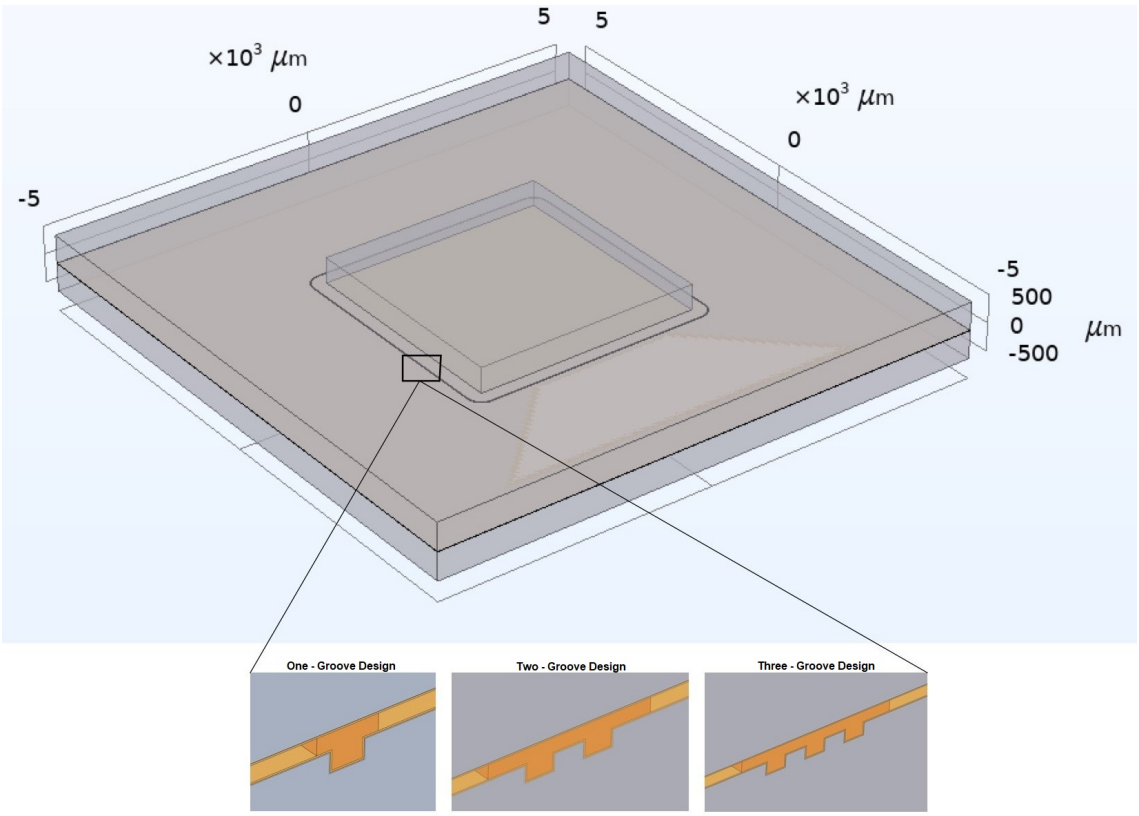


Figure 3-3: Proposed design with a groove-based structure.

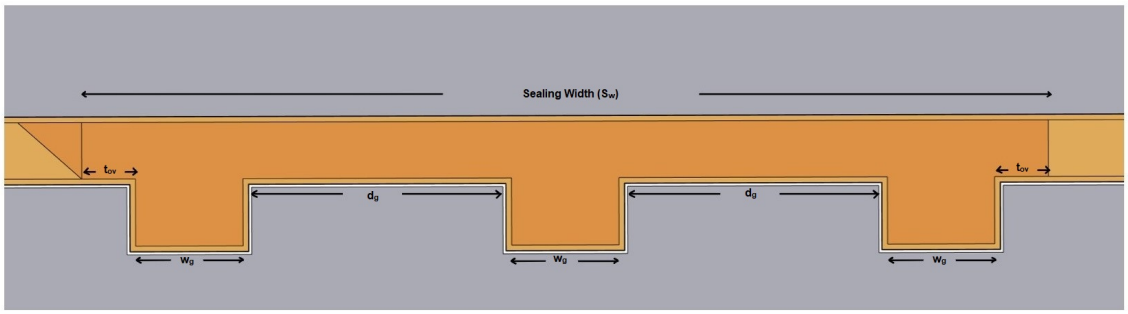


Figure 3-4: The various design variables of the groove structure.

Table 3-1: Details of each of the designs.

Design Number	**Number of Grooves** (N_g)	**Distance between Grooves** (d_g)	**Overlap Width** (t_{ov})	**Design Name**	**Sealing Width** (S_W)
1.	1	-	2μm	**G1-O2**	8μm
2.	1	-	4μm	**G1-O4**	12μm
3.	1	-	6μm	**G1-O6**	16μm
4.	2	5μm	2μm	**G2-O2-D5**	17μm
5.	2	5μm	4μm	**G2-O4-D5**	21μm
6.	2	5μm	6μm	**G2-O6-D5**	25μm
7.	2	10μm	2μm	**G2-O2-D10**	22μm
8.	2	10μm	4μm	**G2-O4-D10**	26μm
9.	2	10μm	6μm	**G2-O6-D10**	30μm
10.	3	5μm	2μm	**G3-O2-D5**	26μm
11.	3	5μm	4μm	**G3-O4-D5**	30μm
12.	3	5μm	6μm	**G3-O6-D5**	34μm
13.	3	10μm	2μm	**G3-O2-D10**	36μm
14.	3	10μm	4μm	**G3-O4-D10**	40μm
15.	3	10μm	6μm	**G3-O6-D10**	44μm

Table 3-2: Important design characteristics of the nano-Cu seal.

Number of Annular grooves (N_g)	1/2/3
Overlap Width(t_{ov})	2μm/4μm/6μm
Distance between grooves (d_g)	5μm/10μm
Width of Grooves (w_g) $\times$ height	4μm
Sealing Ring Width (S_W)	(8μm - 44μm)$\times 3.5\mu$m
Cavity Size ($l \times w \times h$)	4000μm$\times 4000\mu$m$\times 450\mu$m
Radius of the rounded corners	250μm

3-4 COMSOL Modelling for design

To validate the theory developed in the preceding section, a COMSOL simulation was carried out using the established design and compared to a design with no grooves in terms of pressure on the seal during the sintering process.

3-4-1 Method

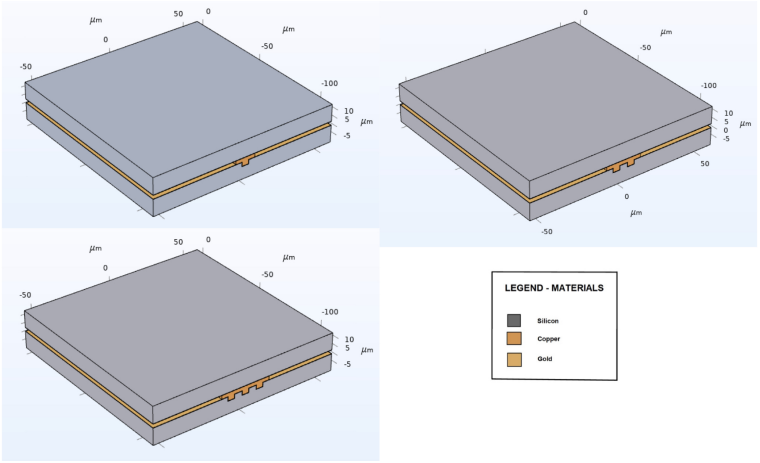


Figure 3-5: . The sub model of the geometry of the groove-based design.

As depicted in figure 3-5, a sub-model was employed to minimize the computing resources required for the simulation and to obtain the appropriate level of detail for the exceedingly small size of the seal ring relative to the overall structure. Furthermore, the following simplifying assumptions were applied:

- The top and the bottom Silicon has been considered to be a rigid body as the dimension of the top and bottom Silicon is much larger than the nano-Cu seal.
- The Titanium and Silicon Dioxide layers have been ignored due to their very small thickness (20nm and 100nm respectively) and location away from the die surface-seal ring interface.
- The nano-Copper layer is considered to be sintered with 0% porosity; thus, properties of bulk Copper have been applied. This assumption may however lead to an overestimation of pressure value due to the higher stiffness of bulk Copper as compared to nano-Copper. However, due to the highly variable, porosity-dependent material properties of nano-Cu paste [148], this assumption has been applied and can be seen as the worst-case scenario within the context of this simulation.

A summary of the material properties used in the simulation have been summarized in table 3-3.

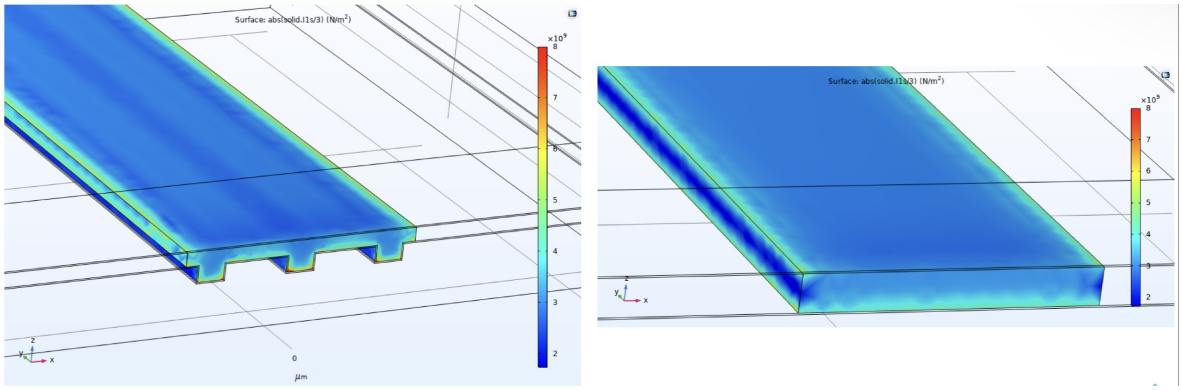
Table 3-3: Summary of material properties used in the simulation.

Material	Young's modulus (GPa)	Poisson ratio	CTE (1/K)	Thermal Conductivity (W/mK)	Length (mm) x Width (mm)	Thickness (μm)
Silicon	170	0.28	2.6×10^{-6}	130	113.4 × 113.4	10
Gold	70	0.44	14.2×10^{-6}	317	113.4 × 113.4	0.2
Nano-Cu	120	0.34	16.5×10^{-6}	401	Design Dependent	4.6

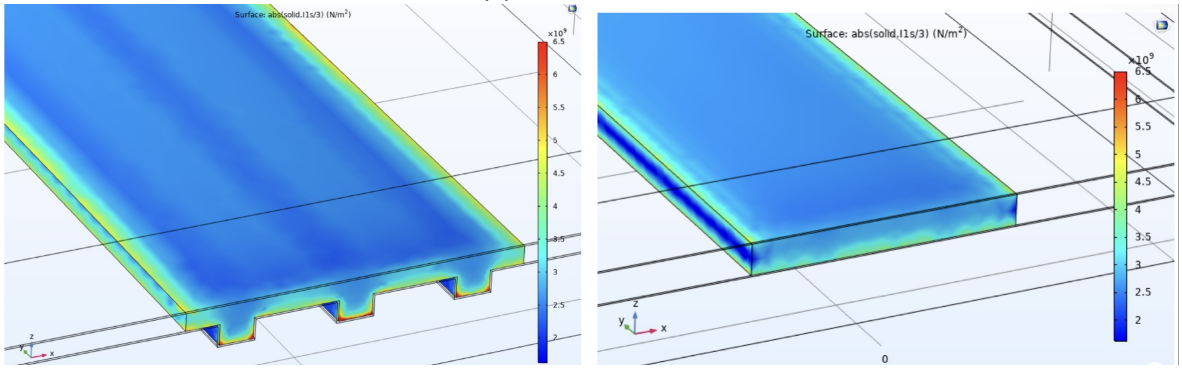
The solid mechanics module of COMSOL Multiphysics was utilized for the model, along with a Multiphysics coupling of the heat transfer in solids module. A stationary analysis was done with an applied body load applied to the top Silicon which is equivalent to the applied force of 2000 N on the 10 mm × 10 mm top die of the proposed design and a temperature of 573.15 K with the initial temperature being 293.15 K. The pressure on the seal ring was visualized using the different plotting options provided in COMSOL Multiphysics followed by the analysis of the results obtained.

3-4-2 Results

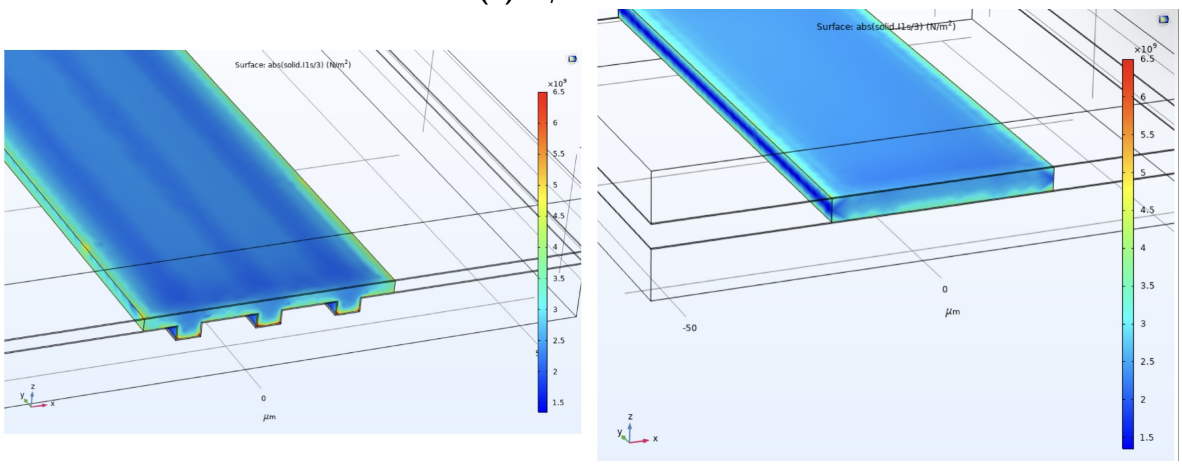
Qualitative Comparison of Pressure on the seal ring



(a) 36μm seal width.



(b) 40μm seal width.



(c) 44μm seal width.

Figure 3-6: Volumetric Pressure Profile of a single groove design.

To have a better understanding of the pressure profile in the sealing ring with the proposed design as opposed to a standard design with no grooves, a surface pressure plot was then

utilized to demonstrate the pressure profile comparison between the groove and no groove cases with the same sealing width as illustrated in figure 3-6.

The pressure plot with all of the different dimensions of the seal width indicates that there is higher volumetric pressure at the seal ring's overlapping regions and the region between the grooves in all of the grove-based designs than in the corresponding no-groove-based design with the non-groove design having a lower pressure at regions away from the interface. Moreover, it can also be seen that the non-groove design has more uniform pressure over the surface, as compared to the groove-based design with lower pressure values near the groove region and higher pressures in the overlap region at the edges and the region between the grooves. This indicates the presence of localized high-pressure regions in the groove-based approach.

Quantitative Comparison of Pressure on the seal ring

Following this, a quantitative comparison of the average volumetric pressure values for each design versus a standard no-groove design was performed and the results have been illustrated in figure 3-7.

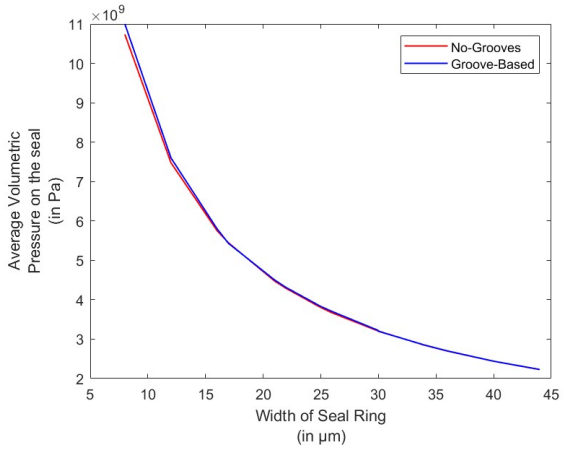


Figure 3-7: Comparison of groove-based design to non-grove design in terms of average pressure vs seal width.

The plot depicts that the average pressure values for both the groove and non-groove-based designs are approximately the same with the groove-based design having slightly higher average pressure at smaller seal widths. To get more insight into the uniformity and distribution of pressure within the volume of the seal ring, a standard deviation plot of the volumetric pressure vs the sealing ring width was plotted for both designs. A higher standard deviation would indicate a higher non-uniformity in the volumetric pressure, with more extreme values of volumetric pressure, thereby confirming the presence of localized higher and lower pressure regions. The results of this analysis have been plotted in figure 3-8

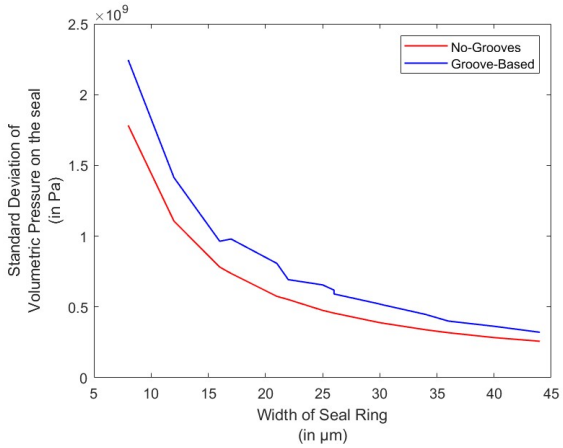


Figure 3-8: Standard Deviation of Volumetric Pressure values on seal ring for different designs during bonding.

The results indicate that the groove-based designs have on average 1.32 times higher standard deviation values for volumetric pressure than the non-groove counterparts for the same seal ring width. This, in combination with the average pressure results, confirms the presence of localized high pressures with the groove-based design, which is consistent with the earlier qualitative analysis that revealed regions of lower and higher pressure with the groove-based design.

Effect of overlap width and distance between the grooves on the standard deviation of volumetric pressure

As established in the previous section, the standard deviation can be used as a means to determine the presence of localized high-pressure hot spots within the sealing ring. Moreover, from the qualitative analysis (section 3-4-2), it could be seen that the hot spots are present in the overlapping regions and the region between the grooves which are defined by the geometry parameters t_{ov} and d_g established in section 3-2.

Therefore, a parametric study was done for the effect of the geometry parameters t_{ov} and d_g, for the different numbers of grooves. Moreover, to mitigate the effect of the seal ring width on the standard deviation values of pressure, the data was normalized by dividing the volumetric pressure standard deviation values of a particular design with a certain seal ring width with the corresponding non-groove design of the same seal ring width. The results were then plotted as a surface plot as depicted in figure 3-9.

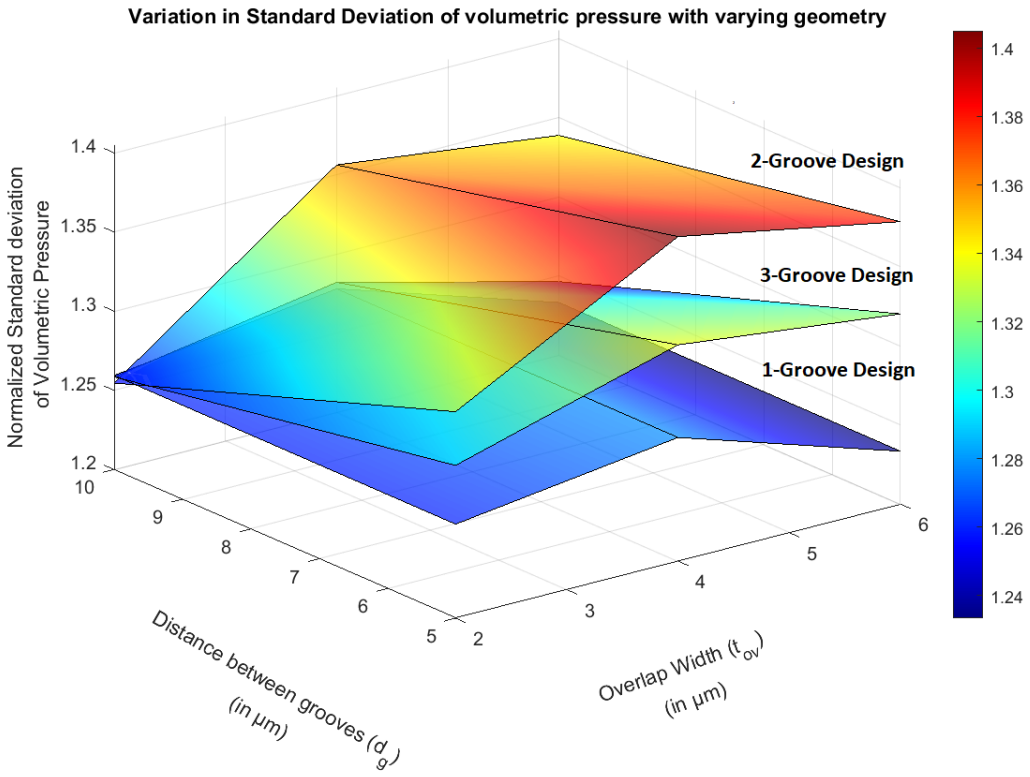


Figure 3-9: Effect of geometry parameters on localized high pressures.

The surface plot indicates that the 2-groove design has the highest standard deviation values, thus having a higher percentage of localized hot spots within the volume of the seal ring, followed by the 3-groove and the 1-groove designs. Moreover, it can be seen that the standard deviation is highest for an overlap width of 4μm for the same number of grooves and the distance between the grooves. Furthermore, the standard deviation for all the designs is approximately the same for an overlap width of 2 μm and the distance between grooves equal to 10 μm, and in general, the values are higher for higher overlap width t_{ov} and lower distance between the grooves d_g.

3-5 Vacuum and Bond Characterization

Following the design and subsequent fabrication, the quality of the created bond must be evaluated. Various bond characterization approaches presented in this section were utilized to study and subsequently draw conclusions regarding the bond formation's quality.

3-5-1 Hermeticity characterization through thin membrane deflection measurement using optical profile measurements

Theoretical Background

This method evaluates the hermeticity of a package by monitoring the pressure-driven deflection of the package cap using an optical interferometer or profilometer [136, 137]. This is the simplest, nondestructive way for testing hermeticity in MEMS devices. After vacuum bonding, the hermetically sealed cavity is exposed to air pressure. If the package is successfully sealed, the membrane will deflect due to the pressure difference between the interior and exterior of the cavity. Figure 3-10 schematically depicts this method.

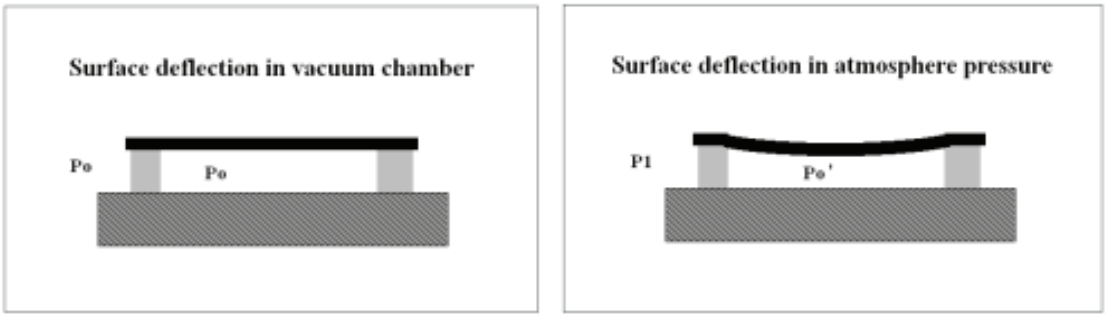


Figure 3-10: The principle of cap-deflection leak test. P_0 equals the pressure in the cavity set by the bonding process parameter, and P_1 is atmospheric pressure[139].

Membrane deflection (δ) is used to determine the pressure difference (ΔP) between the inside and outside of the package. Equation 3-2[139] illustrates the relationship between the membrane deflection (δ) and the pressure difference between inside and outside the cavity (ΔP).

$$\Delta P = \frac{\delta E d^3}{a x^4} \tag{3-2}$$

Where E is the young's modulus of Silicon in [Pa], d is membrane thickness in [μm]; a is the shape constant equal to 0.0138 when the membrane shape is square and x is the membrane length in [μm].

By measuring the change in surface deflection over time, the stability of the hermetic package may be determined using this method. If the package has a fine leak, the deflection will progressively decrease until the internal and external pressures of the cavity are equalized. The deflection in the diaphragm's center is proportional to the differential pressure, and the leak rate L can be calculated using equation 3-3 [7]:

$$L = ln\left(\frac{W_{t1}}{W_{t2}}\right)\left(\frac{VP_0}{t_2 - t_1}\right) \tag{3-3}$$

where W_{t1} and W_{t2} are the maximum deflections at the centre of the diaphragm at times t_1 and t_2 respectively; P_0 is the ambient pressure outside the cavity and V is the volume of the cavity.

Hermeticity evaluation using FEA

To validate the theory developed in the preceding section, a COMSOL simulation was carried out to get maximum deflection vs pressure inside the cavity for the established design.

Simulation setup

To efficiently get results from the simulation and save a lot of computational resources without compromising the accuracy of the solution, some assumptions were applied. These have been listed as under:

- The 3D model is symmetrical, so only a quarter of the structure has been used for the geometrical specifications of the model.
- Similar to the sub-model used in section 3-4-1, the nano-Copper layer is considered to be sintered with no porosity; thus, properties of bulk Copper have been applied.

Furthermore, due to the wide range of dimensions (0.02um - 4000um) of the various parts of the geometry simulated with the model, the COMSOL automatic mesher that generates tetrahedral elements produced a large number of elements for the model that was well beyond the computational capabilities of the workstation. As a result, manual meshing techniques such as boundary meshing and sweep meshing were applied to reduce the model's computational cost even further. The manual meshing allowed for the use of finer elements at the point of interest, i.e., the seal ring, while employing a considerably coarser element size in other sections of the geometry. This resulted in faster computations without sacrificing solution accuracy.Figure 3-11 depicts the geometry utilized in the model.

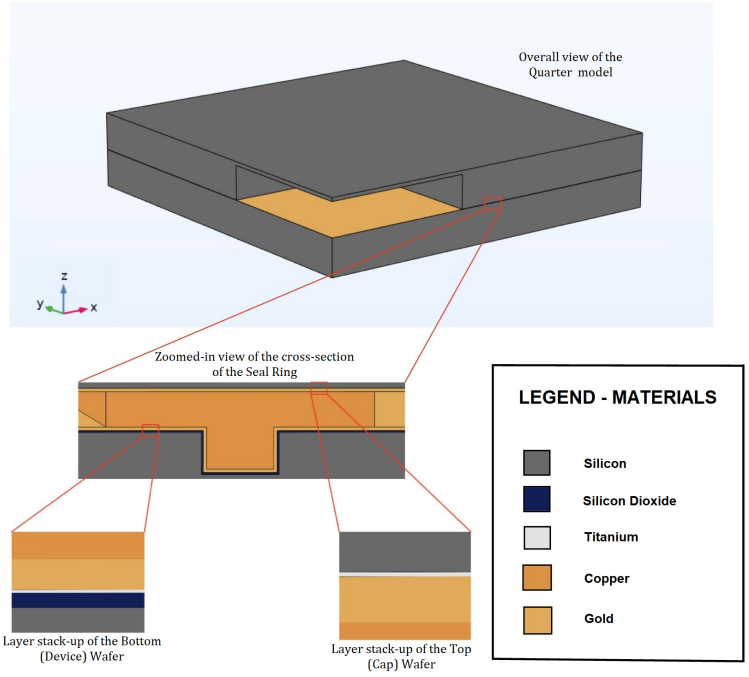


Figure 3-11: . The quarter model of the geometry of the G1-O4 design.

Results

For this study, the solid mechanics module with multiphysics coupling to the heat transfer in solids was used. The exterior boundary of the geometry was kept at a pressure of 1×10^5 Pa to emulate the atmospheric pressure values in accordance with values provided by the local weather stations. A parametric study was run with a membrane thickness of 50 μm with applied pressure ranging from absolute vacuum pressure level (0Pa) to the atmospheric pressure level in Delft over the past three months(100000Pa) followed by the usage of the curve-fitting on the simulation data (figure 3-12).

From figure 3-12, it can be seen that the relationship between the deflection and the internal pressure is linear which is evident from the R-Square value of the curve fitting algorithm being 1 indicating a perfect fit, which is in accordance with the finding from literature.

Moreover, the same pressure values were used to plot deflection vs pressure using equation 3-2 for the sake of comparison with theory. The results from both the simulation and the theoretical model have been illustrated in figure 3-13. Comparing the analytical and simulation model, it can be seen that there is an error in terms of the slope of the graph, with the analytical model having a higher slope, thus leading to higher maximum deflection values (δ) for the same cavity interior pressure (P_{vac}). The reason for this could be the idealized value of the shape constant (a) used for the analytical model. The equations for both the models has been tabulated in table 3-4

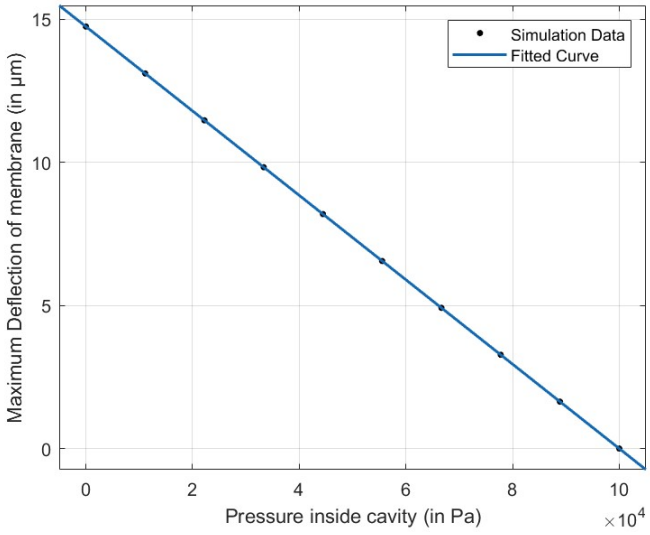


Figure 3-12: Curve fitting of the obtained simulation data

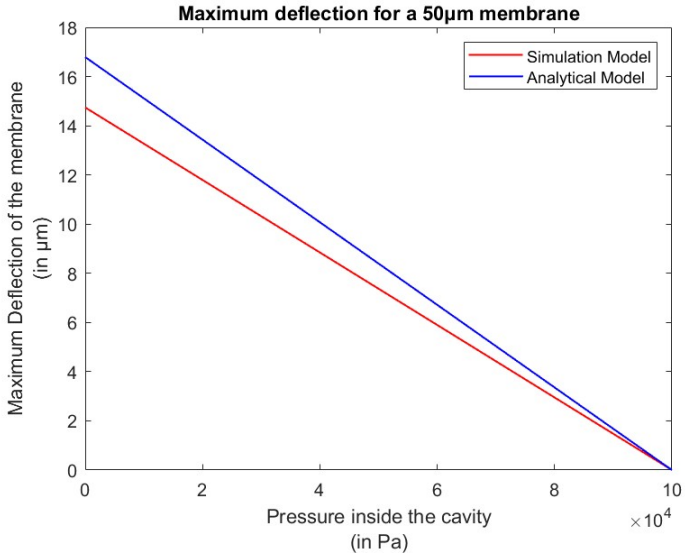
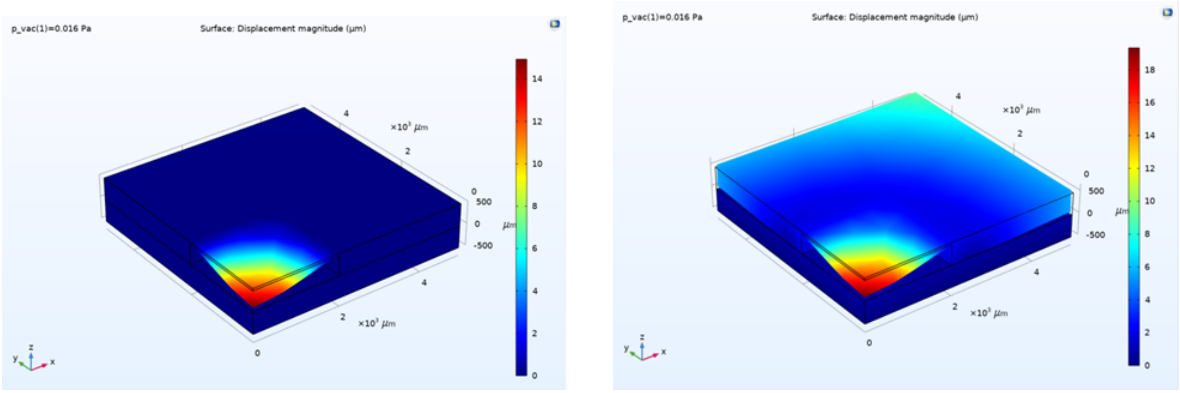


Figure 3-13: Simulation Model vs Analytical model results.

Table 3-4: Equations for relationship between pressure inside vacuum and maximum deflection for a 50 μm membrane.

Model Type	**Equation**
Analytical Model	$\delta = 16.792 - 0.00016792 P_{vac}$
COMSOL Model	$\delta = 14.74 - 0.0001474 P_{vac}$



(a) Without Thermal Stress. **(b)** With Thermal Stress.

Figure 3-14: Solid Displacement plot with a cavity pressure of 0.016 Pa.

The advantage of using the simulation model is that the thermal effect of bonding due to the temperature difference from bonding at 300 °C to room temperature at 20 °C due to CTE mismatch can be easily incorporated into the model. The solid displacement plot of the two cases in COMSOL, as shown in the figure 3-14, clearly shows the difference between the two cases at a pressure of 0.016 Pa inside the cavity. The plot clearly illustrates that when thermal stress is incorporated, warpage effect leads to offset from the no thermal effect case and a higher maximum deflection for the same pressure inside the cavity as depicted in figure 3-15.

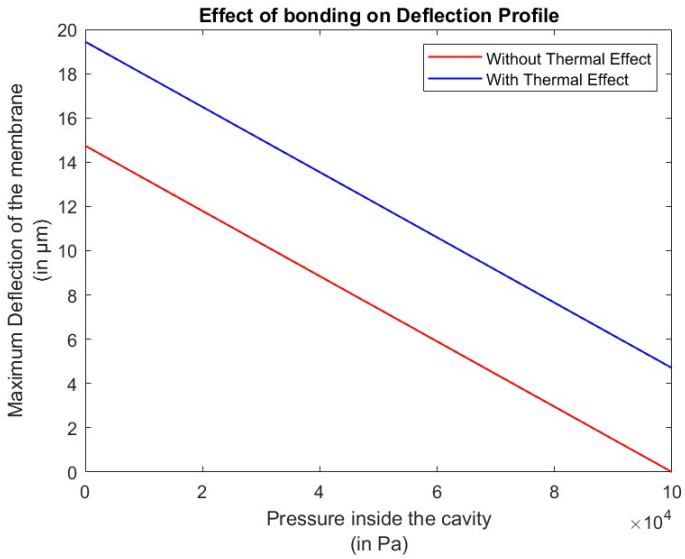


Figure 3-15: Effect of bonding temperature on maximum deflection vs cavity interior pressure.

The simulation result with the thermal effect of bonding incorporated is then curve fitted to a linear fit and the equation obtained can be used to measure pressure inside the cavities for the corresponding membrane thickness(450 μm in this case) as illustrated by equation 3-4

$$\delta = 19.44 - 0.0001474 P_{vac} \tag{3-4}$$

where P_{vac} is the pressure inside the cavity and δ is the maximum deflection of the membrane.

3-5-2 Bond Strength measurement using Die-shear test

Theoretical Background

Shear tests are commonly used for determining the bond strength of structures with die-to-die or die-to-wafer bonds. Fig. 3-16 [3] shows a typical die shear test setup. The top die is in contact with the tool head of the bond tester machine, while the bonded dies are mounted on a clamped metal holder. The load-displacement curve generated by the force the tool head exerts on the top die is recorded by a load cell. The top die must be subjected to a stress parallel to the plane of the die attach substrate; in this instance, the bottom die, in accordance with Mil-Std-883 industry guidelines, as described in [134]. If a die attach substance is present at the die-die contact, this action results in shear stress between:

- the top die-die attach material interface.
- the substrate- die to attach material interface.

The top die separates from the substrate once the maximum shear force is attained. The shear stress (τ) in Eq.3-5 , where F_{shear} is the highest shear force, and A is the contact area between the top die and the substrate, gives the shear bond strength [135].

$$\tau = \frac{F_{shear}}{A} \tag{3-5}$$

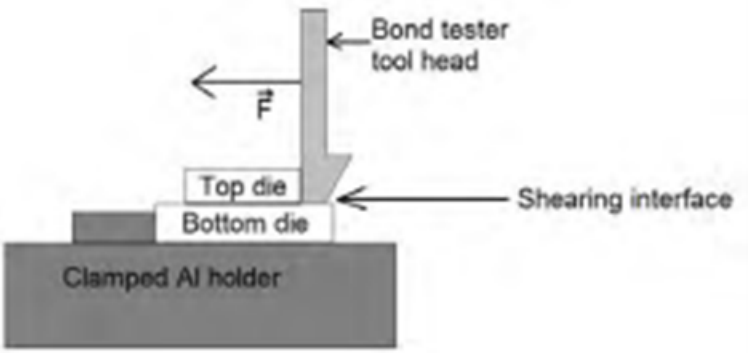


Figure 3-16: Schematic of die shear testing setup [3].

Several crucial factors must be carefully regulated for a valid shear test to be carried out correctly. The tool head must make complete contact with the die edge to apply the shear force uniformly. The substrate holder should be able to revolve to align the toolhead with the die edge. Additionally, the tool head must be parallel to the die attach plane. The tool head cannot be moved vertically after the initial contact between the toolhead and the die. This prevents the toolhead from contacting the substrate, or the die attach material. Following shearing, the mode of separation may be classified into [134]:

- The die shears as a result of a bulk failure, with silicon material still connected to it.
- The die and die attach material is separated.
- The substrate is separated from both the die and the die attach material

3-5-3 Cross-sectional analysis of the bond

Cross-sectional analysis, a destructive characterization technique, can be performed by cleaving the sample at the bonded interface.The cleavage can be done using Focused Ion Beam (FIB) milling. Various studies have imaged bonded interfaces at a sub-micrometer scale using a scanning electron microscope (SEM) and transmission electron microscopy methods. These investigations have contributed to our comprehension of the bonded interface's structure [132]. Several groups have shown the value of this method, especially for viewing "microvoids" that range in size in the order of tens of micrometers [133]. Moreover, the SEM can also be used to do an Energy Dispersive X-Ray Analysis (EDX), referred to as EDS or EDAX, which is an x-ray technique used to identify the elemental composition of materials in the given sample.

3-6 Conclusion

In this chapter, the choice of materials and the geometry of the MEMS cavity to be used were finalized. Moreover, the groove-based design was analyzed through finite element simulations. From the simulations, it was observed that the groove-based design have on average 1.35 times higher standard deviation values of volumetric pressure as compared to a non-groove based design of the same sealing width while the average pressure values remain the same. Thus, it can be concluded that the groove-based designs lead to non-uniform distribution of volumetric

pressure inside the seal ring with high localized pressures in the overlap regions between the grooves and the nano-Cu seal ring in addition to the regions between the grooves.

Moreover, it was found that the standard deviation values and hence localized pressures for different number of grooves were highest for overlap value of 4 μm for the distance between the grooves of 5 μm. However, the standard deviation values are the same for different number of grooves when the distance between the grooves is 10 μm. Furthermore, over the different geometry variations, two groove design has the highest standard deviation values followed by a 3-groove design and finally the 1-groove design.

Furthermore, the bond and vacuum characterization methods that will be used for assessing the quality and hermeticity of the bond formed have also been established within this chapter.

Now, the next phase of this study is the actual fabrication of the proposed designs in this chapter which has been elaborated upon in the next chapter.

Mask Design and Fabrication

4-1 Introduction

In the previous chapters, the design of the structures was finalized with the help of COMSOL simulations along with cues taken from the literature regarding the choice of materials to be used. In this chapter, the process flow for the die level bonding followed by the wafer level bonding will be discussed in detail, starting from the mask design to the definition of the flowchart and processing in the cleanroom.

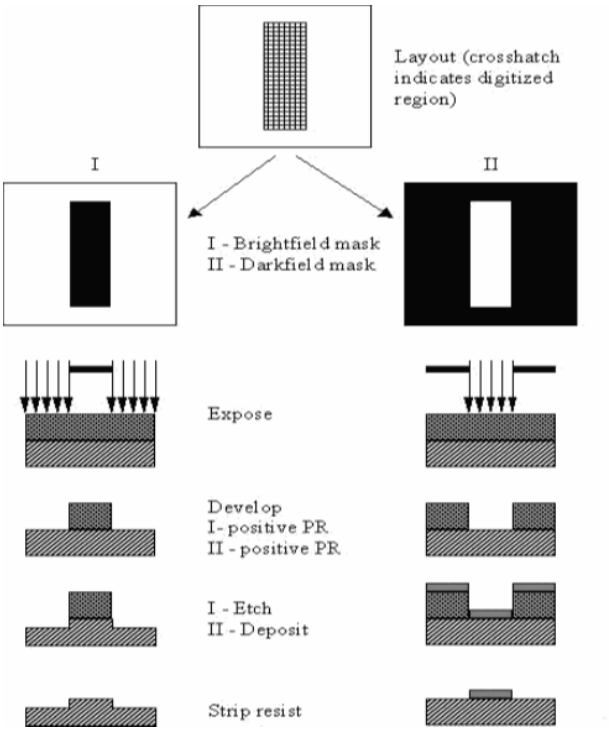


Figure 4-1: Illustration of Brightfield and Darkfield Photomasks on a positive photoresist [57].

4-2 Mask Design

A photomask is a transparent plate with certain opaque sections that generate patterns on the exposed substrate when light is transmitted through it. A photomask is categorized as brightfield or darkfield based on the sort of patterns it contains.

- **Brightfield Mask:** The pattern to be defined in a brightfield mask is opaque. This is depicted in Figure 4.1. When the substrate is exposed to UV light through this mask, all areas other than the pattern to be defined are exposed to the UV radiation.
- **Darkfield Mask:** The pattern to be defined in a darkfield mask is transparent. This is depicted in Figure 4.1. Only the parts that define the pattern are exposed when the substrate is exposed to UV rays through this mask.

However, it is not feasible to form patterns on bare Silicon when exposed to UV light (unless with high density lasers), thus we employ a photosensitive layer that can be deposited on Silicon to make these patterns conceivable. Photoresist is the name given to this photosensitive layer. When exposed to UV light, photoresist undergoes a structural change and becomes either insoluble to a photoresist developer or easily soluble and subsequently removed by a photoresist developer. Positive and negative photoresists are the two kinds of photoresists. This is seen in Figure 4.2.

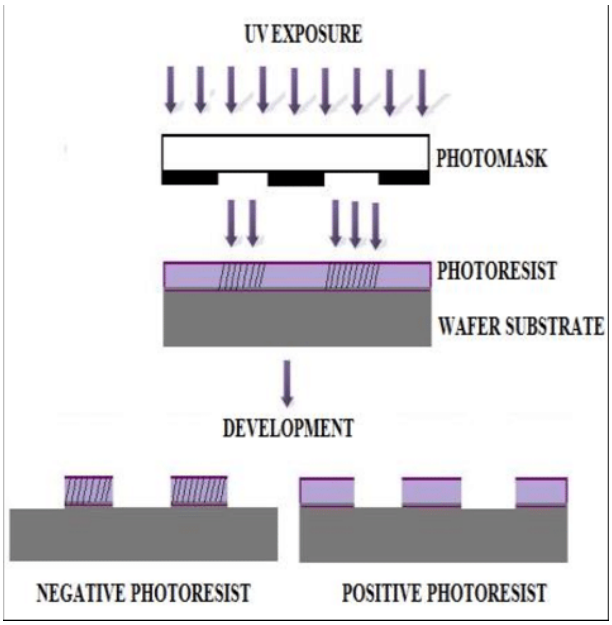


Figure 4-2: Photoresist types when exposed through a brightfield mask[104]

4-2-1 Layers

Patterns on the substrate are defined by the combination of the two different types of masks and photoresists. The patterns can be defined to remove sections of the substrate or to introduce new layers to specified sections of the substrate.

To materialize the devices detailed in previous sections, various processes involving both the addition of new layers and the removal of material in specified regions must be performed. The kind of mask and associated photoresist are determined by the layer type. Bonding experiments were performed in this work initially at the die level and subsequently at the wafer level. Except for two extra masks in the wafer-level bonding process flow, the process steps are nearly identical in both situations. Looking at our MEMS cavity construction, the layers and the corresponding masks can be defined as follows:

Top Wafer (Front Side)

- **MASK 1 - CAVITY ETCH:** This is a darkfield mask and is used to form windows in the photoresist/SiO2 for the deep reactive ion etching (DRIE) of the cavities into the silicon. This mask consists of a square (figure 4-3) which is replicated for all the dies.

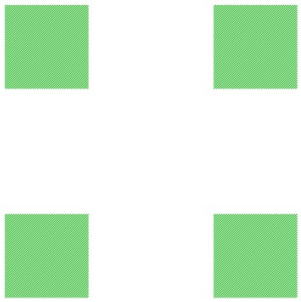


Figure 4-3: Cavity etch square for forming windows in the masking material.

Top Wafer (Back Side)

- **MASK 2 - Die Labels and Dicing Marks:** This darkfield mask is the only mask intended for the back side of the top die and is used to imprint dicing marks and die labels on the back side of the top wafer.

Figure 4-4: Mask for die labels and dicing marks on the back side of the top wafer.

Bottom Wafer (Front Side)

- **MASK 3 - GROOVES:** This mask is a darkfield mask and is deployed to etch grooves into the Silicon Bottom Wafer. Fifteen Designs as formulated in the previous chapter were spread across the mask. The figure 4-5 shows the die consisting of the G2O4D5 design.

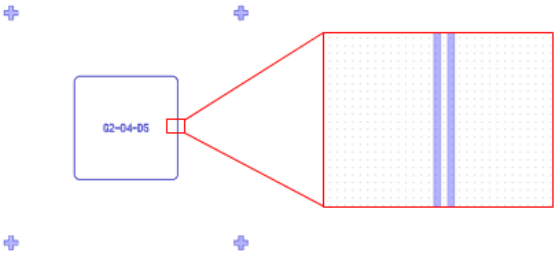


Figure 4-5: Mask for etching of grooves.

- **MASK 4 - SEAL RING:** This is a brightfield mask and is the final mask that is used for the bottom wafer. This mask also consists of the fifteen different designs with different dimensions spread out around the wafer in the same order as in the GROOVES mask.

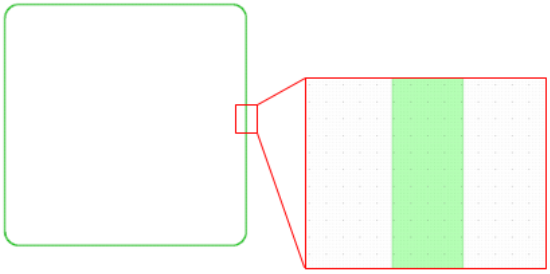


Figure 4-6: Mask for patterning of PR Stencil

4-3 Process Flow

A die level process as summarized in figure 4-7 was carried out. This was done to avoid inconsistencies in the uniformity of the dispensed nano-Copper paste on the patterned substrate caused by the larger area required with wafer-level packing. Furthermore, by employing the die level technique, a large number of samples may be examined with minimal resource wastage. Moreover, due to the constraint on the upper limit of the force (12000N) that could be applied using the AML bonder, the pressures required for the densification of the NP's while sintering could not be reached. Therefore, a die level process was employed for this given study.

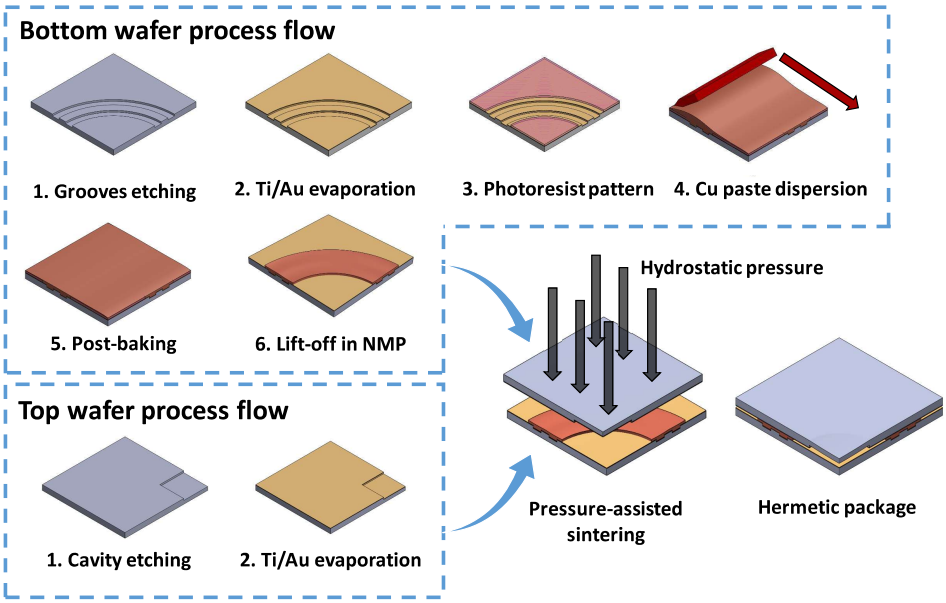


Figure 4-7: Summary of the fabrication process flow.

BOTTOM WAFER

Step 1: Creation of zero layer with FWAM Alignment Markers

Figure 4-8: Etching of alignment markers

We begin with 4-inch dual-side single-side polished p-type doped Si wafers. The first step is to inscribe alignment markers on the wafers. This process entails the lithographic process of PR application, FWAM Mask exposure and development followed by plasma etching of 120nm deep alignment marks into the Si wafer. These marks facilitate the alignment of the mask's various layers to the wafers. Finally, the PR is removed using a plasma strip, followed by a cleaning cycle.

Step 2: Etching of Grooves

The next step is the etching of the grooves in the silicon wafer. This was accomplished by coating the wafer with a 3.1 µm Co-3027 positive PR, followed by a 420 mJ/cm2 exposure via the mask GROOVES utilizing a SUSS MA8 manual aligner. This is followed by a single puddle development and etching with the plasma etcher. To accurately estimate the time necessary to etch the appropriate depth of silicon, the default plasma etcher recipe was tested on a test wafer for various etching times. Table 4-1 tabulates the etch depth vs. etch time data acquired from test fabrication on test wafers.

Figure 4-9: Etching of 2500nm Grooves.

Table 4-1: Plasma Etcher etching rate.

Etch Time (mm:ss)	**Depth of Silicon etched (nm)**
00:40	120
02:00	225
04:13	400
10:00	808

This data was fit to a linear curve revealing the relationship between Etch rate and etch time as :

$$t_E = \frac{d_E - 82.667}{1.20889} \tag{4-1}$$

Where d_E is the etched depth in nanometers (nm) and t_E is the etch duration in seconds (s). According to the design, the groove depth should be 2500nm. When this is substituted into the equation, the time required to etch 2.5 um is 33 minutes and 20 seconds. The plasma etcher was employed for the calculated etch time, and the actual depth of the grooves after etching was measured using a Keyence profilometer, revealing a 2.6 µm depth of Si etched. This has been illustrated in figure 4-10.

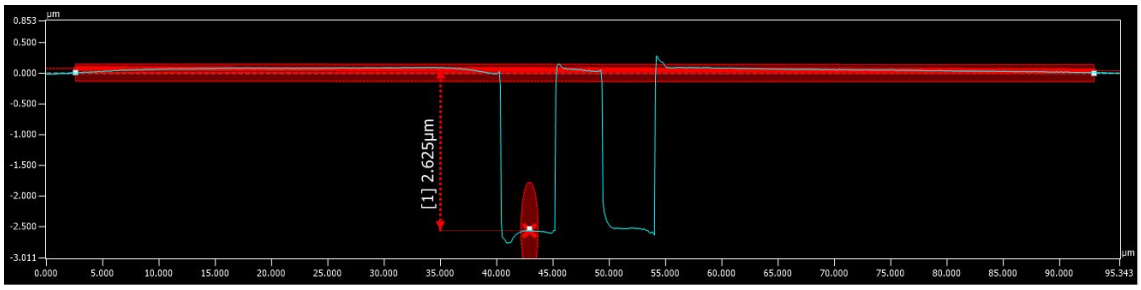


Figure 4-10: Substrate profile after the plasma etch.

The etching was followed by the plasma strip of the PR and finally a cleaning step.

Step 3: Thermal Oxidation of Silicon

The wafers are then wet oxidized, and approximately 100 nm of oxide is grown on the wafer. The Deal & Grove model [64] was used to compute the needed wet oxidation time, which was determined to be 10 minutes and 4 seconds. For this procedure, the recipe WET1000 was utilized, and the specifics of this process step are summarized in Table 4-2. Figure depicts

Table 4-2: Summary of the Wet Oxidation Process

Process	Temperature (in °C)	Gases & Flows (in liter/min)	Time (in min:sec)	Remarks
boat in	600	nitrogen: 6.0	05:00	
stabilize	600	nitrogen: 6.0	10:00	
anneal	600	nitrogen: 6.0	15:00	
heat up	+10°C/min	nitrogen: 3.0 oxygen: 0.3	40:00	
stabilize	1000	nitrogen: 3.0 oxygen: 0.3	02:00	
oxidation	1000	oxygen: 2.25 hydrogen: 3.85	10:04	Target 100nm oxide thickness
cool down	-7°C/min	oxygen: 2.25 hydrogen: 3.85	05:00	
boat in	600	nitrogen: 3.0	05:00	

the state of the wafer following this fabrication step. Furthermore, the layer thickness was measured using the Woollam Ellipsometer, and the average measured thickness of the oxide was 100.65 nm with a standard deviation of 1.0281nm.

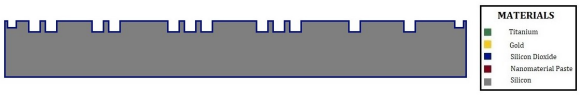


Figure 4-11: 100nm oxide growth by wet oxidation.

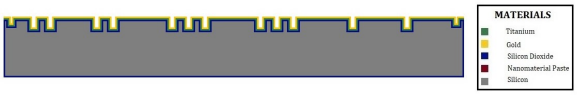
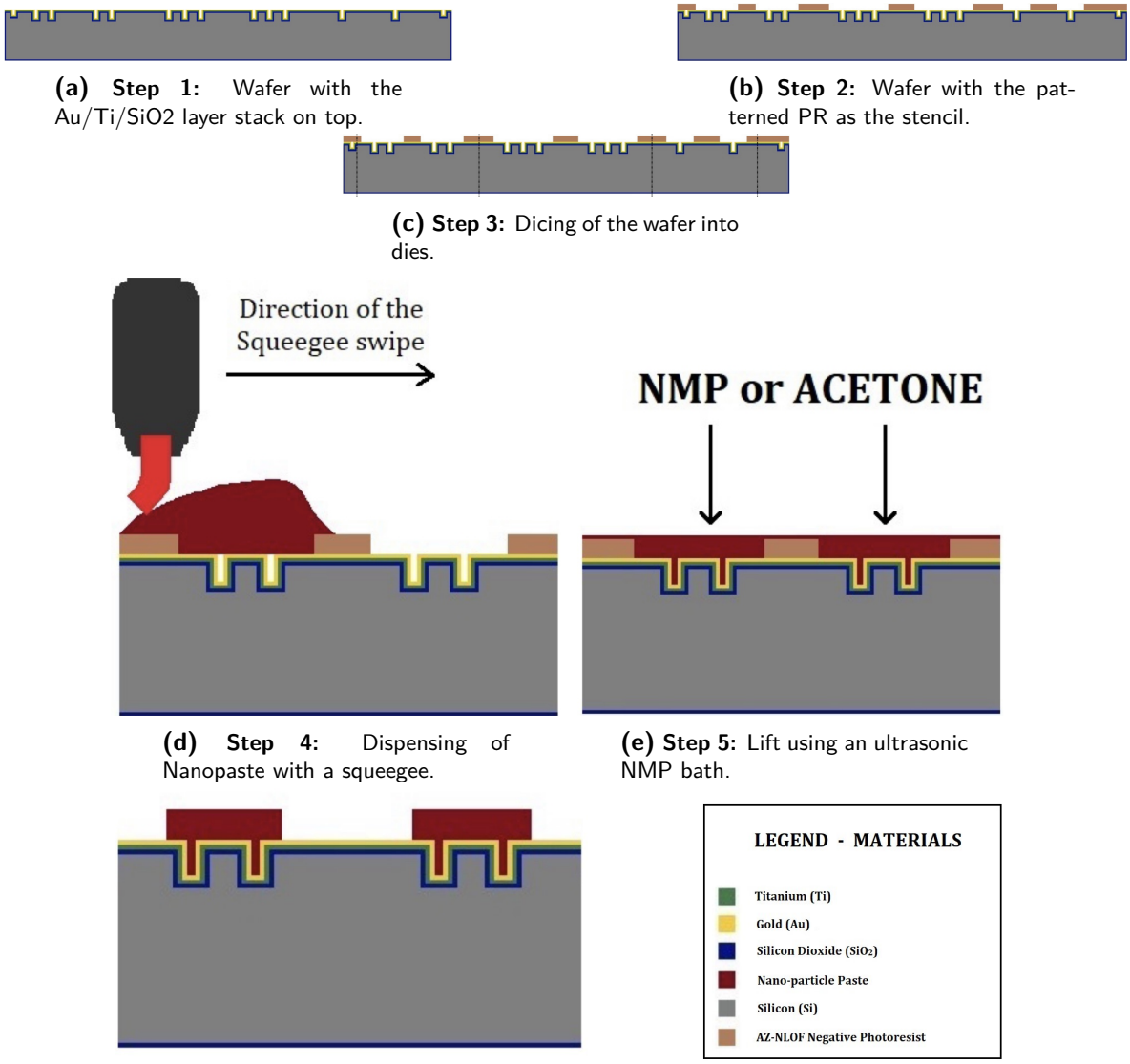


Figure 4-12: Physical vapor deposition of Au/Ti bi-layer using the CHA Solutions evaporator.

Step 4: Metallization

Following oxidation, a metallization process involving the deposition of 20nm/200nm Ti/Au bi-layer was done using the CHA Solutions physical vapor evaporator in CR10000. Furthermore, the actual measured Au layer and Ti layer thicknesses were 200.3 nm and 22 nm as per the readings from the equipment.



(a) Step 1: Wafer with the Au/Ti/SiO2 layer stack on top.

(b) Step 2: Wafer with the patterned PR as the stencil.

(c) Step 3: Dicing of the wafer into dies.

(d) Step 4: Dispensing of Nanopaste with a squeegee.

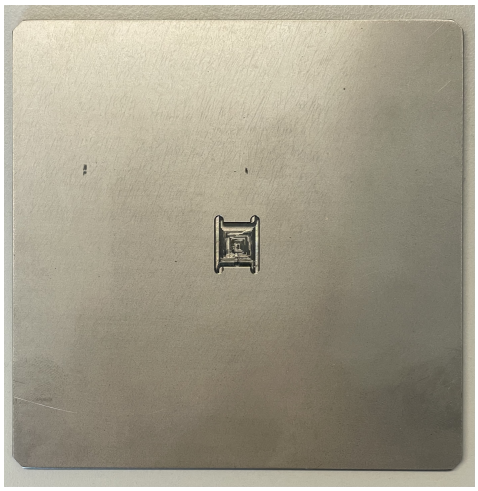
(e) Step 5: Lift using an ultrasonic NMP bath.

(f) Step 6: Wafer with patterned nanopaste.

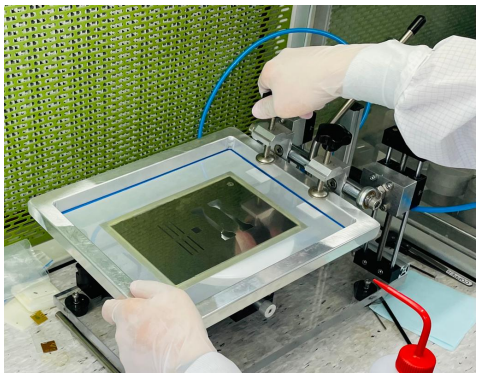
Figure 4-13: Schematic illustration of photolithographically defined stencil based nano-paste screen printing.

Step 5: Screen Printing of Nanoparticles

Screen printing is a prominent technique for printed electronics and solar cell metallization. The method is based on pattern transfer from a stencil to the substrate. To squeeze the ink/paste into the stencil openings, a squeegee with a fill blade is swept across the stencil while applying a certain pressure. The stencil is mechanically removed, leaving the patterned paste on the substrate. This method's resolution is mostly constrained by the stencil size, the particle size of the paste and its composition.



(a) Tool for holding the 10 x 10 mm dies in place..



(b) Setup for other die sizes with a vacuum chuck.

Figure 4-14: Image of the setups used for nano-particle stencil printing for various die sizes.

In this study, a photolithographically patterned photoresist is employed as a stencil for nanoparticle screen printing. This process has been diagramatically illustrated in figure for the die-level bonding process. For pattern transfer, the wafers were coated with a layer of AZ NLOF negative PR with a subsequent exposure using the SEAL RING mask followed by a single puddle development process. For the bonding experiments, the wafers with the patterned resist were diced into dies of varying sizes (10mm $\times$ 10mm, 20mm $\times$ 20mm, 10mm $\times$ 20mm) and a setup as described in fig 4-14 was used to hold the die in place for the screen printing process. This was followed by screen printing of the nanopaste using a squeegee blade (figure 4-15). This was followed by the baking of the die at 80°C for five minutes to evaporate the organic solvent of the nano-paste with the subsequent lift-off.

The surface condition of the die with the patterned seal ring on top is very important for the hermeticity of package. This entails ensuring a fairly uniform profile of the dispensed nano-paste with minimal residue on the surface as it may cause uneven pressure leading to non-uniform densification which can prove detrimental in ensuring the hermeticity of the sealed cavity. To ensure such conditions, the whole process of stencil printing needs to be carefully optimized. Screen printing conditions like the amount of pressure used while swiping the squeegee blade, and lift-off parameters like chemicals use, temperature, bath time and presence/absence of temperature were varied to optimize the liftoff process and facilitate a good quality of patterning of the nano-paste on the die.

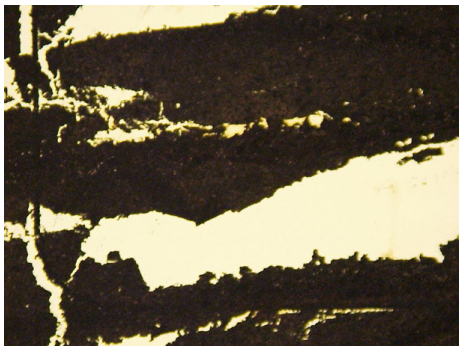


Figure 4-16: Liftoff at room temperature in a 120s Acetone bath.

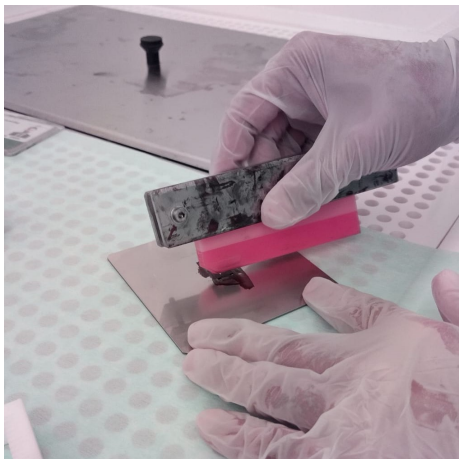


Figure 4-15: Screen printng process.

4-3-1 Optimization of the lift-off process of Nano-paste.

The nano-paste, being a viscous material required very specific lift-off parameters in order to ensure a good quality patterning of the nano-paste on the die. To accomplish this, a lift optimization experiment was carried by varying lift-off parameters like temperature, presence/absence of ultrasonic agitation, bath time and the solvent used. The results were observed via an imaging and profilometric analysis of the dies using the Keyence VK250 profilometer after the lift-off process. The whole optimization experiment has been summarized in table 4-3 and a detailed imaging analysis has been provided in Appendix B.

Initially,with a 2 μm thick patterned resist on top, the standard lift-off process was used by submerging the dies with dispensed nano-copper paste on top in Acetone with no agitation for 120s. This however led to the photoresist not being lifted-off from multiple places as seen in figure 4-16. After this, keeping solvent the same, the temperature and ultrasonic bath time was varied with the final parameters being acetone bath for 30 seconds in total at 35 °C with 10 seconds of ultrasonic agitation for the first 10 seconds of the bath.The ultrasonic agitation allows the infiltration of NMP through the nanoparticle paste to the photoresist to enable its dissolution.

Table 4-3: Summary of Lift-Off Optimization.

Solvent	**Temperature in °C**	**Total Bath Time (s)**	**Ultrasonic time (s)**	**Remarks**
Acetone	20	60	0	PR from majority of the die area not removed.
Acetone	25	40	40	Removal of the nano-paste from the pattern in a lot of places.
Acetone	25	30	30	Portions of the patterned ring removed but the percentage area is much lesser.
Acetone	25	10	10	The patterned nano-paste is intact. However, some PR residue left at some places.
Acetone	35	30	10	A very good pattern but nano-paste residue left on the die with very tiny portions of the seal coming off.
NMP	25	15	15	Complete removal of PR and nano-paste seal as well.
NMP	25	10	10	Partial removal of nano-paste seal at several regions.
NMP	50	120	0	Some PR residue still left behind at some places.
NMP	80	60	0	Very good patterning, but tiny residual nano-paste particles left.
NMP (Sample Tilted downwards)	80	60	0	Excellent ptterning with no or minimal residue left.

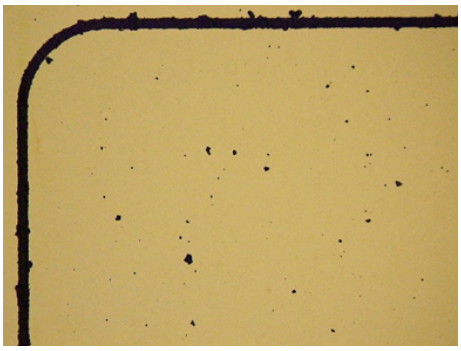


Figure 4-17: Liftoff at 35°C temperature in a 30s Acetone bath with 10 seconds of agitation.

As can be seen from the figure 4-17, a well defined seal ring was obtained. However there are still some residues of the nano-particle paste elsewhere on the wafer. Furthermore, on closer inspection, it can be seen that some parts of the seal ring have also come off (figure 4-18). This can be attributed to the brittle nature of the nano-paste in addition to its weak adhesion to the substrate which resulted in the mechanical agitation being too aggressive for the weakly adhered nano-paste. The same problem was noted with NMP as the solvent when using agitation as paste began coming off from seal (figure 4-19).

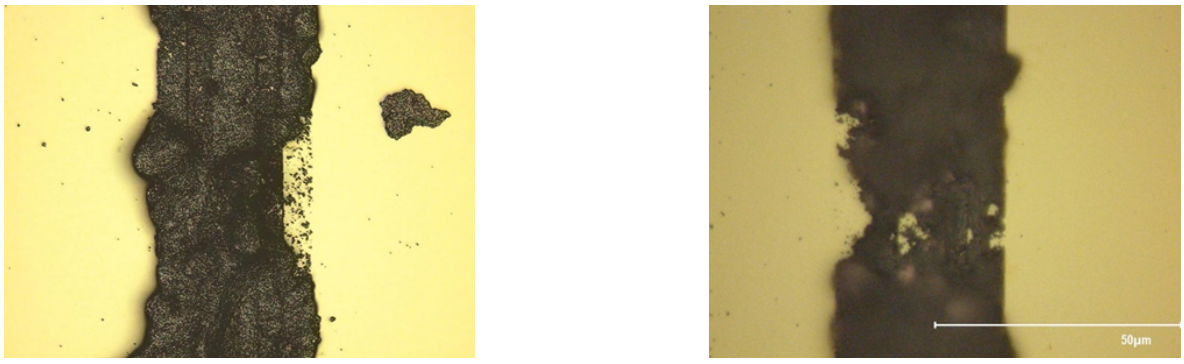
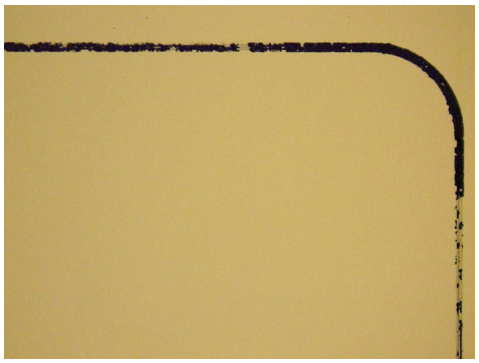
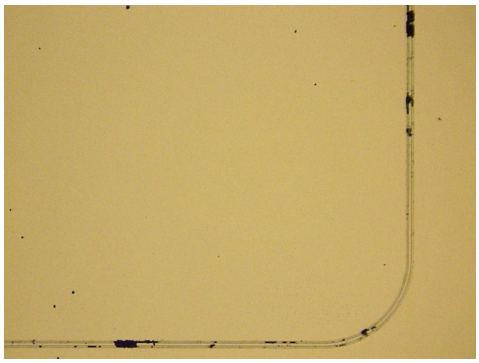


Figure 4-18: Portions of the Nano-Paste seal coming off after using agitation in an Acetone bath.



(a) Liftoff at 25°C temperature in a 60s NMP bath with 10 seconds of agitation.



(b) Liftoff at 25°C temperature in a 60s NMP bath with 15 seconds of agitation.

Figure 4-19: Portions of the Nano-Paste seal coming off after using agitation in an NMP bath.

To mitigate this, it was decided to remove the mechanical agitation and only use the non-mechanical chemical method to lift-off the photoresist. To compensate for the lack of agitation, it was decided to increase the temperature of the bath to increase the solubility rate of the photoresist in the solvent. However, due to the high vapour pressure of Acetone leading higher evaporation rates at higher temperatures; NMP, which has a lower vapour pressure and thus suitable for higher temperature was decided to be used as a solvent for higher temperatures [144]. The lift-off process was then optimized as summarized in table 4-3 and the final conditions were decided as 60 second NMP bath with no agitation at 80°C. Imaging analysis as presented in figure 4-20 show similar results as the optimized Acetone bath with ultrasonic agitation (figure 4-17). However, just like in the case of Acetone, there is still some residue on other parts of the die with the NMP.

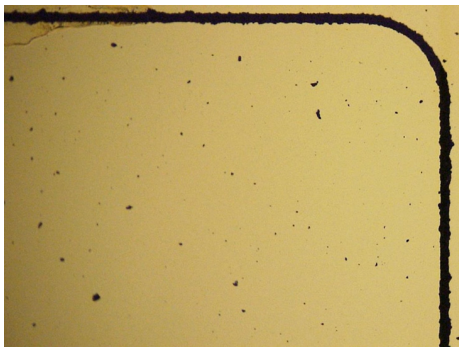
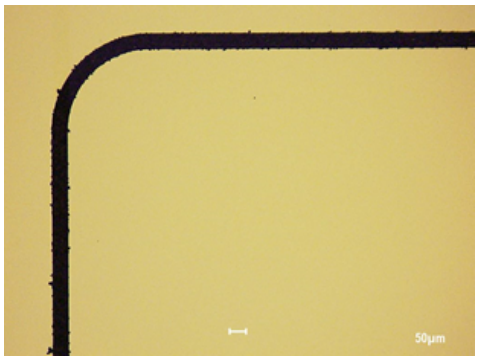
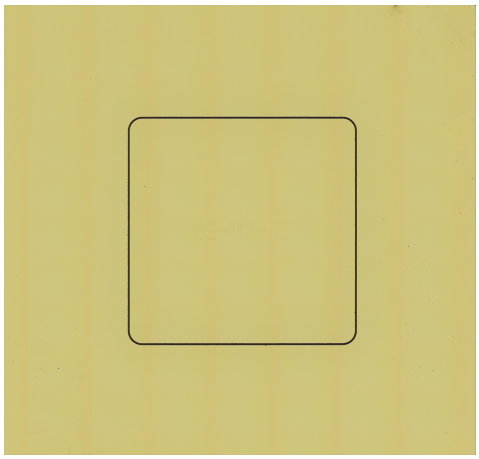


Figure 4-20: Liftoff at 80°C temperature in a 60s Acetone bath with no agitation.

Redeposition of the nano-paste was theorized to be the cause of this residue and so, the sample was tilted downwards with the side with the resist facing the bottom of the beaker during the bath, and a very pristine die with well patterned ring and minimal residue was obtained (figure 4-21).



(a) Zoomed-in View of the ring.

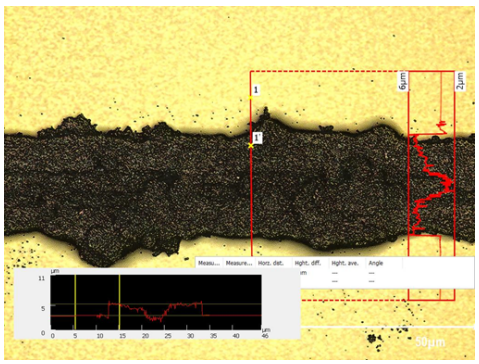


(b) Full view of the patterned die with optimized lift-off process.

Figure 4-21: Liftoff at 80°C temperature in a 60s Acetone bath with no agitation and sample tilted downwards.

4-3-2 Effect of Post screen-printing Baking

After the post screen baking for 5 minutes at 80 °C to evaporate the organic solvents, the volume of the patterned nano-paste also decreases leading to a decrease in the height of the patterned nano-paste. Due to there being more nano-paste in the groove region as compared to the other regions, the volumetric loss is more on top of the grooves leading to the formation of deppressions in the profile of nano-paste at the top of the groove region. This has been illustrated in figure4-22.



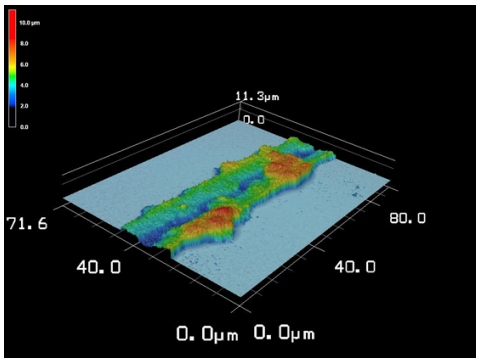


Figure 4-22: Depression in the groove part of the nano-paste seal after post-stencil printing bake and subsequent lift-off.

It can be seen that the depression is around 2 μm which is the height of photoresist. This region may create more voids as the level of the nano-paste is below the surface level of the die.

4-3-3 Height Variability of patterned paste due to pressure variability of swiping.

Another feature that was found to influence the profile of the nano-paste was the pressure applied on the squeegee blade while swiping and dispensing the nano-paste with the patterned photoresist on top. It was found that light swiping with minimal applied pressure (no squeegee blade deformation) led to excess nanopaste leading to height of the patterned nano-paste that was higher than the intended 2^{μ}m. Moreover, as can be seen from the figure within the same section, we have a big variability in height within the same section of the seal ring (figure4-23).

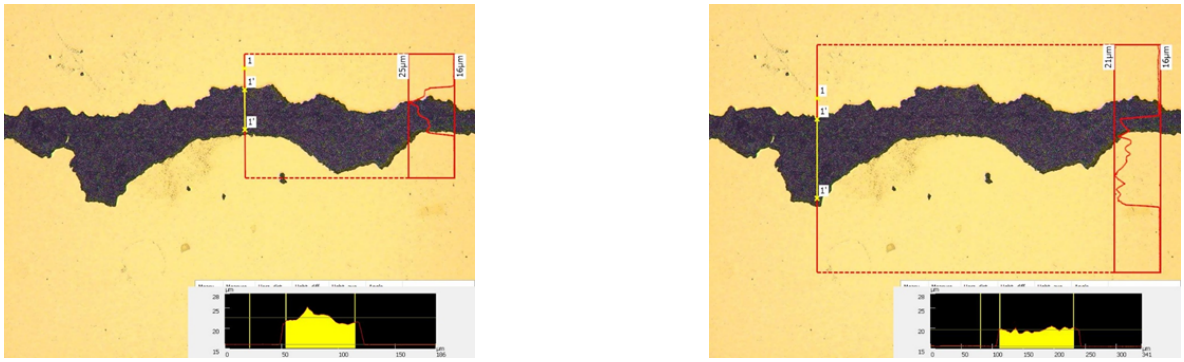


Figure 4-23: Height variability in height of patterned nanopaste in the same section.

On the other extreme, when a high pressure which in this context translates to the deformation of the squeegee blade while swiping, was applied, some parts were taken off due to roughness of the squeegee blade edge or the particles on it. This can be seen in figure 4-24 where the paste has been taken off with the direction of swiping leading to the formation of a void in the middle and the gold surface exposed.

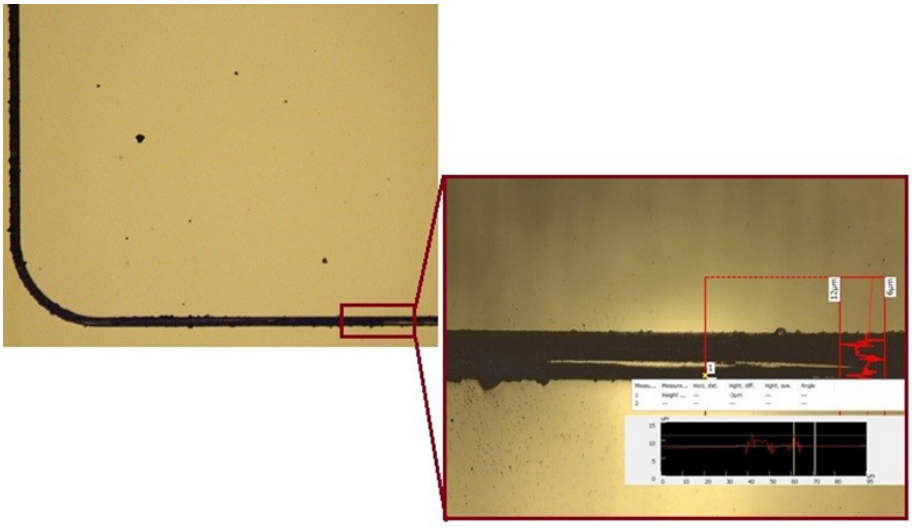
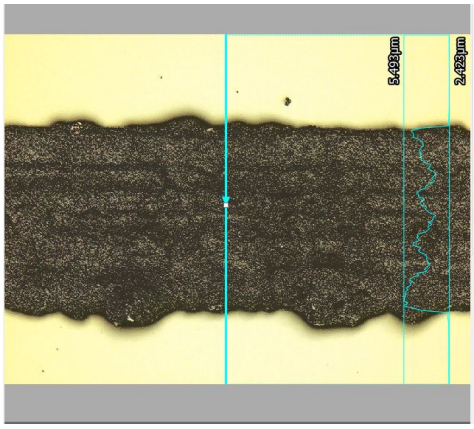


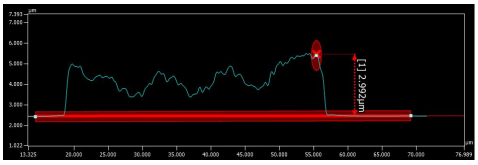
Figure 4-24: Effect of application of higher pressure while swiping.

To mitigate the effect of baking time, a 3.5 μm resist was decided to be employed. On the other hand, for the height variability, a two step manual swiping process was employed,

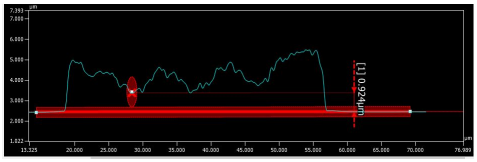
wherein, the nanopaste was swiped with a high pressure first to fill up the grooves completely and remove excess paste on top of the resist followed by light swiping to fill up the seal ring and form a very thin layer on top of the die.The application of these enhancements resulted in an improvement in the overall profile and height uniformity of the patterned seal, with the maximum and minimum heights being 2.992μm and 0.924 μm, respectively, and the average and standard deviation values being 1.91μm and 0.51μm, respectively. height equal These improvements have been illustrated in figure 4-25.



(a) Profile and image of the dispensed seal after improvements in swiping and increase in PR thickness.



(b) Improvement in the patterning and profile of the dispensed nano-paste seal ring.



(c) Improvement in the patterning and profile of the dispensed nano-paste seal ring.

Figure 4-25: Profilometric analysis of the improvement in the patterning and profile of the dispensed nano-paste seal ring.

From the figure, it can be observed that the depressions on top of the groove layers are still there. however the level of the nano-paste is still above the surface level of the bottom die. Furthermore, a much more uniform deposition can also be observed after employing the two step squeegee swiping process.

Even with all the optimization, all samples were visually inspected through a microscope before deploying them for various bonding experiments to make the surface conditions for various bonding experiments as consistent as possible.

TOP WAFER

Step 1: Creation of zero layer with FWAM (Frontside)

Six 4-inch double side polished p-type doped wafers are used. Just like the bottom wafer,

the processing for this also begins with the coating of the wafer with 1.4um PR followed by exposure through the COMURK MASK using job litho/zefwamFTBA with the wafer stepper with the subsequent development step. Finally 120nm urks are etched into the Si using the plasma etcher followed by a plasma PR strip and cleaning.

Figure 4-26: Back-side zero layer creation.

Step 2 : Creation of zero layer with FWAM (Backside)
The processing of the back side of the six wafers processed in the previous step also proceeds with the inscribing of full wafer alignment markers (FWAM) aligned to the front side alignment markers using the same steps as described in the previous section. Figure 4-27 illustrates the state of the wafer after this step.

Figure 4-27: Back-side zero layer creation aligned to the front side.

Step 3 : Inscribing of die labels and dicing marks (Backside)
The zero layer processing of the backside is succeeded by photo-lithographic steps as done in the previous step, but the mask used in this step is the DICING MARKS and exposure is done using the Suss MA8 manual aligner. This has been illustrated in the fig 4-28.This concludes the processing of the back side of the top wafer.

Figure 4-28: Back-side Dicing marks and Die label etching.

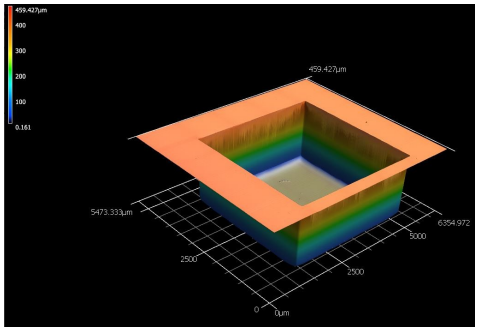
Step 4: Cavity Formation
To form the cavity, deep reactive ion etching was employed to etch away 450um of Silicon. To etch away such large depths an SiO2 hard mask of 5um thickness was used. A 5um PECVD oxide was deposited using the Novellus Concept One PECVD reactor , followed by application of 3.1 um PR. This was followed up by exposure through the mask CAVITY ETCH followed by dry etching of the oxide using the Drytek Triode 384T.

(a) Patterned PECVD oxide used as hardmask for cavity openings.

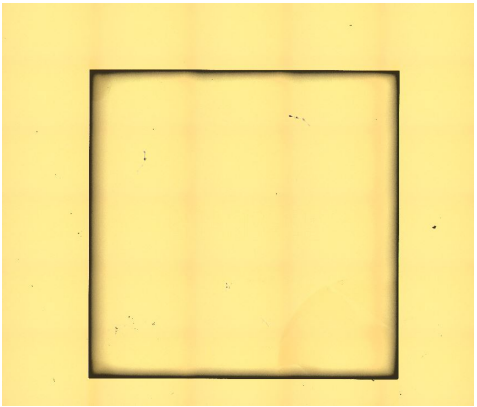
(b) State of wafer after DRIE and removal of PECVD oxide.

Figure 4-29: Cavity Formation in the top wafer.

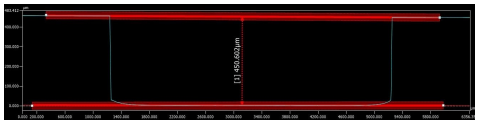
Subsequently, deep reactive ion etching was done for the formation of the cavity in the wafer with the Rapier DRIE tool followed by the removal of oxide layer using a BHF 1:7 bath. The deep reactive ion etching step was done in two steps. Two hundred loops were used in the first step to figure out the etch rate of the recipe. The etch rate was computed to be 0.73 μm per loop. Therefore, 415 additional loops were used and profile as illustrated in figure 4-29 was obtained.



(a) 3D profile image of the deep reactive ion etched cavity.



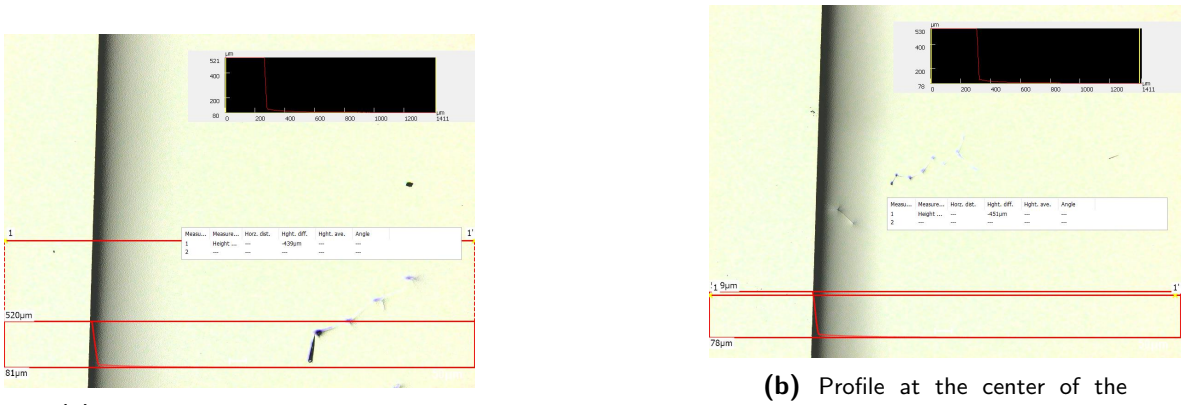
(b) Optical image of the DRIE etched cavity.



(c) Profile data of the cavity.

Figure 4-30: Deep Reactive ion etching for Cavity Formation.

As can be seen from figure 4-30, the edges do not have a sharp transition. Instead, the edges of the cavity are smoother at the depth of the cavity.



(a) Profile at the edge of the wafer.

(b) Profile at the center of the wafer.

Figure 4-31: Variability in the etched depth.

Moreover, variability in the depth of the etched Silicon can be observed. This has been illustrated from the profilometer images in figure 4-31, wherein the depth of the cavity is around 451μm at the center and around 439μm at the edge of the wafer. Moreover, with the wafer processed at a later point in time for the preparation of the final samples, the cavity depth variation was observed with the central part having a cavity depth of 434.54 μm and 424.4 μm at the same edge location measured for the older wafer. These variations need to be taken into account later while performing the hermeticity evaluation of the bonded structures using the cap deflection method as described in section 3-5-1. Therefore, the profile of all the cavities on the wafer used for fabrication of final samples was measured using the Dektak 150 Surface Profilometer to gauge the absolute pressure inside the sealed cavities as accurately as possible. (Figure 4-32).

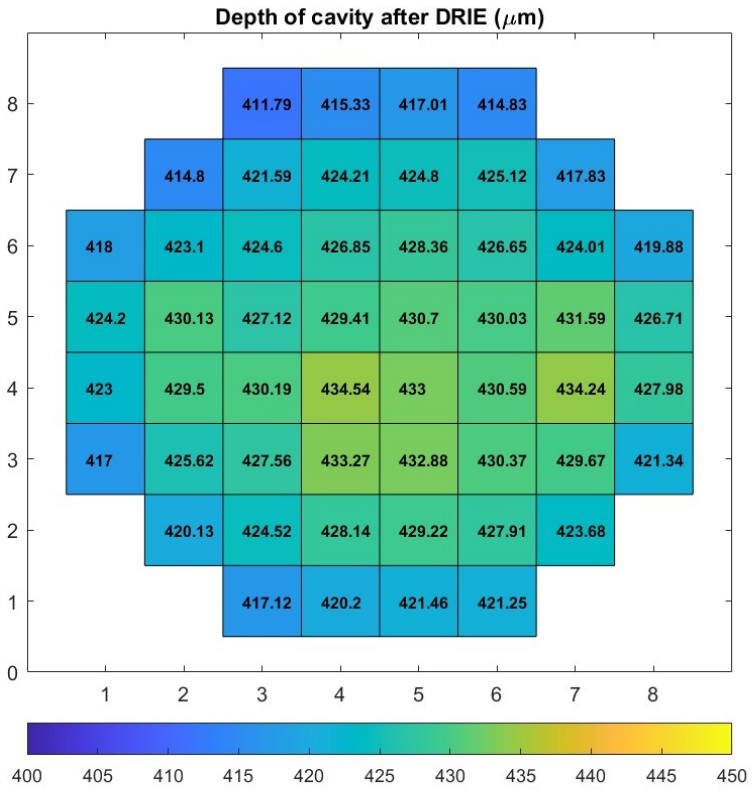


Figure 4-32: Measurement of depth of all cavities on the wafer.

Step 5: Metallization

The metallization process as described in Step 4 of the bottom wafer process flow is employed which culminates in the deposition of 20nm/200nm Ti/Au bi-layer.

Figure 4-33: Physical Vapor deposition of Au/Ti bi-layer.

Step 6: Wafer Dicing

The wafer is then diced into die sizes of 10mm ×10mm and 20mm ×20mm for the bonding experiments to be carried out. For the dicing, the dicing tool disco DAD 321 with was used to dice the wafers using the dicing marks on the back side of the top wafer.

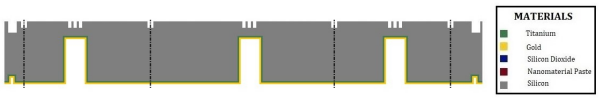


Figure 4-34: Dicing of the top wafer using a mechanical dicing tool.

4-3-4 Die-Die Bonding

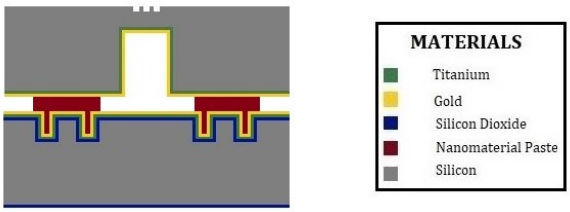


Figure 4-35: Die to die bonding experiment.

Following the fabrication of the top and the bottom wafer, the bonding of the dies was done. A bonding experiment with varying bonding with different platen temperatures was carried out. The bonding was performed using an AML-AWB-04 aligner wafer bonder machine. The top dies were manually aligned to the bottom dies and then placed between two platens inside the wafer bonder. The bonding chamber was pumped down to a UHV pressure of 10^{-6} mbar. The bonding process starts with pumping down the bonding chamber to a UHV followed by a temperature ramp to the set temperature. Once, the temperature reaches its set point, the set force is applied along with formic gas being introduced into the chamber to reduce any copper oxide that might have formed on the surfaces. This is done for 10 minutes with the pressure inside the chamber being 1 mbar for this time duration. After this phase, the formic gas inlet is switched off and the pressure goes back to the UHV conditions of $\leq 10^{-4}$ mbar and the force is kept on for another 20 minutes to let the copper nanostructures densify. Finally, at the 20-minute mark, the force is switched off and the sample is allowed to cool down under passive cooling till the temperature is below 100°C to avoid oxidation of the fused copper at the elevated temperatures. Following this, the various aspects of bonding like, bond strength, hermeticity, and reliability were analyzed, which have been elaborated upon in the next chapter.

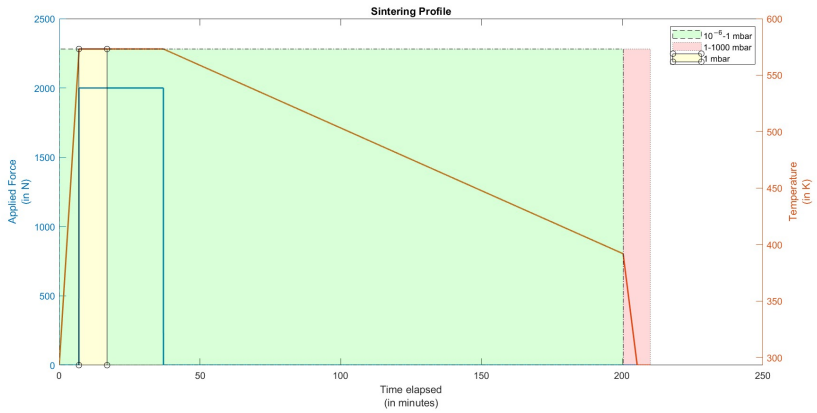


Figure 4-36: Sintering profile while die bonding.

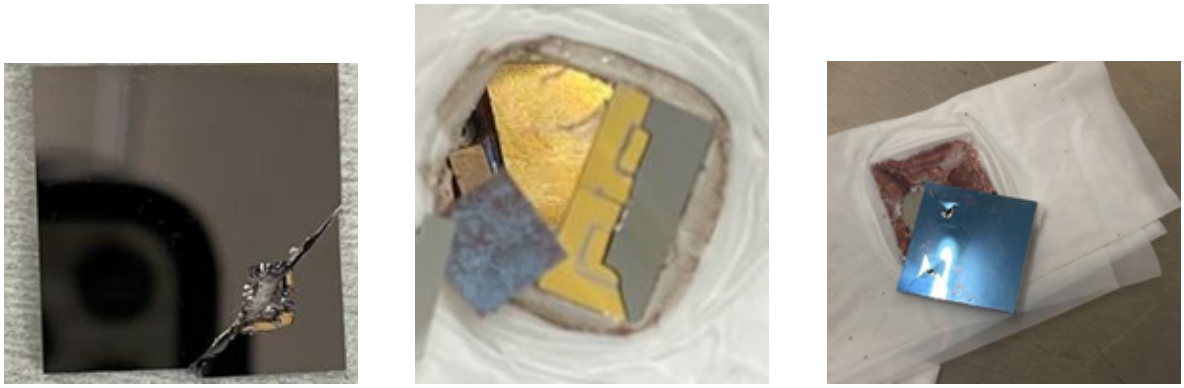


Figure 4-37: Breaking of dies during bonding.

During the initial bonding experiments, several dies were found to be broken, as illustrated in figure 4-37. This problem was attributed to the presence of nano-Cu residues left on the backside of the bottom die, residues on the platen of the bonder and a problem with the leveling of the top chuck, leading to uneven pressures across the die, thereby causing higher stress in certain regions of the dies to be bonded.

Also, because die bonding was done manually, there was a misalignment between the top die and the bottom die. This was especially caused by the sliding of the dies when they were put into contact manually before the bonding experiments (figure 4-38).

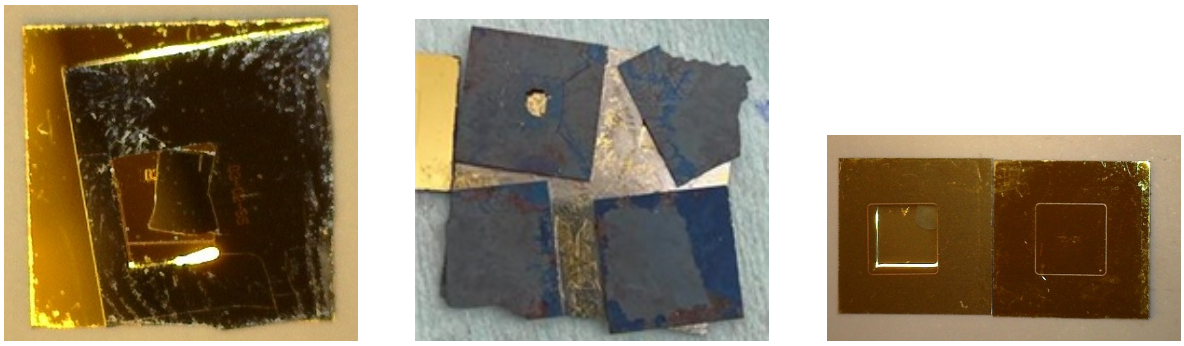


Figure 4-38: Breaking of dies during bonding.

In order to overcome these issues, several measures were taken which include putting dummy wafers on the top and the bottom platen of the bonder, cleaning of the backside of the dies and using teflon film and Kapton tape to fix the dies in place while bonding. These measures have been pictured in figure 4-39.

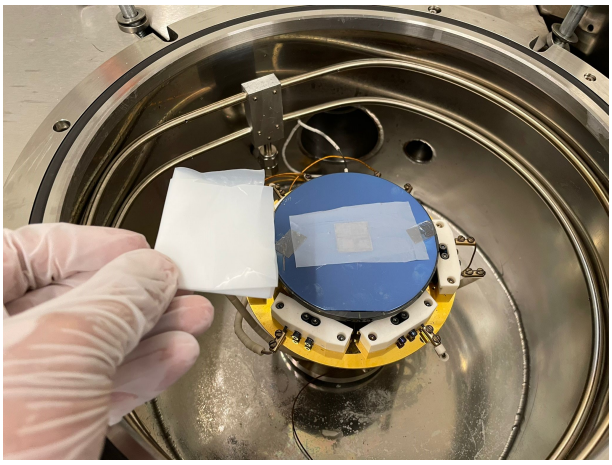


Figure 4-39: Mitigation measures for preventing die breakage.

4-4 Conclusion

In this chapter, the design that were proposed in Chapter 2 for the commencement of the bonding experiments were successfully fabricated.

The most critical step in the process, i.e., the screen printing of the nano-paste and its lift-off was successfully optimized to ensure a good quality of patterning. At the end of the optimization process, a very well-defined seal patterned with minimal or no residue was obtained. However, since screen printing is a manual process, the repeatability of the uniformity of the seal ring is an issue. Moreover, due to the rough edges and the nano paste itself being solidified along the edge of the squeegee blade, the uniformity of the profile is very difficult to control. Therefore, every sample before being sent for bonding was analyzed using optical and profilometry tools to ensure good uniformity of profile along the seal to do away with any large pressure unevenness on the seal during the bonding experiments.

Another important aspect of the fabrication was the depth of the cavity that was etched during the deep reactive ion etching step. The variability in depth was around 10 μm from the centre to the edge of the wafer which may pose a problem in the measurement of the absolute pressure inside the cavity using the thin cap deflection method.

Experimentation and Results

Experiments on bonding with changing parameters such as sintering pressure and temperature are explored in detail in this chapter. This is then followed by the usage of the cap deflection method to characterize the hermeticity of the cavity, which includes determining the absolute pressure inside the cavity along with the leak rate evaluation of the bonding approach. In addition, a residual stress analysis will be conducted on the designed structure followed by the assessment of bond quality with the help of bond shear test analysis followed by the analysis of failure using SEM imaging and EDX characterization of the fracture surface.

5-1 Vacuum Characterization of the structures.

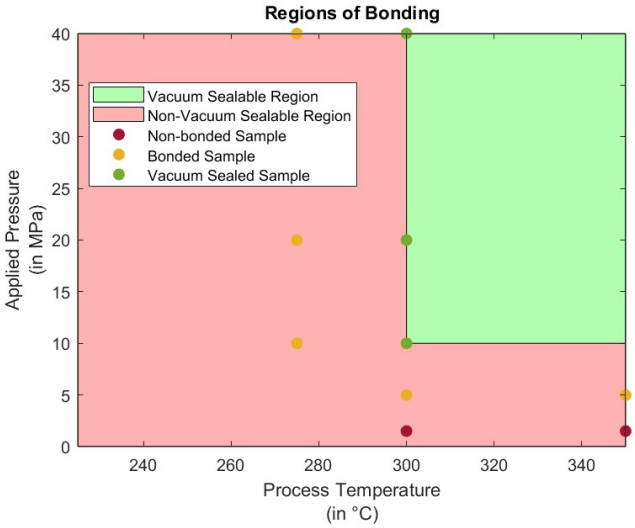


Figure 5-1: Various regions of bondability.

5-1-1 Hermeticity dependence on Bonding Parameters

An experimental study of bonding was run to investigate hermeticity at the various bonding temperature and pressure combinations.

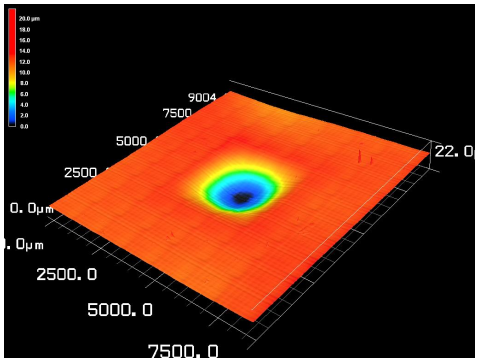
Initially, the wafer-level bonding could not be carried out due to the levelling problem of the top chuck of the AML bonder which didn't allow for the uniformity of force over the entire

wafer. From the manual of the AML Bonder, it was found that the maximum allowable force for the equipment was 12 kN which translates to a pressure of 1.5 MPa over the wafer. Therefore, to investigate bonding at higher pressures, die-level approach was used due to the smaller surface area of the die allowing for higher pressure for the same value of force applied. Thus, the wafer level bonding was simulated with the die level approach by the application of 1.5 MPa at a temperature of 300 °C as the starting temperature as this is the temperature where the organic solvent fully evaporates from the paste[149]. The experiment revealed no hermetic sealing. The process temperature was increased to 350 °C to further assist the sintering process at the same pressure with no successful hermetic sealing obtained. Now this process was repeated for higher pressure values of 5 MPa, 10 MPa, 20 MPa and 40 MPa with the design of experiments tabulated in table 5-1. All of the experiments were performed with the G1O2 (8 μm) and G3O4D10 (40 μm) designs as the two extreme geometries of the sealing ring. Moreover, a dummy gold-gold bonding experiment was also done at vacuum sealable pressures for the nano-Cu ring to exclude the possibility of the Gold causing the hermetic sealing. The hermetic sealing was confirmed by visual inspection of the bonded

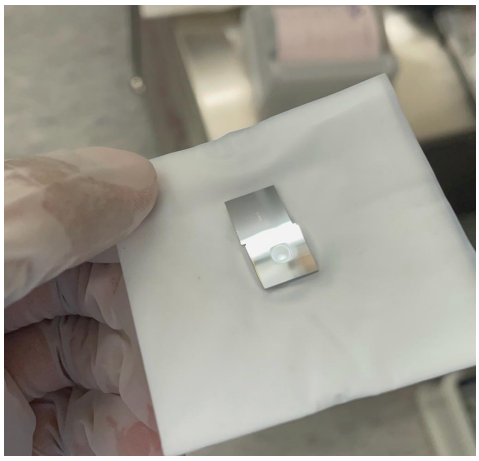
Table 5-1: Design of Experiments for hermeticity investigation.

DOE Number	**Pressure (MPa)**	**Temperature (°C)**
1	1.5	300
2	1.5	350
3	5	300
4	5	350
5	10	300
6	10	275
7	20	300
8	20	275
9	40	300
10	40	275

sample having a visible deflection of the thin membrane on top, followed by observation using the Keyence VK-250 Scanning microscope, as illustrated in figure 5-2, for a sample bonded at 40 MPa/300°C with the G3-O4-D10 design.



(a) 3-D image of the profile of the top die surface.



(b) Visible deflection on top of the vacuum-sealed cavity.

Figure 5-2: Profilometric data of the first successful hermetic sealing experiment.

The outcome of the experiments were used to determine various regions of bonding, as graphically illustrated in figure 5-1. The various regions of bonding can be defined as under:

- **Non-Vacuum Sealable Region:** This region occurs at the combination of temperatures less than 300 °C and applied pressure value of less than 10 MPa. In this region of bonding, the samples were found to be bonded at process parameters greater than or equal to 5 MPa of applied pressure and 300 °C. However, no bonding or a very weak bond with bond failure occurring during handling was observed for samples bonded at 1.5 MPa of applied pressure at 300°C and 350°C.

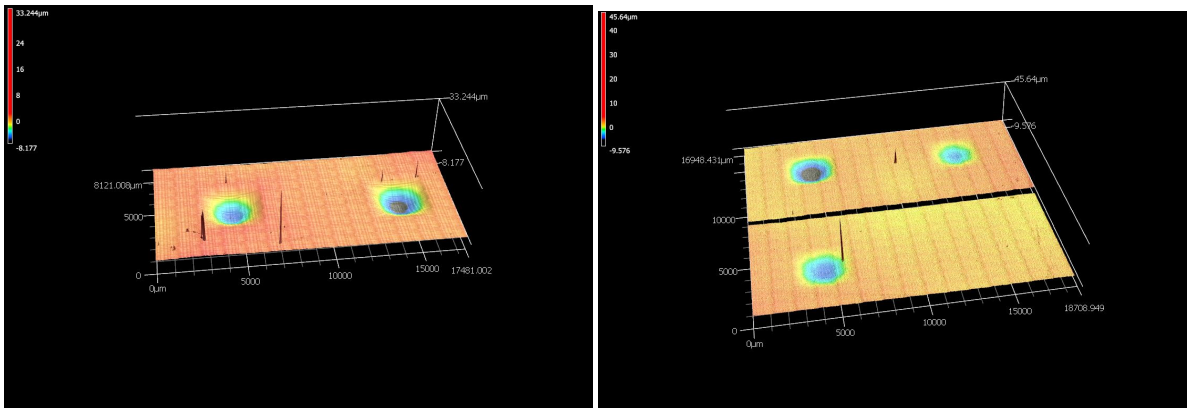
- **Vacuum Sealable Region:** This region includes process parameters of greater than or equal to 10 MPa pressure and 300 °C. However, the yield at 10 MPa was low with only one out of five samples being vacuum sealed. On the other hand for an applied pressure of 20 MPa, 50% of the samples that were bonded were vacuum sealed. The yield values remain the same for both 20 MPa and 40 MPa. Therefore for further bonding studies with multiple-die bonding, the applied pressure was fixed at 20 MPa.

5-1-2 Measurement of Absolute level of vacuum for various sealed samples.

To get a bigger sample size for the investigation of the encapsulated vacuum levels obtainable with the bonding approach used in this study, multi-die level bonding was done at 20 MPa and 300 °C which was successful in the batch fabrication of hermetically sealed cavities.

Table 5-2: Summary of the vacuum sealed samples.

Sample No.	Design	Membrane thickness (μm)	Deflection (μm)	Equation used	Bonding Temperature (°C)	Bonding Pressure (MPa)
1.	G3-O6-D10	69.87	9.36	$\delta = 10.56 - 5.84 \times 10^{-5} P_{vac}$	300	20
2.	G2-O4-D10	82	5.555	$\delta = 8.481 - 3.745 \times 10^{-5} P_{vac}$	300	20
3.	G2-O4-D10	88.21	6.161	$\delta = 7.807 - 3.058 \times 10^{-5} P_{vac}$	300	20
4.	G2-O2-D10	75.48	6.827	$\delta = 9.441 - 4.711 \times 10^{-5} P_{vac}$	300	20
5.	G3-O2-D5	71.86	8.101	$\delta = 10.13 - 5.401 \times 10^{-5} P_{vac}$	300	20
6.	G2-O4-D5	76.32	3.916	$\delta = 9.297 - 4.569 \times 10^{-5} P_{vac}$	300	20
7.	G1-O4	70.59	6.945	$\delta = 10.32 - 5.62 \times 10^{-5} P_{vac}$	300	20
8.	G1-O4	70.59	6.961	$\delta = 10.32 - 5.62 \times 10^{-5} P_{vac}$	300	20
9.	G3-O4-D10	83	2.565	$\delta = 8.359 - 3.62 \times 10^{-5} P_{vac}$	300	20
10.	G3-O6-D5	69.87	8.76	$\delta = 10.56 - 5.84 \times 10^{-5} P_{vac}$	300	20
11.	G3-O6-D5	75.4	7.81	$\delta = 9.186 - 3.856 \times 10^{-5} P_{vac}$	300	20
12.	G2-O2-D5	71.86	8.23	$\delta = 10.13 - 5.401 \times 10^{-5} P_{vac}$	300	20
13.	G1-O2	70.59	7.21	$\delta = 10.32 - 5.62 \times 10^{-5} P_{vac}$	300	20
14.	G3-O6-D10	59	12.592	$\delta = 14.043 - 9.3342 \times 10^{-5} P_{vac}$	300	20
15.	G3-O4-D10	74.38	8.265	$\delta = 9.231 - 3.919 \times 10^{-5} P_{vac}$	300	20
16.	G1-O2	85.2	6.480	$\delta = 8.11 - 3.367 \times 10^{-5} P_{vac}$	300	20
17.	G3-O4-D10	46	21.897	$\delta = 23.23 - 18.532 \times 10^{-5} P_{vac}$	300	40
18.	G1-O2	78.41	5.655	$\delta = 8.92 - 4.12 \times 10^{-5} P_{vac}$	300	10



(a) Two dies bonded at once. **(b)** Four dies bonded at once.

Figure 5-3: Multi-die level bonding at 20 MPa/300 °C.

For the measurement of the absolute pressures, the cap deflection method as described in section 3-5-1 was used. The deflections of the various vacuum-sealed samples were measured using the profile measurement functionality of the Keyence VK-250 scanning microscope as illustrated in figure 5-4.

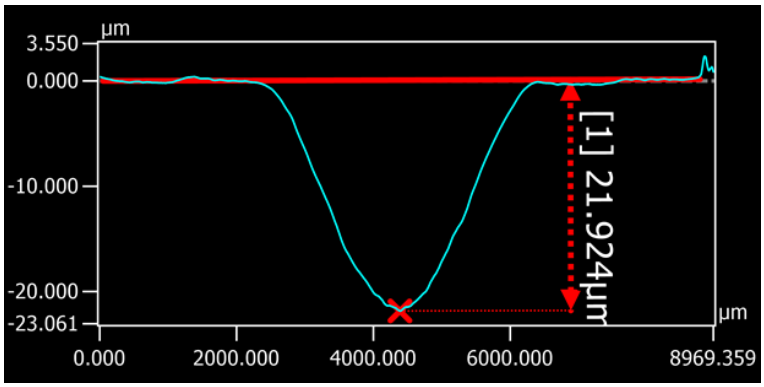


Figure 5-4: Deflection measurement of a samplewith G3-O4-D10 design bonded at 40 MPa/300°C.

Furthermore, simulations were run for each of the samples with varying cavity depths and hence membrane thickness using figure 4-32 followed by fitting a linear curve to each of the samples with different membrane thicknesses. The results of this procedure have been tabulated in table 5-2.

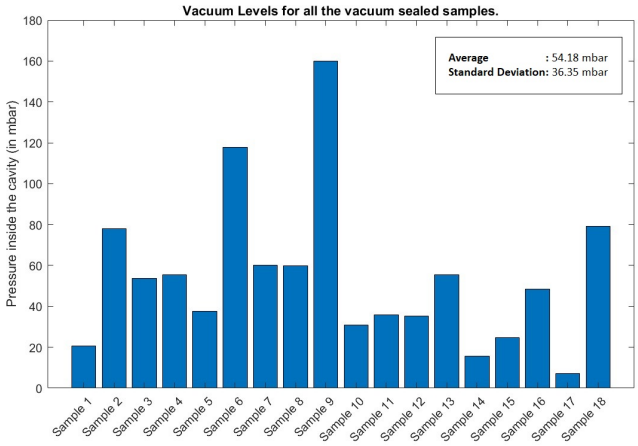


Figure 5-5: Absolute Pressure level for all sealed cavities.

Following the simulations, the absolute pressure values for the cavity interiors of the various vacuum samples were calculated and have been illustrated in figure 5-5. It was observed that there was no discernible trend in the vacuum levels with respect to the geometry variations or process conditions. The sealed samples have a mean vacuum level of 54.18 mbar. This pressure is higher than the range of pressure levels (10^{-6} mbar to 10^{-3} mbar) at which the samples were bonded. This points to the fact that the nano-Cu may have some residual organic solvents leading to outgassing after the hermetic seal was established leading to higher pressure levels inside the cavity. Moreover, this can also explain the wide variation in the encapsulated pressure values as indicated by the standard deviation of 36.35 mbar as different samples may have a different amount of residual organic solvents thereby leading to different amounts of outgassing.

5-1-3 Leak Rate

Leak rate testing as described in section 3-5-1 was used to determine the stability of the hermetically sealed packages by measuring the pressure-driven deflection using the Keyence VK-250 scanning microscope as depicted in figure 5-6. Three samples bonded at 300°C and 20 MPa with different designs (G1-O2 (8μm sealing width), G3-O4-D10 (40μm sealing width), and G3-O6-D10 (44μm sealing width)) with the G1-O2 and G3-O4-D10 sample kept in storage for 36 days and G3-O6-D10 sample for 48 days to investigate the influence of geometry on the leak rate. Moreover, one sample bonded at 300°C and 40 MPa with design and one sample bonded at 300°C and 10 MPa with design G1-O2 were also kept in storage for 41 days and 11 days respectively for leak rate testing to investigate the influence of sintering pressure on the leakage of the seal.

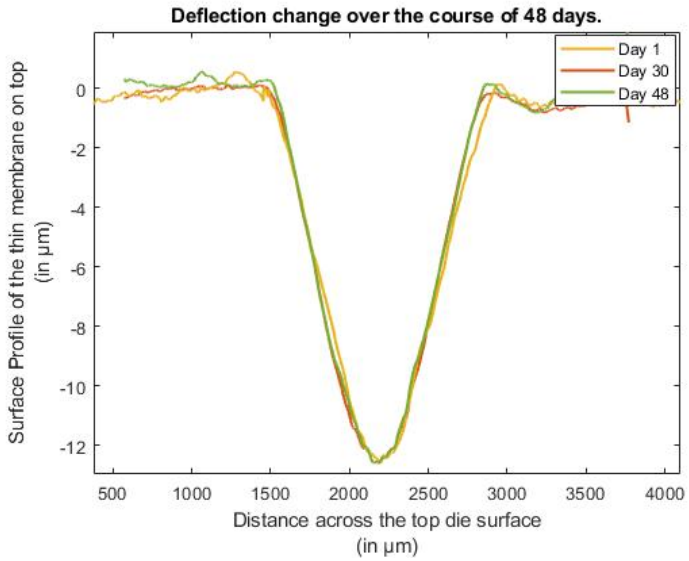


Figure 5-6: Variation of membrane deflection over 48 days for the sample with G3-O6-D10 bonded at 300°C and 20 MPa.

Leak Rate Comparison of various designs bonded at same process conditions of 20 MPa and 300 °C

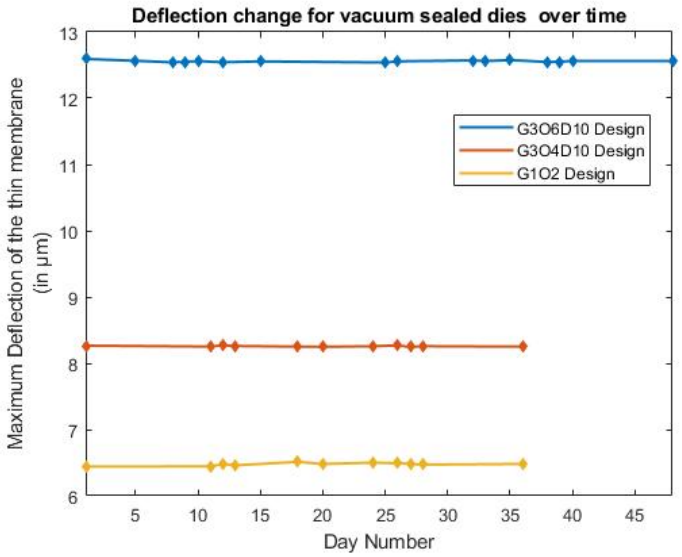


Figure 5-7: Variation of membrane deflection over time.

From the recorded data depicted in figure 5-7, it is evident that there is no discernible trend in the deflection changes over time, since both positive and negative changes were detected during the evaluation period. This indicates that the variations of measured deflections are equivalent to the measurement system's noise, which reflects the detection limit of this measurement.

Under the premise that the cavity is a perfect cuboid, the volume of the cavity was determined to be 7.223×10^{-6} L. In actuality, however, the cavity volume is smaller due to diaphragm deflection, so using this assumption for calculation will result in a conservative estimate of the leak rate. Local weather stations provided the average value of air pressure of 1013.35 mbar over the two months during which the samples were in storage that was used for the measurement of the leak rate. By a cautious estimate, using the worst case change in deflection of 0.032 μm for the G1-O2 design between day 18 and day 20, 0.024 μm for the G3-O4-D10 design between day 26 and day 27, and 0.028 μm for the G3-O6-D10 design between day 1 and day 5 and using equation 3-3, the leak rate has been tabulated in table 5-3.

Table 5-3: Leak rate evaluation of different designs at the same process conditions of temperature and pressure of 300°C/20 MPa.

Design Name	Leak Rate (mbarL/sec)
G1-O2	2.1×10^{-10}
G3-O4-D10	2.46×10^{-10}
G3-O6-D10	4.7×10^{-11}

However, the actual leak rates of the sealed cavities should be lower than this figure.

Leak Rate Comparison of various designs bonded at different pressures

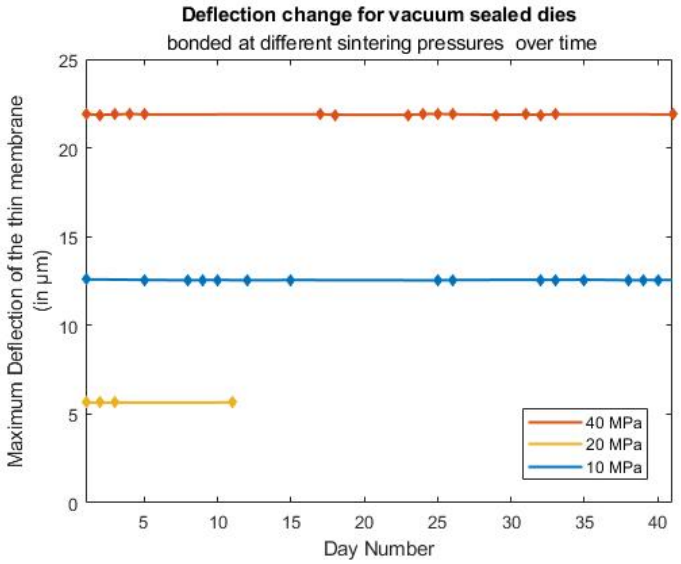


Figure 5-8: Variation of membrane deflection over time for vacuum sealed samples bonded at different pressures.

Similar to the different geometries under constant process conditions, there is no clear pattern in the deflection changes over time for vacuum-sealed cavities bonded at different pressures of 10 MPa, 20 MPa, and 40 MPa at 300°C with both positive and negative changes found over the assessment period in this case as well. Using the procedure used in the previous section,

a conservative estimate of the leak rate with different sintering pressures has been tabulated in table 5-4.

Table 5-4: Leak rate evaluation at different sintering conditions.

Sintering Pressure	Leak Rate (mbarL/sec)
10 MPa	3×10^{-11}
20 MPa	2.46×10^{-10}
40 MPa	1.43×10^{-10}

5-2 Residual Stress Analysis

The equivalent stress or the von Mises yield was used to examine the reliability of the structure. This stress depicts the yielding of the material subjected to loading. The von Mises criterion states that yielding happens when applied stresses exceed the materials requirement [145]. This analysis is helpful in the understanding of fatigue failure in materials.

The FEM method was used to determine the von Mises stress in the seal ring after the completion of the sintering process of the Copper nano-particles.

5-2-1 Method

The quarter model (figure 3-11) described in section 3-5-1 was used for this simulation as well. A time domain analysis was done to accurately simulate the process conditions that occur during the sintering process. During the simulation, the package is first heated from room temperature (20°C) up to the sintering temperature within seven minutes and then the temperature was kept at a constant sintering temperature for 30 minutes followed by cooling to room temperature (20°C) within 3 hours. An external pressure is applied on thof the side of the structure to simulate pressure assisted sintering during the reduction of Copper paste and the sintering phase. The default general material properties provided iMSOL were used for the simulation and have been summarized in table 5-5. Furthermore, the same assumptions used in section 3-5-1 were also considered for this time-domain simulation.

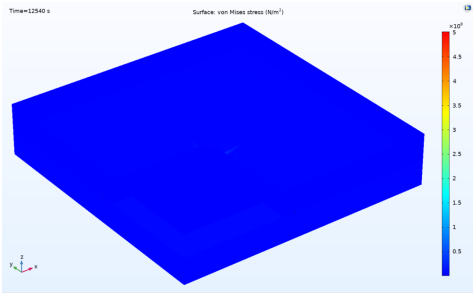
Table 5-5: Summary of Material Properties used for the simulation.

Material	Young's modulus (GPa)	Poisson ratio	CTE (1/K)	Thermal Conductivity (W/mK)
Silicon	170	0.28	2.6×10^{-6}	130
Gold	70	0.44	14.2×10^{-6}	317
Titanium	115.7	0.321	8.6×10^{-6}	21.9
Silicon Dioxide	70	0.17	0.5×10^{-6}	1.4
Nano-Copper	120	0.34	16.5×10^{-6}	401

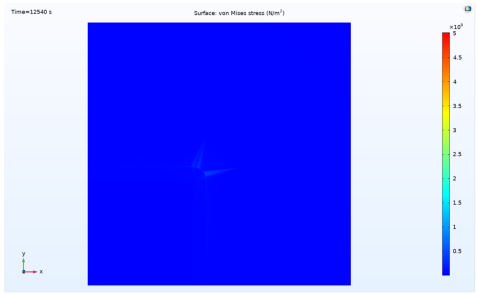
5-2-2 Results

Analysis of Stress distribution in the cavity

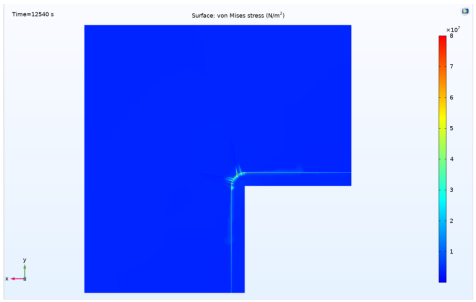
For this analysis, due to the fact that there was no discernible trend with respect to the maximum stress values for the different designs, G1-O2, having the worst-case scenario of the highest maximum pressure was chosen for the residual stress analysis. From the 3D plot of the entire cavity, it can be seen stress is confined to the seal ring. This trend can be seen for all the designs with different sealing widths. The rest of the structure practically exhibits no residual stress which makes sense considering the bulk of the structure consists of Silicon only which has a high Young's Modulus and a lower CTE and thus doesn't deform easily, while on the other hand, Cu has a lower Young's Modulus and a much higher CTE leading to higher deformation and thus residual stress.



(a) Overall View of the structure.



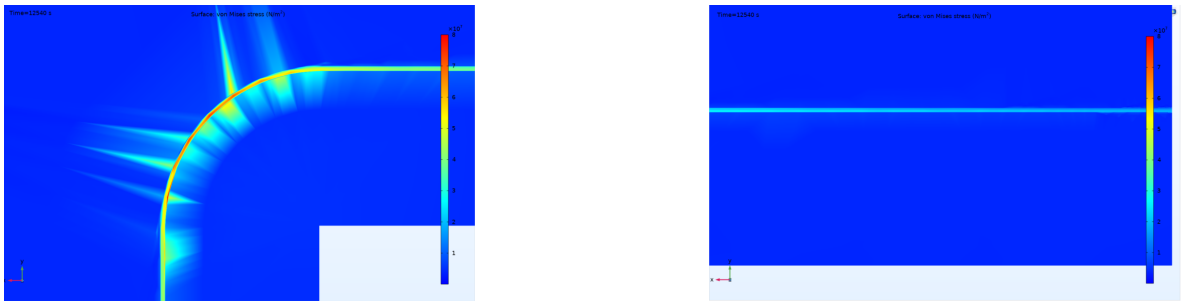
(b) Top view of the structure.



(c) Cut Plane view of the sealing ring.

Figure 5-9: Image of the setups used for nano-particle stencil printing for various die sizes.

On closer inspection (figure 5-10), it can be observed that the stress values are much higher at the rounded corners of the seal ring as compared to the straight edges. A maximum stress value of 165MPa was found to be present at the rounded edges as compared to 60 MPa near the straight edges. Thus, delamination will tend to occur in this region of high residual stress.



(a) Zoomed-in view of the corner. **(b)** Zoomed in view of the edge.

Figure 5-10: Image of the setups used for nano-particle stencil printing for various die sizes.

Effect of Applied Pressure on Residual Stress

The application of pressure during sintering aids in the densification of the copper nano-particles by increasing the contact area between them. Nonetheless, it will also result in deformation during bonding, thereby introducing residual stress. With the sintering pressure

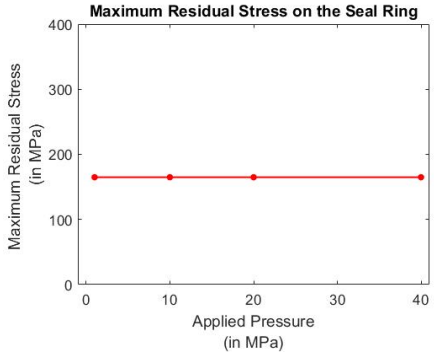


Figure 5-11: Maximum Residual Pressure vs Applied sintering Pressure.

increasing from 1MPa to 40 MPa while keeping temperature constant at 300°C, the maximum residual stress remains the same, as illustrated in figure 5-11. Even at a modest sintering pressure of 1 MPa, the stress value had already reached 165 MPa. This analysis concludes that an increase in applied pressure does not result in an increase in the maximum residual stress.

Effect of Applied Temperature on Residual Stress

As shown in section 2-3, the use of temperature in conjunction with a greater sintering pressure can amplify the effect of Cu nanoparticles coalescing. Nonetheless, temperature fluctuations are one of the principal sources of residual stress induction. At a constant pressure of 20 MPa, the influence of different temperatures on the maximum residual stress was investigated. The results are depicted in the figure 5-12.

It can be observed that the residual stress increases with increase in the bonding temperature. This is due to the fact that the increase in temperature increases the CTE mismatch leading due a higher residual stress.

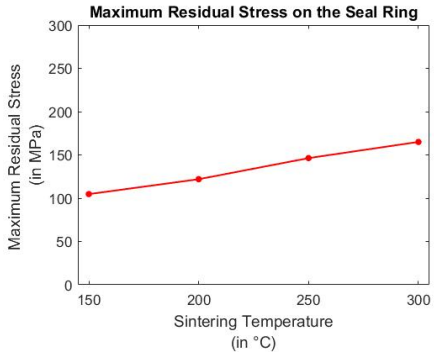


Figure 5-12: Maximum Residual Pressure vs Applied sintering Temperature.

5-3 Bond Strength Testing

To mechanically assess the bonding quality of the nano-Cu seal, bond shear test as described in section 3-5-2 were performed for various designs to investigate the effect of geometry on the bond strength. Moreover, a parametric study was also done to determine the effect of sintering pressure on the bond strength. This was followed by the analysis of failure modes through which the various samples failed during the bond shear testing.

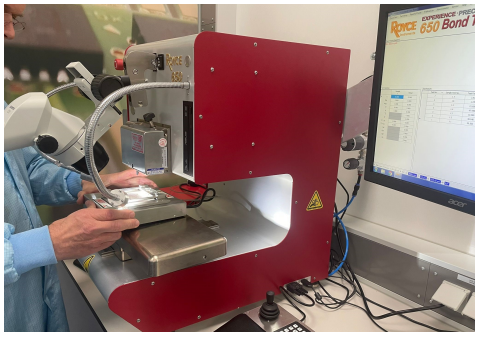


Figure 5-13: Royce 650 Universal Bond Tester.

5-3-1 Description of Test Setup

The shear tests were performed on the Royce 650 universal bond tester as illustrated in figure 5-13. The various recipe variables that were used while testing have been tabulated in table 5-6.

Table 5-6: Recipe parameters used while bonding. With 1 kgf being equal to 9.8 Newton.

Parameter	Value
Test Start Force	0.1 kgf
Shear Speed	50μm/s
Upper Force Specification limit	10 kgf
Lower Force Specification limit	0 kgf

The equipment only allowed for the testing of 5 mm dies, therefore the samples had to be diced into quarters before the commencement of shear testing. Dicing was done using the Disco DAD321 dicer. A lower feed speed of 1mm/s and the S3560 dicing blade was used to allow for cleaner cuts, thereby ensuring minimum damage to the bond interface. However, despite these measures, the dicing led to the failure of some diced samples with the bond being broken as depicted in figure 5-14.

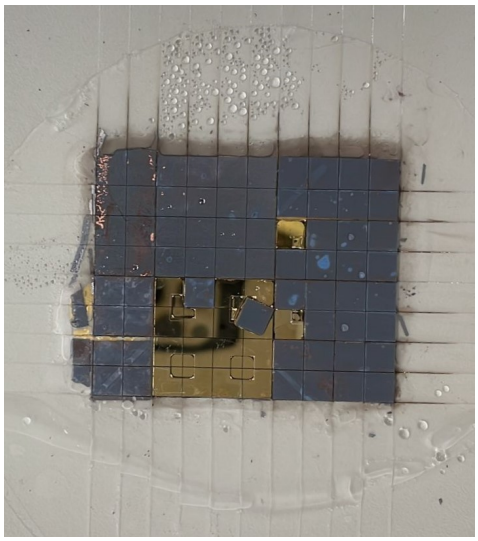


Figure 5-14: Damaged dies after dicing.

Out of the 180 samples prepared for the die shear, 137 survived the dicing operation. Following dicing, the samples were placed in a sample holder with thermal paste on the sample positions. This was followed by curing of the glue at 150 °C for 5 minutes on a hotplate (figure 5-15) .

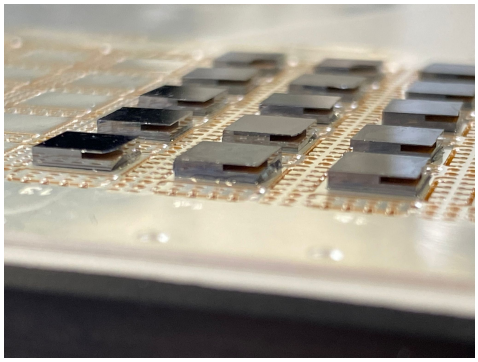


Figure 5-15: Prepared samples on top of the sample holder.

After the preparation of the samples, the dies were sent for shear force testing with multiple samples on a single sample holder, and proper care was taken to ensure the alignment of the shear head with the edge of the samples.

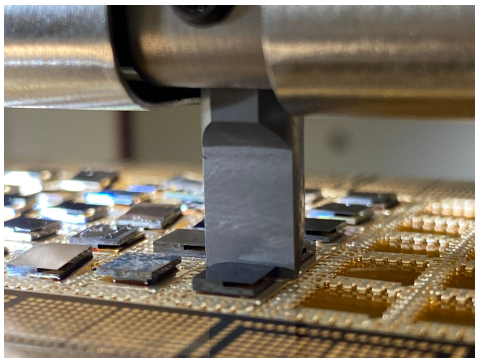


Figure 5-16: Shear testing in action.

5-3-2 Results

Following the shear testing of the samples, it was observed that a large number of dies did not fail even at high shear forces of greater than 7 kgf to the point where the sample holder began to break under the force. On closer inspection, it was noted that for some of these samples, the thermal glue had seeped into the interface between the bottom and the top die. This was observed for 35 out of the 137 samples, thus the results of these samples were deemed inadmissible and hence discarded. Furthermore, two gold-gold bonded dies without the nano-Cu seal ring were subjected to shear test and the shear test revealed a shear force strength of 1.2 kgf. This pointed to the fact that the gold-gold bonding was also playing a role in the shear strength of the dies. Moreover, some of the samples were also failing at a 0 kgf shear force even though they were vacuum sealed prior to the dicing, which implied damage due to the dicing procedure. Owing to these non-idealities, the effect of geometric variations on the bond strength could not be investigated, and it was decided to investigate the failure modes of the various shear-tested samples by observation of the fracture surface using SEM imaging.

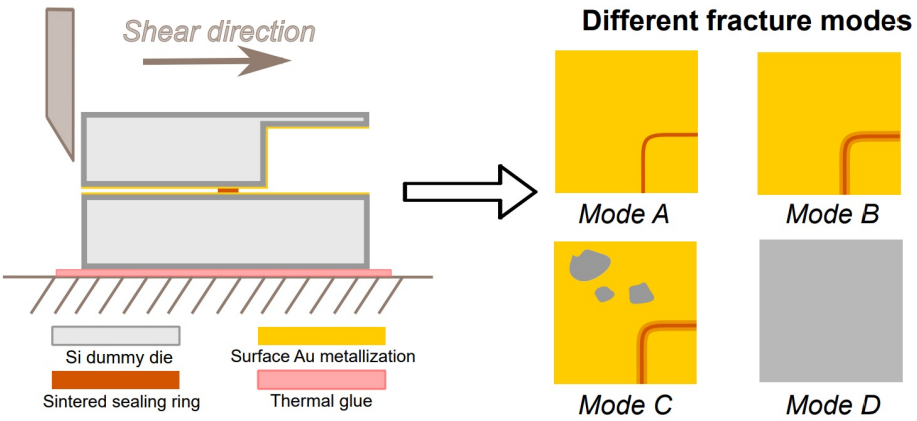


Figure 5-17: Failure modes of samples after shear testing.

Failure Analysis

On visual inspection of the samples after the die shear test, it was observed that the failure occurred through four modes as depicted graphically in figure 5-17. These failures were further studied to investigate the failure mechanisms for the various samples.

Mode A

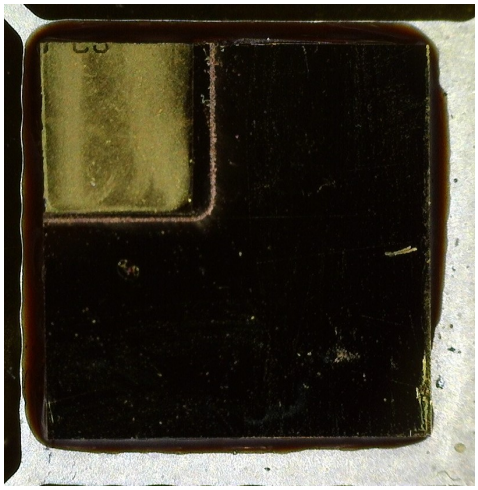
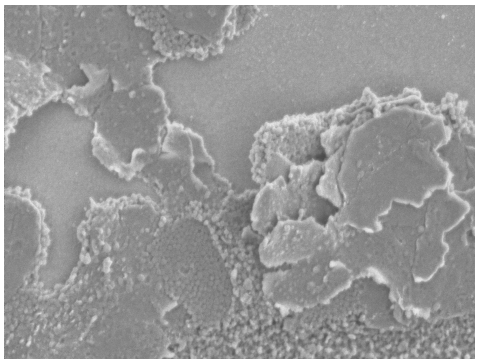
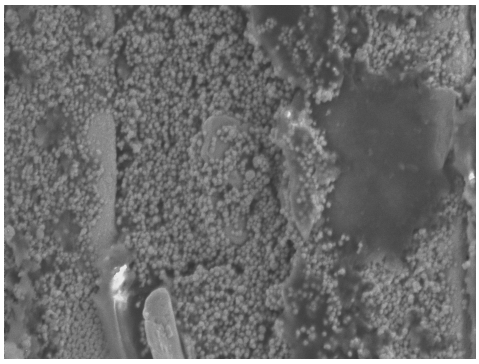


Figure 5-18: sample with failure Mode A.

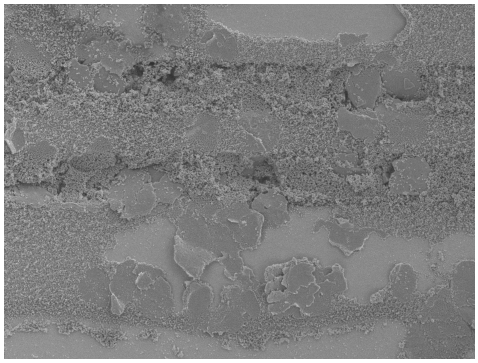
In this mode of failure, the bond appears to have cleaved from the nano-Cu seal itself, with no gold ripped off from the surface of the die (figure 5-18). The sample was then examined under the SEM to gain more insight into the surface fracture morphology.



(a) Partially sintered Cu nanoparticles near the overlap regions.



(b) Unsintered Cu nanoparticles inside the groove.



(c) Overview of the seal ring at 2000x magnification.

Figure 5-19: Samples with Failure Mode A.

The overview of the seal ring's SEM picture (figure5-19) reveals patches of unsintered Copper. Inside the grooves, a closer examination reveals that the nanoparticles are unsintered and have negligible neck development during sintering. In addition, partial sintering can be observed in the region adjacent to the groove as a result of higher localized pressure, which is consistent with the design simulation results described in section 3-4. Thus, the cause of failure for samples exhibiting this failure mode can be attributed to the increased porosity of the nano-Cu seal as a result of less extent of sintering of the nanoparticles.

Mode B

This failure mode is characterized by the appearance of a border around the seal ring with the top die coming off without leaving any residues or taking off the gold from the surface of the bottom die (figure 5-20).

The SEM imaging overview of the seal rings reveals rice grain-like structures at the edges of the grooves. Moreover, it can be seen that parts of the groove have been taken off completely (figure 5-21).

Results from the EDX characterization revealed that the bottom die's Au/Ti layer has been entirely peeled off, as shown by the presence of 72.5% by weight silicon and 24.24% by weight

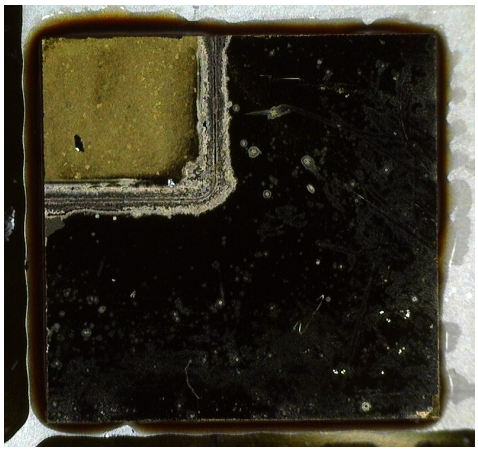


Figure 5-20: Sample with failure Mode B.

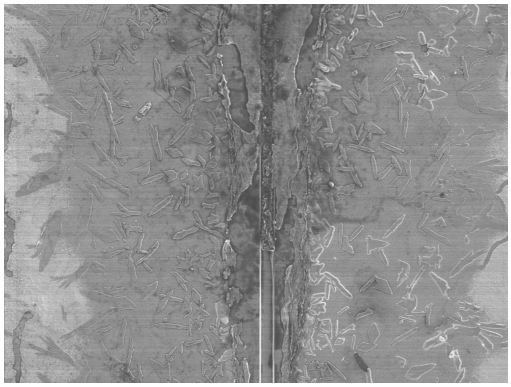


Figure 5-21: SEM overwiew image of Mode B failure at 250x.

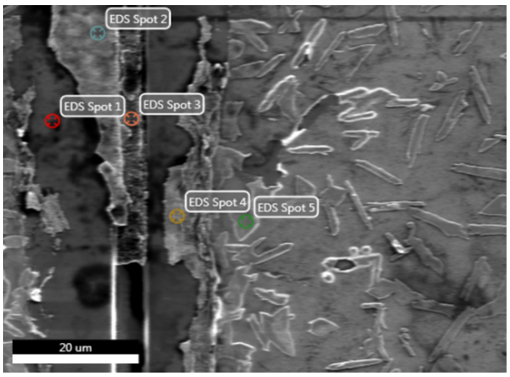


Figure 5-22: SEM image for EDAX characterization of Mode B Failure.

oxygen at spot 1 indicating the presence of silicon dioxide, which is adjacent to the groove's edge. In addition, at spot 2, it can be noted that this area comprises mostly of Gold (58.29% by weight) with Carbon(17.36% by weight) and fused Copper(19.72% by weight), indicating the presence of organic solvent residue in the fused nano-Copper. In addition, the structure resembling rice grains was evaluated with EDX at spots 4 and 5, with spot 5 being mostly Silicon(48.46% by weight) and spot 4 containing predominantly Gold (84.80 % by weight). This shows that these formations are the result of the removal of the Gold/Ti bilayer during die shearing. Thus, given this failure mode, it is possible to assume that the dies with this failure mode consist of nano-Copper that is thoroughly sintered and, consequently, extremely well attached to the gold layer underneath. In addition, the removal of the Au/Ti layer suggests that failure occurs when the shear stress exceeds the adhesion strength of Titanium to Silicon Dioxide. However, the presence of carbon suggests the presence of organics inside the layers of fused Copper, which may also have contributed to the weakening of the nano-Cu structure that resulted after sintering.

Mode C

This failure mode is distinguished by the existence of a border-like structure similar to Mode

Table 5-7: Spot-wise EDX characterization for figure 5-22

Element	Weight %	Atomic %	Net Int.	Error %	Kratio	Z	A	F
SPOT 1								
C K	3.23	6.17	108.71	7.98	0.0176	0.8103	0.6724	1.0000
O K	24.24	34.70	1236.82	4.87	0.1720	0.7684	0.9232	1.0000
SiK	72.52	59.13	2060.19	5.60	0.5265	0.7245	1.0016	1.0002
SPOT 2								
C K	17.36	65.15	922.61	5.74	0.1437	0.9968	0.8305	1.0000
CuL	19.72	14.00	571.67	5.13	0.1291	0.6394	1.0237	1.0000
SiK	4.69	7.52	167.94	7.90	0.0412	0.9004	0.9765	1.0005
AuM	58.23	13.33	581.26	7.41	0.3163	0.5211	1.0433	0.9992
SPOT 3								
CuL	100.00	100.00	2200.75	5.07	0.6434	0.6093	1.0560	1.0000
SPOT 4								
C K	11.62	63.41	432.86	6.10	0.1044	1.0994	0.8172	1.0000
SiK	3.58	8.36	91.37	9.82	0.0347	0.9916	0.9776	1.0005
AuM	84.80	28.23	613.29	7.10	0.5166	0.5868	1.0393	0.9998
SPOT 5								
C K	3.57	11.04	122.93	7.67	0.0228	0.8923	0.7162	1.0000
TiL	24.44	18.95	94.36	5.41	0.1609	0.6071	1.0840	1.0000
CuL	3.74	2.18	83.94	8.06	0.0226	0.5816	1.0402	1.0000
SiK	48.46	64.08	1322.71	5.75	0.3872	0.8038	0.9934	1.0006
AuM	19.79	3.73	142.49	9.27	0.0924	0.4496	1.0413	0.9972

B, but with remnants of the top wafer or a portion of the bottom die missing (figure 5-23). Additionally, SEM and EDX analyses were conducted on the sample exhibiting this failure mechanism. The overview of the sealing ring (figure 5-24) revealed the same surface morphology with rice-grain-like shaped structures as encountered in Mode B. However, it can be observed that the region adjacent to the grooves is a lot smoother. To investigate further, the sample was subjected to EDX characterization with the results depicted in figure 5-25.

EDX characterization revealed that the smooth looking region near the groove edge is Silicon, with the Gold almost completely gone (figure 5-25). This implies that the Au/Ti bi-layer was completely taken off from these regions after shearing of the sample.

Moreover, the regions with residues on the surface of the sample away from the ring was also investigated using Spot EDX (figure 5-26).

EDX analysis results (figure 5-26) at spots 1 and 3 reveal the presence of copper (65.04% and 100% by weight respectively) at these locations. This can be attributed to the small residue of Copper that was left behind after the liftoff process. In addition, Silicon(59.49% by weight) and Oxygen(23.56% by weight) were detected at spot 5, indicating the presence of silicon dioxide. This indicates that the Au/Ti layer was removed from this site. In addition, the detection of Copper (16.64% by weight) at spot 6 confirms that this portion was removed owing to the presence of nano-Cu residues at this specific location.

Similar to the case of Mode B, the removal of the Au/Ti layer near the grooves suggests that the failure was initiated at a shear force that exceeded the adhesion strength of the Ti to

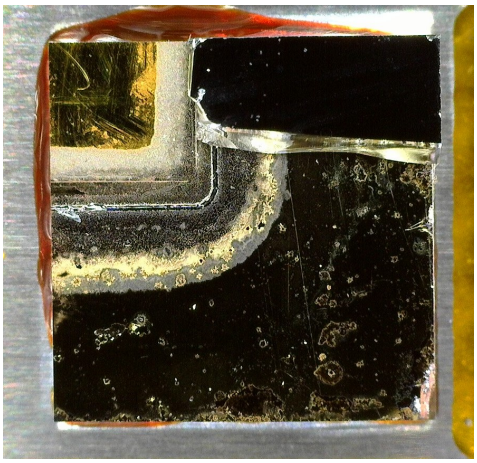
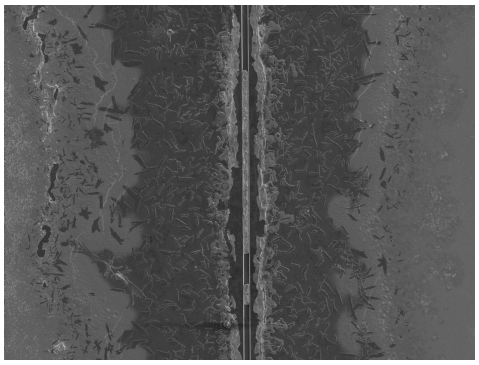
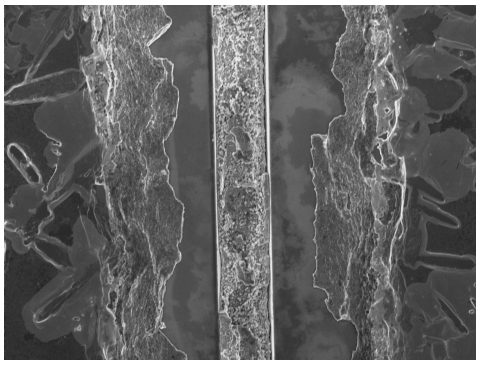


Figure 5-23: Optical Image of Mode C



(a) Overview of the sealing ring at 250x.



(b) Zoomed in view of the sample at 2000x.

Figure 5-24: SEM analysis of failure mode C.

Silicon Dioxide layer.

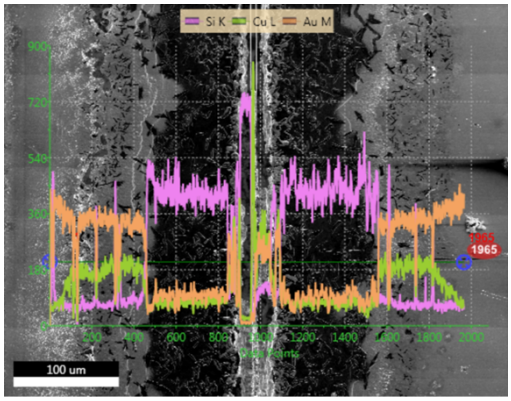


Figure 5-25: EDX characterization of Mode C.

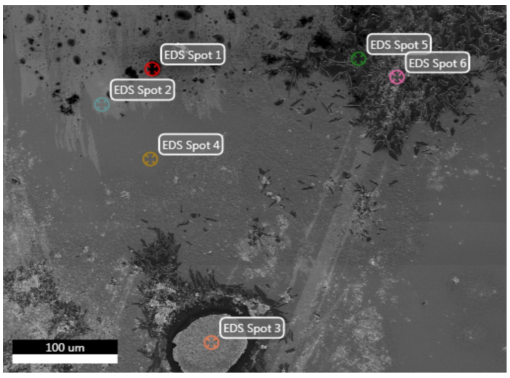


Figure 5-26: EDX characterization at residues away from the grooves for Mode C.

Mode D

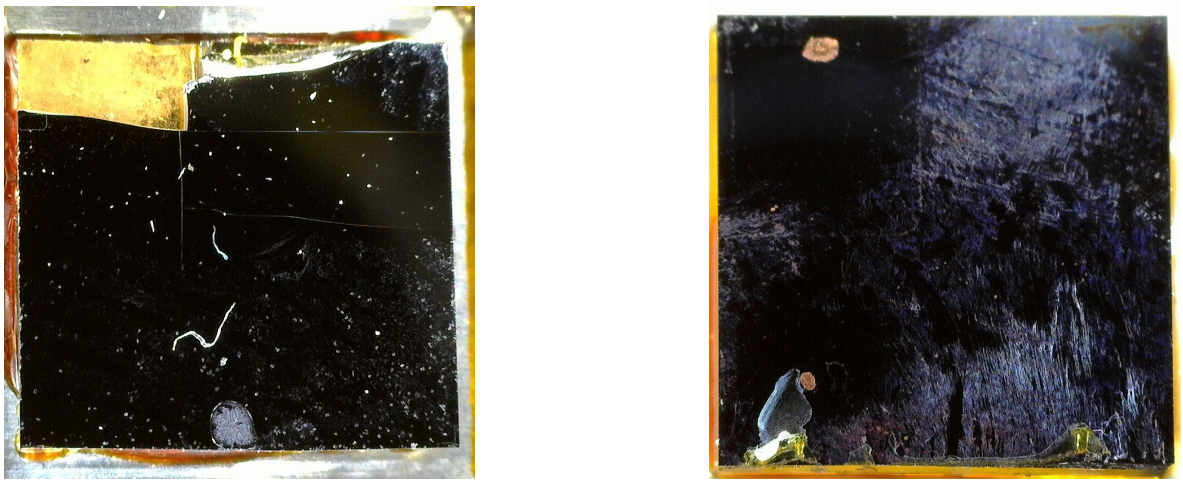


Figure 5-27: Samples with Failure Mode D.

This mode of failure was characterized by the failure of the sample holder without the shearing of the sample even at shear force values of greater than 7kgf. the reasoning for this could be the higher degree of gold-gold bonding. Focused Ion Beam milling (FIB) was used to get a better look at the cross-section. However, due to the damage caused by dicing, no valuable conclusion could be drawn for the morphology of the bond interface.

Shear Strength comparison of failure modes.

Following the commencement of the shear tests, the bond strength of all four failure modes for various samples was compared. The results have been plotted in figure 5-28. It can be seen that the average bond shear strength increases in the order Mode A $<$ Mode B $<$ Mode C $<$ Mode D. This is in agreement with the observations from the failure analysis with the Mode B and Mode C sharing a common fracture mode, thereby having comparable bond strengths and Mode C having slightly higher bond strength due to the bonding of nano-Cu

Table 5-8: Spot-wise EDX characterisation for figure 5-26

Element	Weight %	Atomic %	Net Int.	Error %	Kratio	Z	A	F
SPOT 1								
C K	65.04	96.83	3902.95	4.03	0.5210	0.8209	0.9758	1.0000
AuM	34.96	3.17	324.62	8.64	0.1514	0.4093	1.0588	0.9995
SPOT 2								
AuM	100.00	100.00	1083.33	6.79	0.6936	0.6736	1.0314	1.0000
SPOT 3								
CuL	100.00	100.00	2668.37	4.99	0.6434	0.6093	1.0560	1.0000
SPOT 4								
AuM	100.00	100.00	1066.85	6.77	0.6936	0.6736	1.0314	1.0000
SPOT 5								
C K	2.57	5.53	84.18	8.06	0.0151	0.8352	0.7003	1.0000
O K	23.56	37.97	1110.57	5.04	0.1704	0.7899	0.9156	1.0000
SiK	59.49	54.62	1583.35	5.67	0.4464	0.7504	0.9996	1.0004
AuM	14.38	1.88	98.63	10.30	0.0616	0.4125	1.0427	0.9965
SPOT 6								
ScL	4.65	4.78	13.50	4.99	0.0288	0.6475	0.9541	1.0000
CuL	16.64	12.09	316.49	5.48	0.1052	0.6030	1.0483	1.0000
SiK	45.87	75.43	1052.47	5.91	0.3802	0.8397	0.9866	1.0005
AuM	32.83	7.70	201.98	8.81	0.1617	0.4763	1.0362	0.9978

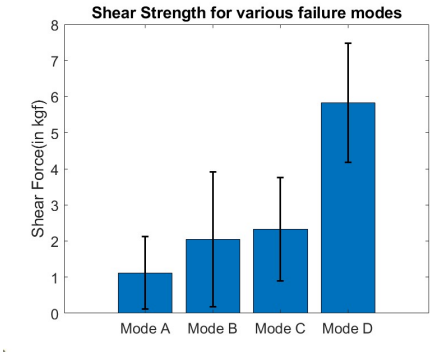


Figure 5-28: Shear strength comparison of samples with different failure modes.

residues in regions other than the seal region on the surface of the die. On the other hand, Mode A has the lowest bond strength due to partial sintering leading to a higher percentage of voids in the nano-Cu structure.

Effect of Applied Pressure on Bond Strength

The effect of applied sintering pressure at a constant temperature (300 °C) and geometry (G3-O2-D5) on the shear strength was also investigated. It can be observed that the bond shear strength increases with the increasing sintering pressure as depicted in figure 5-29, which is expected since the increased pressure increases the contact surface area between particles

leading to faster neck formation, which results in higher densification of the nanoparticles resulting in increased bond strength.

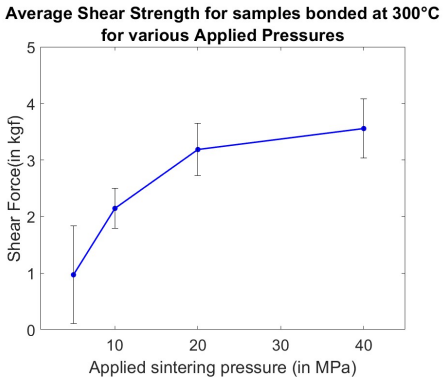


Figure 5-29: Shear Strength of the G3-O2-D5 design (26μm width seal) at varying pressures at 300°C.

5-4 Cross-sectional analysis using SEM imaging

Following the bonding experiments, the cross-sectional analysis of the bond was decided to be investigated by bond cleavage followed by SEM imaging. Due to the high wafer thickness of 510 μm, the FIB milling technique was rendered impractical in our case. Thus as an alternative, bond cleavage by way of mechanical dicing was implemented. However, due to the very small seal rings (8μm - 44μm), the bond cross-section was too damaged for the SEM imaging to visualize the cross-section. Therefore it was decided first to dice the wafer, followed by FIB milling. However, none of the samples survived the procedure. An illustration of a broken cross-section has been presented in figure 5-30.

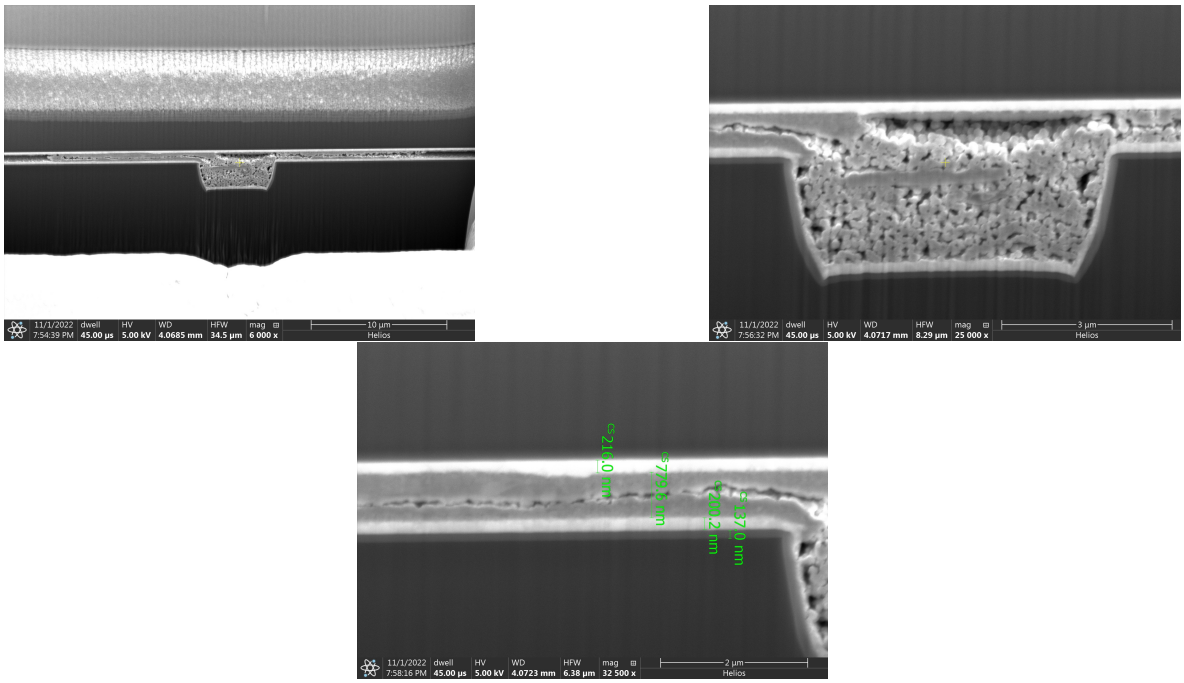


Figure 5-30: Cross section broken after dicing.

As can be seen in figure 5-30, there is a clear fracture along the middle of the nano-Cu seal. However, it can be seen that at the overlap regions, the nano-Cu looks continuous with no visible porosity. However, on the other hand, there is a lot of porosity in the grooves filled with unsintered nano-Copper. This can be explained by the combination of factors which include the depression of the nano-paste after post lift-off baking (section 4-3-2) and lower localized pressure in the groove region as per the simulation results described in section 3-4. Moreover, a bond layer thickness of 779.6nm was noted which translates to a 59.2 % reduction in height.

5-5 Discussion

In this chapter, various bonding experiments were carried out to investigate the hermeticity of the nano-Cu bond. The bonding experiments concluded that a combination of temperature and pressure values equal to or greater than 300°C and 10 MPa was sufficient for the hermetic sealing. Moreover, for the sake of comparison, a dummy gold-to-gold die and three samples with no groove design sealing ring were also bonded together. However, none of them demonstrated hermeticity at 300°C and 20MPa. After the bonding, the samples which bonded at 20 MPa/300°C were kept in storage for a period of 36-48 days for different geometries. Furthermore, no discernible pattern in membrane deflection was observed, with both positive and negative changes happening, which can be attributed to the limit of the resolution of measurement with the setup in place. Moreover, to investigate the effect of bonding pressure on leak rate, samples bonded at 10 MPa, 20 MPa and 40 MPa were also kept in storage for leak rate evaluation over a period of 11 to 41 days. However, no net variations were noted, thus confirming the stability of the encapsulated vacuum. Moreover, the absolute

vacuum level measurement of all the samples revealed an average encapsulated vacuum level of 54.18 mbar with a standard deviation of 36.35mbar. This pressure level is higher than the pressure level at which the samples were bonded (10^{-6} - 10^{-3} mbar), which indicates the presence of outgassing in the cavity. The source of this outgassing can be suggested to be the presence of residual organic solvents in the cavity, the presence of which was confirmed with the failure analysis done later on after the bond shear testing. This concluded the hermetic characterization of the bonding for this study.

Following the hermeticity characterization, a residual stress analysis was conducted using COMSOL, which revealed the worst-case residual stress of 165 MPa for the G1O2 design at the rounded corners and a residual stress of 60 MPa at the straight edges. Furthermore, it was observed that the applied sintering pressure did not influence the residual stress, while increasing the temperature was found to increase the residual stress due to a larger CTE mismatch at higher temperatures, leading to a higher deformation and hence higher residual stress.

Nextly, bond shear testing was done to assess the bond quality using the metric of bond shear strength. however, it was observed that the gold-gold bonding was also adding up to the shear strength. Due to the variability, the investigation of bond shear strength as a function of varying geometries could not be performed. However, four common failure modes were observed. A failure analysis was conducted for each failure mode using SEM imaging in conjugation with EDX characterization for the fracture surface morphologies revealing some notable details about the nature of bonding. It was found that with failure modes B and C, the fracture occurred by the ripping off of the top Au/Ti bilayer, which indicates the strength of this bonding. Moreover, carbon was also detected for Mode A, Mode B, and Mode C, which pointed to the presence of organic solvent residues within the sintered nano-copper, which may lead to the weakening of the bond. Furthermore, the samples falling in the category of Mode D did not shear owing to the failure of the sample holder before bond failure could occur. The reason for such high bond strength could be the larger involvement of the Gold-Gold bonding, which owing to its larger bonding area, leads to higher shear strength. Following this, the average bond strength for various failure modes was plotted with Mode 2 and Mode 3 having comparable bond strengths, which is confirmed by their similar fracture surface morphology, and samples with Mode A failure faring the worst due to the presence of partially sintered or unsintered nano-Cu in the seal ring. Moreover, a parametric study of bond strength for the same design at increasing pressure conditions was also done, which revealed the expected result of higher bond strength at higher applied pressure. However, it was observed that the rate of increase of the bond strength decreases as higher pressure is applied. This can be explained by the fact that at higher pressures, the nano-Cu is already well sintered, thereby leading to a saturative behaviour for the bond strength at higher applied pressure values.

For the final analysis, Cross-sectional bond imaging using FIB milling was tried but due to the damage of the dies during dicing, all the cross-sections of the various dies were damaged. A damaged sample was then investigated using SEM imaging, and it could be seen that the nano copper was fully sintered at the overlap regions of the grooves with the nano Copper in the grooves partially sintered.

Conclusions

In order for heterogeneous integration to realize its full potential, MEMS manufacturing techniques must continue to reduce the size, weight, power, and cost (SWaP-C) of MEMS components. MEMS packaging contributes up to 80% of the cost and size of a product. Thus, the utilization of low-cost, high-volume packaging alternatives is needed to optimize heterogeneous integration technology.

Many semiconductor sensors, particularly MEMS sensors such as inertial, temperature, pressure, and resonance sensors need a vacuum environment for optimal performance and sensitivity in addition to the improvement in their long-term reliability. When MEMS and CMOS ICs are integrated, Wafer Level Vacuum Packaging (WLVP) confronts extra challenges due to the need for thermal, chemical, and mechanical compatibility between the sensing element and CMOS ICs. Current WLVP approaches for packaging discrete MEMS devices, including anodic, direct, and glass frit bonding, are incompatible with the IC's temperature budget and/or require an excessively large sensor area. Cu is increasingly used in 3-D IC technologies' advanced CMOS circuits and electrical vias. Cu is compatible with sophisticated CMOS circuits and 3-D IC fabrication, making it a suitable material for bonding and sealing in microsystems of the future generation. Cu is suitable for thin sealing rings due to its mechanical strength, resulting in compact package sizes. Cu thermocompression bonding can accomplish wafer-level vacuum sealing at low temperatures, but it needs flat, clean Cu surfaces or additional capping layers, and the bonding regions are still rather large.

In order to overcome these drawbacks, the use of Cu-NP paste has been proposed. The high surface-to-volume ratio of nanoparticles allows for low-temperature sintering, which reduces the bonding temperature. Sub-micron nanoparticles can establish a surface-compliant bond that compensates for the surface roughness of the wafer surface. This study was conducted for the investigation of the usage of nano-Cu paste as a seal for the realization of wafer-level vacuum packaging. The main challenge with this approach is the porosity of the sintered nanoparticles, which can prove detrimental to the hermetic sealing of MEMS cavities. Within the next section, a complete overview of the research work done in this study has been summarized, followed by future work and recommendations.

6-1 Summary of the research work

- Firstly an extensive literature survey was done to gain more insight into the traditional as well as some novel bonding approaches. Metal-based bonding was found to be superior to other traditional bonding methods due to its suitability for wafer-level vacuum packaging. Moreover, extensive research was done on the densification mechanism of

Cu nanoparticles, which led to the conclusion of using pressure-assisted sintering as it allows for a larger contact area between nanoparticles, resulting in a high extent of densification of the nanoparticles.

- Next up, taking cues from the literature, a groove-based design for the sealing ring was investigated for the presence of localized high pressure using FEA simulations. The quantification of the presence of localized high pressures was done by comparing the groove-based design under similar pressure and temperature conditions. It was found that the standard deviation of volumetric pressure for the groove-based design was on average 1.35 times higher than that of a non-groove-based design with the same seal width indicating the presence of localized high and low pressures for a groove-based design. Moreover, a simulation model was developed to detect the absolute vacuum levels inside the sealed cavities using the principle of thin membrane deflection.
- The next step was the mask design and fabrication of the proposed design which was successfully accomplished. Firstly, a successful optimization of the patterning and the subsequent lift-off process of the Cu-Nanopaste for obtaining a high aspect ratio, and well-defined patterns of the Cu-Nanopaste on the wafer with minimal residue.
- A die-level and multi-die-level bonding study at various temperatures and pressures was done for the investigation of hermeticity using Copper NP as the seal ring material. Following this, the hermeticity characterization of the vacuum-sealed samples was carried out via leak rate testing, and the measurement of absolute encapsulated pressure using the thin cap deflection method.
- Further, bond shear testing was followed by fracture analysis and SEM imaging, and EDX characterization to investigate the nature of bonding, finally followed by cross-sectional analysis.

In this research work, we have successfully demonstrated the hermetic sealing of a microcavity using nano-copper paste for the first time in literature with a sealing ring dimension as small as 8μm. The hermetic sealing showed excellent stability over time which was confirmed by the leak rate evaluation, with no discernible leaks observed over a period of 48 days. Moreover, multi-die level hermetic sealing was also demonstrated. The bond shear testing and the subsequent failure analysis revealed excellent adhesion of the nano-copper paste to the gold layer and hence excellent bond strength. With this, we have resolved our research goal of demonstrating hermetic sealing using copper nanoparticle paste. However, wafer-level hermetic sealing could not be attained in this study.

6-2 Recommendations for Future Work

- Die misalignment was found to be one of the major causes of sealing failure. Therefore, an automatic pick and place tool or an automated die-aligning system could be used to accurately gauge the vacuum sealing yield of the bonding approach.
- It was observed that the encapsulated pressure inside the cavity was higher than the pressure it was bonded at. Therefore the usage of getter material could be investigated for the improvement in the vacuum level.
- To more accurately gauge the vacuum inside the cavity, more accurate vacuum level characterization methods like Residual Gas Analysis could be used.
- An active device like a Q-resonator or a Pirani gauge can be fabricated with this sealing method to investigate the influence of this method on their performance.

- The process of patterning could be automated to get more uniform profiles and more well-defined structures of the nano-Cu seal ring.
- The reliability of the nano copper sintering-based hermetically sealed bond can be evaluated via reliability tests like thermal shock, humidity, and mechanical shock testing.

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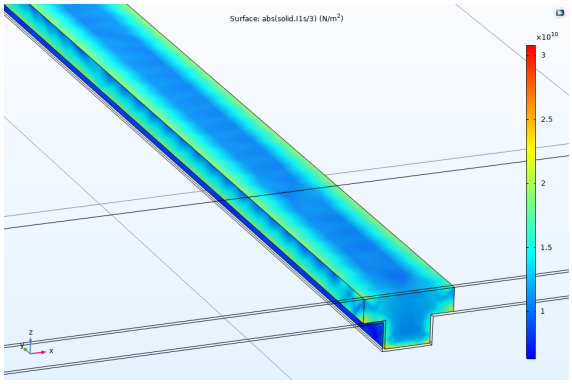
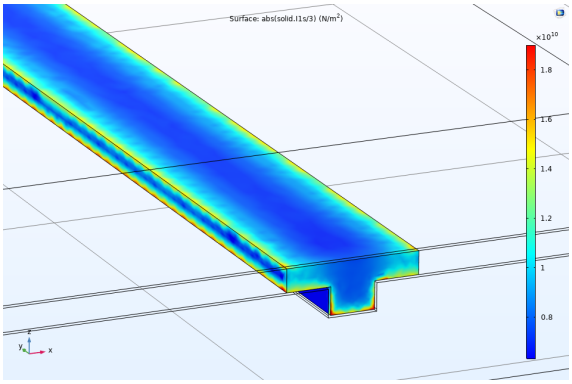
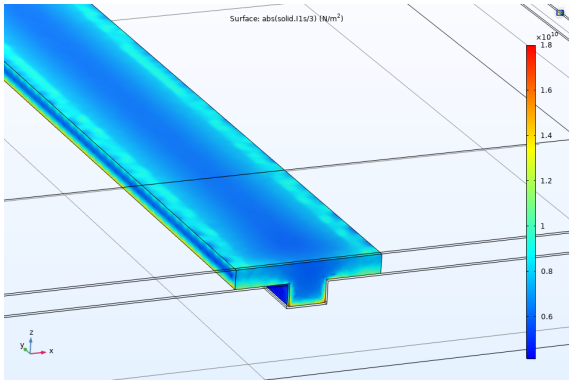
Appendix A: Solid Plot of Volumetric Pressure on seal ring for various groove-based designs.



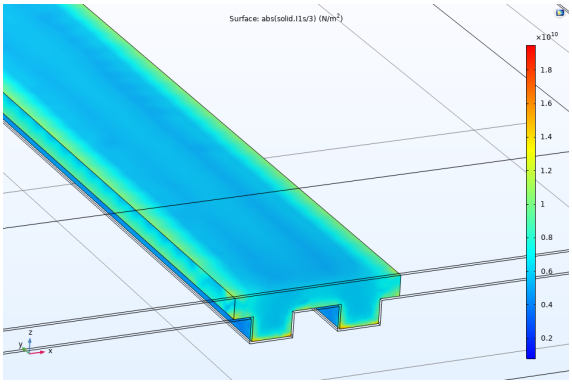
(a) G1-O2 Design (8 μm)



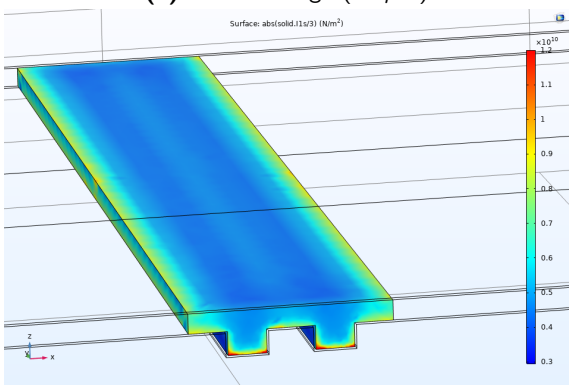
(b) G1-O4 Design (12 μm)



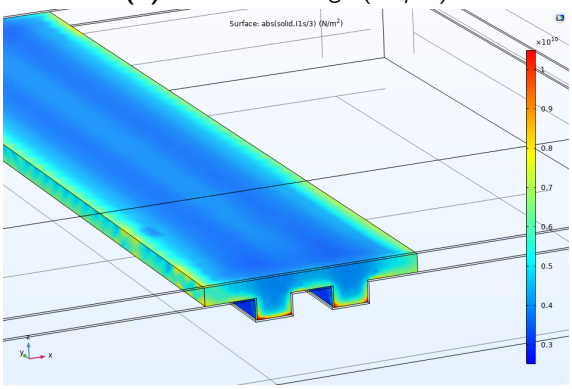
(c) G1-O6 Design (16 μm)



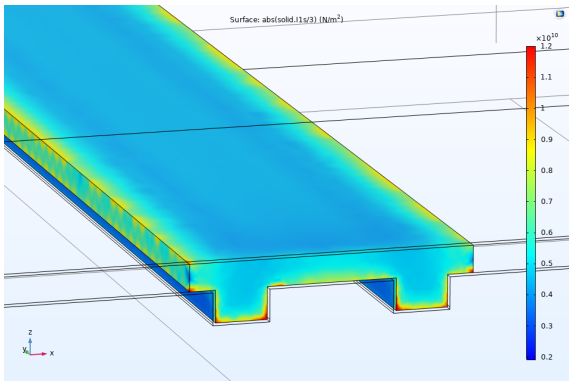
(d) G2-O2-D5 Design (17 μm)



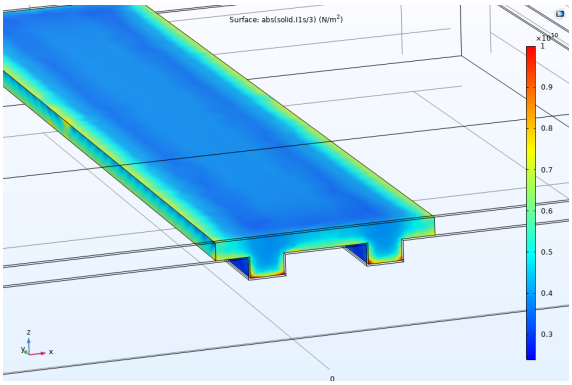
(e) G2-O4-D5 Design (21 μm)



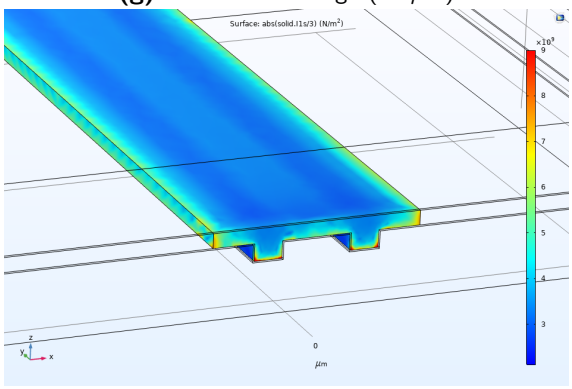
(f) G2-O6-D5 Design (25 μm)



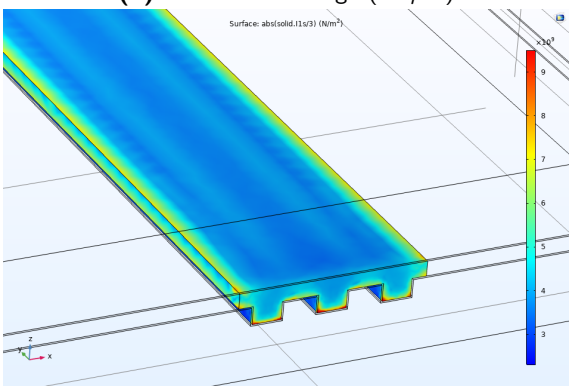
(g) G2-O2-D10 Design (22 μm)



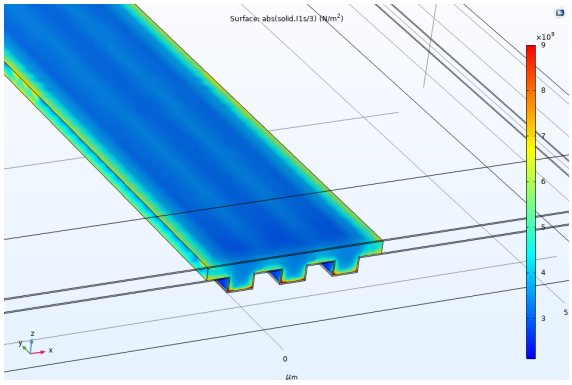
(h) G2-O4-D10 Design (26 μm)



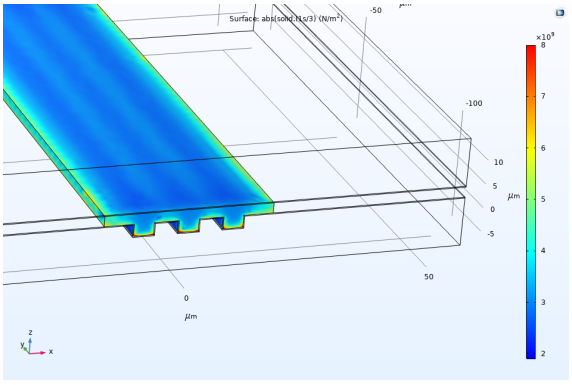
(i) G2-O6-D10 Design (30 μm)



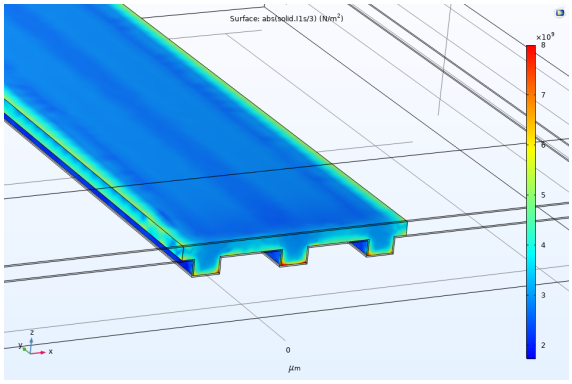
(j) G3-O2-D5 Design (26 μm)



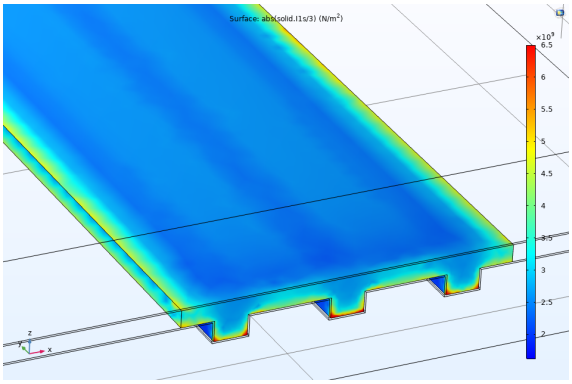
(k) G3-O4-D5 Design (30 μm)



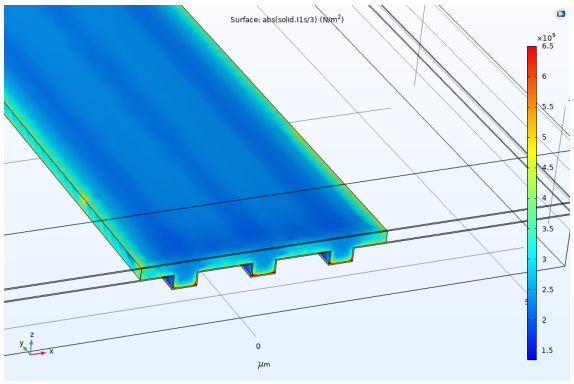
(l) G3-O6-D5 Design (34 μm)



(m) G3-O2-D10 Design (36 μm)

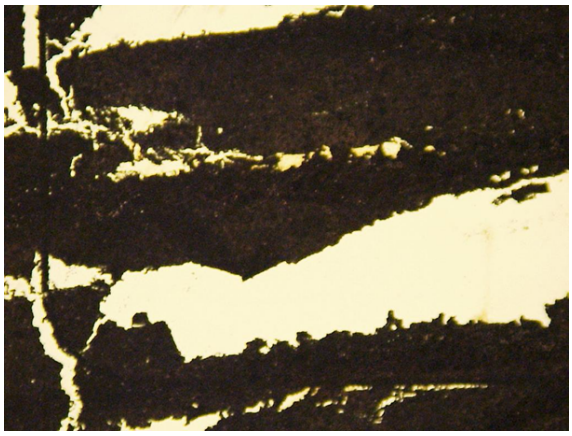


(n) G3-O4-D10 Design (40 μm)

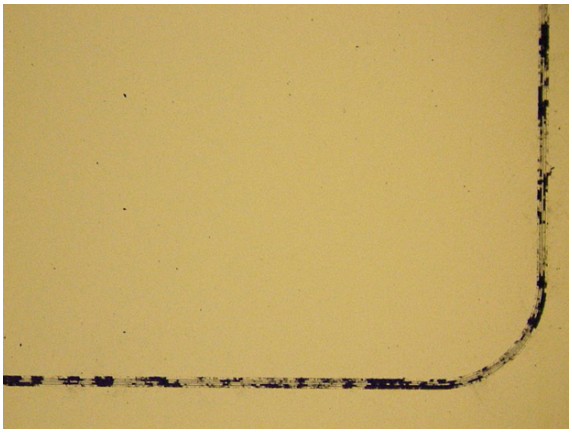


(a) G3-O6-D10 Design (44 μm)

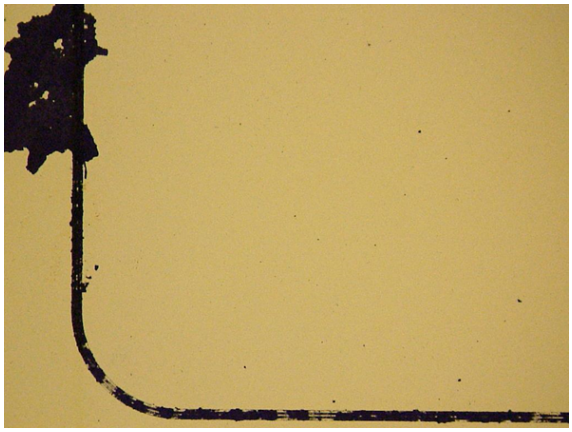
Appendix B : Nanoparticle Lift-Off Optimization



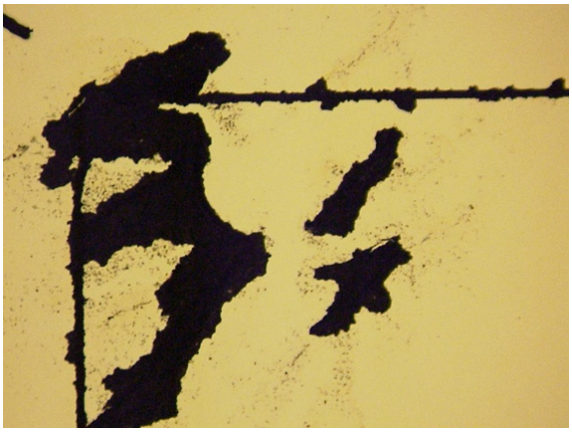
(a) Room Temperature Acetone bath for 120 seconds with no agitation.



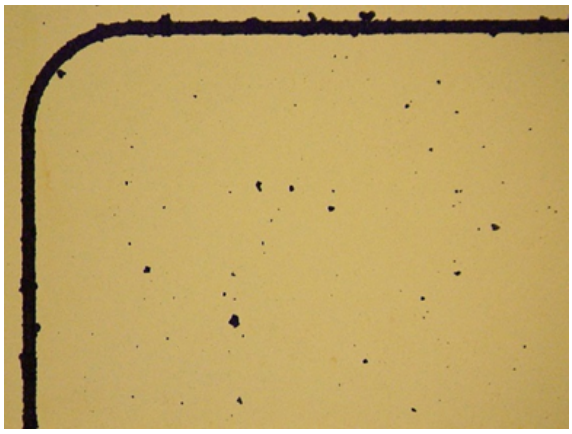
(b) 25°C Acetone bath for 40 seconds with 40 seconds of ultrasonic agitation.



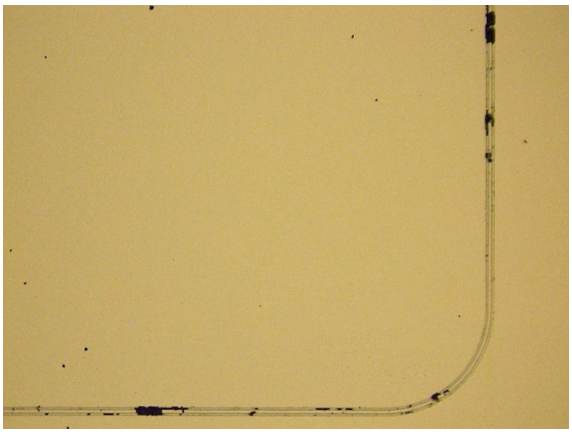
(c) 25°C Acetone bath for 40 seconds with 30 seconds of ultrasonic agitation.



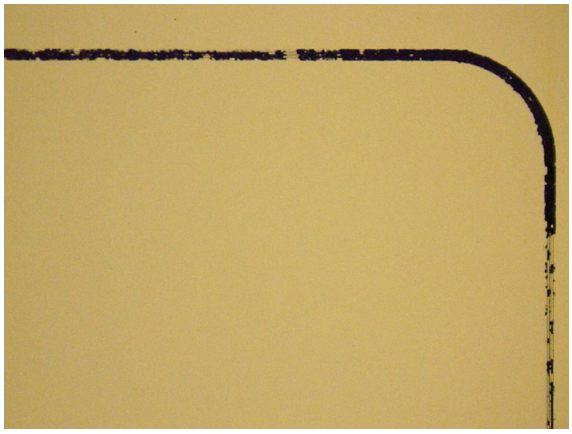
(d) 25°C Acetone bath for 30 seconds with 30 seconds of ultrasonic agitation.



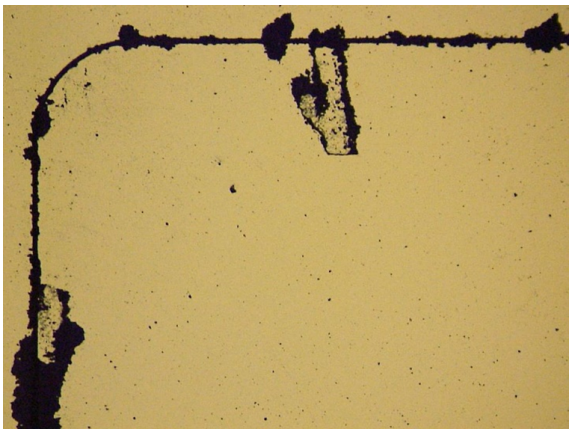
(e) 35°C Acetone bath for 30 seconds with 10 seconds of ultrasonic agitation.



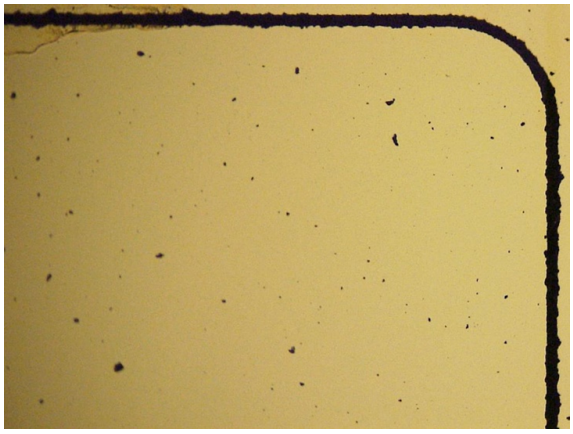
(f) 25°C N-Methy1-2-pyrrolidone (NMP) bath for 60 seconds with 15 seconds of ultrasonic agitation.



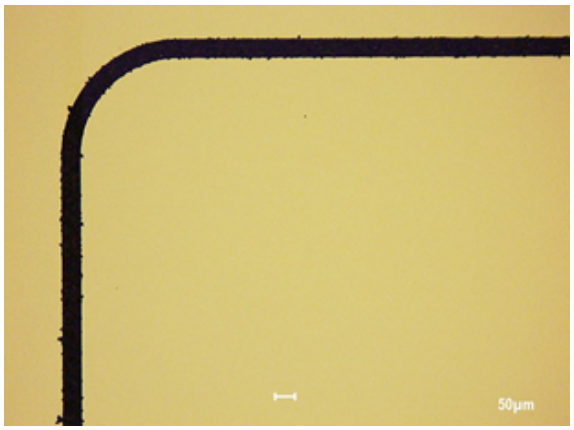
(g) 25°C N-Methy1-2-pyrrolidone (NMP) bath for 60 seconds with 10 seconds of ultrasonic agitation.



(h) 50°C N-Methy1-2-pyrrolidone (NMP) bath for 120 seconds with no ultrasonic agitation.



(i) 80°C N-Methy1-2-pyrrolidone (NMP) bath for 60 seconds with no ultrasonic agitation.



(j) 80°C N-Methy1-2-pyrrolidone (NMP) bath for 120 seconds with no ultrasonic agitation and the sample tilted downwards.