High-Efficiency Dual Transistor Base Drive Circuit Based on the Cuk Converter Topology

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Abstract—**A dual transistor base drive circuit that unifies all important functions is described: on-state base current power supply for two power transistors, off-state negative $U_{be} = -5$ V base-emitter voltage, overcurrent and short circuit protection scheme based on saturation voltage, and on- and off-state monitoring circuits. The unit provides two base drive outputs using a single switching converter. It can be used to control two individual power transistors in different inverter configurations, e.g., common emitter or bridge configuration.**

Introduction

THE PATH of semiconductor development leads almost every day to more and more powerful switching components. From the viewpoint of driving powerful components, the most attractive choices are MOSFET's and IGBT's because of the low driving power level. For applications such as high-power, high-frequency, and low-input voltage, one great shortcoming of MOSFET's and IGBT's is remarkable. High collector-emitter saturation voltage decreases the total efficiency of the converter owing to the high power losses during the on state. In systems of medium power range (typically 30–50 kVA), the input current could be on the order of kiloamperes in dc/ac converters fed from a low-voltage battery. Typical applications are mobile and telecommunication uninterruptable power supplies or power converters fed from photovoltaic arrays or other renewable energy sources [4], [5]. Switching components having low collector-emitter saturation voltage like high power bipolar transistors and ac-compensated Darlington configurations [1]–[3] offer advantages in this respect. Using the ac-compensated Darlington configuration gives as good results as a discrete bipolar transistor [1] having a very low saturation voltage ($U_{cesat} = 0.2$–0.4 V) but a more expensive solution. The use of high-power bipolar transistors requires a high-power and high-efficiency base drive unit.

Structure of the Dual Transistor Base Drive Circuit

The structure of the base drive circuit is presented in Fig. 1. The heart of the driver stage unit is a Cuk converter having an integrated magnetic structure and zero ripple input and output conditions [6]. The experimental circuit is designed for driving two Darlington modules (Mitsubishi QM300HA-H, $I_c = 300$ A and $U_{ce} = 1000$ V). The required base saturation current in this case is $I_{bsat} = 4$ A. The Cuk transformer and its integrated input and output filter inductances is constructed for about 30 W base drive power. Approximately, one third of the total power is used for the base current supply, and the rest is used for the power supply of the protection circuits of the two secondary sides. The same converter supplies galvanically insulated driving logic circuits. The 250-kHz switching frequency of the Cuk converter enables a very compact design of the transformer and input and output filter capacitors. For the prototype design, a small E-core Siemens EF-16 was used; it has an effective magnetic cross section $A = 20$ mm^2, which represents the only magnetic element of the dual transistor driver unit.

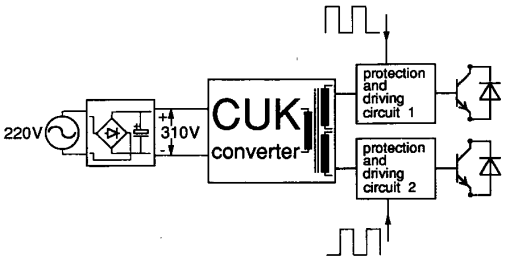

Fig. 1. Structure of the dual driver.

The input power supply $U_i = 310$ V dc is directly obtained from the 220-V ac mains by way of rectification and filtering. It is also a conceptual adventage that no additional power supply units are required. Only a low-power ± 15 V voltage source is required to supply the 250-kHz PWM signal generator on the primary side. This generator controls the MOSFET switch.

Representation of the Dual Transistor Base Drive Circuit

The circuit diagram of the dual base drive unit is presented in Fig. 2.

It is a merit of the Cuk converter topology that it enables zero ripple at the input and output terminals. Hence, no additional input and output filters are needed. Only a small capacitor of $C = 22$ nF is paralleled to the high-voltage input. The PWM signal ($f = 250$ kHz, duty cycle up to

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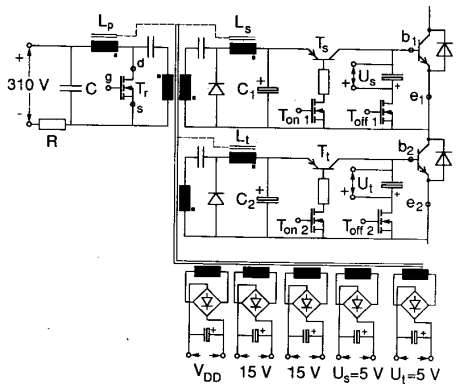

Fig. 2. Power circuit.

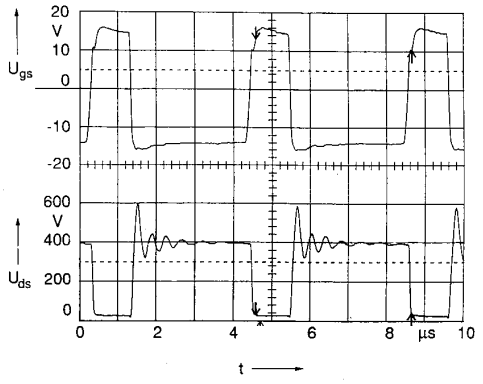

Fig. 3. Gate voltage and drain-source signal of the MOSFET Tr.

$D = 0.3$) is generated in a simple way using a feedback signal taken from the shunt resistor R on the primary side to control the base current on the secondary. The gate signal of T_r and the waveform of the drain-source voltage of the same transistor are shown in Fig. 3.

As the transition time during turn off of the MOSFET devices is very short, the current rapidly changes direction in the primary of the transformer (the current in the primary inductance L_p is supposed to be constant) [7]. This gives rise to induced voltages in stray inductances of the wiring. Under normal conditions, these voltages can assume the order of several hundred volts. The induced voltages add to the voltage stress of a device at turnoff and hence, must be reduced to a minimum. This is achieved by reducing the stray inductances of the wiring. The critical commutation loops of the printed circuit board are designed to provide a minimum leakage flux area. In Fig. 3, voltage spikes of the drain-source voltage U_{ds} reach $U_{ds\,peak} = 200$ V. The basic principle of the Cuk converter is given in Fig. 4 [6].

Two secondary circuits of the Cuk converter supply the base current to the two power transistors alternately. As seen from the primary side, the load appears to be constant, and no additional input voltage stresses exist. Experimental base current waveforms delivered at the output of the base drive circuit to two power darlingtons QM300HA-H are depicted in Fig. 5. The corresponding base-emitter voltage waveform is shown in Fig. 6.

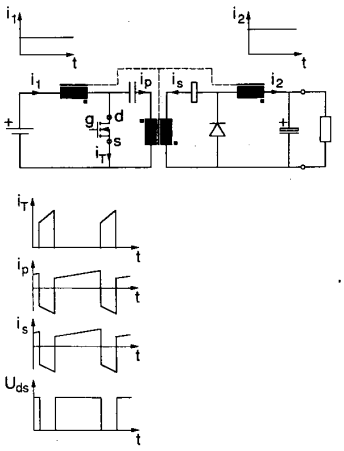

Fig. 4. Basic principle of the Cuk converter.

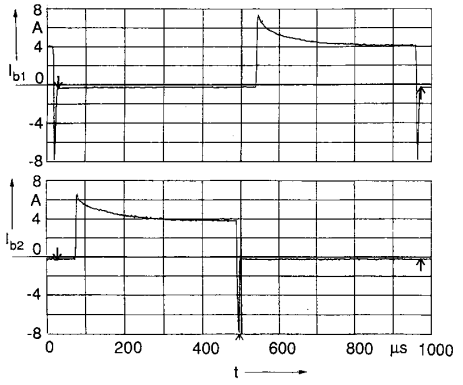

Fig. 5. Base current waveform of the power transistor.

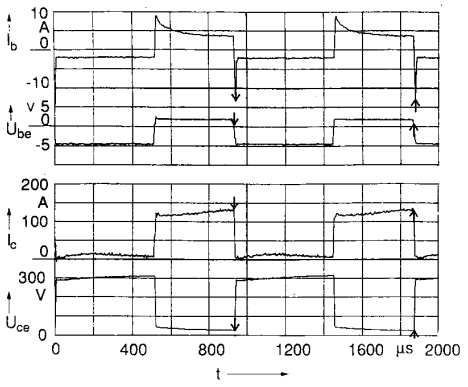

Fig. 6. Base current Ib, base-emitter voltage Ube, power transistor collector current Ic, and collector-emitter voltage Uce.

Using only miniaturized components, high-amplitude base currents are achieved, having a steep slope of the rising edge as well as a steep falling slope of the trailing edge. Fig. 7 is an oscillogram of the magnified rising slope of the base current. The current slope is $di_b/dt = 1.6$ A/µs.

The required turn-on overcurrent peak is obtained in a very simple way. Using a p-n-p bipolar transistor T_s (or T_t respectively), the base current is switched on or off (Fig. 2).

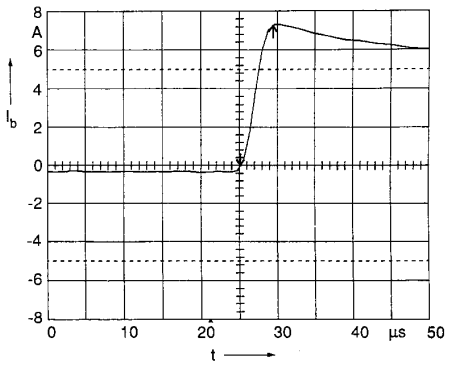

Fig. 7. Magnified rising slope of the base current.

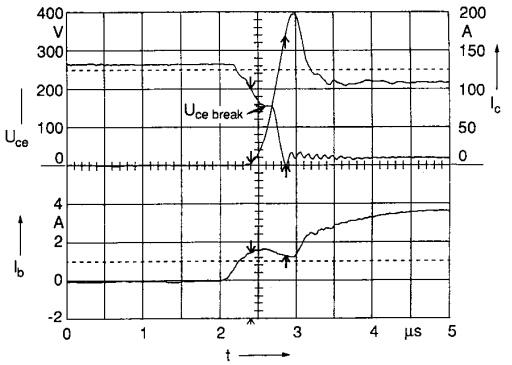

Fig. 8. Magnified turn-on waveforms.

In the moment of turn off, accumulated energy in the secondary inductance L_s (L_t) flows into the capacitor C_1 (C_2), raising its voltage and protecting the transistor T_s (T_t) from overvoltage stresses (a kind of a snubber). This energy is stored in the capacitor until the beginning of the next on state of T_s (T_t). The capacitor then discharges its energy, producing a high current spike. This provides very fast base junction charging and, hence, fast turn on of the power transistor.

The oscillogram of the power module QM300HA-H turn-on process (in the experimental half-bridge configuration device) is shown in Fig. 8. The I_c peak = 200 A current spike is the reverse recovery current of the freewheeling diode incorporated in the power module. High di_c/dt during reverse recovery time causes a voltage drop over the stray inductances of the wiring circuits, which results with a collector emitter voltage breakdown at $U_{ce\ break}$ = 150 V (Fig. 8):

$$U_{cebreak} = U_{ce} - L_p * \frac{di_c}{dt} \qquad (1)$$

where L_p is the stray inductance of the wiring.

The complete sequence of switchings of the power transistor is presented in Fig. 6.

The turn-off base-emitter voltage waveform U_{be} and associated base power module's current I_b of one power stage is shown in Fig. 9. During the off state of the power transistor, MOSFET T_{off1} (T_{off2}) is turned on (Fig. 2); hence, the base is supplied with a negative voltage $U_{be} = -6$ V.

During the first 5 µs after turnoff, the base charge is intensively extracted (negative $I_b = -9$ A current spike). The base voltage during this period of time is equal to zero (Fig. 9), and the recombination in both p-n junctions of the switching device is regular. No collector current tail is noticeable. Fig. 10 is an oscillogram of the turn-off process, illustrating storage time of the darlington power module.

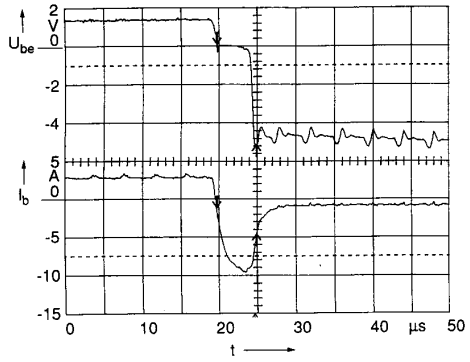

Fig. 9. Magnified waveforms at turnoff.

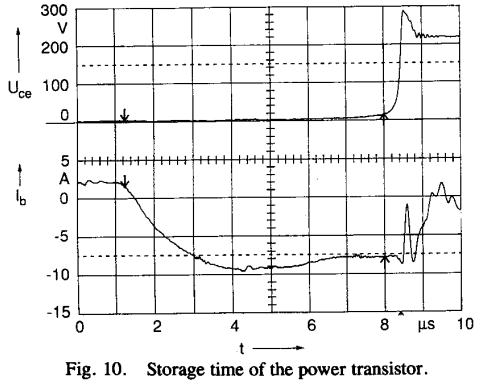

Fig. 10. Storage time of the power transistor.

Driving and Protection

The driving and protection circuits are powered by the converter itself. The scheme of one of those circuits is shown in Fig. 11.

The logic control signals are transmitted through optocouplers having a very high common mode rejection value (HCPL221, 5000 V/µs). The collector-emitter saturation voltage of the power transistor $U_{ce\ sat}$ is sensed for overcur-

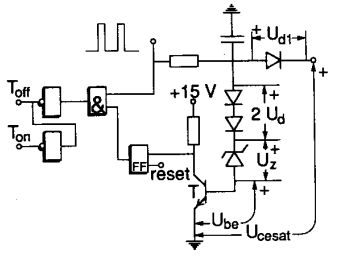

Fig. 11. Driving and protection circuit.

rent and short circuit protection. It is monitored using a high voltage diode $d1$, as is shown in Fig. 11.

$$U_z = U_{cesat} + U_{d1} - 2*U_d - U_{be}. \quad (2)$$

When the collector-emitter saturation voltage $U_{ce\ sat}$ reaches a certain level, which is determined by a Zener diode threshold voltage, transistor T turns on, and a fault signal is stored in a Flip-Flop (FF) circuit. The time delay of the protection is defined by the time constant of the RC filter, which is also depicted in Fig. 11. Hence, the protection can be unsusceptible to short over current events, which is not really dangerous for the power switch.

The fault signal blocks the AND circuit (&), which causes durable turn off (negative base-emitter bias of the power switch), and the power transistor is turned off. Reset signal again enables normal function of the device.

The Cuk Integrated Magnetics Circuit

ac Conditions in the Core

An $A = 20\ mm^2$ effective magnetic cross section E core is used for the integrated magnetics design [6]. One input and two output filter inductances are wound on outer legs. The primary winding and seven secondary windings are located on the central leg. This technique permits a small air gap in the core and achieves dc zero ripple conditions in input and output inductances. A simplified magnetic circuit is presented in Fig. 12.

The magnetic circuit can be represented by a reluctance equivalent circuit model shown in Fig. 14. The leakage flux ϕ_l and the associated leakage inductance L_l of the center winding, because it is the most important one, should be taken into account. The leakage flux ϕ_l could be physically represented through an additional parallel magnetic branch to the center winding with an air gap l and corresponding leakage reluctance R_l. The outer legs are represented only by the respective reluctances R_x and R_y of the air gaps x and y because the reluctances of magnetic paths are negligible. The reluctance model is depicted in Fig. 13.

We have

$$R_x = \frac{x}{\mu_o * A}$$
$$R_y = \frac{y}{\mu_o * A}$$
$$R_l = \frac{l}{\mu_o * A} \quad (3)$$

where x, y, l are the respective air gap lengths, and A is the core cross section.

Let us assume the ripple input and output current of the dc chokes N_1 and N_2 to be zero; then, the corresponding ampere-turn generators $N_1 * i_1$ and $N_2 * i_2$ could be shorted because $d\phi_1/dt = 0$ and $d\phi_2/dt = 0$. Hence, a very simple ac model is obtained (Fig. 14).

Considering Fig. 12, we have from Faraday's law

$$v_1 = N_1 * d\phi_1/dt \quad (4)$$

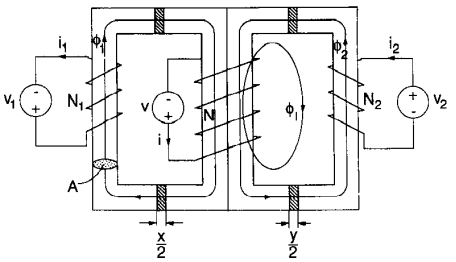

Fig. 12. Simplified magnetic circuit.

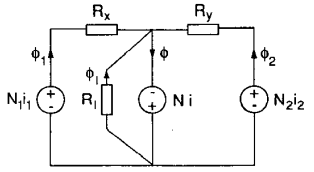

Fig. 13. Reluctance equivalent circuit model.

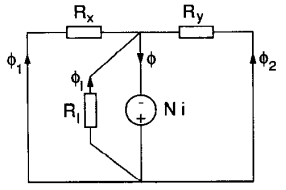

Fig. 14. ac reluctance model.

$$v = N * d\phi/dt \quad (5)$$
$$v_2 = N_2 * d\phi_2/dt \quad (6)$$

where N_1 and N_2 are turn numbers of the outer legs' inductances winding, respectively, and N turn numbers of the central leg winding.

For simplicity, we assume

$$N_1 = N_2. \quad (7)$$

Hence

$$\phi_1 = \phi_2 = \phi_0/N_1; \quad \text{where } \phi_0 = \phi * N. \quad (8)$$

Using the loop equation

$$R_x * \phi_1 = R_l * \phi_l \quad (9)$$

and the node equation

$$\phi_l = \phi - \phi_1 - \phi_2 = \phi_0 * (1/N - 2/N_1) \quad (10)$$

we have

$$R_x/N_1 = R_l * (N_1/N - 2)$$
$$x = l * (N_1/N - 2)$$
$$y = l * (N_2/N - 2). \quad (11)$$

The most interesting case for the practical implementation is given by

$$N_1/N = 3. \quad (12)$$

Then

$$x = y = l. \quad (13)$$

Hence all gaps are equal, and there is no need for fine tuning. The parameter l is called the "leakage parameter" and can be obtained from the center winding leakage reluctance by measuring the leakage inductance of the center winding [6]:

$$l = \mu_o * A * R_l \tag{14}$$

$$R_l = N^2 / L_l \tag{15}$$

$$l = (\mu_o * A * N^2) / L_l. \tag{16}$$

dc Conditions in the Core

From the dc saturation conditions, the following equations can be found (Fig. 13):

$$\frac{B_m}{\mu_o} \geq N * I * \left[\frac{1}{x} + \frac{1}{l}\right] + N_1 * I_1 * \frac{1}{x} \tag{17}$$

$$\frac{B_m}{\mu_o} \geq N * I \left[\frac{1}{y} + \frac{1}{l}\right] + N_2 * I_2 * \frac{1}{y} \tag{18}$$

$$L = \mu_o * A * N^2 * \left[\frac{1}{2*x} + \frac{1}{2*y} + \frac{1}{l}\right] \tag{19}$$

where

- B_m maximal allowed induction in the core
- A core cross section
- L inductance of the central winding
- μ_o permeability of the vacuum.

Design Equations of the Transformer

From the ac and dc condition, in the core final, general design equations can be evaluated. The most practical structure of the core is one with equal gaps $x = y$.

If

- L desired main inductance of the transformer
- I_1 input inductor current
- I current through transformer
- l estimated leakage parameter (2–4 mm)
- B_m maximum induction in the core
- A core cross section

are known and $N, N1, x$ are unknown and if we also assume $N_1 = N_2$ and $I_1 = I_2$, then

$$N = \frac{L * (I + 2 * I_1)}{B_m * A} \tag{20}$$

$$L_1 = \frac{N^2 * \mu_o * A}{l} \tag{21}$$

$$x = \frac{L_1}{L - L_1} * l \tag{22}$$

$$N_1 = \frac{L}{L - L_1} * 2 * N \tag{23}$$

where L_l is the leakage inductance of the transformer.

Practical Implementation

The Cuk transformer with multiple secondary sides and integrated inductances is designed for 30-W power.

- Siemens EF-16 core is chosen with cross section $A = 20$ mm^2
- primary transformer winding $N' = 60$, $S_{cu} = 0.1$ mm^2
- two secondary windings $2*(N'' = 3)$, $S_{cu} = 0.4$ mm^2
- input inductor $N_1 = 146$, $S_{cu} = 0.1$ mm^2
- two output inductors $2*(N_2 = 8)$, $S_{cu} = 0.4$ mm^2
- two windings for 15-V power supply of secondary side control and protection units $2*(N_{34} = 3)$
- two windings for 5-V negative supply for turn-off power modules $2*(N_{56} = 2)$
- one winding for external power supply $N_7 = 6$.

Conclusion

The concept of a dual transistor base drive circuit using the Cuk switching regulator topology enables the low volume construction of a high-efficiency base drive unit for a high-power transistor inverter bridge leg. The circuit is powered from a common dc rail. The base current waveforms are characterized by steep slopes and an overcurrent peak at turn on. The scheme comprises overcurrent, short-circuit protection, and a switching state monitoring circuit. It can be used for the direct base drive control of discrete high-power transistors in high-efficiency power converters, especially for renewable energy schemes. This device is accomplished and experimentally tested as a half bridge converter driver. Switching devices were two Darlington power modules Mitsubishi QM300HA-H, $I_c = 300$ A, and $U_{ce} = 1000$ V. All oscillograms in the paper depict real working conditions of the device.

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