Cryogenic DAC for the Biasing of Spin Qubits

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Exploration and design of a scalable DC Biasing Solution

by

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Abstract

Disruptive changes in the fields of cryptography and quantum chemistry can be achieved through quantum computing, as specific computations can be sped up significantly. Thousands to millions of qubits are required to perform these computations, illustrating the need for large quantum computers. These qubits must be cooled to cryogenic temperatures in order to operate. Currently operations on few qubits can be done, these are commonly controlled with room temperature equipment. However as the number of qubits becomes larger, scalable and integrated electronics is required to reduce the interconnect. This has promoted research in cryogenic electronics that can be located close to the qubits.

This thesis presents a low power, scalable cryogenic DC biasing solution for the biasing of spin qubits. The presented DC-DAC has been implemented in the Intel 22-nm finFET process. Unlike conventional DACs, the designed DC-DAC periodically generates all possible voltages in the full scale output voltage range, and drives a multiplexer that connects a sample and hold capacitors when the right bias voltage for the electrode has been generated. The DAC is able to achieve a high resolution of 16 bits with low noise performance by using an offset-compensated switched capacitor integrator. By offering a DC input to the integrator the full scale output voltage range can be generated, while using the offset-compensated switched capacitor integrator allows reduction of offset and 1/f noise which are expected to degrade at cryogenic temperatures.

The DC-DAC is designed to meet a large voltage output range of 3 V, which breaks compliance with the nominal 1.8 V compliance of the thick oxide transistors in the process. While it is possible to put larger voltages over the transistors, it is currently unknown how this will affect the reliability and behavior of the thick oxide transistors. Therefore, a two-stage amplifier has been implemented where the second stage uses a supply of 3.6 V. The voltage compliance in the second stage is guaranteed through cascode transistors that are dynamically biased by additional DACs. As the addition of the second stage of the amplifier and coarse DACs introduce another voltage domain, additional circuitry such as logic level shifters, diode stacks and cascode transistors have been added to ensure that voltage compliance is throughout the entire DAC.

The DC-DAC achieves a LSB step of 45.1 μV, a voltage output range of 3 V, integrated noise of 17 μV_{rms} and dissipates a total of 187 μW while not consuming more than 0.078 mm^2. The high resolution, large voltage output range and low power of the DAC enable integration of the DAC with the qubits, paving the way for scalable quantum computers.

Acknowledgments

The past 9 months have been a wild ride, a pandemic has taken over the world and this has caused a lot of uncertainty and changed the pace of our society. It has made me wonder multiple times whether what I am working on can help make a difference and help shape a better future. I am convinced that quantum computing has a place in this future, as I believe it will allow better research. I dearly hope that this thesis can be an useful contribution to the first practical quantum computers.

The thesis presented here is not only the product of my work and ideas, but also the result of many discussions and a lot of feedback. Therefore some acknowledgments are in place. First and foremost, I would like to thank Fabio Sebastiano, for the supervision, fruitful discussions and critical questions. Furthermore I would like to thank the Coolgroup, throughout my thesis they have supported me both academically as socially through interesting questions and discussions. Especially a word of appreciation to Job and Jiang, we have been in the 22nm tape-out together as a team and without the two of you I do not think I would have made the finish line. Of course more thanks are in place to my friends and family, all of which have helped me become the person I am today, while also being a mental support for me during these volatile and stressful times.

Luc Enthoven
Delft, 04-09-2020

Contents

1 Introduction

This thesis covers the implementation of a low power, low noise and high resolution cryogenic Digital to Analog Converter (DAC). The presented DAC is used for creating the DC voltages that are used for the biasing of spin qubits in a quantum computer. As the DAC performs the DC biasing, the designed DAC is also referred to as the DC-DAC. In this thesis the DC-DAC is combined with a multiplexer that has hold capacitors at the output channels, which are used to sample and hold the DC bias voltages. Both the DC-DAC and multiplexer are designed to operate at cryogenic temperatures close to the qubits. The objective of the thesis is to analyze and develop a scalable solution for the biasing requirements of spin qubits. In order to account for scalability, the thesis focuses on developing a solution that has a lower power per qubit.

First, some aspects of quantum computers are explained in this chapter, including why it is of interest and illustrating why a scalable structure is needed. Then the interest in spin qubits is discussed and how they can be implemented is touched upon. Cryogenic electronics is introduced and some changes in device behavior compared to room temperature is listed. An overview is presented on available literature on cryogenic DACs and ADCs, in order to grasp what is possible with cryogenic electronics and what the current state of the art is. The chapter is concluded by introducing the structure of the rest of the thesis.

1.1. Quantum Computing

Quantum computing has gained increased interest over the last few years and is deemed to be a promising new technology. It is predicted that quantum computing will allow for exponential speedup in algorithms that would otherwise require hundreds of years to complete [1]. Because of this, there is an increased interest towards quantum computing from a wide range of companies such as Intel, IBM and Google, which fund large research efforts in order to speed up the timeline towards the first practical quantum computers. A first milestone has been achieved in the past year, when an algorithm achieved significant speedup when running on a quantum computer was performed by Google in the publication of Arute et al [2].

Quantum computing is based on performing calculations with quantum bits (qubits), which draws the analogy with classical computing performing computations with classical bits. The primary difference between qubits and classical bits is that, where a classical bit has a discrete value of either 0 or 1, qubits can be 0 and 1 simultaneously, which is a phenomenon known as superposition. In addition, it is possible to entangle qubits, making two qubits dependent on each other's state. Exploiting both superposition and entanglement allows for significant speed up for specific kinds of calculations [3]. A disadvantage of qubits compared to classical bits is that qubits are fragile and do not retain information indefinitely. The time information can be stored is typically correlated to the type and operating temperature of the qubit [4].

Current predictions indicate that quantum computing will allow speedup in relevant applications, such as quantum chemistry problems and complex optimization [5, 6]. However, depending on the algorithm that has to be ran, a large number of qubits is required. This can range from hundreds to thousands or millions of qubits. In addition, a qubit used for computation, also called a logical qubit,

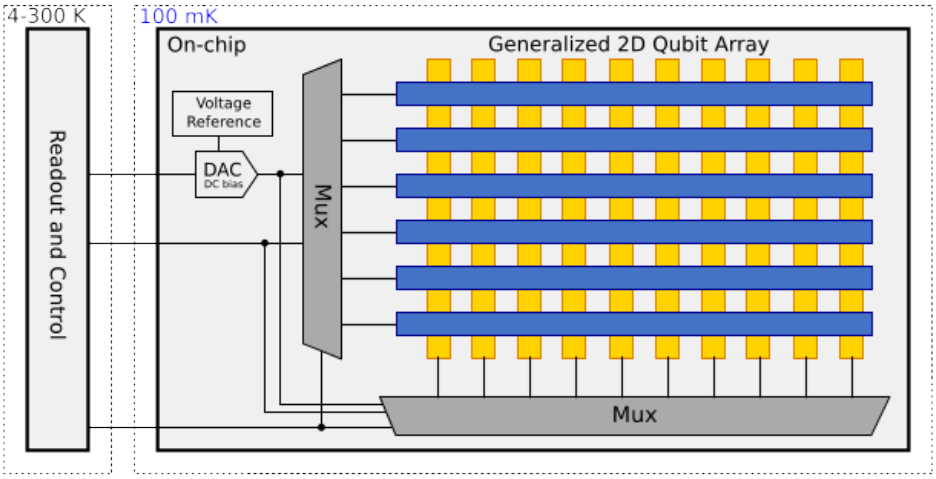


Figure 1.1: System diagram of a Quantum Computer, illustrating the biasing electronics operating at temperatures close to the qubit temperatures (image copied from [12]).

can be encoded in multiple physical qubits to improve fault-tolerance [7]. Using current state-of-the-art qubits, up to 1000 physical qubits may be required for each logical qubit [8]. This illustrates the need for scalable qubit systems, also promoting development towards integrated quantum controllers which have error correction embedded [9]. In this thesis, a scalable DC biasing solution is presented that can be used to create spin qubits [10].

Qubits can be implemented in various ways by exploiting certain physical phenomena. This has given rise to different types of qubits based on spin, ion traps, superconduction and more [3]. Generally, these qubits require operation at cryogenic temperatures below 4 K. At higher temperatures, thermal energy can make it difficult to encode and perform computation on the qubit in a robust and reliable manner. In addition to cryogenic temperatures, qubits require control electronics to perform operations and readout. The amount of interconnect required to connect the qubits to current room-temperature control electronics becomes unpractical when scaling to millions of qubits, as the amount of wires scales accordingly. Therefore, proposals have been made to integrate the control electronics at cryogenic temperatures to reduce the amount of interconnect required as illustrated in Figure 1.1 [6, 11]. This has stimulated research towards electronics operating at cryogenic temperatures in the operating range of 0-4 K.

1.1.1. Spin qubits

In this project, the target quantum technology are spin qubits. Spin qubits allow encoding of the state of a qubit in either the spin of a one single electron or in the spins of multiple electrons [13]. Spin qubits benefit from long coherence times, i.e. they are able to preserve the state of the qubit for a large amount of time. In order to trap single or few electrons, quantum dots are used. These quantum dots typically consist of 3-5 electrodes, that require accurate biasing in order to trap a single or few electrons [14].

Spin qubits are promising, as they can be implemented in different semiconductor technologies such as SiMOS or GaAs [4, 15]. This allows the quantum technology to benefit from the reliability and scaling developed in semiconductor chip fabrication. Using semiconductor technologies also allows for the integration of control electronics with the qubits. Predictions have been made that through semiconductor scaling, a million of qubits can be fit on a chip of 151mm^2 [16].

As scaling towards million of qubits is desired, research has been done towards scalable structures in which the qubits can be implemented. These structures include 2-dimensional arrays [16] or cross-bar networks [17]. These scalable structures aim to resolve interconnect issues that arises when the number of qubits increases.

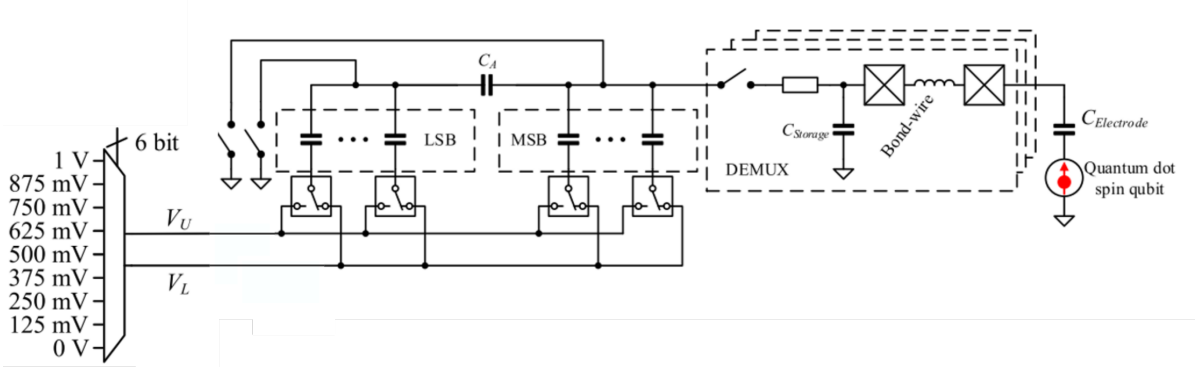


Figure 1.2: The R-DAC - C-DAC implemented by Vliex et al. used to bias GaAs spin qubits (image reproduced from [29]).

1.2. Cryogenic Electronics

Semiconductor technologies and devices are often characterized down to -55°C, which is the lower limit of the industrial operating range [18]. Cooling down the electronics further may cause unknown or undesired behavior. For instance, measurements of different devices has illustrated that silicon bipolar transistors do not operate at cryogenic temperatures or that the resistivity of certain resistors can increase significantly as the temperature becomes lower [6]. MOS devices have been shown to work at cryogenic temperatures, though they suffer from increased threshold voltages, a change in mobility and increased mismatch [19, 20]. Technologies with a large feature size have shown hysteresis in the current/voltage characteristic of MOS transistors at cryogenic temperatures, while in technologies with smaller feature size this has been found absent [21].

Designing electronics for operation at cryogenic temperatures requires additional attention from the designer compared to room temperature. Characterization of the devices that are to be used must be done such that it is known which devices function properly and which abnormalities can be expected. Designing cryogenic electronics requires additional awareness of the above mentioned effects to avoid malfunctioning circuits at cryogenic temperatures. Validation and simulation at cryogenic temperatures can often not be done as device models for cryogenic temperatures are not available, not complete or not mature as the field of application is much newer.

1.2.1. Cryogenic Data Converters

Most literature present on cryogenic DACs is focused on the AC excitation required for performing qubit operations. This is illustrated by publications on current DACs (I-DACs) operating close to or at cryogenic temperatures[22–25]. In these DACs, the focus is on the INL and DNL performance, as the linearity tends to degrade when moving to cryogenic temperatures[9].

The literature presented on cryogenic ADCs are applied in different domains such as infrared detectors and qubit readout. Implemented structures for these ADCs are a Sigma Delta ADC[26], TDC[27] and a flash converter[28]. This illustrates that functionally speaking, most known data converter architectures can be implemented to operate at cryogenic temperatures and the basic building blocks such as comparators, inverters and integrators can be used.

Thus far, not much literature is present that focuses exclusively on a scalable qubit biasing solution. One DAC has recently been presented in literature to be used for the biasing of spin qubits implemented in GaAs [29]. The paper presents a 13-bit two stage DAC, which combines a resistive ladder, multiplexer and a C-DAC to generate the bias voltages as illustrated in Figure 1.2. The C-DAC is not buffered resulting in a low power dissipation as no amplifier is present. By not having a buffered output, the channel is only fully biased after multiple conversion cycles. In addition, unbuffered operation causes the output voltage of the DAC becomes load dependent on $C_{storage}$. The two-stage DAC structure is sensitive to parasitic capacitances, which require careful calibration to prevent having large missing step sizes in the voltage output range. With this two-stage DAC, a low power dissipation of 2.7 μW per channel can be achieved at an operating frequency of 3.9kHz, of which most is caused by the digital logic and memory [29].

1.3. Thesis Organization

The thesis is organized as follows: First, in chapter 2 an analysis of the required specifications for the biasing of spin qubits is made, by the end of which specifications for the designed DC-DAC are derived. In chapter 3, modeling of different DAC implementations is done in order to gain insight in how increasing the number of qubits scales with the design of the DC-DAC. chapter 4 presents the implemented DAC including design equations and trade-offs. Afterwards, the implementation of the DAC in the 22-nm finFET technology of Intel is shown in chapter 5 including layout and simulation results. As preparation for the measurements, a preliminary measurement plan and setup is presented in chapter 6. Finally, chapter 7 and chapter 8 present recommendations for future work and the conclusion of the thesis, respectively.

2

Application specifications

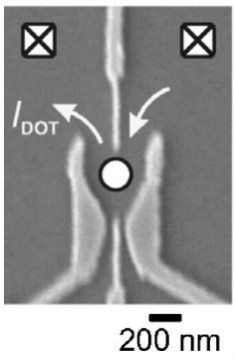
For quantum computation based on spin qubits, single electrons need to be trapped and their spin needs to be manipulated. This chapter first introduces single electron transistors (SETs), in which quantum dots and thus spin qubits can be created. How qubits can be created and manipulated is then briefly introduced. This information is used to derive biasing specifications for the gates of SETs and quantum dots. Afterwards, analysis of additional biasing constraints and other system level considerations for achieving scalability are presented. Finally, an overview of the final specifications is presented and this is compared to the currently used equipment.

2.1. Single Electron Transistors

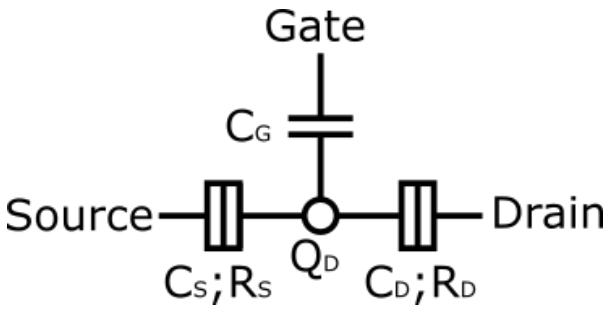
Single-electron spin qubits are qubits where the information is encoded in the spin of a single electron. Therefore, to be able to create a spin qubit, a single electron needs to be trapped. In order to trap a single electron, a single electron transistor is used [4].

A single electron transistor has an equivalent electrical model as shown in (b) of Figure 2.1 which shows a tunnel barrier from the source and drain to point Q_D (the quantum dot, also called the island in literature). There is capacitive coupling between the Gate and Q_D, which allows a gate voltage to increase or decrease the energy level of the quantum dot. The quantum dot Q_D has discrete energy levels, which correlate to the amount of electrons present in the quantum dot. Whenever an energy level is between the energy levels of the source and the drain as shown in b) of Figure 2.2, it allows electrons to tunnel from the higher potential energy to the quantum dot and to tunnel from the quantum dot to the lower potential energy [30]. Whenever tunneling occurs, a current can be measured due to the movement of electrons. A typical layout of a Single Electron Transistor is shown in (a) of Figure 2.1.

In order for a single electron transistor to operate as previously described, it is important that [14]:



(a) Layout of a single Quantum Dot(image copied from [30])



(b) Single electron transistor model [31].

Figure 2.1: Single Electron Transistor

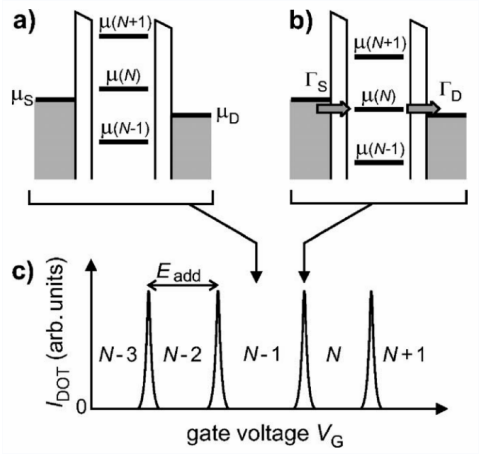


Figure 2.2: a) illustrates the energy level of the quantum dot, b) illustrates the energy levels of the quantum dot when a current can flow. c) illustrates the observable current as a function of voltage for a varying V_G (image copied from [30]).

- The thermal energy is smaller than the charging energy ($k_bT << \frac{e}{C}$), as otherwise electrons would be able to tunnel in and out of the quantum dot due to thermal excitation.
- The tunneling resistance R_t is larger than $\frac{h}{e^2}$ as it is possible for electrons to be in the quantum dot due to the uncertainty principle [32].

A single electron transistor owes its name due to its operation. Figure 2.1 shows that a current is able to flow when the energy level of a single electron being present between μ_s and μ_d, allowing electrons to flow from a high energy state into a lower energy state. C) in Figure 2.2 illustrates how the electron number can be mapped as a function of V_G and I_{dot}. By performing a voltage sweep on V_G, coulomb peaks become visible and it possible to detect how many electrons are present in the island by counting the number of current peaks. Once the coulomb peaks stop, it is clear that no electrons are in the quantum dot and the gate potential for having a single electron in the quantum dot can be found. For example, in a) of Figure 2.2, $(N-1)$ electrons are present in the quantum dot as the potential line of $\mu(N-1)$ is below the potential line of μ_s and μ_d. This allows to determine when only a single electron is present in the quantum dot, which in turn allows creation of a single-electron spin qubit.

2.1.1. Biasing the SET

Single electron transistors contain multiple electrodes, which need independent biasing. The accuracy of the biasing needed is dependent on multiple aspects. First, not all electrodes are required to have a high resolution. Some electrodes are used as shielding and present a potential barrier which prevent the electrons from moving. These barrier electrodes do not require a fine resolution.

For the gate electrode (also referred to as plunger electrode or plunger gate in literature), it is considered that a fine resolution is needed. In section 2.2 the different operations which put constraints on the resolution are explored and a conclusion on the factors affecting the resolution is reached. The biasing levels that map a gate voltage to a number of electrons are not identical for each SET, as there is a dependence on device geometries and capacitive coupling. Therefore, characterizing the Coulomb peaks as seen in c) of Figure 2.2 is required for every device to find the relation between gate voltage and number of electrons in the quantum dot.

2.1.2. Lever Effect

A voltage change in the electrode does not create a 1:1 change in energy in the quantum dot. There is a lever effect present in the electrodes, which means that a large voltage change on the electrodes can cause only a small change in energy in the quantum dot. This is caused by the electrodes creating an electric field in a 2-dimensional plane, causing a capacitive division with the quantum dot. As this is an effect that is caused by geometric properties, the lever ratio will depend on the size and shape of the quantum dot. Interestingly, this also allows for a trade-off. In case the electrode is very close to the dot, a very fine resolution but also a very narrow voltage range will suffice, whereas with an electrode

far from the dot, a larger resolution paired with a larger voltage range is needed. Note that in case of the two scenarios, the latter can be estimated to be more power consuming and less sensitive to noise due to the larger required voltage range.

In section 2.2, formulas are given that help determine the minimum resolution required in order to control the number of electron in a quantum dot. The equations presented in this section do not take into account the lever effect. Logically, it can be assumed that the lever effect does not amplify the energy added to the quantum dot. It is assumed that the lever effect is always lower than 1, such that an increase in gate voltage V_G results in a smaller increase in energy in the quantum dot. If the lever effect is assumed to be 1, the requirements for resolution step on V_G are most stringent. Therefor for determining the minimum required resolution, a lever ratio of 1 is used.

2.2. Qubit Operating Condition

Now that the structure of the single electron transistor is introduced, the next domain of interest is how electrons can exactly be trapped and how operations on these electrons can be performed such that computations for quantum computing can be done. Throughout this section, focus will be put on the requirements for DC voltage control for the operations.

2.2.1. Electrons in the Quantum Dot

The quantum dot can be modeled by a capacitance from the gate electrode to the quantum dot. The quantum dot capacitance can be modeled as that of a 2-dimensional disc with radius R_{dot}, which is given by $C_{qd} = 8\epsilon_0\epsilon_r R_{dot}$ [14]. Using this capacitance, an indication of the voltage step for each added electron can be given through Equation 2.1, where the charge q is equal to the electron charge ($1.6 \cdot 10^{-19}$).

$$V = \frac{q}{C_{qd}} \tag{2.1}$$

This allows for estimations of the required voltage resolution through the size of the quantum dot, as shown in Equation 2.2. Quantum dots that are presented in literature typically have a size below 100 nm [13].

$$\Delta V_{charge} = \frac{q}{C_{qd}} = \frac{q}{8\epsilon_0\epsilon_r R_{dot}} \tag{2.2}$$

2.2.2. Coulomb Peaks

As indicated in subsection 2.1.1, it should be possible to measure coulomb peaks on the single electron transistor in order to determine the number of electrons present in the quantum dot [31]. Monotonic behavior of the DAC is required as otherwise the peaks may not occur consecutively due to non-monotonic behavior, which increases the difficulty on determining the number of electrons present. In order to measure coulomb peaks, it is required to have a resolution less than half of ΔV_{charge}. This is illustrated in Figure 2.3, where μ_s and μ_d need to be spaced by half V_{charge}.

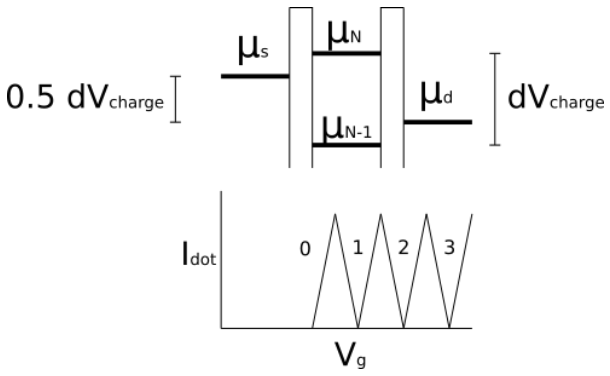


Figure 2.3: Coulomb peaks with minimal resolution

Practically, there is a limitation to this. In case the energy difference between μ_s and μ_d is large, a large current will flow. A large current will cause self-heating, which locally increases the temperature

and may cause random tunneling of electrons. For simplicity, it is however assumed that V_{charge} will be small enough such that such effect will not occur.

2.2.3. Qubit Readout

The previous two subsections have presented the requirements for biasing the single electron transistor for trapping individual electrons. The coming two paragraphs will focus on the requirements presented by readout. Through readout, the spin of the electron in the quantum dot is to be measured.

In spin qubits, a distinction between an electron with spin 1 or spin 0 (also called spin up or spin down) can be made through the introduction of a magnetic field. When applying a magnetic field, the spin up and spin down state are split by the Zeeman-energy $\Delta E_z = g\mu_b B$, where g is the g-factor of the material and μ_b the magnetic permeability. Using $\Delta E_z = \frac{1}{2} C_{qd} \Delta V_z^2$ this energy can be translated to a voltage requirement and yields Equation 2.3. For readout, it is generally required to bias the quantum dot between the spin up and spin down state.

$$\Delta V_z = \sqrt{\frac{2E_z}{C_{qd}}} = \sqrt{\frac{2g\mu_b B}{C_{qd}}} \tag{2.3}$$

Pauli Spin Blockade

The first method of readout is through the Pauli spin blockade. This method exploits the Pauli exclusion principle, which states that two electrons with the same spin can not be in the same energy level of a quantum dot. Using the principle, a spin dependent blockade of current can be created. This spin dependent current can then be used for readout and is illustrated in Figure 2.4 [33, 34]. The figure shows two quantum dots: in the left one, an electron with spin up or spin down to be read out is present, while in the right quantum dot an electron with spin up is present. In the right quantum dot, the dashed lines represent the energy levels of adding another electron with spin up or spin down to the dot. In the left configuration of Figure 2.4, the electron can not move to a higher energy state resulting in no measurable current. In the right configuration, the electron can move to a lower energy state as it is possible to have a spin up and spin down electron in the same energy level, causing a measurable current.

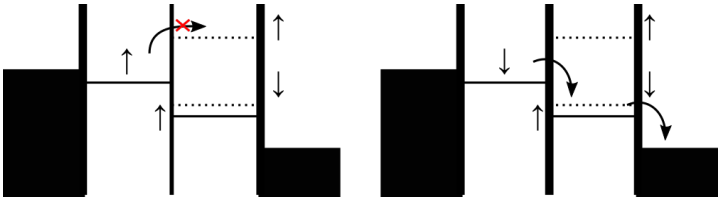


Figure 2.4: Illustration of readout using Pauli Spin Blockade. The dashed lines represent the energy level of the spin up or spin down state. In the right dot an electron with spin up is present.

This method requires biasing the left quantum dot between the split energy levels, which in literature has been given to be approximately 5-200μeV [4]. Recent work has shown improvement in the signal to noise (SNR) of the readout through an electron cascade, making it a promising readout method [35].

Elzerman Readout

The second method for readout is called Elzerman readout [refernce]. For Elzerman readout, there is another 'sensing' quantum dot present near the quantum dot containing the qubit. The quantum dot with the qubit should be biased such that the energy level of the sensing dot is between the energy level of a spin up or spin down state. In case the qubit is in the spin up state, no charge will be observed as illustrated in a) of Figure 2.5. If the qubit is in the spin down state, the electron with spin down will move to a lower energy state, allowing a charge to be measured. Then an electron with spin up will move into the quantum dot as that state has the lowest energy potential as illustrated in b) of Figure 2.5 [36].

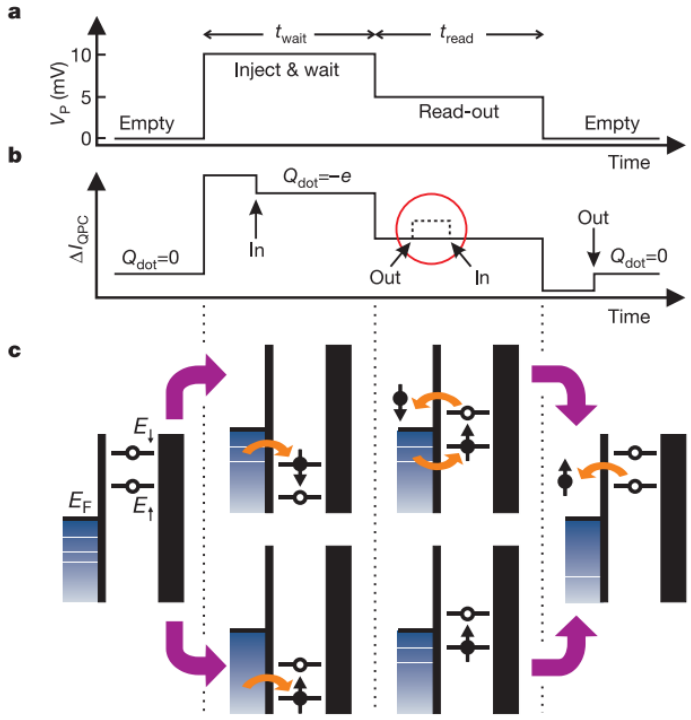


Figure 2.5: Illustration depicting Elzerman Readout (image copied from[36]).

2.3. Qubit Operations

For quantum computing, qubit operations need to be performed. These qubit operations are implemented using AC excitation of electron spin resonance (ESR) lines, barrier electrodes or plunger electrodes[1]. Figure 2.6 shows a structure that can be used to control and perform qubit operations. Previous work has shown requirements for the AC excitation for qubit operations, however the DC requirements are not explicitly stated [37].

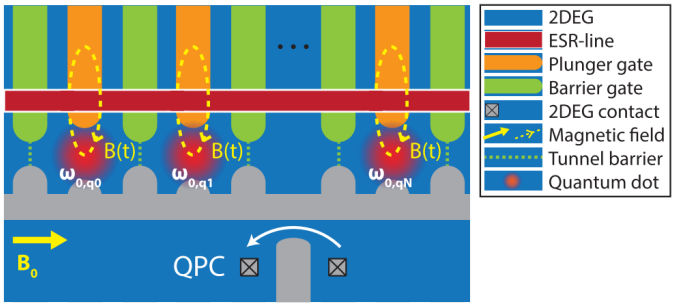


Figure 2.6: Possible setup for creating and manipulating spin qubits with different gates (image copied from [38]).

2.3.1. Single-Qubit Operations

Single qubit operations are performed by applying an alternating magnetic field on the qubits. The magnetic field is generated using a high frequency signal coming from a RF-DAC, which generates a magnetic field by applying a current through an ESR line close to the electrons [5]. Therefore no DC-specifications are required, as no DC voltage needs to be put on the ESR line.

[1]Some literature uses gates instead of electrodes.

2.3.2. Two-qubit operations

For two qubit operations, the barrier and plunger gates of two qubits are modulated with AC signals. The voltage of the barrier between the two electrons is set by the DC-DAC, however an AC signal can be superimposed on this DC value. In case it is assumed that the AC signal has sufficient resolution and output range, only a coarse DC resolution needs to be set on this barrier [5].

2.4. 2D-Array Structure

A quantum computer requires a significant amount of logical qubits in order to be able to execute algorithms. A logical qubit usually consists of multiple physical qubits. This allows for redundancy and can help increase fault-tolerance through quantum error correction [10]. Therefore, creating a scalable structure for creating and manipulating qubits is required. A method to increase the density of qubits is to move from 1 dimensional vectors (as shown in Figure 2.6) to 2 dimensional arrays of quantum dots. Several approaches have been published that illustrate 2 dimensional arrays. These arrays show that the number of electrodes scales linearly with the number of qubits, which can vary from 10 to 15 electrodes per qubit[4, 11, 16].

As the target application aims to bias millions of qubits, the DC-DAC should be able to scale well as the number of qubits grow. A distinction in resolution requirements has been made in the qubit array proposed by Boter et al[16]. Electrodes can be grouped in a coarse and fine resolution category depending on what their functionality is.

2.4.1. Resolution Requirement Electrodes

The requirements posed in section 2.2 are important for the plunger electrode, which is equivalent to the gate in Figure 2.1. Barrier electrodes (Figure 2.6) help prevent coupling between neighboring quantum dots. These barrier electrodes should have a high energy potential such that electrons can not pass through and therefore only require a coarse DC resolution. For two qubit operations, the barriers are AC modulated. Based on the previous sections and literature a distinction of electrodes can be made as shown in Table 2.1.

Table 2.1: Electrodes in qubit Arrays

Electrode	Resolution Requirement
Plunger Electrode	Fine DC + AC Excitation
Barrier Electrode	Coarse DC + AC Excitation
ESR-line (Single Qubit Operation)	AC Excitation
Source and Drain	Fine DC

There are a few points which will be assumed for the derivation of the specifications in the rest of this chapter:

- No distinction will be made between the coarse and fine DC resolution when designing the DC-DAC. The fine DC resolution should also be able to bias the coarse DC resolution electrodes. For future biasing solutions, this distinction between coarse and fine resolution could help reduce the power consumption of the DC-DAC.
- It is assumed that 1- or 2-qubit operations do not introduce additional biasing considerations.
- The source and drain of the single electron transistor require a buffered bias signal. As there is only one source and one drain in the current experiments, it is assumed that this is not limited by scalability and therefore still can be applied by an external DC source.

With these assumptions, the DC-DAC can be designed to be a scalable structure that can bias an increasing number of electrodes.

2.4.2. Multiplexer

In case the number of qubits is low, it is possible to use a DAC for each electrode. However this does not scale well once the number of qubits increase, which is why a multiplexer is introduced.

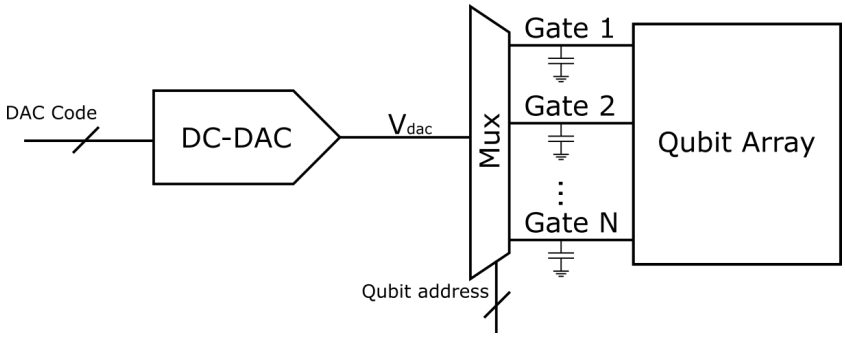


Figure 2.7: Generalized overview of the DC biasing system for qubits.

Each multiplexer channel has a hold capacitors on which bias voltages can be sampled as shown in Figure 2.7. These channels are in turn connected to electrodes required for creating qubits. The multiplexer allows a single DC-DAC to be used. In case more electrodes need to be biased, additional multiplexers can be connected requiring only a few extra control signals [16, 17]. A multiplexer for this purpose has currently been designed which has 14pF hold capacitors.

2.5. Biasing Requirements

The previous sections have illustrated requirements for voltage resolution for the electrodes. From this, a specification of the voltage resolution can be derived. In addition, this section will present considerations for the refresh rate required for the bias voltages.

2.5.1. Voltage range

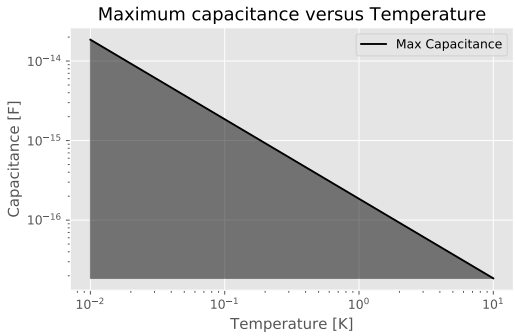
The voltage range required to successfully create a quantum dot, depends on the technology in which the quantum dot has been implemented. Quantum dots can be implemented using various technologies, such as SiMOS and SiGe. A SiMOS sample is available on which quantum dots have been successfully formed by using a 1-4 V voltage range, while for the SiGe sample a voltage range of approximately -0.5-1 V is required to create quantum dots. Based on these samples, it can be concluded that an output voltage range of 1.5 to 3 V is required depending on the technology used. A large voltage range could be needed to deplete the substrate of free electrons. Additionally, the lever arm effect could play an important role in what the required output range is, as the lever arm determines how effectively energy is added to the quantum dot.

The DC-DAC is to be used with a SiMOS qubit sample, therefore the target output voltage range is 3 V. Eventually, this should also allow for flexibility with other technologies, as it would also be compatible with the mentioned SiGe sample.

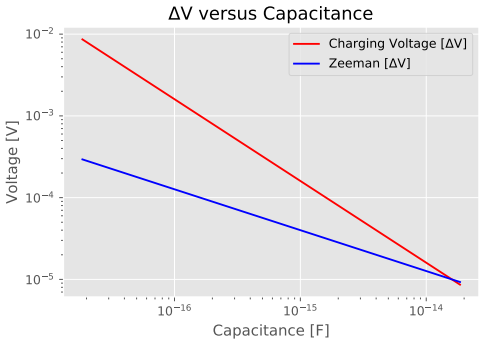
2.5.2. Voltage resolution

Based on the constraints posed in section 2.1 and section 2.2, a minimum LSB step of the DAC can be derived such that control over the number of electron in the quantum dot can be achieved and readout is possible. For the following derivations, it is assumed that the thermal energy of electrons need to be 10 times smaller than the charging energy. In addition, the Zeeman energy is assumed to be $5\ \mu eV$ [4]. These are pessimistic assumptions which should give a lower bound value for the required voltage resolution. The thermal energy constraints the maximum capacitance C_{qd} for a certain temperature as illustrated in (a) of Figure 2.8. The capacitance can then be coupled to a minimum LSB step depending on the splitting of energy states caused by Zeeman splitting.

Based on the assumed values, the plots in Figure 2.8 can be derived. For the DAC resolution, a LSB step of $50\ \mu V$ has been selected. This LSB value allows for a theoretical maximum capacitance of 0.65 fF, which is equivalent to an approximate dot size of 780 nm. This dot size is larger than what is practically implemented. The targeted resolution should allow for forming qubits and be versatile enough to be used in an experimental setup.



(a) Dependence on allowed quantum dot capacitance versus temperature, note that a larger dot capacitance requires operation at lower temperatures.



(b) Quantum dot capacitance versus LSB step. Larger capacitances require finer resolutions.

Figure 2.8: Modeling to derive specifications.

2.5.3. Stability

Electrodes that are connected to the multiplexer require a certain voltage stability. This stability is the variance that the voltage on the electrode may have while keeping the qubits properly biased. The stability is determined by:

- The leakage of the hold capacitor C_h.
- The sampling noise on the hold capacitor.
- The DC-DAC output noise.

The stability is therefore a combination of both noise and leakage factors from the DC-DAC and multiplexer. How the voltage changes is illustrated in Figure 2.9. Here the shaded area is used to illustrate the output voltage of the DC-DAC with noise.

Some prior art states that this stability should be below the charge noise in experiments [11]. An important note is that the voltages in the system illustrated in Figure 2.7 are sampled. Therefore, the noise contributions of the DC-DAC and the sampling noise on C_h will be static and only be change in case the electrode is sampled again. During operation, only the change in biasing voltage due to leakage is visible on the electrode. Literature has shown that the capacitor leakage is low at cryogenic temperatures ($V_{leak} < 1\ \mu V/s$ [39]). It is therefore assumed that during a qubit operation, which is in the order of microseconds, the bias voltage remains constant and does not affect the operation. The DC-DAC will be designed such that the stability budget will be below the specified voltage resolution.

2.5.4. Linearity

The DC-DAC does not perform any kind of AC excitation on the qubits. Therefore, properties like 2nd order distortion or 3rd order distortion will not be of interest. There is a requirement for the DAC to be monotonic in order to properly create coulomb peaks. Formally this results in the specification that the $|DNL_{max}| < 1$. Where the formula of the DNL is given by Equation 2.4, where A(i) is the output voltage of the DAC for the digital input code i. In terms of linearity, the DAC has no requirement for the INL, while there is a constraint on the DNL such that $|DNL_{max}| < 1$ [40].

$$|DNL_{max}| = MAX[|\frac{A(i+1) - A(i)}{A_{lsb}} - 1|] \tag{2.4}$$

2.5.5. Power

In order to reach cryogenic temperatures, dilution refrigerators are used which can reach cryogenic temperatures below 200 mK. At these temperatures the refrigerator only has a limited cooling power. If more power is dissipated than the available cooling power, the refrigerator heats up and cannot maintain the temperature. The available cooling power depends on the desired operating temperature. For 4 K, the cooling power is rated to be ≈1 W, while for 200 mK, the cooling power is in the order of $200\ \mu W$

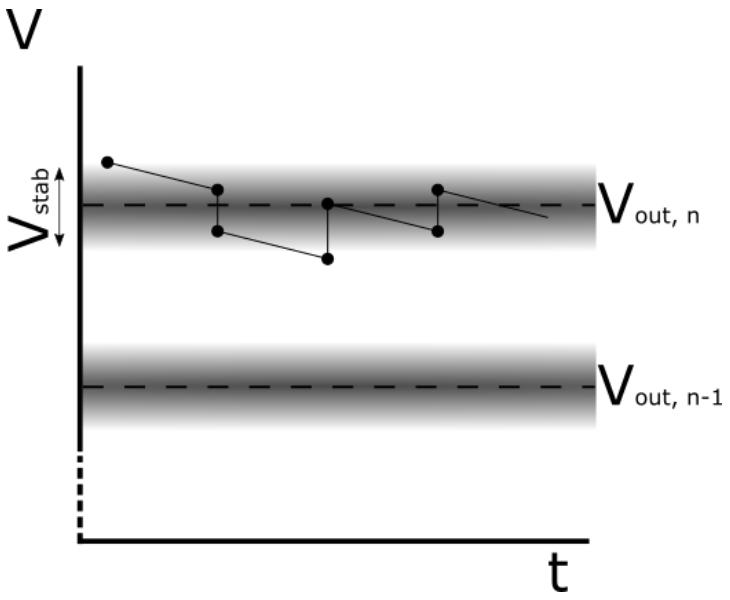


Figure 2.9: Development of the multiplexer hold voltage over time.

[41]. The power dissipation of the control electronics needs to be limited such that it can operate at these temperatures without exceeding the available cooling power.

Considering that the DC biasing of the qubits is an important but minor component of the full system, the power consumption of the DC-DAC needs to be limited. In this thesis a maximum allowed dissipation of 1mW is targeted.

2.6. System Level Considerations

To achieve scalability in biasing, there are a few additional system level considerations.

This section aims to present some of the trade-offs for these considerations.

2.6.1. Feedback Loop

The structure presented in Figure 2.7 illustrates an open-loop structure for biasing the qubit array. One could consider having a feedback loop from the qubit array which measures the voltage on the multiplexer channels. Then only when the bias voltages go outside of the stability region, it is reset.

The advantage is that the bias voltages are only reset once it moves outside of the stability region. This is beneficial as the leakage current reduces at cryogenic temperatures[39] and the DAC can then be turned off when refreshing the bias voltages is not required.

Measurement the bias voltages would be done through an Analog to Digital Converter. Connecting an ADC to one of the electrodes has some disadvantages. First, connecting the ADC to a multiplexer channel loads the input capacitor, which causes the charge on the hold capacitor to divide. This affects the voltage stability on the hold capacitor. Additionally, an ADC internally has a DAC in order to perform the conversion. This ADC is used to monitor whether the voltage is outside of the desired stability range, therefore this ADC needs to be able to measure a finer voltage resolution than that the DAC is able to set. This makes the ADC for the feedback more power consuming than the DAC used to set the bias voltages if they are to operate at the same speed.

From the presented disadvantaged, it can be concluded that measuring all multiplexer channels will be power consuming and will not scale well as the number of qubits increase. However it can be of interest to have an ADC connected to a single multiplexer channel that is used to characterize the leakage present at the multiplexer. This way, the required refresh rate can be determined before the quantum computer begins operation which allows refreshing the voltages only when needed.

2.6.2. Unbuffered Operation

Previous work presented by Vliex et al. [11, 29, 42, 43] illustrates the use of a capacitive DAC which does not have an output buffer. The hold capacitors that are connected to the electrodes are charged

in multiple cycles. This saves power, as the operational amplifier which serves as buffer is consuming continuous static power. However, as the capacitive DAC is unbuffered it creates an output voltage that is dependent on the connected capacitive load. This makes it difficult to accurately determine both the value of the voltage on the hold capacitor and whether the voltage has been properly set on the hold capacitor. If coulomb peaks can be measured to map the digital input code to the number of electrons, this should not be an issue.

2.7. DC-DAC specifications

This chapter has presented constraints, limitations and requirements for implementing the DC-DAC at cryogenic temperatures. The target specification have been summarized in Table 2.2.

For current qubit experiments at QuTech, internally developed electronics are used, also known as the SPI rack [44]. This SPI rack has been developed as a piece of general purpose electronics and is not solely used for performing qubit experiments. Compared to the derived specifications put in Table 2.2, this SPI-rack has a larger voltage output range (4-16V), a finer LSB step resolution (300nV) and a lower integrated noise (0.5μV_{rms} between 0.1-10Hz). It offers these specifications at the power consumption of 100 mW. The SPI rack is used to connect directly to the gates, therefore it does not take into account the effect of the sample and hold of the multiplexer, which may lead to a larger static sampled error, but no continuous noise on the electrode.

The specifications of the DC-DAC have a better LSB resolution and a lower voltage output range compared to what the current equipment offers but it is expected that the derived specifications should be more than sufficient.

Table 2.2: DC-DAC Specifications

Specification	Value
Operating Temperature	0.2-4 K
Resolution (V_{lsb})	<50 μV
Voltage range	3 V
Integrated Noise	13.2 μV
P_{DAC}	<1 mW
Linearity	Monotonic
Output load	>14 pF

3

DAC Architectures

The biasing of the spin qubits will be done through a Digital to Analog Converter (DAC). The DAC should meet the specifications as presented in Table 2.2. A high level overview of DAC conversion domains is given and general advantages and disadvantages are enumerated. Then, two DAC architectures will be more elaborately discussed and compared on a high level. Based on the high level comparison, observations are made and an architecture for the DC-DAC is selected.

3.1. Overview DAC architectures

In the process of deciding which DAC architecture is most suitable for biasing qubits, prior art on the different DAC architectures has been analyzed. From this a mind map as shown in Figure 3.1 has been made in order to present an overview of available structures [40]. This shows an overview of the four conversion domains which can be used for the digital to analog conversion. Each conversion domain has possible DAC architectures attached to it.

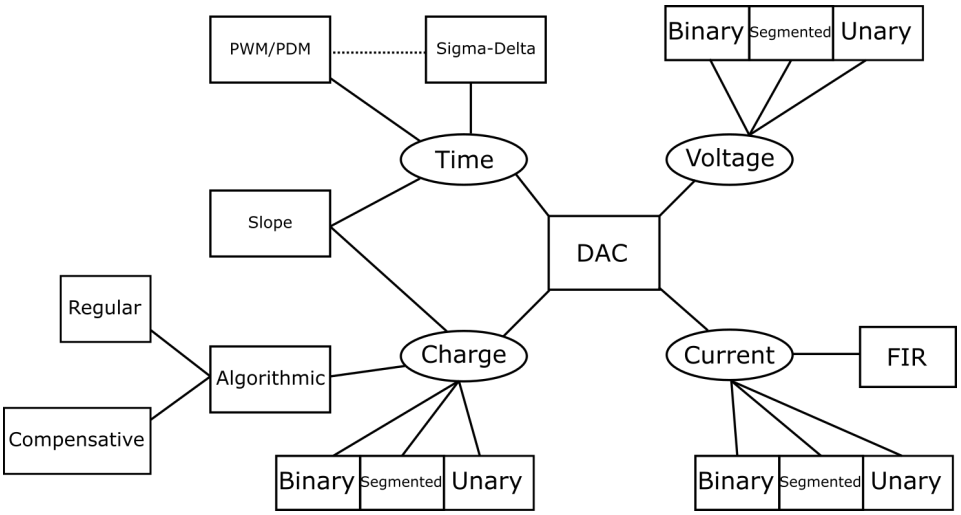


Figure 3.1: Overview of different DAC architectures, divided by conversion domain.

From the literature, some superficial conclusions can be drawn on the application area of certain architectures and domains. These conclusions help limit the scope for suitable DAC architectures. In the following subsections, the different domains are covered and their strengths and weaknesses are discussed [40].

3.1.1. Binary, Unary and Segmented structure

Common among the voltage, current and charge domain are the binary, unary and segmented structure. The binary, unary and segmented structure determines how components (resistors, current sources,

capacitors) are switched. In a unary structure, for each increment in bitcode an additional component is switched. For a binary structure, components are sized according to 2^N which are switched similarly to a binary code. A segmented structure combines binary and unary structures, resulting in segment that is binary switched and segment that is unary switched.

3.1.2. Voltage Domain DACs

Voltage Domain DACs are created using resistors and are present in binary, unary and segmented structures. The common structures therefore result in resistor strings (unary structure) and R-2R ladders (binary structure) [40]. These structures have static dissipation and have a limited speed due to parasitic capacitances. In order lower the noise of these DACs, small resistances are needed which generally require a larger area and have a larger static power dissipation.

3.1.3. Current Domain DACs

Current Domain DACs use current sources to source or sink a current through a load. These DACs have a high power consumption and operate at high speeds, making them suitable for high speed applications. For the designed DAC, voltages will need to be set, which means that a conversion from the current to voltage domain will still has to be performed.

3.1.4. Charge Domain DACs

Charge Domain DACs use capacitors to create an output voltage. The usage of capacitors is favorable in terms of power, as only dynamic power is consumed by charging the capacitors and switching the transistors. Additionally, there are a few alternative structures which utilize the fact that capacitors store charge, such as Algorithmic DACs.

3.1.5. Time Domain DACs

Time Domain DACs utilize time as a primary quantity for the conversion from the digital to analog domain. These DACs still use a voltage, current or charge DACs, however by oversampling and modulating signals in the time domain, the resolution at the output of these DACs is increased. This category includes Sigma Delta modulators and PWM modulators and more.

3.1.6. Conclusion

Based on the superficial analyses in this section, a conclusion is reached that for the low-power operation, a charge domain DAC should be used for implementation of the DC-DAC. In this chapter, specifications of the common C-DAC (section 3.3) and a newly introduced slope DAC (section 3.4) are estimated and an overview to compare these architectures is presented in Table 3.1.

3.2. Buffered output

The voltage created at the output of the DAC is not necessarily buffered and designs have been presented that do not have a buffer at the output [29]. In this chapter, it is assumed that all DAC architectures make use of an operational amplifier; either as output buffer or as core component in the DAC. In order to estimate the noise and power dissipation of the amplifier, Equation 3.1 and Equation 3.2 are used [45].

$$v^2_{opamp,noise} = \alpha \frac{kT}{C_o} \tag{3.1}$$

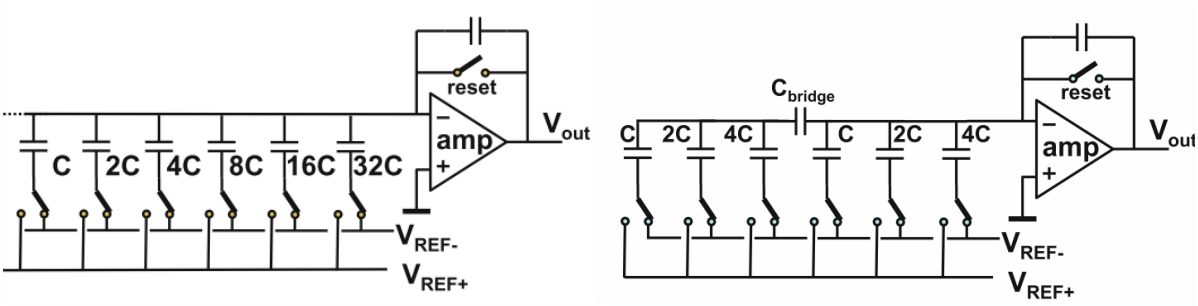
$$I_d = 2N_{settle} F_{clk} A_0 C_l \frac{\frac{nkT}{q}}{\eta_{gm}} \tag{3.2}$$

There is temperature dependence in both equations, which means that generally low temperature operation should be favorable in case these equations accurately model the behavior down to cryogenic temperatures.

As an operational amplifier is connected directly to the output, it will contribute in noise as given by Equation 3.1. The allowed noise power should therefore be divided accordingly between the operational amplifier and the noise from the DAC architecture used.

3.3. Single stage C-DAC

A low-power DAC architecture common in literature is a single stage binary C-DAC as shown in Figure 3.2. The output voltage is generated by switching the capacitors in the capacitive bank between V_{ref-} and V_{ref+}, allowing a capacitive division which sets the output voltage V_{out}. Within this section, not only the binary C-DAC will be discussed, but also variations that use a bridge capacitor or a segmented structure will be touched upon to present their advantages and disadvantages.



(a) Regular structure

(b) Structure with capacitve bridge

Figure 3.2: Single-Stage C-DAC structures (images copied from [40])

Area

Considering the binary C-DAC structure in Figure 3.2 with unit capacitance C, it can be observed that an additional capacitor is added for every bit. This capacitor needs to be one C larger than all the capacitors present in the C-DAC. The capacitance of the C-DAC architecture will therefore scale with 2^N, where N is the number of bits of the DAC, regardless if the C-DAC is unary or binary structured, causing the area to scale accordingly. In case the C-DAC is structured in an unary manner, the total required area for the capacitors would remain the same, however more switches are also needed.

It is possible to reduce the area by using bridge capacitors as shown in (b) of Figure 3.2. The bridge capacitor is used to create a series connection of capacitors, reducing the effective output capacitance seen from the node connected to the amplifier. A single bridge capacitor allows reducing the area from 2^N to a smaller $2^{N/2+1}$.

Power

As this is a capacitor bank, the energy required to charge all the capacitors for an output voltage V_{out} is equal to $E = \frac{1}{2}C_{in}V_{out}$, where C_{in} is the total capacitance seen from V_{ref+} and V_{ref-} for charging.

The average energy required to charge the DAC to a voltage output is given by evaluating the integral $E_{avg} = \frac{1}{V_{dd}}\int_0^{V_{dd}} \frac{1}{2}C_{in}V^2 dV$, which results in $E_{avg} = \frac{1}{6}C_{in}V_{dd}^2$ and assumes an uniform distribution of the DAC output voltages. This leads to the conclusion that a larger capacitor bank results in a larger power dissipation, making it desired to keep the capacitor bank as small as possible for low power operation.

With the bridge capacitor in place, the total capacitance is lower compared to the classical structure, allowing for more energy efficient operation.

Noise

The noise depends on the total output capacitance of the bank. Each capacitor is linked to either V_{ref+} or V_{ref-} through switching. From the output, this can be seen as if the capacitors connected to V_{ref+} and V_{ref-} are connected in parallel. For a C-DAC without a bridge capacitor, this means that $C_{in} = C_{out}$ and this results in an output noise of as shown in Equation 3.3. It can be observed that all energy which is put in the DAC improves the noise performance with a 1:1 ratio.

$$V_n^2 = \frac{k_b T}{C_{out}} \tag{3.3}$$

With the bridge capacitor the output capacitance is not equal to the total bank capacitance, but is lower due to the series connected bridge capacitor. Assuming the two capacitor banks are equal (C_{bank}), then the output capacitance is given by Equation 3.4.

$$C_{out} = C_{bank} + \frac{C_{bank}C_{bridge}}{C_{bank} + C_{bridge}} \tag{3.4}$$

By using the bridge capacitor the effective output capacitance becomes lower, resulting in worse noise performance for the same area and power as Equation 3.3 holds. This means that not all energy input into the DAC improves the noise performance with a 1:1 ratio, which is the case without the bridge capacitor. This makes a C-DAC with bridge capacitor more power consuming when the design is noise limited.

Linearity

In order to have monotonous behavior in the DAC, the switching to the MSB capacitor (from digital code $2^{N-1} - 1$ to 2^{N-1}) needs to be smaller than a LSB step. This transition is assumed to be dominant as this is the most sensitive transition. The probability that the transition is monotonic can be described by $\frac{\sigma_{\Delta Ci}}{C} = \frac{\sigma_C}{C}\sqrt{2^N - 1}$, where $\frac{\sigma_c}{C}$ is the error percentage in capacitance per $\sqrt{fF}$ and $\frac{\sigma_{\Delta Ci}}{C}$ the variance of the transition in terms of C_{LSB} [40].

The transition can be improved by using a segmented structure as shown in Figure 3.3. Here the critical switching is determined by the transition of the binary part of the C-DAC to the Unary part. For a segmented structure, it is assumed that k bits are implemented as a binary C-DAC and the structure has a total of N bits. The probability that this is larger than a LSB step can be described by $\frac{\sigma_{\Delta Ci}}{C} = \frac{\sigma_C}{C}2^{N-k}\sqrt{2^{k+1} - 1}$. The term 2^{N-k} is added because there are 2^{N-k} unary capacitors present, so the transition from the binary to unary part happens 2^{N-k} times and each transition has to be below the LSB step. Using this equation when designing a segmented C-DAC, monotonicity can be achieved.

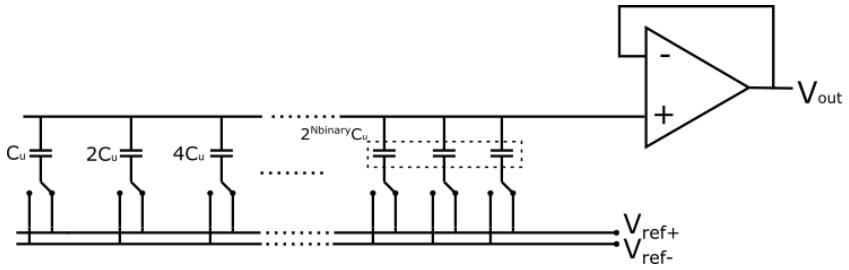


Figure 3.3: Segmented C-DAC

Speed

The speed of this stage is constant. The charging and discharging of the capacitive bank is dependent on the size of the capacitors and the on resistance of the switches. Generally, a smaller C-DAC is able to operate faster as a lower capacitance allows faster settling. From literature, it can be concluded that these C-DACs can easily reach speeds of above tens of Megahertz [46]. The C-DAC should therefore be able to bias millions of qubits in case the refresh rate of the bias voltages is one second.

3.4. Slope C-DAC

The C-DAC works by receiving a digital input code and outputting a voltage. All qubit voltages need to be set accurately once and refreshed periodically due to leakage. Therefore a possible alternative method for biasing could be to use an accurately generated slope which generates the full voltage output range incrementally. This ramp periodically generates the entire voltage output range, which can be used to refresh the bias voltages.

Such a slope can be generated through an integrator combined with a DC input signal. An integrator can be implemented in the continuous time domain through a current or in the discrete time domain through charge. The primary difference between continuous time and discrete time operation is the

way noise accumulates and the control and timing accuracy required. Because operating in the charge domain is favorable for low power operation, a slope C-DAC is illustrated in this section.

A circuit that operates as a switched capacitor integrator is illustrated in Figure 3.4. The switched capacitor integrator operates by first sampling an input voltage on C_{add} in Φ_1, which is then integrated onto C_{int} during Φ_2. By swapping around the phases on switches M_1 and M_2, it is possible to achieve either positive or negative integration. The V_{lsb} step at the output is given by Equation 3.5, illustrating that for a DAC with a high number of bits, the ratio between C_{add} and C_{int} needs to be large.

$$V_{lsb} = V_{in}\frac{C_{add}}{C_{int}} \tag{3.5}$$

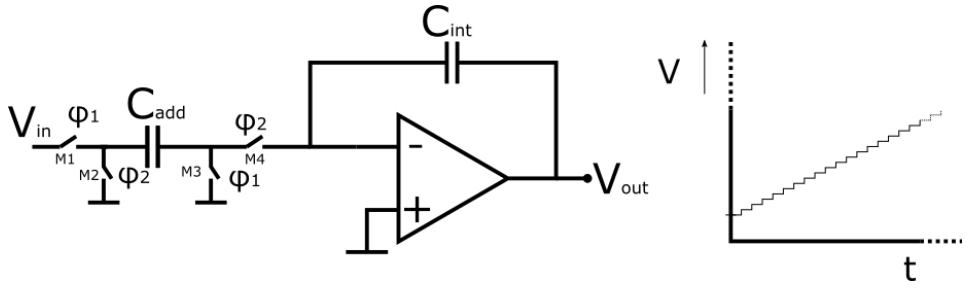


Figure 3.4: Switched Capacitor Integrator core circuit on the left, with the output voltage graphed on the right.

Area

The total area required is determined by the operational amplifier, loading capacitor and integrating capacitor as shown in Figure 3.4. Here, the integrating capacitor is the primary contributor for the required area. The integrating capacitor C_{int} is sized to meet the noise requirements of the DAC. To meet the LSB step, the loading capacitor C_{add} is sized such that it achieves a desired ratio with the integrating capacitor and input voltage. In case C_{add} can not be sized to meet this requirement, the size of the integrating capacitor can also be increased to create the required LSB step.

Power

For a single ramp, the integrating capacitor needs to charge once from 0V to V_{max}, requiring a total energy of $E = \frac{1}{2}C_{int}V_{max}^2$. As it is possible to generate all bias voltages and therefore bias a lot of qubits from a single ramp, the efficiency can be high as shown in Equation 3.6.

$$E_{qubit} = \frac{\frac{1}{2}C_{int}V_{max}^2}{N_{qubits}} \tag{3.6}$$

The power required for efficient operation is primarily determined by the size of the integration capacitor C_{int}. Comparing the energy required to charge C_{int} from 0V to V_{max} to the power dissipation of the operational amplifier, it can be observed that the energy required to charge C_{int} is significantly smaller and recharging C_{int} only has to be done once every second. Therefore having a large C_{int} size is not problematic in terms of power.

Noise

The noise in the switched capacitor integrator consists of two parts, the noise of the operational amplifier (Equation 3.1) and the accumulated noise in the integrator. Here an expression is derived that shows the dependence of the capacitor size on the accumulated noise. The accumulated noise can be dissected in several components, here all charge noise contributions in C_{int} are analyzed [47]:

- On reset, $Q_{ncint}^2 = kTC_{int}$ is sampled on C_{int}
- In operation, V_{in} is sampled on C_{add}, the total charge noise power on C_{add} is equal to $Q_{ncadd}^2 = kTC_{add}$. The charge on C_{add} is then integrated on C_{int} in Φ_2.

- When the integrating switches (M_2, M_4) are opened, the series connection of C_{int} and C_{add} through the op-amp is broken and charge noise equal to kTC_{eq} is added on C_{int}. Here $C_{eq} = \frac{C_{int}C_{add}}{C_{int}+C_{add}} \approx C_{add}$.
- As the integration is repeated 2^N times, this results in a total charge noise as shown in resulting in Equation 3.7.

$$Q^2_{ncint} = kTC_{int} + 2^{N+1}kTC_{add} \tag{3.7}$$

Equation 3.7 can be simplified by assuming that $V_{in} = V_{max}$ and C_{add} is chosen such that $C_{add} = 2^{-N}C_{int}\frac{V_{max}}{V_{in}}$, resulting in Equation 3.8.

$$V^2_{nint} = \frac{kTC_{int} + 2^{N+1}kTC_{add}}{C^2_{int}} = \frac{3kT}{C_{int}} \tag{3.8}$$

Linearity

In theory, this integration method is inherently linear and guarantees monotonous behavior by design. Non-monotonic behavior can be introduced due to noise. Therefore the LSB step size should be larger than the integrated noise at the output.

Speed

The operation speed of this DAC is slow. In case a bias voltage needs to be set, there is only a periodic window in which this voltage is available. This means that latency is introduced, which depending on the application can be an issue or not. In the scenario of biasing capacitors where only periodic refreshing is required and it is expected that latency does not form an issue.

3.5. Other Architectures

For brevity, only two architectures have been listed elaborately in this section. Other architectures have been considered, but were deemed not promising enough. For completeness, the other considered architectures including their interesting properties are listed here. Derivations and images of these architectures can be found in Appendix A.

- Multi-stage DACs, which combines multiple R-DAC and C-DAC stages together. An interesting property of having the DAC split over multiple stages is that these stages can be located at different temperature stages. This way it could be possible to put a R-DAC at 4K and a C-DAC at 200 mK. The implementation of a multi-stage DAC implemented at the same temperature stage has been demonstrated by Vliex et al [29].
- Algorithmic DACs, which operate by switching two capacitors to control the charge. Variations of this DAC can be implemented with a relatively small area. Using intelligent switching of the capacitors, voltages can be generated accurately negating the effect of mismatch between the capacitors [48]. Algorithmic switching requires switching capacitors often, resulting in relatively large power dissipation which makes this architecture less attractive.
- A slope DAC based on a continuous time current integrator, this generates a slope similar to the switched capacitor integrator but then in the continuous time domain. Operating such a current integrating DAC requires accurate timing and low jitter to allow for low noise operation which can make it more power consuming.

3.6. Address and voltage based biasing

Comparing the two DAC architectures presented here, a difference in operation can be observed. This is illustrated in Figure 3.5, where on the left address based biasing is shown and on the right voltage based biasing is illustrated. In case of address based biasing, the waveform output by the DAC can be considered random and dependent on the address. For voltage based biasing, the waveform output by the DAC is considered as a degree of freedom and is designed to efficiently generate all required bias voltages once. This section compares the two biasing methodologies and illustrates what is preferred when aiming for biasing scalability.

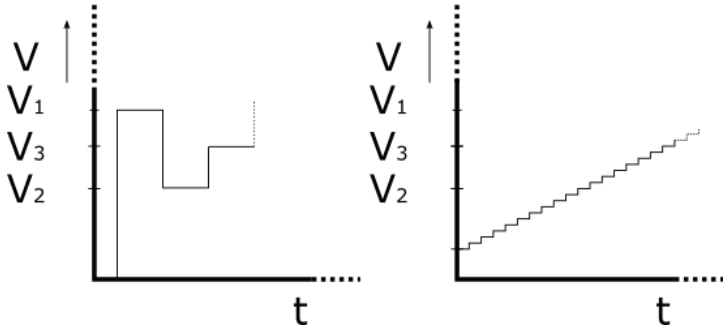


Figure 3.5: Left illustrates address based biasing, right illustrates voltage based biasing.

Address based biasing

When address based biasing is applied, a list of addresses and according bias voltages is used. In the case of the qubit biasing system, these addresses are multiplexer channels with a fixed load capacitance. An advantage of this biasing scheme is that it is fast, as the required bias voltage is available with minimum delay. Additionally, if only a single address is biased at the a time, the load capacitance is well known. However as can be observed in Figure 3.5 the DAC output waveform changes significantly over time, dissipating a lot of power due to switching losses. Through address based biasing, each additional electrode that needs biasing causes extra power dissipation due to the induced switching losses.

Voltage based biasing

Voltage based biasing uses the output waveform of the DAC as a design degree of freedom to generate all bias voltages once. If electrodes require the same biasing voltage, these can be biased simultaneously or consecutively. The power dissipation for creating the slope is constant, independent of the number of electrodes that are connected. This allows for biasing scalability as the number of qubits increase as shown in Equation 3.6. The disadvantage of voltage based biasing is that there can be a variable load present at the output of the DAC depending on how the multiplexer is switched. Additionally in case voltage based biasing is used, latency is introduced as each voltage is only available periodically.

3.7. Overview

In this chapter, two DAC architectures have been analyzed extensively. How these architectures scale with respect to the number of bits N and maximum output voltage V_{max} has been summarized in Table 3.1. Having an overview of these criteria and seeing the scaling properties helps determine a suitable architecture for the DC-DAC.

From the equations in Table 3.1 and section 3.2 plots can be made to illustrate the power dissipation versus number of qubits. In these plots, the Effective Number Of Bits (ENOB) of the DAC architecture is estimated based on Table 3.1, where only signal and noise contributions are considered. These plots are shown in Figure 3.6, for generating these plots, it is assumed that:

- A noise limited design is assumed, so the capacitor sizes are determined by noise. It is assumed that monotonicity can be guaranteed in the C-DAC architecture through a segmented structure.
- The bandwidth of the operational amplifier (used in Equation 3.2) is fixed for the C-DAC.
- For the C-DAC, an operating frequency of 10kHz is assumed.
- For the slope DAC, it is assumed that $V_{in} = V_{max}$ and a single ramp is generated every second. This requires that the bandwidth of the amplifier increases as the number of bits increase.

Based on the presented information in this chapter, the following conclusions can be drawn with respect to the C-DAC and SC-Integrator architectures and their biasing methodologies:

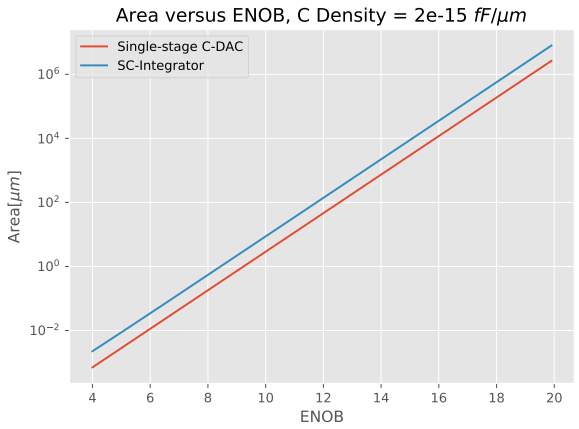
- The SC-Integrator requires approximately 3 times the area of the C-DAC when noise limited while the area of both scale exponentially with the number of bits.

Table 3.1: Approximations of DAC structures versus resolution

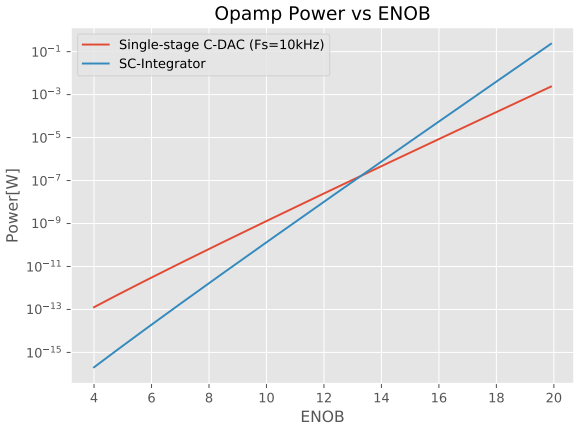
	Single-stage C-DAC	SC-Integrator
Architecture Energy	$\frac{1}{6}C_{bank}V_{max}^2$	$\frac{1}{2}C_{int}V_{max}^2$
Area	2^N	2^N
$\overline{V_{noise}}^2$	$\frac{k_bT}{C_{out}}$	$\frac{3k_bT}{C_{int}}$
Linearity (monotonous)	$\frac{\sigma_{\Delta Ci}}{C} = \frac{\sigma_C}{C}\sqrt{2^N - 1}$	$V_{lsb} > V_{noise,rms}$
Max Delay	Constant	2^N

- For the SC-Integrator, the power dissipation is dominated by the operational amplifier.
- Address based biasing results in a constant power per qubit as the number of qubits increases.
- Voltage based biasing optimizes the output waveform of the DAC and results in reduced power per qubit as the number of qubits increases.

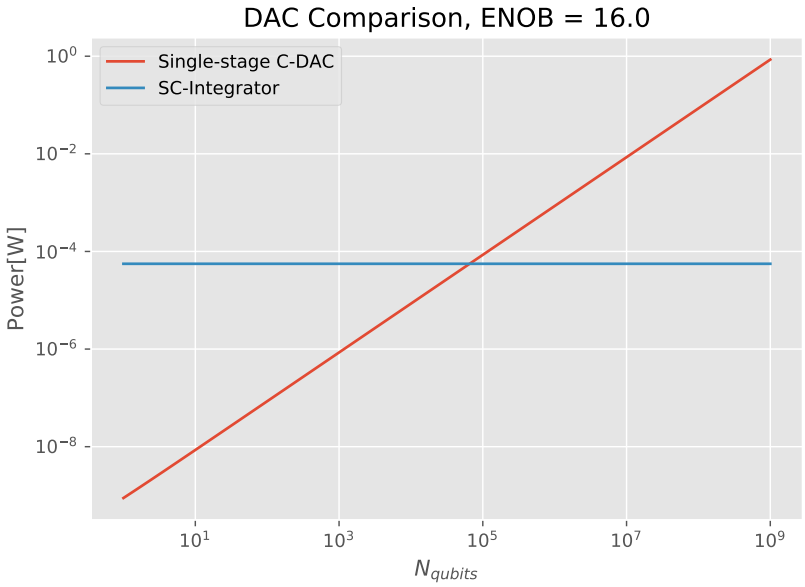
The plots in Figure 3.6 indicate that the most suitable DAC architecture depends on several factors, like the number of qubits present and the refresh rate required. For the DC-DAC it is desired to create a scalable structure from which many qubits can be biased. Therefore the decision has been made to implement the slope C-DAC based on a SC-integrator and to find out to what extent the scalability can be achieved with this architecture.



(a) Area



(b) Power of the operational amplifier



(c) Power dissipation DAC

Figure 3.6: Modeling plots for analysis

4 System Design

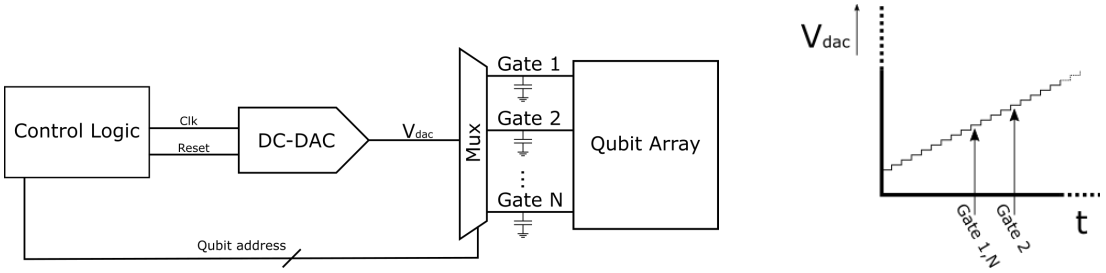
From the analysis presented in chapter 3, it becomes clear that a slope DAC based on a switched capacitor integrator yields interesting scaling properties for the biasing of spin qubits. This chapter presents a digital to analog biasing system based on the SC-integrator.

First, a system overview is presented in addition to some system level limitations. Then the core circuit is introduced and analyzed. Finally, specifications for the operational amplifier are derived and the impact of non-idealities in the operational amplifier are presented.

4.1. System Overview

In conventional DAC systems, the control logic sends the bit code to the DAC which generates a voltage based on the value of the code. The qubit address is then sent to the multiplexer, allowing the right electrode to be biased.

The target of the switched capacitor integrator is to generate the full voltage output range with very accurate steps. The voltage can therefore not be directly controlled by a bit code sent from the control logic as the voltage at the output of the DAC depends on the previous values. Instead, the control logic can only send a next or reset signal to the integrating DAC as illustrated in (a) of Figure 4.1. In the control logic, a counter will need to be present in order to keep track of the number of 'Next' pulses which have been sent previously. Then, whenever the counter matches the voltage code for a qubit, the multiplexer is set for this qubit address and opened.



(a) Integrating DAC system overview.

(b) Generated slope of V_{dac}, indication when the multiplexer is opened is illustrated.

Figure 4.1: System level functionality of the discrete integrating DAC.

4.1.1. Steady State Biasing

At cryogenic temperatures, it is expected that the leakage on capacitors is significantly reduced [39]. That means that for the hold capacitors behind the multiplexer shown in Figure 4.1, most of the charge will still be present on the capacitors. Therefore, once all capacitors have been fully charged to the right biasing voltages, relatively little current is needed to keep these capacitors at the right bias voltages.

Equation 4.1 illustrates the maximum peak current that can be drawn from the operational amplifier by a single electrode. The peak current is a function of bias voltage V_{bias}, leakage V_{leak}, noise voltage $V_{n,rms}$ and on resistance of the multiplexer R_{on}. Here it is assumed that R_{on} becomes lower once multiple gates are simultaneously connected to the DAC.

$$I_{peak} = \frac{V_{bias} - V_{leak} \pm V_{n,rms}}{R_{on}} \tag{4.1}$$

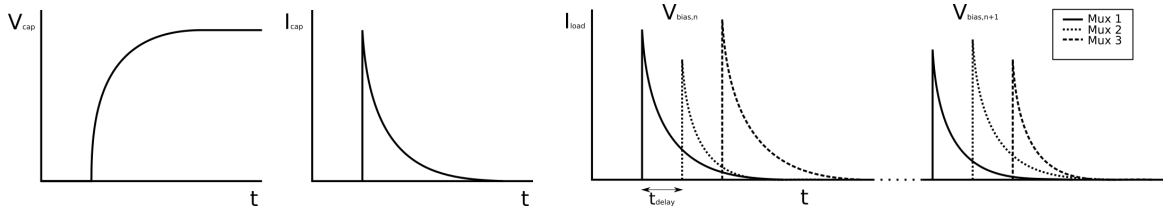
This equation illustrates that even when the gate has been properly set and $V_{leak} = 0$, the noise in combination with R_{on} can still cause current to flow from and to the electrode.

4.1.2. Initial Biasing

In Figure 3.4, the output voltage V_{out} is held by an operational amplifier. Therefore, if too much current is drawn from the amplifier, slewing will occur. When the biasing system is starting up and all capacitors are discharged, this might cause large currents to be drawn from the DAC. As the DAC is used to charge capacitors to the right bias voltages, settling behavior is expected as illustrated in (a) of Figure 4.2.

One possibility to prevent slewing from happening when doing initial biasing, is to incrementally open more multiplexer channels instead of opening all the multiplexer channels at once. This is illustrated in (b) of Figure 4.2. This causes multiple current peaks to be created which can all be below the maximally allowed I_{peak}

Another possibility is to first set voltages on the multiplexer channels coarsely. Once the coarse voltage has been set, charge is present on all gates and less current is required set the exact bias voltages.



(a) Drawn transient of voltage and current when charging a capacitor.

(b) Incrementally opening different multiplexer channels to spread the current peaks.

Figure 4.2: Voltage and current transients during startup behavior.

4.2. Offset-Compensated Switched Capacitor Integrator

The multiplexer is directly connected to the output of the operational amplifier, therefore any noise at the output of the amplifier will also be present at the multiplexer. It is known that the thermal noise of the amplifier reduces at cryogenic temperatures and its flicker noise increases, resulting in a larger 1/f corner [6]. For low-noise operation as indicated by the specifications in Table 2.2, it is therefore preferred to reduce the 1/f noise in this system. Hence an offset-compensated switched-capacitor integrator as shown in Figure 4.3 is used.

4.2.1. Core circuit

The offset compensated switched capacitor integrator works similar to the switched capacitor integrator presented in section 3.4. During Φ_1, charge is sampled on C_{add}. In addition to this, the virtual ground node at V_2 is sampled on C_h. V_2 is equal to V_+ when an ideal amplifier is assumed, resulting in C_h sampling $V_{os,i}$. During Φ_2, V_1 becomes the virtual ground node without the offset and reduced 1/f noise. This results in a more accurate integration of C_{add} and the offset $V_{os,i}$ and slow moving 1/f noise not being visible at the output.

There are several circuits that can operate as a offset-compensated SC-integrator[49, 50]. The circuit in Figure 4.3 has been chosen due to the two following reasons:

1. The circuit allows both inverting and non-inverting operation by changing the clock phases of switch M_1 and M_2. Non-inverting operation is desired as that allows an increasing output ramp to be created.

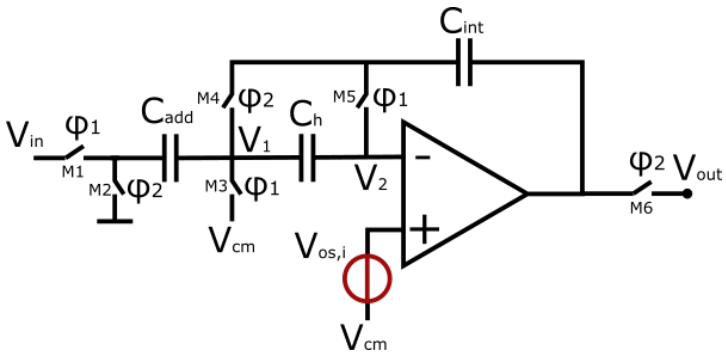


Figure 4.3: Offset compensated SC-Integrator

2. The circuit does not have a large change at the output in the different phases, which can relax the slewing requirements of the op-amp. This behavior is also desired as the op-amp will have a high voltage output stage as described in section 5.4, which will not allow for large swings at the output.

Furthermore, this circuit has the additional benefit of reducing the impact of limited gain of the op-amp. The virtual ground node V_2 is sampled and the gain error on this node is removed similar to the offset. The offset compensated output is available during Φ_2, and the switch M_6 in Figure 4.3 should be implemented by the multiplexer.

4.2.2. Voltage Step Size

In this subsection, the output voltage is shown for different phases and it is illustrated how the voltage over the integrating capacitor C_{int} increments over a single period. For this analysis, the input voltage V_{in}, common mode voltage V_{cm} and offset voltage V_{os} are assumed constant. The circuit is analyzed for non-inverting operation. The full derivation has been placed in section B.1. The relevant equations have been copied here for clarity. The LSB voltage step is shown in Equation 4.2. The output voltage of Φ_1 is shown in Equation 4.3, the output voltage of Φ_2 in Equation 4.4.

$$V_{lsb} = V_{in}\frac{C_{add}}{C_{int} + \frac{C_{add}}{(A+1)} + \frac{C_h}{(A+1)} + \frac{C_h \cdot C_{add}}{C_{int}\cdot(A+1)^2}} \tag{4.2}$$

$$V_{out,n}^{\Phi_1} = \frac{V_{cm} + V_{os} - \frac{(n-1)V_{lsb}}{A}}{1 + \frac{1}{A}} + (n-1)V_{lsb} - \frac{\frac{V_{lsb}}{A+1}\cdot C_h}{C_{int}} \tag{4.3}$$

$$V_{out,n}^{\Phi_2} = V_{cm} - V_{in}\frac{1}{1 + \frac{C_{int}}{C_{add}}(A+1)} + nV_{lsb} \tag{4.4}$$

It can be observed that in case the gain of the operational amplifier A is made infinite, the LSB step is given by:

$$V_{lsb} = V_{in}\frac{C_{add}}{C_{int}} \tag{4.5}$$

The output voltage in phase 1 becomes:

$$V_{out,n}^{\Phi_1} = V_{cm} + V_{os} + (n-1)V_{lsb} \tag{4.6}$$

And the output voltage in phase 2 becomes:

$$V_{out,n}^{\Phi_2} = V_{cm} + nV_{lsb} \tag{4.7}$$

These equations provide a coarse idea of how the waveforms in the circuit develop over time which is useful when designing and simulating the circuit. Equation 4.7 illustrates that during operation, V_{os} is effectively canceled. Equation 4.5 can be used as a design equation when determining the capacitor size.

4.2.3. Output Noise

The DAC is to be used at cryogenic temperatures and needs to meet low noise specifications. At cryogenic temperatures, certain noise sources become worse like 1/f noise, while others reduce like thermal noise [6]. Understanding the different noise sources and deriving expressions for the output noise is necessary to design the DAC such that it meets the specification.

The noise sources at the output of the DAC can be split in three different noise sources as illustrated in Equation 4.8, where ${v_{n,op}}^2$ is the noise of the operational amplifier, ${v_{n,ktc}}^2$ is the KT/C noise on capacitor C_h[1] and ${v_{n,Cint}}^2$ is the accumulated noise in C_{int}. These noise sources are covered individually in the following paragraphs.

$$V_{n,out}^2 = {v_{n,op}}^2 + {v_{n,ktc}}^2 + {v_{n,Cint}}^2 \tag{4.8}$$

Op-amp noise

For the operational amplifier, two primary noise components are considered. First is the 1/f noise, which is suppressed through the offset compensation of the integrator. Second is the thermal noise of the operational amplifier, which is expected to reduce at cryogenic temperatures [6]. As the 1/f noise is suppressed, the noise of the operational amplifier is approximated by Equation 4.9 and a 10x reduction in thermal noise power is expected at cryogenic temperatures. α in this equation represents the noise excess factor and C_o the noise limiting capacitor of the operational amplifier.

$$v_{n,op}^2 = \alpha \frac{kT}{C_o} \tag{4.9}$$

KT/C noise

In the presented circuit, KT/C noise is present on capacitors once switches are opened. This noise can be considered to be thermal noise from a switch which is band-limited by a capacitor. The noise power spectral density depends on the resistor, whereas the bandwidth of the noise is determined by the resistor and capacitor. When sampling, the entire noise spectrum is aliased, resulting in an integrated noise power as shown in Equation 4.10 [47].

$${v_{n,ktc}}^2 = \frac{kT}{C_h} \tag{4.10}$$

As this noise is caused by the thermal noise of a resistor, it is expected that the integrated noise power of ${v_{n,ktc}}^2$ will reduce proportional to the temperature down to the cryogenic operating range.

Accumulated noise

In order to derive expression for the accumulated noise, both phase 1 and phase 2 of the circuit are analyzed. The final expression of the accumulated noise in ${V_{n,Cint}}^2$ is given in Equation 4.11. The full derivation for this expression can be found in section B.2. For the derivation, it has been assumed that the bandwidth of the operational amplifier is smaller than the bandwidth of $R_{on}C_{eq}$ and that the power spectral density of the operational amplifier is higher than the power spectral density caused by the on resistance R_{on} of the switches[47, 51].

$${v_{n,Cint}}^2 = \frac{kT}{C_{int}} + \frac{nkT}{C_{int}^2}\left(C_{add} + \frac{\alpha}{C_o}(C_{add}^2 + C_h^2)\right) \tag{4.11}$$

The expression for the accumulated noise contains several components. First it contains $\frac{kT}{C_{int}}$ noise from the initial reset. The other components in the noise expression occur every cycle, and therefore are accumulated n times. The term C_{add} comes from charge noise sampled onto C_{add} which is accumulated in the integrating capacitor. The final term $\frac{\alpha}{C_o}(C_{add}^2 + C_h^2)$ is caused by the integrated noise of the operational amplifier, which results in added charge noise in C_{int} when the feedback loop is switched.

It is expected that the accumulated noise reduces significantly when operating at cryogenic temperatures. Equation 4.11 can be well used to aid circuit design and presents a few interesting trade-offs. To further improve insight, rewriting Equation 4.5 into Equation 4.11 results in Equation 4.12.

$${v_{n,Cint}}^2 = \frac{kT}{C_{int}} + \frac{nkT}{C_{int}^2}\left(V_{lsb}\frac{C_{int}}{V_{in}} + \frac{\alpha}{C_o}\left(V_{lsb}\frac{C_{int}}{V_{in}}\right)^2 + C_h^2\right)\right) \tag{4.12}$$

[1] ${v_{n,ktc}}^2$ is added due to the addition of C_h, therefore it is not present in the derivation for noise in section 3.4.

From these equations some conclusions can be made:

- It is desired to maximize the ratio of added charge versus added charge noise to limit the accumulated noise in C_{int}. In order to achieve a large ratio, a large V_{in} and small C_{add} is desired.
- Limiting n (number of integration cycles) is desired as n becomes exponentially larger with the number of bits of the DAC. In order to have the same voltage output range when reducing n, it is needed to increase C_{add}. This results in more charge noise being sampled on C_{add}, resulting in the same charge noise contribution due to C_{add}. However, limiting n helps reduce the accumulated charge noise added due to C_h. C_h turns out to be a dominant source in Equation 4.11, as C_h also needs to be sized for the KT/C noise which results in $C_h >> C_{add}$.

4.2.4. Non-idealities

This subsection covers other non-idealities in the presented circuit. First the effect of parasitic capacitances is covered, after which the effect of charge injection and gate leakage is considered.

Parasitic Capacitances

The parasitic capacitances of nodes in the circuit are illustrated in Figure 4.4. As a general consideration, the parasitic capacitances cause current to flow in different paths which can cause errors in the integration. A lot of voltages in the circuit are however static, and therefore yield the same error regardless of the output voltage V_{out}. It can be reasoned that due to parasitic capacitances gain errors are introduced, which results in an alteration in V_{lsb} compared to Equation 4.5. In case the operational amplifier has a high gain, some effects of the parasitic capacitances can be suppressed.

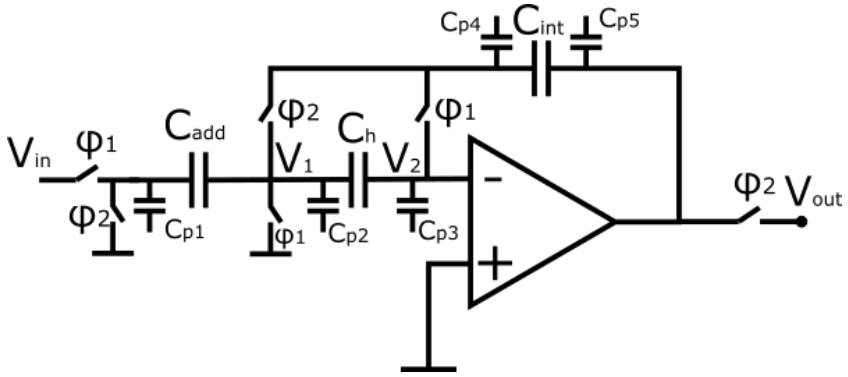


Figure 4.4: Visualization of parasitic capacitances

Charge Injection

The switches are not ideal and release charge when they are opened. The amount of charge in the channel can be described by Equation 4.13 [52]. This equation shows the dependence of the charge on the gate-source voltage of the transistors. In the designed circuit, a lot of the gate-source voltages in this topology are constant (V_{in} is constant, V_{cm} is constant, V_1 and V_2 vary slightly depending on the gain of the operational amplifier). Charge injection therefore results in a constant gain error, similar to parasitic capacitances. So charge injection has a similar effect as parasitic capacitances and result in an alteration of V_{lsb}.

$$Q_{ch} = -WLC_{ox}(V_{gs} - V_{th}) \tag{4.13}$$

Table 4.1 shows how switches M_1 - M_5 of Figure 4.3 are implemented. While pass gates can help reduce the effect of charge injection as the charge injected by PMOS and NMOS devices can help cancel each other out, only single devices have been used for simplicity and since the charge injection is constant.

Table 4.1: Implementation of the switches M_1-M_5 of Figure 4.3.

Switch	Voltage	Type
M_1	V_{in}	PMOS
M_2	GND	NMOS
M_3	V_{cm}	NMOS
M_4	$\approx V_{cm}$	NMOS
M_5	$\approx V_{cm}$	NMOS

Leakage current

There are two types of leakage currents present in the circuit, drain-source leakage caused by the sub-threshold current of a transistor and gate leakage caused by thin gate oxides. The drain-source leakage current has been shown to reduce at cryogenic temperatures [20], while there is no strong temperature dependence for the gate leakage current is expected.

In Figure 4.3 gate leakage can be considered resulting in a small DC current flowing into the amplifier. When considering the output V_{out} during Φ_2 when the output is stable, it can be observed that this leakage current flows through C_h. The output voltage V_{out} depends on the voltage held on C_h, therefore during Φ_2 voltage droop on V_{out} can be observed. This can be significant in case the circuit operates at low speeds. Additionally, it can be observed that this leakage current also flows through the integrating capacitor C_{int}, slowly altering the charge stored in the capacitor.

4.2.5. Capacitor Sizing

After analysis of the output voltage and noise of the integrator, capacitor sizes can be determined which meet the resolution and noise specifications. The values for the capacitors are given in Table 4.2.

Table 4.2: Capacitor sizes and calculated noise

Parameter	$V_{in} = 1.8$ V
C_{add}	870 aF
C_h	1.76 pF
C_{int}	34.6 pF
C_o	34.8 pF
Total allowed noise power	$175\ pV^2$
Noise power C_h (4K)	$32\ pV^2$
Noise power C_h (300K)	$2.4\ nV^2$
Noise power Op-amp (4K, 300K)	$130\ pV^2$
Allowed integration cycles	2441
Total expected noise power	$462\ pV^2$

A total integrated noise power of $175 \cdot 10^{-12} V^2$ is allowed to meet the specification of 13.2 μV_{rms} from Table 2.2. For this noise budget, a pessimistic assumption has been made that most of the noise power comes from the operational amplifier, and that the operational amplifier does not gain any improvement in terms of noise performance when cooling down to cryogenic temperatures.

For the operational amplifier noise, a noise excess factor of 1.1 is assumed, with a noise limiting capacitor of 34.8pF this results in a total thermal noise of $130 \cdot 10^{-12} V^2$ using Equation 5.2.

There is a trade-off required for the size of C_h, as Equation 4.11 shows that a large C_h results in a larger accumulated noise, while Equation 4.10 shows that a smaller C_h results in larger ${v_{n,ktc}}^2$ noise. This makes it difficult to determine an optimal value as the optimal value would depend on the number of integration cycles n. It is therefore useful to add methods that are able to reduce the number of integration cycles as is implemented in section 5.5.

In case the accumulated noise needs to be reduced, increasing the size of C_{int} can help reduce the accumulated noise power. The size of C_{add} is set by the maximum input voltage, the desired LSB step and the size of C_{int}. With the capacitor sizes indicated in Table 4.2, a total of 2441 integration

steps can be performed before the total allowed noise power is exceeded. From system level simulations, one can observe that the noise power is strongly dependent on the op-amp noise and C_h in Equation 4.11. Eventually, the total accumulated noise is heavily dependent on how the amplifier noise changes at cryogenic temperatures, as this contributes to both ${v_{n,Cint}}^2$ and ${v_{n,op}}^2$. An option to reduce the accumulated noise power, is to only switch on the offset compensation if the output is used by the multiplexer. This allows removing the C_h term from Equation 4.11 which is significantly larger than C_{add} and contributes most to the accumulated noise with the current capacitor sizing.

4.2.6. Operation Speed

Due to low leakage of the hold capacitors attached to the multiplexer channels, it is assumed that every second the voltages on these capacitors need to be refreshed in order to remain in the biasing range. Therefore, every second, the circuit should be able to generate a full ramp. The DAC is designed to have 16 bits resolution, meaning that the full scale slope consists of 2^{16} integration steps. The integrator should therefore operate at a frequency of $2^{16} \approx 65\ kHz$. This allows for a slow operational amplifier and low power operation.

4.3. Operational Amplifier

Within the design of the integrator, a core building block is the operational amplifier. This section covers the specifications of the operational amplifier as shown in Table 4.3. The primary considerations for the operational amplifier are the output voltage range, the input common mode range and the noise. The specification from the op-amp noise comes from Table 2.2.

Spec	Value
F_{clk}	65.5 kHz
Bandwidth	target during design $\approx$ 1 MHz
Input common mode	0.3 V
Output Swing	3 V
Noise power	$< 12\ \mu V_{rms}$
P_{amp}	$< 200\ \mu W$
Gain	>60dB
PSRR	>60dB

Table 4.3: Op-amp Specification table

4.3.1. Limited Gain

In case the operational amplifier has limited gain, this results in a larger voltage on the virtual ground node (V_2 in Figure 4.3). Due to the offset-compensated topology used, this virtual ground node is sampled and subtracted each phase. Therefore a limited gain alters V_{lsb} in a constant manner as illustrated in Equation 4.2. A higher gain within the operational amplifier allows for better suppression of the error voltage on the virtual ground node. The minimum specification of the gain of the operational amplifier has been set to 60dB.

4.3.2. Input Common Mode & Output Swing

The input common mode voltage together with the output swing of the amplifier determine the output range of the DAC. The output voltage can be approximated as $V_{cm} + V_{Cint}$ and with positive integration V_{Cint} becomes larger during operation. The operational amplifier should be designed such that it can handle a low V_{cm} of 0.3V. In order to have a voltage output range of 3 V for the DAC, the operational amplifier should also be able to achieve a voltage swing of 3 volt at the output. These two specifications together result in the output range of the amplifier of 0.3-3.3V, which will also be the output range of the DAC. As the circuit is single ended, it is difficult to implement the exact voltage range of 0-3V. With a V_{cm} of 0.3V, the specifications of the required 3V output range is met with a small offset.

4.3.3. Limited Bandwidth

In case the bandwidth of the amplifier is low, there is no complete settling of the integration step and a settling error is introduced. This will result in a smaller V_{lsb} step. This should pose no problem as long as the incomplete integration is constant and the circuit does not suffer from significant clock jitter.

Since the integrator operates as a slow frequency of 65kHz, it is not required to implement an operational amplifier with a large bandwidth. In order to have sufficient testing flexibility (f.e. increasing F_{clk} of the integrator), the specification for the bandwidth of the operational amplifier has been set to 1MHz.

4.3.4. Offset

At cryogenic temperatures, the effects of mismatch (the cause of offset) become worse. Therefore it is expected that the operational amplifier will have larger offset. The integrator performs offset-compensation, causing the offset to be visible at the output when switching between Φ_1 and Φ_2. It is expected that the offset is not large enough to cause undesired effects, and therefore no specification for offset has been listed.

4.3.5. PSRR

A high Power Supply Rejection Ratio (PSRR) is desired in order to prevent any noise of the supply translating to the output. The current specification of 60dB has been set based on what has previously been achieved in references at cryogenic temperatures[53].

5

Circuit Design

This chapter covers the implementation of the the system described in chapter 4 in the Intel 22-nm finFET technology. The full system is dissected in smaller components which are described in more detail in this chapter. In addition, simulations of these smaller components are shown and their functionality is verified. In the tape-out, two versions of the chip have been made. This chapter focuses on the implementation of the first version (DC-DAC V1), while also the differences of the second version (DC-DAC V2) with respect to DC-DAC V1 are covered.

The organization of the chapter is as follows. First, some considerations with respect to high-voltage and cryogenic operation are presented as these are general considerations for all implemented circuits. Then the full circuit is shown to illustrate the separate components and their interaction, after which the implementation of these individual components are discussed. Finally, the full functionality of the circuit is illustrated, including simulations and the according layout.

5.1. High-Voltage Compliance

The 22-nm finFET technology of Intel is used for creating the integrated circuit. One challenge posed by this technology with respect to the set specifications in Table 2.2, is the nominal voltage of the devices. In the technology, two types of devices are present with different nominal voltages, the thin oxide devices and thick oxide devices. The voltage compliance of these devices respectively is 1 V and 1.8 V. This means that if a 3 V output range is to be achieved, this is not trivial to achieve as it is desired not to exceed the voltage compliance of a single device for reliability purposes. How the output range is implemented in the operational amplifier is further described in section 5.4. In addition to transistors, capacitors are much used in the switched capacitor integrator. Capacitors in this technology have a voltage compliance that reaches up to 3.6V and can therefore safely be used without further considerations [54].

5.1.1. Diode stacks

Within the circuits presented in this chapter, there are two supply voltage levels, 1.8 V (VDD) and 3.6 V (VDD_{plus}). In several circuit blocks, a current goes from ground to 3.6 V. Generally, such a current branch has a current source or sink on one side, and a diode connected transistor on the other rail to bias the next transistor.

In order to allow for voltage compliance in the transistor sourcing or sinking the current, extra diode connected transistors are added in the current path as can be observed in Figure 5.3. These diode connected transistors reduce the voltage drop by several V_{th}, allowing the voltage compliance of 1.8V per device to be met.

5.1.2. Cascode transistor

Another method to help meet the voltage compliance is to add cascode transistors in the current path. By adding a properly biased cascode transistor, the source of the transistor will be set to $V_g - V_{th}$[55]. This allows control on the voltage on certain nodes and helps meet the voltage compliance of the

transistors. This method is applied in the output stage of the operational amplifier (section 5.4) and in the coarse DAC (section 5.6).

5.2. Cryogenic operation considerations

Aside from the measures taken with respect to voltage compliance, additional considerations are required when it is desired to operate at cryogenic temperatures. In literature several effects have been known to occur when moving electronics to very low temperatures. This section covers only the effects that are relevant for the technology and circuit design in this chapter.

5.2.1. Threshold increase

When moving to cryogenic temperatures, an increase in threshold voltage of transistors can be expected. Literature has shown that this occurs for both NMOS and PMOS devices similarly. Generally, operation with a large range in threshold devices should be considered. For this process, no cryogenic models are available for thick oxide devices and therefore simulation of the increased threshold voltage at these temperature is not possible. If one were to assume that thin oxide and thick oxide devices have a similar increase in V_{th}, the minimum V_{th} of thick oxide devices is approximately 400 mV at room temperature, while at cryogenic temperatures the V_{th} increases to approximately 650 mV in the typical process corner.

In the previous section, the threshold voltage of diode connected devices has been used to reduce the voltage headroom of a current source or sink. To account for the change in threshold voltage, extra transistors are added that can short a diode connected device (f.e. in Figure 5.3). This is useful in case the V_{th} at cryogenic temperatures becomes large enough to push the current source or sink out of saturation.

5.2.2. Device functionality

It has been shown that not all devices operate down to the cryogenic temperature range of 0.2-4 K. In the 22-nm finFET technology, the finFET devices have been shown to operate down to 200 mK. It is known that thin film resistors in this technology become superconducting below 1 K, limiting the temperature range in which the circuit can operate.

Some of the circuits presented in this chapter use these thin film resistors. In order to also allow operation below 1K, a second version of the chip has been made with slight alterations. These changes are made to remove the resistors present in the circuit such that operation below 1K is possible.

5.3. Circuit Overview

The full DC-DAC system is illustrated in Figure 5.1. In addition to the offset-compensated switched-capacitor circuit described in section 4.2, additional components such as the capacitive bank (C-Bank), clock & reference generation and Coarse DAC are added as well as additional components that allow for better testing functionality. The configuration bits CFG are set in a shift register.

The signals in Table 5.1 illustrate which of the signals are connected to pads, what the signal type is and what kind of voltage domain it operates in. In the following chapter, VDD is assumed to be 1.8 V, whereas VDD_{plus} is assumed to be 3.6 V.

The implementation in this chapter results in a single ended implementation of the offset-compensated switched-capacitor integrator shown in Figure 5.1. The output range of this integrator has been designed to be from 0.3-3.3 V and control of the integrator C-bank is done through the shift register. The two bits ($B_{0,1}$) are present to indicate the where the integrator slope is, as the operational amplifier is biased depending on the output voltage.

5.3.1. Extra functionality

In Figure 5.1, extra multiplexers and switches have been added in order to allow for better testing functionality, two primary functions that have been added:

1. In order to allow operation with and without offset compensation, additional control logic for M_3 and the transistor M_4 has been added.

Table 5.1: Signals that are connected to pads.

Signal	In/Out	Signal Type	Voltage domain
V_{in}, V_{cm}, V_{ref}, V_{comp}, I_{in}, VDD, VSS	In	Analog	1.8 V
$I_{bias,out}$	Out	Analog	1.8V
$I_{bias,out}$	Out	Analog	1.8 V
$B_{0,1}$, Clk, Rst, Clk_cfg_in, Data_cfg_in, Ld_cfg_in	In	Digital	1.8 V
Clk_cfg_out, Data_cfg_out, Ld_cfg_out	Out	Digital	1.8 V
V_{out}, VDD_{plus}	Out	Analog	3.6 V

2. The multiplexers (MUX) that are connected to the C-Bank allow switching the clock phases, resulting in either positive or negative integration.

5.3.2. Reset

If a single transistor is used to reset C_{int}, this transistor would have a V_{ds} equal to 3 V, which is the maximum voltage over C_{int} when the integrator is at its highest value. Therefore, a more complex reset loop is formed using M_5, M_6 and M_7 which allows for voltage compliance. During operation, M_5 and M_6 are off. As M_6 is connected to the output V_{out} which moves from 0.3-3.3 V, it is required to bias the gate of M_6 accordingly. Once the output is at 1.8 V (when B_1 is switched high), the gate of M_6 is put to 1.8 V such that it meets the voltage compliance. M_7 is present to bias the node connected to M_5 and M_6 to 1.8 V, allowing both voltage compliance over M_5 and M_6.

5.4. High-Voltage Op-Amp

The operational amplifier used is a two stage amplifier with Miller compensation as shown in Figure 5.2. As the DAC needs to have an output range of 3 V as indicated in Table 2.2, the amplifier also needs to have an output range of 3 V. This is difficult to achieve with the nominal supply voltage of 1.8 V. Therefore, a high voltage output stage is introduced which has a supply voltage of 3.6 V. M_7 and M_8 are transistors added as cascode devices in order to allow voltage compliance on node V_x and V_y during operation. The voltages can be approximated by $V_x = V_{DAC,l} - V_{th,M7}$ and $V_y = V_{DAC,h} + V_{th,M8}$. The voltage of the Coarse DAC's are controlled by $B_{0,1}$ and coarsely indicate the range of the output voltage V_{out}

As the output voltage does not change rapidly and the integration results in a single slope with expected incremental steps, this allows the coarse DACs to be slow and have large steps. This section first covers the considerations for the operational amplifier, whereas section 5.6 covers the implementation of the coarse DAC.

Due to the high voltage output range, adding a buffer to the system is not trivial, as significant switching overhead is required in order to meet the voltage compliance rules. Therefore the op-amp has currently been designed to be able to drive a large output load in the range of 200-800 pF such that an additional on-chip output buffer is not required. Alternatively, a voltage buffer on the PCB can be added which can handle the output range.

5.4.1. Sizing Considerations

For the two stage amplifier shown in Figure 5.3, the bandwidth is primarily determined by the transconductance of the input (M_1/M_2) and the miller capacitance C_m. The gain bandwidth is approximated by Equation 5.1. The total thermal noise of the operational amplifier can be approximated by Equation 4.9, which has been repeated here in Equation 5.2 for clarity.

$$GBW = \frac{g_{m1}}{2\pi C_m} \tag{5.1}$$

$$v_{n,op}^2 = \alpha \frac{kT}{C_m} \tag{5.2}$$

The equations illustrate that a large miller capacitance is needed to achieve low noise operation, however this will also reduce the bandwidth unless the transconductance of the input pair is increased.

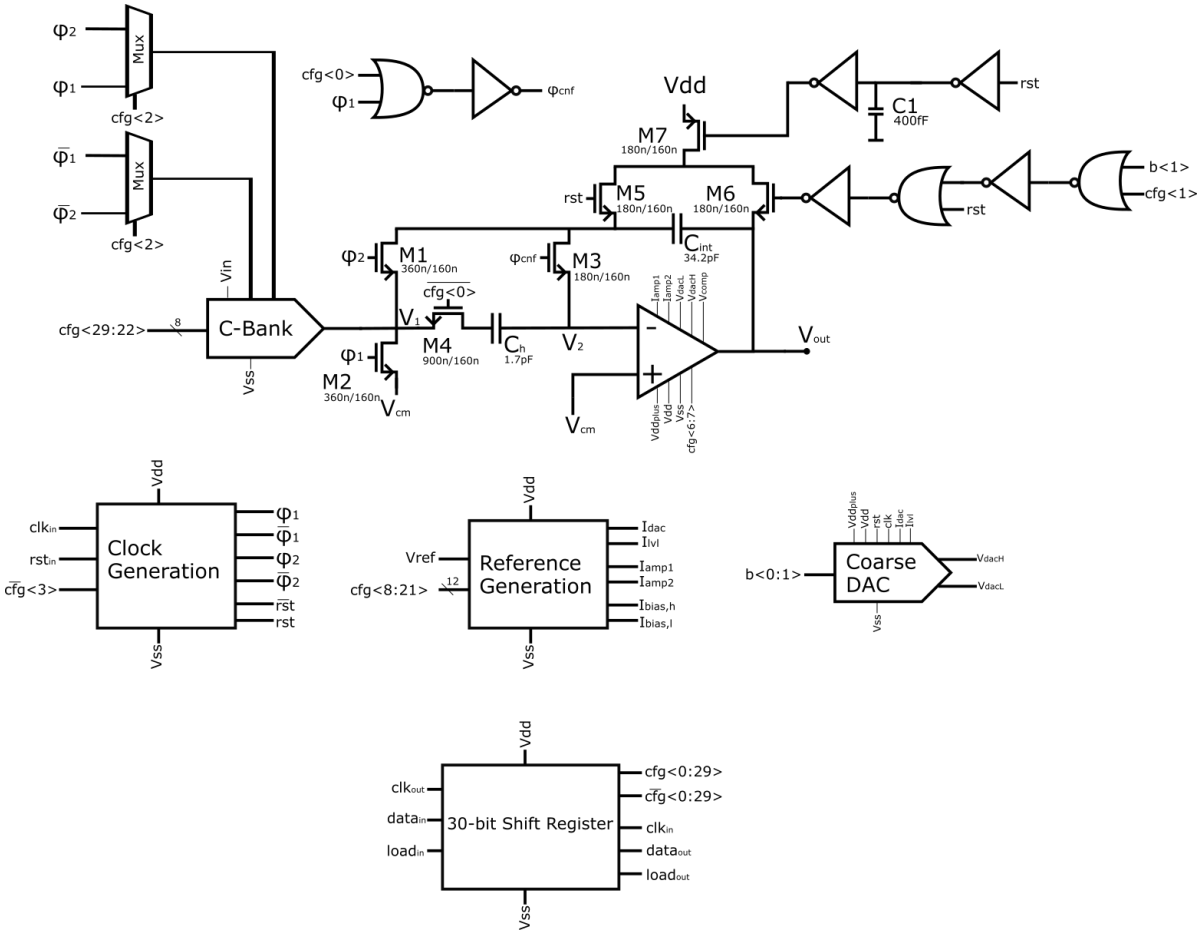


Figure 5.1: Fully implemented system, the current configuration also shows testing configurations.

The two-stage operational amplifier has initially been designed such that no systematic offset is present at the output. In order to achieve this, it is required to match the current density of M_4 and M_6 of Figure 5.2. If the differential voltage is equal to 0, $V_{ds,m3} = V_{ds,m4} = V_{gs,m4}$ due to the symmetry present. This then requires the all current in the second stage to go into M_6. Therefore requiring the current densities of M_4 and M_6 to match and causing no offset[52]. While the circuit topology cancels the offset during Φ_2, there is still switching between between Φ_1 and Φ_2 depending on V_{os} as illustrated in Equation 4.6 and Equation 4.7, which raises the argument that V_{os} should be limited.

Stage 1

The first stage is implemented with a differential input pair (M_1, M_2) and a current mirror (M_3, M_4) to yield a single ended output. As the V_+ is connected to $V_{cm} = 300\ mV$, a PMOS input pair is used. The transconductance of the first stage is of the input stage can be described with $G_m = g_{m1,2}$ and its output impedance is approximately given by $R_o = r_{o2}||r_{o4}$.Together this yields an expression for the DC gain approximately equal to $A = g_{m1,m2}(r_{o2}||r_{o4})$[55]. The DC gain of the first stage according to the sizing shown in Figure 5.2 is approximately 42dB.

With respect to noise, there are two considerations in the first stage.

1. The noise excess factor should be minimized. To minimize the noise excess factor, the contribution of $\frac{g_{m3,4}}{g_{m1,2}^2}$ as shown in Equation 5.3 should be minimized. Therefore, the sizing ratios (W/L) of M_3 and M_4 should be significantly smaller than M_1 and M_2.

$$V_n = 8kT\gamma(\frac{1}{g_{m1,2}} + \frac{g_{m3,4}}{g_{m1,2}^2}) = 8kT\gamma\frac{1}{g_{m1,2}}(1 + \frac{g_{m3,4}}{g_{m1,2}}) \tag{5.3}$$

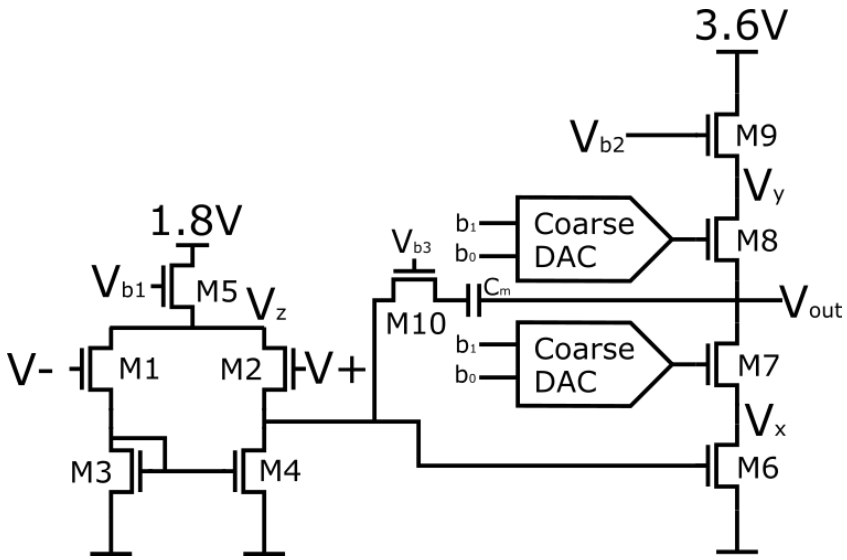


Figure 5.2: Two-stage High-Voltage Op-Amp with miller compensation. V_{b1} and V_{b2} are generated in the biasing network of the operational amplifier shown in Figure 5.3.

2. The 1/f noise corner should be close to or lower than the operation frequency of the circuit. Otherwise, 1/f noise at higher frequencies will not be fully canceled. From noise simulations, it can be seen that the 1/f noise corner is at approximately 100 kHz for an area of 28.8 μM^2. For the design presented in this report a 1/f corner of 100kHz was considered sufficient. It is expected that the thermal noise floor will reduce when moving to cryogenic operation. This consequently means that the 1/f corner will increase. However, to keep the gate leakage and the parasitic capacitance of the operational amplifier limited, the input stage was not increased further.

The input pair therefore presents a trade-off when sizing. It should be large enough to sufficiently reduce the 1/f noise corner but small enough to reduce the impact of gate leakage and parasitic capacitances.

Stage 2

The second stage of the operational amplifier is a cascode stage made from M_6-M_9. As previously mentioned, the input stage M_6 in Figure 5.2 needs to have the same current density as M_4 to prevent a systematic offset. Therefore the $(\frac{I}{W/L})_{M4} = (\frac{I}{W/L})_{M6}$. It is assumed that the gain of the first stage is large enough to make the noise of the second stage negligible, which is verified through simulation.

5.4.2. Compensation

As a two stage amplifier is used, the phase margin of the two stages without any compensation may be too low and cause it to be unstable. In order to improve the stability of the amplifier, a compensation capacitor is introduced. This capacitors splits the poles of the two stages and reduces the bandwidth. To further improve the phase response, a compensation resistor is introduced which adds a zero to the circuit. Equation 5.4, Equation 5.5 and Equation 5.6 respectively approximate the first pole, second pole and zero[52]. Equation 5.6 shows that the zero location depends on g_{m6}, to improve the tolerance against process variation, resistor R_c is implemented using a transistor biased in the triode region proportional to g_{m6}. Through simulation it has been verified that the phase margin changes less than $5°$ over the process corners.

$$\omega_{p1} \approx \frac{g_{m1}}{C_m} \tag{5.4}$$

$$\omega_{p2} \approx \frac{g_{m6}}{C_{load}} \tag{5.5}$$

$$\omega_z \approx \frac{-1}{C_m(\frac{1}{g_{m6}} - R_c)} \tag{5.6}$$

5.4.3. Biasing

The circuit used for generating the bias voltages is shown in Figure 5.3. The bias circuit takes two input currents from the reference generation described in section 5.7 and generates the bias voltages of the two operational amplifier stage separately using diode connected transistors. C_1 and C_2 are present to provide decoupling of the bias voltages.

The current in the branches is a tenth of the current in the op-amp. This helps reduce the power dissipation of the biasing network. The biasing network also generates the voltage for the compensation transistor [52]. Furthermore, a stack of diode-connected transistors is present in order to reduce the voltage headroom, here M_5 and M_8 can be used to short out a diode connected transistor.

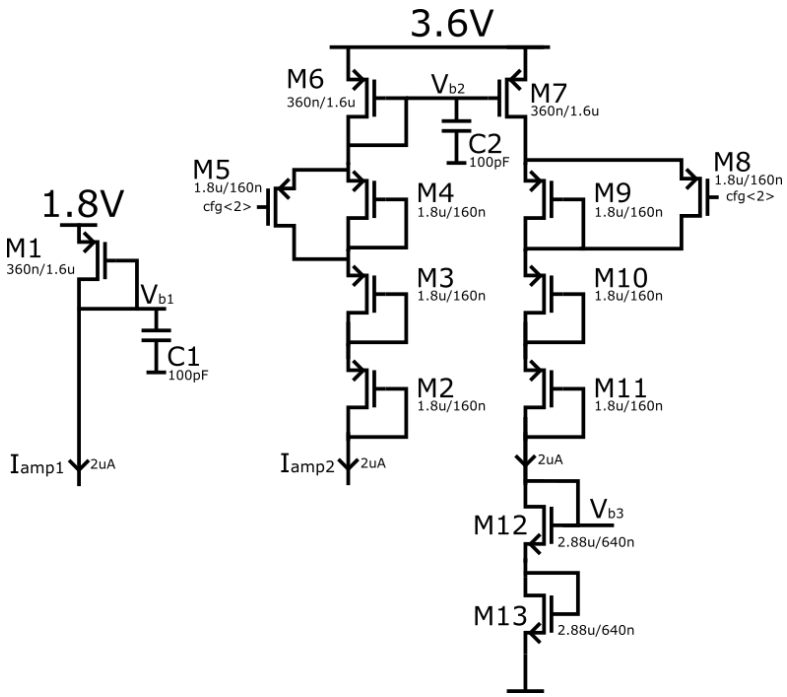


Figure 5.3: Two-stage HV-opamp biasing.

5.4.4. Layout

The two-stage amplifier has been implemented as illustrated in Figure 5.4. In the layout, the decoupling capacitors for the bias voltage lines are not illustrated. As a testing feature, double the miller capacitance has been put on chip which can be switched on or off. This allows flexibility when moving towards cryogenic temperatures.

5.4.5. Simulation

Simulations of the operational amplifier are illustrated in Figure 5.5 and Figure 5.6. Figure 5.5 illustrates the gain and phase response of both the schematic and extracted simulation, where the load is varied between 200pF-800pF. The simulation illustrates that there is a minor degradation in phase margin in the extracted version of the operational amplifier. Additionally it illustrates that the operational amplifier is able to drive a large output while maintaining a unity gain bandwidth between 500kHz - 2MHz. The achieved specifications of the amplifier have been summarized in Table 5.2.

Figure 5.6 illustrates the variation in gain and phase response as the output voltage of the amplifier changes. The gain and phase response vary, as the cascodes are dynamically biased. The gain varies between 90-140dB, where a lower gain is achieved when V_{out} is close to ground or VDD_{plus}.

Additionally, corner simulation has been performed to verify the robustness of the compensation against PVT-variations. Across the 4σ corners, the gain and bandwidth vary, however the phase response only fluctuates 5° over the corners. This validates that the compensation implemented through the triode transistor M_{10} is robust against PVT.

The integrated noise of the operational amplifier is 19 μV_{rms}, with a 1/f noise corner at 100kHz.

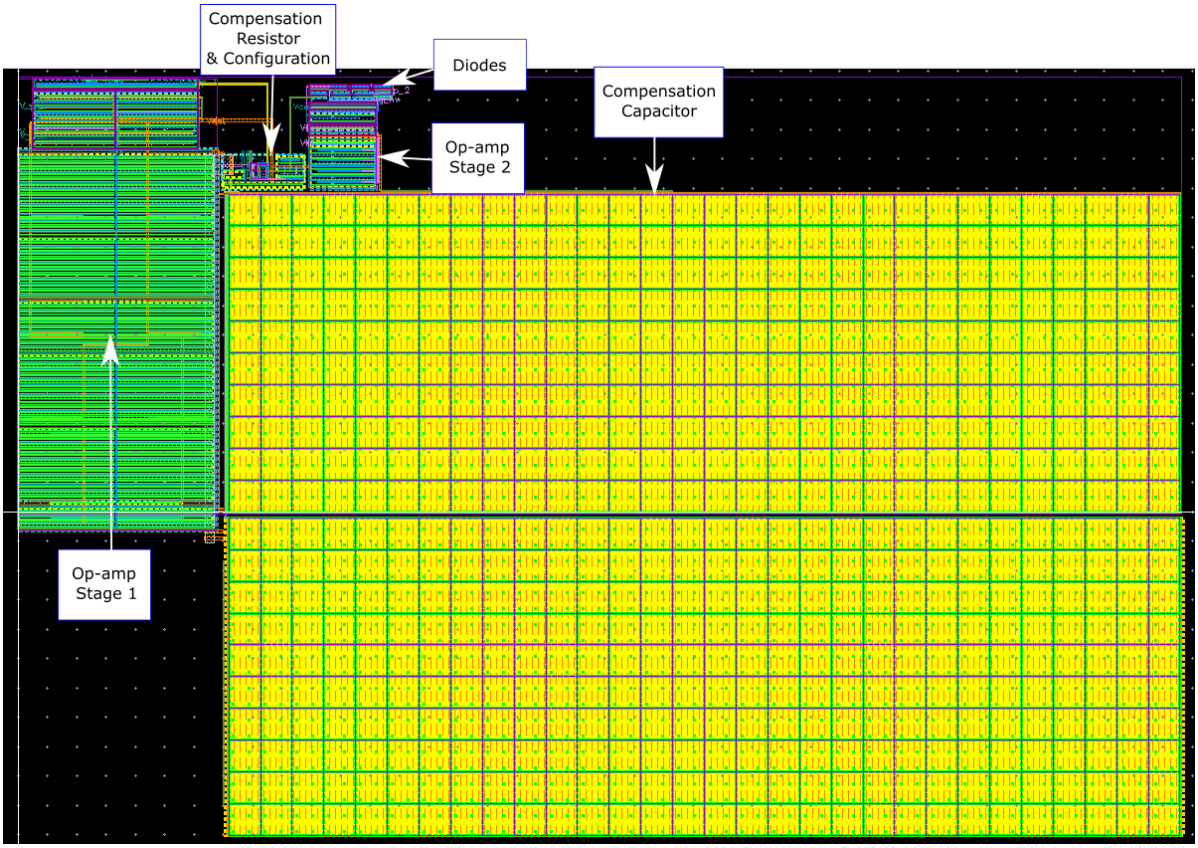


Figure 5.4: HV-opamp layout with labels. The decoupling capacitors for bias voltages V_{b1} and V_{b2} are not illustrated here.

With the reduction in 1/f noise due to the offset compensation, it is expected that the 1/f noise corner is reduced and the total noise is lower than the designed noise of 12 μV_{rms}.

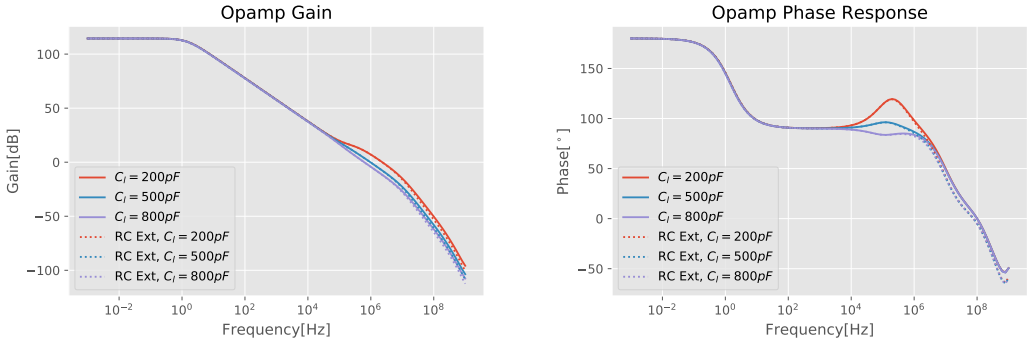
Table 5.2: Achieved Op-amp Specifications for the operating range of 0.3-3.3V. Scaling of the current can still be done and can cause specifications to change.

Spec	Value
Bandwidth ($C_l = 500pF$)	930 kHz
Input common mode	0.3V
Output Swing	3V
Noise power (T=300k, 1/f corner @ 100kHz)	19.2 μV_{rms}
P_{amp}	165 μW
Gain	93 - 142 dB
PSRR	102dB

5.5. Input C-Bank

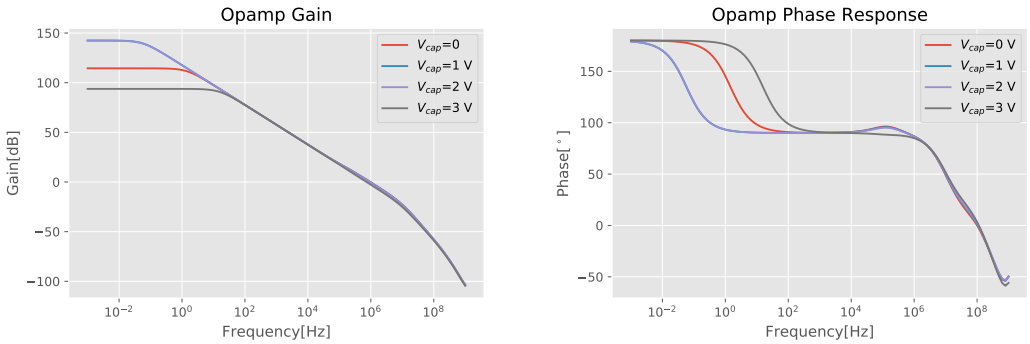
Equation 4.11 and Table 4.2 illustrate that only a number of integration cycles can be performed before the maximum allowed noise power is exceeded. Therefore, it is desired to control the size of C_{add} such that more charge can be added in a single step. Multiple input stages are designed to achieve this.

The general implementation of these input stages is shown in Figure 5.7. In total, 8 input channels are implemented with the capacitor C_{add} ranging from C_{add} to $2^7 C_{add}$ in binary steps. Transistor M_2 and M_4 are connected to the clock phases Φ_1 and Φ_2, which as shown in Figure 5.1 can be swapped in order to provide positive and negative integration. Transistor M_1, M_3, M_5 and M_6 are present in order to switch on or off a channel. When a channel is switched off, both sides of M_3 are connected to V_{cm} to prevent floating nodes.



(a) Gain Response (b) Phase Response

Figure 5.5: Schematic and RC-extracted simulations of the Op-amp AC Gain and Phase response with a variable load.



(a) Gain Response (b) Phase Response

Figure 5.6: Schematic simulations of the Op-amp AC Gain and Phase response with variable voltage over C_{int}.

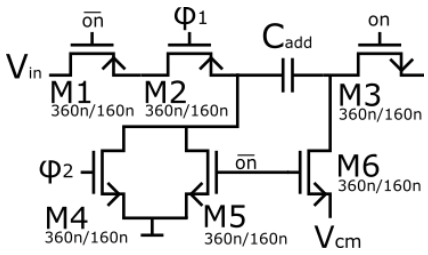


Figure 5.7: Input stage for the integrator.

5.6. Coarse DAC

For the operational amplifier, two low resolution DACs are needed to bias the cascode transistors. Estimations of the required DAC output voltage in order to bias node V_x and V_y at the allowed voltages is shown in Table 5.3. As the primary purpose of the DAC is to allow voltage compliance for all transistors, it can be reasoned that a DAC with a single bit is sufficient. In a scenario where the Coarse DAC has 1 bit, the DAC would switch once the output node V_{out} is approximately 1.8 V. However, in order to ease the transition and prevent transistors from moving out of their operating point, a two bit Coarse DAC has been designed. Table 5.3 illustrates the need for the coarse DACs to operate between 0-3.6V. For $V_{dac,L}$, the expected required output range is 0.6-2.2 V, whereas for $V_{dac,H}$ the expected output range is between 1.4-3 V. Additionally, these voltages are dependent on V_{th}, which increases at cryogenic temperatures.

These DACs have been implemented using a resistive ladder as shown in Figure 5.8. The output of the DAC is dependent on the resistive ladder and a diode connected transistor. Furthermore, M_7 and M_{10} are present in order to serve as a buffer for the voltage headroom. These transistors can be considered a cascode stage with VDD, which ensure that the voltage drop over both M_8 and M_9 does not exceed 1.8V.

Table 5.3: Approximation of the DAC voltages. V_{dsat} is assumed to be approximately 200 mV and V_{th} is assumed 400 mV

Node	Min Voltage[V]	Max Voltage[V]	Min voltage DAC [V]	Max voltage DAC [V]
V_x	V_{dsat}	1.8	$V_{dsat} + V_{th2} \approx 0.6$	$V_{th2} + 1.8 \approx 2.2$
V_y	1.8	$VDD_{plus} - V_{dsat}$	$1.8 - V_{th3} \approx 1.4$	$VDD_{plus} - V_{dsat} - V_{th3} \approx 3$

5.6.1. PVT-invariability

In order to be able to accurately set the voltage V_x and V_y, the DAC is designed such that it has robustness against PVT variations.

First, the diode connected transistors M_6 and M_{11} helps remove the dependence of the DAC output voltage to the threshold voltage of either NMOS or PMOS devices. Therefore in case the threshold increases or changes due to cryogenic operation, it should remain robust and allow accurate setting of V_x and V_y regardless of process corners or temperature change.

Second, it is desired to create an accurate voltage drop over the resistors, regardless of process variations. The accurate voltage drop over resistors is achieved through the biasing circuit shown in Figure 5.3. Here an operational amplifier is used to set the voltage drop over a resistor. This biasing current is then used in the coarse DAC, the magnitude of the current is in the order of $\approx 1\mu A$.

The biasing current is dependent on the resistivity of resistors generated during processing, therefore it is desired to accurately copy this current. One method for accurately copying this current is through cascode current mirrors. A cascode current mirror allows setting the V_{ds} of the transistor acting as current source by the cascoded transistor, at the expense of reducing the voltage headroom by V_{th}. As the increase in threshold voltage of the thick-oxide devices at cryogenic temperature is currently not well characterized, this was however not implemented in order to prevent running into voltage headroom issues.

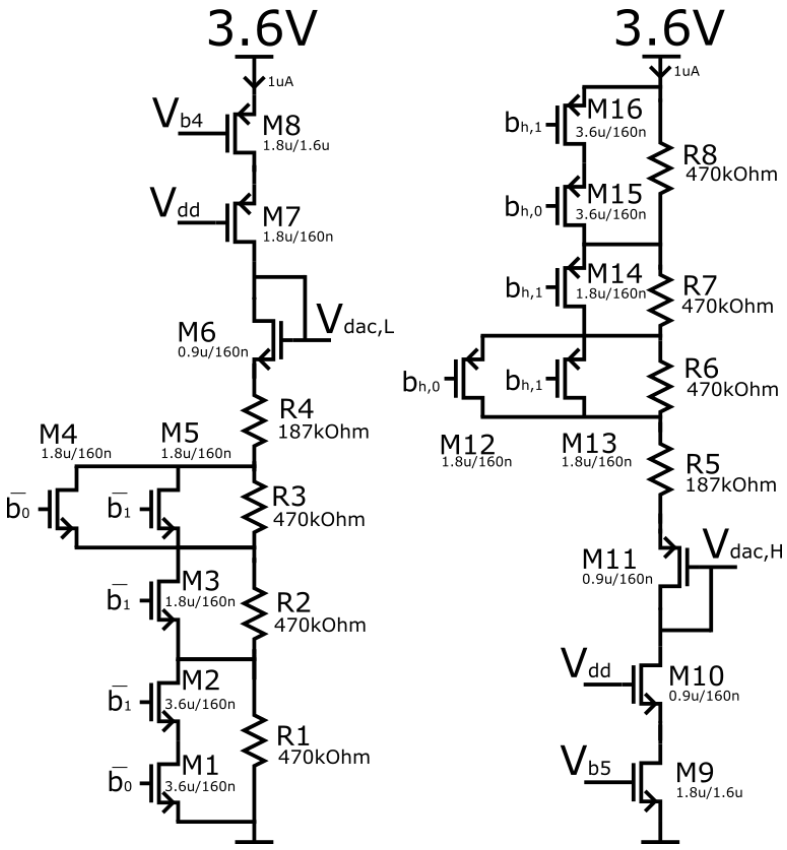


Figure 5.8: Coarse DAC implementation, left shows the low side DAC, right shows the high side DAC.

5.6.2. Digital level Shifter

In the design there are two voltage domains: 1.8 V and 3.6 V. All digital circuitry works with a nominal voltage of 0 V low - 1.8 V high digital signal (abbreviated 0-1.8 V). Considering the need for control of the coarse DAC shown in Figure 5.8, one can observe that for generating $V_{dac,H}$, the resistors and switches are attached to the 3.6 V supply rail. In order to meet voltage compliance on these switches, is is therefore not possible to use 0-1.8V logic. Instead, these switches should be controlled with digital signals that are 1.8 V low - 3.6 V high (abbreviated 1.8-3.6 V).

In order to translate a 0-1.8 V to a 1.8-3.6 V signal, the logic level shifter shown in Figure 5.10 has been designed. The biasing of the logic level shifter is done with the circuit shown in Figure 5.11. The main logic level shifter circuit translates the logic low or logic high signal to a current. This current is sent to the 1.8-3.6 V domain through a stack of diode connected transistors to allow voltage compliance. Transistor M_{16} is present such that there is a static current also when V_{in} is low. M_{16} together with the current mirror M_2 and M_3 creates a small static current through the diode connected transistor stack, allowing voltage drops over the diode connected transistors. M_{14} is an additional current source, which is turned on or off depending on the input voltage V_{in}. The created current flows through M_{15}, creating a voltage which is then buffered by two inverters (M_{10} - M_{13}), yielding the digital output voltage signal.

In order to verify functionality and robustness against PVT-corners, the logic level shifter has been functionally tested across 4σ corners and tested using Monte Carlo simulations. The Monte Carlo simulation modeled process and mismatch variation in the nominal corner, with 5000 runs it resulted in a 100% yield.

5.6.3. Coarse DAC overview

Aside from the level shifters and coarse DAC core, also D flip-flops and multiplexers are present as shown in Figure 5.12. Having the D flip-flops present helps prevent race conditions and the multiplexer allows forcing the correct DAC voltages when the integrator is reset.

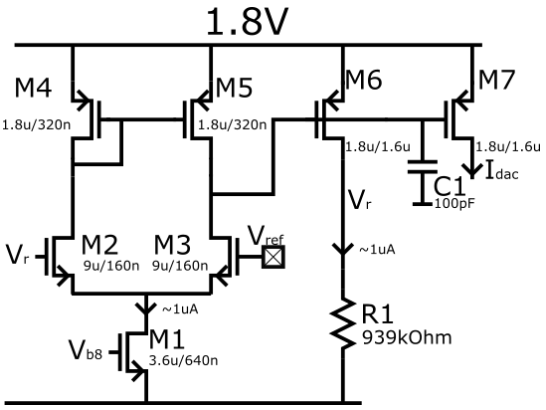


Figure 5.9: Coarse DAC bias current generation.

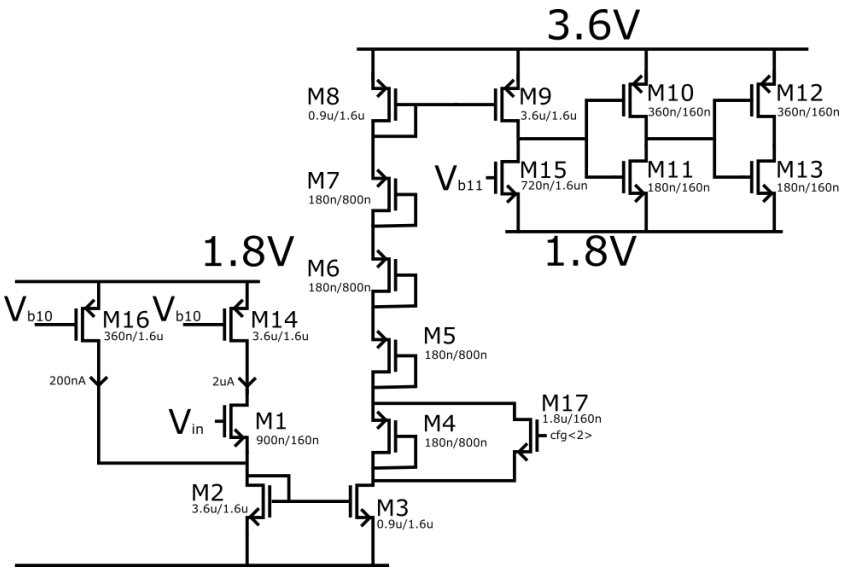


Figure 5.10: Logic Level Shifter.

5.6.4. Layout

The coarse DAC of Figure 5.12 has been implemented in Figure 5.13. In the layout, deep-nwells have been used to bias the bulk to 1.8 V and nwell to 3.6V for the 'raised' digital logic of $V_{dac,h}$.

The layout for generating the coarse DAC biasing current is in the reference block, and therefore not visible in this layout.

5.6.5. Simulation

Figure 5.14 shows simulations of the Coarse DAC voltages across the 4σ corners. In (a), $V_{dac,l}$ is plotted for a bitcode of 11, which is where the largest variations in voltages can be observed. Similarly in (b), $V_{dac,h}$ is plotted for a bitcode of 00, where again the largest variations can be observed. For $V_{dac,l}$, a variation of approximately 150 mV can be observed, while for $V_{dac,h}$, a variation of less then 100 mV is observed.

The observed variation across the corners could be reduced by increasing the gain of the op-amp in Figure 5.9 or by using cascoded current mirrors which allow more accurate distribution of the generated bias currents. The observed variation is within limits of what is allowed and therefore the current implementation of the coarse DAC should be sufficient.

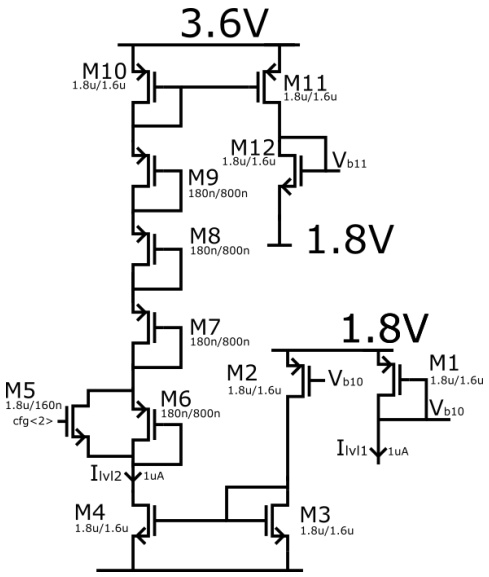


Figure 5.11: Logic Level Shifter biasing circuit.

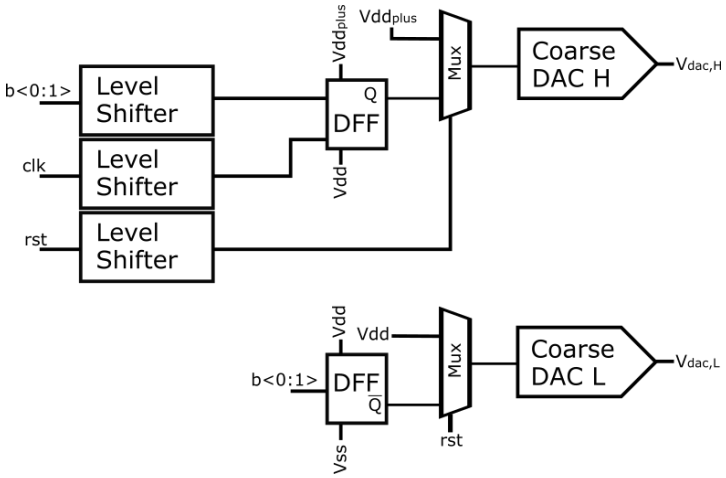


Figure 5.12: Coarse DAC with supporting components.

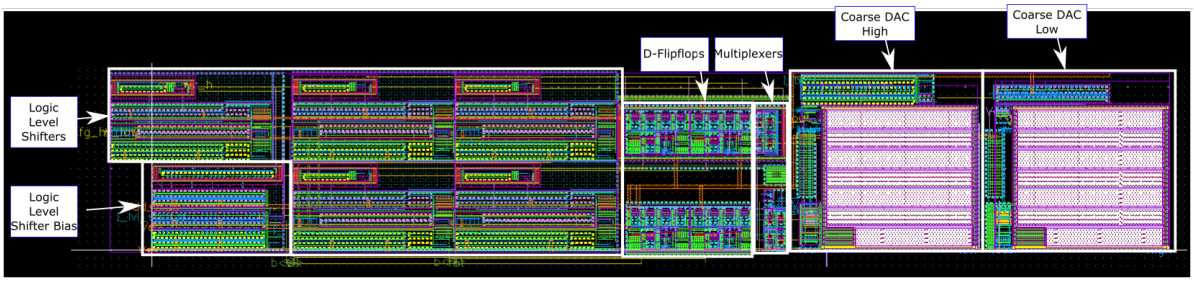
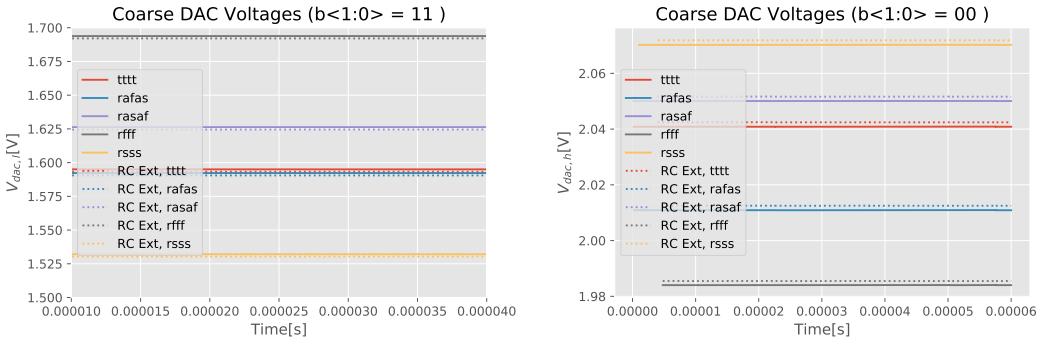


Figure 5.13: Layout of the Coarse DAC depicted in Figure 5.12



(a) $V_{dac,l}$ for a bitcode b<0:1> of 11

(b) $V_{dac,h}$ for a bitcode b<0:1> of 00

Figure 5.14: Schematic and RC-extracted simulations of the Coarse DAC across corners.

5.7. Reference Generation

The current generation of the operational amplifier is generated by a gm-reference circuit. The circuit which is used for this is shown in Figure 5.15. The main gm-reference is formed with M_{1-4} and R_1. In addition, it is possible to use an external bias current through transistor M_{5-7}. In the circuit, two I-DACs are present to bias the two stages of the operational amplifier independently. For the first stage, an I-DAC with 5 bits is present, for the second stage an I-DAC with 7 bits is used. The generated bias current is used in the digital level shifter and a copy of the bias current is connected to a pad, which allows verifying the functionality of the reference generation.

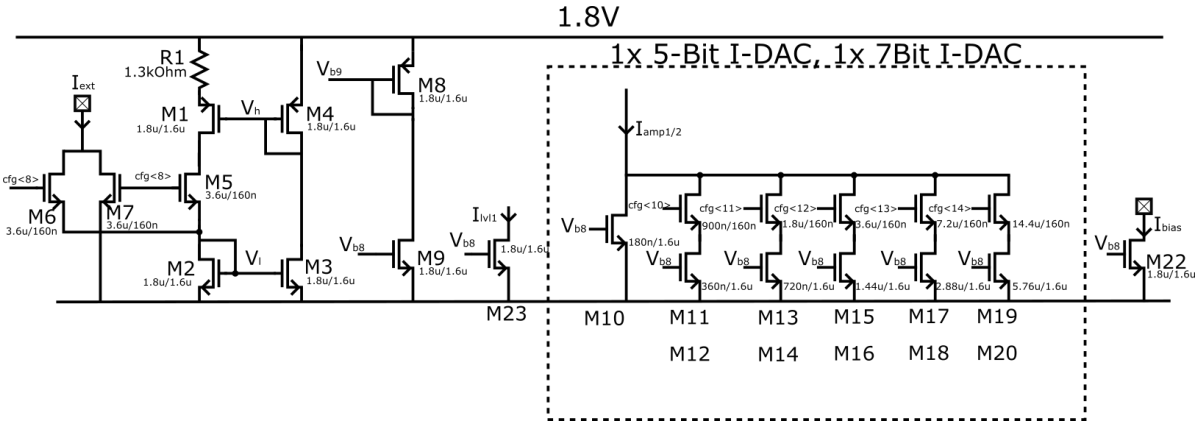


Figure 5.15: GM reference implementation.

5.7.1. Startup Circuit

A gm-reference block as shown in Figure 5.15 has two stable operating points, one operating point is when there is no current present (circuit is off), the other is when there is a current which depends on R1. A startup circuit is needed to move it to the right operating point[52, 55]. The startup circuit which is commonly used is a stack of diode connected devices between the nodes V_h and V_l. In case the circuit has no current flowing, $V_h \approx 1.8\ V$ and $V_l \approx 0\ V$. If a stack of diode connected devices is connected between these nodes, a current can flow that allows the circuit to start. Using such a diode connected stack of devices is however difficult when there is a large variation in V_{th}, as an increase in threshold voltage can stop the startup circuit from working.

As an alternative solution, the startup circuit shown in Figure 5.16 is implemented. This startup circuit relies on a pull-up transistor M_8. By default, when switching from an external source to the gm-reference (CFG_8), a pulse is generated which briefly pulls up the node V_l to 1.8V, creating a startup current. This pull-up transistor can also be forced on by enabling CFG_9, which together should allow robust startup of the gm-reference.

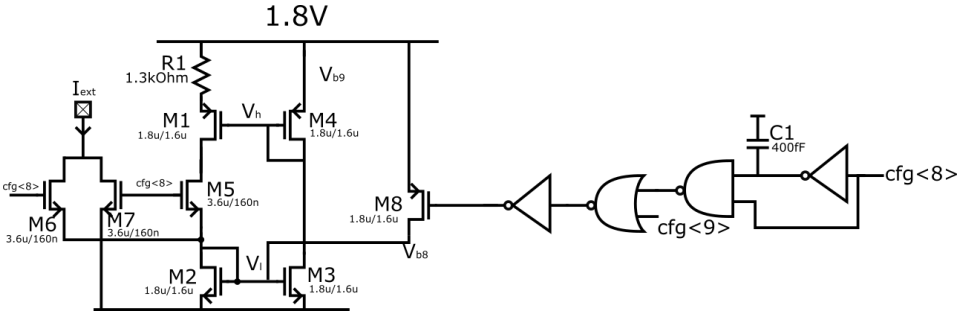


Figure 5.16: Startup circuit for GM reference.

5.8. Clock Generation

It is desired to use a non-overlapping clock for the integrator. In order to implement this non-overlapping clock, the circuit in Figure 5.17 is used. In addition to generating the clock, it is also possible to force Φ_1 high when the reset is high. With a C_1 and C_2 of 400 fF, a non-overlap of approximately 1.8 ns in the nominal process corner is achieved.

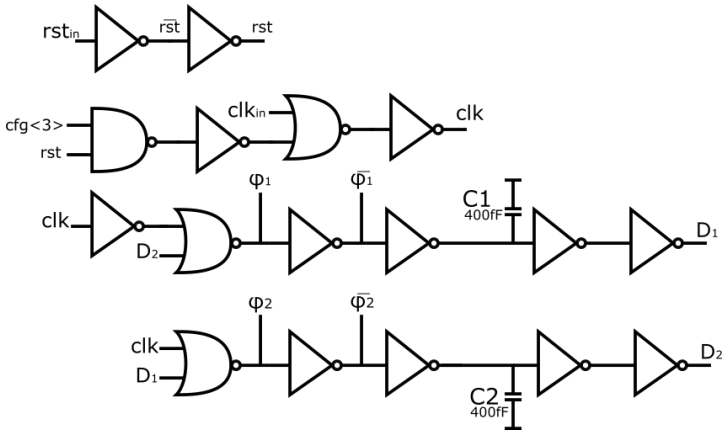


Figure 5.17: Non-overlapping clock generation circuit.

5.9. Second chip modifications

As the desired operating range of the DAC is 0.2-4 K, there is an issue arising as resistors in this process are superconducting below 1 K. A second version of the chip has therefore been made which removes all resistors used. There are two circuit blocks affected by this change:

1. The Coarse DAC has a connection to a pad instead of to a resistive ladder as shown in Figure 5.18. This allows for off chip components to generate the correct bias voltage for the chip.

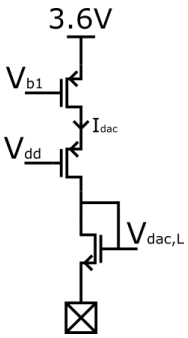


Figure 5.18: Altered version of the Coarse DAC.

2. The gm-reference circuit, where the resistor has been replaced with the R_{on} of a PMOS device.

In addition to the removal of resistors, M_1, M_2 and M_3 shown in Figure 5.1 have been replaced with pass-gates in order to better compensate charge injection. The changed layout of the DC-DAC V2 is illustrated in Appendix C.

5.10. Full Circuit

This section contains a layout overview and simulations of the full DC-DAC. All of the layout and simulations presented here are for Version 1 and is the implemented version of Figure 5.1. In addition to the circuit components in this chapter, a few test devices have been added on chip which allow quick characterization of the threshold voltage at cryogenic temperatures.

5.10.1. Layout

The layout of the full DAC can be observed in Figure 5.19. Here, in addition to the layout shown in Figure 5.4 and Figure 5.13, the multiple input channels, C_{int}, C_h, the reference generation, clock generation and shift register are shown. The core area of the circuit, without the decoupling capacitors for the bias voltages has a total area of 0.078 mm^2.

5.10.2. Simulations

Simulations of both the schematic and extracted DC-DAC can be seen in Figure 5.20. In these simulations, the output voltage is plotted together with the node V_x and V_y of Figure 5.2 which illustrates correct biasing of the intermediate nodes by the coarse DAC. The voltage step made by V_{out} has been plotted and is taken as voltages exactly F_{clk} apart. It can be observed that the voltage step of the RC-extracted simulation seems to be a lot more noisy which is due to convergence of the simulator. The average step of the RC-Extracted simulation is $45.1\ \mu V$, which is slightly increased compared to the schematic $44.7\ \mu V$. The slight increase is expected to come from parasitic capacitances.

There is some switching of the output voltage V_{out} observed between Φ_1 and Φ_2, which is caused by switching of the feedback loop. The switching between the feedback loops results in a small step of V_{out} in the order of a few hundred μV. It has been observed in case the offset-compensation is turned off, this switching does not occur.

Zooming in on a single period, it can be observed that the settling of both the schematic and RC-extracted simulation is according to expectation. The settling appears to be quick, matching the behavior of the operational amplifier with a phase margin close to 90°.

Simulating the full noise behavior requires a long amount of time, as the full slope would need to be simulated, which is 2^{16} integration steps. As the noise of interest is in the aliasing and folding of high frequency noise, this has to be simulated with small time-steps, resulting in long simulation times. In order to verify the noise behavior, a periodic noise simulation has been ran on a single period with two different hold capacitor sizes as illustrated in (a) of Figure 5.21. This illustrates the effect of offset compensation and the aliasing of noise on C_h. In Φ_2 the offset compensation reduces the 1/f noise corner by a factor 100, while the aliasing of noise on C_h increases the thermal noise floor. During Φ_2 at 300 K, the total integrated noise is 17.0 μV_{rms} which is expected to reduce at 4 K as the aliased noise on C_h will become lower.

To verify the functionality across corners, a corner simulation has been ran and the resulting voltage step at the output has been provided in (b) of Figure 5.21. In the tttt, rafas and rsss corner, there are 'slow' PMOS devices and the achieved voltage step is similar. There is a large observed difference with the rfff and rasaf corner where fast PMOS transistors are present. The voltage step is smaller due to the leakage current going into the operational amplifier, which is larger for fast PMOS devices.

The simulated performance of the DAC is listed in Table 5.4. As the noise has proven difficult to simulate properly and no conclusive noise simulation has been performed, no definitive value for the noise is added in this table. Based on the analysis in subsection 4.2.5, it is expected that the DC-DAC will meet the noise specification as the presented analysis assumes that no improvement in amplifier noise will be present. At 4 Kelvin, it is expected that the total amplifier noise will reduce, allowing for a lower total noise power (Equation 4.8) at the output of the DC-DAC and a lower accumulated noise(Equation 4.11).

Table 5.4: Simulated DC-DAC Performance.

Specification	Target Value (T = 4 K)	Achieved Value (T = 300 K)
Resolution (V_{lsb})	50 μV<	45.1 μV
Voltage range	3 V	3 V
Integrated Noise (In Φ_2)	13.2 μV_{rms}	17.0 μV_{rms}
Op-amp	12.0 μV_{rms}	19.2 μV_{rms}
P_{DAC}	1 mW<	187 μW
Linearity	Monotonic	Monotonic
Output load	>14 pF	500 pF

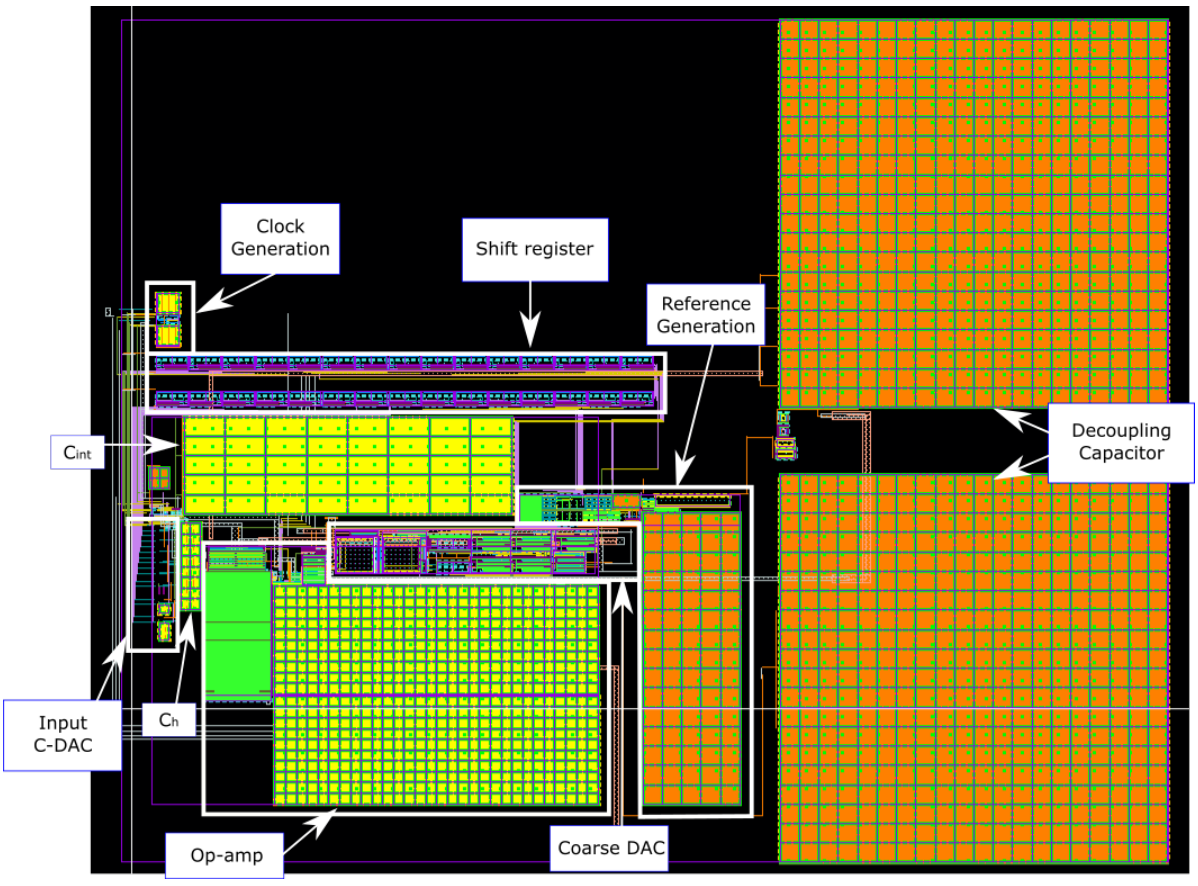
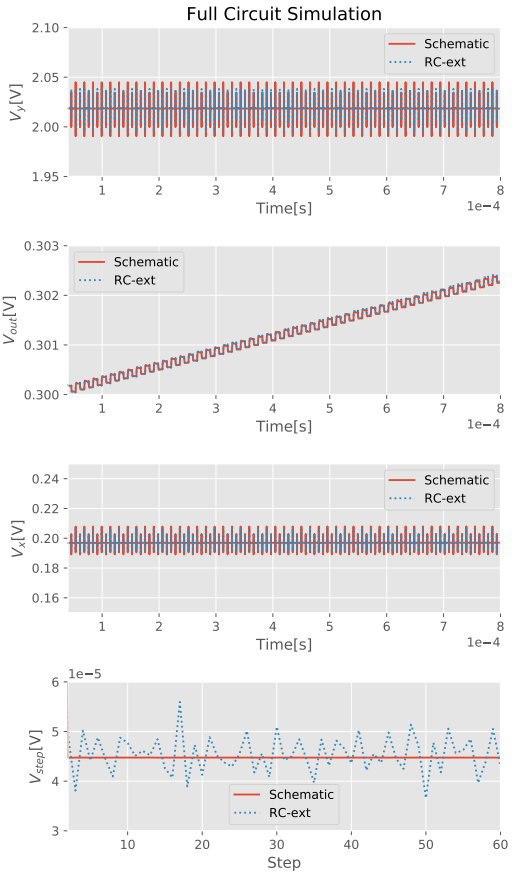
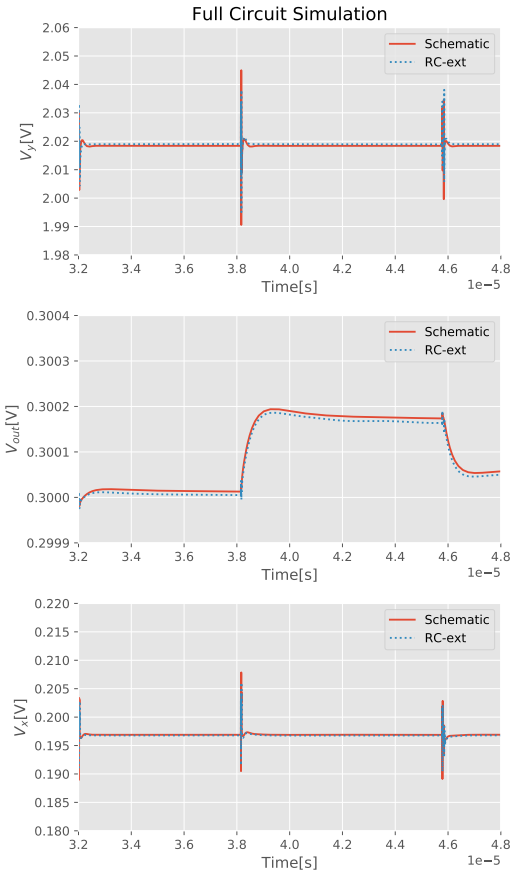


Figure 5.19: Full DC-DAC layout without the IO ring.

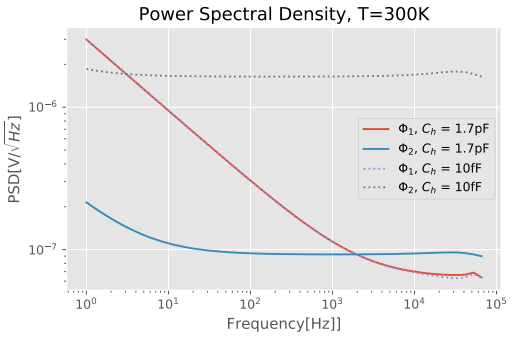


(a) Schematic and RC-extracted simulation of the full DC-DAC

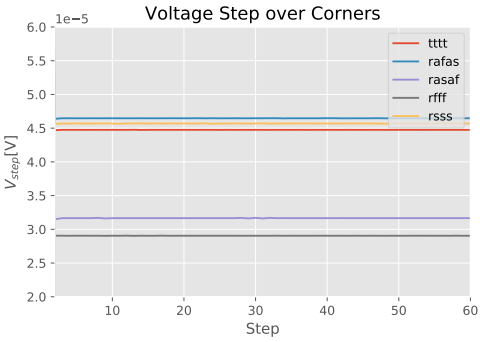


(b) Schematic and RC-extracted simulation of a single period

Figure 5.20: Schematic and RC-extracted simulations of the DC-DAC, also showing the intermediate node V_x and V_y of the operational amplifier.



(a) Periodic noise simulation, using two different capacitor sizes to show the KT/C noise aliasing on the hold capacitor C_h.



(b) Schematic simulation of the voltage step across corners

Figure 5.21: Additional simulations of the DC-DAC, illustrating the noise and variability of the DC-DAC step across corners.

6 Measurement Plan

This chapter elaborates on the measurements to be done when the chip has been received. The measurement plan can set requirements for the PCB and surrounding components of the chip.

First the measurement targets are discussed, after which a setup to measure the chip performance is presented with focus on critical components and how cryogenic measurements are to be performed.

6.1. Measurement Targets

As previously mentioned, some of the device behavior at cryogenic temperatures is not fully known and simulation of devices at these temperatures is currently not possible. The following verification is desired in order to characterize the performance of the DAC:

- At both *room temperature* and *Cryogenic temperatures (4K)*
  - Measure the test devices
  - Characterize the Op-amp:
    - Gain
    - Settling
    - Noise without offset compensation
    - Noise with offset compensation
  - Characterize the SC-Integrator:
    - Step sizes V_{lsb}
    - Charge injection
    - Droop at the output
    - kT/C noise
    - Accumulated noise
    - Power dissipation

In order to enable these measurements, different testing modes as have been implemented on the chip have to be used. The op-amp can for example be used as a unity gain buffer by disabling the offset compensation and enabling the reset, allowing characterization of the gain and response.

With these measurements, it can be verified whether the integrator meets the designed specifications of Table 2.2. After verification of the specifications has been done, the DAC can be used together with the multiplexer to create the qubit biasing system as illustrated in Figure 6.1 in order to perform biasing experiments on a qubit sample.

6.2. Setup

In order to perform the measurements of section 6.1, a PCB is to be designed which allows debugging of the chip, allows operation at cryogenic operations and enables the measurements of the desired

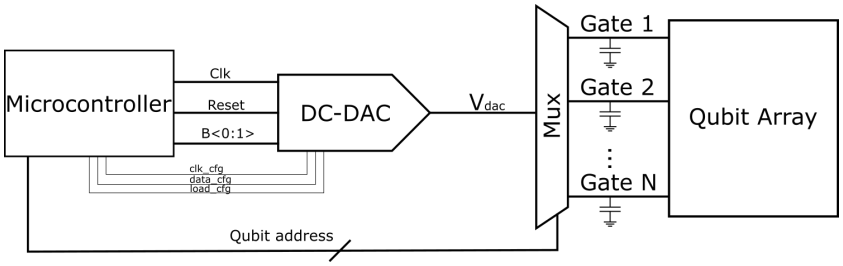


Figure 6.1: System overview for DC biasing of qubits

specifications. This section first discusses the methods of temperature control available and constraints posed by these methods, after which other considerations for the PCB and measurement setup are discussed.

6.2.1. Components at cryogenic temperatures

Integrated circuits and passive devices such as capacitors and resistors are generally developed and tested at temperatures above -55 $^{\circ}C$. The behavior of these devices is therefore unknown at cryogenic temperatures. In case active or passive components are to be used at cryogenic temperatures, it is important to first fully verify the behavior of the component individually at cryogenic temperatures. For instance, it is undesired to have a resistor that becomes superconducting or a LDO that malfunctions when operating at low temperatures. Previous work has shown operation of components at 4 Kelvin, though the performance of these components does change at these cryogenic temperatures[18].

As a rule of thumb to minimize the testing overhead, components are to be places at room temperature where they have been designed for. In the current test setup, only passives and a voltage buffer are to be placed on the PCB that is put at cryogenic temperatures.

In [56], operation of several operational amplifiers has been shown at 4 Kelvin. As an optional off-chip voltage buffer is to be implemented, the Analog Devices AD8651 or AD8605 can be used. For passive components such as capacitors and resistors, devices tested and listed in [18] will be used.

6.2.2. Temperature Control

Reaching and maintaining cryogenic temperatures is not trivial. Therefore, this section introduces the two options for reaching these temperatures that can be used with the designed chip; using a helium dewar and using a Dilution Refrigerator (Figure 6.2).

Using a cryogenic probe-station is also an option, however this is not considered here as the probe-station is generally more useful for characterizing single devices and more control wires and voltages are required for the designed DAC.

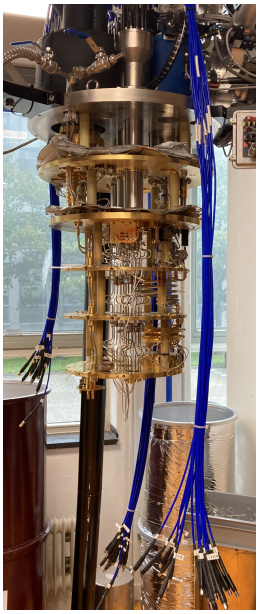
Helium Dewar

A helium dewar is a large container of liquid helium which has a temperature of 4.2 Kelvin. The minimum temperature that can therefore be achieved in a dewar is 4.2 Kelvin. In order to cool the chip down, a PCB with the chip is mounted on a long rod, which is submerged into the liquid. While this allows a stable minimum temperature, it is difficult to measure at temperatures between 4.2K and room temperature as there is not active temperature control present. Within the AQUA research group, this has proven to be an effective method to perform cryogenic measurements.

A large rod, also referred to as dipstick, is used to connect the submerged PCB to room temperature equipment and control. Therefore it is good to consider the inputs and outputs required for the PCB, as the dipstick can only have limited wires to room temperature. Within the AQUA research group, different dipstick have been created that are able to carry more than 10 signals to the submerged PCB.

An advantage of using a helium dewar is that cooling down to cryogenic temperatures happens fast, and there is quite some cooling power available at the minimum temperature of 4.2K. For characterization of the DAC, operating in a helium dewar is preferred, as it allows for quicker measurements, debugging and also a larger power consumption due to the available cooling power.

(a) Helium dewar in an active measurement setup.



(b) Opened Dilution refrigerator.

Figure 6.2: Setups that can be used to perform measurements at cryogenic temperatures.

Dilution Refrigerator

A dilution refrigerator actively uses different helium atoms to reach low temperatures[57]. Unlike the helium dewar, the dilution refrigerator can reach temperatures below 4K. Taking the BlueForce BF-H400 dilution refrigerator as an example, one can observe that at low temperatures such as 200mK the cooling power is limited to approximately $200\mu W$. In addition, the time required to cool down to cryogenic temperatures is larger compared to a helium dewar[41].

For testing the multiplexer with the qubit sample, usage of the dilution refrigerator is required as it is expected that the qubit samples will require temperatures of approximately 200mK to operate.

6.2.3. Sensitive nodes

When considering the design of the integrator in Figure 4.3, one can observe that the quality of certain voltages can limit the observed performance. For example, if V_{cm} suffers from significant fluctuation, this will directly translate to the output of the DAC. In total, 4 bias voltages are required for the DAC as illustrated in Table 5.3.

In order to create stable voltages with low noise and enough supply rejection, low dropout regulators (LDO's) with adjustable output voltages should be used. LDO's can operate at both at room or at cryogenic temperatures[18], though at cryogenic temperatures the performance differs from what it is designed compared to room temperature.

6.2.4. Output Measurement

The DAC has a large voltage range in combination with a small LSB step. In addition the voltage held by the DAC is not completely static due to non-idealities such as droop. In order to be able to accurately characterize the DAC an acquisition card and a bench-top multimeter will be used at room temperature. Together the combination of the acquisition card and multimeter should have:

- Sufficient bandwidth to accurately capture the transient response of the DC-DAC
- Sufficient resolution to measure the V_{lsb} voltage step
- Low enough noise to allow measurement of the DC-DAC noise

An acquisition card available within the AQUA group is the Spectrum M2p.5911-x4[58]. This card has an RMS noise voltage of 10 μV_{rms} at the smallest input range, which is good enough to measure the

response and possibly the resolution of the voltage step. For noise measurements a lower noise floor is required as the 10 μV_{rms} is close to the specified 13.2 μV_{rms} the DAC is designed for, which is why a bench-top multimeter is also included in the measurement setup. Especially for noise measurements at cryogenic temperatures this is a relevant consideration as the noise of some components are expected to drop significantly.

6.2.5. Full measurement setup overview

Based on the descriptions provided in this section, the preliminary measurement setup as shown in Figure 6.3 has been designed for the characterization of the DC-DAC.

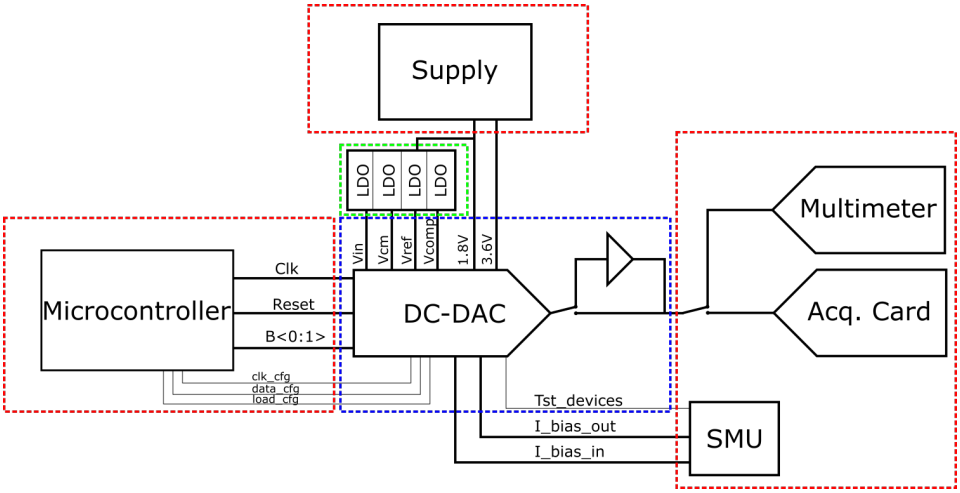


Figure 6.3: Preliminary measurement setup. The dashed squares indicate the operating temperature of the components, red indicate room temperature, blue indicates cryogenic temperatures and green indicates possibly room temperatures with the option to operate at cryogenic temperatures.

7

Future Work

Recommendations for future work are presented in this chapter. The future work does not only cover the DC-DAC, but also its operation in combination with the full biasing system. On a system level, recommendations for future work are possible that can help make the DC-biasing of spin qubits more efficient.

C-DAC

In theory, the approach of voltage based biasing which is utilized by the SC-integrator can be implemented through a C-DAC. This could yield a slightly more efficient DAC in terms of area and power consumption. Especially at cryogenic temperatures a C-DAC implementation can be interesting, as the C-DAC can hold a voltage well due to the low leakage.

One issue for implementing such a C-DAC in the chosen 22-nm process is however that the voltage compliance becomes a larger issue. A C-DAC usually has large switching at the output when going from reset to its output voltage. Therefore an operational amplifier with a high voltage output stage described in section 5.4 might not be able to meet the voltage compliance.

Operational Amplifier

Currently, the implemented operational amplifier is a two-stage amplifier with a high-voltage output. This allows voltage compliance with the required output range at the cost of some flexibility of the operational amplifier.

One can for example imagine that a single stage amplifier is used in combination the the multiplexer. In this scenario, the noise limiting capacitor of the amplifier is limited by the load capacitance, assuming that the 1/f noise is successfully canceled. The multiplexer can be used to dynamically scale the output load. Multiple output channels can be left connected, allowing a larger noise limiting capacitor. Dynamically scaling the output load can be done in order to meet the required noise performance. With the two-stage amplifier presented in section 5.4 this is not possible, as the bandwidth and noise performance is limited by the internal miller capacitor.

Alternatively, one can attempt to dynamically bias the single-stage amplifier according to the capacitive load. For a single stage amplifier this is easier to achieve, as generally less issues with instability are present.

Process

The current chips have been successfully implemented in the Intel 22-nm finFET process. While the process has some advantages, such as a high f_t and high mobility, the voltage compliance and gate leakage[1] do not make it the most suitable technology for this application.

The voltage compliance reduces the degree of freedom there are for a designer, as overhead in the circuit need to be implemented to limit the voltage as illustrated in section 5.4 or section 5.6. While the gate leakage is comparatively low when comparing the thick-oxide to the thin-oxide devices, it can still be significant as the DC-DAC currently targets operation at low frequencies.

[1] Even with Thick oxide devices, the effect of gate leakage can be significant as finFETs have a larger effective gate area.

Moving to a larger technology could therefore be beneficial, as in larger technologies the voltage compliance is generally larger and the gate leakage current of devices is lower due to thicker oxide thicknesses. An alternative option could also be to introduce a new flavor of devices in the Intel 22-nm process that allow voltage compliance with the required output range.

Leakage

In this thesis, two kinds of leakages are of interest. The drain-source leakage that allows for the discharging of the hold capacitors behind the multiplexer, and gate leakage that causes a DC current to flow in the amplifier.

Gate leakage is the primary factor that limits how well the DAC can hold a voltage, as the DC current flows through C_h during Φ_2. It could be of interest research whether compensation of the gate leakage can be done as otherwise increasing the size of C_h is required, which already has a trade-off as described in subsection 4.2.5.

Monitoring the drain-source leakage experienced on the Multiplexer provides useful information, as this allows determining how often the bias voltages need to be refreshed. With this information, the DAC can be turned off when refreshing the bias voltages is not yet needed.

Operating Speed & Phases

The current implementation of the DC-DAC is designed to generate a 16-bit full scale output voltage range every second. The estimate of requiring a full slope every second is based on the fact that the leakage voltage on the sample and hold capacitors is sufficiently low. There is a trade-off for the operating speed of the DAC. A fast operating integrator will require a higher speed operational amplifier, but it will also be able to better reduce the 1/f noise and have less effect from gate leakage of the amplifier. This will therefore be more power consuming, but also allow for faster operation. In such a scenario, it is possible to switch off the DAC most of the time.

Additionally, the phases Φ_1 and Φ_2 have been assumed to be balanced thus far in this work, however it could be of interest to increase the duration of Φ_2 to increase the validity of V_{out}. In case faster operation is achieved, it is also important to consider the speed and timing accuracy with which the multiplexer can switch on and off channels.

Distribution of Biasing voltages

Currently, the specification of the DC-DAC has been set up as illustrated in chapter 2. These specifications have been set up with coarse and pessimistic assumptions on the required biasing voltages required. It can be well possible that out of the designed operating range of 3V, only 1V of the output range is frequently used. Based on this information, design or operation of the presented DC-DAC can be altered. For example by setting the initial V_{cm} just below the first required voltage, reducing the number of integration steps required to get to the first voltage.

8

Conclusion

This thesis presents the analysis and design of a DC-DAC operating at cryogenic temperatures. First, specifications required for the biasing of spin qubits are derived, after which a modeling study is done in order to determine an efficient and scalable biasing architecture. Then circuit design equations for the selected architecture are derived and an implementation of the DAC in the 22-nm finFET Technology of Intel is given. Finally, preliminary ideas for the measurements are presented that will be used to verify the specifications of the DAC and ideas for future work are given.

In order to allow scalibility with the number of electrodes that need to be biased to create qubits, the thesis proposes using a voltage based biasing approach opposed to address based biasing. Through voltage based biasing, once a voltage is generated, all electrodes that need this voltage are connected to the DAC simultaneously or consecutively. This prevents switching losses associated with generating the biasing voltages for each electrode separately, and allows decoupling of the power dissipation of the DAC to the number of electrodes that are present.

Taking into account the change in noise sources at cryogenic temperatures, an offset compensated switched capacitor integrator has been chosen as DAC architecture and thoroughly analyzed. Design equations for the circuit have been set up, allowing conscious trade-offs when determining the capacitor sizes and the effect of non-idealities in the circuit have been presented.

The DC-DAC has been implemented in the 22-nm finFET technology of Intel and features circuit components such as a high-voltage output stage of the operational amplifier and a coarse DAC to guarantee voltage compliance with the required voltage output range. The achieved specifications during simulation of the DAC are summarized in Table 5.4. While measurements at cryogenic temperatures still have to be performed, the circuit has been designed to be robust against PVT variations and takes into account large variations in V_{th}, raising the expectation for correct functionality and desired performance at cryogenic temperatures.

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A

Additional DAC structures

In the initial exploration of DAC architectures, not only the architectures in chapter 3 have been considered. The other considered architectures that have been considered are presented here for completeness and reasons why they have not been chosen are presented.

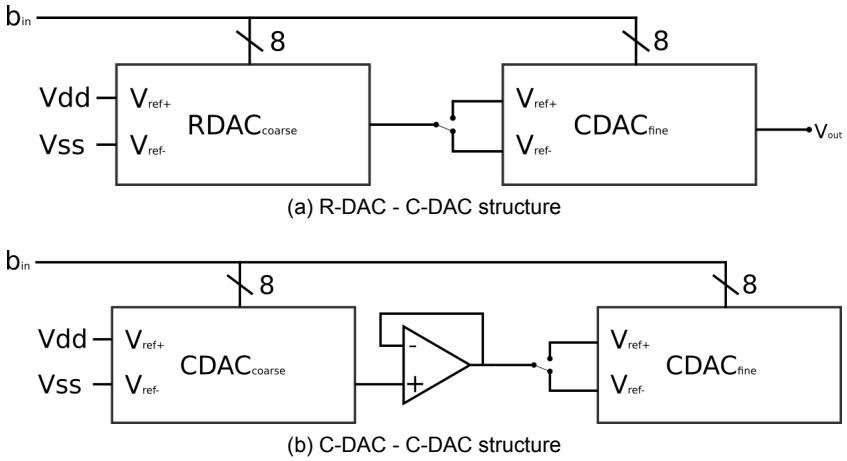
A.1. Multi-stage DAC

A limiting factor of single-stage C-DAC is the capacitance required. The needed capacitance scales with 2^N and therefore the area and power do too. While implementing a bridge capacitor improves this, it yields less optimal energy to noise performance. This section presents a different method of limiting the number of bits needed by a single stage by cascading DAC's.

A.1.1. Two-stage DAC

Reducing the number of bits could reduce the total capacitance could be done by using a two-stage DAC as shown in Figure A.1. There are multiple combinations of forming a two-stage DAC. Here focus will be on the R-DAC - C-DAC and C-DAC - C-DAC combination as these should result in low-power operation.

For the R-DAC, C-DAC structure, the resistive ladder sets the reference voltages of the C-DAC. If the R-DAC and C-DAC are connected through two multiplexers, the voltages V_{ref+} and V_{ref-} can be set simultaneously. In case only one voltage can be output from the R-DAC, the voltages V_{ref+} and V_{ref-} can be set consecutively. This is also how operation with a multi-stage C-DAC, C-DAC structure would work.



(a) R-DAC - C-DAC structure

(b) C-DAC - C-DAC structure

Figure A.1: Two Stage structures

Area

For an R-2R DAC stage, the area scales linearly with the number of bits. For a C-DAC stage, the area scales with 2^N. As the type of stages is not set, the upper bound can be approximated with $M2^N$ where M is the number of stages and N the number of bits of each stage.

Power

A R-DAC stage has a static dissipation, this is equal to $P_{static} = \frac{(V_{ref+} - V_{ref-})^2}{R_{in}}$ where R_{in} is the input resistance seen from the voltage sources. In order to have a good power dissipation, the resistances should be as large as possible in order to have a small power consumption.

The power dissipation of the C-DAC stage is similar to the single stage C-DAC mentioned previously. Splitting the stage in two parts however allows the C-DAC stage to have a significantly lower area, making the design similar to the single stage C-DAC with bridge.

Noise

For the R-DAC stage, the spectral noise power is equal to $V_n^2 = 4k_bTR_{out}BW$ where R_{out} is equal to R_u. For the C-DAC stage, the integrated noise is equal to $V_n^2 = \frac{k_bT}{C_{out}}$.

In case multiple C-DAC stages are cascaded, the noise powers are added of the different stages due to the signal with noise of the first stage is sampled by the second stage, which will add noise around this signal + noise. (The noise of the output will be correlated to the noise on C1). For a C-DAC - C-DAC combination, the noise would accumulate to: $V_n^2 = \frac{k_bT}{C_{out1}} + n_{buffer} + \frac{k_bT}{C_{out2}}$.

In case an R-DAC and a C-DAC stage are cascaded, The C-DAC will limit the bandwidth of the R-DAC, limiting the noise to the output stage which results in $v_n^2 = \frac{k_bT}{C_{out}}$.

Linearity

For monotonic behavior the criteria is needed for each individual stage to be monotonic. Each N-bit stage needs to be $\frac{\sigma_{\Delta Ci}}{C} = \frac{\sigma_C}{C}\sqrt{2^N - 1}$. In case multiple buffers which can have different offsets are used, monkey switching can be considered to nullify the impact of these different offsets.

Speed

Due to multiple stages being used, the speed scales linearly with with M, or the number of stages being used. Aside the speed is limited to the settling of the stages.

A.1.2. Cyclic C-DAC

A variety to the multi-stage DAC is a DAC which works in a cyclic manner as shown in Figure A.2. This cyclic C-DAC works similar to a two-stage C-DAC, however hold capacitors are present in order to hold the output voltages.

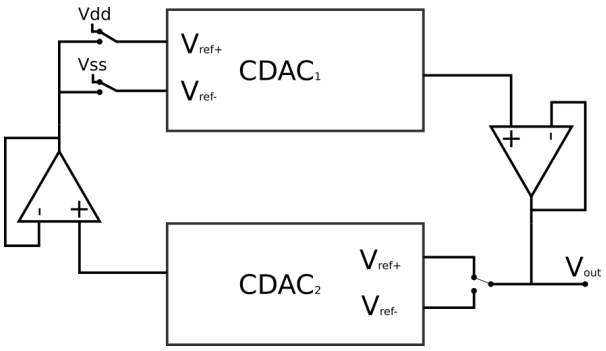


Figure A.2: Illustration of a Cyclic-DAC

Area
In terms of area, this architecture contains more components. The following elements are present:

- Hold Capacitors for the reference levels
- N-bit C-DAC arrays
- Buffer

These can however remain constant as finer resolutions can be generated by doing multiple passes. This allows for quite some flexibility in terms of design and operation.

Power
Splitting out the power used by different elements:

- Hold Capacitor for references: $E = C_{ref}V_{ref+}^2$
- C-DAC array : $E = M\frac{1}{6}C_{dac,in}V_{dd}^2$
- Buffer: $P = V_{dd}I_{buff}$

For operation, there need to be 4 hold capacitors present (2 for the 'old' references, 2 for the 'new' references). These can have a worst case energy consumption of needing to be charged to V_{dd}.

The energy used by the C-DAC is maximally $E = M\frac{1}{2}C_{dac}V_{ref+}^2$, as V_{ref+} of the first cycle gives the upper limit of the voltage. It is assumed that similar to the single stage C-DAC, the average energy for a code is needed Charge of the first cycle will ideally be held on the capacitor bank and after the first pass, most of the charge is in the capacitor bank. The energy which needs to be supplied will therefore be lower and is dominated by the first cycle.

The buffer stage uses static dissipation. Requirements for such a buffer are similar to the requirements shown later is this chapter for other architectures.

Noise
Splitting out the power used by different elements:

- Hold Capacitor for references: $V_n^2 = \frac{k_bT}{C_{ref}}$
- C-DAC array: $V_n^2 = \frac{k_bT}{C_{dac,out}}$
- Buffer: integrated noise of op-amp/buffer stage

Resulting in $v_n^2 = M(2\frac{k_bT}{C_{ref}} + \frac{k_bT}{C_{dac,out}} + n_{buffer})$ This indicates that the total noise power is significant and needs to be limited.

Linearity
Need to have an N-bit monotonic behavior within a single C-DAC stage, so $\frac{\sigma_{\Delta Ci}}{C} = \frac{\sigma_C}{C}\sqrt{2^N - 1}$.

Speed
Scales with the number of passes, each time two reference voltages needs to be set. Scales with 2M.

A.1.3. Conclusion
The multi-stage DACs presented in this section can be interesting alternative compared to existing architectures such as the regular C-DAC. However, this depends on the factor limiting performance of the DAC. In case noise is the limiting factor, only a multi-stage DAC consisting of a R and C stage is interesting.

Cascaded C-DAC stages generally require additional components such as buffers or hold capacitors to store voltages. In case multiple C-DACs are cascaded, the KT/C noise accumulates and the capacitors in the cascaded C-DACs have to be scaled larger compared to a single stage C-DAC in order to meet similar noise performance. This makes it not a favorable architecture in terms of noise, which is one of the primary focus in this thesis.

A.2. Algorithmic DAC

The DC-DAC is used to set DC voltages and there are is necessary speed constraints. Therefore architectures like an Algorithmic DAC can be interesting.

This architecture is based on a switched capacitor scheme making use of two capacitors. The structure for this is shown in Figure A.3, and the voltage generated is described by the recursive formula $V(i) = \frac{V(i-1)+b_{n+1-i}V_r}{2}$.

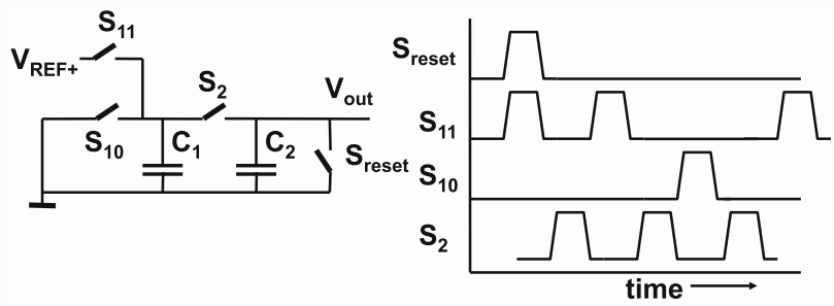


Figure A.3: Algorithmic C-DAC

A.2.1. Regular Switching

In literature, there exist multiple methods of switching the algorithmic DAC. In this section, first the regular switching will be considered.

Area

The area is not directly related to N, as only two capacitors and a switch are needed. The size of the capacitors has to be rather large due to noise, as will be shown later.

However, this architecture does not directly scale in size with the number of bits which need to be be made. Only when the noise performance needs to be improved, the capacitors need to become larger.

Power

The energy needed in order to execute the algorithmic conversion a single time is code dependent. There are two possible events, the capacitor is either charged or discharged:

- For a single charging event, the energy which needs to be input is equal to $E = \frac{1}{2}C[(V_{ref+}^2 - V_{c,old}^2]$
- for a discharging event, the energy dissipated is $E = \frac{1}{2}CV_{c,old}^2$

Where $V_{c,old}$ is the voltage on both capacitors after S2 being closed.

As the energy which needs to be added to the system depends on the code, there are certain codes which require less energy than others. This is primarily determined by the number of times energy needs to be input into the system. If the capacitor only needs to be charged once, then the energy input into the system is equal to $\frac{1}{2}CV_{ref+}^2$. Before the first charge, there is no energy in the system and therefore it is independent on when or where it is charged. The maximum energy needed has an upper bound of $\frac{N}{2}CV_{ref+}$, through simulation it is found that the average energy needed can be approximated by $E = \frac{N}{4}CV_{ref+}$.

Noise

The noise accumulation of the algorithmic switched capacitor circuit is not straightforward compared to the Multi-stage/Cyclic DAC or single stage C-DAC structures. At the start of the algorithm, the capacitors are both reset to 0 through a transistor, so noise is sampled on both capacitors after the reset phase. ϕ_1 is after the voltage has been set to either VDD or GND:

$$q_{n,C1}^{\Phi_1}{}^2 = (kTC_1 + kTC_2)(\frac{C_1}{C_1 + C_2})^2$$

$$q_{n,C2}^{\Phi_1}{}^2 = (kTC_1 + kTC_2)(\frac{C_2}{C_1 + C_2})^2$$

ϕ_2 is after the redistribution phase of the capacitors:

$$q_{n,C1}^{\Phi_2}{}^2 = (kTC_1 + kTC_2)(\frac{C_1}{C_1 + C_2})^2 + kT\frac{C_1C_2}{C_1 + C_2}$$

$$q_{n,C2}^{\Phi_2}{}^2 = (kTC_1 + kTC_2)(\frac{C_2}{C_1 + C_2})^2 + kT\frac{C_1C_2}{C_1 + C_2}$$

Here, the term $(\frac{C_x}{C_1+C_2})^2$ is because the noise power is multiplied by the power of the transfer function. Alternatively, one can reason that both capacitors have uncorrelated distributions, resulting in an averaging of the noise. ϕ_3 is after the redistribution switch is opened:

C1:

$$q_{n,C1}^{\Phi_3}{}^2 = (kTC_1 + kTC_2)(\frac{C_1}{C_1 + C_2})^2 + kT\frac{C_1C_2}{C_1 + C_2} \rightarrow q_n^2 = kT\frac{C_1(C_1 + C_2)}{(C_1 + C_2)^2} + kT\frac{C_1C_2}{C_1 + C_2} = kTC_1$$

C2:

$$q_{n,C2}^{\Phi_3}{}^2 = (kTC_1 + kTC_2)(\frac{C_2}{C_1 + C_2})^2 + kT\frac{C_1C_2}{C_1 + C_2} \rightarrow q_n^2 = kT\frac{C_2(C_1 + C_2)}{(C_1 + C_2)^2} + kT\frac{C_1C_2}{C_1 + C_2} = kTC_2$$

Which shows that when the redistribution switch is opened, the capacitors are in series as seen from the switch resulting in a charge noise of $kT\frac{C_1C_2}{C_1+C_2}$. Simplifying the equation results in the effective charge noise after the redistribution process being equal to the originally sampled noise.

Linearity

For monotonic behavior, again the transition between the MSB and MSB-1 bit should hold. As the two capacitors are repeatedly used to divide and average the voltages, the error caused by mismatch between the two capacitors can be described by $\epsilon = \frac{C_2-C_1}{C_2+C_1} < 2^{-N}$. The mismatch for a certain capacitor size $(\frac{\sigma_c}{C})$ should be below the 2^{-N} level in order to have monotonic behaviour[59, 60].

Speed

The speed of the algorithmic scales linearly with the number of bits, as every step a binary decision is made.

A.2.2. Compensative switching

With the observation that switching C1 and C2 results approximately in the reciprocal transfer, a compensative switching method has been presented in literature which allows for better linearity at the expense of some additional components and power. Operation of such a compensative switching method is shown in Figure A.4.

Area

In addition to the capacitors, this will require overhead of additional capacitors and an op-amp. Therefore the circuit approximately doubles in size compared to the regular switching methodology. This area does still remain constant with respect to the number of bits.

Power

The energy needed in order to execute the algorithmic conversion is twice that of the regular algorithm and thus a worst case approximation of the energy can be given with $E = NCV_{ref+}^2$. On average, the energy will be $E = \frac{N}{2}C_{in}V^2$, which ignores the op-amp power dissipation.

Noise

If it is assumed that the noise is primarily caused by the two switching capacitors and not the op-amp or hold capacitor„ one can consider that the noise is averaged once more compared to the regular algorithm, resulting in an improvement by 2. $(v_n^2 = \frac{1}{2}\frac{K_bT}{C})$

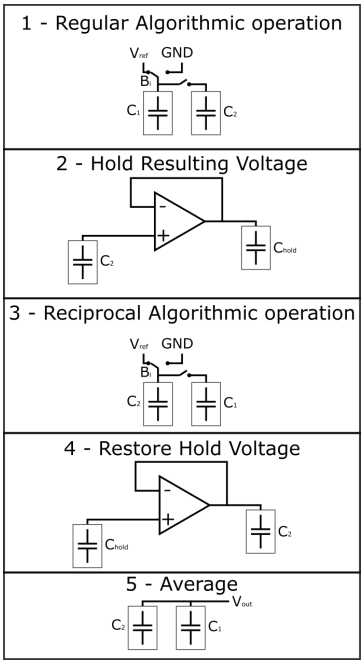


Figure A.4: Compensative switching example

Linearity

Due to the averaging of the two values, the error due to mismatch is reduced significantly. This results in $\frac{\sigma_{\Delta Ci}}{C} = \frac{3}{8}(\frac{\sigma_C}{C})^2 2^N$[60].

Speed

As the regular scheme needs to be repeated twice, this scheme scales linearly with 2N.

A.2.3. Conclusion

The algorithmic DAC is interesting in case the design is area and power limited. This kind of DAC does not yield any improvement in terms of noise compared to the single stage DAC. In case noise is limiting, the total capacitance of an algorithmic DAC needs to be equal to a single-stage DAC while there is more switching present, making it more power consuming. The improvement in power is typically achieved due to the smaller capacitances that can be used with this kind of DAC architecture.

Additionally, when considering compensative switching algorithms, the power consumption increases as additional components such as buffers and hold capacitors are again required. The designed DC-DAC needs a high resolution, making it unfavorable to use the algorithmic DAC as compensative switching structures would be needed and therefore additional power will be consumed.

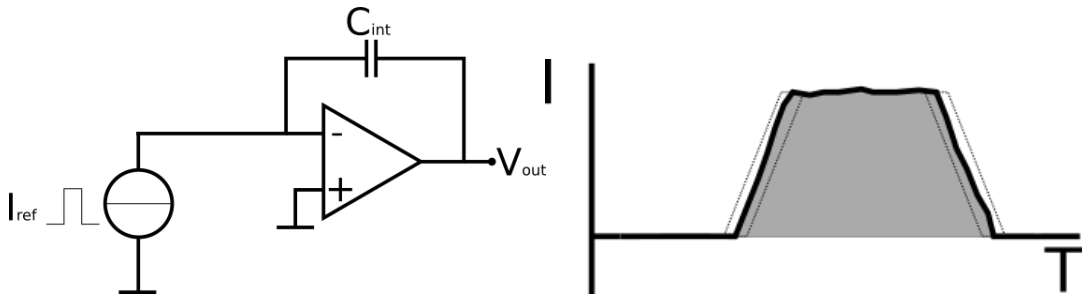
A.3. Slope I-DAC

The switched capacitor integrator in **??** performs integration in the charge domain. It is also possible to perform such operation in the current domain, where a DC current source is used together with accurate timing to create the ramp. Integrating a current is often used in dual-slope ADC's[40]. The core structure of this DAC is shown in Figure A.5. Here is is assumed that current pulses are used to create discrete integration steps, however it is also possible to create the slope through a continuously integrating current.

Operation using a voltage source is also possible, however that would require a voltage in combination with the resistor to generate the integrating current.

Area

The area is determined by the Op-Amp, current generation circuitry and integrating capacitor as shown in figure 3.4. The integrating capacitor will be sized for noise, whereas the current generation circuitry is designed to accommodate a LSB step.



(a) Schematic (b) Noise overview

Figure A.5: Discrete Slope I-DAC

Power

For a single ramp, the integrating capacitor needs to charged once to $E = \frac{1}{2}C_{int}V_{dd}^2$. Additionally, there is the requirement of the op-amp and accurate clock which adds power. The op-amp will be considered seperately, however for the accurate clock, a period of T_{lsb} such that $V_{lsb} = T_{lsb}I$ needs to be present. Using a low current allows the use of a less-accurate clock and slower clock. Generally, the desired clock speed is approximately in the range of a few hunderd kHz till a few MHz.

Noise

Similarly to the SC-integrator, noise that is accumulated in operation can be split in several parts:

- On reset, the integrating capacitor will be shorted to ground through a switch, resulting in $Q_{ncint}^2 = kTC_{int}$ or $V_{ncint}^2 = \frac{kT}{C_{int}}$
- When the current is starting, there is an uncertainty in time of the exact starting and ending moment which translates to a power spectral density of $\sigma_v^2 = 2\sigma_t^2\frac{dV}{dT}^2$. Here σ_t is the rms jitter of the signal and $\frac{dV}{dT}$ is given by the integrating capacitor ($\frac{dV}{dT} = \frac{I}{C_{int}}$). This noise is sampled 2^N times, and therefore has an additive effect.
- There is also cyclo-stationary noise from the current source. This comes from the current source (transistor, which contains thermal noise) and can be described by: $\overline{I_{c,out}^2} = 4kT\gamma_p G_m$ This noise is input referred to the operational amplifier. Therefore it is translated through the amplifier by its transfer function. This results in a noise of $\overline{I_{c,out}^2}BW$ where the bandwidth is defined as: $BW = \frac{gm}{2\pi A_{req}C_l}$. Combined with the transfer function from current to voltage this becomes:

  $$\overline{V_{cp,out}^2} = 4kT\gamma_p G_{mp}\frac{gm}{2\pi A_{req}C_l}$$

  .

  This results in total this results in a PSD which is band-limited by a low-pass filter

  $$\overline{v_n^2} = (2\sigma_t^2\frac{dV}{dT}^2 + \frac{4KT}{g_m}(\frac{g_m}{2\pi A_{req}C_l}))$$

- Finally, there is the amplifier noise which can be described by $V_{n,out}^2 = \frac{kTA_{req}}{C_l}$

Combined, this results in the approximation of the noise as in Equation A.1 which illustrate the components adding noise in the DAC. Note that A_{req} drops out as it is ≈1.

$$v_n^2 = 2^N 2\sigma_t^2\frac{dV}{dT}^2 + \frac{4}{2\pi}\frac{KT}{C_l} + \frac{KT}{C_l} + \frac{kT}{C_{int}} \tag{A.1}$$

Similarly to the SC-integrator, the noise of the op-amp is present at the output voltage, this is determined by the amplifier noise and the bandwidth which is set by the loading capacitance. In case this architecture is used, noise power should be budgeted among the two components.

Linearity

As increments of an LSB step are taken, this is monotonous as long as the noise is lower than the LSB step size.

Speed

This DAC could operate in two modes, one where it increments in single steps. The other where the timer is running upto the desired level to immediately generate the output voltage value. These two operating modes can be considered with implementation.

A.3.1. Conclusion

The continuous time slope I-DAC can be an interesting DAC and there is flexibility in terms of operations. Compared to the SC-integrator, there is a primary difference in how the noise is accumulated. Additionally, a slope I-DAC would require an accurate clock in order to keep track of the integration steps and achieving a low jitter. This also requires power and therefore it is less favorable to the SC-integrator.

In case the slope I-DAC is implemented with a continuous current, it requires accurate timing and can cause tighter constraints to be placed on the multiplexer in order to allow for accurate biasing.

B

Appendix: Offset-compensated Switched-Capacitor Integrator Derivations

This appendix contains derivations for the equations presented in chapter 4 with intermediate steps and images. The notation is brief and to the point in order to keep the derivations concise.

B.1. Output voltage

First, a figure of how voltages develop during different phases is presented Then, expressions for the voltages are given for phase 1 and phase 2 respectively.

B.1.1. Waveform

An illustration of the waveforms is shown in Figure B.1. The LSB step (V_{lsb}) is considered the step between two consecutive Φ_2 phases. Additional argumentation for the waveforms can be found in the following subsection

B.1.2. Operation

The offset compensated circuit is analyzed for positive integration. The expression derived here consider the operation together with the impact of limited gain A. The subscript n V_n is used to denote the voltage in the n'th cycle and V_{n-1} the voltage in the cycle before the n'th cycle. Additionally, superscript is denoted to distinguish between the final values of the different phases.

Phase 1

The circuit during Φ_1 is illustrated in Figure B.2.

V_{in} is sampled on C_{add} by a voltage reference

$$V_{Cadd} = V_{in} - V_{cm}$$

V_2 is equal to the virtual ground node V_- and $V_+ = V_{cm} + V_{os}$, the op-amp gives:

$$V_{out} = A(V_{cm} + V_{os} - V_2)$$

Additionally: $V_{out} = V_2 + V_{Cint,n-1}^{\Phi_2}$

$$V_2 + V_{Cint,n-1}^{\Phi_2} = A(V_{cm} + V_{os} - V_2)$$

$$V_2(1 + \frac{1}{A}) = V_{cm} + V_{os} - \frac{V_{Cint,n-1}^{\Phi_2}}{A}$$

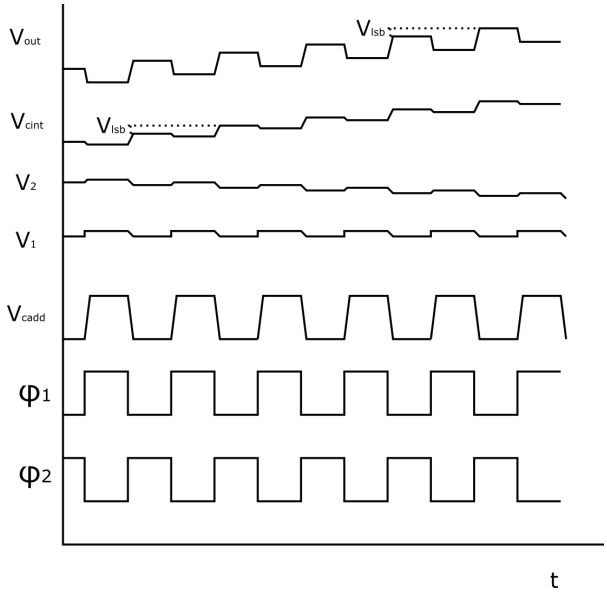


Figure B.1: Illustration of the development of waveforms over time

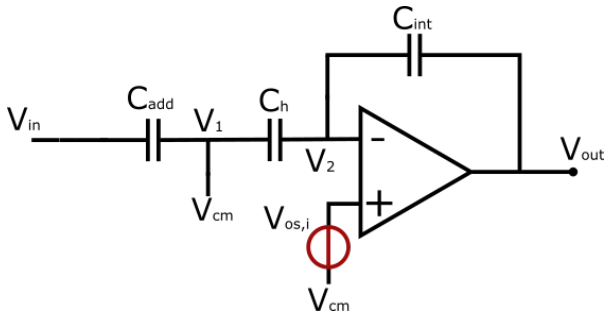


Figure B.2: Offset compensated SC-Integrator - Phase 1

$$V_2 = \frac{V_{cm} + V_{os} - \frac{V_{Cint,n-1}^{\Phi_2}}{A}}{1 + \frac{1}{A}}$$

C_h samples the voltage $V_2 - V_1$:

$$V_{ch,n} = \frac{V_{cm} + V_{os} - \frac{V_{Cint,n-1}^{\Phi_2}}{A}}{1 + \frac{1}{A}} - V_{cm}$$

So for Φ_1 the voltages can initially be described with:

$$V_{2,n} = \frac{V_{cm} + V_{os} - \frac{V_{Cint,n-1}^{\Phi_2}}{A}}{1 + \frac{1}{A}}$$

$$V_{out} = \frac{V_{cm} + V_{os} - \frac{V_{Cint,n-1}^{\Phi_2}}{A}}{1 + \frac{1}{A}} + V_{Cint,n-1}^{\Phi_2}$$

In order to change the voltage V_{ch}, a current should flow from the amplifier through C_{int}. Therefore there will be a decrease in voltage over C_{int}. The bias voltage V_{cm} can be assumed constant. In the presented analysis, it is assumed that the offset and bias voltage are constant $V_{os,n} = V_{os,n-1}$, $V_{cm,n} = V_{cm,n-1}$. V_{lsb} is the voltage increase on V_{Cint} of a full period and the voltage change on node V_- due to the charge transfer is the same for different periods[1].

$$\Delta Q_{Ch} = (V_{Ch,n} - V_{Ch,n-1}) \cdot C_h$$

$$\Delta Q_{Ch} = \left(\frac{V_{os,n} - \frac{1}{A}(V_{Cint,n}^{\Phi_2} + V_{b,n})}{1 + \frac{1}{A}} - \frac{V_{os,n-1} - \frac{1}{A}(V_{Cint,n-1}^{\Phi_2} + V_{b,n-1})}{1 + \frac{1}{A}}\right) \cdot C_h$$

$$\Delta Q_{Ch} = \left(\frac{\frac{V_{Cint,n-1}^{\Phi_2}}{A} - \frac{V_{Cint,n}^{\Phi_2}}{A}}{1 + \frac{1}{A}}\right) \cdot C_h$$

$$\Delta Q_{Ch} = \frac{-V_{lsb}}{A+1} \cdot C_h$$

$$\Delta V_{Cint} = \frac{\Delta Q}{C_{int}}$$

$$\Delta V_{Cint} = \frac{\frac{-V_{lsb}}{A+1} \cdot C_h}{C_{int}}$$

This leads us to conclude that during Φ_1, when the output is in the 'hold' mode, there is a small voltage drop on V_{Cint} due to the current required to add charge to C_h. This drop can be suppressed with a large enough gain.

This leads for the following conditions for the steady state of the phase:

$$V_{Cint,n}^{\Phi_1} = V_{Cint,n-1}^{\Phi_2} - \frac{\frac{V_{lsb}}{A+1} \cdot C_h}{C_{int}}$$

$$V_2 = \frac{V_{cm} + V_{os} - \frac{V_{Cint,n}^{\Phi_1}}{A}}{1 + \frac{1}{A}}$$

$$V_{ch} = V_2 - V_1$$

$$V_{out,n}^{\Phi_1} = V_2 + V_{Cint,n}^{\Phi_1}$$

[1] Which is valid as long as V_{lsb} is constant

Phase 2

The circuit during Φ_2 is illustrated in Figure B.2.

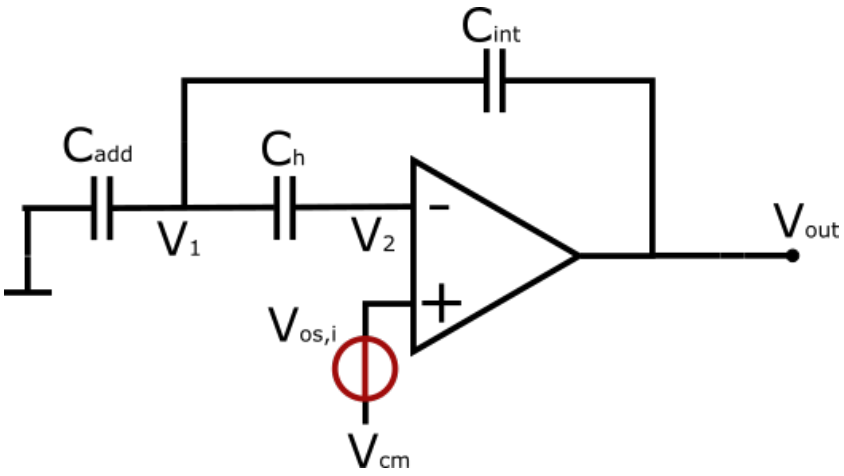


Figure B.3: Offset compensated SC-Integrator

From the previous phase:

$$V_{ch} = \frac{V_{cm} + V_{os} - \frac{V_{Cint,n}^{\Phi_1}}{A}}{1 + \frac{1}{A}} - V_{cm}$$

$$V_2 = \frac{V_{cm} + V_{os} - \frac{V_{Cint,n}^{\Phi_1}}{A}}{1 + \frac{1}{A}}$$

This gives initially for V_1:

$$V_1 = V_2 - V_{ch}$$

$$V_1 = V_{cm}$$

The output voltage is given by:

$$V_{out} = V_1 + V_{Cint,n}^{\Phi_1}$$

So initially:

$$V_2 = \frac{V_{cm} + V_{os} - \frac{V_{Cint,n}^{\Phi_1}}{A}}{1 + \frac{1}{A}}$$

$$V_1 = V_{cm}$$

$$V_{out} = V_1 + V_{Cint,n}^{\Phi_1}$$

The charged capacitor C_{add} was initially charged to

$$V_{Cadd} = V_{in} - V_{cm}$$

and gets discharged to

$$V_{Cadd} = 0 - V_1$$

A current through C_{add} causes the discharge, causing a change of V_{Cint}.

As the output voltage changes, a change at $V_-(V_2)$ also occurs due to finite gain. Assuming no current runs through C_h, this change in V_- also occurs at V_1. Additionally, assuming that no change in V_+ takes place this results in:

$$\Delta V_{out} = -A\Delta V_-$$

Where eventually, once the charge has transferred:

$$V_1 = V_{cm} + \Delta V_-; \text{ w.r.t. the beginning of the phase} \Delta V_1 = \Delta V_-$$

The current will transfer a total charge of:

$$\Delta Q = (V_{in} - V_{cm}) - (0 - V_1) \cdot C_{add} = (V_{in} + \Delta V_{-}) \cdot C_{add}$$

Which translates to a difference in charge and thus voltage on C_{int}:

$$\Delta V_{Cint} = \frac{\Delta Q}{C_{int}}$$

$$\Delta V_{Cint} = (V_{in} + \Delta V_{-}) \frac{C_{add}}{C_{int}}$$

$$\Delta V_{Cint} = (V_{in} - \frac{\Delta V_{out}}{A}) \frac{C_{add}}{C_{int}}$$

$$\Delta V_{Cint} + \frac{\Delta V_{out}}{A} \frac{C_{add}}{C_{int}} = V_{in} \frac{C_{add}}{C_{int}}$$

note that: $\Delta V_{out} = \Delta V_1 + \Delta V_{Cint} = \Delta V_{-} + \Delta V_{Cint}$

or: $\Delta V_{out}(1 + \frac{1}{A}) = \Delta V_{Cint}$

rewrites to: $\Delta V_{out} = \Delta V_{Cint} \frac{A}{A+1}$

$$\Delta V_{Cint} + \Delta V_{Cint} \frac{A}{A+1} \frac{1}{A} \frac{C_{add}}{C_{int}} = V_{in} \frac{C_{add}}{C_{int}}$$

$$\Delta V_{Cint}(1 + \frac{1}{A+1} \frac{C_{add}}{C_{int}}) = V_{in} \frac{C_{add}}{C_{int}}$$

$$\Delta V_{Cint}(\frac{AC_{int} + C_{int} + C_{add}}{AC_{int} + C_{int}}) = V_{in} \frac{C_{add}}{C_{int}}$$

$$\Delta V_{Cint} = V_{in} \frac{C_{add}}{C_{int}} \frac{AC_{int} + C_{int}}{AC_{int} + C_{int} + C_{add}}$$

$$\Delta V_{Cint} = V_{in} \frac{C_{add}(A+1)}{C_{int}(A+1) + C_{add}}$$

$$\Delta V_{Cint} = V_{in} \frac{C_{add}}{C_{int} + \frac{C_{add}}{(A+1)}} \tag{B.1}$$

Finally, at the output a change is observed of:

$$\Delta V_{out} = V_{in} \frac{C_{add}}{C_{int} + \frac{C_{add}}{(A+1)}} \frac{A}{A+1}$$

$$\Delta V_{out} = V_{in} \frac{C_{add}}{C_{int} + \frac{C_{int} + C_{add}}{A}} \tag{B.2}$$

Combined expressions

V_{lsb} is the accumulated change observed at V_{out} of phase one and two combined.

$$V_{lsb} = V_{in}\frac{C_{add}}{C_{int} + \frac{C_{add}}{(A+1)}} - \frac{\frac{V_{lsb}}{A+1}\cdot C_h}{C_{int}}$$

$$V_{lsb}(1 + \frac{\frac{1}{A+1}\cdot C_h}{C_{int}}) = V_{in}\frac{C_{add}}{C_{int} + \frac{C_{add}}{(A+1)}}$$

$$V_{lsb} = V_{in}\frac{(A+1)C_{int}\cdot C_{add}}{(A+1)C_{int}^2 + C_{int}\cdot C_{add} + C_h\cdot C_{int} + \frac{C_h\cdot C_{add}}{(A+1)}}$$

$$V_{lsb} = V_{in}\frac{C_{add}}{C_{int} + \frac{C_{add}}{(A+1)} + \frac{C_h}{(A+1)} + \frac{C_h\cdot C_{add}}{C_{int}\cdot(A+1)^2}} \tag{B.3}$$

$$V_{Cint,n} = n\cdot V_{lsb}$$

Both B.1 and B.2 show dependence on the gain of the amplifier, when it is infinite it results in an 'ideal' integration. If an ideal amplifier is assumed, it can be observed that the expression in Equation B.3 translates to Equation 4.5.

The presented analysis results in the final steady states:

$$V_1^{\Phi_2} = V_{cm} - V_{in}\frac{C_{add}}{AC_{int} + C_{int} + C_{add}}$$

$$V_1^{\Phi_2} = V_{cm} - V_{in}\frac{1}{1 + \frac{C_{int}}{C_{add}}(A+1)}$$

$$V_{Cint,n}^{\Phi_2} = n\cdot V_{lsb}$$

$$V_{out} = V_1^{\Phi_2} + nV_{lsb}$$

The outputs during the two phases can thus be described as:

$$V_{out,n}^{\Phi_1} = \frac{V_{cm} + V_{os} - \frac{(n-1)V_{lsb}}{A}}{1 + \frac{1}{A}} + (n-1)V_{lsb} - \frac{\frac{V_{lsb}}{A+1}\cdot C_h}{C_{int}}$$

$$V_{out,n}^{\Phi_2} = V_{cm} - V_{in}\frac{1}{1 + \frac{C_{int}}{C_{add}}(A+1)} + nV_{lsb}$$

These descriptions have a part which describes voltage V_1 and V_2 and a part which describes the development of the voltage over V_{Cint} (which uses V_{lsb}). This representation helps to explain the switching effect which can be observed, as the output is dependent on the bias voltage and the gain, which causes small jumps in the voltage to be observed when the feedback loop is switched.

B.2. Noise

This section contains a workout of the accumulated architecture noise where the noise of the op-amp is included. This derivation results in Equation 4.11. On the initial reset, the noise of the architecture depends on the kt/c noise of the individual components. In favor of complexity, all switches are opened simultaneously and no parasitic capacitance is assumed present.

Reset

During the reset, it is assumed that all capacitors can be reset to their initial conditions causing the following charge noise:

$$Q_{Cadd}^{rst\ 2} = kTC_{add}$$

$$Q_{Cint}^{rst\ 2} = kTC_{int}$$

$$Q_{Ch}^{rst\ 2} = kTC_{h}$$

Phase 1

During Φ_1, the circuit can be divided in two parts as shown in Figure B.4.

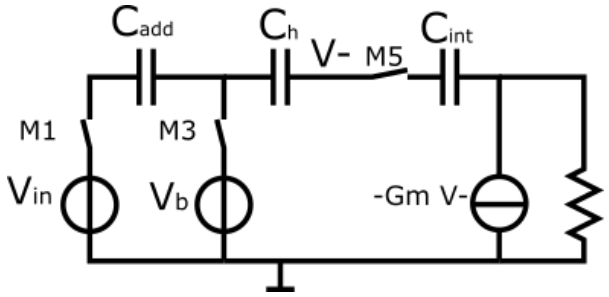


Figure B.4: Simplified schematic of Phase 1 for the noise derivation.

From this, it is clear that:

$$q_{Cadd}^{\Phi_1\ 2} = kTC_{add}$$

The virtual ground node V_- introduces the op-amp noise $v_{n,op}^2$. The op-amp noise is assumed to have only thermal noise. The following expressions can be used to characterize the noise spectrum, bandwidth and integrated noise power:

$$S_{op} = \alpha 4kT\frac{1}{g_{m1}}$$

$$BW = \frac{g_{m1}}{4C_o}$$

$$v_{n,op}^2 = \alpha\frac{kT}{C_o}$$

Where C_o is the noise limiting capacitor of the operational amplifier and α the noise excess factor.

It can be noted that as both C_h and C_{int} are in series, they suffer from the same charge noise. In addition to the noise of the op-amp, the switches introduce thermal noise:

$$S_{ron}^2 = 4kTR_{on}$$

$$v_{sw}^2 = 4kTR_{on}\frac{\pi}{2}BW$$

The bandwidth BW is dominated by either the op-amp or switches. In favor of power consumption, it is assumed that the op-amp limits the bandwidth [51]. Therefore $BW = \frac{1}{4}\frac{g_{m1}}{C_o}$. This results in the approximate expression for the noise voltage at V_{out}:

$$V_{n,out}^{\Phi_1\ 2} = 4kTBWr_{s,3}(\frac{C_h + C_{int}}{C_{int}})^2 + 4kTBWr_{s,5} + \alpha(\frac{C_h + C_{int}}{C_{int}})^2\frac{4kTBW}{g_{m1}}$$

Which approximates to the next expression under the assumption that $\frac{1}{g_{m1}} >> r_s$

$$V_{n,out}^{\Phi_1}{}^2 = \alpha(\frac{C_h + C_{int}}{C_{int}})^2 \frac{kT}{C_o}$$

$$v_{n,Ch}^{\Phi_1}{}^2 = \alpha \frac{kT}{C_o}$$

Resulting in the following charge noise on C_h and C_{int}:

$$q_{n,Ch}^{\Phi_1}{}^2 = q_{n,Cint}^2 = \alpha kT \frac{C_h^2}{C_o}$$

Phase 2

For the second phase, the configuration in Figure B.5 can be assumed.

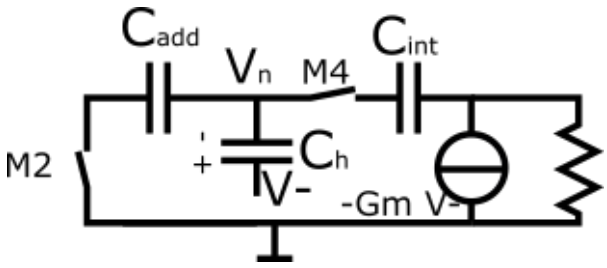


Figure B.5: Simplified schematic of Phase 2 for the noise derivation.

First, it can be observed that the noise charge from $q_{Cadd}^{\Phi_1}{}^2$ is integrated onto C_{int}.

There is a similar situation as in phase 1, C_{add} and C_{int} are in series. As C_h sampled the noise source, only the high-pass component of the noise will appear at the output and 1/f noise of the amplifier will be reduced. As V_{Ch} is sampled in the time domain, it will result in a function of the noise spectrum multiplied by sinc. As the bandwidth is rather high, aliasing components will still contribute significant noise (BW of the sinc function is approx 10 times lower than the BW of the OTA). Which leads to not full cancellation of the thermal and 1/f noise, high frequency noise will still be visible at the output. For ease of computation, it is assumed that the noise observed at C_{add} is the op-amp noise:

$$v_{n,cadd}^{\phi_2}{}^2 = \alpha \frac{kT}{C_o}$$

Taking the assumption that the charge noise on C_{add} is also present on C_{int} results in:

$$q_{n,Cadd}^{\Phi_2}{}^2 = q_{n,Cint}^{\Phi_2}{}^2 = \alpha kT \frac{C_{add}^2}{C_o}$$

This charge noise is also present on C_{int}

Repetition

This cycle is repeated $n = 2^N$ times. This accumulates charge noise on C_{int} which is visible at the output. The charge noise can be translated to a voltage by multiplying with $(\frac{1}{C_{int}})^2$. The accumulated voltage noise on C_{int} at the end of 2^N cycles is given by Equation B.4.

$$v_{Cint}{}^2 = \frac{kT}{C_{int}} + \frac{nkT}{C_{int}^2}(C_{add} + \frac{\alpha}{C_o}(C_{add}^2 + C_h^2)) \tag{B.4}$$

Conclusion

During Φ_1, the bandwidth of noise on C_{add} is determined by R_{on} of the switches, causing aliasing of the full bandwidth to alias and resulting in a noise charge of KTC_{add}.

Simultaneously during this phase, the noise spectrum on C_h and C_{int} is set by the operational amplifier, which has a bandwidth significantly lower than the bandwidth caused by the capacitors and switches. Similarly, the amplitude of the noise spectrum of the op-amp is larger (as $\frac{1}{gm_1} >> R_{on}$). This leads to the operational amplifier dominating the noise and causing an integrated noise voltage equal to $v_{n,op}$ of capacitor C_h. This is equivalent to a noise charge of $C_h^2 v_{n,op}$ which is also present (and therefore added) on C_{int}.

During the second phase Φ_2, the aliased charge noise of C_{add} is integrated to C_{int} and similarly to previous phase, the operational amplifier dominates the bandwidth and noise spectrum, leading to an added charge noise of $C_h^2 v_{n,op}$ on C_{add} which is also present on C_{int}.

Which is then repeated $n = 2^N$ times during operation.

C

Appendix: Layout images

This appendix contains additional layout images to illustrate how the chip has been fully implemented. The first section contains additional layout images of the IO ring of DC-DAC V1. The second section contains detailed layout images of the altered DAC core and additional remarks about the changes to the IO ring.

C.1. DC-DAC V1

The layout of version 1 of the DC-DAC has been elaborately covered in chapter 5. This section contains supplementary layout images.

C.1.1. IO Ring

The IO ring including the port names are illustrated in Figure C.1. It can be observed that there are added pads for test structures, these are present for quick characterization of devices at cryogenic temperatures.

C.2. DC-DAC V2

The second version of the DC-DAC is largely similar to the first version. The changes are listed in section 5.9. in the following subsection, the changed coarse DAC, circuit core and IO ring are illustrated.

C.2.1. Coarse DAC

The updated coarse DAC is illustrated in Figure C.2. Compared to Figure 5.13, there is no resistor ladder present and only one digital level shifter needs to be present. This version of the Coarse DAC therefore has a significantly reduced area.

C.2.2. Full Circuit

With the updated Coarse DAC, the full circuits is as illustrated in Figure C.3.

C.2.3. IO Ring

As the coarse DAC is connected to pads, the IO ring has to be changed. Table C.1 shows the signals connected to pads, compared to Table 5.1, the signals $V_{dac,l}$, $V_{dac,h}$ have been added. The IO ring has been changed accordingly to allow for $V_{dac,l}$, $V_{dac,h}$ to be in the 3.6V domain. The altered IO ring is illustrated in Figure C.4.

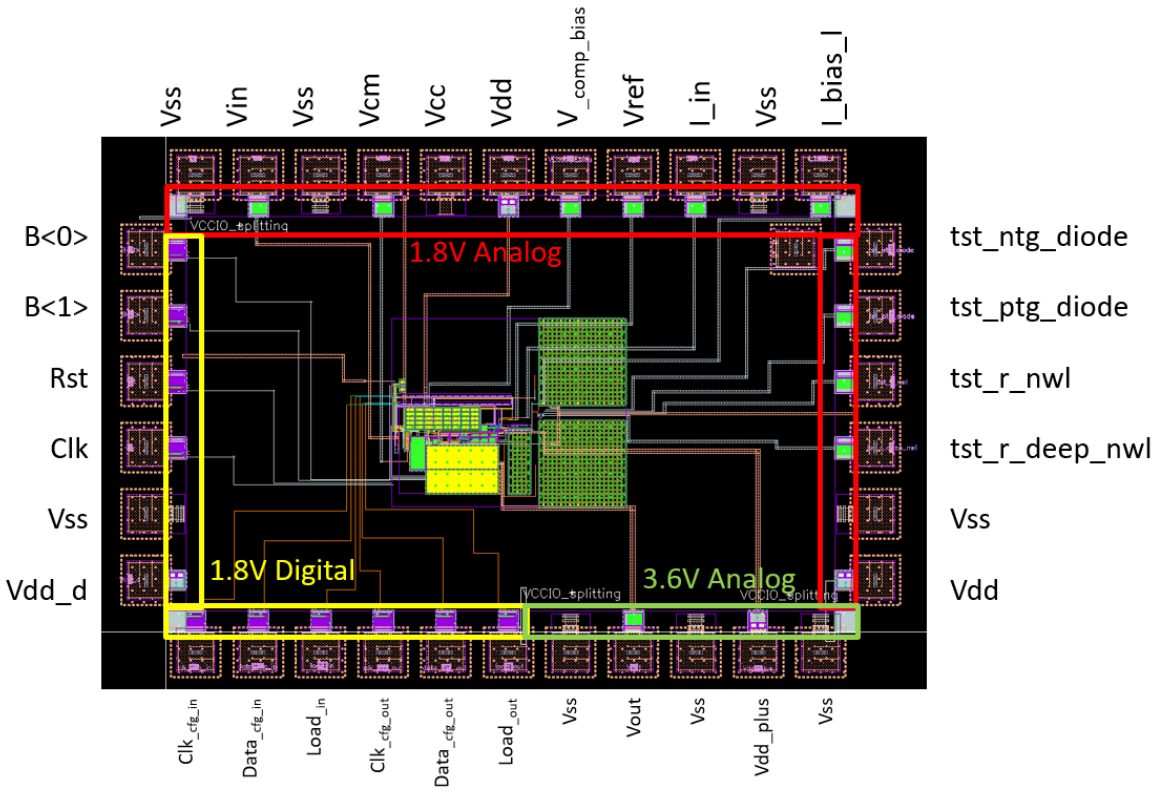


Figure C.1: IO Ring of the DC-DAC V1

Table C.1: Signals that are connected to pads in the DC-DAC V2.

Signal	In/Out	Signal Type	Voltage domain
V_{in}, V_{cm}, V_{ref}, V_{comp}, I_{in}, VDD, VSS	In	Analog	1.8V
$B_{0,1}$, Clk, Rst, Clk_cfg_in, Data_cfg_in, Ld_cfg_in	In	Digital	1.8V
Clk_cfg_out, Data_cfg_out, Ld_cfg_out	Out	Digital	1.8V
$I_{bias,out}$	Out	Analog	1.8V
$V_{dac,l}$, $V_{dac,h}$	In	Analog	3.6V
V_{out}, VDD_{plus}	Out	Analog	3.6V

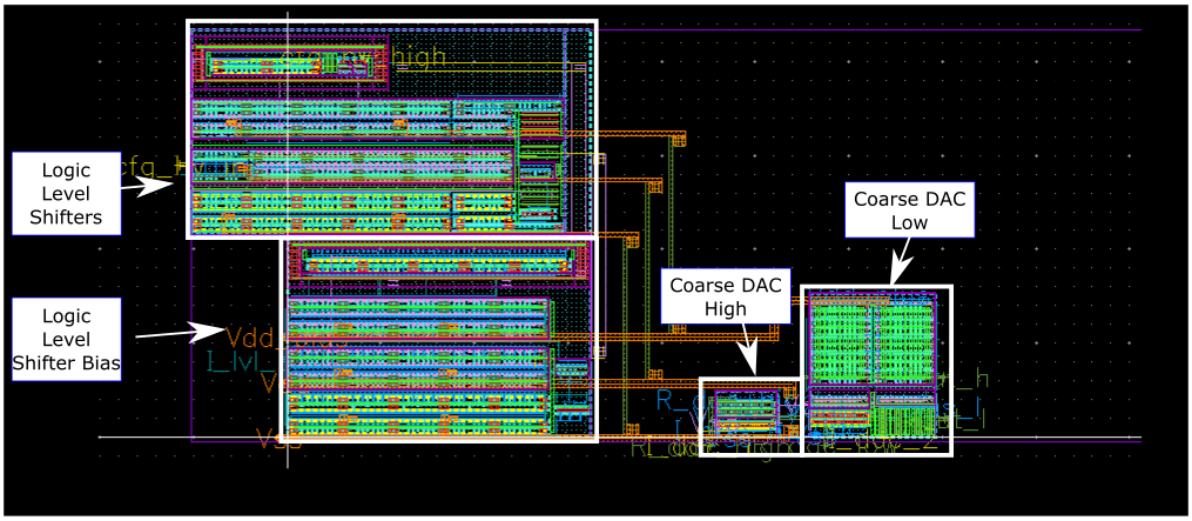


Figure C.2: Coarse DAC for the DC-DAC V2.

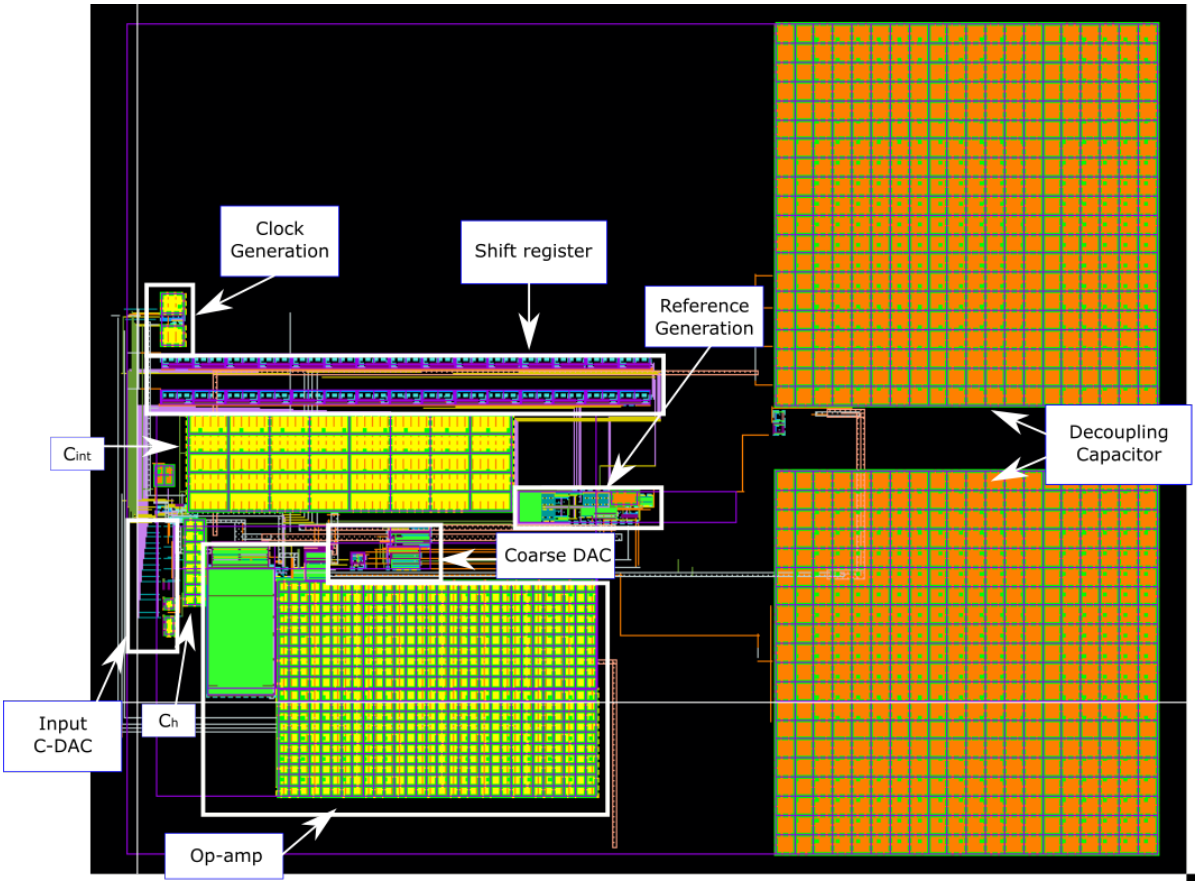


Figure C.3: Full Circuit of the DC-DAC V2.

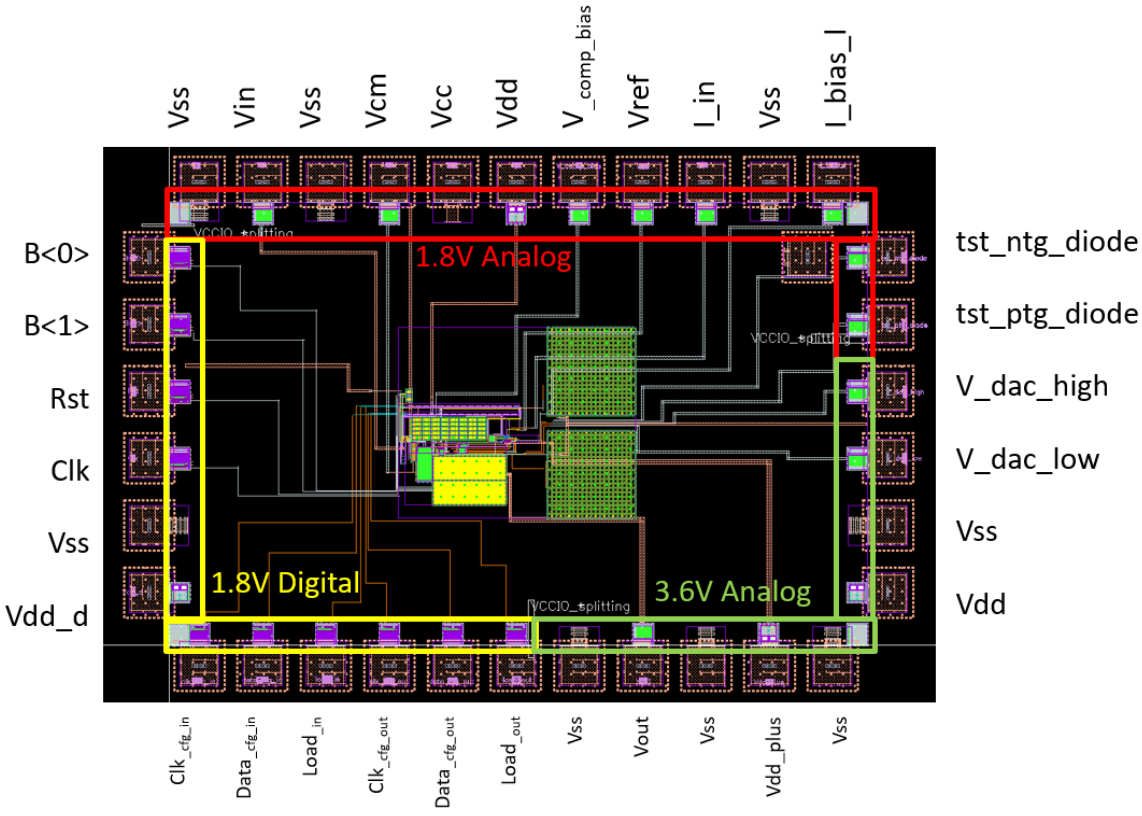


Figure C.4: IO Ring of the DC DAC V2.

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