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Highly Efficient and Linear Class-E CMOS Digital Power Amplifier Using a Compensated Marchand Balun and Circuit-Level Linearization Achieving 67% Peak DE and -40dBc ACLR without DPD

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***Abstract*— A highly efficient and linear wideband digital polar CMOS class-E power amplifier (DPA) is presented. Using a compensated wideband Marchand balun with re-entrant coupled lines for the output matching network, more than 50% peak drain efficiency over 2.2-3GHz with 16-17dBm P_{OUT} are achieved. The linearity is significantly improved by nonlinearly sizing the DPA array along with overdrive-voltage control and concurrent multiphase RF clocking. The chip prototype is fabricated in 40nm bulk CMOS and the balun is fabricated on a two-layer PCB. Measured results show -40dBc for a 40MHz QAM signal at 2.6GHz without using any sort of DPD. The measured peak P_{OUT}, DE and PAE at 2.6GHz are 17.2dBm, 67% and 45% with VDD=0.7V.**

***Index Terms*— Class-E, CMOS, digital PA, DPD-less, efficient, linear, wideband.**

I. Introduction

Linearity and efficiency are key parameters in a transmitter (TX) which are mostly influenced by the power amplifier (PA). In a digital polar TX, the digital PA (DPA) is typically implemented as an array of sub-PAs, in which the output amplitude is digitally controlled by the number of sub-PAs that are switched on. To achieve high efficiency at full power, the DPA is normally designed in switched-mode classes (E, D or D^{-1}) but it typically suffers from high nonlinearity in its AM-code-word (ACW)-to-AM and ACW-PM conversions [1]-[2] which are conventionally corrected by DPD [1]-[3] leading to extra bandwidth expansion, more complicated baseband signal processing and higher power consumption. In order to avoid DPD, in [3] ACW-PM is corrected by dynamically biasing varactors to adjust the input RF delay, yet requiring DPD for correcting ACW-AM. In [4], the bias point of a class-B PA array is adaptively tuned by a feedback from an analog AM-replica. While as mentioned a class-E DPA is highly nonlinear, in [5] we demonstrated the first linear class-E DPA in which the ACW-AM and ACW-PM distortions are corrected by using nonlinear sizing along with overdrive-voltage control and multiphase RF clocking without using DPD. Typically, a DPA implemented with on-chip matching network, cannot achieve DE higher than 50% [1]-[5], while with an off-chip matching network higher efficiencies are feasible [6].

In this paper, a highly DPD-less linear, wideband, efficient differential polar class-E DPA is presented. In order to achieve DE higher than 50% over a wide RF bandwidth, a novel wideband compensated Marchand balun using re-entrant coupled lines is designed. By using novel circuit level linearization techniques, high efficiency and high linearity are achieved without compromising one for the other.

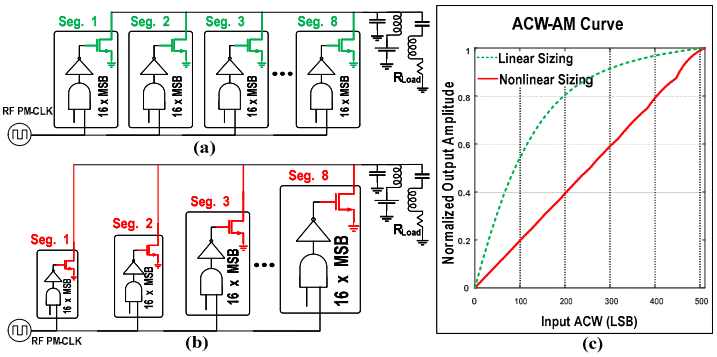

Fig. 1. Simplified single-ended digital class-E PA. (a) Convectional DPA with linear sizing and 8 uniform segments. (b) Nonlinearly sized array using 8 different segments. (c) Simulated ACW-AM curves of (a) and (b).

II. Design of a Linear Efficient Class-E DPA

A. Linearizing ACW-AM

In the switch-mode classes of digital PA (E, D or D^{-1}), the DPA array acts as a segmented switch in which the AM modulation is performed by modulating the effective on-resistance of the active switches. In a conventional DPA design with linear sizing of the switching elements, the total size of the on-switches is a linear function of the input ACW. A typical configuration of such a design as a 9-bit single-ended class-E DPA with 8 similar segments (rows) is depicted in Fig 1.a (2 LSB bits are not shown). These segments are switched on in a thermometer code fashion. However, linear sizing results in a highly nonlinear ACW-AM curve that without DPD it cannot be used for any communication standard with AM modulation. In this work, the 8 segments of the DPA array shown in Fig 1.b are nonlinearly sized with 8 different segments sizes so that the total size of switched-on devices is a nonlinear increasing function of the input ACW [5]. Each segment consists of 16 MSB (4b) unit-cell and 3 smaller LSB cells (2b). In Fig 1.c. the ACW-AM curve of the conventional linear sizing and the nonlinear sizing technique are plotted. Since the on-resistance (R_{ON}) is also a function of the overdrive voltage, to compensate for the changes in R_{ON} and R_{Load} caused by PVT or frequency shifts, the voltage of the RF clock applied to the gate of the sw-

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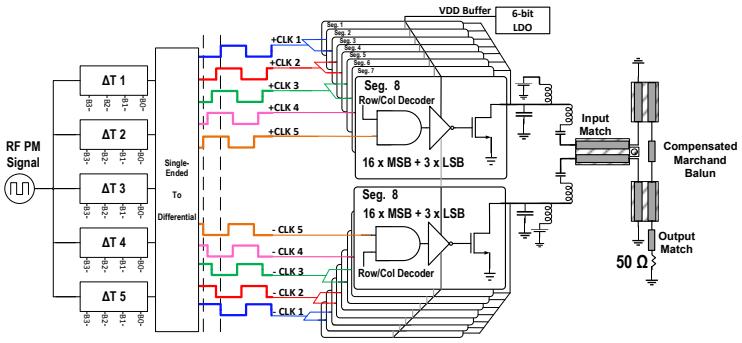

Fig. 2. Simplified block diagram of DPA showing the concurrent multi-phase RF clocking used to correct the ACW-PM distortion, nonlinear sizing along with on-chip 6-bit programmable LDO and the output load network.

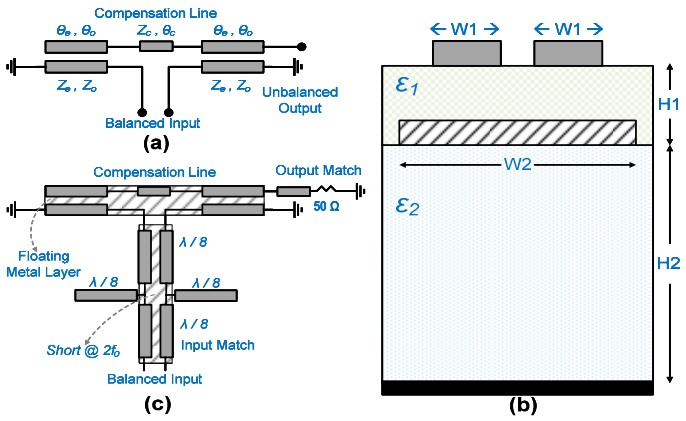

Fig. 3. (a) Marchand Balun with compensation line. (b) Re-entrant coupled lines cross section. (c) Compensated Marchand Balun with 2nd Harmonic termination implemented by λ/8 lines.

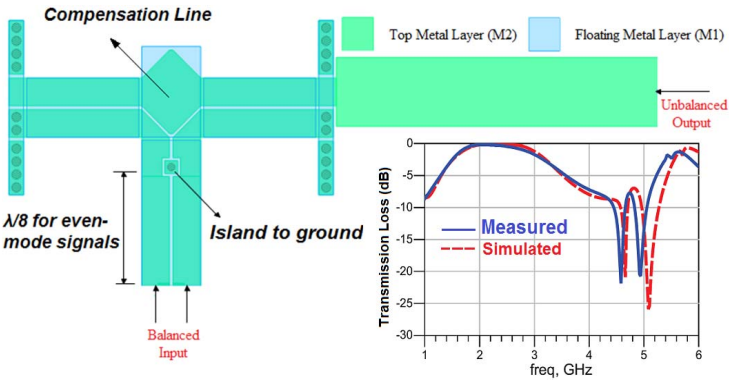

Fig. 4. Proposed compensated Marchand balun with 2nd Harmonic termination implemented by a via and the measured and simulated differential-to-single-ended transmission loss.

itches, i.e. the overdrive voltage, can be digitally tuned by an on-chip 6-bit low-dropout (LDO) DC voltage regulator, without significantly affecting peak efficiency and output power.

B. Linearizing ACW-PM

In a conventional class-E DPA as the ACW increases the output phase decreases, which leads to considerable phase distortion. In the time domain, this translates into a higher output delay for a smaller ACW. By equalizing the overall delay for smaller segments with respect to the largest segment, the overall phase distortion is corrected [5]. In this work, as depicted in Fig 2, concurrent multiphase RF clocking technique is utilized in which the input RF clock passes through a set of 5 different delay offsets to allow different phases of phase modulated RF clock to be applied to different DPA segments. In order to compensate for PVT and frequency variations, the delay-offsets are implemented by 4-bit programmable delay lines. In contrast to a conventional DPA with AM-PM correction, the delay offsets are fixed during the normal operation of the DPA and they don't adjust dynamically. In addition, all of the 5 different generated phases of RF clock are applied simultaneously to different segments. For example, at full power, all the 8 differential segments are switched on and all the 5 different phases of differential RF clocks are applied to them, while at the 6dB back-off power, the first four segments are switched on and only the RF clocks 1 and 2 (see Fig. 2) are applied to them at the same time. At the output, the currents flowing through different segments with different phases are summed and the overall phase is averaged resulting in a significant reduction in the phase distortion from 35 degrees to less than 3-5 degrees.

C. Wideband Marchand Balun

The planar Marchand balun is an attractive transmission-line based balun topology due to its wideband amplitude and phase balance and relative ease of implementation [5]-[6]. The conventional planar Marchand balun consists of two symmetrical λ/4 coupled lines with open and short circuited terminations at specified ports to provide a balanced loading condition resulting from a single-ended load. However, directly employing the coupled lines in a practical Marchand balun will lead to imperfect conversion from the unbalanced signal into the balanced signal due to unequal even- and odd- mode phase velocities. To address this issue, a compensation technique [6] shown in Fig 3.a is adopted to reduce the imbalance of the balun. In order to obtain a wideband Marchand balun at a low impedance level, a tight coupling with high even-mode impedance is required. Re-entrant coupled lines have been used to achieve tight coupling without strict requirements in circuit fabrications [5]. Fig. 3.b presents a general re-entrant type coupled line configuration. By employing the re-entrant type coupled lines with proper dielectric constant and reasonable dielectric layer thickness between the conductors, the expected tight coupling is achieved, yielding a very low-loss and wideband balun. Combining the core network of the Marchand balun with a differential re-entrant type impedance inverter (total length λ/4) using 2nd harmonic impedance control, wideband class-E digital PA performance can be facilitated. To achieve this, the network impedance provided to the differential digital class-E PA should provide an open condition for all higher harmonics and in particular for the second harmonic. In principle, by having a 2nd harmonic short circuit termination for the second harmonic after the first λ/8 section, an open circuit at the reference plane of the DPA can be achieved.

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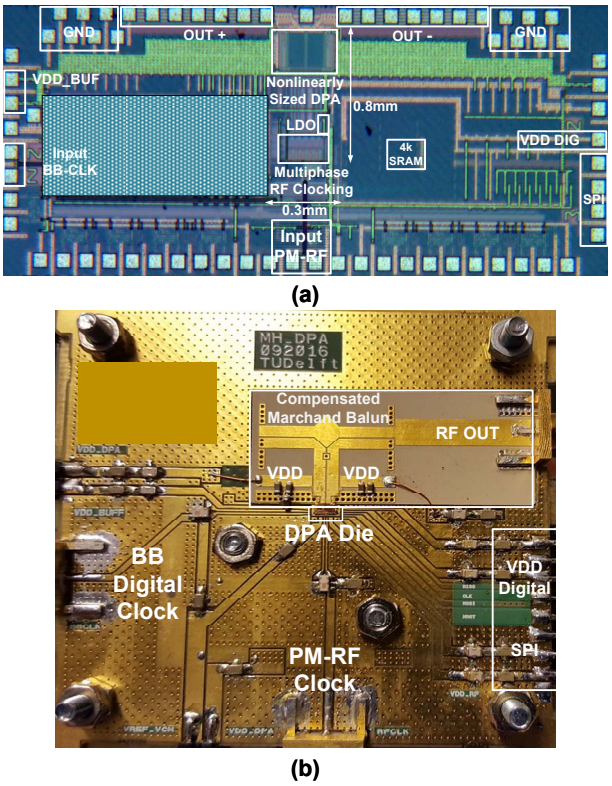

Fig. 5. (a) Die micrograph. (b) Fabricated PCBs.

However, use of two open λ/8 stubs (Fig. 3.c) for this purpose works out to be impractical, due to the large differences in even and odd mode velocities, while these stubs would also affect the fundamental impedance. Fortunately, the required even-mode 2nd harmonic short-circuit condition in the re-entrant coupled lines can be also realized by adding a simple via from the floating middle-layer conductor to ground at the position where the (even-mode) electrical length for the second harmonic $2f_0$ equals λ/8. Due to the tight coupling between the three conductors, the top metals are also automatically forced to ground for their even-mode signals, while the differential operation/terminations remain unaffected. In Fig. 4 the layout of the proposed balun with its simulated and measured transmission losses are shown.

III. Fabrication and Measurement

A prototype of the DPA is fabricated in 40nm bulk CMOS as shown in Fig 5.a. The ACW codes are stored in a 4K on-chip SRAM running at 625MHz. The DPA die is mounted on a FR4 PCB. The Marchand balun, shown in Fig 5.b, is fabricated separately on a two-layer Rogers material. The phase-modulated (PM) RF signal is generated off-chip by a differential I/Q modulator. Coarse time-alignment between the ACW and PM signals is performed in digital domain while fine tuning is realized by a 4-bit on-chip delay line. In Fig 6.a, the peak P_{OUT}, DE and PAE are measured and plotted versus center frequency for VDD = 0.7 which demonstrate a very wideband performance,

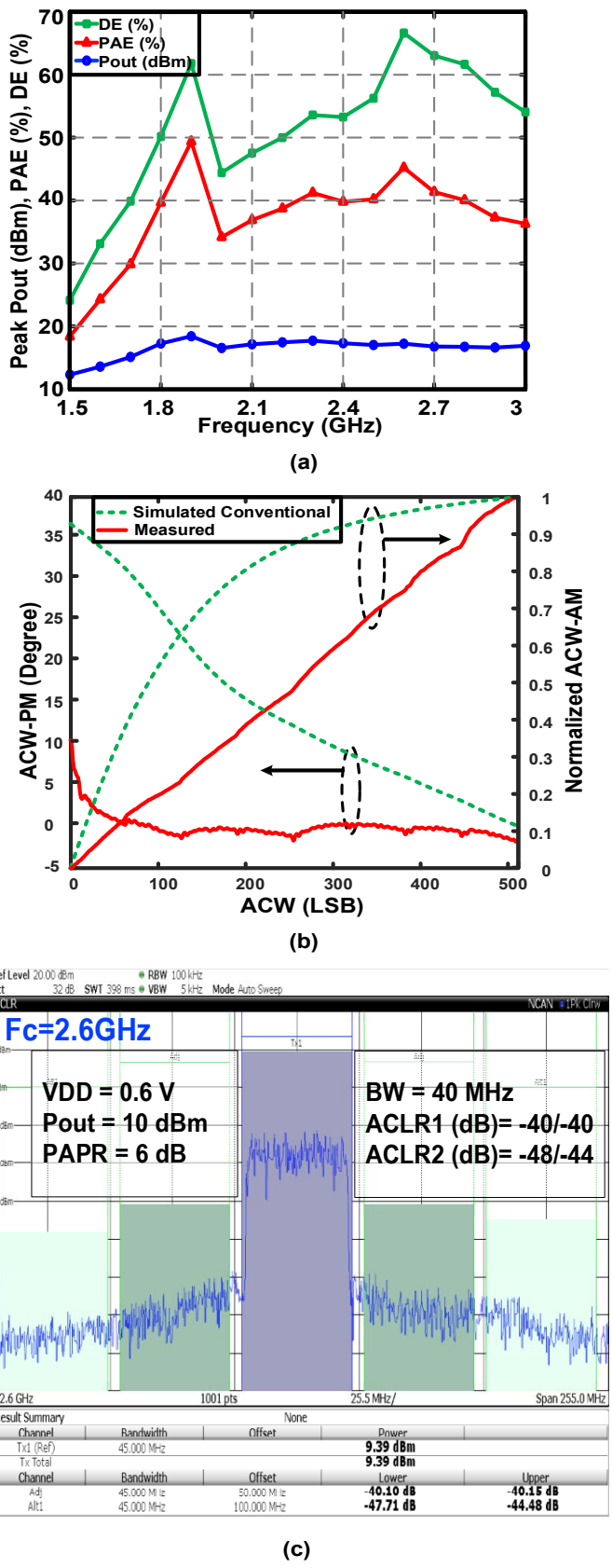

Fig. 6. (a) Static measured results Peak P_{OUT}, PAE and DE vs F_C. (b) ACW-AM and ACW-PM. (c) Output spectrum of 40MHz QAM signal.

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TABLE I
PERFORMANCE SUMMARY AND COMPARISON TABLE

Reference	**This Work**	[3]	[4]	[5]	[6]
DPA Architecture	**Class-E**	Class-D^{-1}	SC	Class-E	Class-G SC
BW (MHz)	**40**	8	20	40	20
ACLR(dBc) / Emission(dBc)	**-40/NA (VDD=0.6)**	-28/NA	NA/-30	-40/NA (F_C=2GHz)	NA/-40
DPD	**NO**	YES	NO	NO	NO
DPA Supply (V)	**0.7**	3	2.1	0.5	1.4/2.8
Fc (GHz)	**2.6**	2.6	2.1	2.2	2.15
P_{SAT} (dBm)	**17.2**	28.1	24	14.6	24.3
Peak DE (%)	**67**	41	35	44	NA
Peak PAE (%)	**45**	35	NA	29	44
Output Balun	**Off-Chip**	On-chip	On-chip	On-chip	Off-chip
CMOS (nm)	**40**	65	65	40	65

with more than 50% DE over 2.2-3GHz at 16-17dBm of output power. The peak Pout, DE and PAE are 17.2dBm, 67% and 45% at 2.6GHz with VDD=0.7. The ACW-AM and ACW-PM curves are measured and plotted in Fig 6.b. In comparison to a simulated conventional class-E DPA, a significant improvement in the linearity without any DPD is achieved, offering advantages in the energy efficient handling of wideband signals. The dynamic performance for a 40MHz QAM signal is measured and depicted in Fig 6.c showing -40dBc ACLR without using any sort of DPD. Table I summarizes and compares this work with prior art.

IV. CONCLUSION

Linearity and efficiency are key parameters in a RF transmitter. By using a novel compensated Marchand balun with re-entrant coupled lines, a very high and wideband efficiency performance is achieved. Without compromising the efficiency, using circuit level linearization techniques, a highly linear polar class-E DPA with programmable linearity is designed and measured. To the best of authors' knowledge, this work presents the highest DE for a CMOS class-E digital PA while achieving wideband RF P_{OUT} and high linearity for wideband modulated signals without using any kind of DPD.

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