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A Single-Stage Four-Phase Hybrid Boost Converter With 11-to-20 VCRs for LiDAR Driver Applications

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***Abstract*—This paper presents a monolithic single-stage, 4-phase switched-capacitor (SC) hybrid boost converter with 11-to-20× voltage conversion ratios (VCRs). The 4-phase operating SC hybrid topology is proposed to achieve high VCRs with only three flying capacitors and one inductor. With the SC topology, the average inductor current and the inductor current ripple are much reduced, releasing both power loss and size requirement for the inductor. A four-phase pulse width modulation (PWM) controller is proposed. A successive ramp generation scheme ensures identical pulse widths across three consecutive phases. A driver-assisted auxiliary charge pump provides sufficient driving voltages for the high-side driver and simplifies the overall circuitry. The proposed hybrid boost converter was implemented in a 0.18 μm process. The measurement results show that the converter achieved a 20-24V output voltage range with a 1.2-1.8 V input voltage. 76.7% peak efficiency was achieved at 13× VCR and power density was 12 mW/mm^3.**

***Index Terms*—Boost converter, multi-phase, hybrid converter, dc–dc converter, switched capacitor (SC) converter, single-stage, LiDAR driving.**

NOMENCLATURE

List of Abbreviations

CBC	Conventional boost converter.
VCR	Voltage conversion ratio.
CCM	Continuous conduction mode.
DCR	DC resistance.
PWM	Pulse width modulation.
SC	Switched-capacitor.

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I. INTRODUCTION

THE proliferation of wireless devices in Internet-of-Things (IoTs) applications necessitates efficient power management systems with photovoltaic power sources to reduce maintenance costs, extending the lifespan of IoT devices [1], [2]. Some PV-powered IoT devices, such as laser diode-based sensors, require a high supply voltage of 20-24 V [3]. A conventional solution is depicted in the upper part of Fig. 1, where the power transfer path includes two separate boost converters and a lithium battery. The first boost converter converts the low input voltage of 1.2-1.8 V from PV panels into the 2.7-3.6 V Li-ion battery voltage with efficiency at around 85%, as estimated in [4]. The second converter then boosts the battery voltage to power the laser sensor [2], working at 20-24 V with an efficiency of 80% [5]. However, utilizing two separate boost converters can reduce the system's overall efficiency to less than 70% with increased complexity and cost. A possible solution involves a single boost converter that directly amplifies the PV voltage to the required supply voltage, minimizing the system's volume and cost. However, the DC-DC converter must supply high-efficiency voltage at 20-24 V under a high voltage conversion ratio (VCR) from 11× to 20×.

Conventional boost converters (CBCs) can achieve voltage boosting with a simple system. In high VCR applications, however, CBC suffers from three main drawbacks. First, CBC requires an extremely small duty ratio (<0.1) at high VCR (>10), which limits the switching frequency and, subsequently, the dynamic performance and power density of the converter. Also, the high voltage swing on the inductor causes a large inductor current ripple, necessitating a large inductor to maintain continuous conduction mode (CCM) operation. Additionally, high-voltage-rating MOSFETs applied in CBC exhibit a more significant form factor ($R_{DSON} \times Q_{gg}$), resulting in larger size and higher switching loss, limiting the overall power efficiency of the converter. These drawbacks deteriorate the power density and efficiency of the converter in high VCR applications. As an alternative, switched capacitor (SC) converters [6] offer advantages in integration and component size reduction [7], [8], [9]. However, SC converters employ PFM control to maintain continuous output voltage regulation, at the cost of reduced power efficiency compared to the open-loop operation, also due to non-optimal switching frequency. At high VCR, the efficiency of the switched-capacitor converter is limited by significant switch-related losses and the capacitor's hard-charging loss [10].

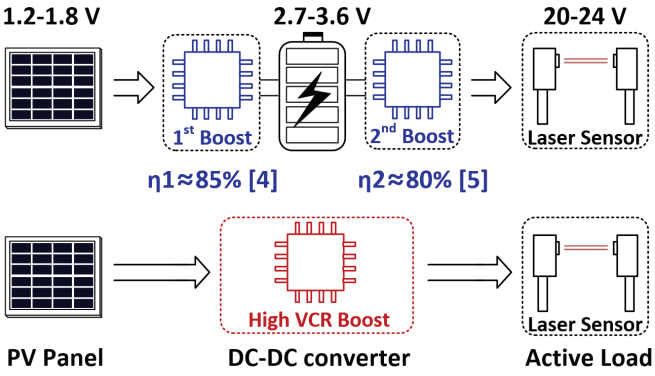

Fig. 1. Applications of a single-stage DC-DC converter in powering laser sensor by PV panel.

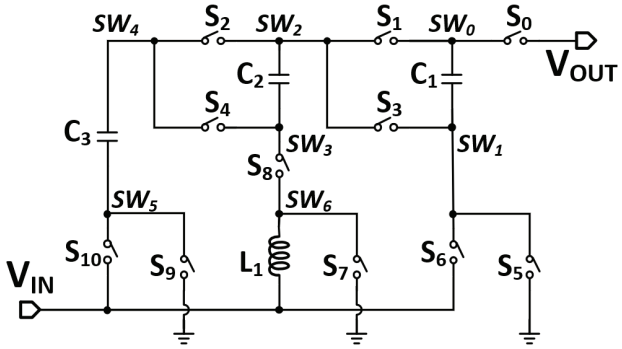

Fig. 2. Proposed four-phase hybrid boost converter.

Recently, hybrid converters, which combine switched capacitors with inductive converters, have garnered significant interest due to their unique advantages [11], [12], [13]. Firstly, hybrid converters leverage switched-capacitor networks to withstand most of the voltage stress, thereby reducing the voltage stress on power switches and minimizing conduction losses and chip size [14]. Secondly, switched capacitors mitigate current ripple by reducing the voltage swing across the inductor, as demonstrated in [11] and [15]. Additionally, hybrid topology enables multi-level voltage switching across the inductor, effectively increasing the equivalent switching frequency and reducing current ripple [16], [17]. Third, inductors can softly charge flying capacitors, reducing hard-charging loss in SC converters [18]. Last, specific hybrid topologies utilize the switched capacitor branch to establish a capacitive current pathway [14], [18], which reduces the average inductor current and the associated DC resistance (DCR) losses of the power inductor.

In high VCR applications, hybrid converters are utilized to achieve high voltage conversion ratios greater than 10× to avoid extremely small duty ratios, which will compromise control precision and increase circuit complexity. However, it may require more than five flying capacitors [11], [14] to obtain such high VCRs, which increases the number of off-chip components and causes a higher bill-of-materials and bigger board size. One possible solution is to utilize multi-phase operations to expand VCR without increasing the number of flying capacitors as in SC converters [6], [19]. This remains unexplored in hybrid boost converters, partly attributed to the challenges of using a PWM controller with multi-phase control.

Another issue with high VCR hybrid converters is the effective bootstrap circuit design. In hybrid buck converters, the drivers can be readily powered by voltage regulators derived from the inherent switch nodes within the power stage [11]. In contrast, hybrid boost converters require additional power rails [14], [17]. The challenge of obtaining adequate bootstrap voltage for high-side switches becomes more intricate as the number of power switches and switch nodes increases in multi-phase power converters.

To tackle the aforementioned issues, we propose a multi-phase hybrid SC boost converter to address the challenges of achieving high voltage conversion ratios with minimal off-chip components. The hybrid converter adopts a four-phase 10× switched capacitor converter to achieve high VCR with only three flying capacitors. The switched capacitor enables a high VCR while reducing output voltage and inductor current ripple. It also shunts the average inductor current, lowering the DCR loss of the inductor. The proposed converter utilizes a four-phase clock generation scheme based on a successive ramp generator and a dual-edge trigger. Two bootstrap methods are developed to achieve simple bootstrapping on the low side and sufficient bootstrap voltage on the high side.

The remainder of this paper is organized as follows. Section II details the concept and operational principles of the proposed boost converter. Section III describes circuit implementation and details the power stage, controller, and bootstrap circuit designs. Section IV presents the measured results, followed by Section V with conclusions.

II. Proposed Topology

Fig. 2 shows the proposed topology of the hybrid converter. It comprises three flying capacitors (C_1, C_2, and C_3), one inductor (L_1), and eleven power transistors (S_{0-10}) operating in four phases. This topology is inspired by the four-phase 10× SC converter, which obtains the highest possible VCR with three flying capacitors [20]. An inductor is incorporated to achieve continuous output and further elevate output voltage at 11× to 20× without increasing the number of passive elements. Another possible solution is using more capacitors, however, it will significantly reduce overall power density. The proposed hybrid boost converter realizes a VCR of $6+4/(1\text{-}D)$ with only three flying capacitors and one inductor, where $(1\text{-}D)$ is the duty ratio of the inductor discharge phase following the conventional boost converter. The design offers several advantages tailored for diode-based sensor applications. Firstly, the inductor enables a continuous and variable VCR, which allows for boosting photovoltaic (PV) voltage (1.2-1.8 V) to the required laser diode voltage (20-24 V) by adjusting the duty ratio (D). Secondly, the SC converter reduces the voltage stress across the inductor, resulting in a smaller inductor size and, consequently, higher power density at the same switching frequency. Thirdly, the SCC design utilizes the highest achievable VCR with three capacitors, offering a more compact solution.

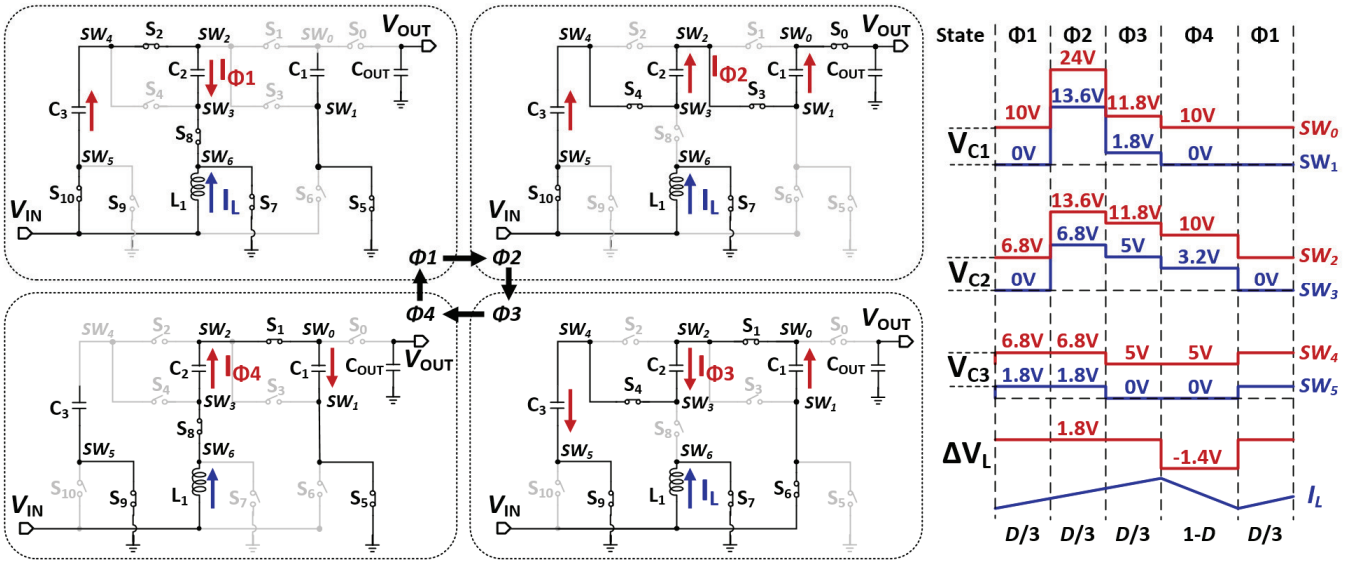

Fig. 3. Block diagram and operational waveforms of the proposed converter.

TABLE I
COMPARISON OF TOPOLOGIES

Topology	Dickson	Series-Parallel	Fibonacci	4-Phase Charge Pump	**4-Phase Hybrid**
No. of C_{FLY}	9	9	5	3	**3**
No. of Switches	28	28	16	11	**11**
No. of Phase	2	2	2	4	**4**
VCRs	10	10	13	10	**(6+4/D)**

Table I compares the number of flying capacitors, switches, and phases with several SC topologies. The proposed converter can achieve a high and continuous VCR with fewer flying capacitors and power switches.

A. Operating Principles

Fig. 3 illustrates the four consecutive operation states of the proposed converter, the operational scheme is similar to the three-capacitor four-phase SC converter.

State Φ_1 (L_1 Magnetizing): Switches S_2, S_5, S_7, S_8 and S_{10} turn on and S_0, S_1, S_3, S_4, S_6, S_9 turn off. The flying capacitor C_1 is floating. C_3 is stacked on top of V_{IN} and connected in parallel with C_2. The purpose of this phase is to obtain a higher voltage $V_{C2} = V_{IN} + V_{C3}$.

State Φ_2 (L_1 Magnetizing): Switches S_0, S_3, S_4, S_7 and S_{10} turn on and S_1, S_2, S_5, S_6, S_8 and S_9 turn off. The flying capacitors C_1, C_2, and C_3 are stacked V_{IN} to charge the output capacitor C_{OUT}. In this phase, the voltage of each flying capacitor adds up with V_{IN} to obtain V_{OUT} by series connection. Hence $V_{IN} + V_{C1} + V_{C2} + V_{C3} = V_{OUT}$.

State Φ_3 (L_1 Magnetizing): In this phase, Switches S_1, S_4, S_6, S_7 and S_9 turn on and S_0, S_2, S_3, S_5, S_8, S_{10} turn off. The flying capacitor C_1 is stacked on V_{IN} and discharges to C_2 and C_3, which are connected in series so that $V_{IN}+V_{C1} = V_{C2}+V_{C3}$.

State Φ_4 (L_1 Demagnetizing): Switches S_1, S_5, S_8 and S_9 turn on and S_0, S_2, S_3, S_4, S_6, S_7 and S_{10} turn off. At this stage, the flying capacitor C_1 is charged by C_2 and L_1 in series. C_3 is floating without any charge transfer. This phase balances the voltage ripple and achieves soft charging of C_1 and C_2.

Based on operational principles, this topology has two benefits: reducing the average inductor current and ripple current. First, in states Φ_1 and Φ_2, a portion of the input current is directed to flying capacitors, which reduces the conduction loss of the inductor. Second, one terminal of the inductor is connected to a fixed voltage (V_{IN}), and the other terminal (SW_6) is switched between ground and 3.2 V during 1.8 V to 24 V boosting. The voltage swing across the inductor, ΔV_L (<1.8 V), is significantly reduced as compared to that of conventional boost (ΔV_{L_Boost} < 22.2 V), such that inductor current ripple is reduced significantly and the required inductance and size of power inductor can be reduced in this topology.

B. Steady-States and Transfer Function Analysis

According to the operational principles in Fig. 3, (1-D) is the duty ratio of the state Φ_4, which is the inductor demagnetizing state as in a conventional boost converter. The duty ratios for the remaining three states are all equal to D/3 to simplify the PWM generator in the controller. In this topology, the inductor raises the voltage of switching node SW_4 to V_{IN}/(1-D) in the Φ_4 instead of V_{IN}, which increases the VCR to be larger than the intrinsic VCR of the charge pump. A quantitative analysis is given in (5)-(8). In the continuous current mode (CCM), based on the voltage-second balance principle of the inductor, the VCR of the proposed hybrid converter can be formulated as follows:

$$(D_{\Phi 1} + D_{\Phi 2} + D_{\Phi 3})V_{IN} + D_{\Phi 4}\,[V_{IN} - (V_{C1} - V_{C2})] = 0. \quad (1)$$

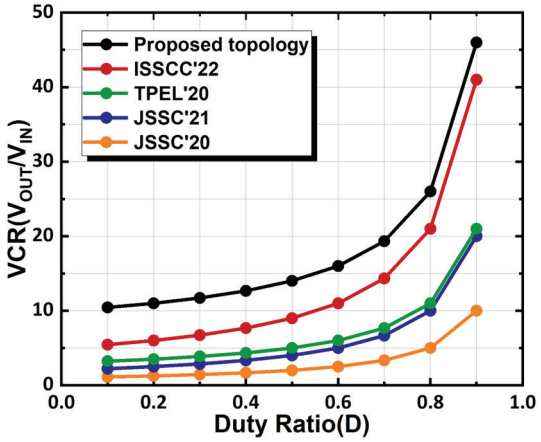

Fig. 4. Comparison of conversion ratio versus duty ratio (D) with state-of-the-art.

The voltages of flying capacitors can be obtained from operational schemes:

$$V_{IN} + V_{C3} = V_{C2}, \tag{2}$$

$$V_{IN} + V_{C1} + V_{C2} + V_{C3} = V_{OUT}, \tag{3}$$

$$V_{IN} + V_{C1} = V_{C2} + V_{C3}. \tag{4}$$

where $D_{\Phi1}$, $D_{\Phi2}$, $D_{\Phi3}$ and $D_{\Phi4}$ are the duty ratios of the states Φ_1, Φ_2, Φ_3 and Φ_4 respectively. V_{C1}, V_{C2}, and V_{C3} are the steady-state voltages of the flying capacitors C_1, C_2, and C_3, respectively. Assuming that $D_{\Phi1} = D_{\Phi2} = D_{\Phi3} = D/3$, and $D_{\Phi4} = 1\text{-}D$, the voltage conversion ratio and flying capacitor voltages are calculated by (1) to (4) and are given in (5) to (8):

$$VCR = \frac{V_{OUT}}{V_{IN}} = 6 + \frac{4}{1-D}, \tag{5}$$

$$V_{C1} = \left(2 + \frac{2}{1-D}\right) V_{IN}, \tag{6}$$

$$V_{C2} = \left(2 + \frac{1}{1-D}\right) V_{IN}, \tag{7}$$

$$V_{C3} = \left(1 + \frac{1}{1-D}\right) V_{IN}. \tag{8}$$

From Eq. (5), the voltage conversion ratio (VCR) of the proposed boost converter exceeds that of the conventional boost converter by at least an order of magnitude. Fig. 3(right) illustrates key waveforms for an input voltage (V_{IN}) of 1.8 V and an output voltage (V_{OUT}) of 24 V, with a VCR of approximately 13 and a duty ratio (D) of 0.46. The voltages across the flying capacitors are stabilized at V_{C1} = 5 V, V_{C2} = 6.8 V, and V_{C3} = 10.4 V. The flying capacitors reduce the voltage stress of power switches. Fig. 4 compares the proposed boost converter (black curve) with recent hybrid boost converters, demonstrating that it achieves a larger VCR under the same duty ratio [11], [17], [21], [22].

Based on the charge balance of capacitors at steady state, the average currents of the capacitors and the inductor for each phase are derived as follows:

$$I_{\phi1} = \frac{6}{D} I_{OUT}, \tag{9}$$

$$I_{\phi2} = \frac{3}{D} I_{OUT}, \tag{10}$$

$$I_{\phi3} = \frac{9}{D} I_{OUT}, \tag{11}$$

$$I_{\phi4} = I_L = \frac{4}{1-D} I_{OUT}, \tag{12}$$

$$I_{IN} = \frac{D}{3}\left(I_{\phi1} + I_{\phi2} + I_{\phi3}\right) + I_L = \left(6 + \frac{4}{1-D}\right) I_{OUT}. \tag{13}$$

Here, $I_{\Phi1}$, $I_{\Phi2}$, $I_{\Phi3}$, and $I_{\Phi4}$ denote the average currents flowing through the flying capacitors during each phase, respectively. The correlation between the input current (I_{IN}) and output current (I_{OUT}) substantiates the VCR calculation. In a conventional boost converter, the inductor current I_L equals the input current I_{IN}, leading to high DCR loss. In the proposed converter, I_{IN} is branched by a capacitive current path during Φ_1 and Φ_2, which can be observed from Fig. 3. I_L is hence significantly reduced according to (12) and (13). For instance, with a duty cycle of 0.46 and a VCR of 13, I_L is reduced to 55% of I_{IN}. Compared to the conventional boost converter where $I_L = I_{IN}$, the proposed converter realizes a 70% reduction of DCR loss associated with the inductor.

The inductor current and output voltage ripples are calculated as

$$\Delta i_L \approx \frac{V_{IN}}{L} D T_{SW} \tag{14}$$

$$\Delta v_{OUT} \approx \frac{V_{OUT}}{RC_{OUT}}\left(1 - \frac{D}{3}\right) T_{SW} = \frac{I_{OUT}}{f_{SW} C_{OUT}}\left[\frac{2}{3} + \frac{4}{3}\left(\frac{V_{IN}}{V_{OUT} - 6V_{IN}}\right)\right]. \tag{15}$$

This design effectively reduces both the inductor current ripple (Δi_L) and the output voltage ripple (Δv_{OUT}). From Eq. (14) and Eq. (15), the values of L and C_{OUT} are determined according to the acceptable inductor current and output voltage ripples under CCM operation. Given the assumptions of I_{OUT} = 10 mA, f_{SW} = 400 kHz, L = 10 μH, and C_{OUT} = 1 μF, and with input and output voltages of 1.8 V and 24 V, respectively, the calculated inductor current ripple and output voltage ripple are approximately 200 mA and 21.2 mV. Compared to a conventional boost converter under the same conditions, the inductor current ripple and output voltage ripple are 416 mA and 23.2 mV, respectively, 108% and 9% higher than this design. This reduces the requirement for the size of the output capacitor and inductor.

According to the steady state equations (5)-(7) and (12)-(13), the state equations of I_{COUT}(t) and V_L(t) can be written as:

$$I_{COUT}(t) = C_{OUT}\frac{dV_{OUT}(t)}{dt} = -\frac{V_{OUT}(t)}{R} + \frac{(1-D)I_L(t)}{4} \tag{16}$$

$$V_L(t) = L\frac{di_L(t)}{dt} = \frac{(5-3D)V_{in}(t)}{2} - \frac{(1-D)V_{OUT}(t)}{4}, \tag{17}$$

where R is the load resistance. After linearization and Laplace transform, the control to output transfer function can be solved

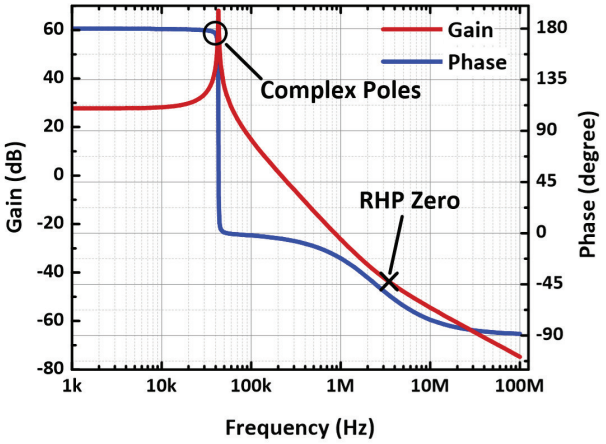

Fig. 5. Simulated open-loop frequency response of proposed converter.

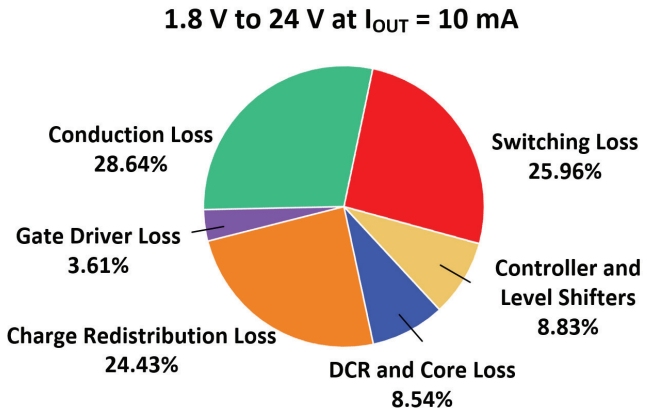

Fig. 6. Power loss breakdown of proposed converter.

as in (18):

$$\frac{\hat{V}_{OUT}}{\hat{d}} = \frac{s\frac{L}{DR}V_{OUT} - \frac{V_{IN}}{4}}{s^2LC_{OUT} + s\frac{L}{R} + \left(\frac{D}{4}\right)^2}. \tag{18}$$

When V_{IN} = 1.8 V, V_{OUT} = 24 V, I_{OUT} = 10 mA and assuming an inductance L = 10 μH and C_1 = C_2 = C_3 = C_{OUT} = 1 μF, the simulated transfer function is plotted as shown in Fig. 5. The proposed boost converter exhibits two complex poles and one high-frequency zero in the right half plane, characteristics similar to those of a conventional boost converter.

C. Power Loss Analysis

The power loss analysis in the proposed boost converter includes the conduction and switching loss, charge redistribution, gate driver loss, and inductor DCR loss.

1) The Conduction and Switching Loss: Conduction losses arise from the on-resistance of the devices, while switching losses result from voltage-current overlap during hard-switching. The switch-related loss P_{switch} includes both losses, as shown in (19).

$$P_{switch} = \sum_i \sum_j \left(D_{\phi i} I_{\phi i}^2 \cdot R_{j,dson} + \frac{2 f_{SW} I_{DS,j} V_{DS,j}^2}{dv_i/dt} \right). \tag{19}$$

In (19), $D_{\Phi\mathrm{i}}$ and $I_{\Phi\mathrm{i}}$ are the duty ratio and steady-state current, $R_{\mathrm{j,dson}}$ is the on-resistance of switch j under state i, and $\mathrm{dv_i/dt}$ is the slew rate of the switching node.

2) The Charge Redistribution Loss: The charge redistribution loss considers the charge transport loss of capacitors in the switching process, as described by Eq. (20).

$$P_C = \sum_i \sum_j \frac{C_i f_{SW}}{2} \cdot \left(V_j^2 - V_{j-1}^2 \right), \tag{20}$$

where V_{j} and $V_{\mathrm{j-1}}$ are the initial and final voltage of capacitance C_{i} at phase j, a high switching frequency and large flying capacitance can increase the charge redistribution loss.

3) The Gate Driver Loss: Gate driver losses are induced by the charging and discharging of the gate capacitor of the power switch, as specified in (21).

$$P_{driver} = \sum_j 2 f_{SW} V_{GS,j}^2 C_{OX,j}, \tag{21}$$

where j is the j_{th} switch and $C_{\mathrm{gate,j}}$ is the oxide-gate capacitance determined by the product of W and L of the power switch, respectively.

4) The Inductor's DCR and Core Loss: The total inductor DCR loss is modeled by (22).

$$P_{DCR} = I_{L,RMS}^2 R_{DCR} = \left(I_L^2 + \frac{\Delta i_L^2}{12} \right) R_{DCR}, \tag{22}$$

where I_{L} and Δi_{L} are given in Eq. (12) and Eq. (14). The core loss of inductor can be estimated by a dedicated tool from the inductor's supplier [23].

Fig. 6 shows a typical loss breakdown for simulations with V_{IN} = 1.8 V, V_{OUT} = 24 V, and P_{OUT} = 240 mW, accounting for conduction and switching losses of the power switches, charge redistribution losses, gate driver losses, controller and level shifter losses, inductor DCR and core losses. The DCR of the inductor is 480 mΩ. In this scenario, conduction, switching, and charge redistribution losses constitute more than 79% of the total losses. The sizes of the power transistors are optimized to minimize the total loss under a 10 mA load and at a switching frequency of 400 kHz.

III. Circuit Implementation

Fig. 7 shows the circuit diagram of the proposed DC-DC converter. The power stage comprises eleven power switches (S_0- S_{10}), three flying capacitors (C_1- C_3), and one inductor L_1. The feedback signal from V_{OUT} is directed to the error amplifier with a type-III compensator. Control logics are generated by the four-phase PWM controller and directed to the drivers of each power switch. The inductor, three flying capacitors, and ten bootstrap capacitors are discrete components mounted on the printed circuit board (PCB). The bootstrap circuit generates all power supply voltages of gate drivers for power switches.

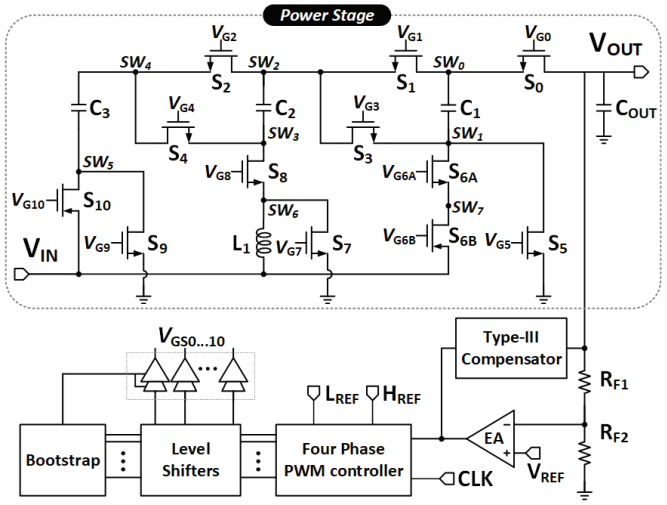

Fig. 7. Circuit implementation of proposed hybrid DC-DC converter.

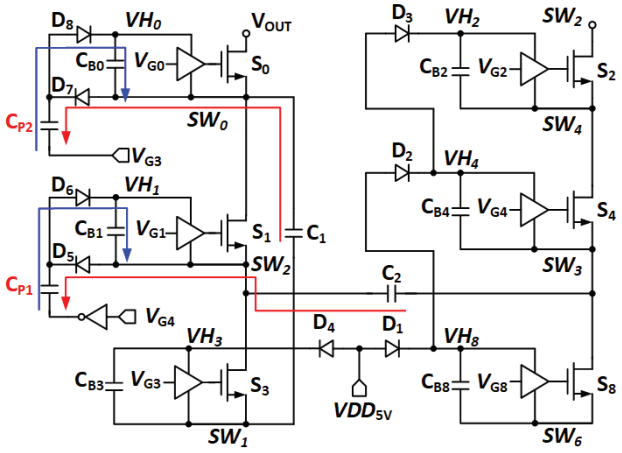

Fig. 8. Bootstrap circuit design for $S_0 - S_4$ and S_8.

TABLE II
SUMMARY OF THE VOLTAGE STRESS, TYPE, AND SIZE OF POWER SWITCHES

Switches	$V_{DS,MAX}$ (V)@1.2-to-24V	MOS Type	W/L(μm/μm)
S0	13.2	15V LDNMOS	6000/0.4
S1	10.8	15V LDNMOS	40000/0.4
S2	6.5	10V LDNMOS	10000/0.5
S3	10.8	15V LDNMOS	5000/0.4
S4	6.48	10V LDNMOS	20000/0.5
S5	13.2	15V LDNMOS	15000/0.4
S6A	13.2	15V LDNMOS	25000/0.4
S6B	1.2	5V PMOS	60000/0.5
S7	4.1	5V NMOS	15200/0.5
S8	6.5	10V LDNMOS	22000/0.5
S9	1.2	5V NMOS	16000/0.5
S10	1.2	5V PMOS	16000/0.5

A. Power Stage Design

From (5) to (8), the voltages of the switching nodes for each state are determined. To ensure adequate voltage endurance, we estimated the maximum voltage stress under the highest voltage conversion ratio (VCR) conditions, with V_{IN} = 1.2 V and V_{OUT} = 26.4 V. The proposed converter comprises eleven power switches, as summarized in Table II. The LV-PMOS S_{10} and LV-NMOS S_9 form an inverter and simplify the logic control circuit, exempting extra bootstrap capacitors and gate drivers. The voltage across V_{IN} and SW_3 is negative in state Φ_2 and stays positive in the remaining states. An LV-PMOS S_{6B} and HV-LDNMOS S_{6A} are applied as back-to-back switches to avoid current leakage through the body diode.

Considering the trade-off between the switching loss and the charge redistribution loss, the switching frequency is 400 kHz. The values of the flying capacitor and the output capacitor are set to 1 μF, resulting in a small output voltage ripple and an appropriate charge redistribution loss for the specified switching frequency and load current. An inductor value of 10 μH is chosen to maintain the power stage in continuous conduction mode (CCM), ensuring that the impact of inductor current ripple on overall efficiency is minimal.

B. Bootstrap Circuit Design

To ensure sufficient power switch driving, a 5 V supply VDD_{5V} is necessary for the bootstrap circuit, which can be sourced from a regulated charge pump or a dedicated boost converter. For a proof of concept, the supply voltage is derived from an additional 5 V voltage source VDD_{5V}.

Fig. 8 illustrates the bootstrap circuits for power switches S_0, S_1, S_2, S_3, S_4, and S_8. D_4 is the body diode of a 10 V-rated LDNMOS to withstand high voltage stress. The remaining diodes D_1-D_3 are Shockley diodes with a forward voltage drop (V_D) of 0.3 V. VDD_{5V} directly powers the drivers for transistors S_5, S_7, S_9, and S_{10}.

Three bootstrap techniques are utilized in this design to drive all switches effectively. C_{B2},C_{B3},C_{B4}, and C_{B8} are charged by conventional bootstrap circuits. For instance, when the switching nodes SW_1 and SW_6 are switched to the ground during states Φ_1 and Φ_3, VDD_{5V} charges C_{B3} and C_{B8} via D_1 and D_4 to VDD_{5V}-V_D(4.7 V). C_{B4} and C_{B2} are charged when switches S_8 and S_4 are on, respectively.

Two issues are concerned with obtaining sufficient driving voltage for the high-side switches S_0 and S_1. First, suppose cascaded bootstraps are applied to S_0 and S_1. In that case, the gate-driving voltages (V_{GS}) will decrease significantly due to the cumulative forward voltage drop across multiple diodes ($4V_D$ for S_0 and $5V_D$ for S_1), leading to increased conduction losses. Moreover, the voltage stress experienced by the high-side diodes in the bootstrap circuits of switching nodes VH_0 and VH_1 exceeds 10 V, making the use of a small V_D Shockley diode impossible in the typical fabrication process. Alternatively, utilizing the body diode of the LDMOS transistor leads to a higher voltage drop (0.7 V).

To address these issues, we employ auxiliary charge pumps with C_{P1} and C_{P2}, which are controlled by the gate driving

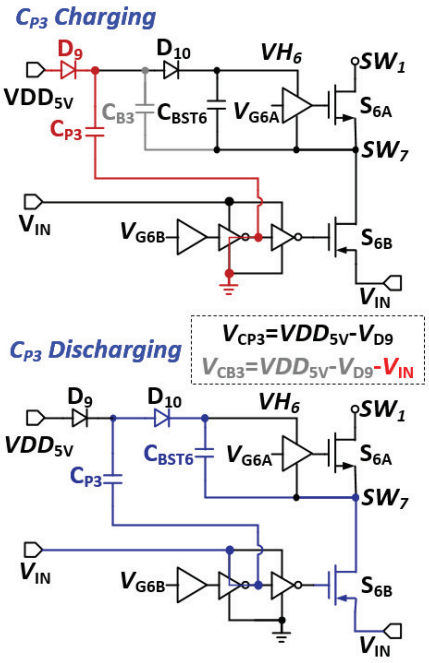

Fig. 9. The operational scheme of bootstrap circuit for back-to-back switches S_{6A} and S_{6B}.

signal V_{G3} and V_{G4}, as illustrated in Fig. 8. Take VH_0 as an example, when V_{G3} is low, C_{P2} is passively charged by C_1 through D_7, hence, $V_{CP2} = V_{C1} - V_{D7}$. When V_{G3} is high at VH_3, C_{B0} is charged by C_{P2} through D_8, hence, $V_{CB0} = V_{H3} + V_{CP2} - V_{D8} - V_{C1} = V_{H3} - V_{D7} - V_{D8}$. VH_1 is obtained with a similar mechanism. When V_{OUT} = 24 V, V_{CP2} equals 6.5 V, while V_{CP1} is 9.7 V. By taking up the majority of the voltage stress, C_{P1} and C_{P2} reduce the voltage stress on diodes D_6 and D_8 to within 5 V, enabling the use of Shockley diodes.

Fig. 9 illustrates the driver-assisted bootstrap circuit and its operational scheme for driving the back-to-back switches S_{6A} and S_{6B}. V_{IN} directly drives the 1.8 V PMOS S_{6B}, and an additional inverter is utilized to charge C_{P3} asynchronously with respect to V_{G6} of PMOS S_{6B}. When V_{G6B} is low, C_{P3} is charged by VDD_{5V} through D_9. When V_{G6B} is high, C_{P3} charges C_{B6} through D_{10}, hence, V_{CP3} equals to VDD_{5V}-V_D. For cascaded bootstrap using C_{B3} as a bootstrap capacitor, $V_{CB3} = VDD_{5V} - V_D - V_{IN}$. Therefore, V_{CP3} is one V_{IN} higher than V_{CB3} by this bootstrap scheme.

C. Four-Phase PWM Controller Design

During start-up or load transients, the output of the error amplifier may become extremely high or low, generating extremely narrow or wide duty cycles after the comparator. Since the voltage stress on power transistors depends on the duty cycle, an unbounded duty cycle can lead to voltage breakdown of the power transistor. To address this issue, a voltage clamping circuit is implemented on the output of the error amplifier, as depicted in Fig. 10. The high voltage boundary H_{REF} and low voltage boundary L_{REF} are derived from a voltage reference and compared with V_{EA}. The limited

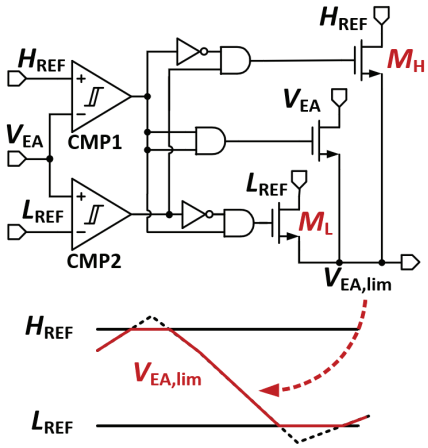

Fig. 10. Implementation and waveform of EA limit circuit.

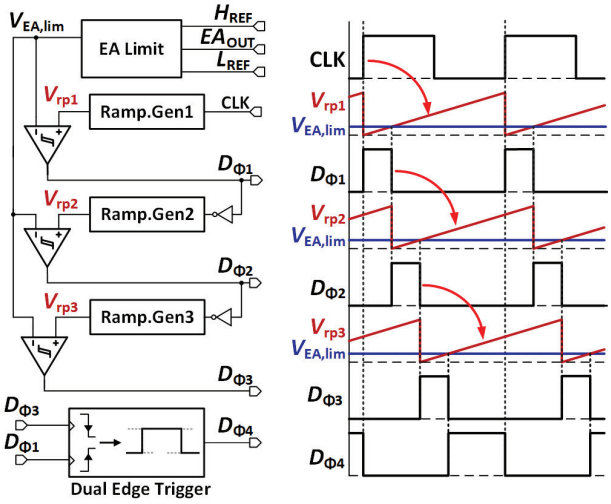

Fig. 11. The four-phase logic generation circuit nd operational waveforms.

V_{EA} signal $V_{EA,lim}$ is clamped by switch M_H and M_L, which is presented by the red line in Fig. 10.

The pulse width of the control signal determines the VCR in hybrid converters, ensuring stable and accurate pulse widths, which is crucial for effective multi-phase control. In [24], a phase copier is proposed to generate an accurate control signal with $T_{sw}/2$ delay. In this design, however, the control signal delay is duty-dependent. A successive ramp generator is proposed to address this requirement. Fig. 11 demonstrates the circuit design and waveforms for generating four-phase control signals $D_{\Phi1}$ -$_{\Phi4}$. Initially, $D_{\Phi1}$ is generated by comparing V_{rp1} with the output of the error limit circuit ($V_{EA,lim}$). The falling edge of $D_{\Phi1}$ then triggers the generation of V_{rp2}, which is subsequently compared with $V_{EA,lim}$ to obtain $D_{\Phi2}$. Similarly, $D_{\Phi3}$ is generated after $D_{\Phi2}$. Since $V_{EA,lim}$ and the three ramp generators are identical, the pulse width of $D_{\Phi1-\Phi3}$ is also equal to $D/3$. Lastly, $D_{\Phi4}$ is generated using a dual edge trigger with its pulse width determined by the falling edge of $D_{\Phi3}$ and the rising edge of $D_{\Phi1}$.

Fig. 12 shows the ramp generator circuit and the dual-edge detection circuit. In Fig. 12(a), a rising edge trigger is

TABLE III
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART BOOST CONVERTERS

Work	This Work	MAX1677[5]	LT1615[25]	TCAS-I 2020[12]	TCAS-II 2023[14]	JSSC 2020[16]
Technology	**180nm BCD**	N/A	N/A	180nm BCD	180nm BCD	65nm CMOS
Topology	**Four-Phase Hybrid Boost**	Conventional Boost	Conventional Boost	Ladder	Fibonacci-Dickon Hybrid Boost	Three-Level Boost
Chip Area	**2.23 mm²**	NA	NA	0.31 mm²	1.36 mm²	0.28 mm²
V_{IN}	**1.2-1.8 V**	0.7-5.5 V	1.2-15 V	1.8 V	2.5-5 V	0.3-3 V
V_{OUT}	**20-24 V**	V_{IN}-28 V	V_{IN}-34 V	10.8 V	40-70 V	2.4-5 V
$I_{OUT, MAX}$	**11 mA**	20 mA	20 mA	0.12 mA	2 mA	83 mA
Inductors	**10 µH**	10 µH	10 µH	NA	4.7 µH×2	1 µH
Capacitors	**1 µF×3, 0.5 µF×2, 1 nF×10**	4.7 µF	1 µF	623 pF on chip	2.2 µF×1, 220 nF×3, 150 nF×1, 1 µF×1, 1.2 nF×7	22 µF×2
Ripple	**20 mV**	25 mV	Not reported	Not reported	57 mV	10 mV
Peak Efficiency @VCR	**76.7%@13**	66%@16.7	75%@8	33%@6	54.8%@13	71%@8
Regulation	**Yes**	Yes	Yes	No	Yes	Yes
Power Density@ Max. Load	**12 mW/mm³**	7.48 mW/mm³*	6.87 mW/mm³*	4.6 mW/mm³*	2.31 mW/mm³	33.07 mW/mm³*

* Estimated from evaluation boards, application notes, and papers. Volume is estimated by summing the areas of all components and multiplying by the maximum height of the design.

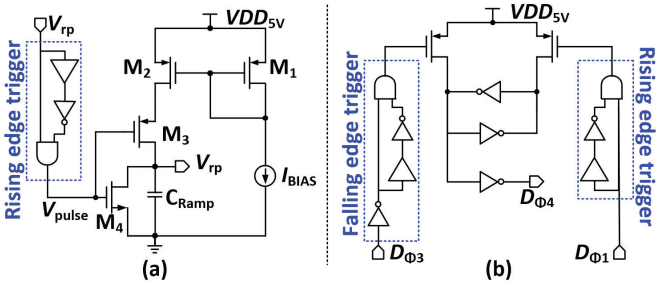

Fig. 12. (a) Ramp generator circuit and (b) dual edge trigger for D_4 generation. EA limit circuit.

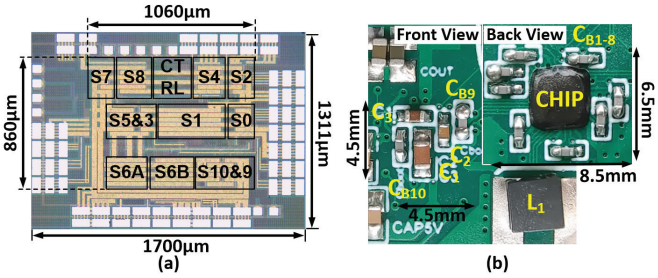

Fig. 13. (a) Die photograph; (b) PCB photograph.

incorporated into the ramp generator to facilitate the generation of sawtooth waves. To generate $D_{\Phi4}$, which equals (1-D), a dual-edge trigger is utilized, as shown in Fig. 12(b), $D_{\Phi3}$ is directed to the falling edge trigger, which subsequently induces the rise of $D_{\Phi4}$. On the other hand, $D_{\Phi1}$ is directed to a rising edge trigger, which triggers the falling edge of $D_{\Phi4}$ to obtain a pulse width equal to (1-D).

IV. MEASUREMENT RESULTS

The proposed converter was fabricated in a 0.18μm SOI process. Fig. 13(a). shows the chip micrograph and the PCB photo. The total chip area is 1700 μm ×1131 μm, limited by test pads. The active area is 1060 μm ×860 μm. On the PCB, flying capacitors C_2 and C_3 are 1 μF ceramic capacitors in the 0402 package, and C_1 is a 1μF ceramic capacitor in the 0603 package for a higher voltage rating. The output capacitors are two 0603 package 500 nF capacitors in parallel. All bootstrap capacitors are 1nF in 0402 packages on the bottom, occupying the same PCB area. The inductor L_1 is a 10μH low-profile power inductor with 480 mΩ DCR and 3 × 3 × 1 mm³ in volume.

Fig. 14a shows the measured steady-state waveforms in the typical condition when V_{IN} = 1.8 V and V_{OUT} = 24 V, achieving 13.3× VCR. Measured waveforms of switching nodes (SW_{0-5}) in four operational phases are also shown. The voltage levels of all switching nodes in steady-state are well matched with the theoretical analysis in (6)-(8). The typical DC voltages of C_{1-3} are 5 V, 6.8 V, and 10.4 V, respectively. Fig. 14b shows the output voltage ripples under different output currents (I_{OUT} = 1 mA to 10 mA), when V_{IN} = 1.8 V and V_{OUT} = 24 V. All measured output voltage ripples (Δv_{OUT}) are less than 100 mV, including the glitches caused by parasitic inductance, which is only 0.4% of V_{OUT}. Fig. 14c shows the measured inductor current with phase control signal Φ_{1-4} at a 10 mA load current. The waveforms of switching nodes during startup are shown in Fig. 14d. During power-on, the switching nodes rise at the same speed. The duties of Φ_1 to Φ_4 are equal, demonstrating the effectiveness of the four-phase controller. The load transient response is measured when V_{IN} = 1.8 V and V_{OUT} = 24 V, as shown in Fig. 15. The undershoot of V_{OUT} during the 0-to-10 mA transition is approximately 238 mV, and the overshoot during the 10-to-0 mA transition is approximately 245 mV, where both are less than 1.5% of V_{OUT}. The voltage deviation of V_{OUT} between heavy/light loads is 90 mV, leading to a voltage accuracy of 9 mV/mA.

Fig. 16 presents the measured power conversion efficiency versus output power P_{OUT} at various input voltages. The peak efficiency is 76.7% at I_{OUT} of 6.48 mA and a P_{OUT} of 155.5 mW. Fig. 17 compares the peak efficiencies versus VCR

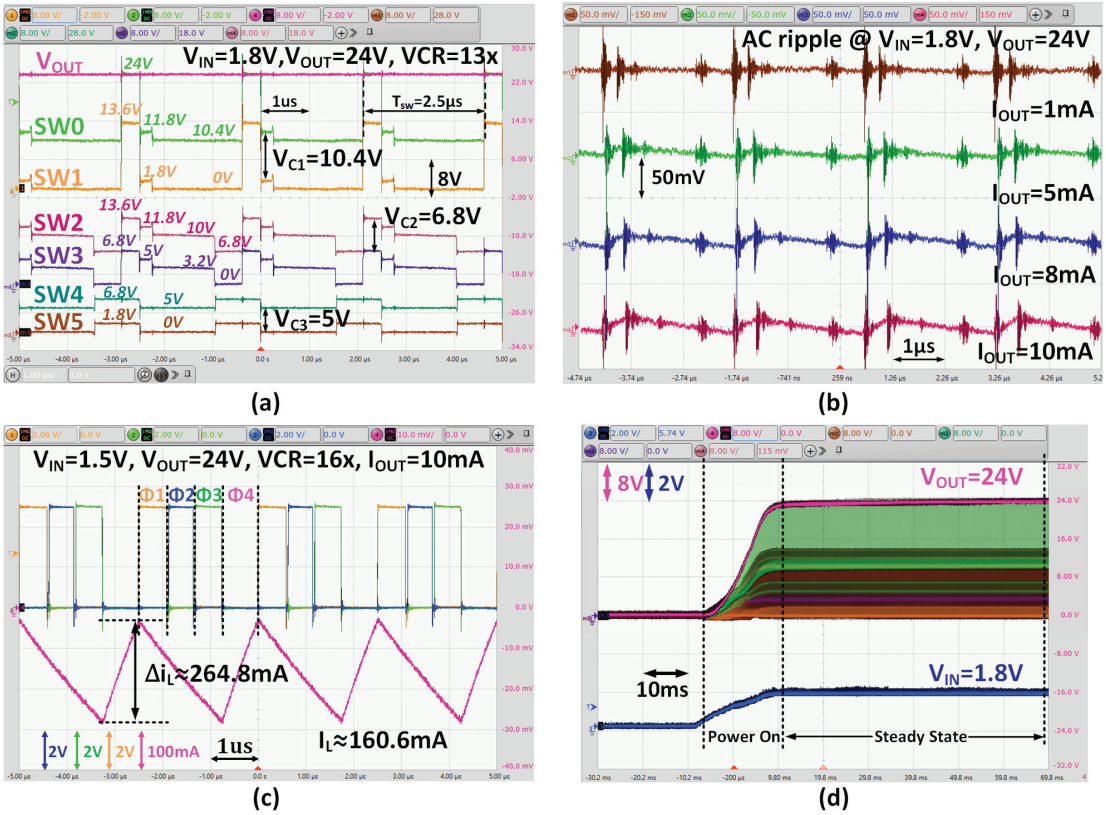

Fig. 14. Measured steady-state waveforms of the converter: (a) V_{OUT} and switching nodes connected with flying capacitors, (b) AC voltage ripple of V_{OUT} at I_{OUT} = 1mA to 10mA, (c) phase control and inductor's current ripple and (d) switching nodes during starting-up and steady state.

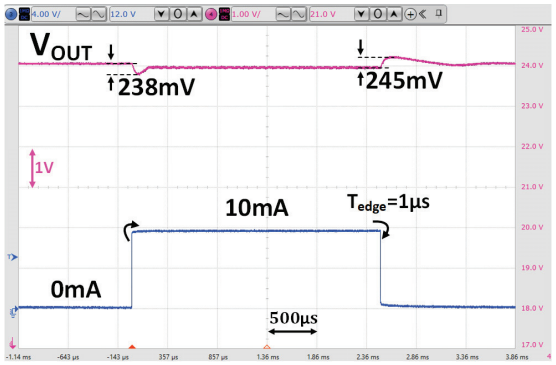

Fig. 15. Measured load transient response.

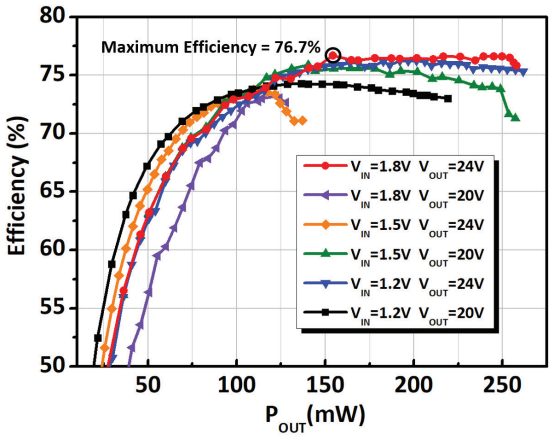

Fig. 16. Measured efficiency versus output power at 1.2V/1.5V/1.8V input, 20V/24V output.

among the state-of-the-art. This work demonstrates the highest peak efficiencies in high VCRs from 11 to 20. The maximum output power is 264 mW at 24 V output voltage. Table III compares this design with the state-of-the-art. This work achieves a regulated output with peak efficiency at 76.7% with a VCR of 13. The power density of this design is 12 mW/mm^3, thanks to the small amount and volume of discrete components, which is the second highest among all. The three-level boost converter in [16] exhibits the highest power density, but the VCR is limited to 1/(1-D), which requires a D as large as 0.95 for 20× VCR. Future improvements to this design can be explored in several directions. First, the present design employs a single current pathway per operational stage, resulting in high DC current stress on the inductor. A capacitive current path could be introduced by utilizing floating capacitors to alleviate this issue. Second, for higher voltage applications, increasing device voltage ratings may degrade topology performance. Voltage stress mitigation techniques—such as adding auxiliary capacitors [26] or clamping diodes [27]—could reduce switch and passive component stress. Third, an additional inductor (as proposed in [17]) may further minimize charge-sharing losses. Last but not least, expanding the operational modes [28] could enhance performance across a broader VCR range.

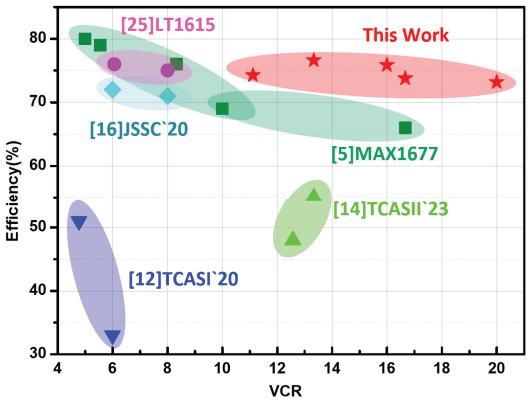

Fig. 17. Comparison on efficiency versus VCR.

V. Conclusion

This paper presents a single-stage, 4-phase SC hybrid boost converter using only three flying capacitors and one inductor to achieve high VCR, high power efficiency, small output voltage ripple, and high power density. The proposed SC hybrid converter utilizes a four-phase operating SC topology to achieve 11× to 20× high VCRs. Compared to the conventional boost converters, it reduced 55% of the average inductor current, 52% of the inductor current ripple, and 10% of the output voltage ripple. Driver-assisted charge pumps are utilized to generate sufficient bootstrap voltages for high-side power switches. The 4-phase logic generation circuit uses a successive ramp generator to obtain three identical phases without complicated phase-copy circuits or delay-locked loops. The converter achieved 20-24 V V_{OUT} with 1.2-1.8 V V_{IN} and peak efficiency at 76.7% when the VCR is 13×, attributed to reduced inductive loss and capacitive hard-charging loss. The output voltage ripple is 20 mV at the maximum load of 10mA, which is merely 0.08% of the V_{OUT}. The V_{OUT} variation of the converter upon load transient response is within 1.5%. A maximum output power of 264 mW and a power density of 12 mW/mm^3 were achieved.

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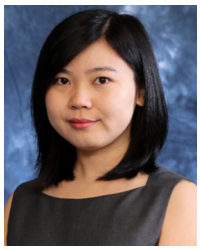

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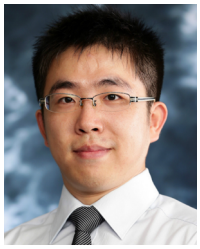

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