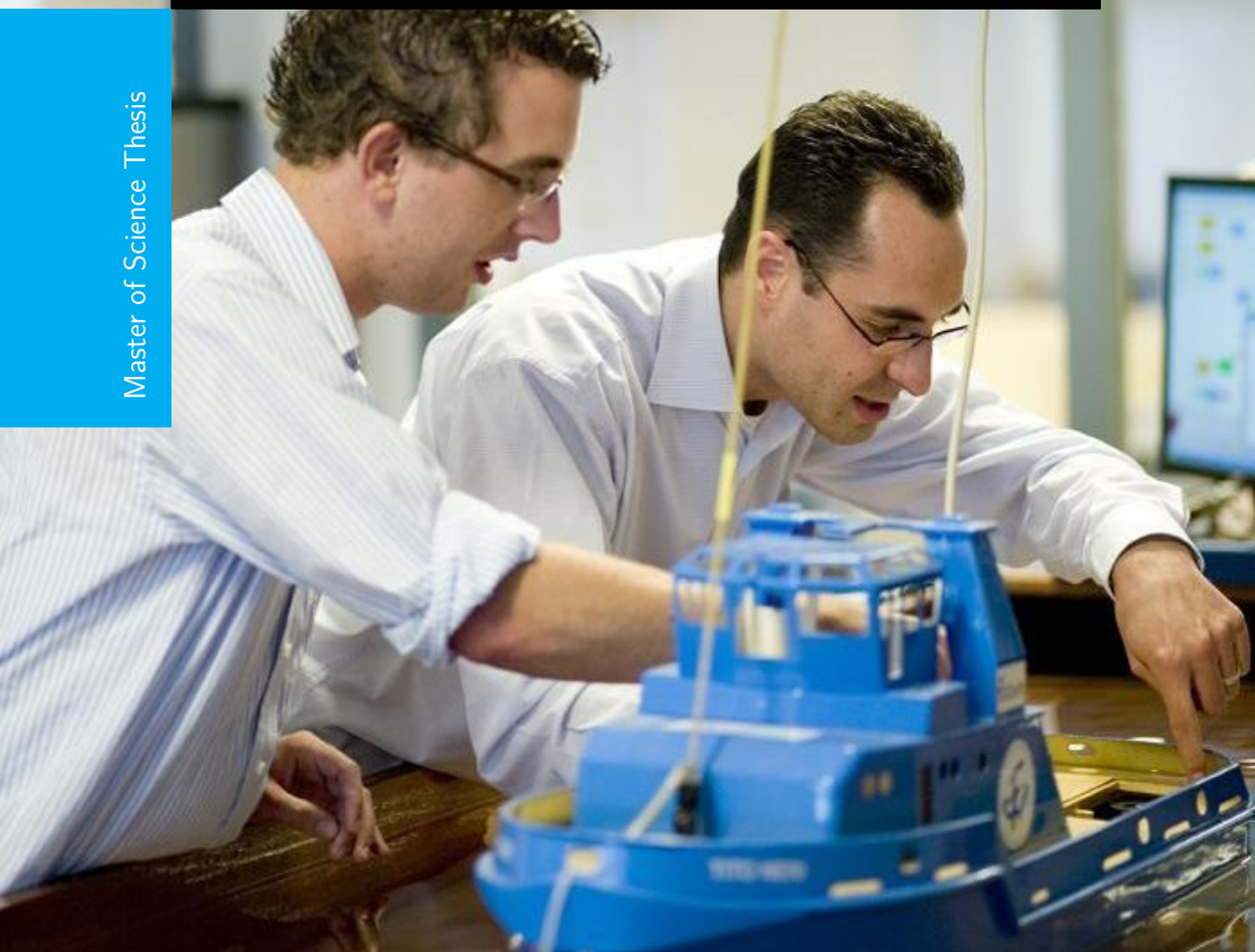


# Design of a highly efficient charger for Nickel-Iron batteries

Anil Kumar Ananda

Master of Science Thesis





# **Design of a highly efficient charger for Nickel-Iron batteries**

MASTER OF SCIENCE THESIS

For the degree of Master of Science in Electrical Power Engineering at  
Delft University of Technology

Anil Kumar Ananda

August 24, 2015

Faculty of Electrical Engineering, Mathematics and Computer Science (EEMCS) · Delft  
University of Technology



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# DESIGN OF A HIGHLY EFFICIENT CHARGER FOR NICKEL-IRON BATTERIES

by

**Anil Kumar Ananda**

in partial fulfillment of the requirements for the degree of

**Master of Science**  
in Electrical Engineering

at the Delft University of Technology,  
to be defended publicly on 28th August, 2015.

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An electronic version of this thesis is available at <http://repository.tudelft.nl/>.



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# Abstract

Obtaining good performance from stand-alone PV systems requires successful integration of batteries that are reliable, effective, long lasting, environmental-friendly and affordable as it is crucial to deal with variable solar illumination throughout the year. Nickel Iron battery technology (Ni-Fe) is a perfect fit for the solar-powered households as it satisfies all the requirements. Charge controllers need to be efficiently designed for Ni-Fe batteries for protection from overcharge/discharge.

This thesis concentrates on selecting the best topology from  $B^2R$  converters from the patent 550 of ESA to be applied for designing the charge controller for Ni-Fe batteries. An analysis is carried out to determine the advantage of  $B^2R$  converters in the patent over conventional buck-boost topologies like SEPIC or Cuk and evaluate their utility for charge control applications. The focal point of topological selection will be the evaluation of topologies on the basis of efficiency and complexity for realistic adaptation into a charge controller. After defining the load power parameters, the operation of the topologies in two different modes of conduction (BCM & CCM) is investigated and an analytical model is developed for losses. Significant factors that play a role in determining the efficiency for varying source parameters (input voltage) are scrutinized. The relative merits of using BCM/CCM for design are inspected by carrying out simulations for loss calculations using the analytical model with data-sheet parameters from realistic components for their suitability for the application. Component selection is done by keeping in mind the prevalent technologies in the market that are cost-effective and the procedure followed in the design of magnetics for the topologies in different modes of conduction and its impact on efficiency is discussed and an assessment is carried out on the performance of the components with variations in input voltage for the same power level.

The proposed analytical models for switching losses in MOSFETs and overall losses topologies are validated by carrying out experiments on the prototypes of two best topologies in both conduction modes. The results critique the accuracy of the analytical model in determining the actual efficiency of the topologies, the margin of deviation by means of comparison with the experimental results and concludes with suggestions for selecting the most efficient topology and recommends a mode of conduction for best results.





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# List of Abbreviations and Acronyms

AC	Alternating Current
BCM	Boundary Conduction Mode
BIPV	Building Integrated Photo Voltaics
BMS	Battery Management System
DET	Direct Energy Transfer
ESR	Equivalent Series Resistance
CCM	Continuous Conduction Mode
CSP	Concentrated Solar Power
DC	Direct Current
DCM	Discontinuous Conduction Mode
ESA - ESTEC	European Space Agency - European Space Research and Technology Centre
GaN	Gallium Nitride
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
Ni -Fe	Nickel - Iron
PV	Photo Voltaic
PVMD	Photo Voltaic Materials and Devices
RMS	Root Mean Square
SEPIC	Single Ended Primary Inductor Converter
SMPS	Switch Mode Power Supplies
VRLA	Valve Regulated Lead Acid
ZCS	Zero Current Switching



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Anil Kumar Ananda  
Delft, June 2015



This thesis is dedicated to my Appa, Amma and Ajji who have encouraged and supported me through all my endeavours. My salutations to you!

“Nothing in life is to be feared, it is only to be understood. Now is the time to understand more, so that we may fear less.”

“Be less curious about people and more curious about ideas.”

— *Marie Skłodowska-Curie*

“Dream is not that which you see while sleeping it is something that does not let you sleep.”

— *A.P.J. Abdul Kalam*



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# Chapter 1

---

## Introduction

The reliance on fossil fuels has seen a slight dip with the proliferation of economic integration of sources with cleaner, greener and sustainable renewable energy source in the 21<sup>st</sup> century. Photovoltaic energy generation is popular and perhaps the most promising emerging renewable energy generation due to the fact that the installation expenses of solar modules have decreased in the recent years and the whole system cost has reduced by as much too.

However, for its successful integration, PV resources are coupled with grids in most parts of Europe. In many developing countries, standalone systems are employed where grids do not exist. For the economical viability of a PV system in an off-grid environment, a reliable battery technology that is inexpensive will be key as the nature of solar insolation varies. As batteries become cheaper and more reliable, solar energy generation can reach high levels and evolve to power households. The main objective of this dissertation is to select the most appropriate DC-DC non-isolated buck-boost topology out of patent 550 [1] of ESA-ESTEC to implement battery charger for Ni-Fe batteries.

### 1-1 Objectives of the thesis

In cases where power electronic topologies are involved, specific details of the active/passive components and power parameters such as current and voltage through them will become crucial which will be explored in the parts of this report and an analytical model for losses is developed for boundary conduction mode (BCM) and continuous conduction mode (CCM) of operation. Experimental determination of results obtained by the analytical model will be verified under lab conditions and the deviation of values in terms of losses calculated will be reasoned with. The problem statement for the thesis will be as follows

### **1-1-1 Research questions**

- Which topology can be selected to build a highly efficient battery charger for Ni-Fe batteries in the patent 550 [1]?
  - For the battery charging application, is BCM or CCM an optimum solution?
  - What are the potential benefits of employing BCM/CCM control?
  - What is the methodology followed to ensure that an optimum topology is chosen?
  - Under BCM/CCM, how can one optimise the design for a specific application?

### **1-1-2 Methodology and thesis layout**

This thesis is intended to analyse the viability and adapt the topologies for battery charging applications.

- In chapter 2, the recent advances in PV generation and battery storage are discussed along with the power electronics which forms the spine for charge control application. Recent trends in battery storage, PV generation for standalone systems and techniques followed to analyse topologies are discussed.
- In chapter 3, all the five topologies are discussed and several criteria including modes of operation and parameters that will aid in simplifying the selection are deliberated.
- In chapter 4, losses in the topologies, the analytical model for calculation in both modes of operation and magnetics associated are discussed and the chapter concludes based upon the results obtained from the simulations carried out for losses and magnetics designed.
- In chapter 5, experimental results are compared to simulations to understand the deviation from theoretically calculated values of the analytical models
- Summing up all the results and conclusion of the thesis is done in chapter 6. This will be followed by the appendix.



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## Chapter 2

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# State of Art

### 2-1 Changing world order - PV proliferation

The shift from fossil fuels to sustainable energy sources is inevitable. With depleting oil resources and greenhouse gas proliferation, it is an undeniable fact that there is a stress on conducting research on the same. The real challenge for the shift is to integrate the sustainable sources is to find viable methodologies to harness these renewable sources and convert the form of energy like wind/solar to practicable form - Electricity [6]. Due to a scarcity of high wind areas in domestic settlements, solar energy is much widely adopted. Ongoing research areas like photovoltaic materials and devices (PVMD) focus on developing effective ways of efficiently converting energy from the Sun, which is a limitless source of energy. Concentrating solar power (E.g. DESERTEC) [7] and photovoltaics (panels) [8] are two common methods of converting energy from solar radiation to electricity. In case of concentrating solar plants (CSP), heliostats focus sunlight onto a tower providing heat for generation of electricity.

An increasingly popular trend that is enabled thanks to feed-in-tariff policies and price decrease is employing PV cells in modules to directly generate DC from the solar insolation. They are easy to install, making them viable for wider adoption. To meet the challenge in making solar energy cost much more competitive, the capital costs for hardware and installation of PV systems can become a bottleneck. To ease these constraints, governments have formulated policies to provide subsidies and feed-in tariffs.

With the growth of PV installations in the residential, utility and commercial segments to continue [6], one of the biggest hassles of PV technology to be adapted as a means of electricity generation is the intermittent behaviour of the source. Combining battery banks with PV systems in the off grid systems is beneficial in remote areas where a centralised grid is not accessible.

Recent advancements in battery technologies and in power electronics and control systems to monitor and control battery power levels, have enabled storage to be viable economically in combination with PV systems to utilise the energy stored during the day, in the evening after the sun has gone down [9].

## 2-2 Nickel Iron batteries

The battery storage can also be of great benefit commercially for those whose utility billing agreements have a requirement to pay demand charges for consuming power during off-peak hours [10]. Selection of a battery for applications is determined by the following parameters [11]

- Cycle life
- Nominal discharge rates
- Self-discharge rate
- Performance under extreme temperature
- Maximum current drain capacity (in Ampere-Hours)
- Watt-hours per unit weight
- Watt-hours per unit volume
- Maintenance over the life cycle
- Cost of operation per watt-hour

The above-discussed parameters are specific for applications. Desired characteristics for a PV battery in terms of performance is summarised in [11] as

- Moderately high cycle life
- High capacity appreciation at slow rate of discharge
- Highly reliable rates under conditions of cyclic discharge
- Necessity of low equalisation and boost charging
- Good watt-hour and ampere-hour efficiency under different SoC (State of Charge)
- Low self-discharge rates
- Broad temperature range under operating conditions
- Requirement for robust construction low maintenance
- Cost effectiveness to integrate with the system with low initial costs

Valve regulated lead acid (VRLA), Nickel-Metal-Hydride (NiMH), Nickel-Iron(Ni-Fe) and Lithium Ion (Li-ion) batteries are most commonly used battery technologies [10] . Ni-Fe batteries are typified by good mechanical strength and long life (up to 8 years) under well-maintained conditions. These batteries can remain non-functional at ambient temperatures of up to 40°C for a long duration under conditions of various SoC performing under negligible loss of charge and deterioration [5].

Battery life for Ni-Fe batteries is unaffected by overcharge at normal charge rates. They have high reversibility of charge/discharge reactions leading to long service life implying that the Ni-Fe batteries are well suited to be used for PV applications [12] [13].

Table 2-1 discusses the risk assessment of batteries of type Valve Regulated Lead Acid (VRLA), Lithium Ion, Ni-Fe and Zinc Bromide redox.

As seen from the table, VRLA and Zinc Bromide redox batteries pose maximum risk of

**Table 2-1:** Risk Assessment for battery technologies [5]

<i>Characteristic</i>	<i>VRLA</i>	<i>Li-ion</i>	<i>Ni-Fe</i>	<i>Zn-Br-Redox</i>
Fire ignition risk	Minimal	Medium	Minimal	High
Self Ignition risk	Minimal	High	Nil	Minimal
Environmental hazards	High	High	Nil	High
Persistence in environment	High	Not established	Nil	High
Human Toxicity risk	High	High	Minimal	High
Recycling requirements	High	Not established	Nil	High
<i>Overall hazard rating</i>	<u>Medium</u>	<u>High</u>	<u>Low</u>	<u>Very High</u>

toxic material to the environment. Lithium-ion battery type has the highest fire risk among the battery technologies. Minimal toxic material risk is observed from components in Ni-Fe batteries. It is environmentally safe to dispose of without any hazardous substance risk and they degrade very slowly with usage. However, Ni-Fe batteries have low capacity at a higher temperature and a very high weight to ampere-hour capacity ratio. Also, they have a self-discharge of up to 1-2% of the rated capacity at 27°C per day [14] and as high as 8-10% of rated capacity per day when the operational temperature reaches 40°C which is a challenge for its successful integration. From the perspective of its utilisation for PV batteries, it can be preferably used for applications in which the duty schedule would allow a recharge at least once in two days so that at least 80% of the rated capacity will be available for the loads during discharge.

## 2-3 Battery charge control

A battery charge control device also known as charge controller maintains the battery array at the highest possible state of charge (SoC) protecting it from over-charge by the PV arrays connected to it and from over-discharge by the loads connected to it. Any system involving loads with high transients, high user intervention and undersized battery storage (economic reasons) has to employ battery charge control [15].

An optimum control strategy is a measure of the effectiveness of charging/discharging of the battery and utilisation of PV generation to meet the demand of the load. However, it should also feature protection against external factors such as temperature; voltage sense leads will

help maintain the battery health and extend its operating lifetime [16] [17].

## 2-4 Role of power converters

The heart of a charge controller is its power converter also known as charger is dedicated to adjust the power parameters suited to operate the battery charging and discharging safely and efficiently despite changing input conditions from the solar panels. The power converters can step-up or step-down or step-up/down the voltage depending upon the power parameters described by the battery and solar panel manufacturers. Normally used power converter topologies for step down, step up and step up/down are the buck, boost and buck-boost/flyback topologies due to their ease of implementation. There are some primary factors to be considered for the purpose of power conversion in charging applications.

- Voltage and current parameters of solar array and battery stack
- Environmental conditions
- Battery technology

Power converters have proliferated in the form of Switched Mode Power Supplies (SMPS) in the past decade and they are turning out to be path-breaking in terms of increasing the power density and reducing the volume of the system [18]. Switches and diodes are undergoing massive face-lifts in their power capability at higher temperatures due to advances in the field of semiconductor technology [19]. Newer technologies like SiC and GaN are expected to improve the switching device efficiencies due to extremely low switching losses under higher temperatures for a higher range of power and frequencies [20] [21].

## 2-5 Topological evaluation

The basic requisites for determining a topology, its components and its design for a specific operation are

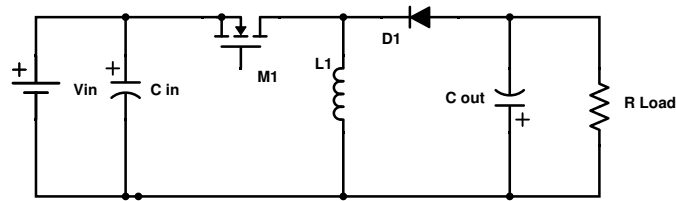
- Input voltage range ( $V_{in}$ )
- Output voltage ( $V_{out}$ )
- Output load current ( $I_{out}$ )
- Output power ( $P_{out}$ )

To evaluate topologies, it is very important to classify the requisite performance parameters for design. Loss mechanisms depend upon the type of semiconductor device used. Hence, development of an analytical model for comparative analysis which involves different power converters is riddled with complexity considering the parameters involved [22]. Some metrics for comparison can become significant

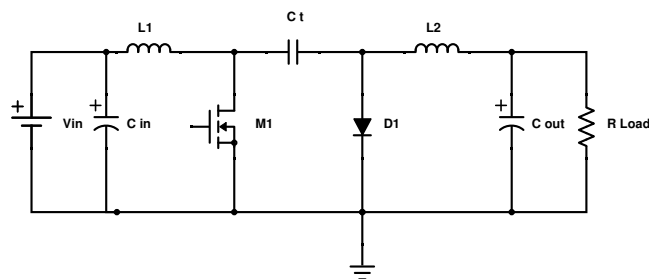
- Robustness
- Power density
- Efficiency
- Construction related aspects and complexity
- Cost

Significant single switch topologies that can carry out step-up/step-down of input voltage are buck-boost, SEPIC and Cuk. They are as follows

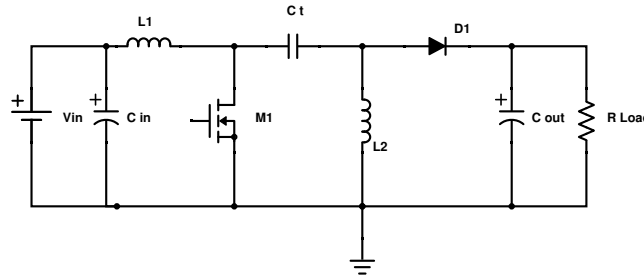
- Output voltage of a single switch buck-boost converter is the opposite polarity with respect to the input and the operating switch needs a high side driver as one of its terminals are not grounded as shown in figure 2-1 .
- A Cuk converter has high number of reactive components, high current stresses on the switch, diode and the transfer capacitor  $C_t$  [23] as shown in figure 2-2.
- In a SEPIC converter, a maximum switch voltage is equal to the input voltage plus the output voltage. Thus voltage stresses in the switches in this types of converter are very high. Figure 2-3 shows a SEPIC converter topology.



**Figure 2-1:** Buck Boost Converter



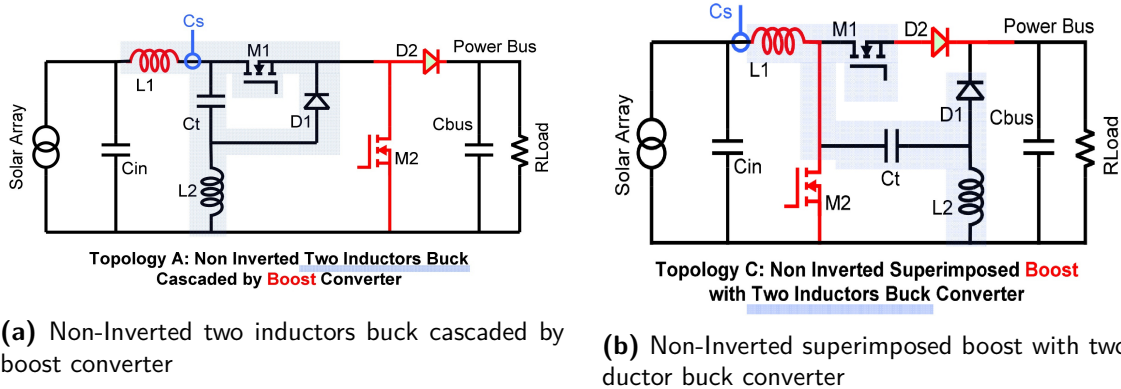
**Figure 2-2:** Cuk Converter



**Figure 2-3:** SEPIC Converter

There are several disadvantages associated with a single switch buck-boost converter as discussed in the above section necessitating the study of topologies with cascaded buck-boost converters with two switches. The topologies on offer for evaluation by ESA for the thesis as summarised in [1] include

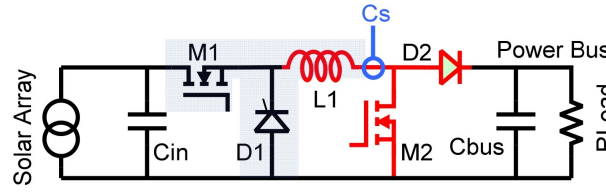
1. Non-Inverted buck cascaded by a boost converter - figure 2-5
2. Non-Inverted two inductors buck cascaded by boost converter - figure 2-4a
3. Non-Inverted superimposed boost with two inductors buck converter - figure 2-4b
4. Non-Inverted superimposed two inductors boost with a buck converter - figure 2-6a
5. Non-Inverted buck cascaded by two inductors boost converter - figure 2-6b



**Figure 2-4:** Two inductors buck converter topologies [1]

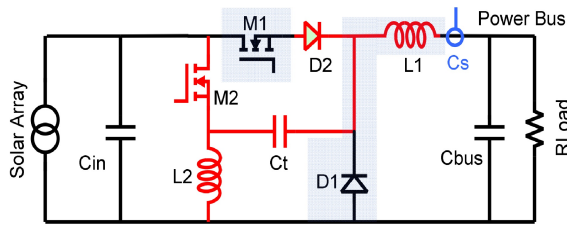
All the topologies are two-switch converters and function as a step-up or step-down depending upon the input/output operating conditions of voltage [24]. Some new topologies have a better switch stress profile as compared to single switch topologies such as buck-boost, SEPIC and Cuk. These new topologies are cascaded, interleaved or superimposed. One way to evaluate topologies is by bringing into focus the active device ratings, their RMS/peak/average current and voltage stress [25].

In the conventional boost and buck converters, output power will contain two components. First component is the indirect power  $P_{indirect}$ , processed by switches by using the inductor for intermediate energy storage. Second component is the direct power,  $P_{direct}$ , which

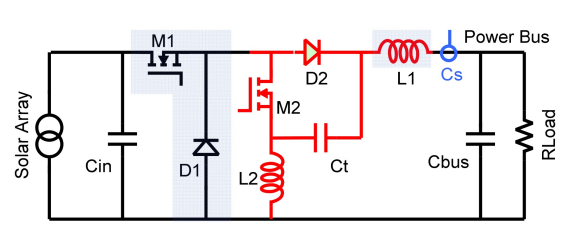


**Topology B: Non Inverted Buck Cascaded by Boost Converter**

**Figure 2-5:** Non-Inverted buck cascaded by a boost converter [1]



**Topology D: Non Inverted Superimposed Two Inductors Boost with Buck Converter**



**Topology E: Non Inverted Buck Cascaded by Two Inductors Boost Converter**

(a) Non-Inverted superimposed two inductors boost with a buck converter

(b) Non-Inverted buck cascaded by two inductors boost converter

**Figure 2-6:** Two inductors boost converter topologies [1]

flows directly to the output terminal by foregoing the intermediate process. In single-switch topologies (i.e. the single switch buck-boost, SEPIC and Cuk)

$$P_{direct} = 0 \quad (2-1)$$

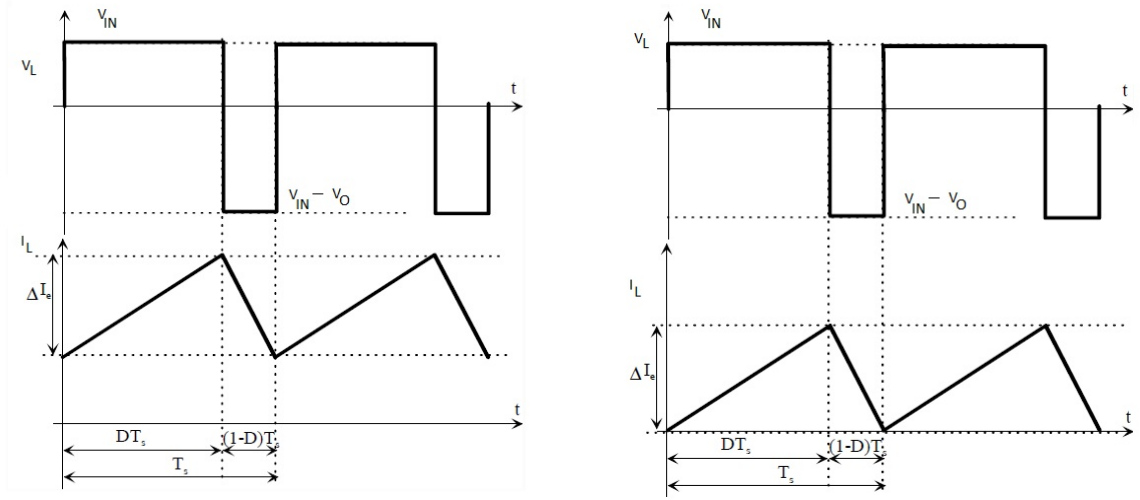
This capability of providing direct energy path indicates lower stresses in the components, lower energy storage and as a result much better efficiency. To determine the most efficient topology is one of the objectives of this thesis as mentioned in chapter 1.

## 2-6 Modes of operation

Operation modes in power converters which are widely used are continuous conduction mode (CCM) and boundary conduction mode (BCM).

CCM and BCM are referred to depending upon the current flow through the inductance of the converter. BCM is the boundary of continuous conduction mode and discontinuous conduction mode [26] [27]. The nature of inductor current in case of CCM is continuous i.e. it never falls to a zero value as shown in figure 2-7a in case of boost operation. However, in case of BCM, a new switching period will be initiated when the value of inductor current dips to zero as shown in figure 2-7b in case of boost operation.

Evidently, BCM will have a higher inductor RMS current value depending upon the voltage parameters and the same higher values can be expected through MOSFETs and diodes. However, it helps in better switching conditions. This is because the reverse recovery in diodes is eliminated and the MOSFET is turned on with zero current effectively reducing the switching on loss [28]. Summarising BCM vis-a-vis CCM, it has following benefits



(a) Boost Converter in Continuous Conduction Mode

(b) Boost Converter in Boundary Conduction Mode

**Figure 2-7: CCM and BCM**

- Self-protection capability as the inductor current reaches a zero value every cycle
- Reduced turn-on losses

Discontinuous conduction mode is not discussed in the latter parts of the report as it was discarded due to its several disadvantages as mentioned below

- Ripple in the output capacitor is higher than the other two modes.
- At lower load condition, it has very low efficiency.

## 2-7 Efficiency calculations

Higher switching frequencies in an SMPS helps in reducing harmonics associated with the converters associated. However, this will cause significant switching power losses and efficiency degradation during the power conversion [29]. The fact that high switching frequencies can effect low conduction and magnetic core related losses is surveyed in [30]. The core losses of magnetic components are independent of the load current. Lower switching frequencies can have the opposite effects. Total losses in a system can be given by

$$P_{total} = P_{active} + P_{passive} \quad (2-2)$$

$$P_{active} = P_{MOSFET} + P_{diode} \quad (2-3)$$

$$P_{passive} = P_{inductor} + P_{capacitor} \quad (2-4)$$

$$P_{inductor} = P_{windings} + P_{core} \quad (2-5)$$



In case of CCM, higher switching frequencies can result in high core losses in inductor core and switching losses in MOSFETs.

In case of BCM, the frequency is dependent upon the difference between the input and output voltages. The frequency of operation is directly proportional to the difference between the input and output voltages.

The stresses in the active devices such as MOSFETs and Schottky diodes yield greater influence on topology metrics like cost, performance and efficiency [31]. The conduction losses in topologies that use MOSFETs as active switching devices rely on the voltage levels that are considered in the initial design specifications. This effect is important as the increase of overall losses impacts the design due to the fact that high volume heat sinks will become necessary to drain the heat. This effect has consequences on the size and volume of the converter [32].

## 2-8 Conclusion

This part of the report provided an insight into the state of the art on prevalent battery charging issues and discussed a few concepts on converter design that provide a basis to build on for evaluation of the topologies. Summarising chapter 2, following conclusions can be drawn,

- PV generation is evolving steadily to become one of the major sources of energy. For PV technology to power households without intermittent behaviour, batteries play a major role in the integration of PV technologies.
- Ni-Fe battery technology is undergoing advancements and will play a pivotal role in blending PV technology. Potentially it can be used for PV applications due to its safety standards, its robustness and inexpensive capital expenditures.
- Battery charge control is a must for any battery technology to ensure that highest SoC is maintained and overcharge or over discharge is prevented.
- To evaluate a topology, an analytical model of its performance under ideal conditions can work as a precursor to determining its suitability for an application. The capability of a topology in providing direct energy path is preferred for higher efficiency and low switch stresses.
- Efficiency calculations under different operation modes for power converters will depend on power parameters, operating frequency and application requirements.



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## Chapter 3

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# Topologies

In chapter 2, we focused on the current state of the art for building power converters for battery charging application and criterion for selection of topologies. Chapter 3 tries to establish basics of how topologies can be evaluated individually and then compared on the basis of modes of conduction.

### 3-1 $B^2R$ DC-DC converter topologies

Single-switch step-up/step-down converters (i.e. buck-boost, SEPIC and Cuk) have higher current stresses on active devices as compared to the conventional buck or boost converter. A buck-boost converter with a couple of independently controlled switches for buck and boost operation can help achieve lower stresses.

The patent 550 [1] showcases a new class of converters achieve buck-boost operation by utilising the cascade, interleaved and superimposed connections of buck and boost converters. There are 5 topologies to be checked for efficiency for the above parameters.

- Topology B - Reference topology - Non-Inverted buck cascaded by a boost converter
- Topology A - Non-Inverted two inductors buck cascaded by boost converter
- Topology C - Non-Inverted superimposed boost with two inductor buck converter
- Topology D - Non-Inverted superimposed two inductors boost with a buck converter
- Topology E - Non-Inverted buck cascaded by two inductors boost converter

To design a converter for a specific application effectively, it is very important to obtain the power parameters. The design of the converter will be carried out for parameters as shown in table 3-1. In each case, we determine conduction and switching losses for a varying input voltage of 30V to 45V.

**Table 3-1:** Power parameters

Maximum Output Power	$P_{o,max}$	106.4W
Minimum output power	$P_{o,min}$	21.28W
Fast charging current	$I_{o,fc}$	2.66A
Minimum input voltage	$V_{in,min}$	30V
Maximum input voltage	$V_{in,max}$	45V
Nominal output voltage	$V_o$	40V
Switching frequency	$f_{sw}$	150kHz

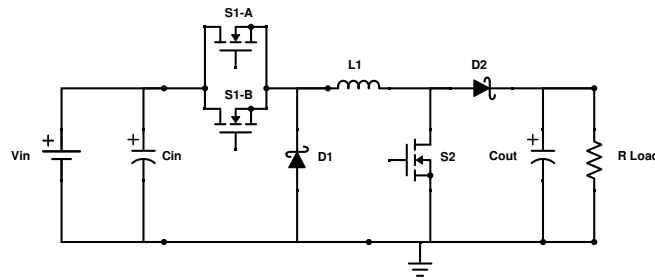
1. Boost mode, when the input voltage is between 30V and 39V.
2. Direct Energy Transfer (DET), when input voltage is equal to 40V.
3. Buck mode, when the input voltage is between 41V and 45V.

N.B. The switching frequency is fixed at 150 kHz for CCM only. The switching frequency varies with the variation in input voltage in case of BCM. This change will be discussed in the subsequent sections in this chapter.

## 3-2 Topologies overview

A buck-boost converter with two independently controlled switches can work as a boost or as a buck converter depending upon input-output conditions and thus achieves lower stresses on components.

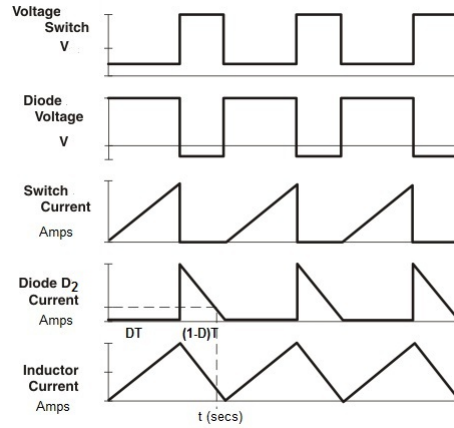
### 3-2-1 Topology B

**Figure 3-1:** Topology B

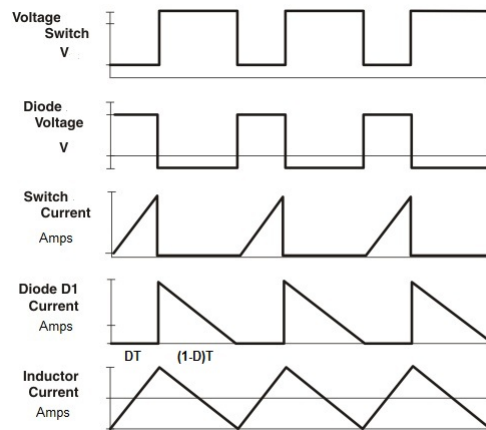
Topology B is a Non-Inverted buck cascaded by a boost converter as shown in figure 3-1. This is practically the simplest power converter among the five topologies as it eliminates the need of an extra inductor and a capacitor with reverse current capability. The selection of components becomes straightforward in comparison to the other four topologies. This topology has the capability for implementing a direct energy path and it has a widely adjustable output voltage.

(In figure 3-1, we observe two switches S1-A and S1-B in place of a single switch S1. The

necessity for such a circuit is explained in the section 3-3.)



**Figure 3-2:** Current and Voltage waveforms in Topology B in Boost mode

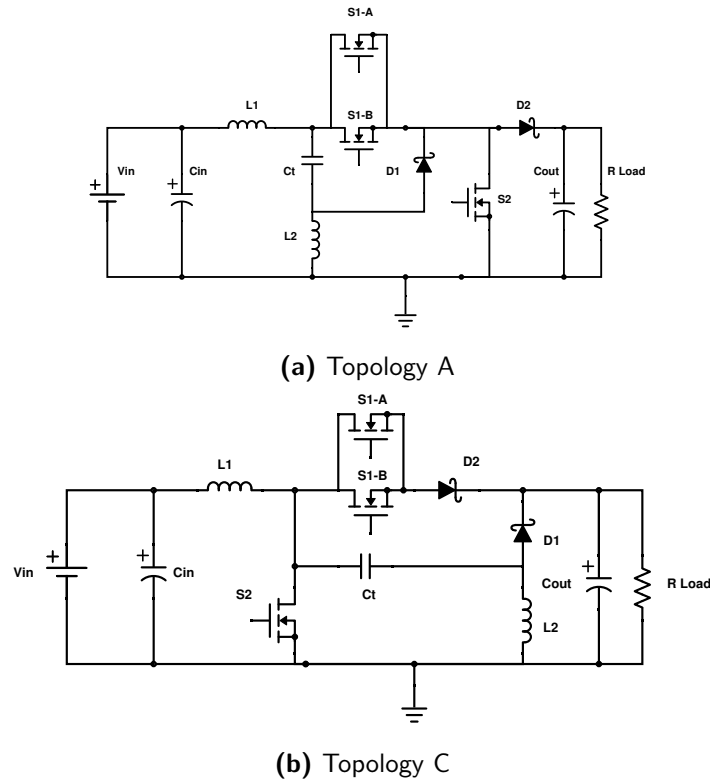


**Figure 3-3:** Current and Voltage waveforms in Topology B in Buck mode

During boost operation, the control should enable the S1-A switch to be always on and S2 is switched for stepping up the voltage. Contrarily, during buck operation, S1-A and S2 are turned off and S1-B is switched. This control scheme enables minimum indirect power characteristic reducing the switch stresses.

The waveforms of currents through devices during buck operation is given in 3-3 and boost is given in 3-2. This topology displays increased conduction losses at the input as a result of MOSFET S1-A during the boost operation and diode conduction losses at D2 during the buck operation. Therefore, other two-switch buck-boost converter topologies are also considered (topology A, C, D, and E) and compared for their performances in metrics of component conduction losses and stresses.

### 3-2-2 Topology A and C



**Figure 3-4:** Two inductor buck based converter topologies

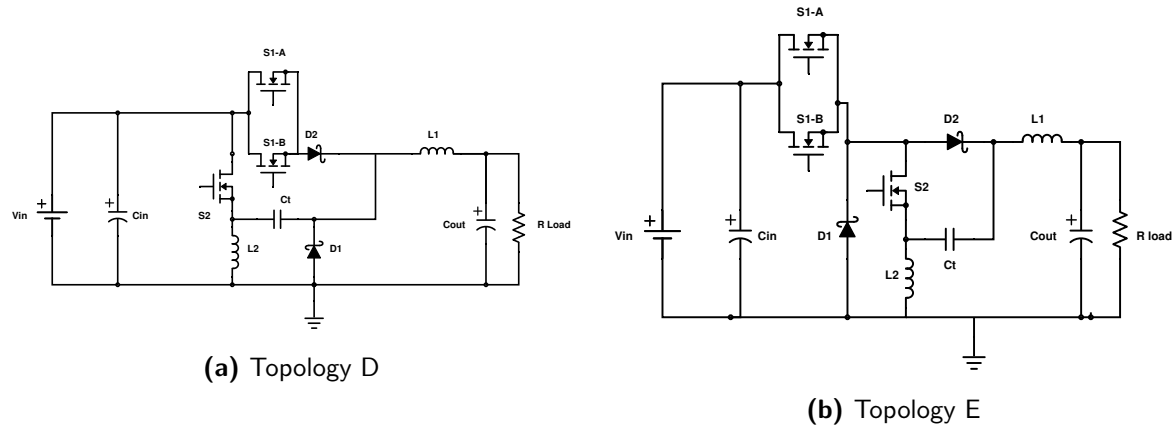
Topology A utilises a two inductor buck cascaded by a conventional boost converter topology for achieving the buck-boost conversion as shown in figure 3-4a. On the other hand, topology C utilises a two inductor buck superimposed by a conventional boost converter topology for achieving the buck-boost conversion as shown in figure 3-4b. Topology A and C operate as follows

- In boost mode, MOSFET S1-A is always switched on and S2 is switched with a PWM.
- In buck mode, MOSFETs S1-A and S2 are switched off and S1-B is switched with a PWM.

### 3-2-3 Topology D and E

Topology D contains a two inductor boost super-imposed with a conventional buck converter topology as shown in figure 3-5a. Topology E contains a conventional buck cascaded with a two inductor boost converter topology as shown in figure 3-5b. Topology D and E operate as follows

- In boost mode, MOSFET S1-A is always switched on and S2 is switched with a PWM.



**Figure 3-5:** Two Inductor Boost Based Converter Topologies

- In buck mode, MOSFETs S1-A and S2 are switched off and S1-B is switched with a PWM.

These topologies can be utilised in situations where a continuous current should be maintained to the load in situations when the output capacitors fail. Inductor  $L_1$  will ensure the current to the output remains continuous.

### 3-3 Necessity of switches S1-A and S1-B

All topologies that are under discussion carry out the buck and boost operations through different switching duty cycles. Let us assume a possibility in which topology B is under operation.

There are two operations the MOSFET S1 is intended to do.

- Operate in '*overdrive*' mode where the MOSFET will be conducting continuously in the boost mode when the input voltage is less than the output voltage as shown in figure 3-6a.
- Operate as a switch for a PWM to carry out buck operation when the input voltage is greater than the output voltage as shown in figure 3-6b.

To achieve these two operations, separate drivers need to be used. Connecting a single switch to two drivers is not advisable as the gate to source terminals connected to a high side driver will be shorted when it is not supplying a signal to the MOSFET for operation. Hence, a two switch solution is utilised where the high-side driver IR-2117 is used the MOSFET S1-B is operated in buck mode and PWM are to be supplied for its operation.

When the input voltage is lesser than the output and the operation is boost, the driver LT-1910 is used in driving S1-A in '*overdrive*' mode in which a continuous gate to source voltage is supplied to the MOSFET.

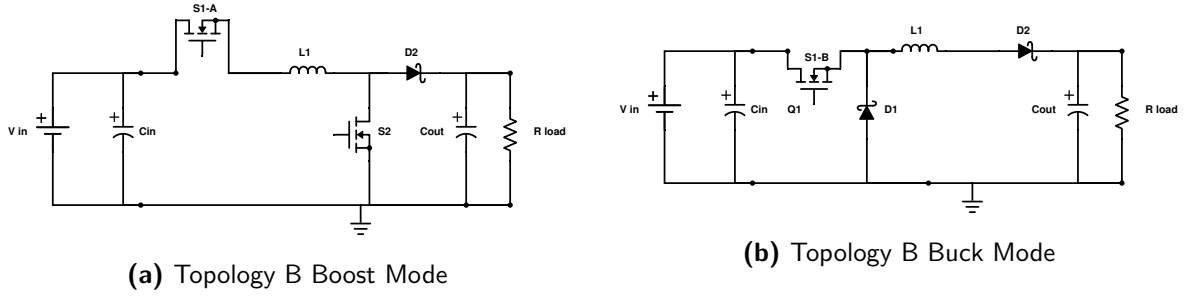


Figure 3-6: Necessity of S1-A and S1-B

### 3-4 Selecting the topology for design

#### Size

The converter designed will be used in the Battery Management System (BMS) that will be used along with the batteries. Since the system will be in operation in a domestic household or a storage room, it is safe to assume that size of the converter to be employed in the system does not have a restriction. Although the size of active devices used is negligible, the major size considerations will be the volume of the passive devices like capacitors and inductors. The effort is made to ensure that the use of a heat sink is avoided by means of effective natural convection.

To make a comparison of the size of the converters of each topology we consider the following parameters

- Energy storage in the passive components which is proportional to their size. The maximum stored energy for an inductor during a cycle is given by  $\frac{1}{2}LI_{L,Peak}^2$  and energy stored in the capacitor is given by  $\frac{1}{2}CV_{C,Peak}^2$ .
- Size of individual components - sometimes it becomes necessary to provide thermal protection and spacing to passive components (with fans) and active components (with heat sinks) which might increase the size of the system [33].

Ni-Fe batteries are characterised by the low energy density and large physical dimensions; the overall size of the converter does not become paramount for selection [27].

#### Overall efficiency

In the process of evaluating topologies for selection, efficiency becomes an important parameter. A decrease in losses enables design with no necessity to use additional cooling methods. The overall efficiency of the system is one of the measures of selecting a suitable topology [34]. By increasing the efficiency, the best utilization of PV generation can be realized.

#### Complexity

The topology selected should be less complex to ensure that it is inexpensive and easier for construction. The complexity can be realised by the number and type of components [35].



## 3-5 Comparison of the topologies

### 3-5-1 Efficiency

The most important selection criterion for the topology in our case is the efficiency of the converter. Although it is possible to achieve high efficiency at the expense of costlier materials and technologies for components, efficiency and cost have to be optimised to ensure that trade-off among the two does not disrupt the design.

Of the power losses in a converter, special attention is given to the switching devices with regards to their switching and conduction losses. Package details for the diodes and switches also play an important role in terms of heat sinking capabilities and their losses due to thermal quantities [36].

Overall efficiency due to magnetics with the ferrite core and winding losses depend upon the switching frequency, the size and the geometry of the component. The output capacitance and input capacitance by employing a proper design are less significant as compared to active devices w.r.t. efficiency. The introduction of transfer capacitance  $C_t$  in the two inductor topologies can reduce the efficiency. A detailed analysis of efficiency will be carried out in the subsequent chapters of this thesis and will dominate the latter part of the analysis for selection of the topologies.

### 3-5-2 Complexity

Among all the topologies, topology B requires the least number of components. The topologies A, C, D and E involve two inductors and a transfer capacitor. The voltage ratings of input and output capacitors are not very high (50V); However, the current rating of  $C_t$ , transfer capacitor is very high. The analytical model for calculating currents, losses and designing the magnetics, as a result, is not straightforward either. Also, the extra magnetic component in the form of an inductor for a converter means that the optimum design will have to be carried out for the specific topology separately.

The number of inductors and capacitors is given by the table 3-2.

**Table 3-2:** Number of passive components

	Inductors	Capacitors
Topology A	2	3
Topology B	1	2
Topology C	2	3
Topology D	2	3
Topology E	2	3

## 3-6 Modes of operation

It is always an interesting prospect to decide on the mode of conduction in Non-Isolated topologies. In CCM (continuous conduction mode), the current through the inductor never

hits zero. On the contrary, in BCM (boundary condition mode), the switching time starts when the current through the inductor returns to zero. Both the modes have their own influence on switching losses and conduction losses. Also, the design of the circuit and the solutions to component selection change as well. Firstly, the three modes of power converters are

1. Continuous Conduction Mode
2. Boundary Conduction Mode
3. Discontinuous Conduction Mode

### **Continuous Conduction Mode - CCM**

In CCM, the current through the inductor has a non-zero positive value all the time. It has 2 components - ripple and DC. The DC value is quite often specified by the average value of the current through the inductor and ripple is defined in terms of peak to peak value which will be triangular. In this mode, the value of inductance will determine the ripple value in the inductor. The frequency of switching will be fixed for an application which utilises CCM.

### **Boundary Conduction Mode - BCM**

In BCM, the switching time starts when the current through the inductor returns to zero. Hence, the current waveshape is a triangular signal and it does not have a DC offset. In this mode, the inductance required will be limited and a variable frequency operation is adopted.

### **Discontinuous Conduction Mode - DCM**

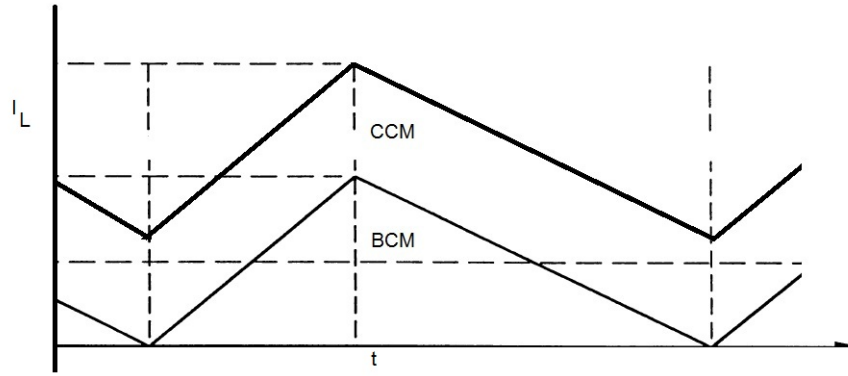
In DCM, the current through the inductor always returns to zero before closing the switch. The converter characteristics will change when it enters DCM and it has several disadvantages

- Ripple in the output capacitor is higher than the other modes restricting its application.
- Lower efficiency at lower load condition as compared to other modes.

### **3-6-1 When can BCM become advantageous over CCM?**

BCM mode has a higher value of RMS current in the inductor and active devices (diode and MOSFET) in conditions when the difference between input and output voltages is very high. But, it enables significantly better switching condition of the active devices. This is because reverse recovery of the devices are eliminated and a fast-recovery would not be quintessential. The switch (MOSFET) will be turned on when there will be zero current through the device reducing the switching on loss.

Upon switching on the MOSFET, the peak inductor current ( $I_{L,peak}$ ) and input Voltage ( $V_{in}$ ) are directly proportional. The current waveform is a triangular one with no DC offset implying



**Figure 3-7:** Diff. in BCM and CCM Modes (Not to scale)

that value of  $V_{avg}$  in one whole period is dependent upon the value of the input voltage and directly proportional.

For a particular power level, even though the peak inductor current ( $I_{L,peak}$ ) is higher for a BCM based topology, the power loss due to RMS value of current in the windings is less when the difference between input and output voltages is less (as frequency decreases) and the value of inductance required in the circuit will become much smaller. These advantages will be discussed in the coming sections.

### 3-6-2 Condition for BCM

To assess if the converter is in BCM, CCM or DCM, the following procedure is employed. We define the current ripple ratio  $r$  as

$$r = \frac{\Delta I}{I_{dc}} \quad (3-1)$$

Where,

$I_{DC}$  = average value of current

$\Delta I$  = ripple current value - peak to peak

In case the value of 'r' is less than 2, CCM exists.

In case the value of 'r' is exactly 2, BCM exists.

Otherwise, the system enters DCM.

The currents through the devices in each mode is derived in the appendix-A and the inductor currents are described in Figure 3-7.

### 3-6-3 Frequency effects

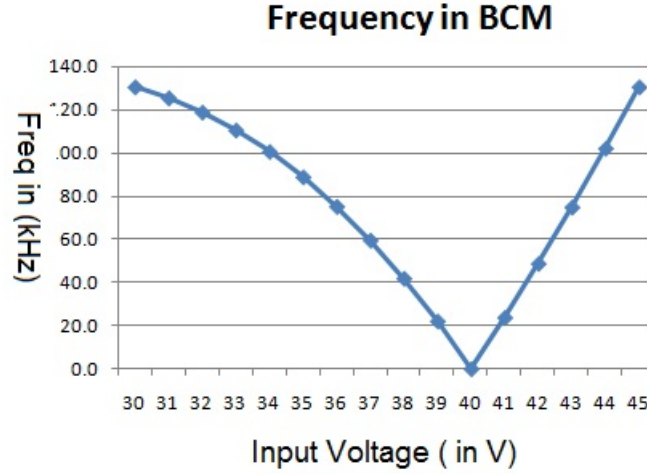
In case of BCM, the frequency can change depending upon a particular value of input voltage and a fixed output voltage. In buck mode, the frequency varies as seen in the eq. 3-2

$$f_{buck} = \frac{V_o^2(V_{in} - V_o)}{2P_{o,max}V_{in}L} \quad (3-2)$$

In boost mode, it varies as shown in eq. 3-3

$$f_{bst} = \frac{V_{in}^2 D}{2P_{o,max} V_{in} L} \quad (3-3)$$

For example, an inductance value of  $8.13\mu H$  would have the following operating frequencies as shown in figure 3-8 for the power parameters mentioned in table 3-1 in page 14. From



**Figure 3-8:** BCM frequencies

figure 3-8, it is evident that a smaller inductance value can be utilised for the purpose of design in case of BCM as varying frequency maintains the ripple current in the inductor. In the topologies for comparison, to optimise the design for comparison, the inductance  $L_1$  is reduced to a lower value to switch it at close to 150 kHz when the highest voltage difference is observed between input and output voltages.

### 3-6-4 Change in magnetics

The magnetics design will have to be optimised for BCM and CCM separately. This is due to the fact that the inductor currents are different for both modes.

#### BCM

In case of BCM, the ripple value will extend from zero to the peak value and is predominant. This significantly modifies the RMS values of currents through windings and it is much desired to reduce the value of AC resistance of the windings. These losses happen due to 'Skin effect' and 'Proximity effect' which can be averted by using customised specifications of windings. This customisation can be the usage of Litz wires [37].

The core losses might be significantly lesser due to the fact that the frequency changes to accommodate for a change in peak current value. This is the reason for which the core material selection in terms of shape and material quality is dependent on the extreme values of operation of the converter.

## CCM

In case of CCM, there are two parts to the inductor current. The DC offset value is usually equated to the average value and the AC component is given by the value of peak to peak ripple. This presents us with a diverse set of equations necessary for calculations.

The winding resistances play an important part in the losses in the inductor. The DC resistance of the winding accounts for the losses due to the average current component and the AC component ensures that the losses due to the peak to peak ripple are taken care of. In case of CCM, it is possible to utilise the normal copper windings instead of Litz due to presence of a DC component and reduced skin effect/proximity effect based losses.

## 3-7 Conclusion

- The five topologies discussed are a new class of converters that work with independent switches by utilising cascade, interleaving and superimposition of buck and boost topologies to achieve buck-boost operation.
- Switches S1-A and S1-B need to be incorporated due to issues with the high side driver for achieving operation in both buck and boost modes.
- Topology selection for a power converter application can be done by assessing size requirements, efficiency and complexity of design.



# Losses and component selection

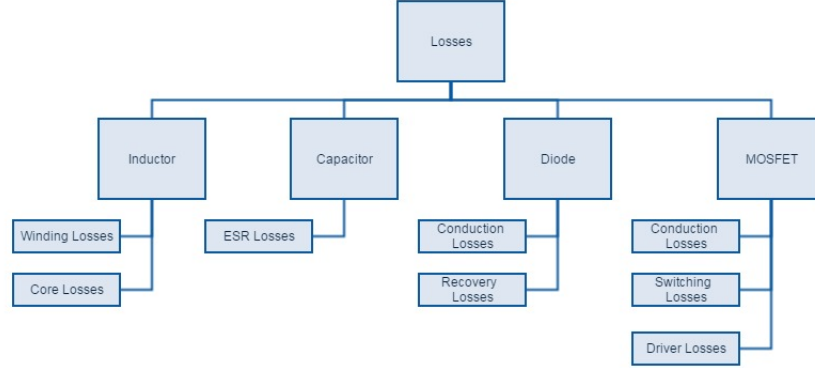
In chapter 3, a discussion was carried out for the contender topologies for the design of the charger for Battery Management System (BMS) of a Ni-Fe battery. The necessary drivers for selection and their performance under different modes of conduction were examined. Efficiency becomes the focal point of selection for which a thorough analysis of losses and its impact on the performance of the topologies for the application has to be carried out. It is the norm to use switched mode power designs as compared to linear power design due to the fact that efficiency is a significant parameter. When a designer is challenged to decrease the power losses of a switched power supply, it is vital to understand the specifics of power dissipation and component selection as key parameters. In this chapter, an effort is made to understand, elucidate and develop analytical models for analysing losses. Component selection will be determined by losses and rating levels of components will depend upon the electrical parameters which the individual devices have to be designed.

### 4-1 Losses overview

In case of inductors, the current through an inductor in CCM can be divided into average current and the ripple current. The purpose of such segregation can be justified due to the nature of winding losses. In case of resistances offered by inductors, due to skin effect, proximity and eddy current losses, an AC component of resistance can be assumed for the ripple in the inductor current. The DC resistance of the winding is first calculated and the AC resistance is calculated by virtue of the Dowell's curve [38].

In case the inductor runs in BCM mode, the total AC resistance is only taken into account to calculate winding losses as the waveform for current is a triangular wave with no DC offset. In case of core losses in the inductor, we observe the factor of frequency coming into play for the core material. The core material selected for the purpose is a ferroxcube 3C95 material and the losses are explained in the coming sections.

Losses in a capacitor are calculated by estimating the ESR value of the capacitor. In case of topology B, the capacitance  $C_t$  is absent. In all other topologies, it is significant as it carries a



**Figure 4-1:** Losses Overview

ripple current through it, indicative of the fact that a low ESR capacitor with reverse current handling capability becomes necessary. ESR also depends upon the frequency at which the ripples are passed through them which needs to be accounted for as well.

Losses in semiconductor elements in the topology can be divided into conduction and switching losses.

- Switching losses - When a MOSFET or diode transitions from blocking to the conducting state and the other way around, there exists significant voltage and current between its terminals. The energy built up between transitions and later, if dissipated is calculated at each such existence.
- Conduction losses - When the device is working in full conduction at rated values of current and voltage, these losses occur in a proportionality to that of the duty cycle.

To calculate the conduction losses in most of the devices,  $R_{device}$  can be DC resistance in case of an inductor, ESR in case of capacitor and  $R_{ds,on}$  in case of a MOSFET. However, there is an exception!

In case of a Schottky diode, there is a necessity to obtain the average and RMS value to account for non-linearity of its forward resistance characteristics.

Since most device currents are either triangular/sawtooth (BCM) or triangular/sawtooth with an offset (CCM) as shown in figure 4-2, the following formula will be applied to find the RMS values of current. In case of a triangular signal

$$I_{rms} = \frac{I_{peak}}{\sqrt{3}} \quad (4-1)$$

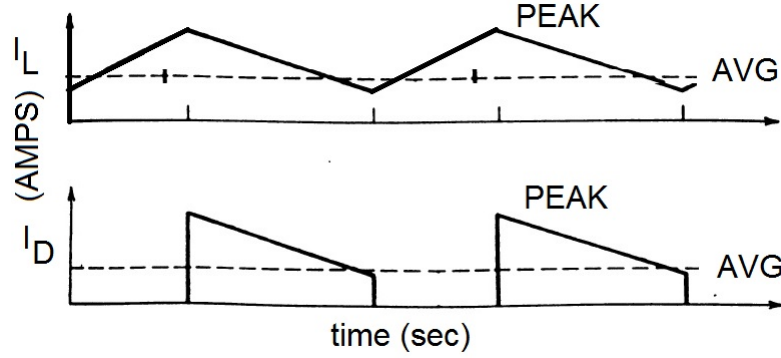
In case of a DC offset-ed triangular signal

$$I_{rms} = I_{avg} \sqrt{1 + \frac{1}{3} \left( \frac{\Delta I_{peak}}{2I_{avg}} \right)^2} \quad (4-2)$$

In case of pulsating signal with linear ripple is given by.

$$I_{rms} = I_{avg} \sqrt{D} \sqrt{1 + \frac{1}{3} \left( \frac{\Delta I_{peak}}{2I_{avg}} \right)^2} \quad (4-3)$$





**Figure 4-2:** Current Wave-shapes

#### 4-1-1 Ripple current and its effect on the device selection

In case of inductor selection and design, ripple currents play a vital role. Ripple and inductance are inversely proportional.

In case of boost operation,

$$\Delta I_{L,pk-pk} = \frac{V_{in} D_{boost}}{L} \quad (4-4)$$

In case of buck operation,

$$\Delta I_{L,pk-pk} = \frac{(V_{in} - V_o) D_{buck}}{L} \quad (4-5)$$

In both circumstances, it can be observed that for a fixed frequency, higher the inductance value, lower the ripple. There exist two modes of operation for which we calculate the currents.

In case of CCM, this value needs to be optimised to achieve necessary operating conditions of ripple.

In case of BCM, this condition is not significant, as the frequency is changed to maintain a triangular signal without a DC offset which ensures that the signal is triangular (Ripple only). However, the  $\Delta I_{L,pk-pk}$  is equal to  $I_{L,peak}$  value in case of BCM.

## 4-2 Capacitor losses

Capacitor losses are assessed as they are crucial for their capability to regulate the voltage at the output, supply for the inductor ripple at the input and transfer of energy between the two inductors (in case of two inductor topologies).

Capacitors with high losses can lead to high leakage current during the operation resulting in an unwarranted temperature increase in them. Internal heat dissipation can aid evaporation of the electrolyte that will harm the quality of the capacitor.

From the datasheets, ESR (Equivalent Series Resistance) value has to be derived for a specific frequency of operation. The discernible power loss, when divided by the reactive power of the capacitor at a particular sinusoidal voltage of specified frequency, is given by

$$\tan\delta = ESR(2\pi fC) \quad (4-6)$$

To find out the ESR at a particular frequency, frequency multipliers are provided in the data-sheets of electrolytic capacitors. Under most circumstances, the ESR of a capacitor is provided at 120 Hz or 100 Hz. Since we operate the switch at 150 kHz, the following conversion is used.

$$\left(\frac{I_{150kHz}}{I_{120Hz}}\right)^2 = \frac{ESR_{120Hz}}{ESR_{100kHz}} = freq.mult^2 \quad (4-7)$$

The most important parameter in a data-sheet for a capacitor is the ripple current rating. The currents in the input, output and transfer capacitance in each mode is as follows,

### Buck

$$I_{Cin,rms} = \sqrt{I_{sw,rms}^2 - I_{sw,avg}^2} \quad (4-8)$$

$$I_{Cout,rms} = \sqrt{I_{L,rms}^2 - I_{L,avg}^2} \quad (4-9)$$

In case of Topologies A and C, through the transfer capacitor  $C_t$ , the RMS value of current is given by

$$I_{Ct,rms} = \sqrt{I_{L1,rms}^2 D_{buck} - I_{L,avg}^2 (1 - D_{buck})} \quad (4-10)$$

### Boost

$$I_{Cin,rms} = \sqrt{I_{L,rms}^2 - I_{L,avg}^2} \quad (4-11)$$

$$I_{Cout,rms} = \sqrt{I_{D,rms}^2 - I_{D,avg}^2} \quad (4-12)$$

In case of Topologies D and E

$$I_{Ct,rms} = \sqrt{I_{L1,rms}^2 D_{boost} - I_{L,avg}^2 (1 - D_{boost})} \quad (4-13)$$

The transfer capacitor  $C_t$  is usually a film type as it can have a high current capability with low ESR.

The power loss in the capacitors in every case is given by

$$P_{cap,loss} = I_{cap,rms}^2 ESR_{cap} \quad (4-14)$$

## 4-3 Diode losses

Due to dynamic resistance property of the diode, it is not straightforward to calculate the conduction and reverse recovery losses of the device. In this segment, we discuss how the calculations are done, the manner in which the assumptions play a role and the parameters that can be neglected. A thorough analysis is done to carry out the conduction loss calculation in the diode for the buck-boost converters. The assumption made in the set of formulae used is that there exists a temperature dependence on the forward voltage and current when it is conducting. The 'On' state voltage drop  $V_F$  is one of the causes for diode losses and results

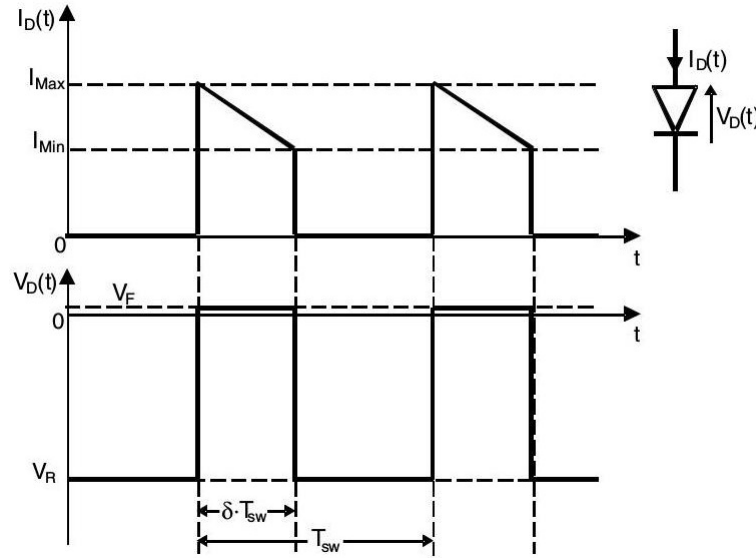


Figure 4-3: Diode current waveform [2]

in power losses and junction temperature increases [2]. Estimating them accurately holds the key to design circuits. The following terms are necessary for the calculation of diode On state losses.

- $f_{sw}$  – Switching frequency, in our case 150kHz for CCM
- $T_{sw}$  – Switching period, the reciprocal of switching frequency
- $D$  – Duty Cycle
- $I_{max}$  or  $I_{peak}$  – Peak current value in forward bias
- $I_{min}$  – Minimum current value in forward bias
- $V_f$  – Forward voltage

The procedure for calculation will be as follows

- Average and RMS currents are calculated for a specific converter type and values of  $I_{f,av}$  and  $I_{f,rms}$  are used to obtain  $V_{t0}$  and  $R_d$  at two different junction temperatures. The values of  $\alpha_{Vt0}$  and  $\alpha_{rd}$  are obtained to obtain a dynamic equation of dynamic resistance and forward voltage dependence on junction temperature.

- Diode forward characteristics modelling -  
At specific junction temperatures  $V_{t0}$  and  $R_d$  are obtained. Later, thermal co-efficient  $\alpha_{Vt0}$  and  $\alpha_{rd}$  are obtained for a specific diode.
- Losses are calculated

#### 4-3-1 Modelling forward characteristics

Current versus Forward voltage waveforms for temperatures  $T_{ref1} = 25^\circ\text{C}$  and  $T_{ref2} = 150^\circ\text{C}$  are obtained for  $I_{max}$  and  $I_{min}$  respectively.  $V_{t0}$  and  $R_d$  are calculated for  $T_{ref1} = 25^\circ\text{C}$  and  $T_{ref2} = 150^\circ\text{C}$  from the data-sheet using the forward voltage versus current characteristics. Later,  $\alpha_{VT0}$  and  $\alpha_{RD}$  are calculated as follows

$$\alpha_{Vt0} = \frac{V_{t0}(T_{ref2}) - V_{t0}(T_{ref1})}{T_{ref2} - T_{ref1}} \quad (4-15)$$

$$\alpha_{rd} = \frac{R_d(T_{ref2}) - R_d(T_{ref1})}{T_{ref2} - T_{ref1}} \quad (4-16)$$

N.B.  $\alpha_{Vt0}$  is always less than zero and  $\alpha_{rd}$  is greater than zero for all diodes.

These are thermal coefficients calculated from two reference temperature data.

A junction temperature  $T_j$  is considered,  $V_F(I_F, T_j)$ ,  $V_{t0}$  and  $R_d$  are obtained for the same by using the following equations

$$V_F(I_F, T_j) = V_F(I_F, T_{jref1}) + (\alpha_{Vt0} + \alpha_{rd} I_F)(T_j - T_{jref1}) \quad (4-17)$$

$$V_{t0}(T_j) = V_{t0}(T_{jref1}) + \alpha_{Vt0}(T_j - T_{jref1}) \quad (4-18)$$

$$R_d(T_j) = R_d(T_{jref1}) + \alpha_{rd}(T_j - T_{jref1}) \quad (4-19)$$

The final conduction loss is given by

$$P_{Cond}(T_j) = V_{t0}(T_j)I_{F(av)} + R_d(T_j)I_{F(rms)}^2 \quad (4-20)$$

#### 4-3-2 Modelling recovery characteristics

Junction temperature ( $T_j$ ) and reverse voltage ( $V_R$ ) are used to calculate the reverse losses. In a Schottky diode, the reverse losses occur due to the reverse bias applied to the diode and the leakage current ( $I_R$ ), as a consequence. The leakage current ( $I_R$ ) exponentially increases as the junction temperature increases.

To calculate leakage current, the following steps are followed.

'c', the thermal coefficient is used as a parameter that is necessary to find out the relationship between leakage current ( $I_R$ ) and the junction temperature. It is given by

$$c = \frac{1}{T_{j,ref2} - T_{j,ref1}} \log\left(\frac{I_R(V_R, T_{j,ref2})}{I_R(V_R, T_{j,ref1})}\right) \quad (4-21)$$

For the device we are using,  $T_{j,ref1} = 25$  and  $T_{j,ref2} = 125$ .

Now, the value of leakage current is given by

$$I_R(V_R, T_j) = I_R(V_R, T_{ref})e^{c(T_j - T_{j,ref})} \quad (4-22)$$

Where,  $V_R$  = Reverse voltage across the diode.

Hence, Power Loss due to reverse conduction is given by

$$P_{Rev,T_j} = (1 - D)V_R I_R(V_R, T_{ref})e^{c(T_j - T_{j,ref})} \quad (4-23)$$

## 4-4 MOSFET losses

Higher the switching frequency, higher the number of changes from On to Off state and vice versa implying that switching losses are proportional to operating frequency. They can be categorised into

- Conduction Losses
- Switching Losses

Conduction loss is the product of current and voltage in a MOSFET or a Schottky diode in the state of conduction. It depends upon the On time of the device and hence becomes dependent on the duty cycle,  $t_{on}f_{sw}$ .

Switching losses occur when there exists a switching transition in a MOSFET between ON and OFF states. Number of transitions per unit time is a good measure of the switching losses and hence they are judged to be dependent on the frequency  $f_{sw}$ .

Gate drive losses occur due to the conduction loss in the MOSFET driver output to the gate-source terminal of the high side switches during the bucking operation.

In calculation of switching losses, we can divide the section into turn on and off transitions and then calculate the  $E_{on,dissipated}$  and  $E_{off,dissipated}$  losses respectively.

In this section, an analytical model is presented for such a calculation by means of simplification of the original MOSFET model and explanation is given as to why some assumptions omit a few parameters. Ideally, a MOSFET has the following properties.

- Zero On state resistance -  $R_{ds,on}$
- Blocking drain to source voltage entirely without a +ve bias from gate to source

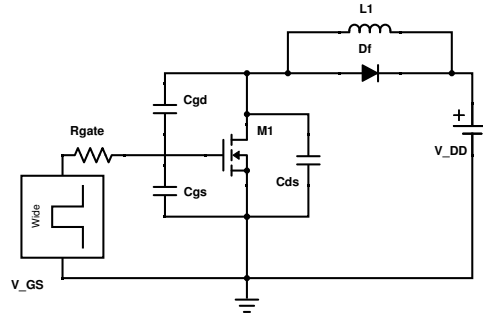
In reality, these properties do not exist and hence to simplify the loss models, the following assumptions are made for calculating the switching losses in both BCM and CCM Modes.

- Inductor current  $I_L$  remains constant during the switching process
- The free-wheeling diode  $D_f$  is ideal, i.e. junction capacitance and forward voltage drop are negligible
- Gate driver  $V_{g,driver}$  is ideal and a step voltage whose ON-state  $V_{GS_{ON}}$  and zero otherwise.
- Parasitic inductance is negligible in the switching devices

#### 4-4-1 Models for analysis

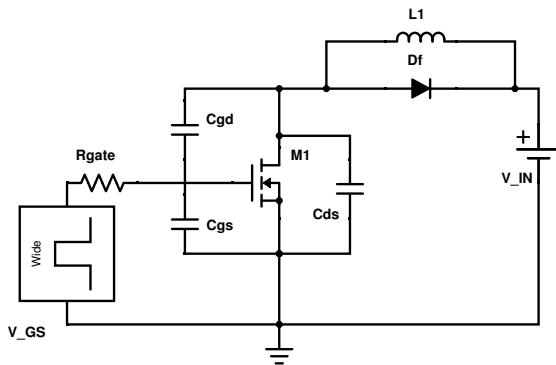
The general model used for analysing the switching transitions and then using the data from transitions to calculate losses is as shown in figure 4-4. References [3] and [39] are used to model the MOSFET devices for losses in this section of the report. Since the condition is considered to be that of a clamped inductive load, inductance  $L_1$  maintains a nearly constant load current. The MOSFET switching times and the load inductor current remain unchanged too. Only the switching current would commute from the MOSFET to the freewheeling diode  $D_f$  during MOSFET turn-off and vice-versa during turn-on.

This model can be adapted in both buck and boost modes with variations as follows.

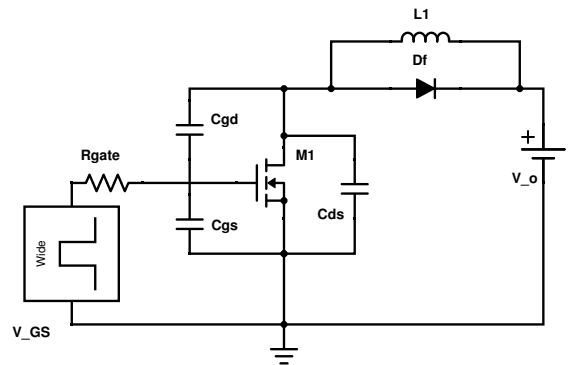


**Figure 4-4:** Switching loss model

- In case of a buck mode, the voltage source is  $V_{DD} = V_{in}$  and inductor current  $I_{L1} = I_o$  as shown in figure 4-5a.
- In case of boost mode, the voltage source is  $V_{DD} = V_{out}$  and inductor current value is  $I_{L1} = I_{in}$  as shown in figure 4-5b.



**(a)** Model for Buck



**(b)** Model for Boost

**Figure 4-5:** Switching loss models for Buck and Boost

### 4-4-2 Switching transitions in CCM

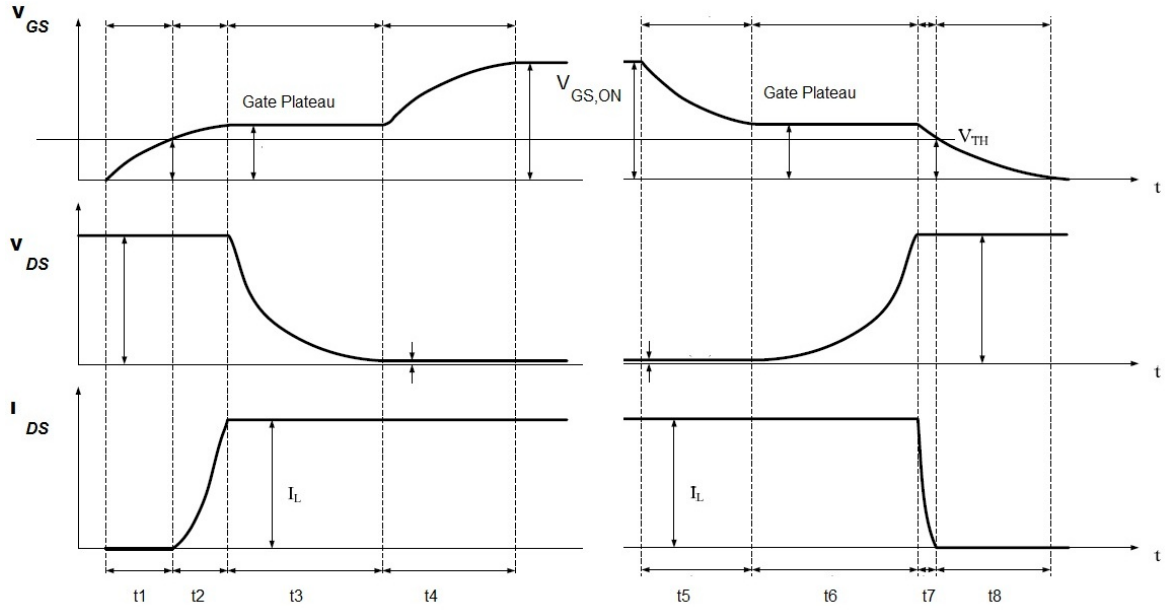
The model used in figure 4-4 is a general model which can be used to calculate the switching losses. Figure 4-6 shows switching transitions that will be discussed in the subsequent sections.

#### Turn on transition

- Turn on delay time -  $t_{d,on} - t_1$   
Upon increasing the gate drive voltage  $V_{GS}$  from zero to its value, parasitic capacitance  $C_{iss}$  of the MOSFET charges and there is an increase in the gate-source voltage  $V_{GS}$ . The MOSFET turns on when  $V_{GS}$  reaches threshold voltage of  $V_{TH}$ .  $V_{GS}$  reaches  $V_{TH}$  at the end of  $t_1$ .
- Current rise period -  $t_{ir} - t_2$   
In this transition, a part of the load current  $I_L$  is transferred from the free-wheeling diode to the MOSFET channel. With the increase in  $V_{GS}$ , the growth of current in the MOSFET increases as the channel resistance decreases although the drain-source terminals continue to block  $V_{DD}$  until the diode is in conduction and by the end of this transition the load current flows entirely through the MOSFET.
- Voltage fall period -  $t_{vf} - t_3$   
In this transition, the value of  $V_{GS} = V_{plateau}$ , which is an almost constant value. This is because the MOSFET is in the saturation region and  $I_{DS} = I_L$ . The gate current discharges  $C_{GD}$ , the Miller capacitance and when  $V_{DS}$  decreases to the rated on-state voltage of the device given by  $R_{ds,on}I_L$ .
- Gate voltage rise period -  $t_{gr} - t_4$   
By the end of  $t_3$ , the turn on process is finished. To enable low channel resistance,  $V_{GS,ON}$  increases to a higher value than  $V_{plateau}$  subsequently to gate driver voltage level that is supplied.

#### Turn off transition

- Turn off delay time -  $t_{d,off} - t_5$   
The gate to source voltage  $V_{GS}$  decreases  $V_{plateau}$  as the gate driver steps down to zero. The drain to source voltage  $V_{DS}$  increases slightly as the channel resistance goes up.
- Voltage rise period -  $t_{vr} - t_6$   
The MOSFET enters saturation as  $V_{DS}$  equals  $V_{DD}$  and current through it is maintained at load current  $I_L$  and  $V_{GS}$  will remain at  $V_{plateau}$ .
- Current fall period -  $t_{if} - t_7$   
The load current  $I_L$  shifts from the MOSFET to the free-wheeling diode  $D_f$  as a result of which  $V_{DS}$  is clamped to the  $V_{DD}$ .  $C_{iss}$  continues getting discharged until the gate voltage reaches the threshold voltage.
- Gate voltage fall period -  $t_{gf} - t_8$   
Although the turn-off of the MOSFET happens at the end of  $t_7$ , the charge stored in  $C_{iss}$  discharges gradually at the until the end of  $t_8$  when  $V_{GS}$  attains a zero value



**Figure 4-6:** Switching transitions in CCM

### Table of transitions in CCM

The losses can be split into turn-on and turn-off losses and calculations carried out for time instants  $t_2$  and  $t_3$  for turn on losses and  $t_6$  and  $t_7$  for turn off losses.

**Table 4-1:** Switching losses in CCM

	$V_{DS}$	$I_{DS}$	t	Phase
$t_1$	$V_{DD}$	0	$R_g C_{iss} \log(\frac{V_{gs,ON}}{V_{gs,ON} - V_{th}})$	Turn-on delay
$t_2$	$V_{DD}$	$g_{fs}(V_{gs} - V_{th})$	$R_g C_{iss} \log(\frac{V_{gs,ON} - V_{th}}{V_{gs,ON} - V_{plateau}})$	Current rise period
$t_3$	$\int_{t_3}^{t_4} (\frac{V_{gs,ON} - V_{plateau}}{R_g C_{gd}}) dt$	$I_L$	$\log(\frac{Q_{gd} R_g}{V_{gs,ON} - V_{plateau}})$	Voltage fall period
$t_4$	$R_{ds,on} I_L$	$I_L$	-	$V_{GS}$ rise period
$t_5$	$R_{ds,on} I_L$	$I_L$	$R_g C_{iss} \log(\frac{V_{gs,ON}}{V_{plateau}})$	Turn off delay
$t_6$	$V_{DD}$	$I_L$	$(\frac{Q_{gd} R_g}{V_{plateau}})$	Voltage rise period
$t_7$	$V_{DD}$	$g_{fs}[V_{gs} - V_{th}]$	$R_g C_{iss} \log(\frac{V_{plateau}}{V_{threshold}})$	Current fall period
$t_8$	$V_{DD}$	0	-	$V_{GS}$ fall period

### 4-4-3 Switching loss calculations in CCM

#### Turn on loss calculations

During the turn-on switching transitions mentioned in the section 4-4-2, the losses are apparent in the time periods  $t_2$  and  $t_3$ .



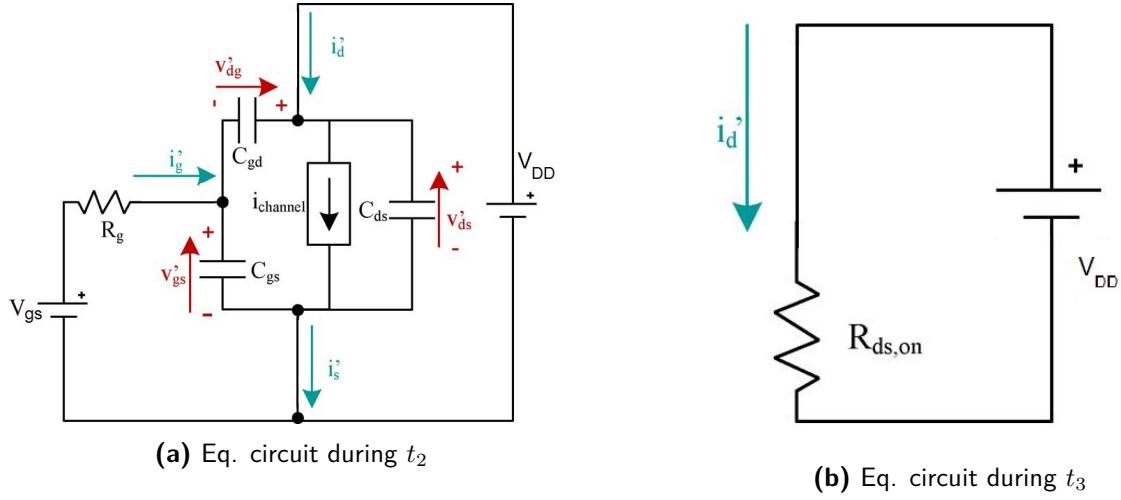


Figure 4-7: Turn on loss equivalent circuits [3]

- $t_2$  - Current rise period

During the start of this transition, the parasitic capacitances are charged as given by figure 4-7a and the  $V_{GS}$  reaches  $V_{threshold}$ . The energy in the capacitances remain the same on the course of the transition and this energy will be dissipated very less or probably not dissipated at all as the channel current can be neglected [3]. Hence, if  $P_2$  is the power loss during this transition,

$$P_2 \approx 0 \quad (4-24)$$

- $t_3$  - Voltage fall period

During transition  $t_3$ , the diode current  $I_f$  falls to zero and blocks voltage implying that  $V_{DS}$  will start decreasing rapidly until it reaches the boundary voltage  $V_{miller}$ . In this instant, the MOSFET starts behaving like a resistor and drain current is proportional to the input voltage source [39]. The equivalent circuit during this transition is given by figure 4-7b

In this stage, the drain current stabilises and this sub-stage exists for a very short period of time. The power loss during this stage can be given by equation 4-25.

$$P_3 = \int_{t_2}^{t_3} I_{DS}(t) V_{DS}(t) dt \quad (4-25)$$

- $t_4$

In this stage, the current through the drain-source channel reaches the value of  $I_{DD}$  and the reverse recovery period begins. The free-wheeling diode is unable to block the reverse voltage until a small magnitude of the charge is removed from the junction resulting in the some losses denoted by the equation 4-26.

$$P_4 = (V_{in} Q_{rr} - \frac{1}{2} C_D V_{DD}^2) f_{sw} \quad (4-26)$$

### Turn off losses

Turn off losses during switching transitions happen during time periods  $t_6$  and  $t_7$ .

- $t_6$  - Voltage rise period

In this stage, the MOSFET channel current suddenly comes down causing an excess current  $I_{DD} - i_{channel}$  to charge the MOSFET capacitances [39]. At the end of the period, drain to source voltage reaches the value of  $V_{DD}$ . The power losses in this period are calculated by equation 4-27.

$$P_6 = \int_{t_5}^{t_6} V_{DS}(t) I_{channel-off} dt \quad (4-27)$$

where

$$I_{channel-off} = I_{off} - I_{DS} - I_{DG}$$

- $t_7$  - Current fall period

In this stage, the  $V_{DS}$  has reached  $V_{DD}$  and increases while the freewheeling diode becomes forward biased. If  $V_{GS}$  is assumed constant, the  $V_{DS}$  continues to increase. This stage ends with  $I_{DS}$  reaching the channel current  $i_{channel}$  and  $V_{DS}$  reaching its peak voltage. [39]

$$P_7 = \int_{t_6}^{t_7} V_{DS}(t) I_{DD}(t) dt \quad (4-28)$$

#### 4-4-4 Switching loss calculations in BCM

As discussed in the previous chapters, in BCM the new switching period will begin when inductor current  $I_L$  hits zero. In BCM, zero current switching (ZCS) takes place enabling less losses in the switching devices which is an advantage for higher frequency operation. The turn off process is similar to that in CCM.

#### Difference in turn-on losses

ZCS ensures that the only the turn on transient losses dissipated in the MOSFET occurs due to the discharge of the parasitic capacitances. Additionally, soft switching of the diode (freewheeling diode  $D_f$ ) takes place in BCM ensuring no reverse recovery current, as a consequence of which, no reverse recovery losses occur [40] [41]. The turn-on losses can be calculated using equation 4-29

$$P_{on} = \left( \frac{1}{2} (C_{ds} + C_{gd}) V_{sw}^2 \right) f_{sw} \quad (4-29)$$

N.B. This model is valid in the analysis of switching losses involving CCM (hard-switched) and BCM only. It cannot be applied to BCM with valley switching. In case of valley switching, the capacitances have to be explicitly stated when the loss equations are derived.

## 4-5 Inductor losses

The inductor is an integral passive component that has to be customized for a specific switching supply operation as it affects the selection and cost of all other associated power components. This section examines the issues and solutions to design the inductor for our application. It involves the determination of inductance values, optimization of the cores and windings for the operation and evaluation of design under BCM and CCM as they have different loss profiles.

In the case of inductor selection, there are many off the shelf inductors available on the market for usage. However, It might not be optimum for our working conditions. In the course of the thesis, customized inductor values are preferable for the following reasons,

- The "on the sheet" ratings are usually mildly overstated as compared the actual capability of the device in our application
- The freedom to make improvements is generally not possible upon changing set parameters
- Off-the-shelf components are optimized usually for the cost. They are utilized in platforms for applications involving mass production and might rarely be an optimized solution for our application

Inductor design for the application for all the five constituent topologies is discussed in detail in the appendix. The subsequent sections will discuss the calculation of losses in BCM and CCM modes of operation.

### 4-5-1 Core loss calculations

#### CCM

In case of CCM, frequency remains constant. For a material like 3C95, core Loss in  $\frac{kW}{m^3}$  [42]

$$P_{core} = C_m f_{sw}^x B^y (C_{t0} - C_{t1}T + C_{t2}T^2) \quad (4-30)$$

where

$C_{t0}$ ,  $C_{t1}$  and  $C_{t2}$  are the curve fit parameters

$x = 1.045$

$y = 2.44$

$C_m = 92.1664$

$C_{t2} = 4.6 \times 10^{-5}$

$C_{t1} = 7.9 \times 10^{-3}$

$C_{t0} = 1.33236$

$f_{sw}$  = specified switching frequency due to CCM

## BCM

In this case, frequency varies according to changes in input voltage. For a material like 3C95, core Loss in  $\frac{kW}{m^3}$

$$P_{core} = C_m f_{sw,BCM}^x B^y (C_{t0} - C_{t1}T + C_{t2}T^2) \quad (4-31)$$

where

$C_{t0}$ ,  $C_{t1}$  and  $C_{t2}$  are the curve fit parameters

$x = 1.045$

$y = 2.44$

$C_m = 92.1664$

$C_{t2} = 4.6 \times 10^{-5}$

$C_{t1} = 7.9 \times 10^{-3}$

$C_{t0} = 1.33236$

$f_{sw,BCM}$  = variable switching frequency due to BCM

N.B. - Values of x, y,  $C_m$ ,  $C_{t2}$ ,  $C_{t1}$  and  $C_{t0}$  are found in [42]

## 4-5-2 Winding loss calculation for CCM

### CCM case

In a CCM based design, the current waveform is triangular with a DC offset meaning that peak and RMS values are calculated as below,

$$I_{L,PEAK} = I_{L,AVG} + \frac{\Delta I_{L,PEAK-PEAK}}{2} \quad (4-32)$$

$$I_{L,RMS} = I_{L,AVG} \sqrt{1 + \frac{1}{3} \left( \frac{\Delta I_{L,PEAK-PEAK}}{2I_{L,AVG}} \right)^2} \quad (4-33)$$

Resistivity of Copper at operating temperature  $t_{op}$  is given by

$$\rho_{Cu,t} = \rho_{Cu,25} \left( 1 + \frac{0.393(t_{op} - 25)}{100} \right) \quad (4-34)$$

$$R_{DC} = DCR = \left( \frac{(\rho_{Cu-wire} l_{total})}{a_w n_s^2} \right) t_{co-eff} \quad (4-35)$$

where

$t_{co-eff}$  is the temperature co-efficient given by

$$t_{co-eff} = 1 + \frac{(t_{co-eff@25^\circ C})(t_{operating})}{100} \quad (4-36)$$

Where

$t_{operating}$  = operating temperature

$l_{total} = (\text{mean length per turn})(\text{number of layers})n_s$

Skin Depth  $\delta$  is calculated as follows

$$\delta = \sqrt{\frac{\rho_{Cu,t}}{\pi\mu_0\mu_r f_{sw}}} \quad (4-37)$$

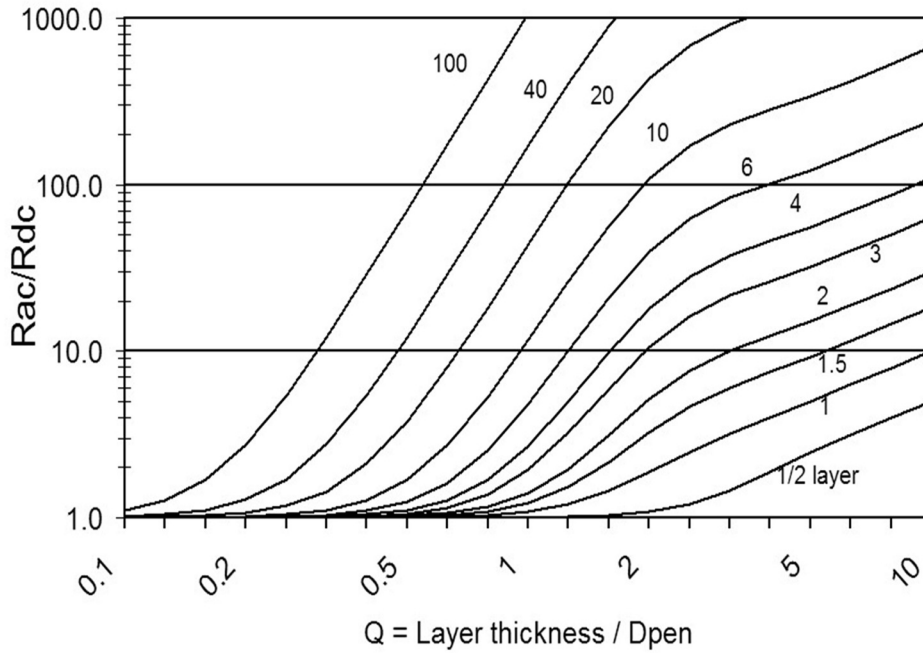
Dowell's curve is used to determine the AC resistance of the windings [4] as shown in figure 4-8. In the Dowell's curve, The Q-factor on the X-axis is given by

$$Q_{factor} = \frac{t_{Cu}}{\delta} \quad (4-38)$$

where

$t_{Cu}$  = thickness of copper per winding On the Y-axis, the ratio of  $R_{AC}$  and  $R_{DC}$  which will be co-related to the  $Q_{factor}$  and the number of layers. Let us call this ratio which is the multiplication factor as  $k_{multi,factor}$ .

The windings Losses due to ripple component corresponds to the AC losses which are given



**Figure 4-8:** Dowell's Curve [4]

by

$$P_{L,WIND,AC} = \Delta I_{L,RMS}^2 R_{AC} \quad (4-39)$$

Losses due to the "offset" DC component is given by

$$P_{L,WIND,DC} = I_{L,AVG}^2 R_{DC} \quad (4-40)$$

### Winding loss calculation for BCM

Contrary to CCM, in case of BCM, this changes as the current waveform is a triangular one with zero DC offset. The peak to peak ripple value of the inductor current becomes equal to

the peak value of current. A Litz wire based construction is employed for BCM to optimize the topology for better performance to compare with CCM. The currents for loss calculations are

$$I_{L,PEAK} = \Delta I_{L,PEAK-PEAK} \quad (4-41)$$

$$I_{L,AVG} = \frac{I_{L,PEAK}}{2} \quad (4-42)$$

$$I_{L,RMS} = \frac{I_{L,PEAK}}{\sqrt{3}} \quad (4-43)$$

$R_{DC}$  is calculated the same way as in the case of CCM. However, this value is significant to determine the parameter  $R_{AC}$  in the Dowell's curve. The winding losses are mostly due to ripple component  $\Delta I_{L,RMS}$  and the AC losses are given by

$$P_{L,WIND,AC} = I_{L,RMS}^2 R_{AC} \quad (4-44)$$

### Litz wire

In case of BCM, with the operating frequency at a higher value, it is preferable to use Litz windings to reduce losses. The design of a Litz wire is dependent on the operating frequency and RMS current required for his application. The main advantage Litz conductor offers is reduction of AC losses in the winding. The operating frequency has a say on the skin depth of the individual winding. Hence, it also influences the authentic Litz construction and determines the individual wire gauge. In table 4-2 a measure of the ratio of AC to DC

**Table 4-2:** Litz wire reference table

Frequency	Recommended AWG	Nominal dia in $\mu m$	DC resistance in $\Omega / \mu m$ (Max)	Single strand $\frac{R_{AC}}{R_{DC}}$ " H "
60 Hz to 1 kHz	28 AWG	0.32	2.61	1.0000
1 kHz to 10 kHz	30 AWG	0.254	4.16	1.0000
10 kHz to 20 kHz	33 AWG	0.18034	8.33	1.0000
20 kHz to 50 kHz	36 AWG	0.127	17.00	1.0000
50 kHz to 100 kHz	38 AWG	0.1016	26.84	1.0000
100 kHz to 200 kHz	40 AWG	0.07874	45.36	1.0000
200 kHz to 350 kHz	42 AWG	0.0635	71	1.0000
350 kHz to 850 kHz	44 AWG	0.0508	113	1.0003
850 kHz to 1.4 MHz	46 AWG	0.04064	178.89	1.0003
1.4MHz to 2.8 MHz	48 AWG	0.03048	286	1.0003

resistance for a solid round wire (H) in terms of a value(X) is given. An individual wire gauge is selected now (In our case, AWG 40) and the following calculations are done. Eddy current basis factor 'G' is given by

$$G = \frac{D_i \sqrt{F}}{10.44} \quad (4-45)$$

Where,

$D_i$  is Diameter of the individual strand (in mm)

$F$  = Switching frequency in Hertz

Number of strands is given by

$$N_{strands} = \frac{D_O}{D_i} \quad (4-46)$$

Where,

$D_i$  = Diameter of the individual strand (in mm)

$D_O$  = Diameter of the finished cable (in mm)

Using the table 4-3, we decide on the factor K.

$N$	3	9	27	$\infty$
$K$	1.55	1.84	1.92	2

**Table 4-3:** Table for correspondence of K

Calculation of DC resistance of the winding

$$R_{DC} = \frac{R_S(1.02)^{N_B}(1.03)^{N_C}}{N_S} \quad (4-47)$$

Where,

$R_S$  = D.C. resistance of the individual strands from table 4-2

$N_B$  = Number of bunching operations

$N_C$  = Number of cabling operations

$N_S$  = Number of individual strands

The ratio of A.C. to D.C. resistance is given by

$$\frac{R_{AC}}{R_{DC}} = H + K \left( \frac{N_S D_i}{D_O} \right)^2 G \quad (4-48)$$

Where,

$H$  = Resistance ratio of individual strands when isolated (from table 4-2)

$G$  = Eddy-current basis factor

$F$  = Frequency in Hertz

$N_S$  = Number of strands in the cable

$D_i$  = Diameter of the individual strands over the copper in inches

$D_O$  = Diameter of the finished cable over the strands in inches

$K$  = Constant depending on N, table 4-3

### Significance of using Litz over Cu-windings

Evidently, using normal copper windings with resistive coatings is straight forward. But when the high-frequency inductor ripple is observed, Litz wire will enable less loss characteristics. Litz winding based inductor has better high-frequency characteristics reducing eddy current losses. In case of size reduction, for the same outer dimensions, Litz occupies a fraction of the total cross section occupied by copper windings.

**Adapting the Litz wire**

As explained, Litz wire selection depends on the operating frequency and RMS current required for his application. The operating frequency  $f_{sw}$  determines the skin depth '  $\delta$  ' of the individual winding and RMS current affects the winding losses. So it has to be selected in case ripple content in the inductor windings are higher. Litz conductor offers a reduced AC loss profile in the winding.

In case of CCM, it is observed that copper windings can effectively be used as the ripple content in the windings of the inductor will be far less than that in BCM. It is beneficial not to use Litz wires in this case as skin effect is not as significant in comparison with BCM.



## 4-6 Component selection

A proper selection of components plays a vital role in the performance with respect to efficiency and thermal characteristics. In this section, there is a discussion on the procedure followed to select the components for design, the calculations behind their selection and significance.

## 4-7 Inductor selection

### 4-7-1 Core selection

Ferrite magnetic materials are manufactured with a mix of oxides of iron and other elements and possess a crystalline molecular structure. The material of the core must withstand the temperature rise and provide less lossy performance at the operating frequency and not saturate. To select the core, a value of maximum flux density  $B_{max}$  in unit 'milli Tesla' is obtained through the graphs. This is the maximum value of AC flux density for a core. This is to ensure the design doesn't drive the core into saturation upon worst case operation due to inductor ripple.

Optimal core material selection for building an inductor coil for power-specific applications is very important. In the target application, core loss parameters and saturation flux density at operating frequency are the main drivers for selection.

For operating frequencies such as ours, soft magnetic materials are predominantly used due to their low core loss. As these losses are a function of switching frequency and the total magnetic flux swing, the selection also depends upon the performance of the core under the circumstances and modes of operation. In our application, we have used Ferroxcube 3C95.

At a frequency of 150 kHz, this core material was deemed fit as for a higher range of temperature, it has a flat curve for Power loss density vs. temperature curve. Additionally, its core loss at room temperature where natural convection is enabled is very less.

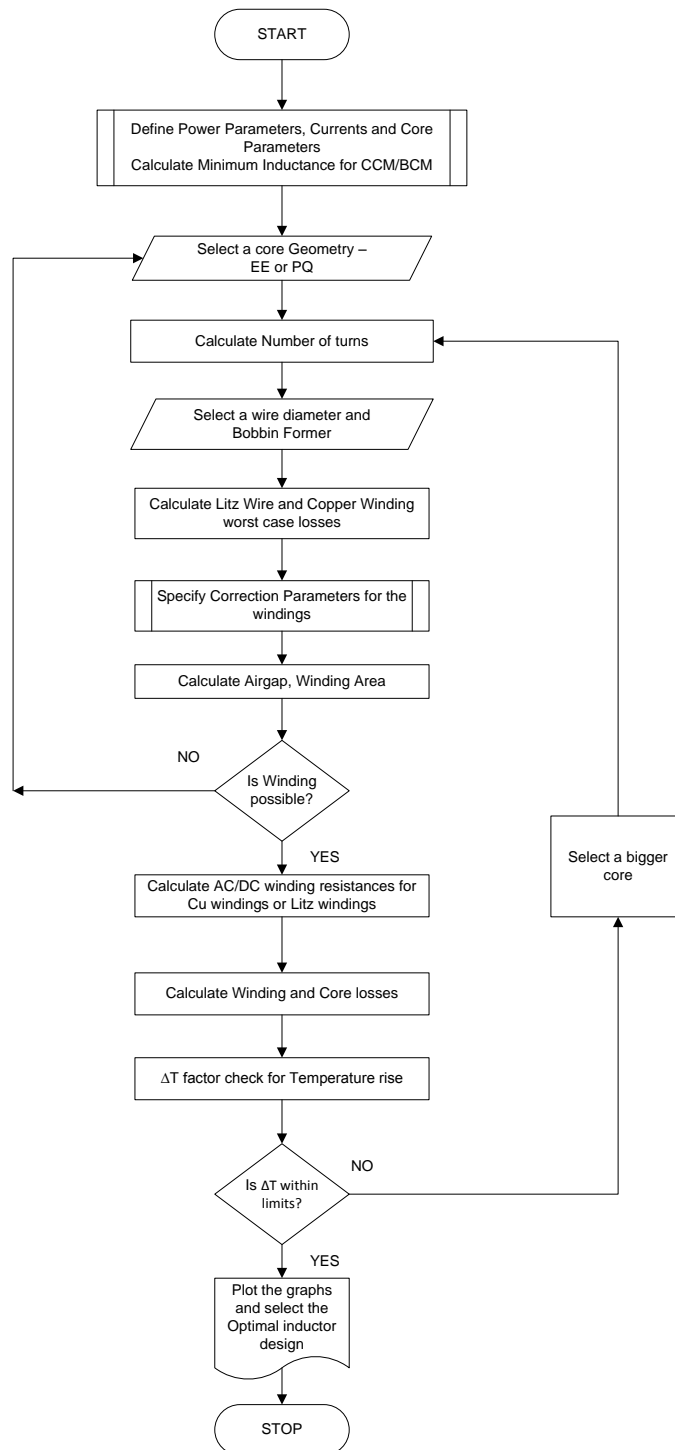
### 4-7-2 Design of the inductor

The methodical design of the inductor is discussed in the chapter of magnetics in the appendix. In this section, a flowchart describing the procedure is presented in figure 4-9. We select PQ and EE cores for the design. We initially pick the smallest core and then proceed to larger cores.

### 4-7-3 Optimising the design

To optimize the selection of the core, the following steps are followed.

An algorithm to equate the analytical loss model of an inductor is developed for both modes of operation (BCM and CCM) of the  $B^2R$  converter i.e. buck, boost and DET to observe for theoretical losses.



**Figure 4-9:** Flowchart for Inductor Design

#### **4-7-4 Windings - Litz wires**

The design of a Litz wire is dependent on the operating frequency and RMS current required for his application. The main advantage Litz conductor offers is reduced AC losses in the winding. The operating frequency has a say on the 'Skin Depth' of the individual winding. Hence, it also influences the Litz construction and determines the individual wire gauge.

#### **4-7-5 Conduction mode based design**

In case of BCM, the switch is operated in such a way that the inductor current hits zero in every cycle.

Whereas in case of CCM, the current through the inductor is ensured to be never falling to a zero value. The inductor design is done keeping in mind that even under worst case situation, the current never falls below zero.

The value of inductance used will be much higher in case of CCM.

## 4-8 Capacitor selection

Capacitors function as elements for energy storage in SMPS. The parasitics in a real capacitor can ruin the choices that a designer must consider. In power electronic topologies, capacitors are to be designed for the following conditions

- Non-sinusoidal Currents
- High percentage of harmonics
- Pulses or current waveforms having a high  $\frac{di}{dt}$
- Broad range operating frequencies

### 4-8-1 Significance of selecting transfer capacitance

Transfer capacitor is preferably a film capacitor to avoid losses and ensure the polarity-less property of it can be used for two inductor topologies. The main advantage of using a plastic film capacitor is it can operate well under conditions of high temperature, have smaller tolerances, a very long service life and high reliability.

The following factors are essential for the pre-selection of capacitors for the topology

- Switching frequency
- Input voltage range
- Output voltage ripple
- Output current ripple

Capacitor selection in our design relied upon

- RMS current of the capacitor
- Self-heating which is directly proportional to RMS current

The following measures can be considered as good design practices to ensure that capacitor related issue occurrence can be minimised

- Maintaining the operating temperature and ripple current applied to be within specified limits.
- Ensuring reverse voltage is not applied to the input and output capacitors. A transfer capacitor is a film type meaning that it is capable of handling reverse voltages.

### 4-8-2 Ripple ratings of capacitors

Losses in the capacitor can increase the temperature in the capacitor which is dependent upon the frequency and type of waveform. Rated ripple current parameter is the maximum value of RMS current that can pass through it during the useful life under specified conditions of frequency.

It should be noted that the actual ripple current is within the limits to ensure higher useful life for a specific rating in lifetime nomogram as provided by the manufacturer.

The input capacitor rating is fixed at 50V as the variance of the input voltage is from 30V up to 45V. The output capacitance is rated at 50V as the output voltage does not cross 40V under normal working conditions of the converter.

## 4-9 Selection of active devices

### 4-9-1 Initial parameters for diode and switch selection

Selection and operation of switches (active devices) are governed by the series of ratings that will define the operating regions. These regions can determine their ability to block voltages and current carrying capability. Some sample ratings of the devices can be

- Limits on peak, average and RMS currents
- Peak forward and reverse voltages
- Rate of change of current and voltages
- Junction temperature

Throughout the course of design, the devices are selected such that worst case scenario under working conditions are considered. The MOSFETs used for the purpose are selected to ensure that there lies an optimized loss to breakdown voltage characteristics at the operating frequency. Similarly, the diodes used have fast recovery mechanism that will ensure less switching losses in the device.

Detailed description of these aspects follows in the coming sections

## 4-10 Diode selection

Diodes that are used for the topologies described must have the following properties preferable.

- Lower forward voltage drop
- Fast reverse recovery characteristics

Limiting factor for selection of power diode technologies in most power electronic circuits are the above two factors. For power levels specified by our design, there are Schottky rectifiers for the specified voltage range can satisfy all such demands. Lower forward voltage drop ensures that the diodes have low rectification losses, hence the better efficiency.

### 4-10-1 Selection of diode technology

The selection of Schottky technology for the diode is hinged upon the following reasons

- Forward voltage,  $V_F$  for a Schottky is less as compared to a p-n junction diode. Lower the value of  $V_F$ , lower the power dissipation and, as a result, better efficiency.
- Forward current,  $I_F$  is lower than a p-n junction diode and  $V_R$  is lower than the p-n diode, for a similar size.

## 4-11 MOSFET selection

MOSFETs are the best known gated switching devices in switching mode power supplies. The selection of a MOSFET depends upon the application under consideration prior to initialising the process of evaluation. Rather than some specifications lauded by manufacturers, it is important to prioritise and scrutinise some specifications. MOSFETs used in DC-DC converter topologies are often designed for better current handling capability.

### 4-11-1 MOSFET selection parameters

Parameters which are vital for MOSFET selection are

- Drain to source breakdown voltage -  $BV_{DSS}$
- Gate charge -  $Q_{GD}$
- Gate driver resistance -  $R_g$
- On state resistance  $R_{ds,on}$
- Safe Operating Area

These parameters can provide with significant resolutions for selection and performance expectations from a MOSFET for an application. A piece-wise linear approximation of switching waveforms is done for MOSFETs using an analytical model. Data-sheet parameters are employed with MATLAB programs for predicting efficiencies by substituting in analytical models for conduction and switching losses calculations.

N.B. Theoretical loss calculations are different to practical switching losses due to ambient temperature changes, parasitics etc.

#### On state resistance

A MOSFET that is turned on behaves like a resistor. This value of resistance between the drain and the source terminals is  $R_{DS(ON)}$ . The power dissipation across the MOSFET during conduction period can be calculated as

$$P_{cond} = I_{DS}^2 R_{DS(ON)} \quad (4-49)$$

Due to its direct proportionality with respect to losses,  $R_{DS(ON)}$  will be significantly important parameter.

#### Reverse breakdown

The blocking capability of a MOSFET against breakdown is  $BV_{DSS}$ , the drain-source breakdown voltage. The devices selected should be capable of blocking reverse voltage to ensure that the devices are safe.

## Gate charge

Gate charge can be stated as one of the factors for switching losses. In the data-sheets, they are specified in nano Coulombs (nC). Gate charge relates to the energy required to charge/discharge MOSFET gate.

MOSFETs which have a lower gate charge characteristics will have a trade-off in such a way that they have slightly higher  $R_{DS(ON)}$  specs. In case of CCM, the switching losses depend upon  $Q_{GD}$  (miller charge - controls the voltage rising and falling time ( $t_{VR}$ )) and  $Q_{GS}$  (gate-source charge).  $Q_{GS}$  of the device is the proportional gate charge that exists when the MOSFET is in transition from threshold voltage until the gate plateau voltage. This controls the time for current rising in the MOSFET and period when it falls. In case of BCM, ZCS exists. This means that the values of  $Q_{GD}$  and  $Q_{GS}$  are not critical as seen in CCM.

## Capacitances - $C_{ds}$ $C_{gs}$ $C_{gd}$

In some data-sheets, the terms  $C_{GD}$ ,  $C_{GS}$  and  $C_{DS}$  are mentioned at specification values of  $V_{DD}$  and  $I_{DS}$ . Similarly, a few manufacturers coin  $C_{OSS}$ ,  $C_{ISS}$  and  $C_{RSS}$ .

To simplify this parameter, we use the conversion factor in terms of  $C_{GD}$ ,  $C_{GS}$  and  $C_{DS}$  to  $C_{OSS}$ ,  $C_{ISS}$  and  $C_{RSS}$ . as shown below.

$$C_{ISS} = C_{GS} + C_{GD} \quad (4-50)$$

$$C_{RSS} = C_{GD} \quad (4-51)$$

$$C_{OSS} = C_{DS} + C_{GD} \quad (4-52)$$

The input capacitance parameters directly affect the delay times associated with switching. 'Turn on delay' is the required time to charge the input capacitance of the device before  $I_{DS}$  can rise and 'Turn off delay' is the time to discharge the input capacitance after the switch off process.

$C_{GD}$  is the Gate to Drain capacitance which varies non-linearly with voltage. It is quintessentially the parameter to be considered as in the switching process it provides with a feedback loop w.r.t. both output and the input of a switch. It is christened 'Miller capacitance' sometimes as the overall dynamic input capacitance becomes larger than the addition of the static capacitances.

## Gate resistance

Series gate resistance ( $R_G$ ) is dependent on the gate to source voltage rating of the MOSFET. A discrete power MOSFET is often depicted (or modelled) as a lumped circuit consisting of parasitic capacitance and resistance of the active cell scaled for area, where the MOSFET internal gate resistance and internal capacitance determine the input impedance and switching speeds.



## 4-12 MOSFET drivers

The operation of the buck converter, regardless of two coil topologies (A, C, D, E) or single coil topology (B), needs a high side driver for the switching operation to be carried out. In case of boost operation, the source terminal is connected to the ground in case of topology A, B and C. In case of topology D and E, a high side driver would be necessary as well. This section deals with selection parameters that were considered for MOSFET drivers in the process.

### 4-12-1 High side and Low side drivers

A high side gate drive for the power MOSFET which is used as a high-side switch (the drain terminal is connected to a non-zero positive voltage point) which is driven in enhancement mode (maximum  $I_{DS}$  and low  $V_{DS}$ ) is selected by these parameters,

- Voltage  $V_{GS}$  to be maintained should be a value of at least 10V ranging to 15V greater than voltage supplied to the source terminal when in switching operation. This also implies that the gate voltage will be much higher than the rail voltage (at the source) meaning this value of voltage will evidently be the highest in the system.
- $V_{GS}$  must be controlled from the controller. Under normal circumstances, the ground reference is employed to measure this voltage.
- Power requirements of the high side gate driver should be within the limits of not disturbing overall efficiency or minimal loss imprint.

#### Buck switch driver for S1-B and S1-A

As mentioned in section 3-3, S1-B is supplied with PWM for switching. The high side driver for the purpose will be an IR2117 as shown in figure 4-10. IR2117 cannot supply a continuous

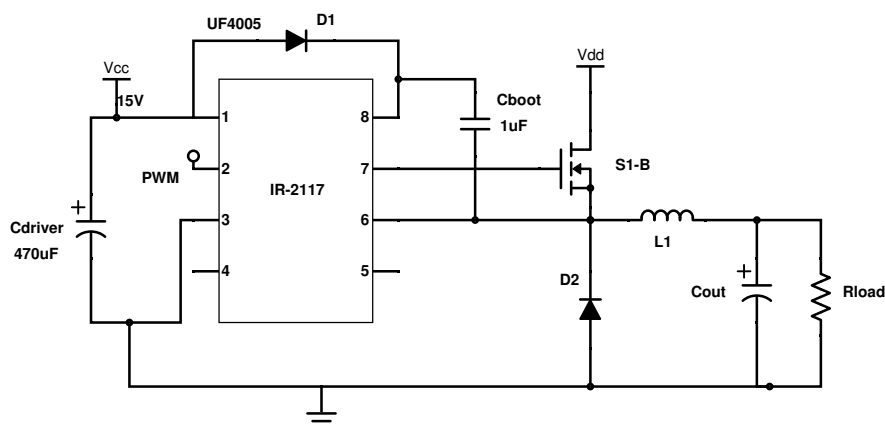
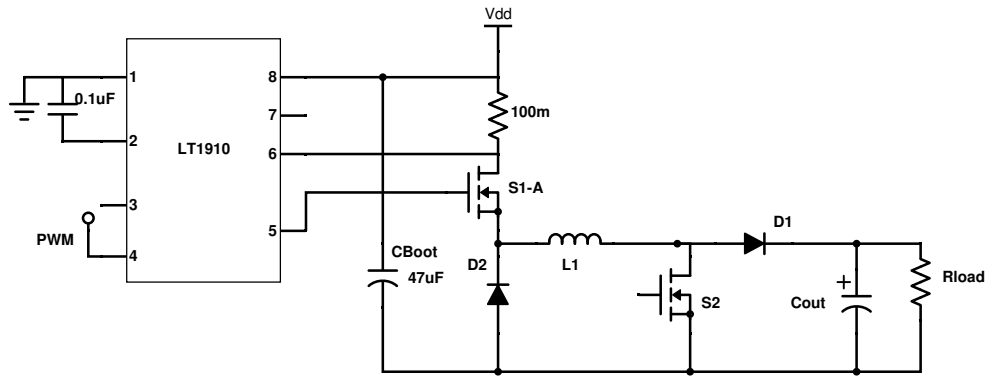


Figure 4-10: IR-2117 Schematic

DC supply to a gate. The switch S1-A is supplied by LT1910 which can be operated during



**Figure 4-11:** LT-1910 Schematic

boost operation as shown in figure 4-11.

In topologies D and E, an additional driver should be used to switch  $S_2$  as the source cannot be supplied with respect to ground.

## 4-13 Simulation results of analytical models

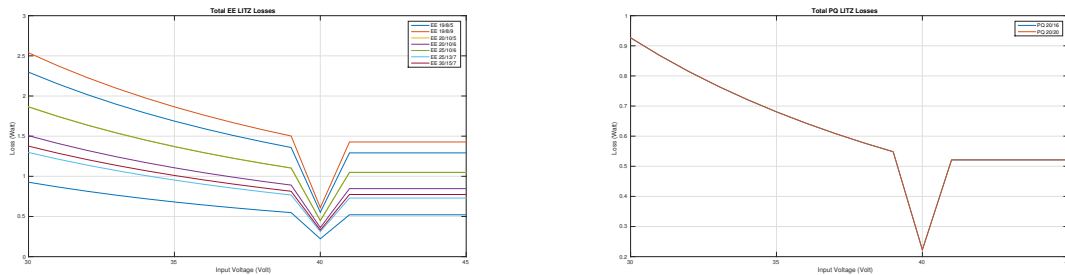
All the analytical models discussed for loss calculation are simulated using MATLAB and results are obtained for BCM and CCM for all the topologies under consideration.

### 4-13-1 Inductor losses

To carry out selection of the core, a number of EE cores and PQ cores are used to obtain results to ascertain the following parameters -

- Losses in the core
- Temperature rise due to losses
- Performance with Litz wires and normal copper windings
- Possibility of winding

As discussed in the previous chapters, Litz windings can be used in BCM and copper windings can be used in CCM. Considering topology B as reference, Figures 4-12 and 4-13 demonstrate the losses in BCM with Litz windings and copper windings respectively.



(a) BCM with Litz winding based inductor with EE Cores

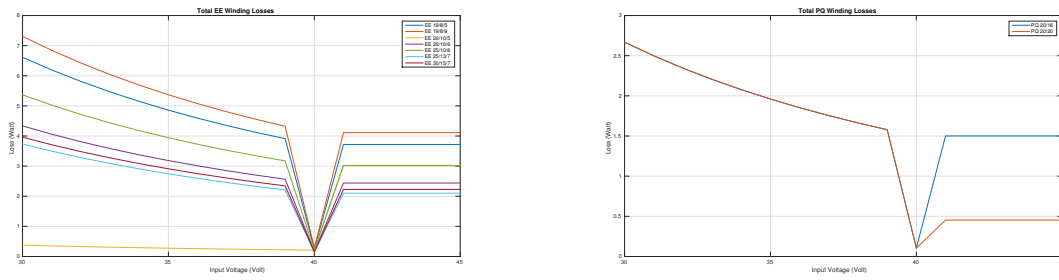
(b) BCM with Litz winding based inductor with PQ Cores

**Figure 4-12:** Litz winding based inductor in BCM

The losses are less for Litz windings evidently due to reduced skin effect. Due to lower magnitude of peak to peak ripple, the skin effect is less as a result of which, the inductors with Litz winding would be inferior w.r.t the losses.

One more significance of such a calculation is the estimation of temperature  $\Delta T$  rise due to power losses. The losses and temperature rise are related in direct proportionality.

N.B. All the cores are simulated and presented in this part of the report as seen in figures 4-13 and 4-12 to signify that selecting the core size can be optimized for a specific application rather than randomly choosing a larger core for a specific application. The optimisation in our case is done by using MATLAB programs to simulate losses at different input voltages for different sized PQ and EE cores.



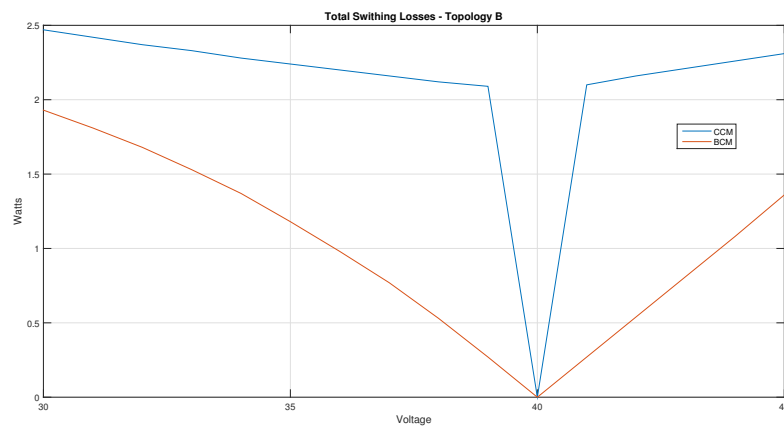
(a) BCM with Copper winding based inductor with EE Cores

(b) BCM with Copper winding based inductor with PQ Cores

**Figure 4-13:** Copper winding based inductor in BCM

### 4-13-2 Switching losses

In sections 4-4-3, we discussed the analytical model for calculation of switching losses. To assess if BCM has better loss profile as compared to CCM, Topology B is considered for comparison. The value of inductance  $L_1$  will be fixed at  $7.125\mu H$  for BCM and  $42.333\mu H$  for CCM. The results of losses during switch transitions is as shown in figure 4-14. Although the



**Figure 4-14:** Overall losses in both buck and boost regions in BCM and CCM

turn off losses can be considered the same, the turn-on losses in case of BCM are negligible values. Also, a sharp dip in losses is observed as the difference in input and output voltage becomes less. This is due to the fact that frequency of switching is variable in BCM and decreases as the difference becomes less. This is one of the reasons where BCM has a clear advantage over CCM.

Figures 4-15a and 4-15b provide us with an estimate of how the switching losses will be reduced in case of BCM and CCM. During switch on transitions while CCM has significant losses, by virtue of ZCS, BCM will have almost zero losses.

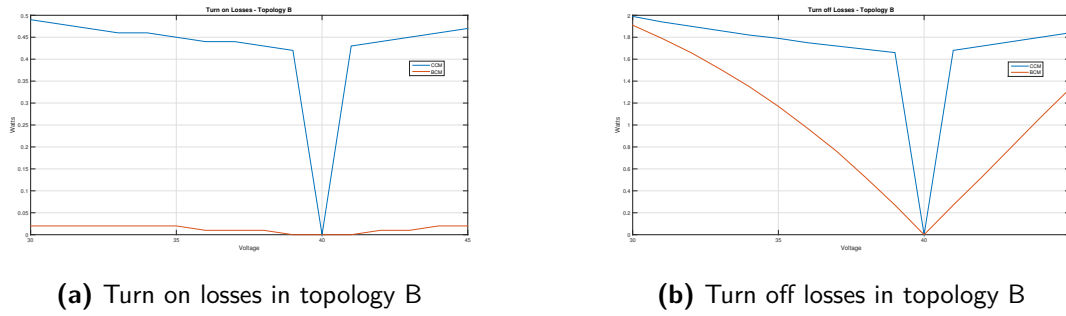


Figure 4-15: Switching loss breakdown

### 4-13-3 Overall efficiency

After calculating all the losses in the converter in each topology, efficiency is calculated as it is one of the primary aspects of design. For a fixed power output, the efficiency is given by

$$\eta = \frac{P_o}{P_{in}} \quad (4-53)$$

Where,

$$P_{in} = P_o + P_{losses}.$$

In case of CCM, the topologies have a higher value of inductance  $L_1$  to ensure continuous current. The switching frequency is  $150kHz$ . The efficiency plots of the topologies under CCM is as shown in the figure 4-16.

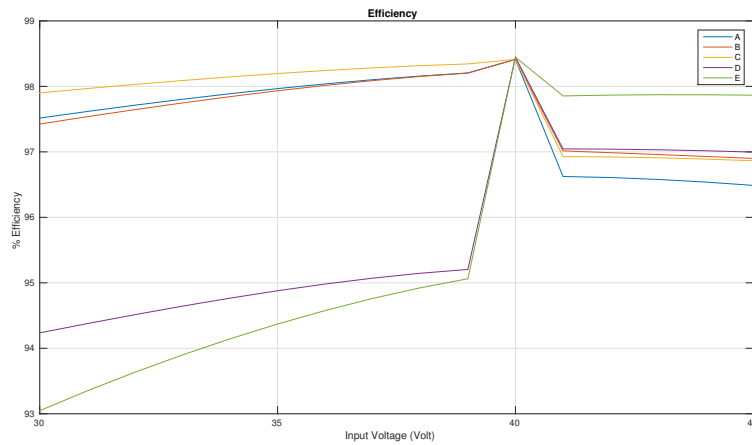


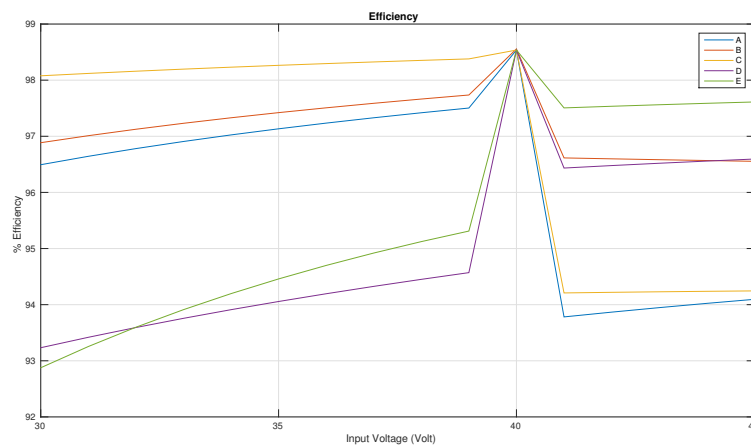
Figure 4-16: Efficiency of Topologies in CCM

In the figure 4-16 shown, the best possible efficiency in every converter is in Direct Energy Transfer (a.k.a. DET) mode. In this mode, the losses are less as the voltages at the output and input become equal and there are only 3 components in the path of power flow - the inductor coil, MOSFET which is in overdrive mode and a Schottky diode that is in full conduction.

- In boost mode, topologies involving two inductor boost (D and E) have the least efficiency. This is due to the fact that currents in boost mode through both inductors add up resulting in higher losses in active devices.
- In buck mode, topologies involving two inductor buck (A and C) have the least efficiency due to the increased currents through active devices.

Topology B has the best overall efficiency among the topologies in CCM.

To simulate the topologies in BCM, the inductor is designed for Litz windings and the results of simulations are as shown in figure 4-17. The trend for efficiency is similar to that of CCM;



**Figure 4-17:** Efficiency of Topologies in BCM

however some points are to be noted.

- In boost mode, the peak value of currents are highest when the difference in voltage magnitudes between  $V_{in}$  and  $V_o$  is the highest. This contributes to higher losses as the frequency of operation is high at these ranges. As the difference becomes lower, the topologies have better efficiency as seen in figure 4-17.
- In buck mode, the efficiency remains almost constant as the variation in current through all topologies is minimal.

## 4-14 Conclusion

This chapter dealt with issues related to losses in the topology and component selection. The summary of this section of the report is as follows

- Analytical modelling of losses is necessary to ascertain the performance of a topology. The losses in inductor, capacitor, MOSFETs and Schottky diode are analytically modelled to predict the results in the prototype.

- Conduction and switching losses in MOSFETs have to be determined in BCM and CCM to understand the suitability for an application. In BCM, MOSFETs perform with less turn-on losses in the analytical model.
- Selection of windings for winding the inductor will be dependent on the frequency and mode of operation. Inductor loss modelling depends upon the mode of operation and types of windings.
- Component selection is vital in designing a highly efficient converter. Every topology has specific requirements that will affect component selection. Two inductor topologies such as A,C,D and E necessitate a film capacitor.
- Simulation results showcase the advantage of BCM over CCM in terms of switching losses (turn on losses particularly). The advantage of Litz windings was highlighted in the simulations and efficiency is calculated for all the topologies in CCM and BCM.
- Topology B is the candidate topology that has the highest overall efficiency among all the constituent topologies.





# Prototypes and Experimental Results

In chapters 3 and 4, topologies and their theoretical aspects are ascertained. However, to arrive at the best topology, it would be best to detail the experimental results of the final prototype/s of the  $B^2R$  converter. The characteristic waveforms concerned with efficiency of the converters during buck and boost operation are presented and the losses were simulated in section 4-13. This section details the experimental setup for different modes of operation for the prototype/s along with the comparison with the simulated results and concluded with a discussion on the results.

Since we are dealing with frequencies above 100kHz, accuracy in determining the losses in switching the devices, current and voltage measurements carried out for turn-on and turn-off losses become very important. MOSFETs in the real world are typified by a high rate of change of voltage and current making measurements with heightened accuracy a challenge. This necessitates the use of better equipment for measurements.

## 5-1 Overview of Measurements

### 5-1-1 Bandwidth of the Oscilloscope

The bandwidth of an oscilloscope or a probe is the range of frequencies it is designed to measure for. It is the point in a plot of amplitude vs frequency, where its response causes a 3dB decrease in amplitude of the output. Beyond these frequencies, unreliability of measurements can be observed as the signal can attenuate extremely. Also, multiple frequency contents are observed in the signals measured with DC-DC converters (sawtooth, triangular etc.). To accurately measure these components, the bandwidth of the oscilloscope for measurement should be at least 5 times the operating frequency [43].

As in case of probes, they must possess adequate bandwidth to capture the signal, with the faster rise and fall for switching transitions. Effective bandwidth of an oscilloscope signal with  $t_r$  (Rise time) and  $t_f$  (fall time) is given in [44] by

$$f_{BandWidth} = \frac{0.35}{\min(t_r, t_f)} \quad (5-1)$$

Where,

$t_r$  = time taken by the signal to ascend from 10% to 90% (w.r.t nominal value)

$t_f$  time was taken by the signal to descend from 90% to 10%

This implies that the interval between the rise and the fall time will decide the bandwidth for the measuring equipment.

### 5-1-2 Voltage measurement

Voltage measurements are necessary for the operational efficiency, switching characterization and analysis of switching losses when a power MOSFET is in operation. Typically  $V_{gs}$ , gate-source voltage and  $V_{ds}$ , the drain-source voltage are measured to ascertain the behaviour of the switch. Although input voltage and output voltage in a DC-DC converter can be measured by a digital multi-meter, it is preferable to document the waveforms for future reference and observe the noise in the signal for designing filters.

Three types of probes under consideration for measurements are

- Differential probe - These probes are used when differential signals are referenced to each other instead of referencing to the earth potential. In case of experiments carried out for switching losses in buck mode, these probes are used to measure drain to source voltage  $V_{DS}$ .
- Voltage divider probe - They are passive probes are used when higher bandwidths are needed. Voltage divider probe has low tip capacitance leading to a high bandwidth (up to GHz) and faster rise times. One disadvantage is that they have relatively high resistive loading.
- Single-ended voltage passive probe - These are passive probes most widely used and are available with attenuation factors of 1X, 10X or 100X; 10X probe being widely used.

### 5-1-3 Current measurement

The drain current  $I_d$  and inductor current values  $I_L$  are necessary for characterization of a power MOSFET and conduction mode of the converter respectively. Due to these measurements, current measurements become crucial.

When current flows through a conductor, an electromagnetic field is observed around it which is sensed by the current probe to convert it to equivalent voltage for measurements. In our experiments, a split-core current probe is used.

## 5-2 Topology B and C experiments

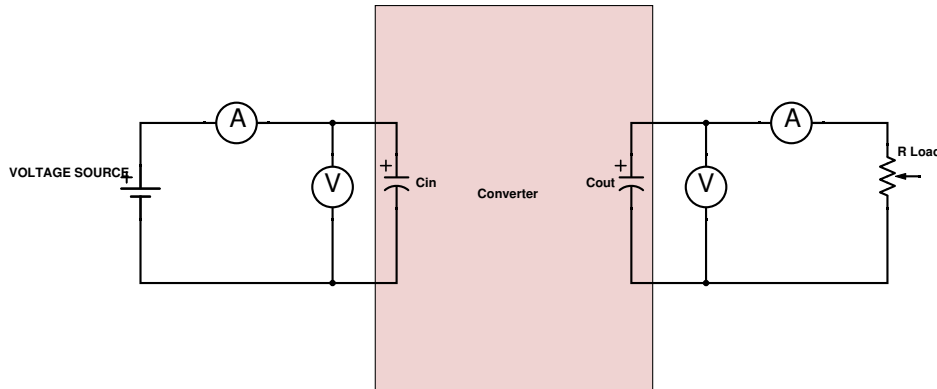
As discussed in the previous chapters, Topology B is most apt for the converter to be implemented; Topology C is the next best.

As per theoretical calculations, the efficiencies are determined for different modes of operation.

An experimental verification would be necessary to compare the validity of the results through simulations with that of the experiments in the lab.

### 5-2-1 Experimental set-up

A schematic of the apparatus for measurements w.r.t. efficiency is as shown in the figure 5-1. The input and output voltages are measured using voltage probes mounted at the input and output capacitors. Current probes are mounted near the source and load to measure the flow of currents closer to each port. The voltage probes for measurement are as *Yokogawa 702906*



**Figure 5-1:** Measurement points

and current probe used is *TEK 702906*. The resistance used as the load is a variable one. This will ensure that it can be changed to correspond to the fraction of the full load current that will flow through it.

The current probe amplifier of *TEK 702906* has the current knob settings at 1A/div and this is corresponded in the oscilloscope *DL-1740EL* by setting the voltage division to 20mV per division for CCM. However, In case of BCM, the current knob is set at 2A/div as the peak value of current to be measured is pretty high.

The signal generator *TTi TG330* supplies for the PWM for the buck and boost operation. The components used for performing experiments are as shown in table 5-1.

**Table 5-1:** Component Values

Component	Part/ Make
S1-A	STF20NF20
S1-B	STF20NF20
S2	STF20NF20
D1	STPS10L60CFP
D2	STPS10L60CFP
S1-A Driver	LT1910
S1-B Driver	IR2117
$C_{in}$	EPCOS EEUFM1H471
$C_{out}$	EPCOS EEUFM1H471
$C_{transfer}$	EPCOS B32529C0105J000
Core Material L1,L2	PQ 20/16 - 3C95

### 5-2-2 Experimental determination of efficiency

Topologies B and C are soldered onto a soldering board and for different input voltages the readings are documented. To select the best topology, the two best topologies are compared. Various parameters discussed in the previous sections about the efficiency of the topologies under BCM and CCM are necessary to be detailed.

The procedure followed to determine efficiency will be as follows.

- A specific mode of conduction is selected. The switching frequency is set accordingly and the inductor current is probed to determine the mode of operation. An example of one of the readings is illustrated for topology B, boost Mode in CCM figure 5-2a and in BCM figure 5-2b. The current probe is placed to measure the inductor current to detect the mode of operation.
- Input and output voltages are probed and the current probe is now used to measure the currents at the load and input. A load current of 2.666A is set as it is ideally the current necessary for charging the battery at a rate of  $C/10$ . This is the optimum rate at which the Ni-Fe battery will be 'fast charged'.
- Efficiency is determined by calculations of documented values of current and voltage. The accuracy of the measuring instruments is determined through data-sheets and calculations are done.

After ascertaining the mode of conduction, to measure the currents and voltages at the input and output ports, probes are positioned as shown in figure 5-1.

#### Buck Mode

Buck Operation in case of topology B involves using a high side driver, IR-2117 as the source terminal of the buck converter is not at common ground, unlike a boost converter. The schematic for the high side driver circuit is as shown in figure 4-10. The supply voltage to the gate to source terminals of switch S1-B, which will be driven by a PWM supplied by the signal generator.

In case of topology C, the buck switch is driven the same way as that in topology B. The input voltage is varied from 41V until 45V and subsequent measurements of voltage and current are documented.

#### Boost Mode

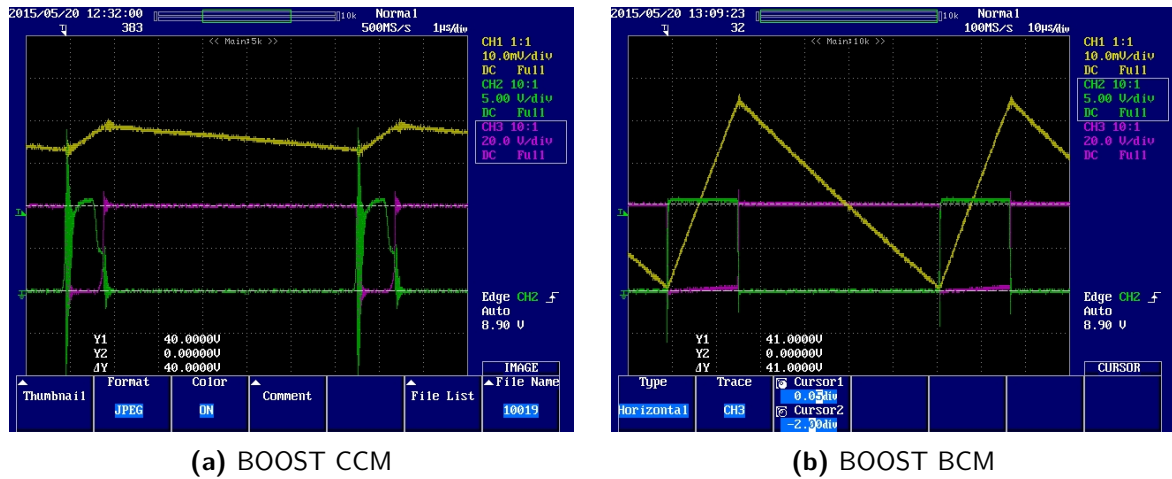
S1-B is connected to a different high side driver (other than IR-2117) that can run the MOSFET in '*Overdrive*' mode, as seen in figure 4-11 in page 52. This is the mode in which the switch S1-B is always on when the input voltage is less than the output. S1-B can be MOSFET which has lower on state resistance to facilitate less losses. S2 is operated both in Topology B and C for boost mode of operation.

### BCM/CCM conduction modes

As discussed earlier, the conduction modes play an important role in the selection of inductor values and winding characteristics.

In case of CCM experiments, the inductors selected contain copper windings.

In case of BCM experiments, the inductors selected will be utilising Litz construction for windings to handle high ripple currents with less losses.



**Figure 5-2: CCM and BCM Boost**

Yellow - Inductor current -  $I_L$   
 Green - Gate to Source voltage  $V_{gs}$   
 Purple - Drain to Source voltage  $V_{ds}$

### 5-2-3 Topology B in CCM and BCM

The results of experiments on topology B in CCM is tabulated in table 5-2 and a plot of efficiency w.r.t. variance in input voltage is given in figure 5-3a.

In *Boost mode*, as expected, the efficiency is lower due to the high RMS value of currents at the input of the converter.

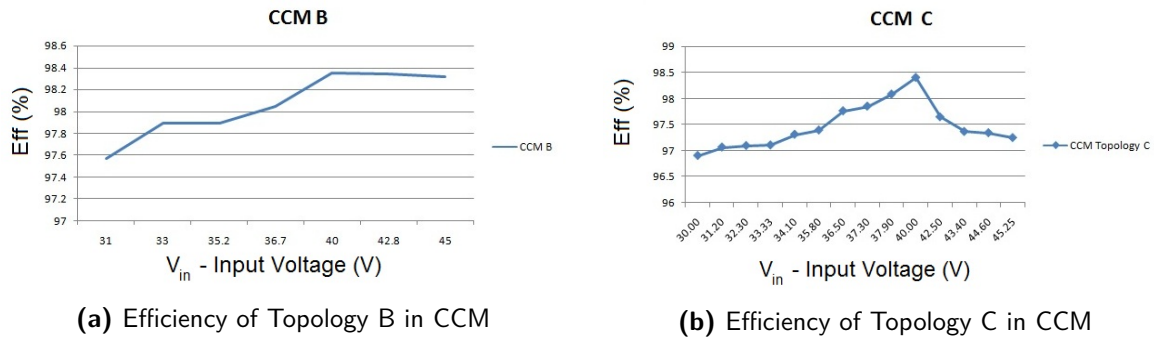
The efficiency increases as the voltage reaches close to the output voltage. The inductance value used for CCM operation is  $L_1 = 42.333\mu H$ . In *DET mode* i.e. at 40V input, topology has the highest efficiency as no switching happens.

In *Buck mode*, the efficiency is fairly constant due to the fact that the duty cycle variation is negligible. The variation of the input current for a fixed load current is minimal. Also, the current at the input is always less than the load.

In case of BCM, to optimise the topology for comparison with the one in CCM, inductance value is fixed at  $L_1 = 8.13\mu H$ . The windings used are Litz wire based windings.

The efficiency is lower for boost mode when the difference between input and output voltage is higher. The circuit is operated at marked decrease in switching frequency as input voltage approaches the output voltage.

Buck Mode shows a better efficiency as compared to the Boost Mode.

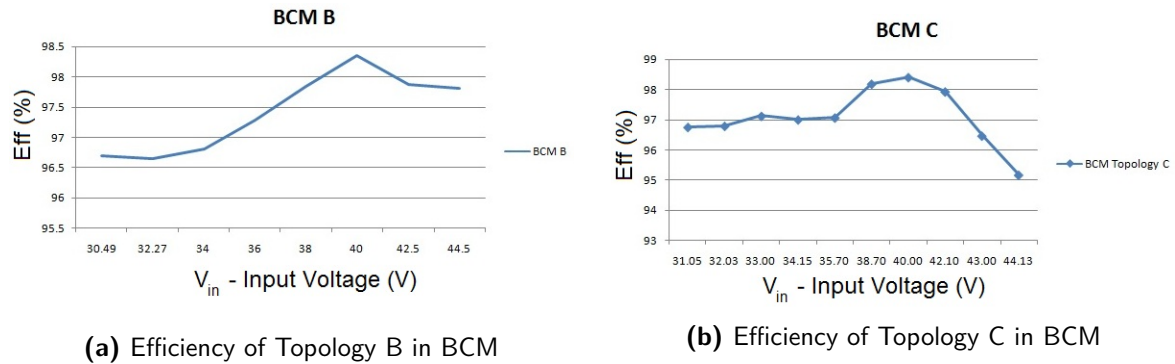


**Figure 5-3:** CCM experimental efficiencies in Topology B and C

**Table 5-2:** Efficiency of Topology B in CCM

$V_{in}$	$V_o$	$I_{in}$	$I_o$	$\% \eta$
31	40.19	3.56	2.67	97.5
33	40.29	3.35	2.68	97.8
35.2	40.17	3.12	2.67	97.8
36.7	40.29	3	2.68	98.0
40	39.32	2.62	2.62	98.3
42.8	39.41	2.46	2.62	98.3
45	39.7	2.37	2.64	98.3

As expected; DET mode has the highest efficiency. The results of BCM based experiments are as shown in table 5-3 and figure 5-4a.



**Figure 5-4:** BCM experimental efficiency in Topology B and C

#### 5-2-4 Topology C in CCM and BCM

Topology C will involve two inductors. The efficiency measurement results are demonstrated in tables 5-4 for CCM and 5-5 for BCM. As expected, the efficiency in BCM or CCM for this topology is less in comparison with that of topology B irrespective of the mode of operation when the voltage difference between input and output is very high. The inductor  $L_1$  is probed for determining the mode of operation. This topology uses a two inductor buck meaning that

**Table 5-3:** Experimental efficiency of Topology B in BCM

$V_{in}$	$V_o$	$I_{in}$	$I_o$	$\% \eta$
30.49	40.58	3.72	2.70	96.6
32.27	40.59	3.52	2.70	96.6
34	39.87	3.22	2.65	96.8
36	40.13	3.07	2.67	97.2
38	40.123	2.89	2.67	97.8
40	39.32	2.62	2.62	98.3
42.5	39.54	2.51	2.63	97.8
44.5	40.12	2.47	2.67	97.8

a transfer capacitor is used with a high current capability.

**Table 5-4:** Experimental efficiency of topology C CCM

$V_{in}$	$V_o$	$I_{in}$	$I_o$	$\% \eta$
30.00	41	3.15	2.23	96.9
32.30	39.6	2.74	2.17	97.1
34.10	40.1	2.65	2.19	97.3
36.50	39.9	2.46	2.20	97.7
37.90	40.6	2.45	2.24	98.0
40.00	39.36	2.18	2.18	98.4
42.50	40.53	2.09	2.14	97.6
44.60	40.41	2.09	2.24	97.3
45.25	40.5	2.08	2.26	97.2

**Table 5-5:** Experimental efficiency of topology C BCM

$V_{in}$	$V_o$	$I_{in}$	$I_o$	$\% \eta$
31.05	39.8	2.88	2.17	96.7
33.00	40.24	2.80	2.23	97.1
35.70	40.4	2.60	2.23	97.0
38.70	40.54	2.39	2.24	98.1
40.00	39.36	2.18	2.18	98.4
42.10	40.5	2.23	2.27	97.9
44.13	40.7	2.20	2.27	95.1

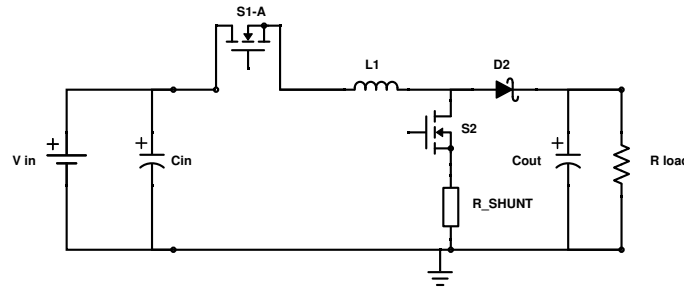
### 5-2-5 Comparison with analytical model for efficiency calculations

The results of experimental validation as shown in figures 5-4a, 5-4b, 5-3a and 5-3b. The comparison between the results of simulations from analytical model using MATLAB and experimental results do not differ very much. Topology B can be concluded to be the best topology when the priority is higher efficiency and less complex system to be built. The peak values of currents are higher in case of BCM in both the topologies and the efficiency of BCM

is higher as the difference between input and output voltages is smaller.

### 5-3 Determination of switching losses

To validate the analytical model, the MOSFETs in each mode will be subjected to test experimentally. To measure the current  $I_{DS}$  in buck/boost mode, a current shunt of  $50m\Omega$  is used. This is one of the practical methods to obtain the voltage equivalent of current and measure the magnitude. The setup for measuring losses in the MOSFET during the switching transition in the boost mode is as shown in the figure 5-5.



**Figure 5-5:** Switch losses determination apparatus for boost mode

The voltage probes are connected to drain and source terminals of the MOSFET  $S_2$  and the voltage is measured across the shunt resistance  $R_{shunt}$ . The current through drain to source terminals is determined by the formula,

$$I_{ds,exp} = \frac{V_{shunt}}{R_{shunt}} \quad (5-2)$$

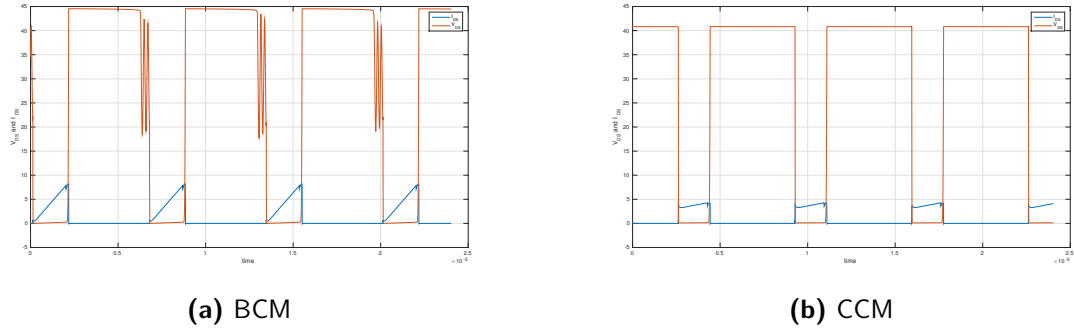
To eliminate the signal components in the waveform (noise) and attain results relevant to operating frequency, the data from the oscilloscope is saved in .mat format and analyzed with a *Butterworth filter*. The results are taken for both the topologies in BCM and CCM operation in boost operation for reasons relating to simplicity of connections and eliminating excessive usage of differential probes. The idea of such an experiment is to verify if BCM has significantly lower losses than BCM as predicted by the analytical models.

The experimental results for losses due to switching transitions are carried out and the results for overall losses due to switching is as shown in figure 5-10. Upon comparison of the experimental results with that of the analytical model simulations, they are found to be coinciding under experimental error limits. The accuracy of such an experiment can be considered tolerable as the current shunt has a tolerance of 1%.

The BCM is beneficial in case of switching losses as the turn-on losses which are experimentally determined are less considerably lower as.

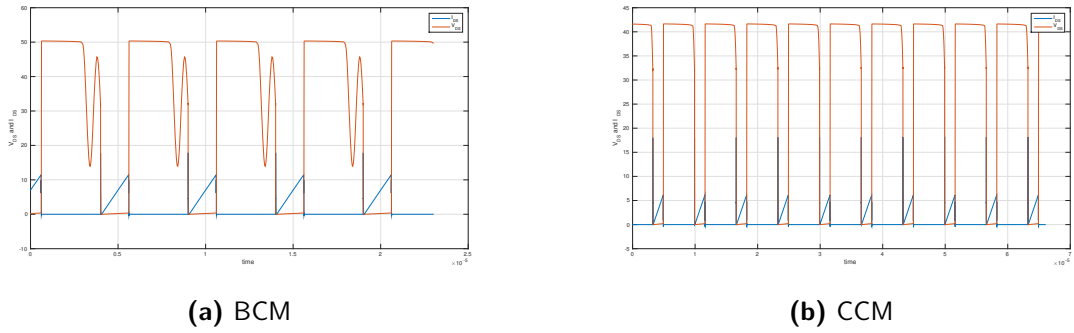
In case of CCM, the turn-on losses are significantly higher than the turn-off losses and this yields higher switching losses during the operation in either topology.





**Figure 5-6:** Switching transitions in topology B in BCM and CCM

In the graphs,  
 Blue -  $V_{ds}$   
 Red -  $I_{ds}$



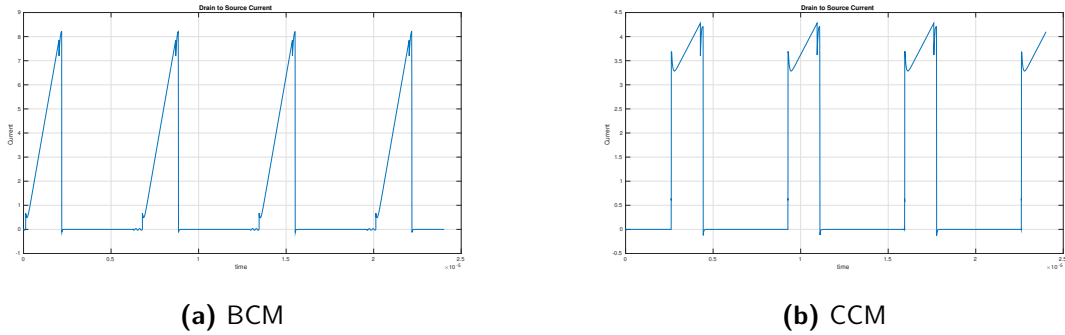
**Figure 5-7:** Switching transitions in topology C in BCM and CCM

In the graphs,  
 Blue -  $V_{ds}$   
 Red -  $I_{ds}$

A closer look at the drain to source current through the MOSFETs reveals a sharp instantaneous current increase during switch on transient as shown in figure 5-8b in case of topology B in CCM. In comparison, in BCM, it has negligible current increase as shown in figure 5-8a. This is attributed to two observations

- Reverse recovery process of the Schottky diode during the previous switching cycle. A good design must involve a diode with good recovery characteristics in cases where hard switching is involved, CCM being a mode in which this idea can be employed. In BCM, during the second half cycle ( $1 - D$ ), the current is controlled to hit a zero value not necessitating a diode with the best reverse recovery characteristics.
- The position of the current shunt for measurement of the drain to source current will facilitate the current that charges  $C_{gs}$  during the turn on transitions.

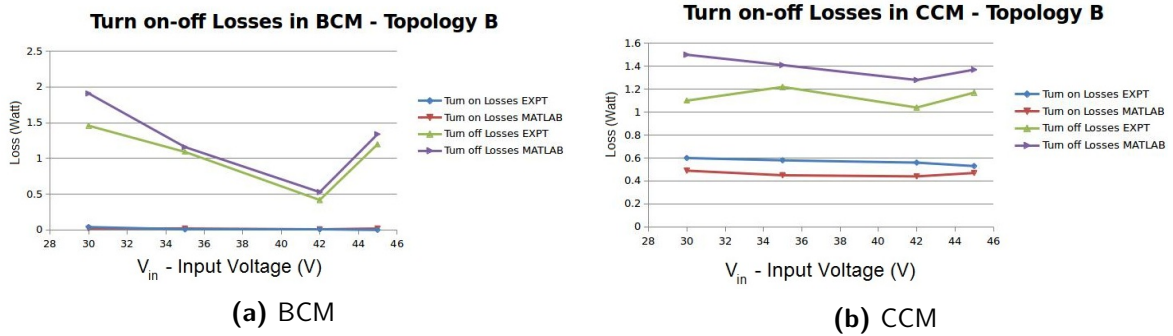
Figures 5-9a and 5-9b show the comparison of the values obtained from the analytical model (indicated by MATLAB) and experimental values(indicated by EXPT). Figure 5-9a shows the



**Figure 5-8:** Recovery during switching on transitions in Topology B in Boost mode

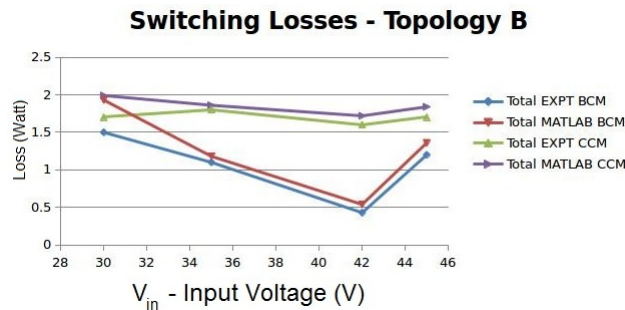
comparison of switching losses in topology B in BCM. The turn-on losses are almost zero. In contrast, the losses in switching due to CCM is as shown in figure 5-9b which is significantly higher.

The analytical model predicts the range of losses due to switching and its pattern in buck and boost modes. Also, the analytical model predicts lesser losses than the experimental results for turn off losses.



**Figure 5-9:** Turn on and off loss- Analytical Model validation

Similarly, overall losses are calculated in both BCM and CCM and plotted to validate the analytical model as shown in figure 5-10.



**Figure 5-10:** Switching loss - overall

# Conclusions and future work

## 6-1 Conclusions

This master thesis project was carried out to select a topology from the patent 550 of ESA to build a highly efficient battery charger for Nickel-Iron batteries. The aspects relating to the procedure to evaluate the topologies, design the magnetics, develop the analytical loss model for assessment of the converters, building the prototype for testing and experimental results are discussed in chapters 3,4 and 5. Upon building the final prototype on the soldering board and carrying out experiments for efficiency between the topologies and later using the results to validate the analytical model, some discussions can be done before concluding with the suggestions for design as below

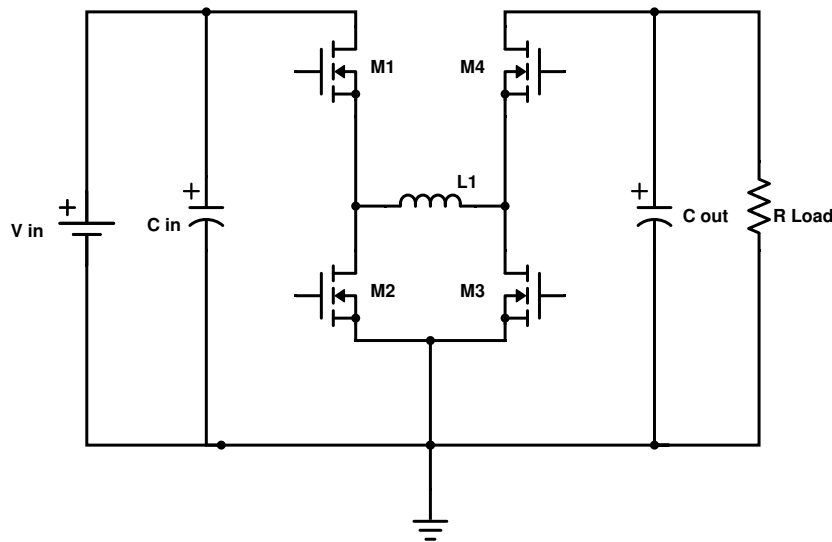
- **Topological selection** - All the five topologies are direct topologies as discussed in chapter 3. Among all the five topologies, Topology B is the most efficient one and has the least lossy profile due to the reason that it uses a single coil and absence of the capacitor  $C_t$ . As size is not a concern and efficiency is one of the vital parameters, topology B can be considered the best candidate for the highly efficient battery charger. Topology B consists of the least components, easier to build for the given power level and has lower switch stresses. Inductor  $L_2$  in case of topologies A, C, D and E carry less current and can be designed with a smaller core and hence with a better design to minimise losses.
- **Conduction Mode** - Although each conduction mode has its relative benefits and drawbacks, boundary conduction mode(BCM) is preferable as it has lower switching losses and soft switching properties. BCM can also operate at an occasional higher switching frequency which can enable reduced passive component sizes and increased power density in the converter. MOSFET switching losses (turn on specifically) are lesser in case of BCM as compared to CCM testifying the fact that they are better due to zero current switching profile. Deep CCM is signified by a higher switching loss profile.

- **Magnetics** - BCM offers a possibility to incorporate a smaller inductance value in the topologies and all topologies operated in BCM preferably need to incorporate Litz windings to ensure they have least winding losses. Although expensive, Litz wires provide better performance for under high ripple applications.  
PQ core will become beneficial in the current circumstance as it provides better  $A_{effective}$  rating for the application as compared to equivalent EE cores.
- **Losses** - Diodes are devices which have maximum losses in the topologies, implying that they need to be chosen for the design. The best possible diode selection for the topologies will be the one having faster recovery characteristics - Schottky becomes the obvious choice. Conduction loss value through switch  $S_1$  is always higher, it would be wise to ensure that it has the least  $R_{ds,on}$  under workable limits. Similarly  $D_2$  can be a Schottky rectifier and it must have the best forward characteristics.  
It is required to check if the temperature increase with respect to power losses in the devices is very high in-order to ensure that the  $\Delta T$  value (temperature rise) is within the stable operating regions a.k.a SOA. If they do not comply, advanced cooling techniques should be utilised. It is always advisable to design the SMPS which can offer reliable operation with natural convection.
- **Analytical Model** - The model developed to assess the total efficiency was validated by experimental results carried out on topologies B and C. In both modes, BCM and CCM, predicted results of switching losses and total efficiency from the analytical models are in accordance with the experimental results of prototypes built for the purpose. Assumptions made for simplifying the simulations w.r.t the analytical models did not offset the results of the topological parameters.
- **Topology B** will be the best topology to be adopted for design.  
**BCM** is the best mode of conduction for the battery charger because of the following benefits
  - Lower switching losses over a wider range of input voltage
  - Necessity of a smaller inductance value
  - Higher efficiency

## 6-2 Suggestions for future work

The following suggestions are made for making a highly efficient battery charger for Ni-Fe battery applications

- Topology B was considered to be the best topology. It would have much lesser losses if a the buck-boost converter can be used in synchronous mode i.e. replacing Schottky diodes with MOSFETs as shown in figure 6-1. This converter can be checked for its on-state losses and if recovery losses are lesser than that of a Schottky diode in boundary conduction mode. This has the potential to be much more efficient and some work on testing this converter vis-a-vis the topologies can be beneficial. One of the issues would be utilize a controller for switching  $M_1$ ,  $M_2$ ,  $M_3$  and  $M_4$  with PWM to obtain the a constant output.



**Figure 6-1:** Synchronous Buck-Boost topology

- Until this point, all devices used were silicon or silicon carbide related switches/diodes. If the charger is set to be deployed in environments where ambient temperature is high and natural convection does not solve the problem, a corrective algorithm can be updated to the existing analytical loss model to predict the efficiency and performance of the devices under worst case scenario to check for Safe operating limits of temperature and currents.



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## Chapter 7

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# Appendix

### Analysis of Individual Topologies

It is evident that there are four individual power converter Topologies that need to be thoroughly understood to design the Converter. The two switch topologies are Cascaded, interleaved or superimposed. Currents in each of the topologies have distinct peak values necessitating different values of rated components. Switches will be presented with different selection issues like Breakdown Voltage and Stress ratings. In this section we shall discuss the methods of finding out currents through every device used in the topology in Both Boundary Conduction Mode and Continuous Conduction Mode.

#### One Inductor Boost - Conventional Boost

As shown in Figure 7-1, A One inductor Boost operates on switching duty cycle of Switch 'S2'. The Duty Cycle of Boost Converter is given by

$$D_{Boost} = 1 - \frac{V_{in}}{V_o} \quad (7-1)$$

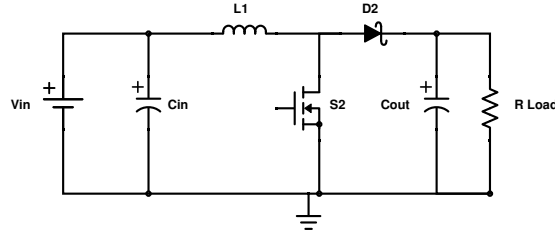
Peak to Peak ripple value will be dependent on the value of Inductance chosen for L1.

$$\Delta I_{L1,Peak} = \frac{V_{in} D_{Boost} T}{L_1} \quad (7-2)$$

#### Continuous Conduction Mode

In case of CCM, The Average Value of Inductor Current is

$$I_{L1,Avg} = \frac{P_{in}}{V_{in}} \quad (7-3)$$



**Figure 7-1:** One Inductor Boost

The Peak Value of Inductor Current is

$$I_{L1,Peak} = I_{L1,Avg} + \frac{\Delta I_{L1,Peak}}{2} \quad (7-4)$$

The RMS Value of Inductor Current is

$$I_{L1,RMS} = I_{L1,Avg} \sqrt{1 + \frac{1}{3} \left( \frac{\Delta I_{L1,Peak}}{2 I_{L1,Avg}} \right)^2} \quad (7-5)$$

The RMS Value of Current through the Switch is

$$I_{SW2,RMS} = \sqrt{D} (I_{L1,RMS}) \quad (7-6)$$

The RMS Value of Current through the Diode is

$$I_{D2,RMS} = \sqrt{(1 - D)} (I_{L1,RMS}) \quad (7-7)$$

The Average Value of Diode Current is

$$I_{D2,Avg} = \frac{P_o}{V_o} \quad (7-8)$$

The RMS Value of Current through the Input Capacitor is

$$I_{Cin,RMS} = \sqrt{I_{L1,RMS}^2 - I_{L1,Avg}^2} \quad (7-9)$$

The RMS Value of Current through the Output Capacitor is

$$I_{Cout,RMS} = \sqrt{I_{D2,RMS}^2 - I_{D2,AVG}^2} \quad (7-10)$$

### Boundary Conduction Mode

In case of BCM, the Peak Value of Inductor Current is

$$I_{L1,Peak} = \Delta I_{L1,Peak} \quad (7-11)$$

The RMS Value of Inductor Current is

$$I_{L1,RMS} = \frac{I_{L1,Peak}}{\sqrt{3}} \quad (7-12)$$



The Average Value of Inductor Current is

$$I_{L1,Avg} = \frac{I_{L1,Peak}}{2} \quad (7-13)$$

The RMS Value of Current through the Switch is

$$I_{SW2,RMS} = \sqrt{D} (I_{L1,RMS}) \quad (7-14)$$

The RMS Value of Current through the Diode is

$$I_{D2,RMS} = \sqrt{(1-D)} (I_{L1,RMS}) \quad (7-15)$$

The Average Value of Diode Current is

$$I_{D2,Avg} = \frac{P_o}{V_o} \quad (7-16)$$

The RMS Value of Current through the Input Capacitor is

$$I_{Cin,RMS} = \sqrt{I_{L1,RMS}^2 - I_{L1,Avg}^2} \quad (7-17)$$

The RMS Value of Current through the Output Capacitor is

$$I_{Cout,RMS} = \sqrt{I_{D2,RMS}^2 - I_{D2,AVG}^2} \quad (7-18)$$

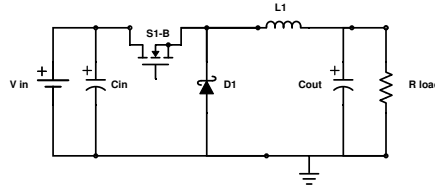
### One Inductor Buck - Conventional Buck

The Duty Cycle of Buck Converter is given by

$$D_{Buck} = \frac{V_o}{V_{in}} \quad (7-19)$$

Peak to Peak ripple value will be dependent on the value of Inductance chosen for L1.

$$\Delta I_{L1,Peak} = \frac{(V_{in} - V_o) D_{Buck} T}{L_1} \quad (7-20)$$



**Figure 7-2:** One Inductor Buck

### Continuous Conduction Mode

In case of CCM, The Average Value of Inductor Current is

$$I_{L1,Avg} = \frac{P_o}{V_o} \quad (7-21)$$

The Peak Value of Inductor Current is

$$I_{L1,Peak} = I_{L1,Avg} + \frac{\Delta I_{L1,Peak}}{2} \quad (7-22)$$

The RMS Value of Inductor Current is

$$I_{L1,RMS} = I_{L1,Avg} \sqrt{1 + \frac{1}{3} \left( \frac{\Delta I_{L1,Peak}}{2 I_{L1,Avg}} \right)^2} \quad (7-23)$$

The RMS Value of Current through the Switch is

$$I_{SW2,RMS} = \sqrt{D} (I_{L1,RMS}) \quad (7-24)$$

The RMS Value of Current through the Diode is

$$I_{D2,RMS} = \sqrt{(1 - D)} (I_{L1,RMS}) \quad (7-25)$$

The Average Value of Diode Current is

$$I_{D2,Avg} = \frac{P_o}{V_o} \quad (7-26)$$

The RMS Value of Current through the Input Capacitor is

$$I_{Cin,RMS} = \sqrt{I_{SW1,RMS}^2 - I_{SW1,Avg}^2} \quad (7-27)$$

The RMS Value of Current through the Output Capacitor is

$$I_{Cout,RMS} = \sqrt{I_{L1,RMS}^2 - I_{L1,AVG}^2} \quad (7-28)$$

### Boundary Conduction Mode

In case of BCM, the Peak Value of Inductor Current is

$$I_{L1,Peak} = \Delta I_{L1,Peak} \quad (7-29)$$

The Average Value of Inductor Current is

$$I_{L1,Avg} = \frac{I_{L1,Peak}}{2} \quad (7-30)$$

The RMS Value of Inductor Current is

$$I_{L1,RMS} = \frac{I_{L1,Peak}}{\sqrt{3}} \quad (7-31)$$

The RMS Value of Current through the Switch is

$$I_{SW2,RMS} = \sqrt{D} (I_{L1,RMS}) \quad (7-32)$$

The RMS Value of Current through the Diode is

$$I_{D2,RMS} = \sqrt{(1-D)} (I_{L1,RMS}) \quad (7-33)$$

The Average Value of Diode Current is

$$I_{D2,Avg} = \frac{P_o}{V_o} \quad (7-34)$$

The RMS Value of Current through the Input Capacitor is

$$I_{Cin,RMS} = \sqrt{I_{SW1,RMS}^2 - I_{SW1,Avg}^2} \quad (7-35)$$

The RMS Value of Current through the Output Capacitor is

$$I_{Cout,RMS} = \sqrt{I_{L1,RMS}^2 - I_{L1,AVG}^2} \quad (7-36)$$

## Two Inductor Boost

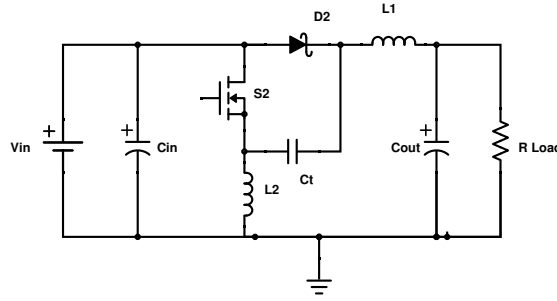
The Duty Cycle of Boost Converter is given by

$$D_{Boost} = 1 - \frac{V_{in}}{V_o} \quad (7-37)$$

Peak to Peak ripple value will be dependent on the values of Inductances chosen for  $L_1$  and  $L_2$ .

$$\Delta I_{L1,Peak} = \frac{V_{in} D_{Boost} T}{L_1} \quad (7-38)$$

$$\Delta I_{L2,Peak} = \frac{V_{in} D_{Boost} T}{L_2} \quad (7-39)$$



**Figure 7-3:** Two Inductor Boost

## Continuous Conduction Mode

In case of CCM, The Average Value of Current through Inductor  $L_1$  is

$$I_{L1,Avg} = \frac{P_o}{V_o} \quad (7-40)$$

The Average Value of Current through Inductor  $L_2$  is

$$I_{L2,Avg} = \frac{P_{in}}{V_{in}} \quad (7-41)$$

The Peak Value of Current through Inductor  $L_1$  is

$$I_{L1,Peak} = I_{L1,Avg} + \frac{\Delta I_{L1,Peak}}{2} \quad (7-42)$$

The Peak Value of Current through Inductor  $L_2$  is

$$I_{L2,Peak} = I_{L2,Avg} + \frac{\Delta I_{L2,Peak}}{2} \quad (7-43)$$

The RMS Value of Current through Inductor  $L_1$  is

$$I_{L1,RMS} = I_{L1,Avg} \sqrt{1 + \frac{1}{3} \left( \frac{\Delta I_{L1,Peak}}{2 I_{L1,Avg}} \right)^2} \quad (7-44)$$

The RMS Value of Current through Inductor  $L_2$  is

$$I_{L2,RMS} = I_{L2,Avg} \sqrt{1 + \frac{1}{3} \left( \frac{\Delta I_{L2,Peak}}{2I_{L2,Avg}} \right)^2} \quad (7-45)$$

The RMS Value of Current through the Switch is

$$I_{SW2,RMS} = \sqrt{D} (I_{L1,RMS} + I_{L2,RMS}) \quad (7-46)$$

The RMS Value of Current through the Diode is

$$I_{D2,RMS} = \sqrt{(1-D)} (I_{L1,RMS} + I_{L2,RMS}) \quad (7-47)$$

The Average Value of Diode Current is

$$I_{D2,Avg} = \frac{P_o}{V_o} \quad (7-48)$$

The RMS Value of Current through the Input Capacitor is

$$I_{Cin,RMS} = \sqrt{I_{LT,RMS}^2 - I_{LT,Avg}^2} \quad (7-49)$$

where,

$$I_{LT,RMS} = I_{L1,RMS} + I_{L2,RMS} \text{ and}$$

$$I_{LT,AVG} = I_{L1,AVG} + I_{L2,AVG}$$

The RMS Value of Current through the Output Capacitor is

$$I_{Cout,RMS} = \sqrt{I_{D2,RMS}^2 - I_{D2,AVG}^2} \quad (7-50)$$

The RMS Value of Current through the Transfer Capacitor is

$$I_{Ct,RMS} = \sqrt{D_{Boost} I_{L1,RMS}^2 - (1 - D_{Boost}) I_{L2,RMS}^2} \quad (7-51)$$

### Boundary Conduction Mode

In case of BCM, The Peak Value of Current through Inductor  $L_1$  is

$$I_{L1,Peak} = \Delta I_{L1,Peak} \quad (7-52)$$

The Peak Value of Current through Inductor  $L_2$  is

$$I_{L2,Peak} = \Delta I_{L2,Peak} \quad (7-53)$$

The Average Value of Current through Inductor  $L_1$  is

$$I_{L1,Avg} = \frac{I_{L1,Peak}}{2} \quad (7-54)$$

The Average Value of Current through Inductor  $L_2$  is

$$I_{L2,Avg} = \frac{I_{L2,Peak}}{2} \quad (7-55)$$

The RMS Value of Current through Inductor  $L_1$  is

$$I_{L1,RMS} = \frac{I_{L1,Peak}}{\sqrt{3}} \quad (7-56)$$

The RMS Value of Current through Inductor  $L_2$  is

$$I_{L2,RMS} = \frac{I_{L2,Peak}}{\sqrt{3}} \quad (7-57)$$

The RMS Value of Current through the Switch is

$$I_{SW2,RMS} = \sqrt{D}(I_{L1,RMS} + I_{L2,RMS}) \quad (7-58)$$

The RMS Value of Current through the Diode is

$$I_{D2,RMS} = \sqrt{(1-D)}(I_{L1,RMS} + I_{L2,RMS}) \quad (7-59)$$

The Average Value of Diode Current is

$$I_{D2,Avg} = (1 - D_{Boost})(I_{L1,AVG} + I_{L2,AVG}) \quad (7-60)$$

The RMS Value of Current through the Input Capacitor is

$$I_{Cin,RMS} = \sqrt{I_{LT,RMS}^2 - I_{LT,Avg}^2} \quad (7-61)$$

where,

$$I_{LT,RMS} = I_{L1,RMS} + I_{L2,RMS} \text{ and}$$

$$I_{LT,AVG} = I_{L1,AVG} + I_{L2,AVG}$$

The RMS Value of Current through the Output Capacitor is

$$I_{Cout,RMS} = \sqrt{I_{D2,RMS}^2 - I_{D2,AVG}^2} \quad (7-62)$$

The RMS Value of Current through the Transfer Capacitor is

$$I_{Ct,RMS} = \sqrt{D_{Boost}I_{L1,RMS}^2 - (1 - D_{Boost})I_{L2,RMS}^2} \quad (7-63)$$

## Two Inductor Buck

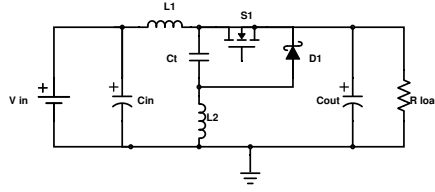
The Duty Cycle of Buck Converter is given by

$$D_{Buck} = \frac{V_o}{V_{in}} \quad (7-64)$$

Peak to Peak ripple value will be dependent on the values of Inductance chosen for  $L_1$  and  $L_2$ .

$$\Delta I_{L1,Peak} = \frac{(V_{in} - V_o) D_{Buck} T}{L_1} \quad (7-65)$$

$$\Delta I_{L2,Peak} = \frac{(V_{in} - V_o) D_{Buck} T}{L_2} \quad (7-66)$$



**Figure 7-4:** Two Inductor Buck

## Continuous Conduction Mode

In case of CCM, The Average Value of Current through Inductor  $L_1$  is

$$I_{L1,Avg} = \frac{P_o}{V_o} \quad (7-67)$$

The Average Value of Current through Inductor  $L_2$  is

$$I_{L2,Avg} = \frac{P_o}{V_o} - \frac{P_{in}}{V_{in}} \quad (7-68)$$

The Peak Value of Inductor Current values are

$$I_{L1,Peak} = I_{L1,Avg} + \frac{\Delta I_{L1,Peak}}{2} \quad (7-69)$$

$$I_{L2,Peak} = I_{L2,Avg} + \frac{\Delta I_{L2,Peak}}{2} \quad (7-70)$$

The RMS Value of Inductor Current values are

$$I_{L1,RMS} = I_{L1,Avg} \sqrt{1 + \frac{1}{3} \left( \frac{\Delta I_{L1,Peak}}{2 I_{L1,Avg}} \right)^2} \quad (7-71)$$

$$I_{L2,RMS} = I_{L2,Avg} \sqrt{1 + \frac{1}{3} \left( \frac{\Delta I_{L2,Peak}}{2 I_{L2,Avg}} \right)^2} \quad (7-72)$$

The RMS Value of Current through the Switch  $S_1$  is

$$I_{SW1,RMS} = \sqrt{D} (I_{LT,RMS}) \quad (7-73)$$

where,

$$I_{LT,RMS} = I_{L1,RMS} + I_{L2,RMS} \text{ and}$$

The RMS Value of Current through the Diode is

$$I_{D2,RMS} = \sqrt{(1-D)} (I_{LT,RMS}) \quad (7-74)$$

The Average Value of Diode Current is

$$I_{D2,Avg} = (1 - D_{Buck}) I_{LT,AVG} \quad (7-75)$$

Where,

$$I_{LT,AVG} = I_{L1,AVG} + I_{L2,AVG}$$

The RMS Value of Current through the Input Capacitor is

$$I_{Cin,RMS} = \sqrt{I_{SW1,RMS}^2 - I_{SW1,Avg}^2} \quad (7-76)$$

The RMS Value of Current through the Output Capacitor is

$$I_{Cout,RMS} = \sqrt{I_{LT,RMS}^2 - I_{LT,AVG}^2} \quad (7-77)$$

The RMS Value of Current through the Transfer Capacitor is

$$I_{Ct,RMS} = \sqrt{D_{Buck} I_{L1,RMS}^2 - (1 - D_{Buck}) I_{L2,RMS}^2} \quad (7-78)$$

### Boundary Conduction Mode

The Peak Value of Inductor Current values are

$$I_{L1,Peak} = \Delta I_{L1,Peak} \quad (7-79)$$

$$I_{L2,Peak} = \Delta I_{L2,Peak} \quad (7-80)$$

The Average Value of Current through Inductor  $L_1$  is

$$I_{L1,Avg} = \frac{I_{L1,Peak}}{2} \quad (7-81)$$

The Average Value of Current through Inductor  $L_2$  is

$$I_{L2,Avg} = \frac{I_{L2,Peak}}{2} \quad (7-82)$$

The RMS Value of Inductor Current values are

$$I_{L1,RMS} = \frac{I_{L1,Peak}}{\sqrt{3}} \quad (7-83)$$



$$I_{L2,RMS} = \frac{I_{L2,Peak}}{\sqrt{3}} \quad (7-84)$$

The RMS Value of Current through the Switch  $S_1$  is

$$I_{SW1,RMS} = \sqrt{D} (I_{LT,RMS}) \quad (7-85)$$

where,

$$I_{LT,RMS} = I_{L1,RMS} + I_{L2,RMS} \text{ and}$$

The RMS Value of Current through the Diode is

$$I_{D2,RMS} = \sqrt{(1-D)} (I_{LT,RMS}) \quad (7-86)$$

The Average Value of Diode Current is

$$I_{D2,Avg} = (1 - D_{Buck}) I_{LT,AVG} \quad (7-87)$$

Where,

$$I_{LT,AVG} = I_{L1,AVG} + I_{L2,AVG}$$

The RMS Value of Current through the Input Capacitor is

$$I_{Cin,RMS} = \sqrt{I_{SW1,RMS}^2 - I_{SW1,Avg}^2} \quad (7-88)$$

The RMS Value of Current through the Output Capacitor is

$$I_{Cout,RMS} = \sqrt{I_{LT,RMS}^2 - I_{LT,AVG}^2} \quad (7-89)$$

The RMS Value of Current through the Transfer Capacitor is

$$I_{Ct,RMS} = \sqrt{D_{Buck} I_{LT,RMS}^2 - (1 - D_{Buck}) I_{LT,RMS}^2} \quad (7-90)$$



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# Diode Currents

## Obtaining RMS and Average Values of Current

### CCM

For the Boost and Buck Mode operation waveforms in CCM, The  $I_{max}$  and  $I_{min}$  are calculated as follows

#### Boost

$$I_{max} = \frac{P_{in}}{V_{in}} + \frac{\Delta I_{L,pk-pk}}{2} \quad (7-91)$$

$$I_{min} = \frac{P_{in}}{V_{in}} - \frac{\Delta I_{L,pk-pk}}{2} \quad (7-92)$$

$$I_{D,Avg} = \frac{(I_{max} + I_{min})(1 - D_{Boost})}{2} \quad (7-93)$$

$$I_{D,RMS} = \sqrt{\frac{(I_{max})^2 + (I_{min})^2 + I_{max} * I_{min})(1 - D_{boost})}{3}} \quad (7-94)$$

#### Buck

$$I_{max} = \frac{P_o}{V_o} + \frac{\Delta I_{L,pk-pk}}{2} \quad (7-95)$$

$$I_{min} = \frac{P_o}{V_o} - \frac{\Delta I_{L,pk-pk}}{2} \quad (7-96)$$

$$I_{D,Avg} = \frac{(I_{max} + I_{min})(1 - D_{Buck})}{2} \quad (7-97)$$

$$I_{D,RMS} = \sqrt{\frac{(I_{max})^2 + (I_{min})^2 + I_{max} * I_{min})(1 - D_{Buck})}{3}} \quad (7-98)$$

## BCM

For the Boost and Buck Mode operation waveforms in BCM, The  $I_{max}$  and  $I_{min}$  are calculated as follows

### Boost

$$I_{max} = \Delta I_{L,pk-pk} \quad (7-99)$$

$$I_{min} = 0 \quad (7-100)$$

$$I_{D,Avg} = \frac{(I_{max} + I_{min})(1 - D_{Boost})}{2} \quad (7-101)$$

$$I_{D,RMS} = \sqrt{\frac{(I_{max})^2 + (I_{min})^2 + I_{max} * I_{min})(1 - D_{boost})}{3}} \quad (7-102)$$

### Buck

$$I_{max} = \Delta I_{L,pk-pk} \quad (7-103)$$

$$I_{min} = 0 \quad (7-104)$$

$$I_{D,Avg} = \frac{(I_{max} + I_{min})(1 - D_{Buck})}{2} \quad (7-105)$$

$$I_{D,RMS} = \sqrt{\frac{(I_{max})^2 + (I_{min})^2 + (I_{max} * I_{min})(1 - D_{Buck})}{3}} \quad (7-106)$$

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# Magnetics - Current Calculations

## Calculation of Inductance $L_1$ for CCM

In CCM, the value of inductor current should never hit a zero value. This effectively means that the ripple needs to be maintained at a minimum over the average value of current flowing through the inductance. So, Design would involve designing the minimum value of Inductance that would satisfy the requirements in buck and boost mode and ensure that it will maintain the mode of CCM for the system to function. Minimum Values of Inductance is calculated in both modes and then the maximum value of Inductance is chosen as a set value.

- The Minimum Inductance of  $L_1$  required for Boost Operation in CCM is given by

$$L_{min,boost} = \frac{V_{in}^2 T (V_o - V_{in})}{2 P_{o,min} V_o} \quad (7-107)$$

- The Minimum Inductance of the Inductance  $L_1$  required for Buck Operation in CCM is given by

$$L_{min,buck} = \frac{V_o^2 T (V_{in} - V_o)}{2 P_{o,min} V_{in}} \quad (7-108)$$

The Value of Inductance that is the highest of the two will ensure that the operation doesn't run into discontinuity at operating frequency.

## Boost Mode of operation in CCM

In this mode of operation, the topology is designed for a variation of input Voltage from 30V to 39V. In this mode the following Values of currents are observed.

- The duty cycle during boost operation is given by

$$D_{boost} = 1 - \frac{V_{in}}{V_o} \quad (7-109)$$

- The Peak to Peak ripple current in Inductor  $L_1$  during boost operation is given by

$$\Delta I_{L1,peak-peak,boost} = \frac{V_{in} D_{boost} T}{L_1} \quad (7-110)$$

- The Peak Current through Inductor  $L_1$  during boost operation is given by

$$I_{L1,peak,boost}^{\wedge} = \frac{P_{in,max}}{V_{in,min}} + \frac{V_{in,min}(V_o - V_{in,min})T}{2L_1 V_o} \quad (7-111)$$

- The Average Current through Inductor  $L_1$  during boost operation is given by

$$I_{L1,Avg,boost} = \frac{P_{in}}{V_{in}} \quad (7-112)$$

- The RMS Current through Inductor  $L_1$  during boost operation is given by

$$I_{L1,rms,boost} = I_{L1,Avg,boost} + \sqrt{1 + \frac{1}{3} \left( \frac{\Delta I_{L1,peak-peak,boost}}{2I_{L1,Avg,boost}} \right)^2} \quad (7-113)$$

### Buck Mode of operation $L_1$ in CCM

In this mode of operation, the topology is designed for a variation of input Voltage from 41V to 45V. In this mode, the following Values of currents are observed.

- The duty cycle during buck operation is given by

$$D_{buck} = \frac{V_o}{V_{in}} \quad (7-114)$$

- The Peak to Peak ripple current in Inductor  $L_1$  during buck operation is given by

$$\Delta I_{L1,peak-peak,buck} = \frac{(V_{in} - V_o) D_{buck} T}{L_1} \quad (7-115)$$

- The Peak Current through Inductor  $L_1$  during buck operation is given by

$$I_{L1,peak,buck}^{\wedge} = \frac{P_{o,max}}{V_o} + \frac{V_o(V_{in,max} - V_o)T}{2L_1 V_{in}} \quad (7-116)$$

- The Average Current through Inductor  $L_1$  during buck operation is given by

$$I_{L1,avg,buck} = \frac{P_{o,max}}{V_o} \quad (7-117)$$

- The RMS Current through Inductor  $L_1$  during buck operation is given by

$$I_{L1,rms,buck} = I_{L1,Avg,buck} + \sqrt{1 + \frac{1}{3} \left( \frac{\Delta I_{L1,peak-peak,buck}}{2I_{L1,Avg,buck}} \right)^2} \quad (7-118)$$

N.B. - Upon calculating the Values of Peak Inductor Current  $\hat{I}_{L1,peak}$ , Peak to Peak Ripple  $\Delta I_{L1,peak-peak}$  and RMS value of current  $I_{L1,rms}$ , we choose the highest values of Peak Current and Ripple current for worst case design.

## Calculation of Inductance $L_2$ for CCM

In case of CCM, The values of  $L_1$  and  $L_2$  are kept equal. This will ensure that the continuous mode is always maintained throughout the operating intervals. The Peak value of current through  $L_2$  will be much different to that in  $L_1$  necessitating change in some Inductor construction parameters like Core/Number of Turns/Airgap etc which will be discussed in subsequent parts of the report.

## Calculation of Inductance $L_1$ for BCM

In case of Boundary Condition Mode, the control is set in such a way that the frequency of the system varies to maintain the condition whereby the currents reaches a zero value every cycle. Hence, the Inductance value chosen can be set to the minimum value and switching frequency will be varied by virtue of control. This is an advantage of BCM.

- The Inductance of the Inductance  $L_1$  required for Boost Operation is given by

$$L_{min,boost} = \frac{V_{in}^2 T (V_o - V_{in})}{2P_{o,min} V_o} \quad (7-119)$$

- The Inductance of the Inductance  $L_1$  required for Buck Operation is given by

$$L_{min,buck} = \frac{V_o^2 T (V_{in} - V_o)}{2P_{o,min} V_{in}} \quad (7-120)$$

The Value of Inductance that is the lowest. The boundary condition of operation is ensured by changing frequency of switching in the MOSFETs.

## Boost Mode of operation in BCM

In this mode of operation, the topology is designed for a variation of input Voltage from 30V to 39V. In this mode, the following Values of currents are observed.

- The highest frequency of switching in units of kHz in case of a boost converter operating in BCM is given by

$$f_{sw} = \frac{V_{in,min}^2 (V_o - V_{in,min})}{2V_o L_1 P_{max}} \quad (7-121)$$

- The duty cycle during boost operation is given by

$$D_{boost} = 1 - \frac{V_{in}}{V_o} \quad (7-122)$$

- The Peak to Peak ripple current in Inductor  $L_1$  during boost operation is given by

$$\Delta I_{L1,peak-peak,boost} = \frac{V_{in} D_{boost} T}{L_1} \quad (7-123)$$

- The Peak Current through Inductor  $L_1$  during boost operation is given by

$$\hat{I}_{L1,peak,boost} = \Delta I_{L1,peak-peak,boost} \quad (7-124)$$

- The RMS Current through Inductor  $L_1$  during boost operation is given by

$$I_{L1,rms,boost} = \frac{\Delta I_{L1,peak-peak,boost}}{\sqrt{3}} \quad (7-125)$$

- The Average Current through Inductor  $L_1$  during boost operation is given by

$$I_{L1,avg,boost} = \frac{\Delta I_{L1,peak-peak,boost}}{2} \quad (7-126)$$

### Buck Mode of operation in BCM

In this mode of operation, the topology is designed for a variation of input Voltage from 41V to 45V. In this mode, the following Values of currents are observed.

- The highest frequency of switching in units of kHz in case of a buck converter operating in BCM is given by

$$f_{sw} = \frac{V_o^2(V_o - V_{in,max})}{2V_{in,max}L_1P_{max}} \quad (7-127)$$

- The duty cycle during buck operation is given by

$$D_{buck} = \frac{V_o}{V_{in}} \quad (7-128)$$

- The Peak to Peak ripple current in Inductor  $L_1$  during buck operation is given by

$$\Delta I_{L1,peak-peak,buck} = \frac{(V_{in} - V_o)D_{buck}T}{L_1} \quad (7-129)$$

- The Peak Current through Inductor  $L_1$  during buck operation is given by

$$\hat{I}_{L1,peak,buck} = \Delta I_{L1,peak-peak,buck} \quad (7-130)$$

- The RMS Current through Inductor  $L_1$  during buck operation is given by

$$I_{L1,rms,buck} = \frac{\Delta I_{L1,peak-peak,buck}}{\sqrt{3}} \quad (7-131)$$

- The Average Current through Inductor  $L_1$  during buck operation is given by

$$I_{L1,avg,buck} = \frac{\Delta I_{L1,peak-peak,buck}}{2} \quad (7-132)$$



## Calculation of Inductance $L_2$ for BCM

In case of BCM, The values of  $L_1$  and  $L_2$  are different ensuring boundary mode is maintained during the switching frequency changes.

- In case Boost mode is in play, the value of  $L_2$  is calculated by the following equation

$$L_{2,BST} = \frac{V_{in}^2(V_o - V_{in})}{2f_{BST}V_oP_{max}} \quad (7-133)$$

- In case of Buck, The value of  $L_2$  is given by

$$L_{2,BUCK} = \frac{V_o^2(V_{in} - V_o)}{2f_{BUCK}V_oP_{max}} \quad (7-134)$$

N.B. - The Values of Peak Inductor Current  $\hat{I}_{L1,peak}$ , Peak to Peak Ripple  $\Delta I_{L1,peak-peak}$  and RMS value of current  $I_{L1,rms}$  are chosen by the highest values of both modes for worst case design. This way, although the inductance value is not optimum for one of the modes, the switching frequency will not cross the specified limit.

## Two Inductor Topologies

In the Patent 550 provided, of the five buck-boost converters, four of them are DC-DC converters with two inductor topologies. For this purpose, additional Coil design of  $L_2$  has to be carried out for efficient utilization of the Topology in a specific mode. This is the reason the customization of coil design becomes vital.

### Case - CCM

In case of CCM, the design of Inductor  $L_1$  follows the same procedure as mentioned in the earlier section. But the design of  $L_2$  is done with different current specifications. The Value of Inductance through  $L_2$  will be the same as  $L_1$ , but the winding and core sizes will differ.

### Two Inductor Buck Topologies

In case of two inductor buck topologies in Topology A and Topology C, the average value of Inductor Current through  $L_2$  can be considered as

$$I_{L2,Avg,buck} = I_{out} - I_{L1,Avg,buck} \quad (7-135)$$

We know that current ripple through  $L_2$  becomes

$$\Delta I_{L2,peak-peak,buck} = \frac{(V_{in} - V_o)D_{buck}T}{L_2} \quad (7-136)$$

Hence, the values of peak and RMS current values can be expressed as

$$I_{L2,peak,buck}^{\wedge} = I_{L2,Avg,buck} + \frac{\Delta I_{L2,peak-peak,buck}}{2} \quad (7-137)$$

$$I_{L2,rms,buck} = I_{L2,Avg,buck} + \sqrt{1 + \frac{1}{3} \left( \frac{\Delta I_{L2,peak-peak,buck}}{2I_{L2,Avg,buck}} \right)^2} \quad (7-138)$$

### Two Inductor Boost Topologies

In case of Topology D and Topology E, the two inductors are used for boost operation. In case of design for  $L_2$ , the average current flowing through it is given by,

$$I_{L2,Avg,boost} = \frac{P_{in,max}}{V_{in}} \quad (7-139)$$

Peak to Peak Ripple current through the Inductor  $L_2$  becomes

$$\Delta I_{L2,peak-peak,boost} = \frac{V_{in} D_{boost} T}{L_2} \quad (7-140)$$

Using the above values, Peak and RMS values of current can be calculated as follows

$$I_{L2,peak,boost}^{\wedge} = I_{L2,Avg,boost} + \frac{\Delta I_{L2,peak-peak,boost}}{2} \quad (7-141)$$

$$I_{L2,rms,boost} = I_{L2,Avg,boost} + \sqrt{1 + \frac{1}{3} \left( \frac{\Delta I_{L2,peak-peak,boost}}{2I_{L2,Avg,boost}} \right)^2} \quad (7-142)$$

### Case BCM

In case of BCM, we need to consider the parameter of frequency to maintain the Boundary condition at the inductor  $L_2$

### Two Inductor Buck Topologies

We know that current ripple though  $L_2$  becomes

$$\Delta I_{L2,peak-peak,buck} = \frac{(V_{in} - V_o) D_{buck} T}{L_2} \quad (7-143)$$

Hence, the values of peak and RMS current values can be expressed as

$$I_{L2,peak,buck}^{\wedge} = \Delta I_{L2,peak-peak,buck} \quad (7-144)$$

$$I_{L2,rms,buck} = \frac{\hat{I}_{L2,peak,buck}}{\sqrt{3}} \quad (7-145)$$

$$I_{L2,Avg,buck} = \frac{\hat{I}_{L2,peak,buck}}{2} \quad (7-146)$$

## Two Inductor Boost Topologies

Peak to Peak Ripple current through the Inductor  $L_2$  becomes

$$\Delta I_{L2,peak-peak,boost} = \frac{V_{in} D_{boost} T}{L_2} \quad (7-147)$$

Using the above calculations, Peak and RMS values of current can be calculated as follows

$$\hat{I}_{L2,peak,boost} = \Delta I_{L2,peak-peak,boost} \quad (7-148)$$

$$I_{L2,rms,boost} = \frac{\Delta I_{L2,peak-peak,boost}}{\sqrt{3}} \quad (7-149)$$

$$I_{L2,Avg,boost} = \frac{\Delta I_{L2,peak-peak,boost}}{2} \quad (7-150)$$

## Selection of the Core

There are two aspects to the selection of a core. The material of the core must withstand the temperature rise and provide less lossy performance for the operating frequency. To select the core, a value of maximum flux density  $B_{max}$  in Unit 'milli Tesla' is obtained through the graphs. This is the maximum value of AC flux density for a core. This is to ensure the design doesn't drive the inductor core into saturation upon worst case operation due to inductor ripple.

## Core Shape and Characteristics

EE and PQ cores are suitable for our application. One measure of the size of the cores will be decided by some reference graphs provided by manufacturers. We use Ferroxcube cores for the purpose with Core material as 3C-95. PQ core is elected over the EE core as it reduces the number of turns due to the large  $A_{effective}$  for comparable sizes. From the datasheets, the permeability of the core material and  $A_{min}$ , a minimum cross-sectional area of the core are obtained. Figure 7-5 shows a core half of the PQ core demonstrating the large  $A_{effective}$  available for inductor construction. The Number of turns is calculated is as follows

$$N = abs\left(\frac{LI_{L,peak}}{B_{m,op}A_{min}}\right) \quad (7-151)$$



**Figure 7-5:** PQ Core Half

We observe that number of turns is inversely proportional to the  $A_{min}$  of the core. Hence, PQ cores hold an advantage in this regard. To ensure saturation of the core is not reached,  $B_{m,op}$  is the operating flux, we set it at 90% of the maximum flux density  $B_{max}$ . Hence

$$B_{m,op} = 90\%B_{max} \quad (7-152)$$

Worst case flux density after selecting the number of turns will be

$$B_m^* = \frac{L}{N_{Selected}A_e}(I_{L,peak}) \quad (7-153)$$

Determining the wire size is dependent on skin depth and DC resistance of the wire. A realistic wire diameter is considered and iterations are carried out to optimize the losses and fit the winding in the inductor core former.

In addition, Litz wire is also considered as they can enable reduced losses due to their performance under conditions where skin effect can become significant (Eg. Boundary Condition Mode). Copper Wire Diameter is set to a realistic value that will ensure winding is hassle free.

$$Dia_{Cu} \leq 0.5mm \quad (7-154)$$

Wire diameter including the thickness of insulation is referred to by using the wire reference Table and christened  $Dia_{winding}$ .

$$Dia_{winding} = Dia_{Cu} + Dia_{insulation} \quad (7-155)$$

Area occupied by the windings is given by

$$A_{wind} = 1.1N\pi \frac{Dia_{winding}^2}{4} n_s \quad (7-156)$$

Where  $n_s$  is the number of strands

1.1 is the correction factor

Air-gap  $l_g$  in the central limb is fixed depending upon the core material.

$$l_g = \frac{\mu_0\mu_r N^2 A_c}{L} \quad (7-157)$$

## Winding Properties

Bobbin thickness,  $t_{bobbin}$  and length of the bobbin,  $l_{bobbin}$  are looked up from the data-sheets. Length available within the bobbin is calculated as

$$l_{available} = l_{bobbin} - 2 * t_{bobbin} \quad (7-158)$$

Bobbin Winding Area is given by winding area bobbin  $A_{bobbin}$  of the bobbin from the data-sheets. A possibility check for windings is carried out. If Area of the Winding < Area of the Bobbin, the winding is possible

This is only a first measure, however, the actual winding possibility will be discussed in detail in the latter part of the document. It depends upon the number of layers and in effect, the thickness of each layer. Total length of copper wire used is given by

$$l_{Cu} = 1.2(MLT)Nn_s \quad (7-159)$$

Where

1.5 is correction factor,

MLT is Mean Length Per turn

$$t_{winding} = t_{insulation} + t_{Cu} \quad (7-160)$$

Where,

$t_{winding}$  is the thickness of the winding that includes insulation.

Bobbin parameters  $A_{bobbin}$  and  $l_{bobbin}$  are important for the calculation of the number of layers and possibility of Winding

$$N_{layers} = \frac{N}{\frac{l_{bobbin}}{t_{winding}} - 1} \quad (7-161)$$

## Calculation of DC Resistance of the windings is as follows

Resistivity of Cu at operating temperature  $t_{op}$  is given by

$$\rho_{Cu,t} = \rho_{Cu,25} \left( 1 + \frac{0.393(t_{op} - 25)}{100} \right) \quad (7-162)$$

$$R_{DC} = DCR = \left( \frac{\rho_{Cu-wire} l_{total}}{a_w n_s^2} \right) t_{co-eff} \quad (7-163)$$

Where

$t_{co-eff}$  is the Temperature Co-efficient given by

$$t_{co-eff} = 1 + \frac{(t_{co-eff@25deg})(t_{operating})}{100} \quad (7-164)$$

Where

$t_{operating}$  = Operating temperature

$l_{total}$  = (Mean Length Per Turn)(Number of Layers) $n_s$

Skin Depth is calculated as follows

$$\delta = \sqrt{\frac{\rho_{Cu,t}}{\pi \mu_0 \mu_r f_{sw}}} \quad (7-165)$$



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