A Compact Ultrasound Low-Noise Amplifier with 40 dB Built-in Time-Gain Compensation

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ABSTRACT

This thesis presents the design of a low-noise amplifier (LNA) with integrated time-gain compensation (TGC) for ultrasound imaging applications. The primary objective is to develop a compact, power-efficient solution that compensates for signal attenuation in deep tissue imaging. Traditional LNA and TGC systems are bulky and power-hungry, but by integrating TGC directly into the LNA, this work optimizes both size and power consumption while maintaining high performance. The design addresses key challenges such as process, voltage, and temperature (PVT) variations, linearity, and noise performance.

The LNA-TGC is designed using TSMC 0.18 µm CMOS technology and features a variable gain range of 40 dB, maintaining a constant unity gain bandwidth (UGBW) to prevent distortion. The feedback network, utilizing two back-to-back MOS transistors in the triode region, is configured to provide an exponentially increasing resistance to enable dynamic gain control. A replica biasing circuit is designed together with feedback network. To ensure low noise and high linearity, the architecture incorporates a four-stage variable gain amplifier with carefully designed feedback paths. A trimming method is explored to tune the gain error against mismatches. Simulation results show that the design meets its noise, gain, and power consumption targets, making it suitable for high-resolution 3D ultrasound probes, particularly in medical imaging applications where space and power are constrained.

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1 INTRODUCTION

1.1 APPLICATION BACKGROUND

The growing prevalence of cardiovascular diseases and other health conditions has driven the increasing demand for advanced medical imaging technologies. According to the World Health Organization (WHO), cardiovascular diseases remain the leading cause of death globally [1]. Early detection and accurate diagnosis are critical for managing these conditions, and medical imaging plays a pivotal role in achieving these goals [2]. Medical imaging encompasses a range of technologies, including ultrasound, magnetic resonance imaging (MRI), computed tomography (CT), and X-ray imaging, each serving distinct diagnostic purposes. Ultrasound imaging is preferred for cardiovascular disease diagnosis and management due to several key advantages over other imaging modalities. One of the primary reasons is its ability to provide real-time imaging, which is crucial for assessing dynamic cardiac functions [3], such as heart valve movements and blood flow, in a non-invasive manner. This real-time capability allows clinicians to make immediate decisions during procedures or assessments, which is critical in acute care settings.

Traditional ultrasound probes are often quite bulky because each transducer element must be individually connected to a coaxial cable, which then interfaces with channels on an external imaging system. These probes typically utilize 1D transducers to generate 2D cross-sectional images. The transducer emits acoustic waves into the body and records the returning echoes. The depth of an echo is determined by its arrival time, while the lateral resolution of objects or scatterers is achieved through beamforming. In 2D ultrasound imaging, a single plane of the body is captured, producing detailed two-dimensional cross-sectional views [4]. This technique is highly effective for real-time monitoring and diagnosis, providing detailed visualizations of organs and tissues. It is particularly valuable in obstetrics for monitoring fetal development and in cardiology for assessing dynamic heart structures and functions.

In contrast, 3D ultrasound imaging expands on the capabilities of 2D imaging by creating a three-dimensional representation from multiple 2D images taken at different angles [4][5]. This approach offers a more comprehensive view of anatomical structures, adding depth and spatial context that 2D imaging lacks. 3D ultrasound is increasingly used in obstetrics for detailed fetal imaging and in cardiology to visualize complex heart structures and diagnose conditions such as congenital heart defects.

For 2D imaging, 1D arrays, such as linear or phased arrays with up to 256 elements [6], are typically used. To produce 3D images, 2D matrix transducer arrays are employed. For

these arrays to achieve high resolution, the element pitch must be kept minimal to avoid grating lobes, while the aperture should be large enough to capture detailed images, necessitating the use of thousands of transducer elements. Conventional 2D probes typically use fine-gauge micro-coaxial cables to connect each transducer element, but as 2D arrays expand in size, accommodating the necessary cables within small devices like catheters becomes increasingly impractical [7].

The practical implementation of fully-sampled 2D arrays in miniature ultrasound probes became feasible with the introduction of subarray receive beamforming [8], which allows for significant cable reduction by incorporating electronics directly into the probe. In conventional 2D imaging systems using 1D phased-array transducers, receive beamforming is typically conducted in the back-end imaging system, where electrical delays are applied to echo signals from individual transducer elements, and these signals are coherently summed to form an acoustic receive beam.

However, for 2D arrays with a large number of elements (hundreds or thousands), directly implementing beamforming within the probe would require extremely long delay lines, leading to prohibitively high hardware costs. To address this, subarray beamforming splits the necessary delays into two stages: a fine delay implemented within the probe with short delay lines and a coarse delay handled by the back-end system. This approach reduces the complexity and power requirements of in-probe electronics, making the use of dense integrated circuits more practical.

For miniature 3D ultrasound probes, where space is highly limited, custom-designed front-end Application-Specific Integrated Circuits (ASICs) are used [9]. These ASICs integrate closely with the 2D transducer array, enabling efficient signal processing and performance optimization. A typical front-end ASIC based on subarray beamforming includes high-voltage transmitters for generating acoustic waves and low-voltage receivers for signal conditioning and beamforming. The signal conditioning circuits within these ASICs often feature a wide range of programmable gain levels, essential for compensating ultrasound wave attenuation and enhancing the dynamic range.

One of the key roles of the ASIC in ultrasound systems is in the Analog Front End (AFE), which is the central block of the receive chain. The AFE is responsible for processing the weak echo signals received by the transducer elements, which involves several critical steps such as amplification, filtering, and analog-to-digital conversion. The performance of the AFE directly impacts the overall quality and resolution of the ultrasound images.

Within the AFE, a time-gain compensation (TGC) and low-noise amplifier are particularly important subcomponents to compensate for the ultrasound wave attenuation. The LNA, on the other hand, is responsible for amplifying the very weak signals captured by the transducer with minimal noise addition.

This work presents the design of a low-noise, area, and power-efficient LNA with built-in TGC functionality, carefully biased to ensure stability across various operating conditions. Additionally, the design addresses PVT (Process, Voltage, and Temperature) variations, incorporating mechanisms to maintain consistent performance despite these fluctuations. The integration of TGC directly within the LNA not only optimizes the overall size and

power consumption but also enhances the robustness of the design against environmental and manufacturing variations.

1.2 ULTRASOUND IMAGING SYSTEMS

Figure 1.1 presents a block diagram of a standard ultrasound imaging system interfaced with a probe that contains an array of N transducer elements. Each of these elements is dual-purpose, functioning to both the transmission of acoustic waves into the body and the reception of the echo signals reflected back from various tissues. During the transmission phase, pulses generated by a TX beamformer are used to control the timing of the transducer elements, focusing the acoustic wave at a specific point along the scan line to be imaged. To ensure that echo signals can be detected even at significant depths, where signal attenuation is substantial, the transducer elements are driven by high-voltage (HV) pulses—ranging from tens of volts to over 100V. These HV pulses are directed through transmit/receive (T/R) switches, which safeguard the sensitive receive circuitry during the transmission phase.

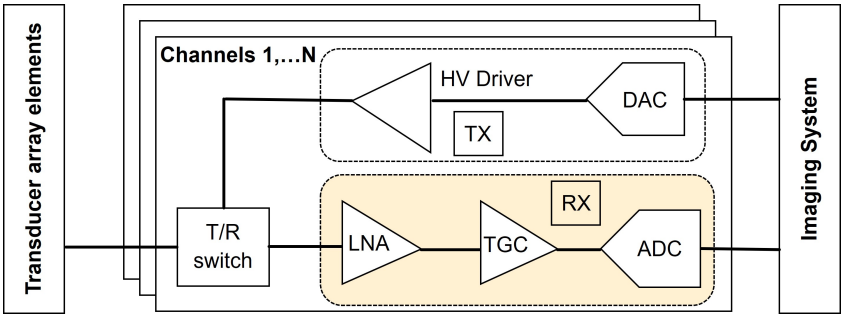


Figure 1.1: Block diagram of a conventional ultrasound imaging system [6]

Upon transmitting the ultrasound signals, the echo signals received by each transducer element are initially amplified by a low-noise amplifier (LNA). In attenuating tissues, such as those found in the human body, the earliest returning echoes come from scatterers located near the surface, which results in higher signal amplitudes. Conversely, echoes originating from deeper scatterers undergo greater attenuation due to the increased travel distance, leading to significantly lower amplitudes [10]. To compensate for this attenuation and ensure uniform signal strength, a time-gain compensation (TGC) amplifier is employed. The TGC amplifier incrementally increases the gain over time, effectively reducing the dynamic range of the signals and ensuring that echoes from deeper structures are adequately amplified. Once the echo signals have been appropriately amplified, they are converted into digital form by an analog-to-digital converter (ADC), typically after passing through an anti-aliasing filter to prevent high-frequency noise. The digitized signals are then processed by an RX beamformer.

The beamformer uses a delay-and-sum method to coherently align and combine signals. This technique enhances the signals from the targeted focal point while diminishing interference from other areas [10]. The signals processed by the RX beamformer are then used

to generate an image. In brightness-mode (B-mode) imaging, both the transmission (TX) and reception (RX) beamformers are precisely focused on a specific point along a scan line within the tissue. The brightness of the image at each point along this line is determined by applying envelope detection to the output of the RX beamformer. This process is repeated across multiple scan lines, with each line requiring its own cycle of pulse transmission and echo reception. The combination of these scan lines ultimately reconstructs the full image, providing a detailed visualization of the internal tissue structure.

1.3 TIME-GAIN COMPENSATION

As the transmitted ultrasound waves penetrate various tissues, they gradually lose energy due to absorption and scattering. This energy loss leads to a reduction in the amplitude of the returning echoes, with the effect becoming more pronounced at greater depths. Without proper compensation, the signals from deeper structures would be significantly weaker, resulting in a loss of image clarity and important diagnostic information. It is clear that the attenuation of ultrasound signals is exponential or linear in dB, proportional to both frequency and the signal travel distance.

To mitigate this, TGC dynamically adjusts the gain applied to the received signals over time. Illustrated in Figure 1.2, the instantaneous dynamic range, defined as the ratio of the largest to the smallest echo-signal amplitudes, remains constant. However, due to signal attenuation, the overall dynamic range exceeds the instantaneous dynamic range significantly. A typical reflected ultrasound signal may exhibit an instantaneous DR of up to 60 dB. When attenuation of 40-50 dB is added, the overall dynamic range surpasses 100 dB [11]. Such a DR exceeds the capability of many standard ADCs, such as a 12-bit ADC that typically has an SNR of around 74 dB [12]. As a result, Time Gain Compensation (TGC) is essential to reduce the overall dynamic range of the output signal. Ideally, the TGC compensates for signal attenuation, ensuring that the overall DR matches the instantaneous DR. The signal attenuation over time is compensated by an ideal linear gain in dB to achieve a constant output amplitude envelope.

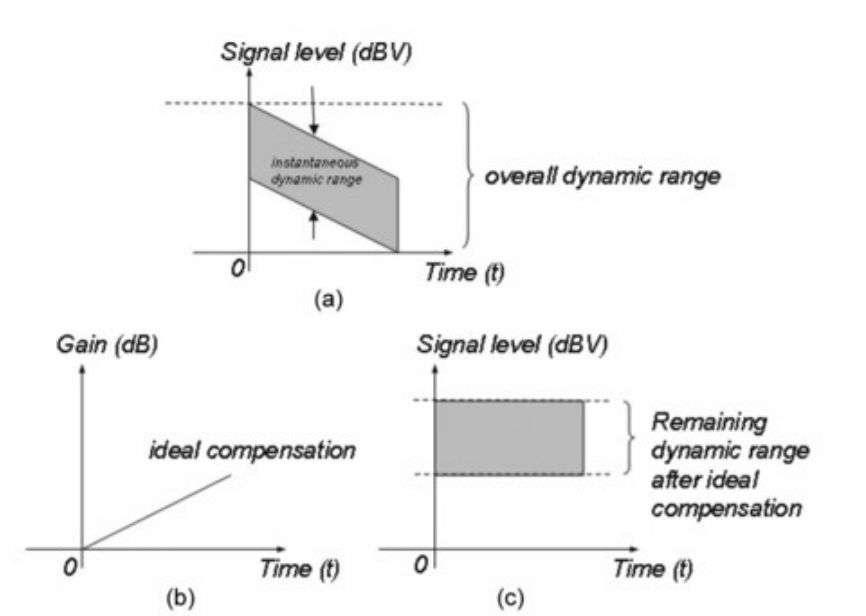


Figure 1.2: The time-gain-compensation scheme and dynamic range: (a) overall dynamic range at the input signal; (b) ideal compensation scheme; (c) output dynamic range after ideal compensation [13]

1.4 MOTIVATION

Figure 1.1 illustrates that in conventional ultrasound imaging systems, TGC is typically performed after the LNA, which implies the need for a power-hungry LNA that can handle the full dynamic range of the echo signal at its output. One major drawback is the increased power consumption, as the LNA must be designed to handle the entire dynamic range of the incoming signals before any gain adjustments are made by the TGC. This typically necessitates a power-hungry LNA, which can be inefficient and less suited for applications where power conservation is critical. Additionally, when TGC is applied after the LNA, any noise introduced by the LNA is also amplified, potentially degrading the overall signal-to-noise ratio (SNR). Moreover, placing the TGC after the LNA can limit the effectiveness of noise reduction, as the LNA's gain is fixed and optimized for low noise. This makes the noise requirements for subsequent stages, including the TGC circuit, more demanding. As a result, additional noise from these later stages can further reduce the overall SNR, especially in low-signal conditions where precise gain control is critical. This can be particularly problematic in sensitive applications like ultrasound imaging, where maintaining a high SNR is crucial for accurate signal interpretation. Moreover, the separation of LNA and TGC stages increases the complexity of the design, requiring more components and interconnections.

Given these disadvantages, our design opts for an LNA with built-in TGC illustrated in Figure 1.3, which allows for more efficient power usage, better noise performance, and a more compact and simplified design. This integrated approach enables dynamic gain control early in the signal chain, optimizing the system's ability to handle wide dynamic

ranges while maintaining a high SNR, ultimately leading to improved overall performance in demanding applications like ultrasound imaging.

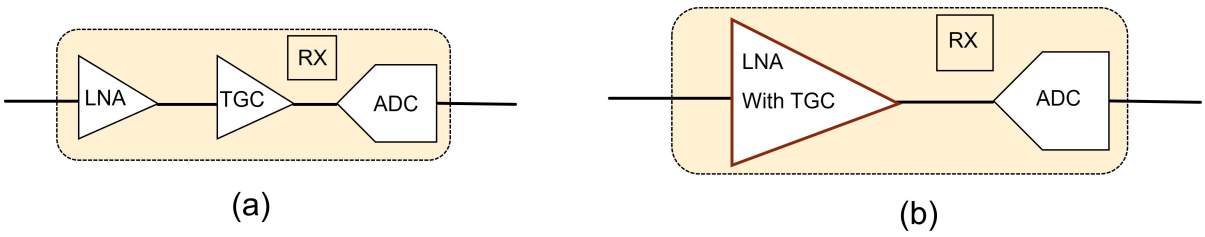


Figure 1.3: (a) Block diagram of the conventional solution of an LNA followed by a TGC amplifier. (b) Block diagram of the proposed LNA with embedded TGC function.

The integration of Time Gain Compensation (TGC) with Low-Noise Amplifiers (LNA) is a challenging design problem that has seen limited exploration in the literature, primarily due to the complex trade-offs involved. Previous studies have explored combined analog front-end (AFE) structures, but each presents its own limitations. While [14] presents one such combined TGC-LNA amplifier, the design is too large for use in miniature 3D imaging probes, which require smaller pitch sizes. The difficulties in combining TGC and LNA functionality arise from the need to balance variable gain control with low noise performance. LNAs typically require high gain to suppress the input-referred noise of subsequent components in the signal chain, but TGC demands variable gain—high for low input amplitudes and lower for larger input currents. This variation in gain can introduce noise performance issues, particularly at lower gain settings. Additionally, maintaining consistent bandwidth while varying gain is critical to avoid signal distortion, yet this can lead to stability problems, as varying impedance values can cause significant shifts in frequency response.

Our motivation in this work is to develop a pitch-matched AFE design that not only addresses the challenges of combining TGC with LNA—such as noise performance, bandwidth, stability, and linearity—but also optimizes power efficiency and minimal die area. Additionally, we aim to solve the critical issue of process, voltage, and temperature (PVT) variations, which can further complicate the design and performance of combined TGC-LNA amplifiers. By overcoming these challenges, we seek to contribute a robust, power-efficient solution that meets the demanding requirements of modern ultrasound imaging systems.

1.5 DESIGN OBJECTIVE

Such design structure has been proposed by [15] and [16], to extend the previous works, this work proposes an LNA-TGC implemented using TSMC 0.18 µm MS technology with a $\pm$0.9 V power supply. The design specifications are detailed in Table. Given the focus on creating a viable solution for miniature 3D probes, minimizing both area and power consumption are top priorities. In previous work [16], the design consumed 6 mW of power. Our goal is to design an LNA with integrated TGC functionality that occupies a

Table 1.1: Target Performance Specification

Input center frequency	7.5 MHz
Bandwidth	5-10 MHz
Gain range	40 dB
Gain error	$\pm$ 1dB
THD	<-40 dB
Peak input signal amplitude	50 μA - 0.5 μA
Receive time period	100 μs
Input referred noise density	1 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$ at 7.5MHz

lower power consumption while maintaining the noise and other performance functionality. Consequently, the design trade-offs are primarily centered on reducing area and power consumption.

Additionally, total harmonic distortion (THD) is considered in the design, as maintaining linearity is crucial for the performance of the LNA-TGC.

1.6 THESIS ORGANISATION

This thesis introduces a variable-gain low-noise amplifier (LNA) equipped with a continuous Time-Gain Compensation (TGC) function. The proposed amplifier is engineered for low power consumption and compactness, making it particularly suitable for integration into miniaturized ultrasound probes.

The thesis is structured as follows: Chapter 1 provides an overview of the research conducted on ultrasound imaging systems, outlines the motivation behind this work, and details the specific design objectives. Chapter 2 offers a literature review of existing LNA designs that incorporate TGC functions, discussing their advantages and limitations, and identifying gaps in the current research. In Chapter 3, the architecture of the proposed LNA is presented, followed by Chapter 4, which delves into the circuit-level implementation of this architecture. Chapter 5 then examines the performance and results of the design. Finally, Chapter 6 presents the conclusions drawn from the research and the future work.

2

LITERATURE REVIEW

The Time Gain Compensation (TGC) amplifier is a specialized form of Variable Gain Amplifier (VGA) designed to adjust its gain dynamically over time. This capability is particularly crucial in ultrasound imaging, where the amplitude of returning echo signals diminishes as they travel deeper into the body. This reduction in signal strength, which occurs in a dB-linear fashion over distance, is due to the exponential attenuation of the sound wave as it penetrates through tissue layers. Assuming a consistent speed of sound, this attenuation leads to a progressively weaker input signal, which ideally requires a corresponding gain increase that follows an exponential pattern.

However, creating a circuit that provides an exact exponential gain response as a function of time presents significant design challenges. To address these challenges, various TGC amplifier designs have been developed, employing different methods and architectures. This chapter aims to review these existing designs by exploring their architectural principles and functional approaches, while also identifying the gaps that this thesis seeks to address.

Various approaches have been taken to realize the amplifiers suitable for the TGC. They can globally be divided into two groups: amplifiers with discrete gain steps, and amplifiers with continuous gain control.

2.1 DISCRETE TIME GAIN COMPENSATION

Amplifiers with discrete gain steps approximate the ideal exponential gain curve by sequentially applying a series of distinct gain levels. One of the key advantages of this approach is the precision with which these gain steps can be defined, typically through digitally programmable feedback networks. This programmability allows for fine control over the gain levels, ensuring that the steps are accurately implemented.

However, transitioning from one discrete gain step to another can introduce switching transients, which may manifest as artifacts in the ultrasound image at the depth corresponding to the moment of gain switching shown in Figure 2.1. This results in the unmatched signal level between instantaneous DR and overall DR. These artifacts can be minimized by reducing the size of each gain step, but this solution necessitates a large number of steps to cover the entire gain range. Consequently, this increases the circuit complexity and requires more die area to implement.

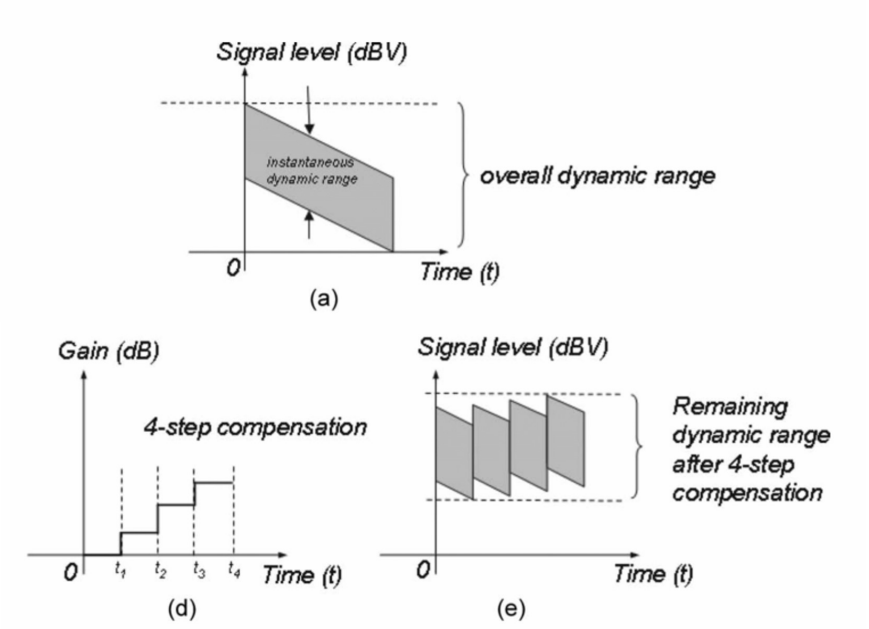


Figure 2.1: Discrete gain variations and instantaneous dynamic range after discrete gain steps.

The transition between gain steps introduces a certain amount of latency, which can be a limitation in real-time applications like ultrasound imaging, where quick and accurate gain adjustments are needed to maintain image quality as the depth of the scanned tissue changes. Besides, the artifacts can negatively impact the quality of ultrasound images, as the switching occurs at specific moments during signal processing. In B-mode imaging, improper TGC can cause variations in image brightness due to mismatches between gain compensation and signal attenuation. Since time correlates with image depth in ultrasound imaging, the artifacts manifest at particular depths corresponding to the gain-switching points. Larger gain steps typically lead to more pronounced settling artifacts, which can degrade the image quality.

Despite these challenges, discrete gain steps remain a popular choice in TGC implementations due to their established presence in the literature and their ability to be adapted for continuous gain variation through the use of analog control signals instead of digital ones. This adaptation can help reduce the impact of switching artifacts and improve the overall performance of the TGC function.

The following section will explore common architectures for implementing TGC with discrete gain steps, examining their strengths, weaknesses, and potential modifications to enhance performance.

2.1.1 *Digitally Programmable Resistive Network*

The TGC amplifier proposed in [17] employs an open-loop amplifier topology, which is chosen to achieve a high bandwidth while keeping power consumption low. In Figure 2.2 the gain is set by $2\mathrm{R_L}/\mathrm{R_S}$.The amplifier consists of a voltage-to-current (V/I) converter and a current-to-voltage (I/V) converter. By switching between different degeneration resistors, the amplifier can achieve discrete gain steps (e.g., 0 dB, 12 dB, 26 dB, and 40 dB). However,

this might result in less precise compensation for signal attenuation, potentially affecting the uniformity of the final image quality.

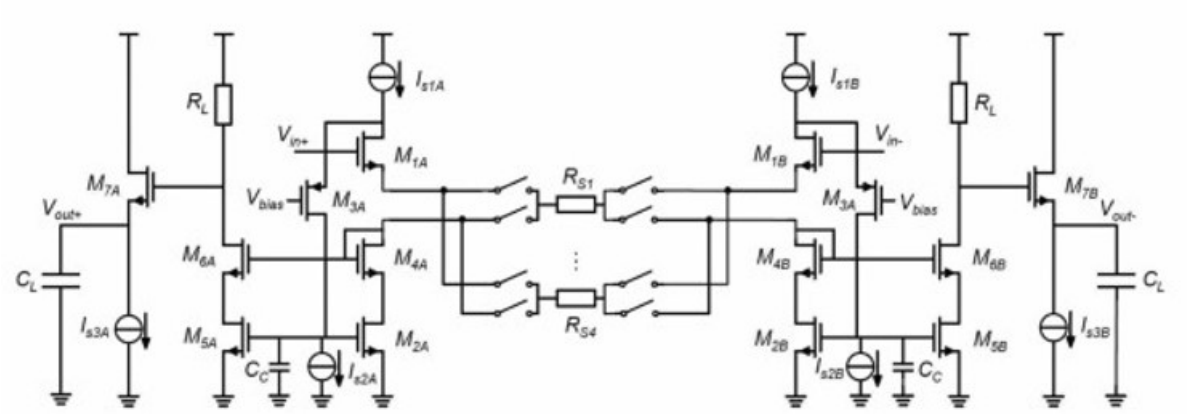


Figure 2.2: Open loop amplifier with digitally programmable degeneration resistors [17]

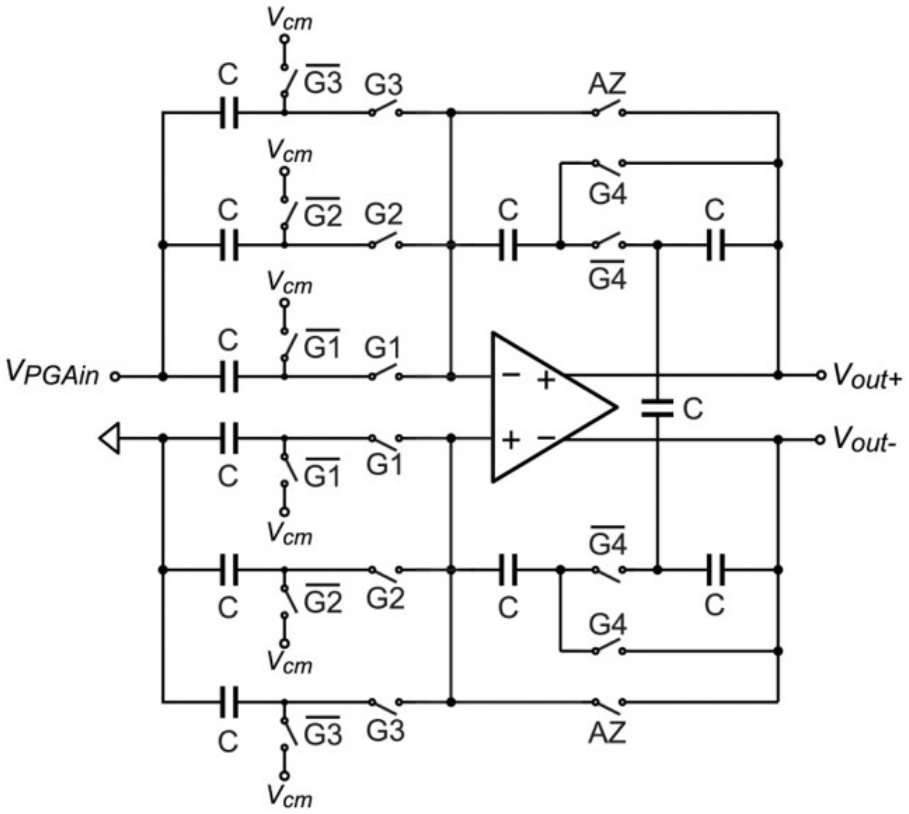
In an open-loop amplifier configuration, the amplifier operates without any feedback, meaning that the output is not influenced by the input signal after amplification. While this setup can provide high gain, it has limitations, such as sensitivity to component variations, increased distortion, and potential instability.

To address these issues, a closed-loop configuration is often employed. In [18], the gain is precisely controlled by adjusting the resistance in the feedback loop through the resistive arrays. Though the benefit is that the feedforward and feedback path can be separately designed, the power is a huge expense. The limited gain resolution provided by the 6-bit control may not be sufficient for applications requiring precise gain adjustments. Additionally, operating in the subthreshold region, while power-efficient, increases sensitivity to process, voltage, and temperature variations, potentially complicating the design and requiring compensation mechanisms to maintain consistent performance. The power vs. performance trade-off is also evident, as achieving low power consumption can result in compromises in speed, linearity, and noise margin. Furthermore, the fixed gain steps inherent in the resistive array approach may not allow for the smooth and continuous gain variation needed in some applications, and the lower transconductance in subthreshold operation could lead to higher noise levels, which is critical in low-noise applications.

2.1.2 *Capacitive Feedback Network*

To address the issue of high noise levels associated with resistive feedback, one alternative is to use capacitive feedback, which can provide a more stable and lower-noise performance [19][20]. Figure 2.3 shows the fully differential amplifier with a digitally programmable capacitive feedback [21]. The PGA employs a programmable capacitor network as the feedback element across a differential telescopic amplifier. This network is designed to provide different gain levels by selecting specific capacitance values, allowing the amplifier to achieve discrete gain steps. The feedback capacitors are arranged in a T-type network, which helps save space on the chip while providing the desired gain levels. The gain of

the amplifier is defined by the ratio of the capacitors in the feedback network to the input capacitance. By switching different capacitors into the feedback path, the gain can be adjusted in predefined steps, from 6 dB to 24 dB, with the specific gain determined by the control code applied to the capacitor network. Capacitive feedback is generally associated with lower noise levels compared to resistive feedback, which is beneficial for maintaining signal integrity in sensitive applications. However implementing a programmable capacitive feedback network can add complexity to the design, particularly in ensuring that the capacitors match precisely and that the switching introduces minimal noise or distortion. Although capacitive feedback is space-efficient, the need to implement a network of capacitors with fine resolution can still be challenging in terms of chip area and power consumption.



	G1	G2	G3	G4
6 dB	0	1	1	1
12 dB	0	1	0	0
18 dB	0	1	1	0
24 dB	1	1	1	0

Figure 2.3: Fully differential programmable gain amplifier with capacitive feedback [21]

2.1.3 *Current Steering*

Figure 2.4 shows that the current steering approach involves controlling the distribution of current between different branches of a circuit to vary the effective gain. This is done by steering currents through programmable resistive paths, which are controlled by an

exponentially scaled control voltage. By directing the current through different paths, the gain of the amplifier can be adjusted in discrete steps. The gain in a current-steering VGA is defined by the ratio of currents that are directed through different branches of the circuit. By adjusting the control voltages that determine which switches are on or off, the amount of current flowing through each branch changes, thus modifying the gain. The relationship between the control voltage and the resulting gain is designed to be linear in decibels (dB), which is often desired in applications requiring smooth gain control.

This method can contribute to lower noise levels in the circuit, as the noise performance is largely dependent on the quality of the switches and the design of the current paths, whereas carefully tuning the switch control and current paths brings complexity to the system and may increase the overall power consumption. The paper highlights that one of the main challenges with current-steering VGAs is the degradation of linearity when dealing with large input signal swings. This can affect the performance of the VGA, particularly in applications that require high linearity across a wide range of signal levels. Another significant drawback is the variation in DC offsets across different gain settings. As the gain is adjusted by steering current through different paths, the DC offset can change, potentially leading to performance issues, especially in sensitive analog circuits. Besides, any noise present on the control voltage, which is used to steer the current and control the gain, can be amplified and result in noise current flowing to the output. This can degrade the signal-to-noise ratio (SNR) of the VGA.

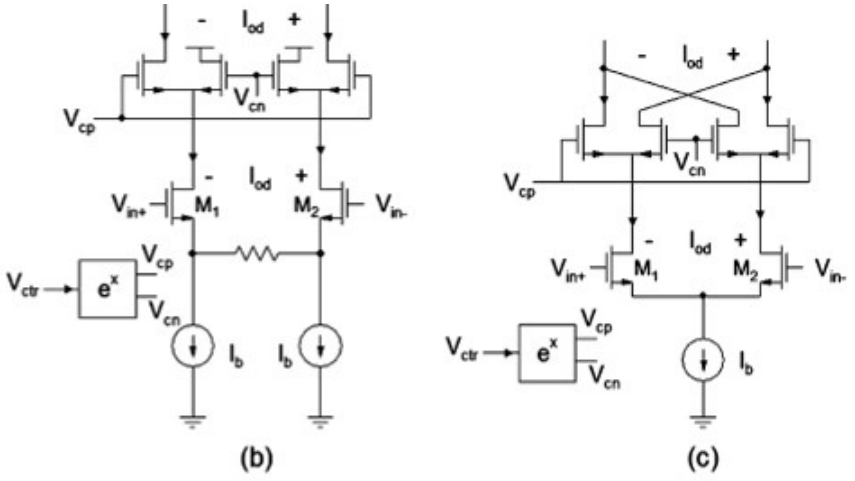


Figure 2.4: (b) Current steering. (c) Differential current steering. [22]

2.2 CONTINUOUS TIME GAIN COMPENSATION

An amplifier with continuous gain control, also known as a Variable Gain Amplifier (VGA), allows its gain to be adjusted by an analog control input, typically a control voltage. The gain of these amplifiers is often (approximately) exponentially related to the control voltage, which facilitates linear dB gain control. By gradually increasing the control voltage as a function of time, the gain can be swept across the desired range to achieve Time Gain Compensation (TGC) without the drawbacks associated with discrete gain steps.

There are two primary methods to achieve this:

- Amplifiers designed with a transfer function that approximates an exponential response.
- Amplifiers that interpolate between discrete gain steps to provide a continuous gain variation.

2.2.1 *Exponential Functionality*

Amplifiers that approximate an exponential transfer function often utilize the nonlinear characteristics of MOSFETs or bipolar transistors to achieve variable gain. For instance, this can be accomplished by adjusting the operating point of a differential pair in response to the gain control voltage, resulting in a variable transconductance. Additionally, incorporating a load whose impedance depends on the same control voltage, such as by altering the operating point of a diode-connected transistor, can produce an amplifier with a nonlinear transfer function, as illustrated in Figure 2.5 [23].

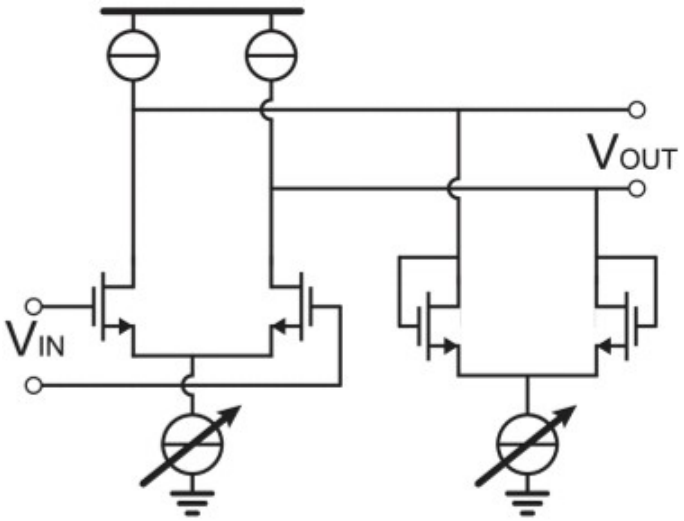


Figure 2.5: Diode-connected load and bias current variation [23]

Moreover, the approximation can also be realized using a circuit where a variable current ratio controls the gain. As shown in Figure 2.6 [24], this ratio is generated by a control circuit that manipulates the currents through specific transistors to follow the desired exponential function closely. The gain of the VGA is defined by the ratio of the currents in the control transistors, which are adjusted by the control voltage. This relationship is designed to be linear in decibels (dB), meaning that a change in the control voltage results in a corresponding exponential change in the gain.

The exponential approximation allows for a very wide gain range, in the case in [24] up to 95 dB, but it only approximates an exponential across a limited gain range. The power consumption is optimized low, which is 6.5mW under 1.8V. However, the gain is sensitive to temperature variations, which can lead to deviations in the expected gain

range. This requires additional circuitry or design considerations to mitigate. Also, the design can be affected by variations in the manufacturing process, which may shift the gain characteristics and require calibration or compensation techniques.

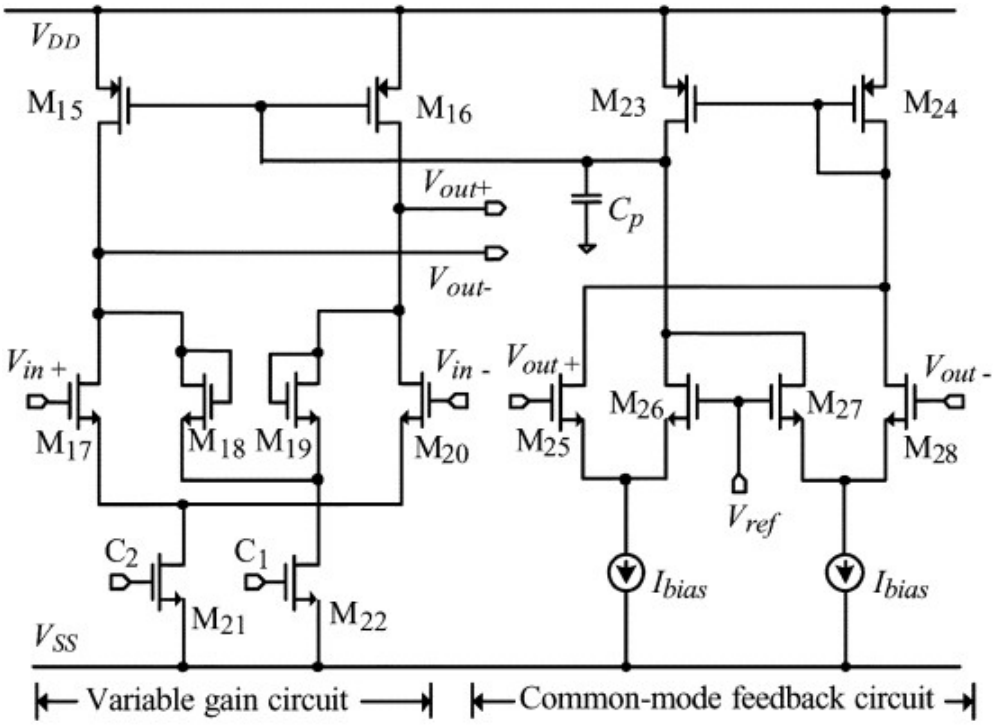


Figure 2.6: The amplifier gain varied by controlling the current [24]

Another approach to achieving a purely exponential transfer function is to leverage the inherent properties of BJTs [25] or MOSFETs operating in the sub-threshold region. The approximation is achieved by manipulating the transconductance of MOS transistors, which are inherently nonlinear, to closely follow the desired exponential function [26]. Figure 2.7 shows the unit cell, by using the combination of NMOS and PMOS transistors, the gain is controlled by tuning the body bias voltage of the PMOS transistors. The voltage gain is simply the transconductance ratio of input pairs and load transistors. The gain can be approximated as:

$$A_v \approx \frac{g_{m5,6}}{g_{m1,2} + g_{m3,4} - \frac{2\Delta I_{DS3,4}}{nV_T}}$$

However, it also introduces challenges related to design complexity, temperature sensitivity, and process variation.

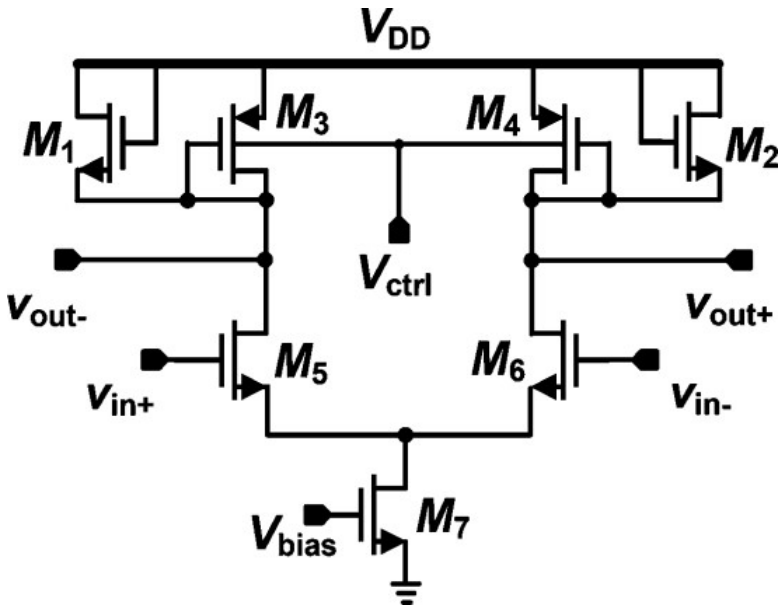


Figure 2.7: Schematic of the unit cell with the body of PMOS tuned [26]

Another method for approximating an exponential transfer function involves using a positive feedback amplifier, which produces an output voltage that increases exponentially within a defined time window [27]. The core of the Programmable-Gain Amplifier (PGA) uses a cross-coupled pair arrangement, which is well-known for its regenerative properties. The regeneration in this circuit leads to an exponential increase in the output voltage, which naturally lends itself to dB-linear gain control. The gain control is achieved by adjusting the regeneration time constant τ_{reg}, which is related to the sampling capacitors and the transconductance of the cross-coupled pairs. By varying the duration of the regeneration phase $\mathrm{T_{reg}}$, the amplifier can achieve a continuous range of gain levels that follow an exponential relationship, which can be expressed by:

$$\mathrm{G} = \mathrm{e}^{\frac{\mathrm{T_{reg}}}{|\tau_{\mathrm{reg}}|}}$$

By linearly varying $\mathrm{T_{reg}}$, the gain changes exponentially. However, this technique requires sampling the input signal at the amplifier's input. By doing so, the positive feedback amplifier can amplify each successive sample, with the gain for each sample being controlled by adjusting the length of the positive feedback time window. The performance of the amplifier, particularly the signal-to-noise ratio (SNR), is sensitive to timing jitter in the control signals.

2.2.2 *Continuous Interpolation*

[28] describe a TGC amplifier topology that interpolates between discrete gain steps. As shown in Figure 2.8, the input signal is attenuated by a resistive ladder network, with each segment of the network providing a fixed attenuation step in dB, which are then fed into a fixed-gain amplifier with multiple input stages. Interpolation comes into play by blending the output from adjacent taps of the resistive ladder. By smoothly transitioning between

the outputs of two consecutive taps, the VGA can achieve a gain level that lies between the discrete steps provided by the ladder.

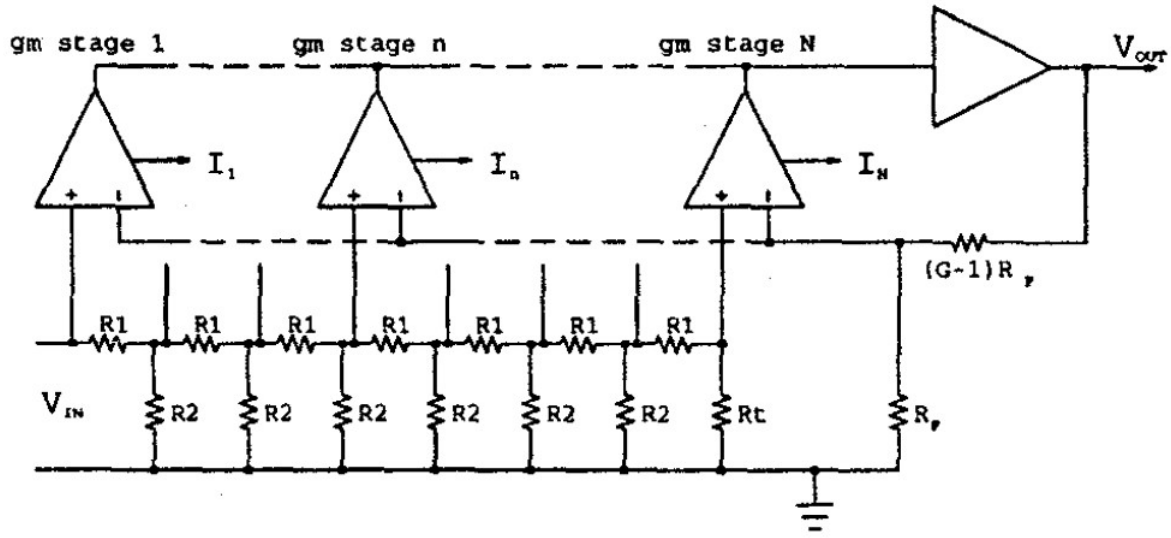


Figure 2.8: Amplifier that interpolates between the outputs of a resistive ladder attenuator[28]

Another approach in [29] allows the gain to be adjusted in large discrete steps using digital controls. A voltage-controlled current attenuator (VCCA), adjusts the effective gain by varying the current that is steered between different paths in the circuit. used current steering to control how much of the output current of the current produced by these input stages is added to the output. By controlling the interpolation factor, the VGA can smoothly adjust the gain between the predefined discrete levels.

In [22] the gain is controlled by employing a differential ramp-based approach. Multiple unit elements, each with a specific resistance, are connected in parallel as shown in Figure 2.9. The control voltage is applied as a ramp to these elements, with the ramp voltage increasing or decreasing the resistance of the elements, thereby adjusting the gain. Interpolation is achieved by varying the ramp voltages and effectively utilizing multiple switches simultaneously in such a way that the resistance changes gradually. This allows the gain to be adjusted continuously, rather than in discrete steps. However, this comes at the price of quite an extensive feedback network. It is area-cost. Moreover, the effectiveness of the interpolation depends on the matching of the unit elements and the accuracy of the ramp voltages, making the design sensitive to process variations and temperature changes. There is an alternative technique that achieves similar results by employing current steering, the point at which feedback is applied can be continuously adjusted [14]. This continuous alteration of the feedback point results in a smoothly varying gain.

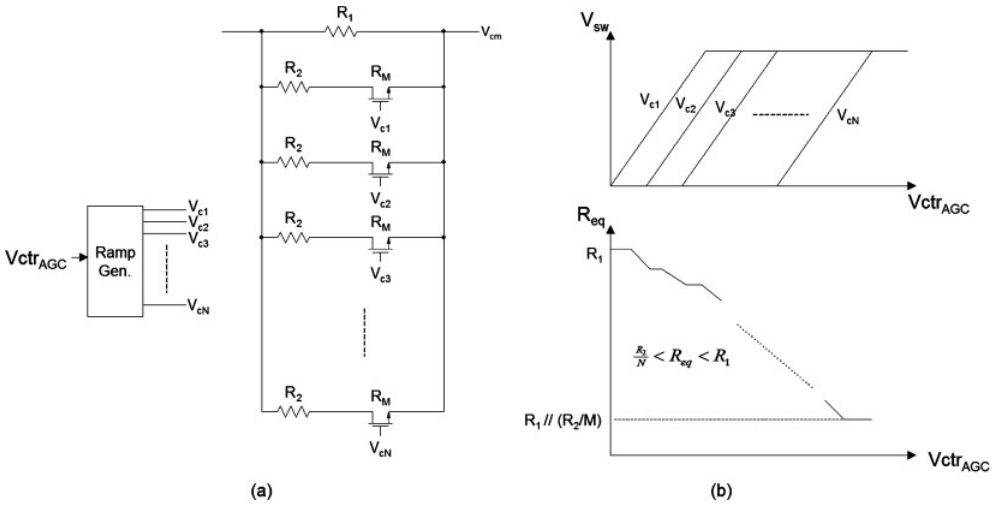


Figure 2.9: (a) Multiple unit elements combined in parallel. (b) Variation of the equivalent resistance with the AGC control voltage. [22]

When using the approach illustrated in Figure 2.10, where interpolation is used, the effective impedance is adjusted. A capacitive ladder feedback network combined with a current-steering mechanism is used to realize interpolation between discrete gain steps. The capacitive ladder provides a series of discrete gain levels. Each gain step consists of ladder capacitors $\mathrm{C_A}$ and $\mathrm{C_T}$ to provide the current gain of $1 + \frac{\mathrm{C_T}}{\mathrm{C_A}}$. The current-steering network then interpolates between these levels by gradually shifting the current from one node of the ladder to another. This approach allows for a quasi-continuous adjustment of gain by controlling the distribution of current across the ladder. As the control voltage varies, the current is steered progressively from one capacitive ladder tap to the next, resulting in smooth transitions between the discrete gain levels.

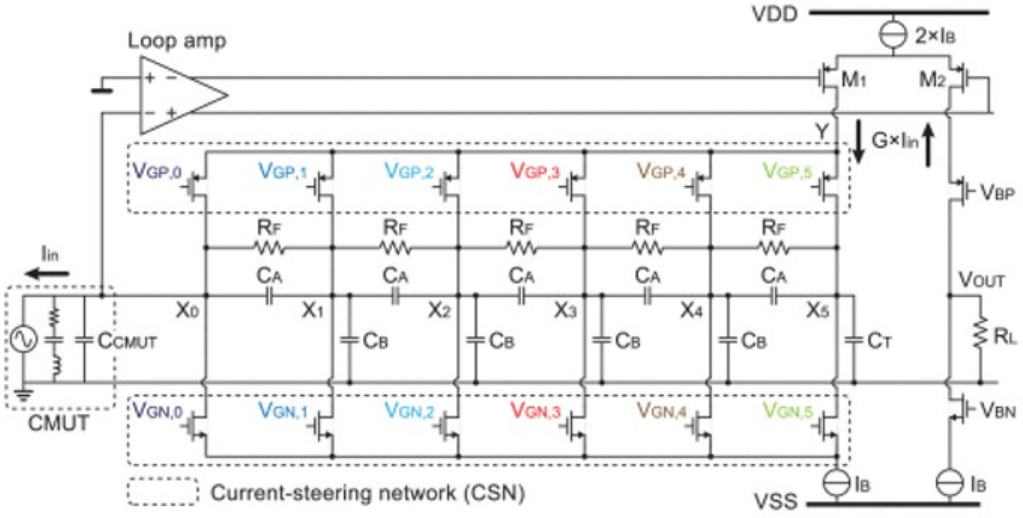


Figure 2.10: Continuous interpolation by means of current steering [14]

2.2.3 *Previous Works*

Inspired by [14], [15] proposes a variable-gain low-noise trans-impedance amplifier to also combine both the LNA with the TGC functionality which utilizes the same input transducer. The overall schematic of the TIA with a pseudo resistor is illustrated in Figure 2.11. The continuous time gain in the TGC-LNA is achieved through the use of an exponentially varying feedback impedance. Specifically, this is implemented using MOS transistors operating in the triode region as voltage-controlled resistors. The impedance of these transistors can be controlled by varying the gate-source voltage, an exponentially decaying voltage over time, the impedance of the transistor increases exponentially. Since there are multiple branches of triode devices to achieve the overall continuous gain range over time, no interpolation methods are needed such as current steering compared to [14].

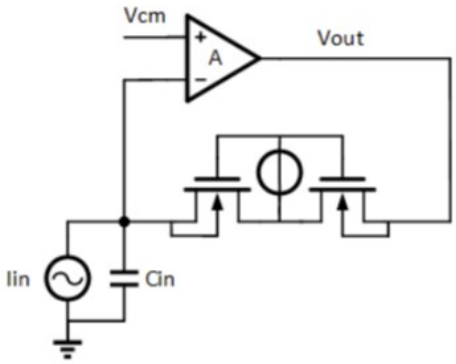


Figure 2.11: Transimpedance amplifier with pseudo resistor configuration [15]

The exponential voltage generator comprises a pre-charged capacitor and a big resistor, the combination resulting in the pure exponentially decaying voltage to apply on the pseudo resistors for the continuous gain. The resistor in the order of MΩ is unrealistic on the chip, so it is replaced by a PMOS transistor operating in saturation region so that a constant current can be drawn to discharge the capacitor. Though the resulting voltage is then not pure exponential, it can still mimic the required exponential by careful design.

Figure 2.12 shows the overall loop amplifier. The amplifier used is a two-stage telescopic operational transconductance amplifier (OTA). The first stage is used to optimize noise performance and to control the gain, while the second stage is used to obtain the required loopgain and output impedance for loop stability.

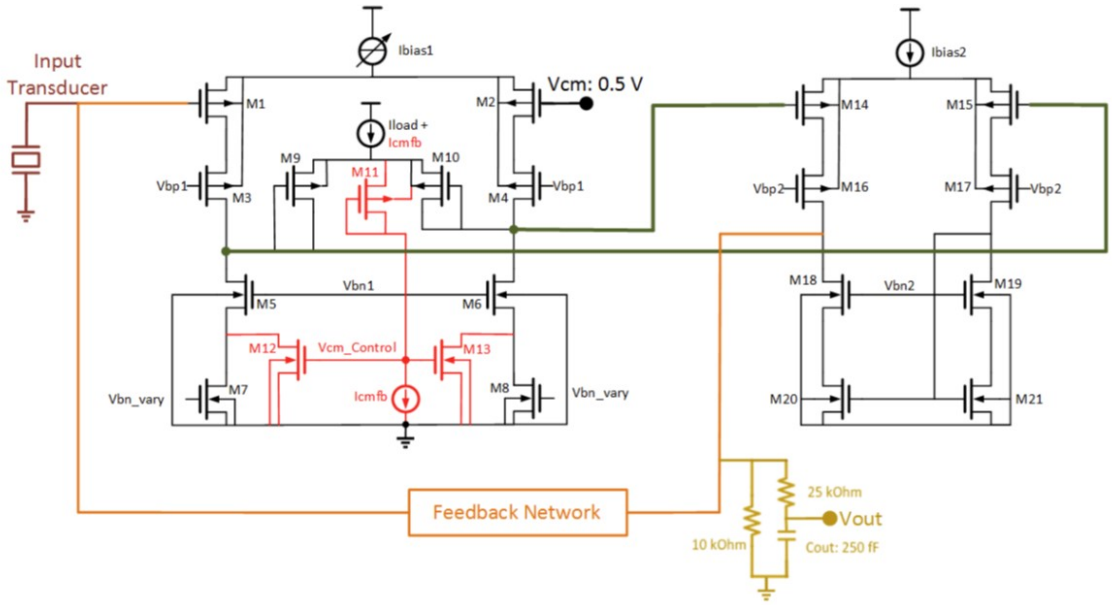


Figure 2.12: Overall loop amplifier, including connections with the input transducer, the feedback network and the output capacitor. [15]

The first stage is made variable to decrease the power consumption and create unity-gain bandwidth. This is done by changing the bias current of the first stage. The CMFB senses the voltage at the source of the load transistors. Since the load current is a constant DC current, the voltage at the source of the load transistors is effectively shifted from the common-mode output voltage by a predictable amount. This shifted voltage is used as an indicator of the common-mode level. The sensed common-mode voltage is then passed through a diode-connected transistor, which drops the voltage by one gate-source voltage. The resulting voltage is used to control the gates of two CMFB control transistors. The Vcm-Control voltage adjusts the gate voltages of these control transistors to stabilize the common-mode voltage at the output. The control transistors work to ensure that any deviation in the common-mode level is corrected by adjusting the bias currents accordingly. However, the variable bias current is designed to linearly depend on the feedback resistance and is then mirrored to the main amplifier. This means that any noise in the variable bias generator is directly copied and amplified in the main amplifier. Even if the initial current noise is minimal, the amplification can significantly increase the noise contribution to the input. Though a low-pass filter is employed, the challenge remains that the varying input transconductance and feedback resistance do not naturally match. Ideally, these two parameters should vary in a synchronized manner to maintain a constant unity-gain bandwidth (UGBW). Unfortunately, as the operating points shift with increasing bias current (Ib), the ratio deviates from the ideal, leading to fluctuations in UGBW and potential instability.

For the second stage, with a large output resistance, the pole presented due to the output capacitance with the output impedance will be at relatively low frequencies. There is a shunt resistance used to provide the resistive broadbanding technique, which is employed to improve the load-driving capability and increase the pole in the loop to higher frequencies to increase loop stability, although it remains limited. Its ability to drive loads

is limited, the output impedance of the loop amplifier should be high to keep the system stable.

Besides, the spot noise density at the center frequency is a fraction larger than the requirements. This can be further improved by the design [16]. The LNA uses the structure of current-reuse amplifiers. The feedforward path comprises a four-stage loop amplifier, optimized for noise requirements in a power-efficient manner by the current reuse amplifier structure. The gain of the loop amplifier varies to maintain a constant UGBW despite the changing feedback resistance. The loop amplifier also have the capability to drive loads effectively, which is achieved through careful design of the output stages.

However, there is still room for improvement. The first is to optimize the gain error, which peaks at the switching moment of resistance in each branch taking over. Additionally, the current design assumes ideal power supplies, which introduces potential vulnerabilities to Process, Voltage, and Temperature (PVT) variations. To enhance the robustness of the circuit, it is necessary to implement improvements that account for these variations. Addressing PVT sensitivity will ensure that the circuit maintains consistent performance under real-world conditions, where fluctuations in power supply and environmental factors can impact the overall reliability and efficiency of the system.

For area estimation, the capacitors in the RC discharge network could be reduced, provided that the mismatch from charge injection remains within acceptable limits. Moreover, there is potential to further enhance the power efficiency of the first stage. While the variable bias current in the first stage currently increases linearly, it could be adjusted to follow an exponential or parabolic curve, maintaining fixed instantaneous transconductance at the highest gain. This adjustment could further minimize power consumption.

3

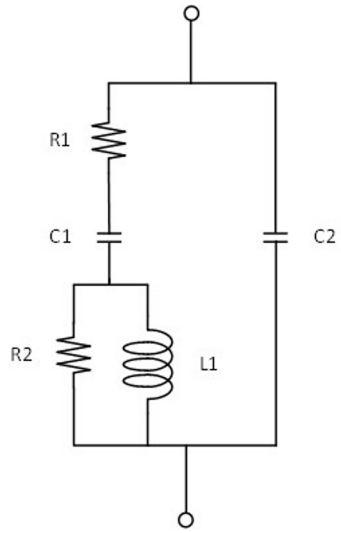
ARCHITECTURE

In this chapter, the architecture of the biasing is designed to be implemented on a low noise amplifier with time gain compensation (LNA-TGC). Starting with the proper signal input source model, a feedback network topology[15] is then designed for TGC functionality while maintaining a relatively small die area. A loop amplifier with a variable gain is then required to adapt to varying feedback resistance while maintaining low power usage.

3.1 MODELING OF TRANSDUCER

The designed TGC-LNA serves as the initial component in the receive path of acoustic echo signals, positioned right after the transducer except for the Transmit/Receive Path (TR switch). The LNA design is critically dependent on the transducer's characteristics. To effectively determine the electrical loading effects at the amplifier's input, a comprehensive examination of the transducer's impedance profile is essential for selecting the optimal LNA topology.

The device in focus for this study is a Capacitive Micromachined Ultrasound Transducer (CMUT), modeled using the Generalized Butterworth-Van Dyke (BVD) Model [30] shown in Figure 3.1, which includes a static capacitive branch and a dynamic RLC branch, with the operational frequency primarily governed by the resonance of the RLC branch. Using the exact CMUT specifications cited in [15], the transducer's central operating frequency is set at 7.5 MHz, with a bandwidth spanning 5-10 MHz. This configuration enables a precise analysis of which branch exerts more significant influence at the resonant frequency, thus informing the tailored design necessary for the most effective LNA topology. By calculation, the capacitive branch has a lower impedance magnitude at the resonant frequency, which means the capacitive branch is the dominant branch.



Component	Value
R_1	1.1mΩ
C_1	16.9kΩ
R_2	2.38 pF
L_1	17.62 pF
C_2	3.1 mH

Figure 3.1: The equivalent Van-Dyke model for CMUT transducers

The transducer impedance around center frequency is calculated to be approximately 1.2 kΩ, which is relatively high. This high impedance level suggests using an amplifier with low input impedance to effectively minimize signal distortion, as a low input impedance amplifier can better handle the high output impedance of the transducer by reducing the voltage drop across the amplifier's input. Consequently, the input signal source is modeled as a current rather than a voltage source. The CMUT transducer is primarily modeled as a large 18 pF capacitor in parallel with a current source for simplicity in subsequent circuit diagrams. The signal current levels decay over time, continuously decreasing from 50 µA to 0.5 µA. This modeling approach is adopted because the total impedance of the transducer is predominantly influenced by this large capacitor, effectively rendering the contributions of the resonant branch negligible in this context.

3.2 TRANSIMPEDANCE AMPLIFIER

Given the relatively high input impedance, the LNA design in this work considers either a Transimpedance Amplifier (TIA) or a Current Amplifier (CA). Since the subsequent analog-to-digital converter stage requires a voltage input, the LNA design must provide a voltage output, necessitating effective current-to-voltage conversion. Therefore, the Transimpedance Amplifier (TIA) is chosen. The optimal gain configuration for the system varies exponentially with time. Achieving this within the TIA topology requires employing a feedback impedance that exhibits an exponential response as a function of time.

Illustrated in Fig 3.2, the chosen TIA employs a closed-loop configuration with resistive feedback, denoted as $\mathrm{R_{fb}}$, with $\mathrm{C_{load}}$ the output capacitance, simplifying the circuit design by optimizing the Low Noise Amplifier (LNA) and Time-Gain Compensation (TGC) functions separately. The feedback controls the gain range, while the feedforward gain path minimizes noise, manages bandwidth, and reduces distortion. This design ensures that the trans-impedance gain closely matches the feedback impedance, especially when the loop amplifier's gain is high, enabling precise control over the gain via an exponentially

varying feedback impedance. Besides, a Variable-Gain Amplifier(VGA) is used as a loop amplifier in this configuration to obtain a gain-independent UGBW to obtain high power efficiency.

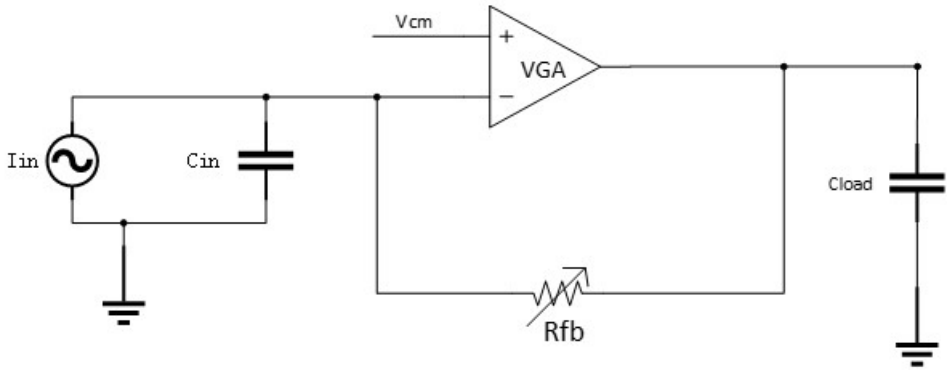


Figure 3.2: General idea of variable-gain-low-noise trans-impedance amplifier

3.3 FEEDBACK NETWORK

As discussed, the TIA topology requires employing a feedback impedance with an exponential dependence on time. In this section, the proper architecture is looked into for realizing an impedance that can change its value exponentially over time.

Considering the benefits of low area compared to the large occupied area by a capacitive feedback array proposed in [14], a resistive feedback network composed of MOS devices used in this work is based on [15]. This scheme creates an exponentially increasing resistance using a MOS transistor with exponentially decaying overdrive voltage in the triode operating region.

3.3.1 *MOS Resistance*

The transistors need to operate in the triode region to operate as controllable resistors, where the drain current [31] is expressed as

$$I_D = \mu_n C_{ox} \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{1}{2}{V_{DS}}^2\right) \tag{3.1}$$

where I_D represents the drain current, μ_n stands for the electron mobility, C_{ox} is the gate oxide capacitance, $\frac{W}{L}$ is the transistor size ratio, V_{GS} the gate-source voltage, V_T the threshold voltage and V_{DS} is the drain source voltage. To mitigate the significant second-order distortion, the quadratic term should be made negligible to avoid the quadratic dependency on the drain-source voltage. This means the device should operate in the deep triode region [31] so that the drain current is expressed by

$$I_D = \mu_n C_{ox} \frac{W}{L}\left((V_{GS} - V_T)V_{DS}\right) \tag{3.2}$$

$$\text{if} \quad V_{DS} < 2(V_{GS} - V_T) \tag{3.3}$$

If the device meets the condition that the drain-source voltage is smaller than two times the overdrive voltage, the minimum overdrive voltage should be two times larger than the limited output swing. In this case, the transistor resistance in the deep triode region can be expressed as:

$$R_{on} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)} \tag{3.4}$$

Reducing the overdrive voltage exponentially allows for exponentially increasing on-resistance, which is crucial for implementing Time-Gain Compensation (TGC) functionality. Ensuring the MOSFET remains in the deep triode region throughout the operation is vital. Failing to maintain this condition can result in the introduction of quadratic terms or, even worse, cause the device to enter the saturation region. The relationship between the output voltage and input current could be disrupted if this occurs.

The condition brings a trade-off between the minimum overdrive voltage and limited output swing. A compromise emerges between expanding the potential resistance range of a transistor and maintaining its linearity performance.

3.3.2 *Linearity MOS Devices*

As revealed from the equation (3.4), the on-resistance depends on the threshold voltage. However, the drain-source voltage may become a nonlinear function due to the body effect, leading to distortion. Given that the input is a pure AC current source, the current reverses direction every half cycle, causing the roles of the drain and source to switch correspondingly. The threshold voltage, which is influenced by the source-bulk voltage V_{SB}, is given by:

$$V_T = V_{T0} + \gamma\left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right) \tag{3.5}$$

In the standard configuration, if only one device is utilized, the side with the lower potential alternates as AC current flows through the triode device, causing the drain and source to switch roles with each half-cycle. This results in the bulk connected to its side of the MOS device, only tracking the source for half the period. This leads to a situation where the on-resistance remains constant for only half of the cycle and varies during the other half. This variability contributes to non-linearity in the overall output.

To enhance the linearity of the triode devices, the configuration of MOS devices can be altered by arranging back-to-back connected in series, with their bulks attached to the external and opposite nodes as shown in Figure 3.3 [15]. The reason for this configuration selection is the resistance changes are equal by both positive and negative AC input currents through series connection and bulk to opposite sides configuration.

This goes for four configurations to choose from: either bulks and floating sources are connected on the same sides or opposite sides. The setup of triode devices with the floating source connected to the middle node is selected under the assumption that the area

required for implementing a separate well for changing bulk connection is smaller than the area required for implementing two floating sources connected to outer nodes by using capacitors. The bulks are connected to the outer nodes also helps to minimize distortion caused by the body effect and elevates the linearity within the feedback network. By balancing the changes in V_{SB}, this modified arrangement of the MOS devices helps stabilize the threshold voltage and minimize nonlinear effects, thus enhancing the consistency and reliability of the circuit's performance.

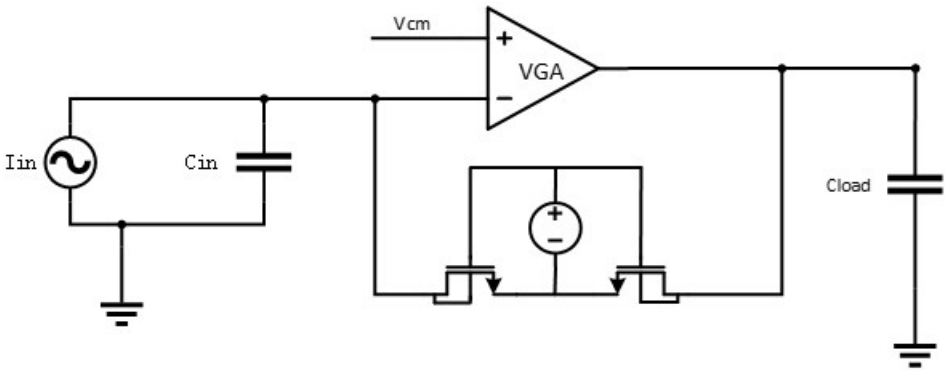


Figure 3.3: TIA structure with back-to-back triode devices configuration with back-to-back bulks-to outer node connection [15]

3.3.3 *Gain Range Feedback Network*

Since linearity has been investigated, the gain range should also be considered. This requires determining the feedback resistance value, which is influenced by two primary considerations. Firstly, the thermal noise generated by the feedback resistors must be minimal to ensure that a substantial portion of the noise budget is reserved for the loop amplifier. The input transducer should dominate the overall output noise, not the TGC-LNA. The noise specification is set as an input-referred current noise density of 1 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$ for the smallest input current. A MOS transistor operating in triode region is as noisy as a standard resistor, with a current noise density of:

$$\mathrm{i_n} = \sqrt{\frac{4\mathrm{kT}}{\mathrm{R}}} \tag{3.6}$$

where R is the equivalent resistance. The operating temperature is set to body temperature since the intended environment for the transducer is inside the human body. If all the noise density arises solely from the resistor, the minimal necessary resistance is calculated to be 17.1 $\mathrm{k\Omega}$. However, to accommodate additional noise contributions from the loop amplifier and to consider the impact of a 17.1 $\mathrm{k\Omega}$ resistor on the output amplitude, which would be just 8.6 mV for the smallest input current of 0.5 $\mu\mathrm{A}$, it is advisable to use a much larger resistance—setting the maximum resistance at about 100 $\mathrm{k\Omega}$, which aligns with leaving approximately 90% of the noise budget for the loop amplifier.

Secondly, the loop gain of TIA structure is defined by the input capacitor$\mathrm{C_{in}}$ and the feedback resistance$\mathrm{R_{fb}}$:

$$\mathrm{Loopgain} = \frac{\mathrm{A_v}}{1 + \mathrm{s} \cdot \mathrm{C_{in}R_{fb}}}$$

Where $\mathrm{A_v}$ is the DC gain of the loop amplifier. For accurate amplification, the loop amplifier needs at least 20 dB of gain, and the dominant pole frequency should be within a reasonable range to ensure stability without excessive power consumption. Considering these factors, the resistance is set at 200 $\mathrm{k\Omega}$ instead of 100 $\mathrm{k\Omega}$ at the higher end, corresponding to a signal swing of about 100 mV. The input pole is defined as:

$$\mathrm{f_{in}} = \frac{1}{2\pi \mathrm{R_{fb}C_{in}}} \tag{3.7}$$

Given that the feedback resistance $\mathrm{R_{fb}}$ is 100 $\mathrm{k\Omega}$ and the input capacitor 18pF, the input frequency is calculated 8.8 MHz, which directly affects the unity-gain bandwidth which will be discussed further in later section 3.4.1. The UGBW should be much larger than the input pole to ensure proper bandwidth and stability, assuming 10X larger, the UGBW is then 88 MHz. Although it provides a better bandwidth, it can be power inefficient as the loop amplifier consumes more power to maintain the high UGBW (will discuss further in section 3.4.1). Also it might introduce secondary poles that would cause instability. To fix these as mentioned, a more reasonable feedback resistance is set to 200 $\mathrm{k\Omega}$. With this higher resistance, the input pole frequency is shifted to a lower, more manageable range, with the output swing is around 100mV. This swing allows for adequate headroom to maintain the output stage in saturation, ensuring consistent and reliable amplifier performance.

As mentioned before, the input current amplitude decays exponentially over time from 50 $\mu\mathrm{A}$ to 0.5 $\mu\mathrm{A}$, increasing the required exponential resistance from 2kΩ to 200 $\mathrm{k\Omega}$, achieving a 40 dB gain range.

For transistors in the triode region, the resistance is inversely proportional to the overdrive voltage; hence, the changes in $\mathrm{V_{OV}}$ lead to changes in the resistance, which in turn affect the current flowing through the device and hence the gain range. Expressly, the minimal overdrive voltage is set to be double the maximal source-drain voltage under the deep triode condition. The chosen output swing of 100 mV calls for a minimal overdrive voltage of 200 mV since only half of the output voltage appears across each of the back-to-back transistors. Furthermore, the maximal overdrive voltage is constrained by the highest potential that the gate voltages can reach, which for 2V transistors, can be up to 2V above the lowest potential terminal.

The maximum possible voltage added on the gate terminal is either the power supply at 0.9 V or the highest potential that the gate voltage can reach 1.9 V (2V - $\mathrm{V_{output}}$). The

maximum output amplitude is 0.1 V. Assuming the threshold voltage of 500 mV, the gain range is computed to be:

$$\frac{V_{OVmax}}{V_{OVmin}} = \frac{0.9V - 0.1V - 0.5V}{0.2V} \equiv 3.5\,dB \qquad \text{(using 0.9 V supply range)} \tag{3.8}$$

$$\frac{V_{OVmax}}{V_{OVmin}} = \frac{1.9V - 0.1V - 0.5V}{0.2V} \equiv 16.25\,dB \qquad \text{(using 1.9V as maximum gate voltage)} \tag{3.9}$$

Employing parallel branches is an effective strategy to expand the gain range beyond 16.25 dB to meet the overall 40 dB gain range target. Three parallel branches operating on a different part of the gain range are utilized, each being dominant within specific time intervals to achieve an overall gain range of 40 dB [15], as illustrated in Fig 3.4. The feedback network uses these branches with adequate gain overlap to ensure smooth transitions between intervals. The control voltage for each branch decreases exponentially, causing the resistance of each branch to increase exponentially over time. The collective resistance forms an approximately exponential curve by designing the triode transistors in each branch with different sizes and applying varying rates of decreasing control voltages. All three branches are active at the lowest gain setting, handling the maximum input amplitude at the beginning with a combined resistance of 2 $k\Omega$. Only one branch remains active at the highest gain setting, amplifying the smallest input signal at the end with a resistance of 200 $k\Omega$.

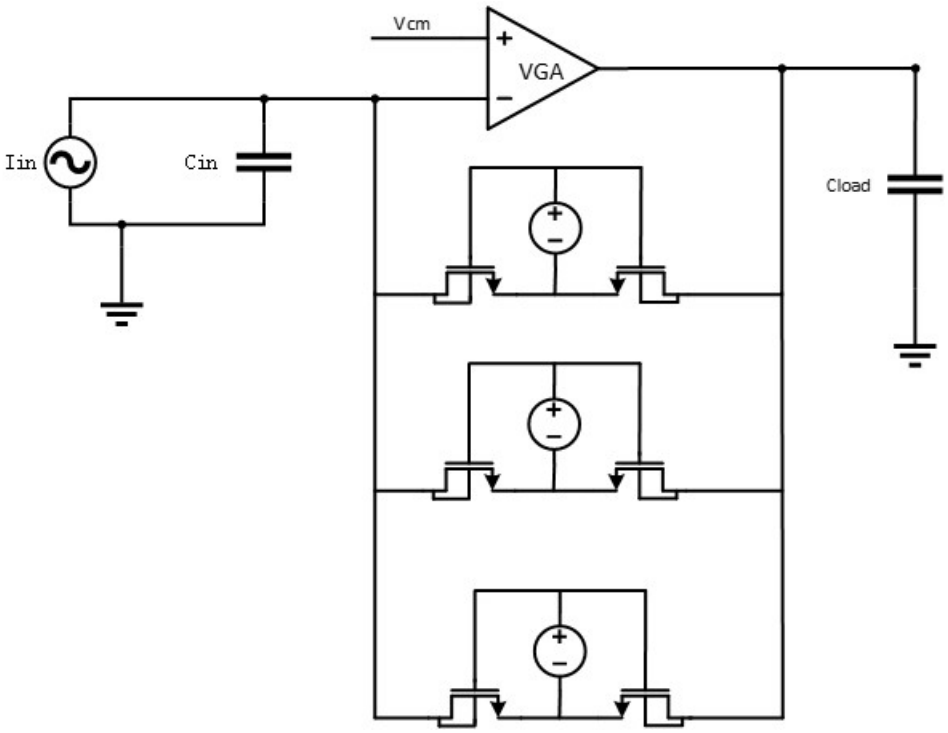


Figure 3.4: the TIA with parallel resistors configuration for overall gain range extension

Gain-extension is achieved by the property of parallel branches, such that the branch with the smallest resistance will be considered more active than those branches with rel-

atively larger resistance. Switching between individual branches can be accomplished by progressively increasing their resistance through the reduction of gate voltages, extending well beyond their respective gain ranges. Even when the gate voltage drops below the threshold voltage, that particular branch is effectively considered deactivated. Smooth transitioning along the smallest-resistance gain curve is ensured if the control voltages for each branch are reduced at varying rates.

3.4 FEEDFORWARD PATH: LOW NOISE AMPLIFIER

Apart from the feedback network, the feedforward path of the TIA architecture is also vital for completing the loop aimed at the design of the proposed TGC-LNA. The amplifier in the feedforward path will strive to achieve noise specifications while maintaining a relatively low power consumption.

3.4.1 *Stability*

Although the feedback network primarily drives the Time-Gain Compensation (TGC) functionality, variations in gain significantly impact the performance of the loop amplifier and must be considered. The TIA system must be analyzed before the amplifier can be designed.

Checking the frequency response is the first step in ensuring system stability. As shown in Figure 3.2, the TIA loop consists of an 18 pF transducer capacitor $\mathrm{C_{in}}$; a 40dB varying feedback network operating in the triode region, seen as a feedback resistor $\mathrm{R_{fb}}$; a load capacitor $\mathrm{C_{load}}$ and output impedance of the loop amplifier noted as $\mathrm{R_{load}}$. The circuit exhibits two poles, each determined by the total capacitance from each node to the ground multiplied by the total resistance seen at the node to the ground. A good way to investigate is to check the poles with RC pairs at each node, where $\omega = \tau^{-1}$. Each node in the circuit contributes one pole to the transfer function. Two poles are located at the input and output nodes respectively, as illustrated in Figure 3.5:

$$\mathrm{s_1} = \frac{1}{\mathrm{C_{in}}(\mathrm{R_{fb}} + \mathrm{R_{load}})}, \qquad \mathrm{s_2} = \frac{1}{\mathrm{C_{load}}(\mathrm{R_{fb}}||\mathrm{R_{load}})} \tag{3.10}$$

The feedback resistance changes over time, ranging from 2kΩ to 200 kΩ as discussed previously, two poles are located at and plotted in Figure3.5:

$$\mathrm{f_1} = 3.53\ \mathrm{MHz}, \mathrm{f_2}\ = 397\ \mathrm{MHz}, @\mathrm{R_{fb}}\ = 2\mathrm{k}\Omega \tag{3.11}$$

$$\mathrm{f_1} = 44\ \mathrm{kHz}, \mathrm{f_2}\ = 319\ \mathrm{MHz}, @\mathrm{R_{fb}}\ = 200\mathrm{k}\Omega \tag{3.12}$$

$$\tag{3.13}$$

The dominant pole is the input pole, which shifts from 3.5MHz to 44kHz while the output pole stays in a higher frequency band to ensure an adequate phase margin. The amplifier should have load-driving capability. Moreover, the output impedance of the loop

amplifier should be inherently low for stability reasons. Since with large load impedance, the higher order poles will shift to a lower frequency band to limit the phase margin. Assume R_{load} is chosen as 500 Ω as a reasonable value as small output impedance requires more power consumption. The load capacitor is 1pF. Apart from that, with a fixed amplifier gain, it can be seen that with the increasing 40 dB feedback resistance, the dominant pole is dropping 40 dB as well. This means there is a 40 dB decreasing unity gain bandwidth (UGBW).

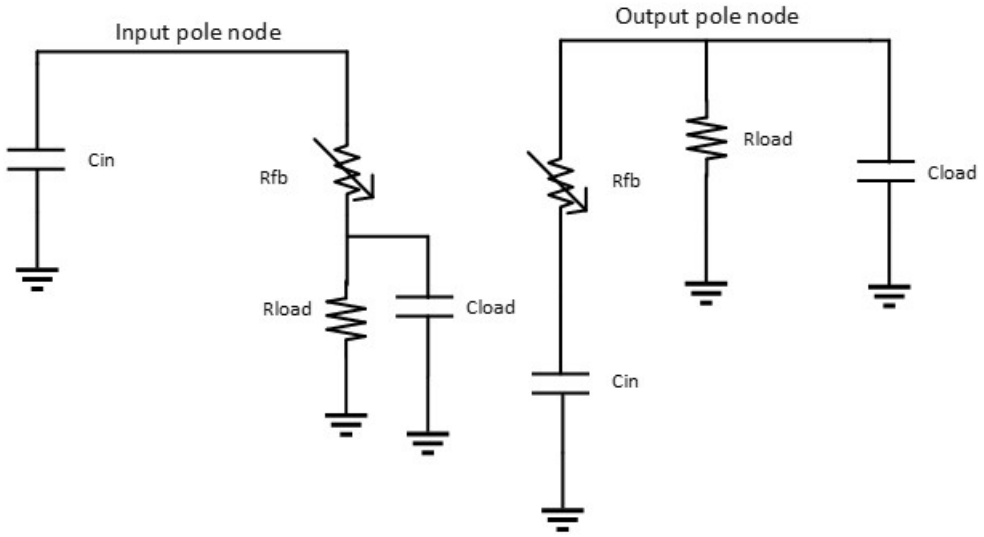


Figure 3.5: Configuration of finding input and output nodes

A varying UGBW will cause serval problems. First, excessive power is used to maintain an unnecessarily large UGBW. Secondly, a variable UGBW can introduce instability issues due to the presence of secondary poles. Ideally, the bandwidth should contain only one dominant pole at lower gains as the output pole is shifted to higher frequencies. However, the loop amplifier requires multiple stages to meet noise, gain, and stability demands. These stages introduce additional output poles that can negatively impact the phase margin, and this effect is more pronounced at lower gains because the reduced loop gain provides less compensation for the phase shift introduced by these poles. Increasing the bandwidth of each stage to counteract this would lead to even higher power consumption, which is undesirable. To ensure stability, it is crucial to maintain a large phase margin. Consequently, maintaining a fixed UGBW is advisable.

The loop gain with varying UGBW is shown in Figure 3.6, the dominant pole is shifting 40dB. A fixed UGBW is also shown in Figure 3.7. To realize this, a variable gain amplifier should be implemented.

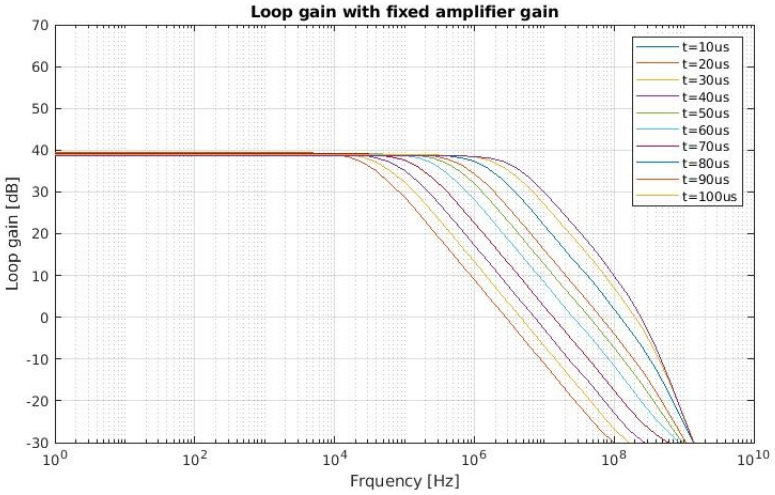


Figure 3.6: Loop gain with fixed loop amplifier gain

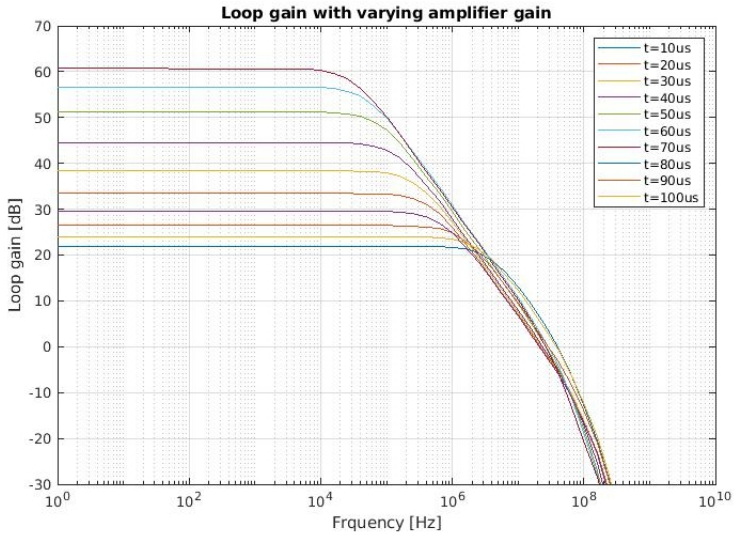


Figure 3.7: Loop gain with varying loop amplifier gain

The selection of the unity-gain bandwidth (UGBW) must be carefully balanced to effectively manage both the amplifier's DC gain and its phase response. The UGBW should be at least larger than the bandwidth. On the other hand, a UGBW that is too large can also be detrimental, as it introduces excessive phase shifts close to the unity gain frequency. This is problematic because excessive phase shifts can push the phase margin too close to instability, leading to potential oscillations in the system. The phase shift, which increases with frequency, must be managed to prevent the feedback from becoming positive (phase inversion), which is characteristic of an oscillatory system.

3.4.2 *Noise Optimization*

The specification for the proposed LNA-TGC is defined as 1 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$ noise density at the center frequency. The total noise comes from several contributors, with primary sources

being the feedback resistances and the loop amplifier. Based on the equation (3.6), with feedback resistance of 200 $\mathrm{k\Omega}$, the current noise density of feedback network is then 0.29 $\mathrm{pA}\sqrt{\mathrm{Hz}}$, while to meet the total noise budget of 1 $\mathrm{pA}\sqrt{\mathrm{Hz}}$, the loop amplifier noise density is allocated the value of 0.96 $\mathrm{pA}\sqrt{\mathrm{Hz}}$ since noises are uncorrelated. Since the input impedance of the transducer is 1.2 $\mathrm{k\Omega}$, the corresponding input-referred voltage noise density for the loop amplifier is 1.15 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$.

Before diving into the amplifier structure, the noise sources should be analyzed. There are two main types of noise: thermal noise and flicker noise [31]. The thermal noise is defined by:

$$\mathrm{V_{n,thermal}} = \sqrt{\frac{4\mathrm{kT}\gamma}{\mathrm{g_m}}}[\frac{\mathrm{V}}{\sqrt{\mathrm{Hz}}}] \tag{3.14}$$

Where $\mathrm{V_{n,thermal}}$ is the input-referred thermal voltage noise density, k is the Boltzman constant, T is the temperature in Kelvin and γ is a process coefficient approximate to 2/3 for long channel devices and $\mathrm{g_m}$ is the transconductance. The tunable variable to achieve the low noise propose is to increase the transconductance.

Another source is the flicker noise, namely 1/f noise, is defined as:

$$\mathrm{V_{n,1.f}} = \sqrt{\frac{1}{\mathrm{f}}\frac{\mathrm{K}}{\mathrm{C_{ox}WL}}}[\frac{\mathrm{V}}{\sqrt{\mathrm{Hz}}}] \tag{3.15}$$

Where $\mathrm{V_{n,1.f}}$ is the flicker noise voltage density, f is the frequency, $\mathrm{C_{ox}}$ is the oxide capacitance, W and L are the device width and length. The tunable variable is the dimensions of the transistor. Increasing the transistor area helps reduce the 1/f noise, as larger transistors have a lower flicker noise density due to the averaging of surface effects over a larger area. However, while this approach effectively reduces flicker noise, it also comes with trade-offs. Specifically, enlarging the transistor increases the gate capacitance, which can impact the overall system stability. The additional capacitance can cause non-dominant poles (higher frequency poles that are not intended to control the system's behavior) to shift towards lower frequencies. If these non-dominant poles move too close to the system's operating bandwidth, they can degrade the phase margin and potentially cause stability issues, such as oscillations or reduced gain.

3.4.3 *Loop amplifier Structure*

To achieve overall lower power consumption, fixing the UGBW at a specific frequency is advantageous, thereby allowing for power reduction when smaller feedback impedances are present. This necessitates the ability to adjust the gain of the loop amplifier in tandem with changes in the feedback impedance. Consequently, the loop amplifier must possess a controllable gain to optimize performance across varying operating conditions.

To achieve the objective of implementing a controllable gain amplifier, we conducted a thorough evaluation of various amplifier architectures. Given the critical requirements for noise and power optimization, the transconductance amplifier emerged as the optimal

choice. Its inherent flexibility in transconductance control facilitates effective noise management and enables adaptive power scaling, making it particularly well-suited for applications where precision and efficiency are paramount.

Adjusting the gain of an amplifier can be achieved through two primary methods: varying transconductance or adjusting the load. Each method offers distinct advantages and comes with inherent challenges that impact their suitability for specific applications.

Varying transconductance directly controls the amplifier's gain by adjusting the proportionality factor between the input voltage and the output current in a transistor. Adjusting transconductance is often done through biasing techniques in MOSFETs [15], which can sometimes be simpler than changing the load in complex circuit configurations. However, this method introduces two main challenges: noise amplification and gain mismatch. Using a variable current source for g_m adjustment often leads to a nonlinear relationship between g_m and the bias source due to inconsistencies in transistor performance. This results in gain mismatches between the bias current and the feedback resistance, complicating gain control and leading to variations in the unity-gain bandwidth (UGBW), potentially destabilizing the amplifier. These issues highlight the complexity and the potential for reliability concerns when using g_m variation as a method for adjusting gain.

On the other hand, varying the load to adjust gain involves changing the load resistance or impedance. This method is straightforward, particularly in simple amplifier configurations, and offers a certain range of adjustability, which provides flexibility in gain settings. It also tends to be robust against changes such as fluctuations in supply voltage and temperature. However, altering the load can lead to inefficiencies, particularly in terms of power consumption. In multi-stage amplifiers, changing the load in one stage can affect other stages, requiring more power and careful design.

Additionally, employing a variable load can cause the output pole to shift significantly, potentially moving across two decades within the frequency band of interest. This large movement occurs when the gain changes drastically in a single stage. However, if the gain is distributed across multiple stages, the pole shift would be less pronounced. The combination of this shifting output pole and a 40 dB moving input pole can significantly affect the phase response at higher gain settings, potentially destabilizing the loop amplifier.

The amplifier design is mainly based on the work [16] that incorporates several strategic elements to address these challenges and enhance stability. The most notable element is the use of multiple stages to distribute the gain, which helps mitigate large shifts in pole frequencies and maintain phase margin.

Firstly, the gain of the loop amplifier is made adjustable by altering the load attached to the amplifier, which allows it to maintain a consistent unity-gain bandwidth (UGBW) across various gain settings, optimizing power efficiency and ensuring stable performance throughout its operating range. Secondly, a buffer stage is implemented at the final stage of the loop amplifier to ensure low output impedance. This is essential for effectively driving loads or subsequent stages without compromising signal integrity, thereby helping to isolate the amplifier from load-induced variations. Lastly, the design of each stage of the loop amplifier aims to push its output pole to higher frequencies. This strategy signific-

antly minimizes the influence of non-dominant poles on the amplifier's critical operational bandwidth, enhancing overall stability and reducing potential adverse effects on loop stability. Collectively, these measures guarantee that the amplifier operates reliably within its desired specifications, striking an effective balance between performance and efficiency.

Thus, the proposed amplifier has four stages to meet the needs, as shown in Figure 3.8. The first stage has a fixed gain and is designed for low noise, so it needs to have a fixed high gain as the noise figure of the first stage dominates the total noise figure of the entire amplifier chain. To achieve a fixed UGBW, variable gain stages are necessary. Since the feedback network achieves a 40 dB gain, the DC gain of the amplifier also needs to vary by 40 dB, which is difficult to accomplish with a single stage. The middle two stages are then designed to provide 20 dB gain each, with appropriate loads. Given that the transducer is grounded on one side, meaning it is a single-ended source, the Low Noise Amplifiers (LNAs) are configured with single-ended structures. However, to mitigate even-order distortion, the earlier stages utilize a fully differential design, necessitating a conversion from differential to single-ended in the output stage. The design details of each stage will be discussed in the next section.

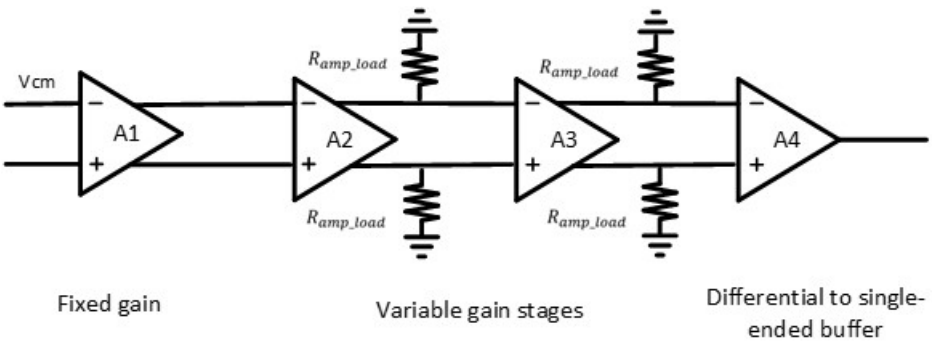


Figure 3.8: Loop amplifier four-stages topology

3.5 LINEARITY

Distortion, or non-linearity, in amplifier circuits can arise from multiple sources. It may originate from non-linear transfer functions or result from imbalances in the circuitry. In the feedback network, the body effect contributes to even-order distortion, particularly second-order harmonics, because of its non-linear influence on the transistor's threshold voltage, which is a significant source of distortion. For instance, a single feedback transistor can show an imbalance in threshold voltage when handling positive and negative input signals. As the input signal causes variations in the source-to-bulk voltage, the resulting asymmetric modulation of the drain current introduces even harmonics into the signal. To correct this, a back-to-back transistor configuration with bulks connected to the outer nodes, the floating source to the middle node is employed to ensure symmetry in the feedback network and reduce distortion [15].

Non-linearity can also arise from small signal gain variations with changing input levels. One effective method to reduce non-linearity is through the use of differential circuits, as

they inherently cancel out even-order harmonics. For this reason, the first three stages of the amplifier are designed as fully-differential structures.

However, all stages experience small signal gain variation, with the effect being most significant in the third stage and the buffer. These stages experience the largest output swing, approximately 100 mV, which can amplify the non-linear behavior of the transistors, leading to odd-order harmonic distortion. Therefore, special design considerations must be taken to mitigate this non-linearity. The cascode structure in the third stage help with the distortion. Also, large signal swings can be minimized by extending the transistors' linear operating region. This can be achieved by reducing the W/L ratio, which increases the overdrive voltage of the input transistors, thereby expanding their linear range.

In the buffer stage, which converts a differential signal to a single-ended signal, even-order harmonics become a dominant source of distortion. The signal paths for positive and negative input signals are different, contributing to imbalance. To minimize these even harmonics, the transconductance of the input transistors should be matched as closely as possible. Besides, reducing the W/L ratio helps improve linearity, provided that low output impedance is preserved.

3.6 OVERVIEW OF THE CHOSEN ARCHITECTURE

In summary in this section, Figure 3.9 illustrates the chosen architecture. The proposed TIA structure consists of a four-stage variable gain amplifier and three branches of back-to-back triode MOS devices as resistive feedback.

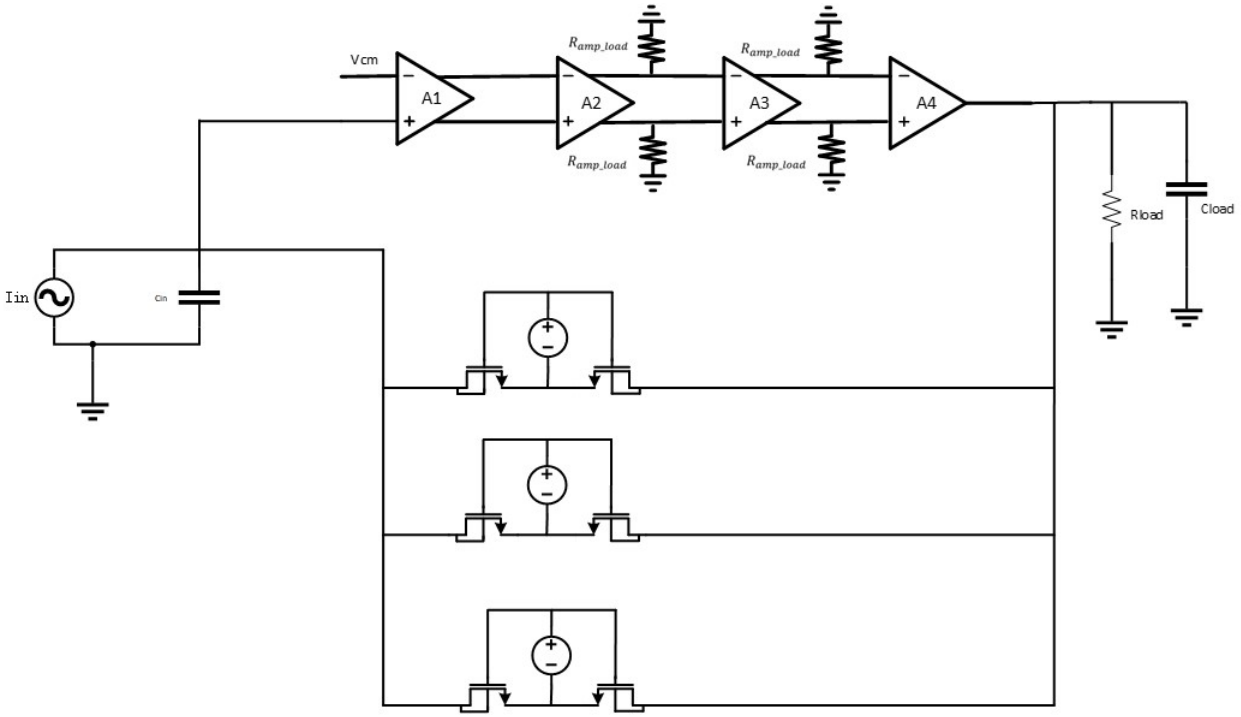


Figure 3.9: Overview of the chosen architecture

4

CIRCUIT IMPLEMENTATION

In the previous chapter, the architectural design of the proposed LNA-TGC has been discussed. This section will further investigate and illustrate the circuit implementation of the feedback network and low-noise amplifier. Different trade-offs motivate the design choices, including noise, power, area, linearity, and stability.

4.1 FEEDBACK NETWORK

4.1.1 *Control Voltage Generation*

The ideal voltage source in Figure 3.4 should offer an exponentially decreasing voltage to get an exponentially increasing on-resistance. An exponential voltage drop is expected when a pre-charged capacitor with a resistor is discharged. This work's total receive period is 100 μs. The required RC time constants for each branch are to be on the order of 10 μs. With a capacitance of a few pF, the discharge resistor needs to be as large as in the order of MΩ. The idea can be further improved by the MOSFET-C network illustrated in Figure 4.1. The needed large resistor can be replaced by a transistor operating in the saturation region. In the saturation region, the drain current is determined by the overdrive voltage, with the drain-source voltage having minimal impact on it. This implies that if the gate-source voltage of the transistor is maintained at a constant level, a steady current can be consistently drawn from a pre-charged capacitor, resulting in a linear discharge to approximate an exponential function. Using this linear discharge technique will cause the overall resistance to deviate from a purely exponential function. The real gain curve, which closely resembles the exponential curve but deviates slightly, is defined as the gain error and can be further improved through additional tuning techniques.

The capacitor $\mathrm{C_{bias1}}$ is denoted as the capacitor connected between the gate and source node of PMOS transistors $\mathrm{M_{source}}$, while $\mathrm{C_{bias}}$ is denoted as the capacitor connected between the source and drain node of $\mathrm{M_{source}}$ as well as connecting between the gate-source node of the back-to-back triode devices $\mathrm{M_{triode}}$. Two capacitors $\mathrm{C_{bias1}}$ and $\mathrm{C_{bias}}$ are pre-charged to the same initial voltage by the same voltage sources in each branch during the short interval before the RX period starts by controlling the switches so that the $\mathrm{M_{source}}$ starts by operating in the saturation region. The pre-charging period is set at 10 μs. After 10 μs, the switch is open for the drain current drawn from $\mathrm{C_{bias}}$ to discharge linearly, forming a linear voltage drop of the gate-source voltage of the back-to-back triode devices $\mathrm{M_{triode}}$.

The purpose of the Sample and Hold network in adding an initial voltage to the capacitors, followed by discharging, is that the nodes connected to the transistor $\mathrm{M_{source}}$ are floating. Once the capacitor is charged, it effectively floats and holds the required voltage, isolated from external fluctuations or noise in the power supply or ground.

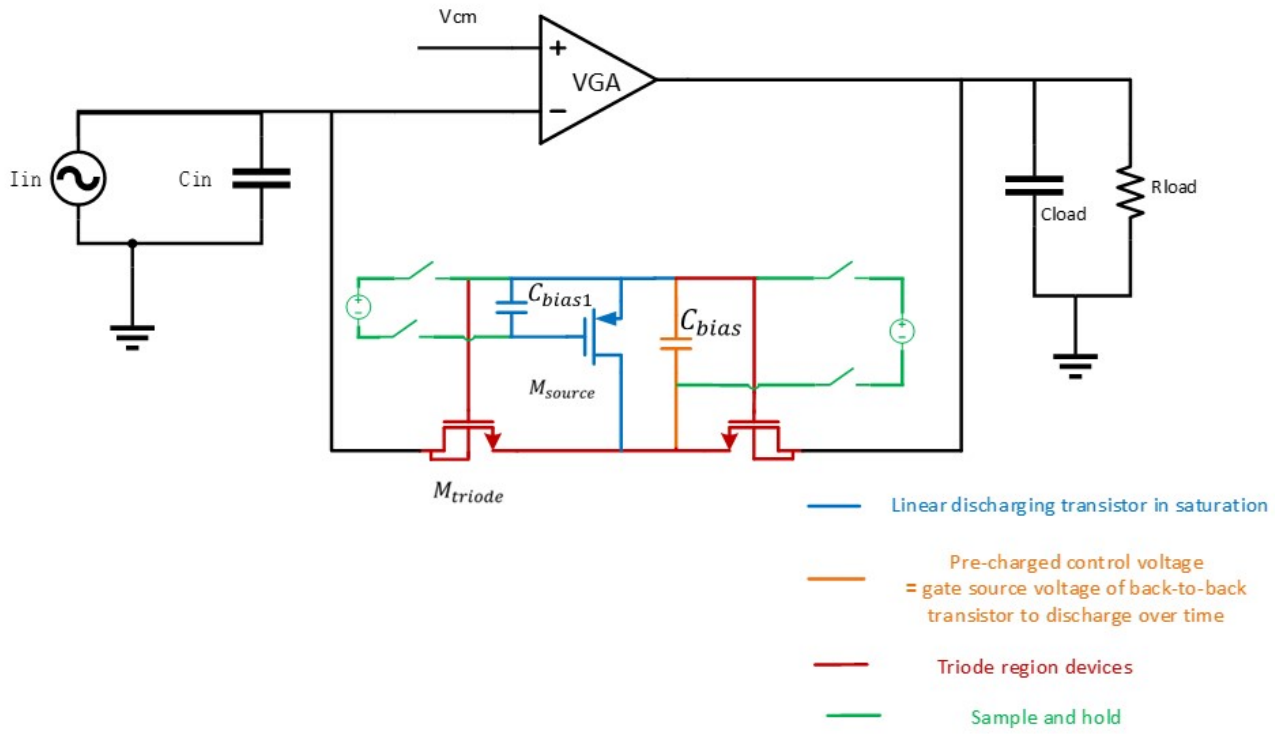


Figure 4.1: Variable bias current source linearly dependent on the feedback resistance, with a low-pass filter [15]

4.1.2 *Three Branches Implementation*

The overall feedback is depicted in Figure 4.2. The structure includes three branches, each featuring a pair of back-to-back transistors with the same unit W/L (width/length) ratios but different M factors to control different on-resistance in each branch for better matching, finer control for flexible adjustment about consistency, and linear discharge MOSFET-C pairs. These configurations allow each pair of transistors to effectively control a specific interval, resulting in an impedance that changes approximately linearly in dB. Three branches operate within distinct time intervals of the total gain range. Due to the properties of parallel impedance, the branch with the smallest impedance will dominate the overall behavior. If the resistance of one branch is much higher than the others, it can effectively be considered off, allowing the remaining branches to take control during their respective time intervals. This method, known as impedance steering, enables precise control of the total gain by allowing each branch to govern the circuit's operation during its designated interval.

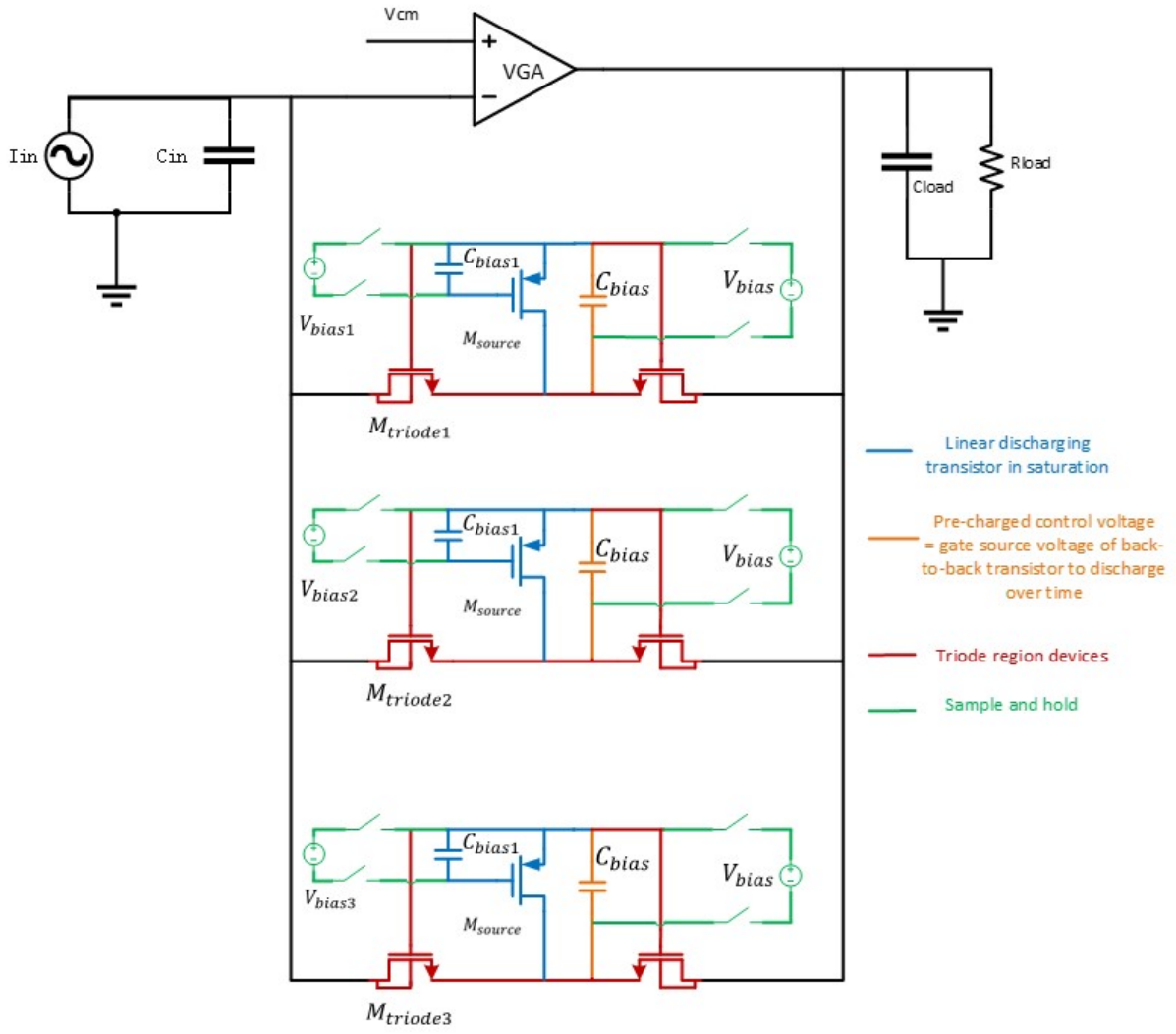


Figure 4.2: TIA with the overall feedback network

The capacitors C_{bias1} and C_{bias} are the same at each branch, while with different pre-charging control voltages V_{bias1}, V_{bias2} and V_{bias3} initially applied to C_{bias1} in each branch respectively, the slopes of discharging voltages in the three branches are different over time, thus the slope of increasing resistance of triode devices $M_{triode1}$, $M_{triode2}$ and $M_{triode3}$ can be independently defined. The PMOS transistors M_{source} operating in saturation region replacing the huge resistors for linearly discharge approximation as discussed before have constant drain current. In the saturation region, the drain current is set by the overdrive voltage. In other words, voltage sources applied on C_{bias1} together with the threshold voltages control the drain current drawn from the capacitors C_{bias}, realizing different slopes of discharging in three different branches. The drain-source voltages can hardly affect the drain current so C_{bias} for three branches are chosen the same.

The voltages V_{bias} in three branches initially applied on C_{bias} are the same, after the switches are open after $10\mu s$, due to the different drain currents drawn from C_{bias} in three branches, the gate-source node voltages of $M_{triode1}$, $M_{triode2}$ and $M_{triode3}$ denoted as V_{ctrl1}, V_{ctrl2} and V_{ctrl3} are dropping in different slopes. Figure 4.3 illustrates these voltages for the three branches. The on-resistances in the three branches depend on gate-source voltages.

The constant drain currents will cause the voltages to decrease at a constant rate, resulting linear discharge curve. Since the voltage is not a pure exponential signal, the expected linear-in-dB gain will have the gain error. This results mainly in artifact at each branch-switching moment, but it can be adjusted easily by the drain current.

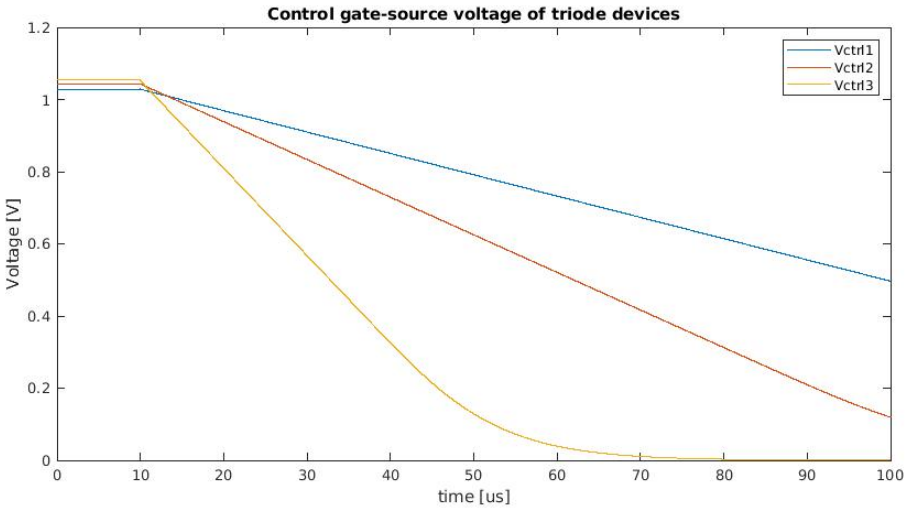


Figure 4.3: Different control signals for three branches

The gain errors occur during the intervals when each of the three branches takes over. The target is to compress these gain errors within $\pm$ 1 dB. The sequential alternation of branches results in a real gain that fluctuates around the linear line, creating an up-and-down pattern. The gain error resembles a sinusoidal-like wave. By controlling the discharge slopes of the three branches, we can adjust the overall gain's linearity in dB, ensuring a more matched transition between branches. This approach averages out the gain error waveform bounded within the $\pm$ 1 dB range, preventing sharp deviations beyond this range. To achieve the desired control over gain error, the existing ideal voltage sources need to be replaced with real biasing circuits. Additionally, an effective method must be implemented to adjust the drain current flowing through the PMOS transistors, allowing careful control over the discharge slope.

During optimizing the gain error within $\pm$ 1dB, several parameters can be tuned. The first is to determine the size of the triode transistors in the feedback, together with the reference resistor $\mathrm{R_{replica}}$ matches the best linearity. Then determine the ratio between branches to set the initial and intermediate value of the whole gain curve to the desired value. After that, tune the current of three branches to switch the matching error between parallel branches so that the error curve can be as much as even as possible.

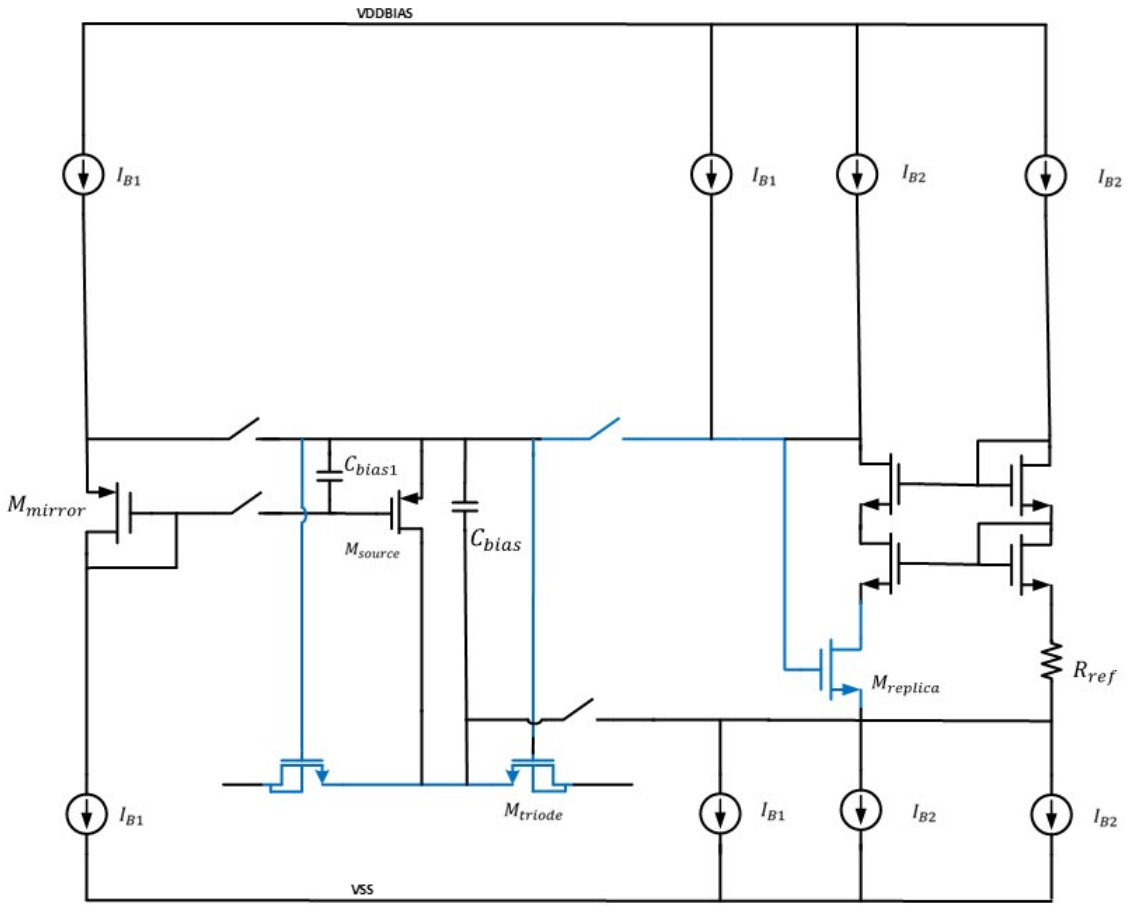


Figure 4.4: Current mirror biasing circuits implemented on feedback network

Besides, the circuit needs to satisfy the target specification over the PVT variations, this is realized by two current mirrors, as shown in Figure 4.4. For simplicity, only one branch is illustrated. Specifically, a current $\mathrm{I_{B1}}$ is passed through a diode-connected replica $\mathrm{M_{mirror}}$ of the PMOS transistor $\mathrm{M_{source}}$, which sets the $\mathrm{V_{SG}}$ of the PMOS transistor $\mathrm{M_{source}}$ required for the desired current. This setup ensures that the drain current discharging the capacitor $\mathrm{C_{bias}}$ is precisely equal to $\mathrm{I_{B1}}$. This configuration not only helps maintain a more consistent $\mathrm{V_{SG}}$, but it also allows for easier adjustment of the gate-source voltage through the current sources. As a result, the circuit becomes more controllable and stable. There is another current path with the same current $\mathrm{I_{B1}}$ flowing through the drain-source of $\mathrm{M_{source}}$ to prevent the copied current from the current mirror structure from affecting the feedback loop, allowing for better management and control of the current.

Another ideal voltage source connected to the drain-source of $\mathrm{M_{source}}$ controls the initial voltages on the transistors $\mathrm{M_{triode}}$ in the feedback network, the initial conditions are required to be determined and tuned. Besides, since the on-resistance value should be stable and carefully monitored over PVT variations, the replica circuit is designed to replace the ideal voltage source. The circuit is structured as a cascode current mirror with source degeneration. In this setup, a NMOS replica transistor, by leveraging the current mirror structure, replicates the resistor's value to establish the initial resistance. The replica transistor operates in the triode region and is controlled by connecting its gate and

source to those of the back-to-back transistor $\mathrm{M_{triode}}$, effectively transferring the initial resistance to $\mathrm{M_{triode}}$. The connection of the replica transistor makes itself a loop to automatically adjust the voltages and on-resistance values to compensate for PVT variations, ensuring stable performance despite changes in process, supply voltage, and temperature. The biasing current $\mathrm{I_{B2}}$ helps to define the initial values of $\mathrm{V_{ctrl1}}$, $\mathrm{V_{ctrl2}}$ and $\mathrm{V_{ctrl3}}$. Since one of the nodes of $\mathrm{M_{triode}}$ is connected to the virtual ground of the amplifier, the common mode is zero, the source connection node between the back-to-back transistors is around zero, which needs the negative supply of the biasing circuit down to -0.9V. The positive power supply is set to 1.8V to get more headroom in the biasing circuit since the PMOS-C network requires a voltage drop over 1V. The cascode current mirrors are used to match the current better.

Figure 4.5 shows the complete feedback network circuit diagram with a biasing circuit at the charging phase. The current biasing circuit includes low-voltage biasing to give more headroom for the cascade mirrors.

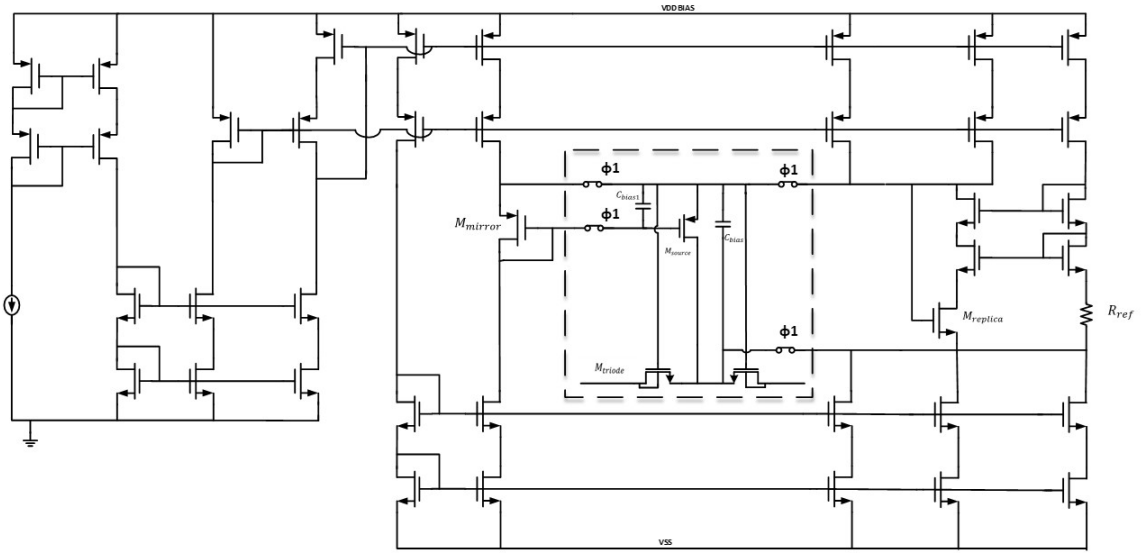


Figure 4.5: Feedback network circuit diagram at charging phase (0μs to 10μs)

After pre-charging the capacitors, the switches are open after 10 μs as shown in Figure 4.6, after which the circuit operates properly as discussed. The drain current flowing in the three branches is denoted as $\mathrm{I_{drift1}}$, $\mathrm{I_{drift2}}$ and $\mathrm{I_{drift3}}$.With this network, the current ratio of three branches can be easily adjusted by biasing current from biasing circuit, which is roughly 1:2:4 for three branches. This approach leverages the ability to linearly control the slopes of discharge voltage, represented by $\mathrm{V_{ctrl1}}$, $\mathrm{V_{ctrl2}}$ and $\mathrm{V_{ctrl3}}$, which can be adjusted through tunable parameters. This flexibility allows for precise tuning of the gain, ensuring that any gain error remains within the specified limits.

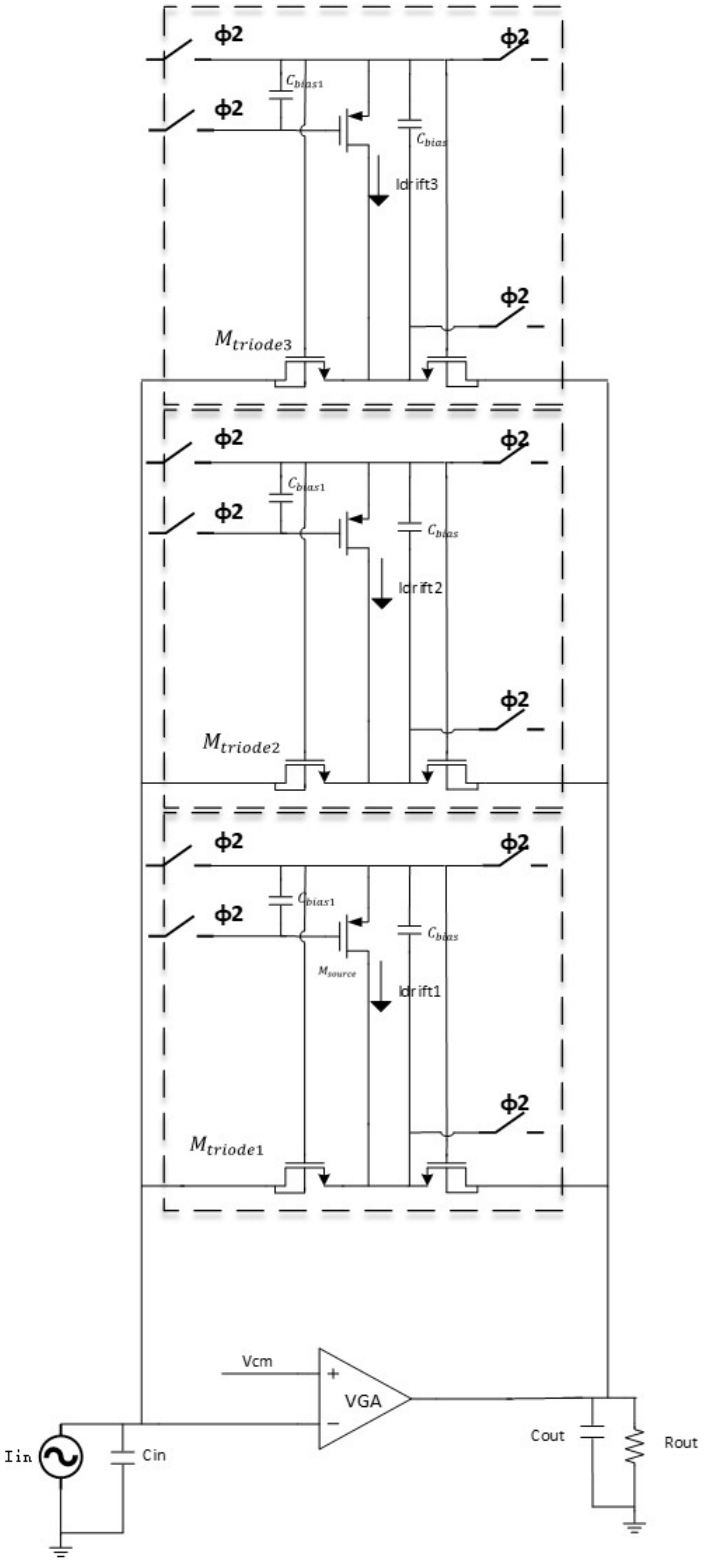


Figure 4.6: TIA at discharging phase (10μs to 100μs)

Since the proposed overall resistive feedback network is designed to occupy less area than a capacitive feedback network, the capacitor size should be carefully chosen. C_{bias1} should be a large capacitor to keep the gate-source voltage stable for a stable drain current during the discharging period. The C_{bias1} is chosen as a 1 pF as a trade-off between minimizing the area cost and obtaining the stable discharge current. Using a 1 pF capacitor,

with a maximum allowable discharge of 5 mV, resulting in a discharge current of 1 nA, is considered acceptable. Additionally, the 1 pF capacitor is advantageous as it conserves the area on the chip. The similar design trade-off applied on C_{bias}. However, due to the structure design, the discharging rate is controlled by the drain current of M_{source}, or the bias current I_{B1} and the capacitor C_{bias}, which should be carefully tuned between three branches to obtain a gain plot with low gain error. To control the discharge rate, a 4 pF capacitor was initially a good choice, and a suitable current was identified accordingly. Subsequently, since the rate of discharging depends on the ratio of the bias current to the capacitor, we can proportionally reduce both the capacitor size and the current while maintaining the desired voltage discharge curve, which also saves area. However, the current cannot be reduced too much, as this could cause some transistors to fall out of the saturation region, increase sensitivity to process variations, and lead to unstable biasing. In sum, the C_{bias} is chosen as 3 pF.

Compared to the Metal-Oxide-Metal (MOM) capacitor that brings larger parasitic capacitance, MIM capacitors are chosen for both C_{bias1} and C_{bias}. Initially, by achieving 3 pF, C_{bias} uses the MOM capacitor. However, since the bottom polysilicon layer is connected to the substrate, it introduces significant parasitic capacitance. When using large MOM capacitors, this parasitic capacitance becomes substantial. In feedback paths, the large parasitic capacitance to ground (around 200fF) can significantly affect the circuit's frequency response and stability: a faster roll-off of the loop gain at high frequencies and significant phase lag causing instability. To mitigate these effects, MIM (Metal-Insulator-Metal) capacitors are preferred. MIM capacitors have significantly lower parasitic capacitance compared to MOM capacitors, as they do not have the bottom polysilicon layer connected to the substrate, resulting in improved stability, better high-frequency performance, and less phase lag.

To further improve the structure of biasing, the branches are re-organized to Figure 4.7 that two branches can share one switch pair.

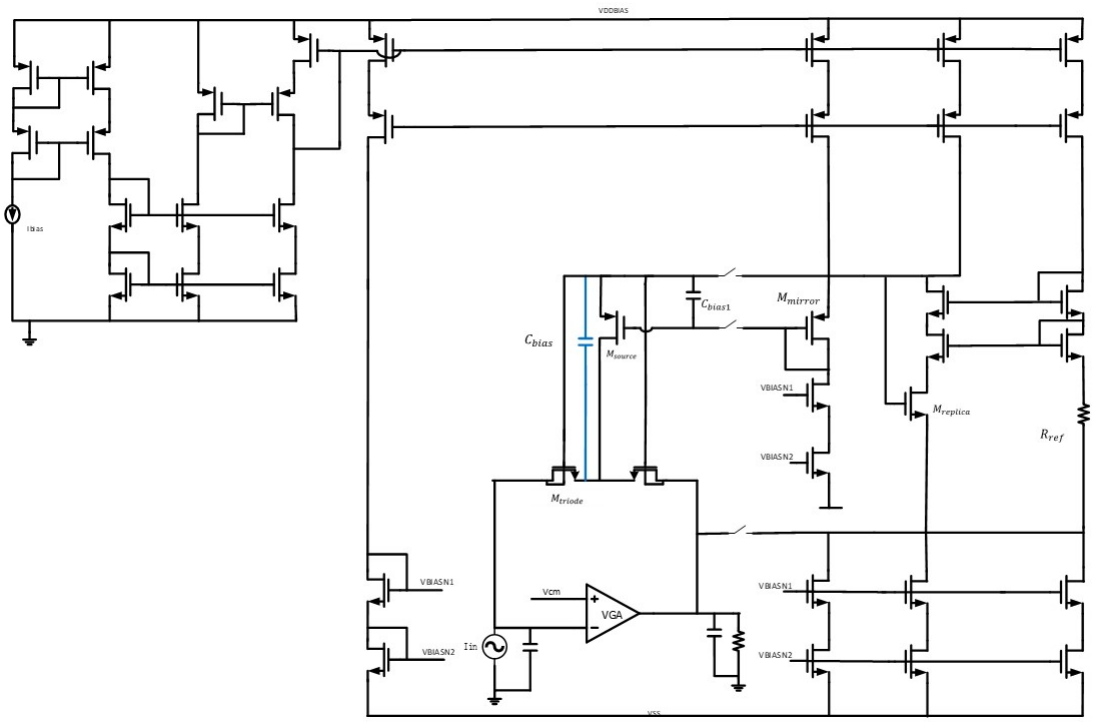


Figure 4.7: Re-organized feedback network

4.2 LOOP AMPLIFIER

4.2.1 *First Stage*

As mentioned in the last section, the amplifier requires low noise, which necessitates high gain in the first stage. For this reason, the current reuse amplifier structure was considered. The current reuse topology allows for higher gain by effectively doubling the transconductance of the stage without increasing power consumption. This is accomplished by stacking transistors so that both contribute to the overall gain while sharing the same current. This high gain in the first stage is crucial for amplifying the signal before the subsequent stages process. In this way, this approach enhances power efficiency due to the effective utilization of the same current in multiple transistors. Despite the many advantages of the current reuse amplifier, it was not utilized in [15] due to its limited headroom where the input voltage is set at 0.5V with a 1.8V supply to allow for large overdrive voltage ranges for the triode feedback transistors. Consequently, in this design, the supply voltage was adjusted to 0.9V, with the input voltage set to 0V, or mid-supply, to better accommodate the design requirements.

Figure 4.8 shows a current reuse amplifier structure with loads [16]. The input pairs consist of both NMOS and PMOS pairs to double the input transconductance of g_{m1}. Besides, the cascode transistors help to increase the output impedance to mitigate the effect of large gate-drain capacitance. Compared to an amplifier stage with a single differential pair, the voltage gain is increased compared to [15] by decreasing the input-referred noise since the input-referred noise is inversely proportional to g_{m1} by a factor of $\sqrt{2}$ [32].

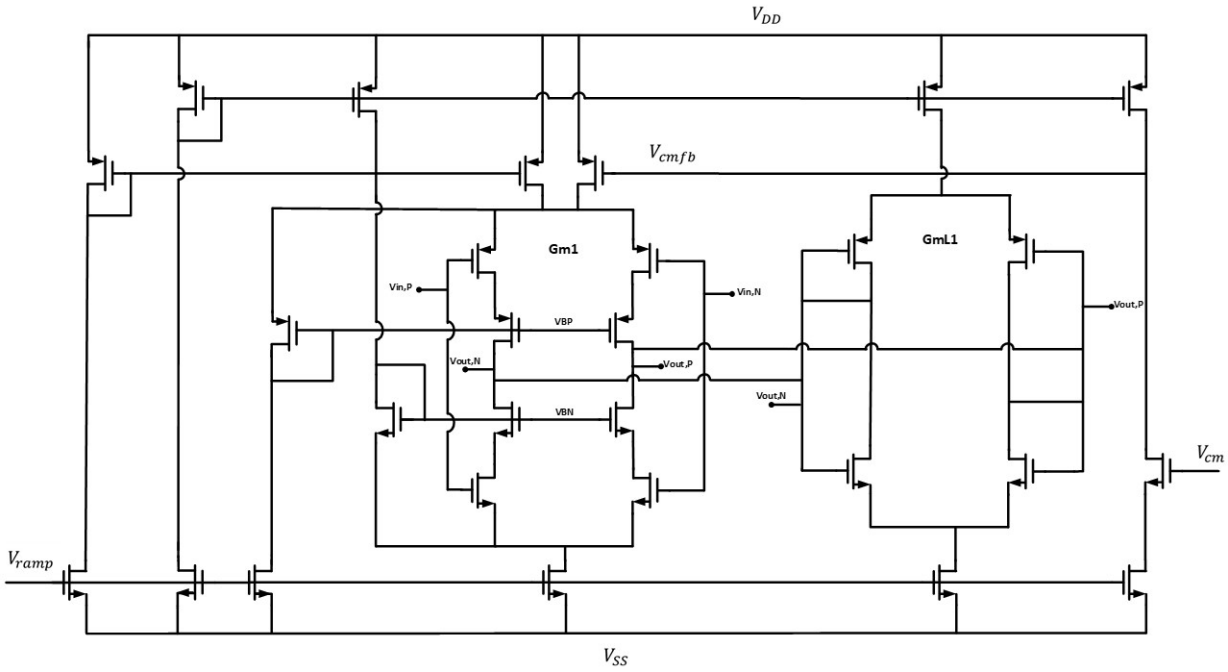


Figure 4.8: First stage schematic [16]

The equivalent input-referred voltage noise is inversely proportional to the transconductance of the input NMOS and PMOS transistors. To obtain a good NEF, MOS input transistors are biased in weak inversion, to take advantage of the high gm/ID ratio. To achieve both aspects, both input MOS transistors should be wide enough. However, the flicker noise and parasitic capacitance should be also taken into consideration. The length of input transistors should also increase to keep the 1/f noise corner frequency relatively low. The large parasitic capacitance will divert a proportional bias current that will introduce extra noise from the bias circuit. The W/L ratios of the input pairs are designed to be 960μm/380nm and 672μm/300nm for the NMOS pair and PMOS pair respectively.

With diode-connected loads, the gain of the first stage is constant at $\frac{g_{m1}}{g_{mL1}}$. The diode-connected loads effectively enhance the gain of the first stage, further increasing the gain on top of what the current reuse structure already provides. Additionally, they help maintain the amplifier's linearity by ensuring that the current through the load transistor remains proportional to the input signal, which reduces distortion and improves overall linearity. If the bias current in a current reuse amplifier is kept constant, it can lead to power wastage because the input-referred current noise density of the feedback resistor is inversely proportional to the feedback resistance, meaning the noise target is lowest at the end of the time. To address this, a ramp voltage generator is applied to deliver an increasing tail current over time as illustrated in Figure 4.9.

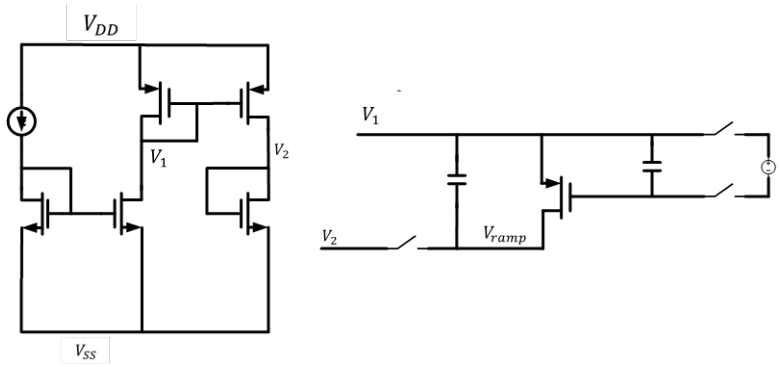


Figure 4.9: First stage schematic [16]

he circuit utilizes a topology similar to one with a feedback network that employs a MOSFET device operating in the saturation region, along with a capacitor that is linearly discharged by the drift current. One side of the capacitor is held at a fixed voltage, while the other side, initially charged to a negative voltage, experiences a gradual increase in voltage as the capacitor discharges. This gradually increasing voltage is referred to as $\mathrm{V_{ramp}}$.

As the capacitor discharges, the voltage across the capacitor decreases, which causes the voltage on the initially negative terminal to rise in a controlled, linear manner. This linear rise in $\mathrm{V_{ramp}}$ can be precisely controlled by the drift current through the MOSFET, which is critical in maintaining a predictable, time-dependent voltage ramp. The rate of discharge, and thus the slope of Vramp, is determined by the size of the capacitor and the current flowing through the MOSFET, both of which can be tuned to achieve the desired performance. The resulting ramp voltage is shown in Figure 4.10.

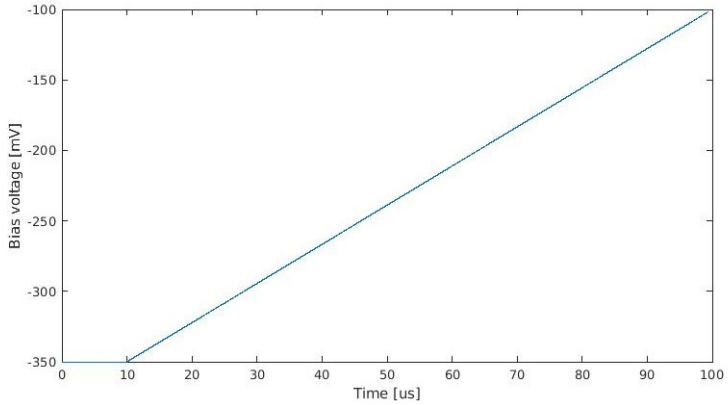


Figure 4.10: The ramp voltage as a function of time

This approach causes the input transconductance to rise gradually, allowing the noise target at each time moment to meet its minimum requirement. As a result, power wastage is avoided, and power efficiency is improved.

4.2.2 *Second & Third Stage*

The middle two stages are designed to maintain a constant transconductance while using variable loads. This setup ensures the transconductance remains stable, keeping the gain and bandwidth consistent. The variable loads allow for DC gain to vary. Since the total DC gain needs to vary by 40 dB, each of the two stages provides 20 dB of gain. These two stages need to have the same structure to ensure uniform performance and symmetry, which is important for minimizing mismatches and achieving the desired gain variation accurately. For simplicity, only one of them is illustrated. As shown in Figure 4.11, the main structure of the second stage is also designed to make it the same as the first stage, by using a current reuse configuration. The advantage of this approach is that it ensures consistent performance across both stages, with a stable transconductance that enhances overall gain and bandwidth. Additionally, using the same current reuse structure in both stages maximizes power efficiency and reduces design complexity, as it allows for uniform biasing and easier integration into the overall amplifier design.

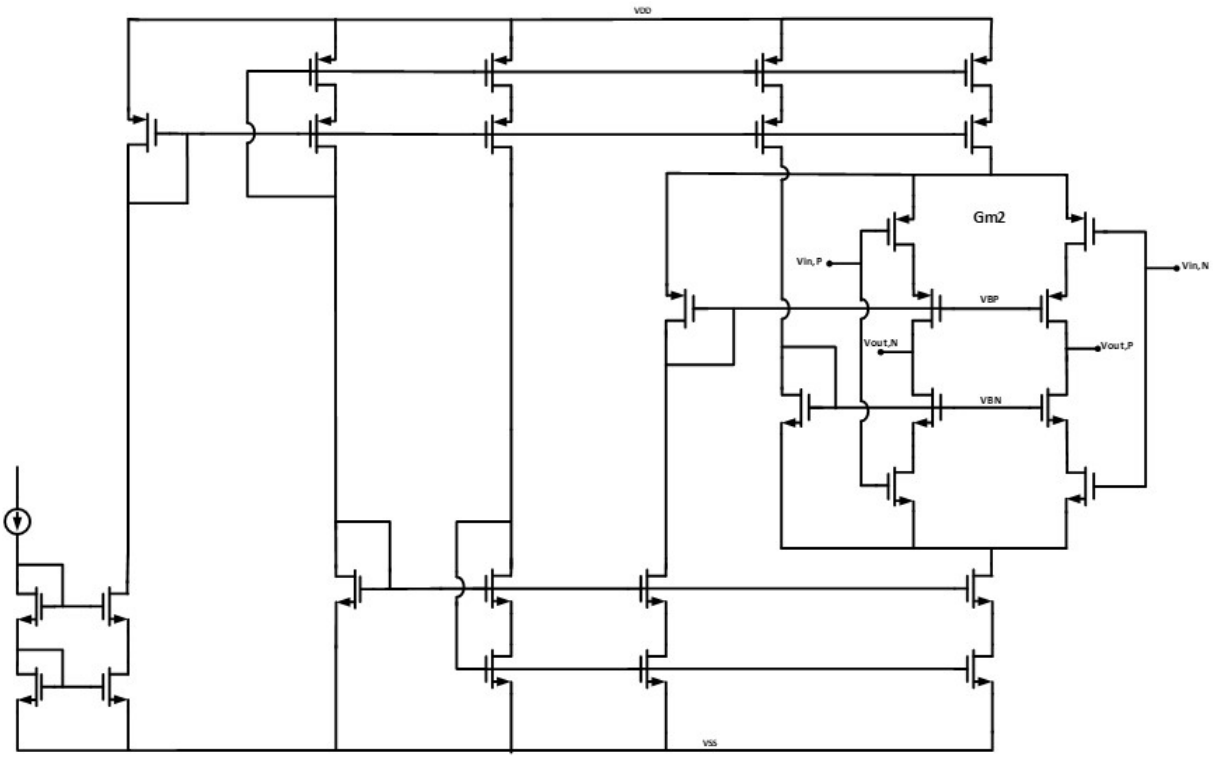


Figure 4.11: Second stage schematic

The variable loads are shown in Figure 4.12, which consists of three parallel transistors with their drain connected to the output nodes of the second stage while the source is connected to the ground. The key benefit of this set of three branches of transistors is that the varying DC gain and feedback resistance to keep constant UGBW is more matched. The load transistors are inspired by the transistor branches from the feedback network with the same ratio. The gate voltages of the load transistor similarly control the on-resistance with the MOSFET-C discharging of the feedback resistors. The advantage of this diagram is

that the common mode feedback is no longer needed, simplifying the circuit. The circuit could better reject the common mode signals if the output is balanced around zero due to symmetry supply signals. The generation of the control signal on gate voltage of load transistors is illustrated in highlighted within the red dashed box in Figure 4.13. A similar MOSFET-C network with NMOS in this case was shared with the biasing network from the feedback block.

The variable loads are shown in Figure 4.12 consist of three parallel transistors with their drains connected to the output nodes of the second stage, and their sources connected to the actual ground. This design first ensures that the varying DC gain and feedback resistance maintain a more consistent UGBW. Additionally, the common-mode feedback is no longer necessary, simplifying the circuit. The balanced output around zero, due to symmetrical supply signals, enhances the circuit's ability to reject common-mode signals.

The load transistors are modeled after the transistor branches in the feedback network, using the same M factors in each branch. The gate-source voltages of these load transistors control the on-resistance similarly to how the MOSFET-C discharges the feedback resistors. The generation of the control signal for the gate voltages of the load transistors is shown in Figure 4.13, where a similar MOSFET-C network, using NMOS in this case, is shared with the biasing network from the feedback block.

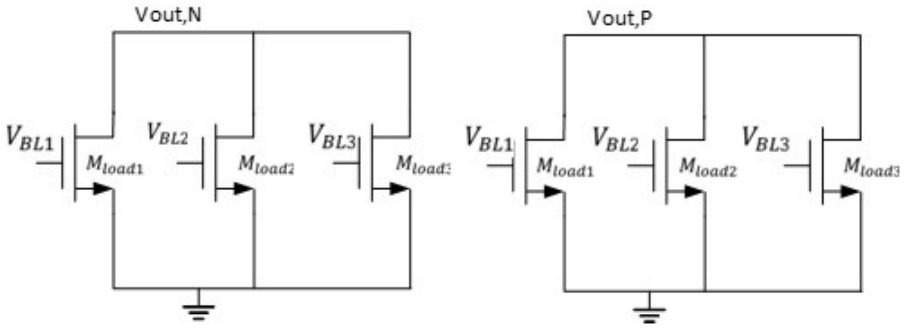


Figure 4.12: Variable loads of the second stage

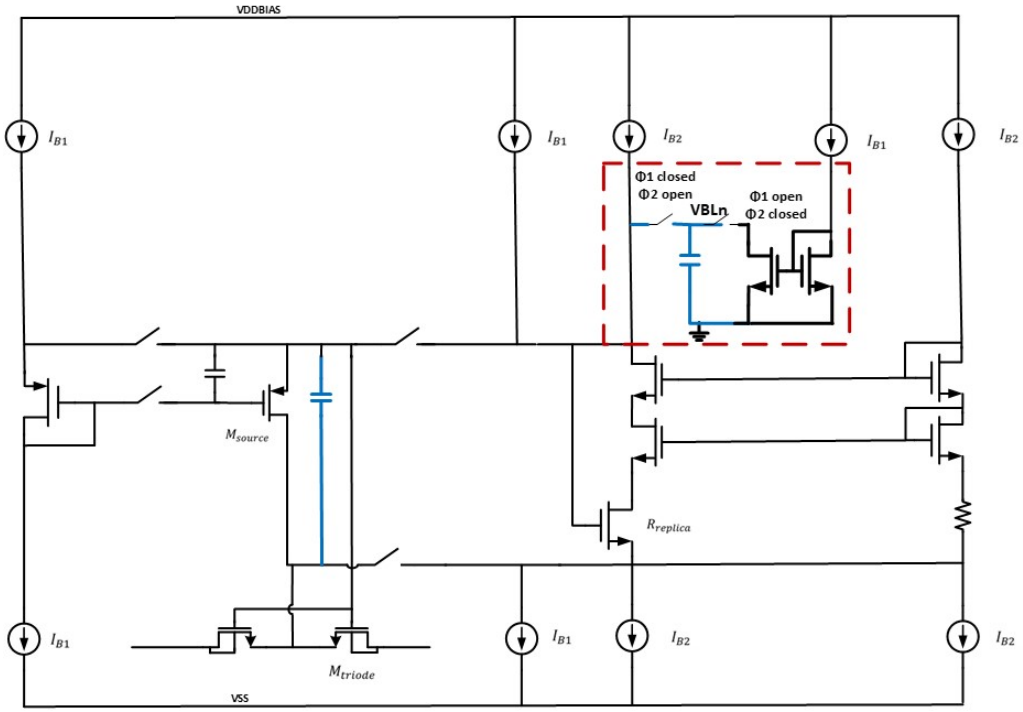


Figure 4.13: Controlling signal generation diagram of gate voltage of load transistors

This is implemented with two stages, each providing a 20dB linear increase. The control voltage in Figure 4.12 V_{BL1}, V_{BL2} and V_{BL3} are adjusted with a slope that decreases by half of V_{ctrl1}, V_{ctrl2} and V_{ctrl3} in feedback network, as shown in Figure 4.14, reaching the voltage level at which the intermediate time point is achieved. As a result, the amplifier's load resistance increases in proportion to the feedback resistance at this intermediate point, realizing half the on-resistance value by the feedback network, allowing each amplifier stage to achieve a 20dB linear increase in DC gain.

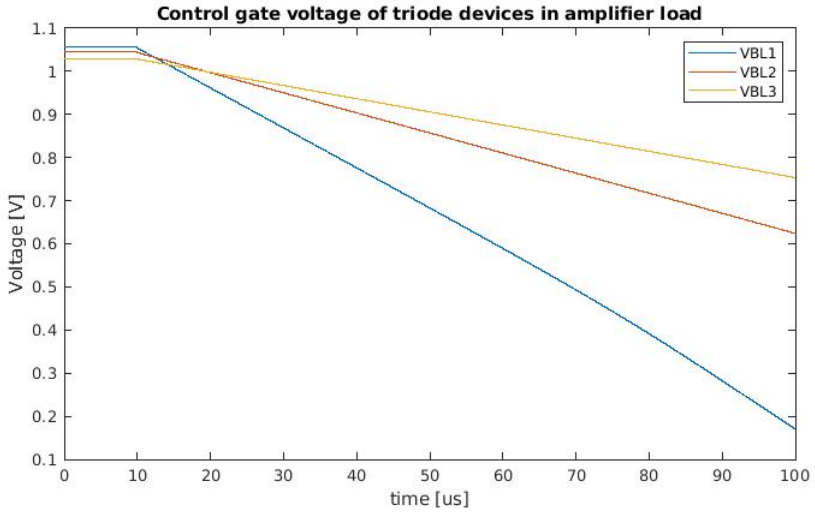


Figure 4.14: Controlling signal of load transistors

4.2.3 *Last Stage (Buffer)*

The circuit's output stage requires a low output impedance and differential to a single-ended conversion, hence the inclusion of a buffer as depicted in Figure 4.15[16]. The buffer combines a source follower with a common source amplifier, which optimally manages this transition. Input capacitors are used to decouple the AC signal swing from the input voltage level, ensuring the signal processing is not influenced by varying input voltages. The bias conditions for the output are established by diode-connected transistors during the pre-charging (TX) phase, which stabilizes the output at the mid-supply voltage. The input capacitance is specifically set at 2 pF to minimize any current leakage, enhancing the overall efficiency and performance of the circuit. By calculation, the output can be expressed by:

$$\mathrm{V_{out}} = \frac{\mathrm{g_{m1}}}{\frac{1}{\mathrm{r_{o1}||r_{o2}}} + \mathrm{g_{m1}}}\mathrm{V_{in,p}} - \frac{\mathrm{g_{m2}}}{\frac{1}{\mathrm{r_{o1}||r_{o2}}} + \mathrm{g_{m1}}}\mathrm{V_{in,n}} \tag{4.1}$$

where $\mathrm{r_{o1}}$,$\mathrm{r_{o2}}$ stands for output resistances of two NMOS devices, $\mathrm{g_{m1}}$,$\mathrm{g_{m2}}$ are transconductance. If $\mathrm{r_{o1}||r_{o2}}$ is big, $\mathrm{g_{m1}} = \mathrm{g_{m2}}$, the output stage can be considered a unity buffer.

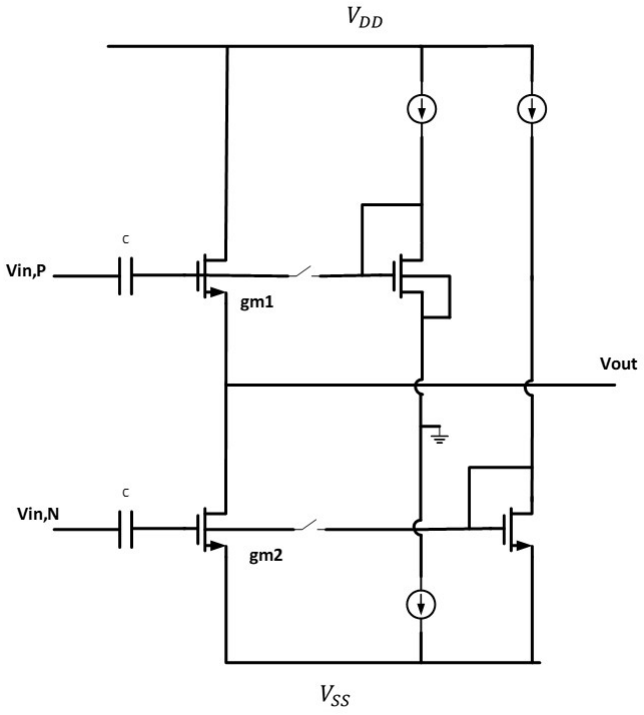


Figure 4.15: The buffer stage, differential to single-ended amplifier

The bulk of the upper NMOS transistor is connected to its source to further decrease the output impedance, which is expressed by:

$$\mathrm{R_{out4thstage}} = \frac{1}{\mathrm{g_{m1}}}||\frac{1}{\mathrm{g_{mb}}}$$

Since previous amplifier gain stages are biased at the level of mA or hundreds of μA, it is worth increasing the bias current of the buffer stage in the order of tens of μA to increase g_{m1}, g_{mb}. In this case, the output pole of the whole amplifier can be pushed further away from the dominant pole to the higher frequency to keep the whole system much more stable. The design choice discussed in 3.4.1 about load resistance of 500 Ω at the cost of power consumption and gain reduction is not worthy. Though by adding output resistance the closed-loop bandwidth will be higher, the output impedance of the buffer stage can already provide enough margin for both closed-loop bandwidth and the second pole for stability.

5

PERFORMANCE

5.1 AC RESPONSE

To simulate both the gain and bandwidth of the combined TGC-LNA amplifier, an AC analysis was performed. Figure 5.1 illustrates the closed-loop AC response of the designed TGC-LNA. Since the receive period is 100μs, the closed-loop gain was simulated at every 10μs, each corresponding to a different gain setting. The AC response indicates that the DC gain varies from 65 to 105 dBΩ, demonstrating that the gain changes by the required 40 dB during the receive period.

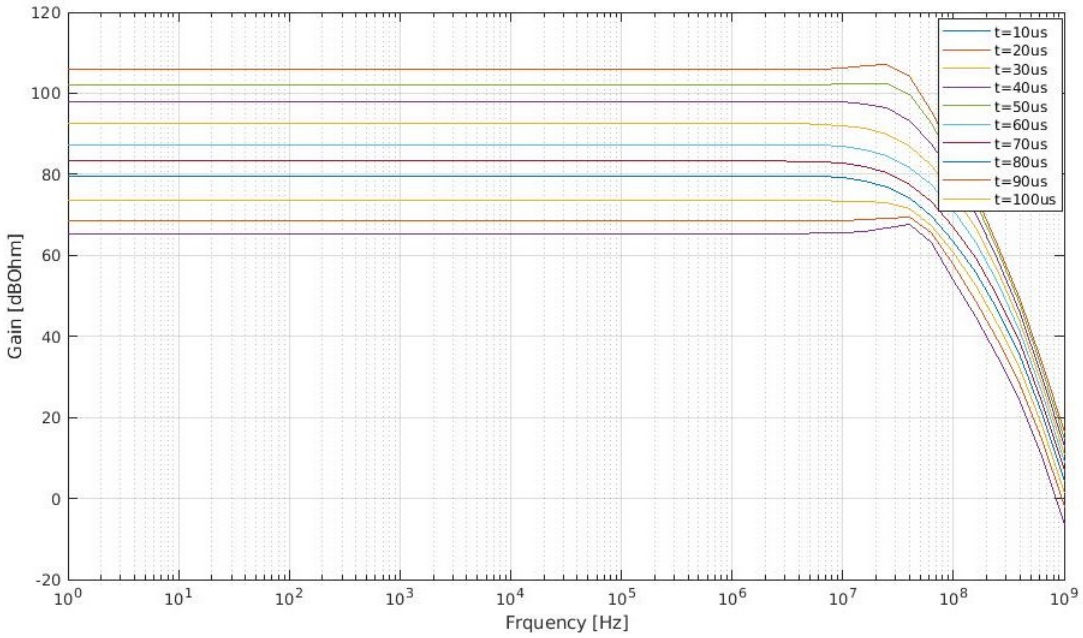


Figure 5.1: The AC closed-loop gain and bandwidth at different gain settings

To meet the gain range requirements within the desired bandwidth, the closed-loop bandwidth must be at least as wide as the bandwidth of interest. Since the transducer operates between 5 and 10 MHz, the -3 dB bandwidth should exceed 10 MHz. In Figure 5.2, it is evident that the -3 dB bandwidth is indeed greater than 10 MHz. The bandwidth does change over time and it remains at least twice as large as the required bandwidth. As a result, both the closed-loop gain and bandwidth meet the necessary requirements.

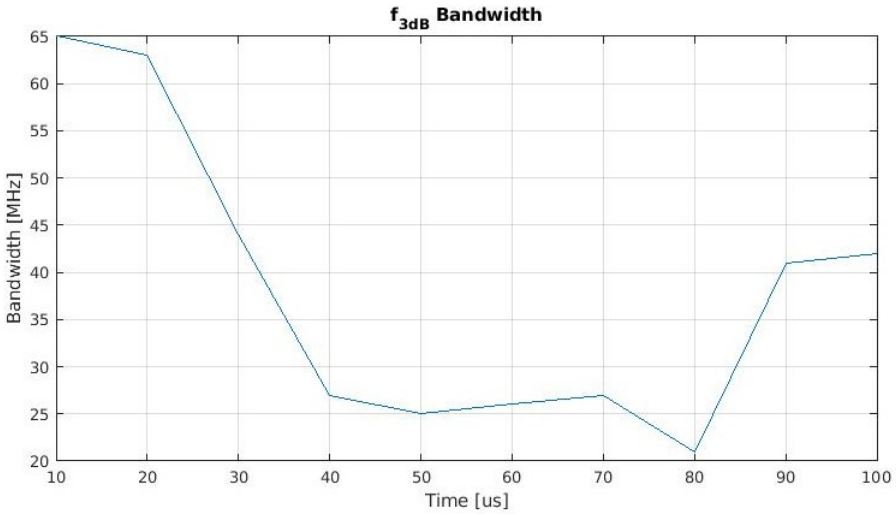


Figure 5.2: -3dB bandwidth variation over time

However, the closed-loop frequency has a large variation at both the beginning and end of the time period which has over 2X larger than the average frequency at around 25 MHz. The significant increase in bandwidth is likely caused by the small resistive loads from the triode transistors together with the amplifier in the second and third loads. There could probably be mismatch of the half-discharging current drifting compared to the feedback network that results in the larger bias voltage to bias the gate of the load transistors in the amplifier than desired. The on-resistance will then be lower than expected, the bandwidth has to increase to compensate for the reduced load resistance. The other reason is that with large M factors in load triode transistors, the parasitic capacitance reduces the effective impedance in high frequencies. The interaction between the smaller resistance and these parasitic capacitances is amplifying the bandwidth effect, leading to the observed 3x increase. In the middle of the frequency range, the feedback loop is effectively controlling the system, keeping it stable and preventing peaking. This is because the loop gain is still high, and the feedback has enough bandwidth to suppress any distortion or resonances.

5.2 STABILITY

The goal of LNA is low-noise, varying gain to maintain a constant unity-gain bandwidth. The stability of the loop is vital to check. Figure 5.3 and 5.4 illustrate the loop gain and phase of the loop amplifier respectively that the DC gain is varying over time to maintain a constant UGBW by matching the varying dominant pole.

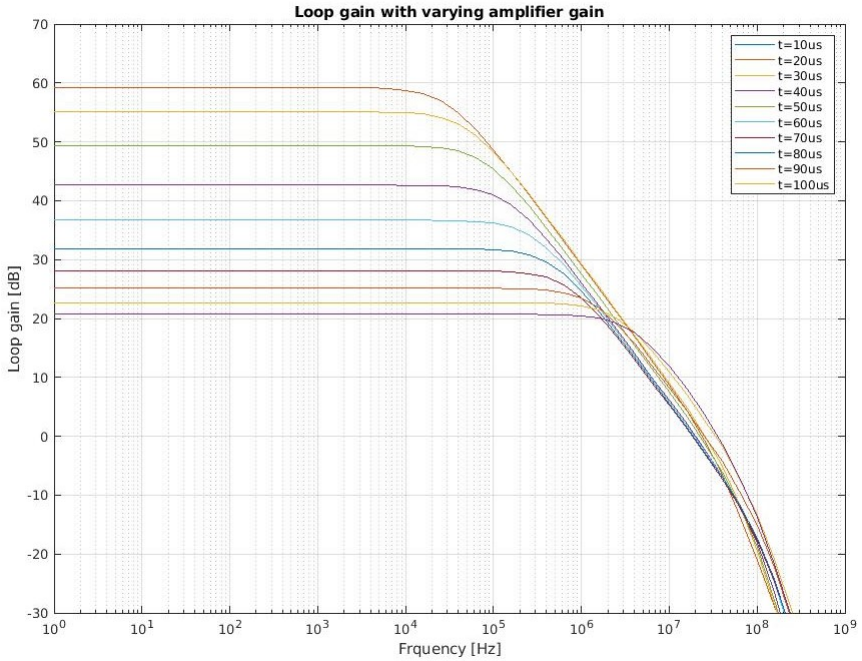


Figure 5.3: Loop gain of the loop amplifier

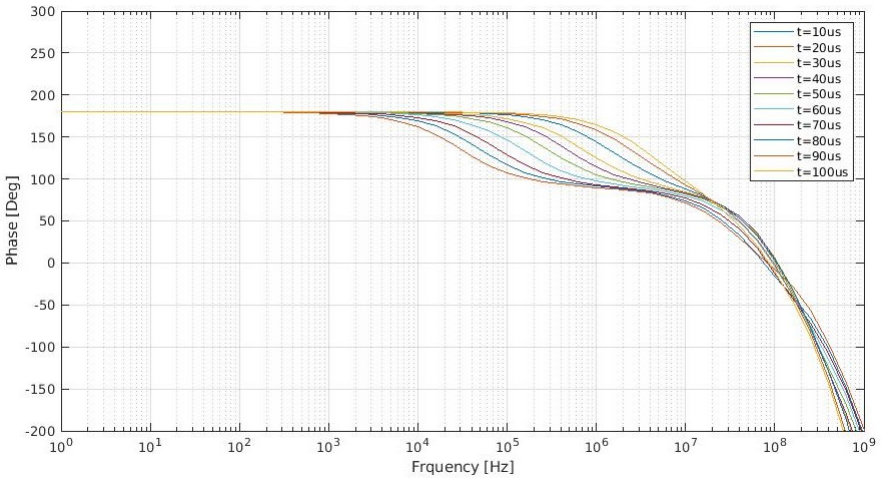


Figure 5.4: Phase of the loop amplifier

The overall phase margin shown in Figure 5.5 is above 45 degrees which proves the system is stable. At the beginning of the receive period, the PM is not as large as the rest of the time. The reason is the mismatch of the feedback resistance and the varying load resistance in the loop amplifier so the feedback is not adequately compensated for the high gain at the beginning of the receive period. The matching performance can be also determined and proved by UGBW shown in Figure5.6 that the UGBW is kept almost at the same frequency at larger gain settings while shifting around 20 MHz at the beginning of the time period.

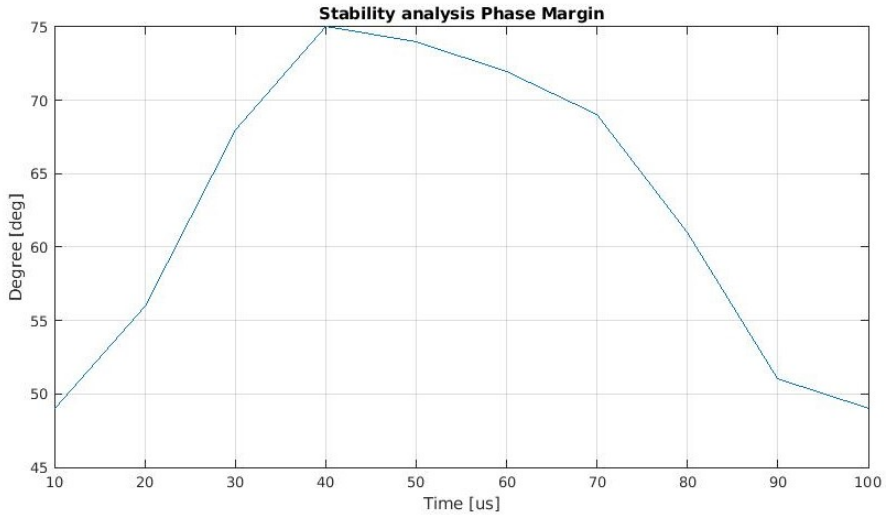


Figure 5.5: Phase margin of the loop amplifier

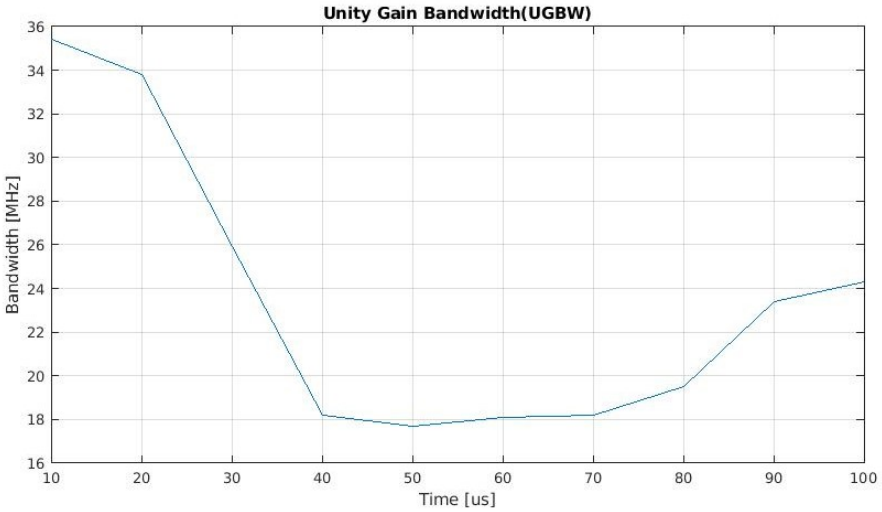


Figure 5.6: UGBW of the loop amplifier

Apart from phase margin, the gain margin stays larger than 10dB in Figure 5.7 showing the system is stable with positive and large numbers, verifying the LNA's stability.

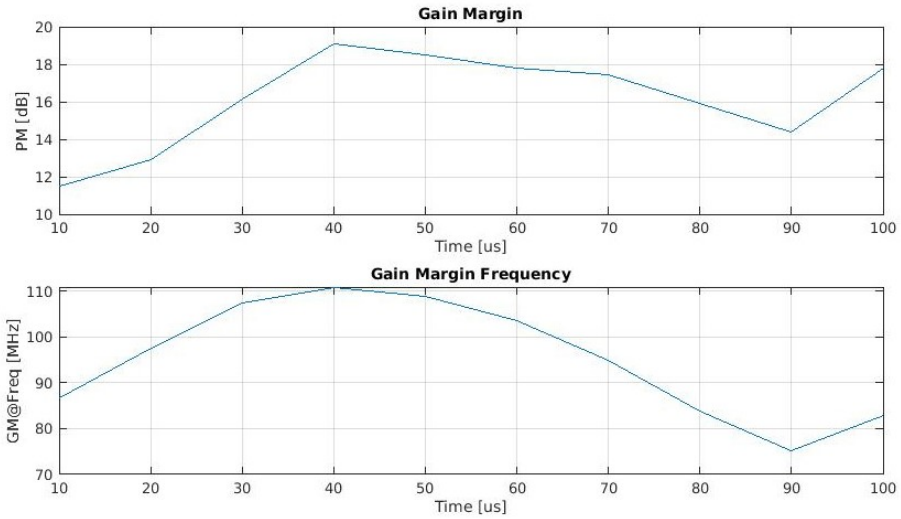


Figure 5.7: Gain margin and frequency of the loop amplifier

5.3 TRANSIENT RESPONSE

Figure 5.8 illustrates the output transient response by applying the exponentially decaying sinusoidal signal at the input. The input signal is a sinusoidal signal with amplitude varying from 50 μA to 0.5 μA at 7.5 MHz. The result proves by applying a 40dB variation input current, the output amplitude voltage delivers an almost constant envelope varying from 84 mV to 112 mV.

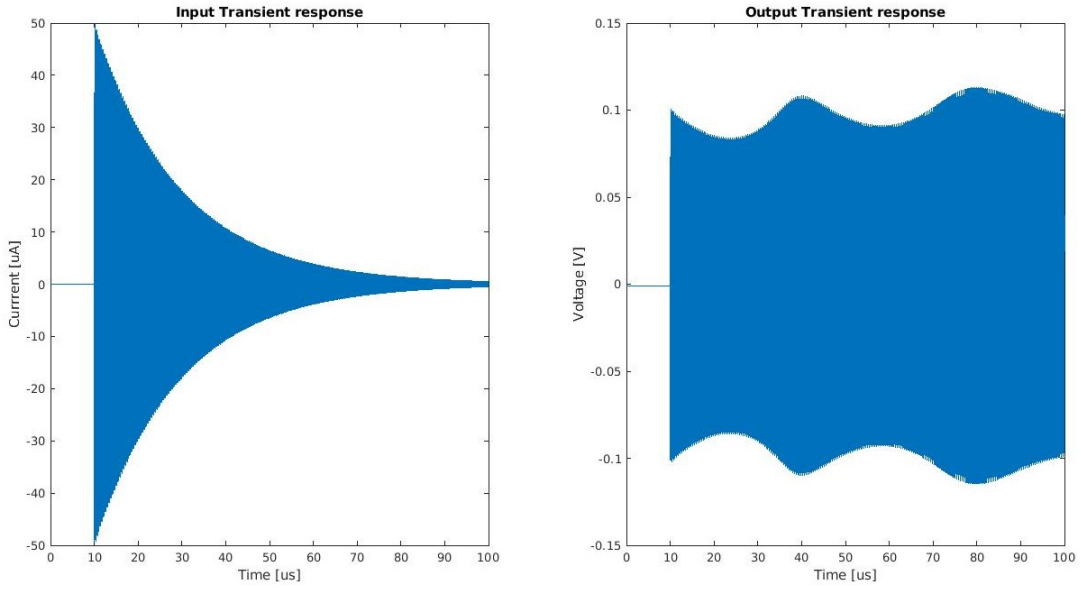


Figure 5.8: Transient response input and output of proposed TGC-LNA

It can be seen that the output exhibits a nearly constant amplitude for most of the duration around 100mV, with noticeable variations in the output waveform at later time intervals. This indicates that the TGC functionality is largely fulfilled, as the system is compensating for the diminishing input signal by maintaining a relatively constant output

voltage. However, the variations in the output signal amplitude suggest some non-linearity in the compensation process. Since the MOSFET-C network is utilized to discharge the triode devices instead of the RC network, the gain obtained is not a pure exponential curve. The gain deviates from the ideal linear-in-db curve due to the parallel structure, resulting in three variations where the parallel branch switching moments happen in the feedback network.

5.4 GAIN ACCURACY AND DISTORTION

Figure 5.9 shows the simulated gain results compared to the ideal linear-in-dB gain curve. The gain error is between -0.8dB to 1.2dB. The gain error is a systematic issue that can be compensated for during external post-processing.

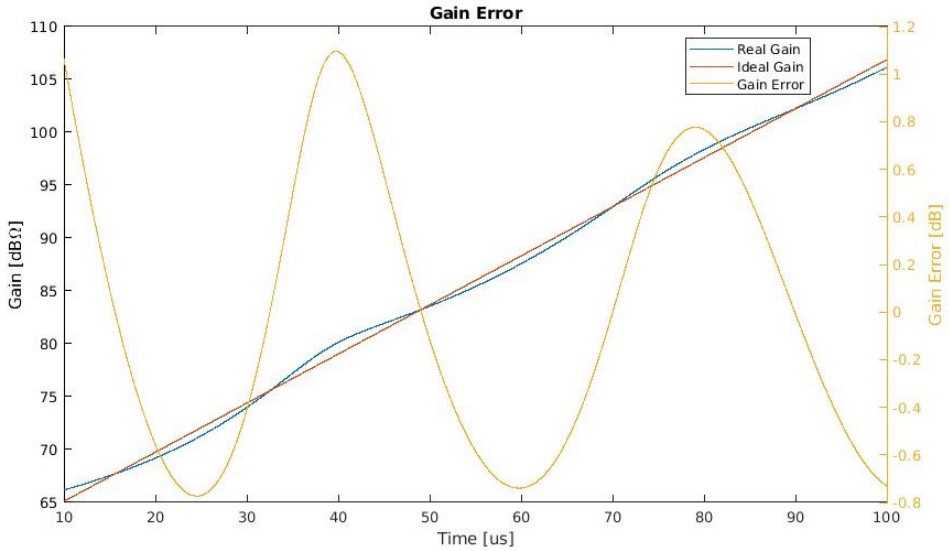


Figure 5.9: Gain accuracy

Figure 5.10 illustrates the output spectrum at each 10 μs time interval. The fundamental harmonic (HD1) corresponds to the 100 mV output voltage. It is evident that the primary contributors to the Total Harmonic Distortion (THD) are the second harmonic (HD2) and third harmonic (HD3). HD2 arises from the imbalance of the differential circuit, or mismatch in the feedback network that result in imbalance. On the other hand, HD3 is primarily due to the limited linearity of the input transistors.

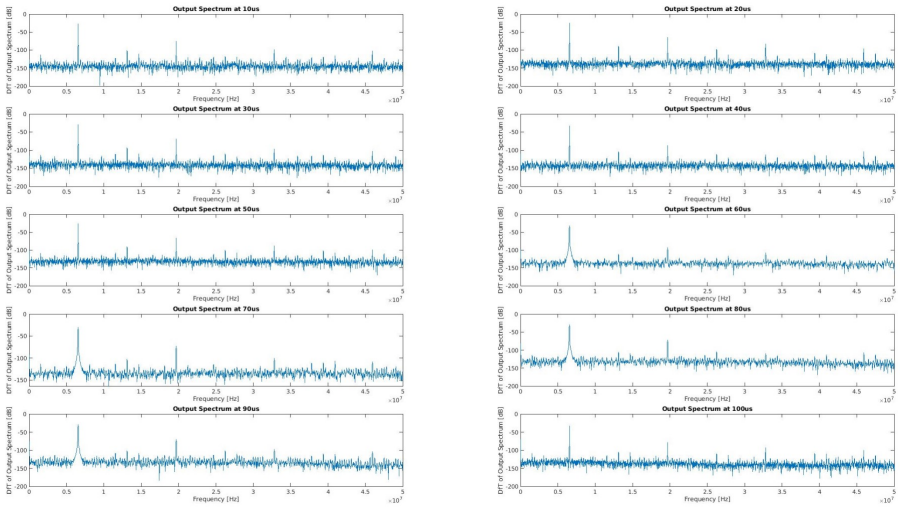


Figure 5.10: DfT Output spectrum at every 10 μs interval

Figure 5.11 shows the total harmonic distortion is overall lower than -40dB, which meets the linearity requirements. However, together with the closed-loop gain in Figure 5.2, the beginning of the time period has some non-linearity. The loop gain is also at its minimum, causing the virtual AC ground to no longer function effectively. As a result, the input signal experiences a swing, which is then amplified and leads to an even larger signal swing in the subsequent stages. This increased signal exceeds the operating range of the transistors in the later stages, pushing them into their non-linear regions and causing significant distortion. In contrast, at higher gain settings, the loop gain is greater, improving stability and reducing signal swing, which helps maintain the MOSFETs in their linear operating regions and results in lower Total Harmonic Distortion (THD).

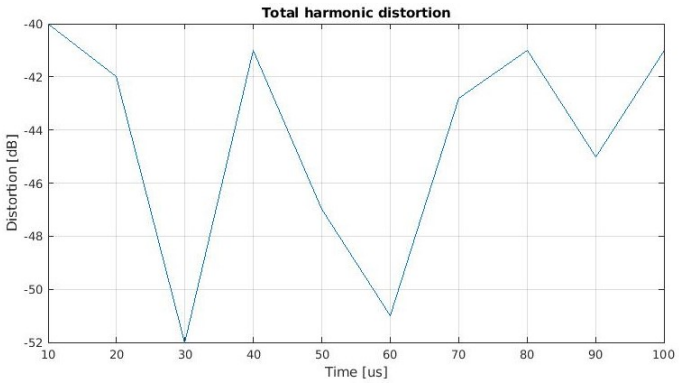


Figure 5.11: The total harmonic distortion over time period

5.5 NOISE PERFORMANCE

The noise target is $1\mathrm{pA}/\sqrt{\mathrm{Hz}}$ at 7.5MHz at the highest gain setting. Since the center frequency is 7.5MHz, a symmetrical frequency range around the center frequency is integrated and checked by extending an equal bandwidth on both sides of that center frequency. The lower and upper frequencies are determined by subtracting and adding half of the

bandwidth to the center frequency, respectively. Integrating from 3.75MHz to 11.25MHz, the simulated input referred noise should be below 2.738 nA.

Figure 5.12 shows the input and output referred noise density. The input-referred noise density is the lowest at the highest gain setting. The simulated input referred noise density is 985 $\mathrm{fA}/\sqrt{\mathrm{Hz}}$ at the center frequency.

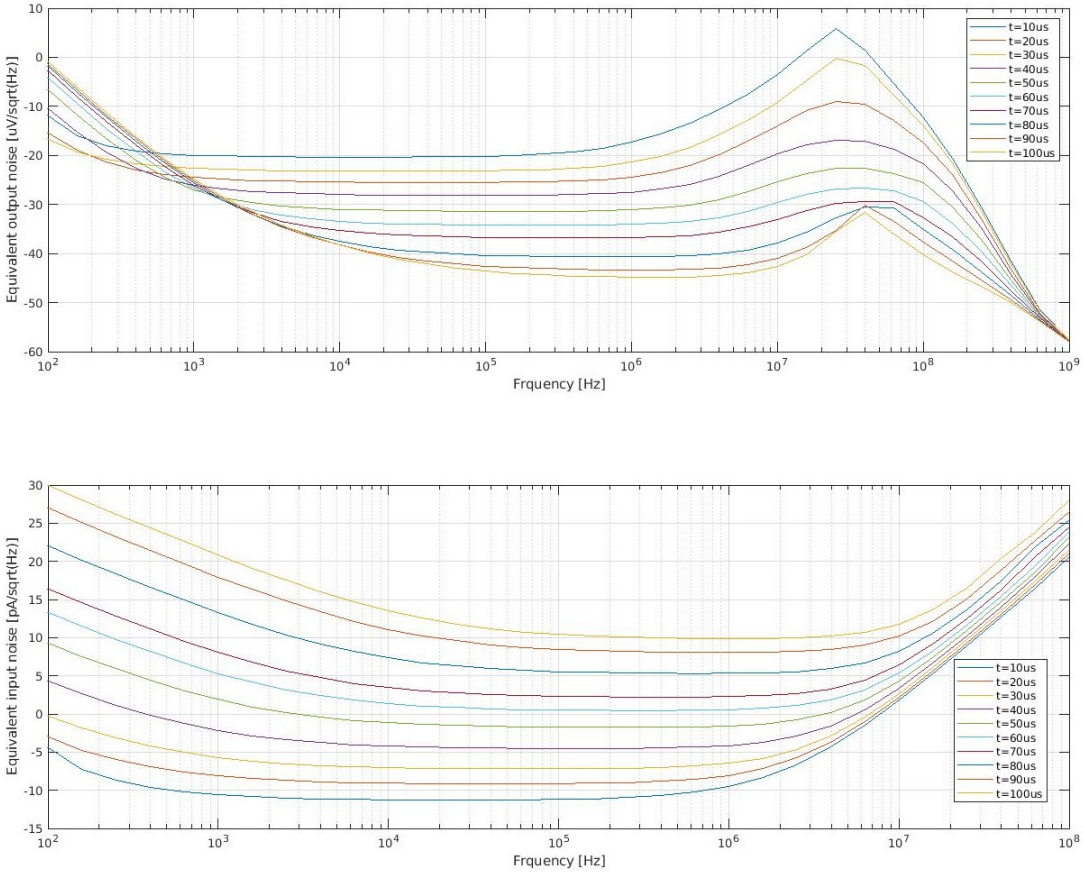


Figure 5.12: Input and output referred noise densities

The simulated input referred noise at the highest gain setting is 2.729 nA which proves the noise requirement. Figure 5.13 shows the integrated noise over bandwidth around 7.5 MHz at every 10 μs.

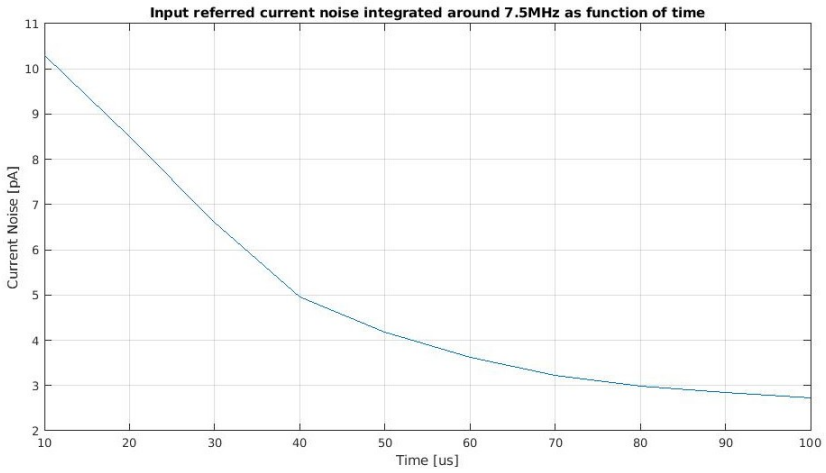


Figure 5.13: Integrated noise over bandwidth around 7.5 MHz at different time

5.6 POWER CONSUMPTION

The computed average power consumption is 4.74mW presented in Figure 5.14. The result is significantly lower than the power consumed in [16] and [15]. The reason is that the current in the second and third stages is significantly reduced by using more load triode transistors in parallel. The area these load triode transistors consume is relatively smaller compared to the feedback network reuse as amplifier loads in [16].

The first stage contributes 50% of the total power consumption, followed by the second stage 10.5% and the third stage 7.5%.

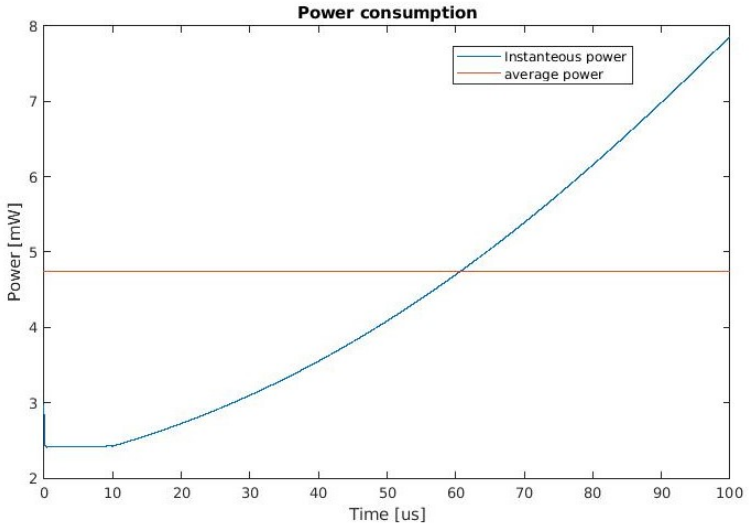


Figure 5.14: Input and output referred noise densities

5.7 SENSITIVITY TEST

Table 5.1 shows the result of the sensitivity text of the gain curve over the time period. Four main tunable parameters can be adjusted to control the overall gain curve as designed:

reference resistor R_{ref}, bias current in three branches I_{drift1}, I_{drift2} and I_{drift3} as discussed in section 4.1.2. It can be seen that by tuning the reference resistor R_{ref}, the gain can be overall increased or decreased to a certain range because the R_{ref} defines the initial resistance value of the back-to-back triode transistors M_{triode}. I_{drift1}, I_{drift2} and I_{drift3}, on the other hand, can control certain intervals of the gain curve where I_{drift1} controls the last time interval, I_{drift2} controlling the intermediate and I_{drift3} changing the beginning of time intervals. I_{drift1} is the branch of the lowest gain of three parallel branches while I_{drift3} controls the branch that goes off the first. This approach is useful against the PVT variations and mismatches. If the gain curve is spread over corner variations much, the currents and resistors canbe trimmed to help to compensate the curve back to the desired values.

Gain difference [dB]				
time interval	0μs - 100μs	60μs - 100μs	30μs - 80μs	10μs - 50μs
controllable unit	Reference resistor	I_{drift1}	I_{drift2}	I_{drift3}
20%	7.5	7.5	2.5	1.3
10%	5	4.5	1.4	0.65
5%	2.75	2.6	0.75	0.375
2%	1.4	1.125	0.32	0.15
1%	0.65	0.57	0.16	0.075
0.5%	0.35	0.3	0.08	0.04
-0.5%	0.35	-0.32	-0.07	-0.03
-1%	-0.65	-0.65	-0.16	-0.075
-2%	-1.25	-1.3	-0.35	-0.15
-5%	-3.75	-3.5	-0.9	-0.43
-10%	-7.5	-6.5	-1.8	-0.89
-20%	-12	-10.5	-4	-2

Table 5.1: Sensitivity test result

5.8 AREA ESTIMATION

The area estimation for the LNA channel is based on the dimensions of the transistors and the overall capacitance used in a single channel. This includes all the necessary components such as the feedback network, loop amplifier, and biasing circuits integral to the LNA design. Based on the automatic layout, the estimated area required for all the transistors and capacitors is approximately 62,500 m^2. This estimation accounts for both the channel area and the source-drain connections, though it excludes the interconnections between components.

To account for potential variations and uncertainties in the layout process, such as process variations, misalignment, or parasitic effects, a 30% margin of error is applied. This results in a revised estimated area of around 81,250 m^2. Given that metal-insulator-metal (MIM) capacitors are used, these capacitors are strategically placed on top of the transistors in the upper metal layers, typically 5th or 6th layers, which maximizes the use of vertical space and minimizes the overall footprint of the design.

The increased area of this design compared to [16] and [15], which is approximately twice as large, can be attributed to several key factors. One of the main reasons is the inclusion of a more extensive biasing network designed to prevent PVT variations. Ensuring robustness against PVT requires additional circuitry, which inevitably increases the overall area, consuming around 26000 um^2.

Moreover, using large resistors as references plays a significant role in the increased area. In this design, poly resistors with an area of around 600 µm² are used. These large resistors are necessary to maintain stable reference values and ensure consistent performance across varying conditions, which is critical in designs sensitive to process variations.

Additionally, the load in the amplifier employs a high multiplication factor to accommodate the lower current use of the amplifier to achieve the desired gain. This approach, while improving the current handling capabilities of the amplifier, requires larger devices, which further contribute to the total area. As a result, the combination of these design choices—additional biasing circuitry, large resistors for reference, and oversized amplifier loads—leads to an area that is approximately double that of comparable designs in [16] and [15].

6

CONCLUSION

In this chapter, the innovation aspects and performance of the design are summmarized and compared with the prior art. Followed by the improvement aspects and future works.

6.1 CONCLUSION

This work presents a compact ultrasound low-noise amplifier with 40 dB built-in TGC function.

The LNA and TGC functions are implemented using a closed-loop structure, enabling separate design for the feedforward and feedback paths. The feedback path consists of a resistive network made up of three parallel back-to-back triode transistors in such way that the distortion and die area requirements are minimized. As the control voltages decrease at varying rates, different branches in the resistive network dominate across specific portions of the gain range of 40 dB. A linear discharge network is employed to replicate the exponential behavior of the control voltage of a capacitor. This compact circuit introduces minimal noise from other sources while allowing the floating nodes to discharge safely. Also, the area can be minimized compared to the RC discharge network, realizing an approximate exponential gain curve. The gain errors are introduced in this case, but it is designed within the $\pm$ 1dB range and can be feasibly controlled between parallel switching moments during the 100 μs period by separately controlling the current drifting at each branch. This trimming method can compensate for the mismatches.

The feedforward path, consisting of a four-stage loop amplifier, helps with the low-noise functionality while saving power by utilizing the current-reuse topology amplifier structure in the first stage. Besides, the LNA has a functionality of variable DC gain to match the feedback variations of 40dB to maintain a constant UGBW. This benefits stability and bandwidth at the highest gain settings. Also, the power is less consumed. The biasing of the first stage also increases over time to adapt to the increased transconductance of the first stage to avoid wasted power consumption. The two intermediate stages have each 20dB load variations to achieve the altering 40dB DC gain for the constant UGBW. The loads operate similarly with the feedback discharging transistors to match with the feedback network and can be feasibly controlled by the ratioed discharging voltage in the feedback network. The last stage is differential to single-ended buffer, which also contains the driving capability. The LNA achieves the noise target of 1 $\mathrm{pA}/\sqrt{\mathrm{Hz}}$ at 7.5MHz at the highest gain setting by maintaining a relatively low power consumption of 4.74mW from

$\pm$ 0.9V supply and 0V to 1.8V biasing supply. The LNA also suppresses the THD below -40dB.

Figure 6.1 shows the comparison of this work to the prior art. Compared to [16], the power consumption is less because [16] utilizes the back-to-back triode transistors again in the amplifier loads, which consumes more power, also the first stage consumes more power in [16] to achieve high noise target. In this work, the noise target is met at the lowest of 0.99 $\mathrm{pA}\sqrt{\mathrm{Hz}}$ at the center frequency compared to [15], [14] and [16].

	This work	[14]	[15]	[16]
Process	0.18 µm CMOS	0.18µm HV BCDMOS	0.18 µm CMOS	0.18 µm CMOS
TGC type	approximate exponential	ITP	approximate exponential	approximate exponential
bandwidth [MHz]	30	7.1	20	50
Max gain [dBΩ]	110	107	100	106
Gain range [dB]	45	33	40	40
Gain error [dB]	± 1	± 1	± 1.4	± 1
Input capacitance [pF]	18	15	18	18
Noise density at center frequency [$\mathrm{pA}/\sqrt{(\mathrm{Hz})}$]	0.99 @7.5MHz	1.7 @ 5MHz	1.12 @ 7.5MHz	1.15 @ 7.5MHz
Power consumption [mW]	4.74	5.2	5.5	6
Worst THD [dB]	-40	–	-44	-40
Area [mm^2]	0.0625	0.12	0.013	0.0339

Table 6.1: Prior comparasion

6.2 FUTURE WORK

This design has been validated through circuit simulations. However, both layout and post-layout simulations are still necessary before creating a prototype. Though with the design from this work, the trimming of mismatches can be realized, conducting corner simulations is crucial before manufacturing, as they ensure the loop meets the target specifications across PVT (Process, Voltage, and Temperature) variations. Some self-biased network circuits or adaptive biasing can be a way of improving the feedback network.

The second optimization focuses on addressing distortion issues, which are most pronounced during large signal swings. The worst Total Harmonic Distortion (THD) occurs when the signal amplitude is high, causing the circuit's gain to vary with the input level. To mitigate this, a linearization technique is needed to minimize the gain's dependence on the input signal. One effective approach is to implement source degeneration and a local feedback network in the third stage, which helps to improve the overall linearity by stabilizing the gain and reducing the impact of large signal swings.

Besides, the biasing network can be further simplified in that three branches can share one biasing current with different ratioed current drifting, which benefits the area consumption. The replica biasing can be further improved. While area and M factors of the transistors as amplifier loads can be further optimized.

Currently, the exponential voltage generator is biased using constant voltage sources, which makes the system susceptible to gain variations. A dedicated bias circuitry for the control voltage generator is yet to be designed.

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