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Cyber-Physical Testbed Co-Simulation Real-Time: Normal and Abnormal System Frequency Response

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***Abstract*—Future carbon-neutral power systems impose many challenges; one is the urgent need for a simulation platform that allows replicating the complex systems' actual dynamic performance. This paper shows the results of implementing a cyber-physical testbed co-simulation in real-time to analyse the system frequency response considering primary frequency control and emergency frequency control: under-frequency load-shedding (UFLS) protection schemes. The proposed testbed uses a physical layer of two real-time simulators from different vendors in a closed loop, Opal-RT OP4510 and Typhoon HIL 604, being the first simulator for test system modelling and the remainder used to implement the UFLS protection scheme. Two connections of the real-time simulators are considered: physical connection using wires to exchange analogue signals and cybernetic digital communication using ANSI C37.118 communication protocol. The cybernetic layer of the testbed models a test system, controls the real-time simulation, and implements digital communication between the simulators. A modified version of the P.M. Anderson 9-bus systems is used for testing purposes, including phasor measurement units (PMUs). Results of the real-time simulation show the appropriate performance of the proposed testbed.**

***Index Terms*—ANSI C37.118, Co-simulation, hardware-in-the-loop, low inertia power systems, real-time, system frequency response.**

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I. Introduction

POWER systems are evolving at breakneck speed toward reaching a carbon-neutral status. Massive energy integration from renewable sources displaces conventional synchronous units from the generation mix, causing several challenges for the secure and economical operation of the electrical power systems, such as reducing the short circuit level, system strength reduction, and reduction in the total inertia of the system, etc. The dramatic decrease of the system's rotational (mechanical) inertia and system strength makes the power system dynamics volatile, with more extreme deviations and speed. Therefore, power systems engineers must consider departing from the classical off-line simulations, and more realistic simulation tools must be used adequately to study the impact of this inertia loss and establish the guidelines for the proper development of future power systems [1].

In this sense, *real-time simulations* (RTS) have been erected as the fundamental tool for testing computer models of physical systems. When the physical system is an electric power system, RTS is a technique for the transient simulation using a digital-computer time-domain solution [2]. However, RTS provide an umbrella for two categories of studies considering the physical domain: (i) fully digital real-time simulation that includes paradigms such as model-in-the-loop, software-in-the-loop, or processor-in-the-loop, and (ii) hardware-in-the-loop (HIL) real-time. In the latest one, part of the system (including control, protection, and other accessories) is modelled in the cybernetic layer and runs in the real-time simulator, and the physical layer is a real physical device involving interfacing or input/outputs (I/Os).

One of the challenges of modern power systems is the reduced rotational inertia and its impact on the power system frequency response. The authors are embarked on developing a platform for conducting rigorous, transparent, and replicable testing of scientific theories, computational tools, and innovative technologies. This scientific paper shows the results of implementing a cyber-physical testbed co-simulation real-time dedicated to normal and abnormal system frequency response (underfrequency load shedding (UFLS) protection schemes). The testbed is intended to use a real-time simulation approach

TABLE I
CURRENT TRENDS IN CYBER-PHYSICAL REAL-TIME CO-SIMULATION TESTBEDS

Reference	Device 1	Purpose of Device 1	Device 2	Purpose of Device 2	Communication
[11], [12]	Typhoon HIL 604	Reactive power control	N/A	N/A	N/A
[13]	OPAL-RT 5700	Microgrid modelling	N/A	N/A	N/A
[14]	RTDS	DC Microgrid modelling	N/A	N/A	Network emulator
[15]	OPAL-RT 5607 (Core 1)	Test system modelling	OPAL-RT 5607 (Core 2)	Intrusion detection system	Modbus and DNP3 protocols
[16]	OPAL-RT 4510	Distributed Energy Resources (DER) modelling	N/A	N/A	IEEE 2030.5 Standard
[17]	OPAL-RT 4510	Test system modelling	Typhoon HIL 604	N/A	Analogue
Proposed	OPAL-RT 4510	Test system modelling	Typhoon HIL 604	UFLS protection scheme	Analogue and ANSI C37.118

to obtaining the system frequency response of a representative test system when subject to a frequency disturbance: a selectable sudden generator outage or load disconnection. There is a large number of publications dedicated to showing real-time testbeds, some of them specifically dedicated to rapid prototyping [3], [4], control in the loop [5], [6], cyber aspects of power systems [7], [8], cyber-security [9], [10], etc.

In particular, some of the published research dealt with cyber-physical testbeds for co-simulation in power systems: In [11], [12], a cyber-physical co-simulation testbed is developed for real-time reactive power control of inverters in smart distribution networks. However, a single Typhoon HIL 604 simulator is used as the physical layer. Work in [13] deals with an improved distributed secondary control of DC microgrids. In this case, the cyber-physical system comprises only an OP5700 simulator to model the microgrid. In [14], a cyber-physical system is presented to analyse cyber adversaries and intrusions in DC microgrid clusters using a real-time simulator from the RTDS manufacturer and a virtual network as the communication layer. In [15], a novel intrusion detection system for distribution systems is realised using a cyber-physical real-time reference model. Although, in this case, the testbed incorporates real protection devices such as relays and a real-time automation controller, the test system and the intrusion detection system run from different cores of the same digital real-time simulator. Work [16] proposes a hardware-in-the-loop testbed for distributed energy resources management in real-time using IEEE 2030.5 standard. The physical layer of the testbed consists of a single OPAL-RT simulator. [17] introduces a cyber-physical testbed comprising two real-time simulators from different vendors for system frequency response analyses. However, analogue signals bypass one RTS, and no control or protection action is performed.

This scientific paper is different from all the previously published papers as this is dedicated explicitly to normal and abnormal system frequency response and considers co-simulation using two real-time simulators (different vendors) in a close loop, being one of the RTS used to model the test system and the remainder used to implement a protection scheme. The novelty in the testbed is related to three main aspects: (i) control modelling: primary frequency control for normal operation and emergency frequency control based on under-frequency load shedding application; (ii) use of multi-platform real-time simulators in the loop to provide scalability, flexibility and reliability to the testbed; (iii) mechanism to close the loop between the real-time simulators: (a) copper wired exchange of analogue signals (b) ethernet based exchange using ANSI C37.118 protocol based signals. Table I manifests the main contributions of the proposed testbed when compared to other existing methods, being the main differences in the use of two separated, non-synchronised real-time simulators, each one dedicated to different purposes and signal exchange based on ANSI C37.118 communication protocol. All the necessary files for replicating the results of this work are publicly available at [18].

The proposed approach offers several advantages; one is that the power systems can be modelled with a deeper level of detail, which means greater fidelity. Furthermore, the computational capacity is improved, making each real-time simulator more adequate for specific tasks. This work is an extension of [17], being the main contributions from the previous results:

- A new input/output (I/O) signal exchange based on the ANSI C37.118 protocol has been configured to establish communication between the two real-time simulators. In this way, the cybernetic layer is enhanced to include the real communication protocol and infrastructure. Adding the communication infrastructure adds the possibility of using the testbed for further specialised studies such as cyber-security (not included in the scope of this paper).
- Emergency frequency control is added as a UFLS protection scheme; this has been implemented in the Typhoon HIL 604 simulator using an ANSI 81 U frequency relay function. Therefore, the test system and the protection function are executed in non-synchronised separated real-time simulators, establishing a testbed based on hardware-in-the-loop.

The remainder of the paper is organised as follows: Section II presents the motivation of the cyber-physical testbed and different elements composing the layers; Section III briefly explains the implementation, and Section IV shows the simulation and results of the proposed testbed. Finally, Section V presents the conclusions of the work.

II. CYBER-PHYSICAL MODELLING

The proposed cyber-physical testbed co-simulation real-time is dedicated to analysing the system frequency response of a test system considering normal and abnormal scenarios; it consists

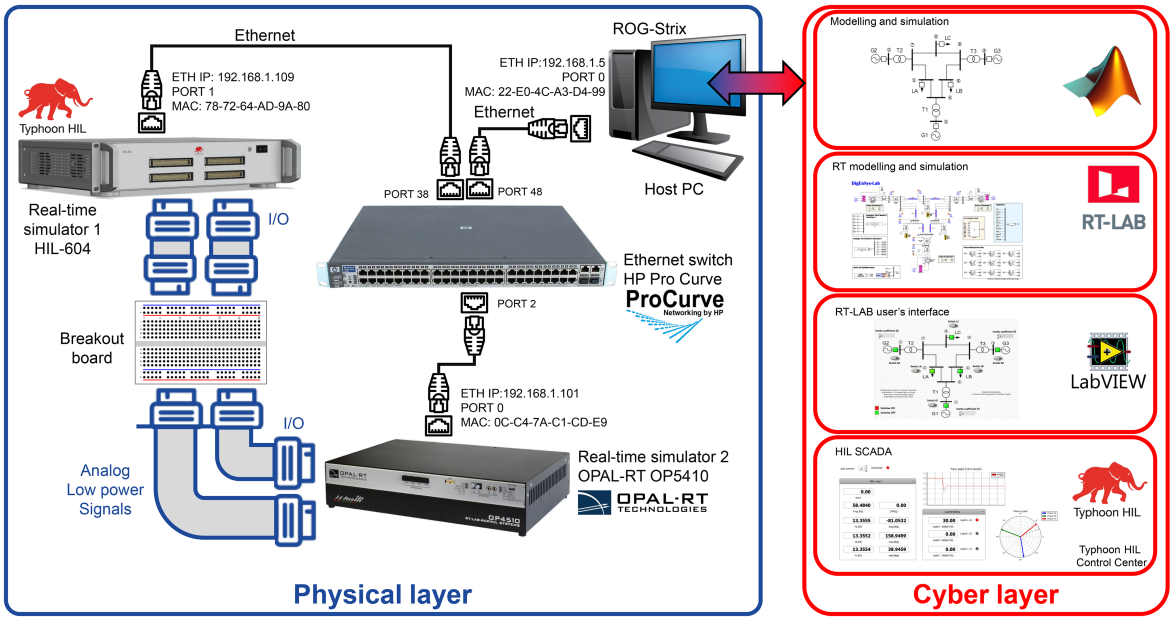

Fig. 1. General structure of the cyber-physical testbed co-simulation Real-Time for system frequency response analysis.

of two layers: (i) the cybernetic layer and (ii) the physical layer.

The cybernetic layer consists of the control and communication elements of the testbed; it includes the components used to monitor and control the physical layer, especially the software used for modelling and simulation of the power system test system and the digital communication via ANSI C37.118 protocol. For simplicity, all the software in the cybernetic layer is run, and they operate from the Host PC (depicted in Fig. 1).

The physical layer involves the hardware used in the testbed, as shown in Fig. 1, and it consists of two different vendors' digital real-time simulators: Typhoon HIL and OPAL-RT. The rationale behind using two real-time simulators from different vendors in a co-simulation framework and closing the loop using analogue electrical (voltages) and digital signals is to provide flexibility and scalability. In fact, the idea is to use these signals to feed physical devices for measurement, control and protection, including phasor measurement units (PMU) and merging units in future testbed developments.

The two information exchange schemes between the simulators are depicted, the wired interface used to interconnect the analogue and digital I/O of the simulators and a digital communication using ANSI C37.118 using copper-ethernet-based cables and an Ethernet switch (HP ProCurve 2610-48). In addition, a digital oscilloscope (not shown in Fig. 1) is used to monitor and capture the analogue signals in the wired close loop between the simulators–Fig. 1 details IP and MAC addresses, Ethernet ports, and connections in the proposed testbed. The following subsections provide more information regarding the modelling used in these layers with their main components.

A. Cybernetic Layer

The core of the cybernetic layer resides inside the Host PC and includes software required for modelling/simulation and to control the digital real-time simulators. The Host PC is based on a Microsoft Windows 11 Home edition operating system; for simplicity in the design of the testbed, the proprietary software for modelling/simulation and running/control of the real-time simulators are running in the same Host PC: Typhoon HIL Control Centre 2023.2 and OPAL-RT RT-Lab 2023.1.0 are used for Typhoon HIL 604 and OPAL-RT OP4510, respectively. In this version of the testbed, a test system is implemented in the OPAL-RT RT-Lab 2023.1.0, and the Typhoon HIL framework is used to implement an under-frequency load shedding protection scheme considering ANSI 81 U under frequency relay function.

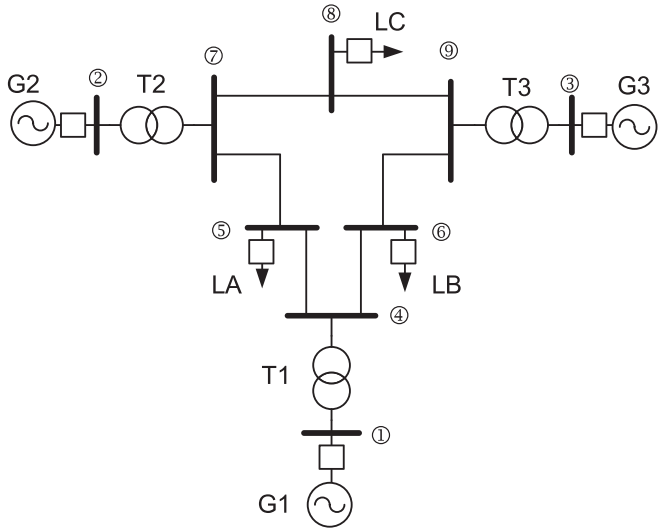

Fig. 2. Test system: a modified version of the P. M. Anderson 9-bus test system [19].

1) Test System: In this paper, a simplified version of the Western System Coordinating Council (WSCC), as described in [19] (see Fig. 2), is used as the test system. It consists

of three synchronous generators, three dynamic loads, three two-winding power transformers and a transmission system of 230 kV. The original test system has been slightly modified: the loads have been deliberately modelled as constant, its initial load has been reduced by 20%, and the two-winding power transformers are considered connected following the Yy0 vector group. The constant PQ model allows the absorbed active power of the loads can be modified in real-time, simulating the trip of an under-frequency (UF) relay and, therefore, shedding part of the load.

As the main interest of the proposed testbed is to mimic a real system during a frequency event, the system is equipped with measurement devices; as a consequence, the buses where there are generation units have been equipped with Phasor Measurement Units (PMUs) to provide measurements of voltage magnitudes ($\boldsymbol{V_{abc}}$), voltage angles ($\boldsymbol{\phi_{abc}}$) and frequency at each measurement point. A three-phase-locked loop was used to represent PMUs, which calculates the positive-sequence component of the input three-phase signal over a running window.

Typical system frequency response is excited by a frequency disturbance. In this testbed, the authors included two types of single contingency events: (i) sudden disconnection of a specific load and (ii) sudden disconnection of one synchronous generation unit. As a consequence, the test system is equipped with six (06) three-phase circuit breakers (CB); each breaker will allow the disconnection of one power equipment (generator or load) during the real-time simulation.

2) Under-Frequency Load Shedding Scheme: The UFLS is an emergency mechanism used in power systems to avoid large drops in frequency. It disconnects a specific load when the measured frequency falls below a threshold. In this paper, the under-frequency load-shedding scheme has been modelled using the ANSI 81U UF relay function. Bus 5 in the test system has been equipped with a UFLS scheme to protect the system against potential blackouts. It is worth noting that setting the optimal configuration and location of under-frequency relays is a complex task [20]. This paper intends to prove the correct functioning of a UFLS protection scheme in a hardware-in-the-loop environment rather than design the optimal UFLS protection scheme.

3) Monitoring and Control System: The monitoring and control system is a Graphic User Interface (GUI) that allows visualise and control simulations in real-time. In particular, this GUI is customised to present the signals generated by PMUs as measurements of the electrical signals in the test system during the real-time simulation; also, the GUI graphically shows the actual status of the six circuit breakers installed in the test system, the numerical values of the rotational inertia constant (H in seconds) of each synchronous generator are presented, and the status and load shedding amount of the UF relay. On the other hand, the GUI is designed to execute control commands in the test model during the real-time simulation by an appropriate flow of control signals. The customised GUI provides complete user control on the status (open/close) on each of the circuit breakers installed at the loads and generators, all of this to allow the user to insert a single contingency (generator disconnection or load disconnection).

The GUI includes the possibility of modifying the rotational inertia constant of each generator during the real-time simulation. However, the authors recognise that it is not a realistic disturbance and is not intended to do so. Instead, it is included as an option for the user to set the value of the rotational inertia of each generator before inserting the disturbance; it will allow the user to define scenarios with different inertia without stopping the real-time simulation and compile/rebuild the simulation model.

4) Digital Communication Protocol: The closed-loop real-time simulators can communicate by two approaches in the proposed testbed: analogue and digital communication. Analogue communication allows the exchange of whichever signal in the test system and the UFLS protection scheme through analogue low-power voltage signals. On the other hand, digital communication is performed through the ANSI C37.118 protocol, which is dedicated to synchrophasor broadcasting. The protocol defines data packets that contain three current and voltage phasors in either polar or rectangular form and frequency and Rate of Change of Frequency (ROCOF) values. The information flow in this protocol is unidirectional, which means that in every digital communication established, there is one device acting as a slave (also known as the publisher, the device which sends data) and another one acting as a master device (also known as the subscriber, the device which receives the data). In the testbed proposed, both real-time simulators act as master and slave simultaneously as they send and receive data from the other simultaneously.

B. Physical Layer

The physical layer is where the co-simulation environment occurs, with two non-synchronised real-time simulators (two different vendors) executed simultaneously but separately, exchanging I/O voltage analogue signals using traditional copper wires and digital signals through a digital communication protocol, and an oscilloscope is used to record physical voltage signals during the real-time simulation. The two real-time simulators in the close-loop co-simulation environments are: (i) OP-4510 from the company Opal-RT, which consists of the main CPU based on Xeon four-core processors and a powerful Xilinx Kintex 7 FPGA; also, it includes digital and analogue I/O. (ii) HIL 604 from Typhoon HIL includes eight processing cores, 2 ARM cores, and digital and analogue I/O.

The loop between the real-time simulators is closed by a galvanic connection using copper wires and a breadboard interconnecting their I/O analogue cards. In addition, the two real-time simulators are connected through copper-based Ethernet cables to establish a digital communication channel. An oscilloscope (Tektronix TBS 1052B-EDU) is installed in the physical layer to display and record analogue voltage signals exchanged in the closed loop. The configuration and execution of the simulators are controlled from the Host PC running the appropriate proprietary software. The Host PC is a workstation based on Ryzen 9 3900X (12 cores), 16 GB of RAM, 1 TB SSD GeForce RTX 2070 SUPER; the computer has an operating system, Microsoft Windows 11.

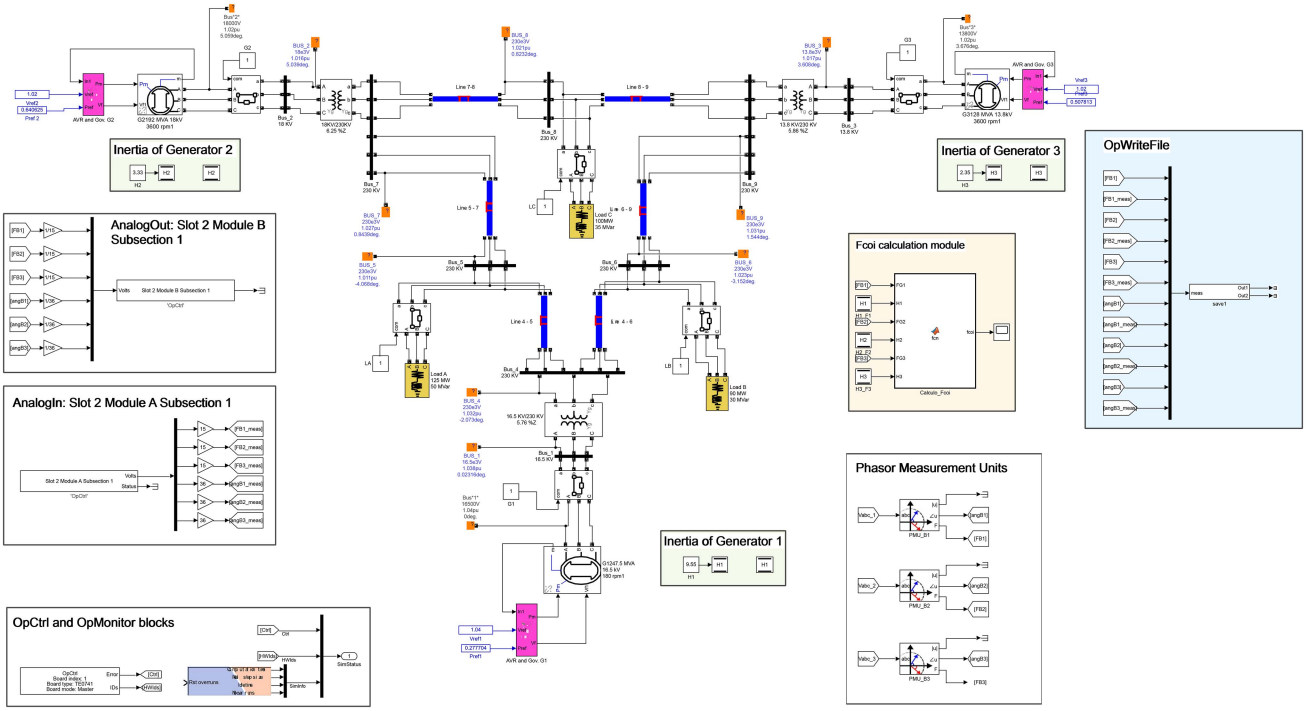

Fig. 3. Overview of the SM_Master subsystem, which includes the test system and additional blocks used in the Real-Time simulation.

III. Implementation

A. Cybernetic Layer

The cybernetic layer is used to create the model of the two main components: the power system test system and the UFLS scheme; additionally, the signal flows (I/O), and the customised GUI is created in this layer. The test system was initially developed using MATLAB Simulink R2021b and then transferred into the OPAL-RT proprietary software RT-Lab v2023.1.0. The customised GUI consists of two parts: the RT-LAB interface was created using LabView 2017 (32 bits) and fully integrated into RT-LAB, and the Typhoon HIL Control Centre's interface was designed using HIL SCADA panels. The following subsections explain the implementation steps of the test system, the monitoring and control system (GUI), the communication protocol and the UFLS protection scheme.

1) Test System: The model of the 9-bus test system has been implemented in MATLAB/Simulink (version R2021b), making it easy to import into the RT-LAB simulation environment. The Simulink file (.slx) must be appropriately separated into subsystems for real-time simulations in RT-LAB. In this very specific, two subsystems have been defined: the SM_Master subsystem, which is the core of the simulation, and the SC_Console subsystem, designed for monitoring purposes. The implemented model can run at a fixed step size of $Ts = 173.6\,\mu s$ using Euler's method as a solver. The test system is located in the SM_Master subsystem (see Fig. 3), together with several blocks whose functions are specified below:

- *OpCtrl:* It controls the programming of OPAL-RT cards by the bitstream file and selects its hardware synchronisation mode. This block is required because it tells the FPGA card where to expect inputs and where to transmit outputs and perform operations on the signals in between.
- *OpMonitor:* It gives timing information about the model, such as the computation time, the idle time, or the number of overruns. The information provided by the OpMonitor block is used to determine if simulations are running in real-time.
- *OpWriteFile:* It saves the input signals to a file. This block is helpful for post-processing the simulation results. In this work, the OpWriteFile block was used to record the digital and analogue versions of measurements from the PMUs.
- *AnalogOut:* It transmits signals of the model to a physical I/O card in the form of output voltages. It also defines the DataIn port number of the bitstream file, the number of AOut channels and the voltage range of the output voltages. These voltages can be measured on the Slot 2 Module B Section 1 of the Opal-RT 4510 simulator.
- *AnalogIn:* It returns voltage values from Analog Input channels of a physical I/O card. It also defines the DataOut port number of the bitstream file and the number of AIn channels. These voltages can be measured on the Slot 2 Module A Section I of the Opal-RT 4510 simulator.
- *OpOutput:* It is the communication block used when transmitting signals to an I/O interface. This block is needed to send signals via the ANSI C37.118 protocol.
- *OpInput:* It is the communication block used when receiving signals from an I/O interface. This block is needed to receive signals via the ANSI C37.118 protocol.
- *Phasor Measurement Units:* They compute the magnitude, phase, and frequency of the positive sequence component of a three-phase signal, and it is inspired by the IEEE Std C37.118.1-2011 [21]. The test system model includes three

PMUs at buses 1, 2, and 3. This block requires as parameters the nominal frequency f_n of the system (60 Hz) and the sampling rate N_{sr} of the signal (points/cycle). In this work, a sampling rate of 24 points/cycle has been chosen. The most significant step size permitted for simulation is determined by the nominal frequency of the system and the number of points per cycle, which is defined by $T_{s,\max} = 1/f_n/N_{sr} = 694.4\,\mu$s. However, as previously stated, $T_s = 173.6\,\mu$s was chosen as the step size in this study to characterise the test system's performance properly. It is worth noting that T_s needs to be a submultiple of $T_{s,\max}$.

- *Calculation module for the frequency of the centre of inertia* (f_{CoI}): It is the frequency weighted by rotation inertia at different locations across the power system. In this work, the f_{CoI} has been calculated as follows:

$$f_{CoI} = \frac{1}{\sum_{i=1}^{N_g} H_i} \sum_{i=1}^{N_g} f_i H_i \tag{1}$$

where f_i is the frequency measured at the *i-th* generator, and H_i is the rotational inertia coefficient of the *i-th* generator, and N_g is the total number of generators ($N_g = 3$, in this test system).

- *Modules to change the inertia of the generators:* These modules allow the modification of the inertia from the GUI during RT simulations or between them.

2) UFLS Scheme: The UFLS protection scheme is implemented in Typhoon HIL Control Centre 2023.2 with a sample time $T_s = 100.0\,\mu$s. The UF relay is modelled with (81U) Under Frequency blocks from the library "Microgrid → Protection" of the THIL software. Each of these blocks mentioned above models one stage of the relay, so connecting as many blocks in parallel to consider different triggering stages is possible. The stages are configured by defining the nominal frequency of the system, the UF threshold and the UF delay, which is the time since the relay detects the UF event until it trips. The Typhoon Schematic Editor file (.tse) is designed with some other blocks that allow the exchange of signals with the outside—all blocks are taken from the library "core":

- *Analog Input:* The block receives an analogue signal from the analogue input index specified to be used in the model.
- *Probe:* This block adds a signal to the analogue signals list in HIL SCADA so the signal can be monitored or even sent to the analogue output interface.
- *PMU Receive:* It implements a C37.118 master device which receives data from an external PMU.
- *PMU Send:* It implements a C37.118 slave device, which sends data to an external C37.118 master.

3) Monitoring and Control System: The feature of monitoring and controlling a real-time simulation is integrated into RT-LAB by using LabView panels. Monitoring is achieved In the Typhoon HIL Control Centre utilising the HIL SCADA feature. The first step in designing a LabView panel consists of creating the *virtual instrument* (.vi) file. Then, from the control palette, a wide variety of control and indicator items, including numeric, Boolean, string or graphical elements, can be added to the panel

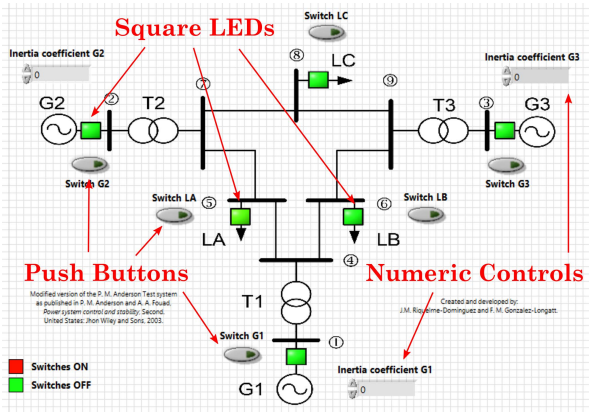

Fig. 4. Configuration of the LabView panel, including squared LEDs, push-buttons and numeric controls.

by simply dragging and dropping. Once the panel is configured, saved, and opened in RT-LAB, the signals and variables from the Simulink model can be assigned to different panel elements. If the RT-LAB model is already compiled, the variables and signals must appear on the corresponding subsystem of the Project Explorer. Then, the assignment is made by dragging the variables and signals from the *Project Explorer* and dropping them on the related elements of the panel. Fig. 4 shows the customised LabView panel designed for this work. It includes the following items:

- *Push Buttons:* allow opening and closing of the three-phase breakers, producing power imbalances and, therefore, exciting the system frequency response.
- *Square LEDs:* indicate the state of the breakers. This information helps identify when a switch is opened or closed during RT simulations (green: open, red: closed).
- *Numerical controls:* modify the coefficient of inertia of the synchronous generators by introducing a new value. This functionality helps compare different scenarios with high or low inertia.

When the Typhoon Schematic Editor file is compiled, HIL SCADA is available in the Typhoon HIL Control Centre. Like LabView panels, HIL SCADA provides a wide variety of widgets that can be used to monitor simulations in real time.

- *Capture/Scope:* The user can capture specified signals when a particular trigger is satisfied. Alternatively, the signal can be continuously monitored through its scope's feature.
- *Digital displays:* They show the numeric value of a specific signal.
- *LEDs:* They indicate the current state of the under-frequency relays.
- *Phasor graphs:* They visually show phasors in polar representation in the complex plane.
- *Trace graphs:* They visually show the evolution of a signal in real time.

4) Digital Communication Protocol: The ANSI C37.118 protocol is available in RT-LAB and Typhoon HIL Control Centre. In RT-LAB, the user must first include *OpInput* and *OpOutput* blocks in the model. Once the model is built, corresponding

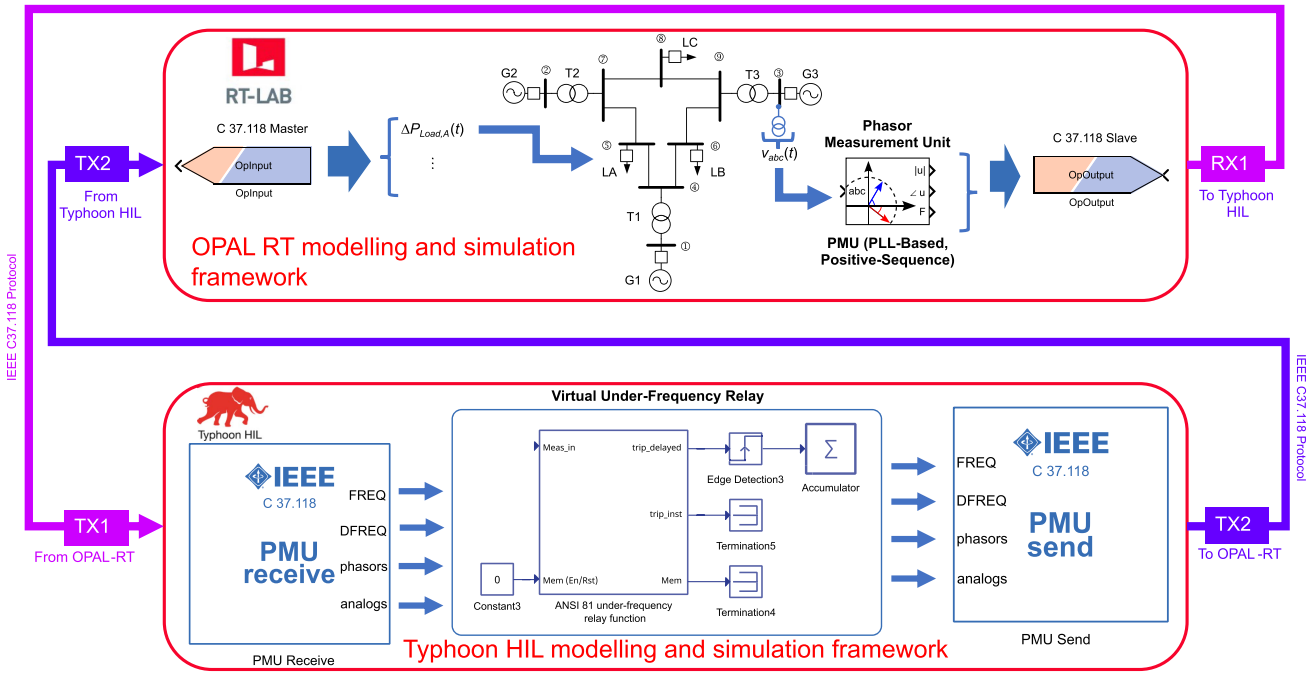

Fig. 5. Overview of the ANSI C37.118 protocol implementation in the proposed testbed.

signals appear in I/O Interfaces section of the *Project Explorer*. Both C37.118 master and slave interfaces should be associated with the computation subsystem of the model and configured appropriately. The configuration consists of assigning a PMU ID, protocol type, TCP/UDP ports, the desired network interface name (NIC name), the IP address of the OPAL simulator, and the configuration of sending/receiving synchrophasors. In the proposed testbed, the PMU ID is set to '1', the TCP protocol is configured with TCP port 4712, 'eth0' is the network interface, and the IP address of the OPAL simulator is 192.168.1.101. Phasors are represented in rectangular format and expressed as 16-bit integers.

In Typhoon HIL Control Centre, *PMU Send*, and *PMU Receive* blocks are configured to match the information provided in RT-LAB. In particular, the *PMU Receive* block needs the IP of the Typhoon HIL simulator (192.168.1.109), the netmask (255.255.255.0), and the destination IP. Fig. 5 depicts the main components of the ANSI C37.118 protocol and its implementation in both real-time simulators.

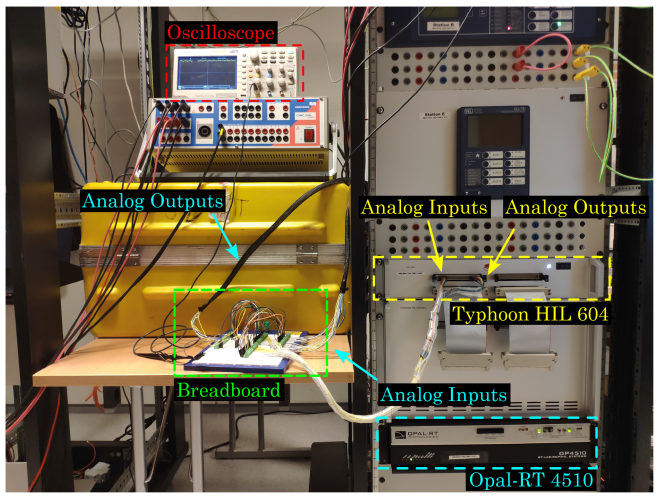

Fig. 6. Experimental setup of the physical layer. The Host PC and the Ethernet connection are not depicted here.

B. Physical Layer

The physical layer related to the closed-loop real-time simulator is implemented by exchanging data between the two real-time simulators using two approaches: wiring analogue I/O and interfacing them with Ethernet connections. The analogue output of the real-time simulator OPAL-RT 4510 consists of signals at the terminal marked positive (1 +, 2 +, 3 +) together with a common ground terminal (GND). These channels send the signals of the generator buses' frequencies (f_{B1}, f_{B2}, f_{B3}) to the real-time simulator Typhoon HIL 604. Typhoon HIL real-time simulator receives these signals in the Analog Input Indexes *AI19* to *AI21*. In the case of digital communication, a single Ethernet cable is enough to connect both real-time simulators, as depicted in Fig. 1. In the latter approach, it is crucial to address the required frequency signals to the corresponding field of the C37.118 master and slave.

Frequency signals feed the UF relay to generate the amount of load to be disconnected ($\Delta P_{Load,A}$), which is then transferred from the Schematic Editor to the HIL SCADA, from where they are sent alternatively: from port *AO33* in the form of an analogue signal or by *PMU Send* block by digital communication to Opal-RT real-time simulator. This way, the co-simulation loop is closed, and the testbed is configured for system frequency studies. Fig. 6 shows the actual experimental setup of the physical layer, with the main components and signals highlighted

(Ethernet connection is not depicted as it is in the rear view of the simulators).

IV. Simulation and Results

This section illustrates and shows the operation of the proposed cyber-physical testbed co-simulation in real time to analyse system frequency response. Two study cases are considered: *Case 1* contemplates the system frequency response considering primary frequency response, and *Case 2* considers a contingency that excites the emergency frequency control: the UFLS protection scheme. In both cases, the sudden loss of a generating unit unleashes the system frequency disturbance. Analogue and digital signals are also collected and compared from the two experiments.

A. Case 1

Initially, the three synchronous generators and the three loads are connected (switches ON, red colour); during these conditions, the test system operates in a steady-state condition, and the frequency is approximately 60 Hz (some minor noise comes from the analogy measurement). Subsequently, the user uses the RT-LAB GUI to open the circuit breaker connecting generator G1 to the grid. The breaker opens at approximately $t = 27.25$ s (in this specific simulation), resulting in an imbalance between generation and demand, and the total system inertia is reduced by the disconnection of generator 1 ($H_1 = 9.55$ s). From that moment on, an under-frequency event occurs, reaching the minimum frequency $f_{\min} = 57.08$ Hz in 3.25 seconds. This situation is maintained until the end of the simulation ($t = 100$ s). Fig. 7 shows the view of the GUI during the RT simulation.

As depicted, the interface represents the breakers' states of the system (with the switch of G1 already in green) and the evolution of the system's frequency during the event. Fig. 8 compares the change of the frequency in its analogue and digital versions. Fig. 9 shows the detail of the system frequency response of Bus 1 in a small-time window around $t = 27.25$ s, the moment that circuit breaker 1 is opened.

As depicted in Figs. 8 and 9, the frequency evolution at Bus 1 is very similar in the cases of analogue and digital communication cases. An analogue signal has an associated noise due to its intrinsic characteristic. The similarity of the signals is confirmed using the relative error, computed as:

$$\sigma = \frac{|y_t - \hat{y}_t|}{y_t} \cdot 100 \tag{2}$$

where y_t and $\hat{y}_t$ are the digital and analogue frequency signals at time t. Fig. 10 shows the evolution of the relative error along the simulation. This error is below 0.20% for the entire simulation.

B. Case 2

It considers a complete UFLS protection scheme for the test system. The UF relay is installed at bus 5 to disconnect a portion of load A. The relay is configured with the settings shown in Table II: it has three stages activated when the frequency drops behind the frequency threshold f_s. When it occurs, the relay

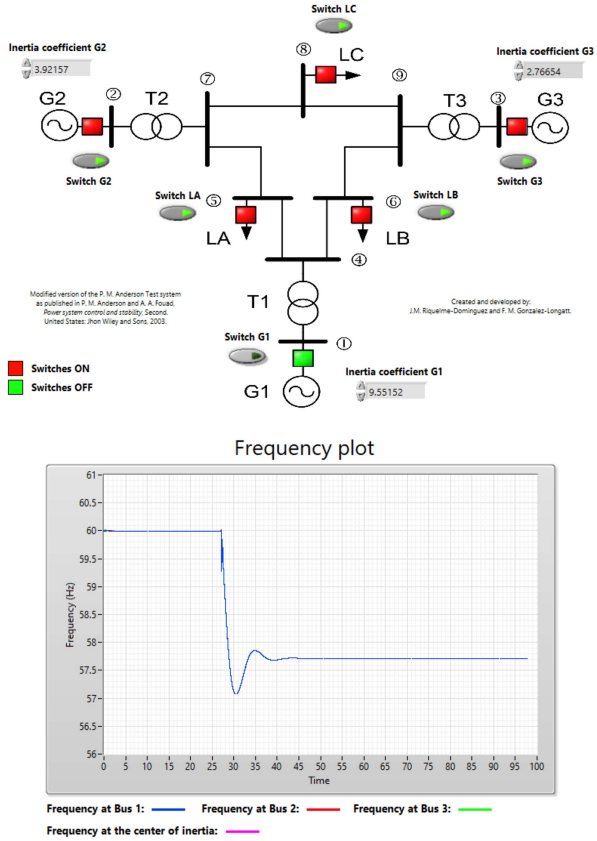

Fig. 7. View of the GUI during the RT simulation: On the top, the real-time state of the test system and, on the bottom, the test system frequency response.

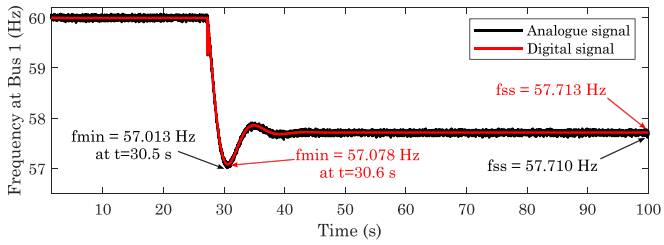

Fig. 8. System frequency response at Bus 1 following the sudden disconnection of G1 at $t = 27.25$ s. Frequency's analogue signal vs digital signal.

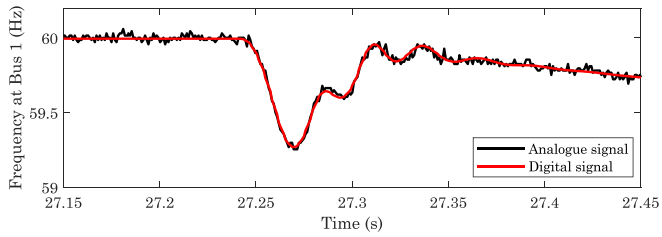

Fig. 9. Detail of the system frequency response of Bus 1 at $t = 27.25$ s. Frequency's analogue signal vs digital signal.

TABLE II
UF Relay Settings

Stage	f_s *(Hz)*	ΔP *(%)*	t_d *(s)*
1	59.0	10	0.10
2	58.0	20	0.10
3	57.0	60	0.10

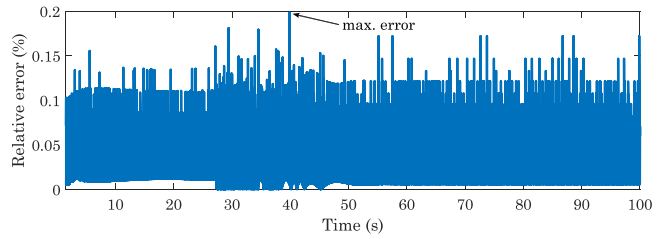

Fig. 10. Comparison of the analogue and digital frequency signals in terms of the relative error.

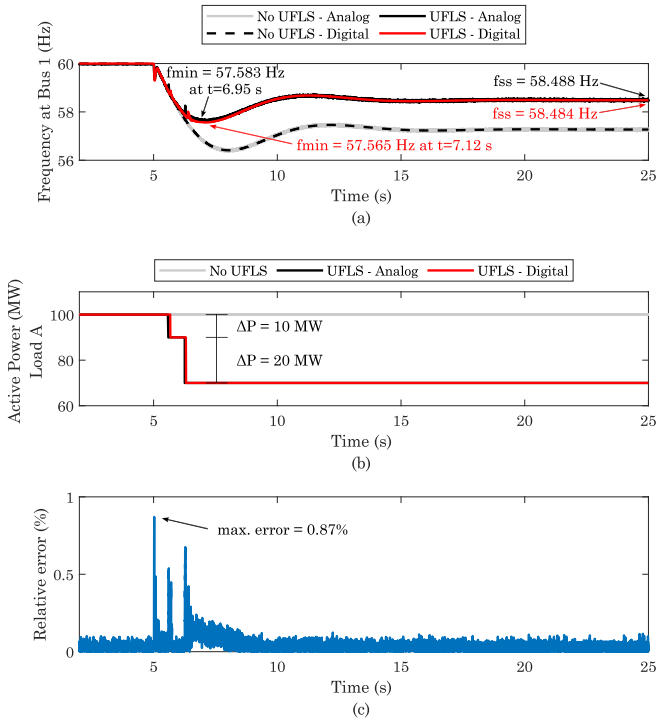

Fig. 11. Results of the UFLS test considering analogue and digital communication: (a) Frequency at Bus 1; (b) Active power of Load A; (c) Relative error along the simulation.

disconnects part of the load $\Delta P_{Load,A}$ after a tripping delay t_d of 0.10 s.

As in *Case 1*, the test system is subjected to a frequency disturbance due to the sudden disconnection of generator unit 1 at $t = 5.0$ s. When synchronous generator G1 is disconnected, the frequency at Bus 1 starts to fall, as depicted in Fig. 11(a), until the frequency crosses the 59 Hz frequency threshold. After 0.10 s, the UF relay is tripped, and 10% of Load A is disconnected (it is assumed that the closest load to Bus 1 is the one that is shredded). As the frequency continues falling, it even crosses the second frequency threshold, so another 20% of Load A is shredded. From this point onwards, the frequency reaches its minimum value and starts to recover until it achieves the steady-state value (f_{ss}).

Fig. 11(a) allows the following analysis: (1) Comparing the cases with and without UFLS protection, it can be seen how the UFLS scheme satisfactorily reduces the frequency drop, not only in terms of the frequency nadir but also in the steady-state frequency value; (2) Considering the case with UFLS protection,

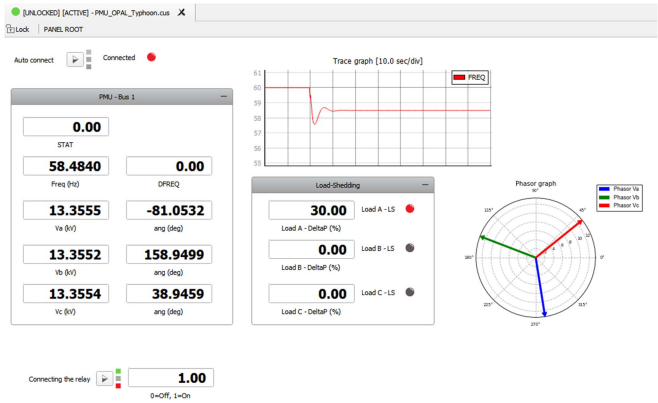

Fig. 12. HIL SCADA panel during the second study case.

a different evolution can be seen for the cases in which analogue and digital signals are used. Contrary to logic, the UF relay trips faster in the case of analogue signals than the one considering digital communication. It can be explained by the noise in measurements, which makes the frequency cross the thresholds before the digital approach. This difference in the trip instant affects the minimum frequency and the moment it is reached in both cases, being in the analogue case $f_{\min} = 57.583$ Hz at $t = 6.95$ s and the digital case $f_{\min} = 57.565$ Hz at $t = 7.12$ s. The steady-state frequency is also slightly different in both cases, in the first one at 58.488 Hz and 58.484 Hz using the ANSI C37.118 protocol. Fig. 11(b) shows the evolution of the absorbed active power by Load A. It can be seen that the load demands 100 MW initially, and then its power is reduced by 10 and 20 MW as the UF-relay stages 1 and 2 are tripped, respectively. Regarding the relative error in Fig. 11(c), it is concluded that the error is below 0.20% except after the tripping of the UF-relay, in which the difference of the analogue and digital frequency signals are more significant, with a maximum relative error of 0.87%.

Fig. 12 shows the HIL SCADA panel during the second study case. It depicts some real-time details of the simulation, such as the three-phase voltage phasors at Bus 1 and the frequency at that system's point. In addition, the status of the UFLS protection scheme is represented.

V. Conclusion

Future carbon-neutral power systems face multiple problems, including developing an advanced simulation platform capable of simulating the real-time dynamic performance of complex systems. This paper presents the results of implementing a cyber-physical testbed co-simulation real-time dedicated to analysing system frequency response considering normal and abnormal (UFLS) situations. The testbed consists of a cyber-physical system with two real-time simulators in a closed loop representing the physical layer: Typhoon HIL 604 and Opal-RT OP4510. The cybernetic layer implements the test system, the UFLS protection scheme, the communication protocol and controls real-time simulations. The frequency response of a modified version of the P.M Anderson 9-bus system utilising phasor measuring units is

shown. Real-time simulation results show the proposed testbed's flexibility and adequacy for system frequency response studies. Analogue and digital communication comparison revealed that the relative error is below 0.2% when considering the system's natural response under a disturbance. However, when implementing a UFLS scheme, analogue noise can unleash UF-relay tripping before it is tripped when using digital communication. Future research will focus on expanding the testbed presented in this paper regarding the test system, protection schemes, and more advanced control and monitoring applications.

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