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Superconducting High-Aspect Ratio Through-Silicon Vias With DC-Sputtered Al for Quantum 3D Integration

J. A. Alfaro-Barrantes, M. Mastrangeli, D. J. Thoen, S. Visser, J. Bueno, J. J. A. Baselmans, and P. M. Sarro

***Abstract*— This paper presents the fabrication and electrical characterization of superconducting high-aspect ratio through-silicon vias DC-sputtered with aluminum. Fully conformal and void-free coating of 300 μm-deep and 50 μm-wide vias with Al, a CMOS-compatible and widely available superconductor, was made possible by tailoring a funneled sidewall profile for the axisymmetric vias. Single-via electric resistance as low as 80.44 mΩ at room temperature and superconductivity below 1.28 K were measured by a cross-bridge Kelvin resistor structure. This work thus demonstrates the fabrication of functional superconducting interposer layers, suitable for high-density 3D integration of silicon-based quantum computing architectures.**

***Index Terms*— Aluminum, cryogenic, interconnects, sputtering, superconducting, through-silicon vias.**

I. Introduction

QUANTUM technology has made remarkable progress in the last two decades [1]. Among quantum technology's four main areas—which also include communication, simulation, and sensing and metrology—quantum computation is gaining particular relevance. In this respect, increasing interest has been recently directed to the possibility of using through-silicon vias (TSVs) at cryogenic temperatures [2]. Such interest was boosted by the demonstration of silicon-based quantum computers, which need to operate at temperatures lower than 1 K [3]. The quest for superconducting vias arises from the realization that the number of physical qubits required for the control and error-correction of logical qubits is nowadays a limitation to compete with the performance of classical computers [1]. Actually, several millions of physical qubits should be integrated on an single chip to achieve substantially higher performance [4]. Current implementations of superconducting and spin qubits in silicon require an area orders of magnitude larger than the size of typical MOS transistors [3]. This severely limits qubit integration density in a single substrate. High qubit integration densities therefore require multilayer technologies, and 3D superconducting interconnects may suit the purpose (Fig. 1): they allow to get rid of interconnecting wires, freeing chip surface to increase qubit density, as well as to vertically stack and interconnect multiple chips [5].

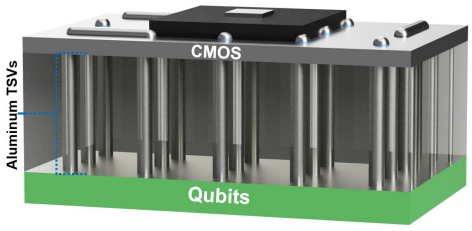

Fig. 1. Sketch of the proposed 3D integration concept for large-scale high-density quantum computing, including a qubit-based layer, TSV-based superconducting interconnects in an interposer layer, and the CMOS circuitry for the control and readout of the qubits.

Copper and doped polysilicon are the most used conductors for (inter)connection and via-filling thanks to their exceptional electrical conductivity and/or thermal stability [6], [7]. However, none of them is superconductive. Moreover, prior work on superconducting interconnections made use of In bumps, TSVs with polymer-filled metallic liner materials or fabrication methods that are not CMOS-compatible or not easily scalable to large substrate areas [8]–[10].

Here we describe a wafer-scale microfabrication process that enables TSVs with high-aspect ratio (HAR, up to 6:1) to be conformally coated with DC-sputtered aluminum, this ensures at once superconducting and CMOS-compatible 3D interconnects. The purpose of the funneled sidewall profile of the TSVs is to facilitate the penetration of the sputtered aluminum into the vias. The sloped surface improves the

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Fig. 2. Sketched cross-sections of a Si substrate illustrating the via fabrication and coating process flow: a) etching of bottom side funnels: isotropic DRIE followed by anisotropic DRIE; b) SiO_2 deposition over bottom side funnels and etch of top side funnels; c) DRIE of straight section of the vias; d) cleaning and thermal growth of insulating SiO_2 layer; e) double-sided sputtering and lithographical patterning of Al/TiN.

coverage and conformality of the Al film on the HAR via sidewalls.

Notably, DC-sputtering is preferable to other Al deposition techniques, such as *e.g.* evaporation, due to the quality of deposited layers, which are homogeneous, free of pores and cracks, and have lower surface roughness [11]. Sputtering additionally affords high throughput and faster depositions, compared with *e.g.* ALD—desirable features for industrialisation and upscaling [12]. TSVs coated with Al by DC-sputtering remained elusive for long.

II. Vias Fabrication

The fabrication process consists of wafer-scale micromachining of TSVs followed by their electrical insulation and conformal coating with TiN-capped Al (Fig. 2).

The fabrication started with thermal growth over a 4", double-side-polished, 300 μm-thick silicon wafer of a 2.6 μm-thick layer of silicon dioxide, used as hard mask for the ensuing steps. Aligned hemispherical cavities ("funnels" in the following, representing the open extremities of the vias) were then etched on both sides of the Si substrate. To achieve this, the SiO_2 layer was first photo-lithographically patterned with circular windows on one side of the wafer (Fig. 2a). Thereafter, isotropic deep reactive ion etching (DRIE) was introduced for 130 s at 25 °C by means of inductively-coupled SF_6 plasma. The plasma was generated near the coils in the upper part of the reactor chamber (Rapier Omega i2l). This step etched wine glass-shaped funnels with pronounced undercuts. The funnels were subsequently plasma-etched anisotropically using an SF_6- and CH_8F_8-based plasma generated in closer proximity of the substrate. This step removed the aforementioned undercuts and broadened the openings of the funnels. The aligned funnels at the other side of the wafer were fabricated in the same way. A protective layer of silicon oxide deposited by plasma-enhanced chemical vapour deposition (PECVD) was then added on the bottom side of the wafer (Fig. 2b). The inner, 50 μm-wide cylindrical section of the vias was drilled by anisotropic Bosch-type etching, landing on the previously deposited SiO_2 layer (Fig. 2c). The wafer was then thoroughly cleaned through exposure to oxygen plasma and immersion in HF and HNO_3 solutions. Repeated oxidation and oxide removal steps were performed for smoothening the sidewalls and for minimizing its undulations. Finally, an additional thermal SiO_2 layer was grown as electric via insulation for the electrical characterization at room temperature (Fig. 2d). Fig. 3a shows a micrograph of vias fabricated through a 300 μm-thick Si wafer.

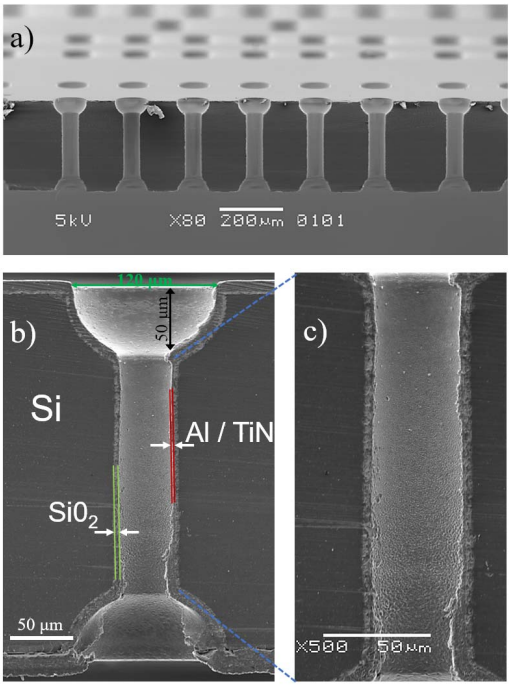

Fig. 3. Scanning electron microscope (SEM) cross-sectional view of TSVs (300 μm-deep, 50 μm-wide) before Al/TiN sputtering (a) and of a single TSV after metal sputtering (b). A close-up of the central part of the via (c) shows fully conformal coating and negligible sidewall undulations.

The metallization of the vias (Fig. 2e), was performed by sequential sputter deposition on each side of the wafer of 4 μm of Al as superconducting layer and of 20 nm of TiN as capping layer. A cryo-pumped Trikon Sigma 204 sputter-coater with a base pressure of 10^{-6} Pa was used. The depositions took 32 minutes per side of the wafer and were performed with a substrate temperature of 25 °C, 50 sccm of argon gas flow and a DC power of 1.3 kW on the 16" Al target. The chamber pressure was set to 244 mPa, obtaining a deposition rate of approximately 2.2 nm/s. The 20 nm of TiN were deposited at 350° C for 58.3 seconds. During the TiN deposition, the pressure was tuned to 4.27 mTorr by using 20 sccm of argon and 70 sccm of nitrogen, and the power was set to 6 kW. The micrographs in Fig. 3b-c show resulting vias after the metallization, and evidence the layers of materials stacked during the fabrication process. The metal layers were finally patterned by lithography (using 12 μm of spin-coated AZ9260 photoresist) and inductively-coupled plasma etching at 25 °C using HBr (30 sccm) and Cl (20 sccm) as reaction gases and 500 W RF power (Fig. 4a-b).

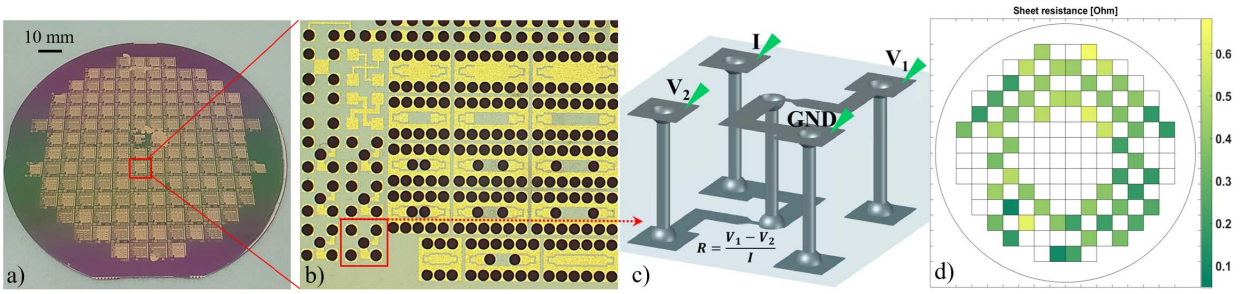

Fig. 4. a) Uniform Al/TiN patterning and interconnect definition over the full 4" Si wafer surface. b) Die singled out from the wafer by saw dicing. c) Sketch of a single cross-bridge Kelvin resistor structure used for the electrical characterization of the TSVs. d) Map showing the fabrication yield and sheet resistance for 4" wafer-level TSVs.

III. Characterisation of Interconnects

Electrical measurements were performed at both room and cryogenic temperature to characterize the fabricated TSVs. Resistance of single TSVs was measured using a 4-terminal cross-bridge Kelvin resistor structure (Fig. 4c) [13], [14]. I-V measurements at room temperature were performed with a parameter analyzer and a multi-probe station. Current was applied at the I terminal of Fig. 4c, and the ensuing voltage drop was measured across terminals V_1 and V_2. Cryogenic DC resistance was measured as a function of temperature using a standard 4-point probe method in a commercial adiabatic demagnetization refrigerator (ADR, Entropy GmbH). The sample was mounted on a copper block weakly coupled to the Gadolinium Gallium Garnet stage of the ADR. A thermometer and a resistive heater allowed to control the stage temperature down to 600 mK, well below the Al superconducting transition. During the measurements the current was kept constant at 30 μA, and the temperature was repeatedly swept upward and downward between 1.1 K and 1.6 K.

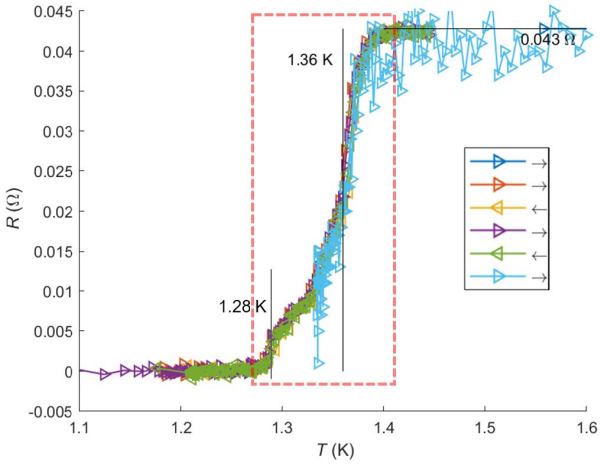

Fig. 5. Superconductive transition measured for a single cross-bridge Kelvin structure with 300 μm-deep Al/TiN-coated TSVs. The overlapping curves represent consecutive upward (→) and downward (←) temperature sweeps, and confirm the repeatibility of the measurements.

IV. Experimental Results

Fig. 3 shows the fully conformal coating of 300 μm-deep HAR TSVs with the Al/TiN stack achieved with the process described above. The funnels are 120 μm-wide and 50 um-deep (Fig. 3b). The minimum via diameter achievable with this technology is around 30um with a height of 300-500 μm.

Fig. 4d shows the resistance measurements at room temperature of the fabricated devices across a 4" wafer. The average electrical resistance value of single vias in the center of the cross-bridge Kelvin resistor structure measured 355.3±138.3 mΩ. The lowest resistance value measured 80.4 mΩ.

The cryogenic resistance measurements evidenced a wide superconducting transition (Fig. 5). This is tentatively attributed to a double superconducting transition in the vias. The transition at 1.36 K originates in the cylindrical section of the via, where the metal film is thinner. The transition at 1.28 K is attributed to the thicker metal film deposited at the junction of the planar and funnel sections of the via (Fig. 3b). This is consistent with prior reports, as the superconducting transition temperature of Al increases for thinner films with higher sheet resistance [15], [16]. Since the ADR at our disposal could not measure I-V curves, we reserve to quantify the TSV's critical current in future work.

V. Conclusion

Superconducting, high-density and high-aspect ratio TSVs were demonstrated for 300 μm-thick Si wafers. Funneled sidewalls enabled conformal DC-sputtering of the TSVs with Al, a CMOS-compatible superconductor. Electrical characterization evidenced single-TSV resistance as low as 80.4 mΩ at 25 °C and superconductivity below 1.28 K. This work prompts the fabrication of superconductive interposer layers for high-density 3D integration for Si-based quantum computing. Determining the critical current of our superconducting TSVs and demonstrating their reliability and integration within quantum 3D architectures will be part of our future work.

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REFERENCES

[1] A. Acín, I. Bloch, H. Buhrman, T. Calarco, C. Eichler, J. Eisert, D. Esteve, N. Gisin, S. J. Glaser, F. Jelezko, S. Kuhr, M. Lewenstein, M. F. Riedel, P. O. Schmidt, R. Thew, A. Wallraff, I. Walmsley, and F. K. Wilhelm, "The quantum technologies roadmap: A European community view," *New J. Phys.*, vol. 20, no. 8, Aug. 2018, Art. no. 080201, doi: 10.1088/1367-2630/aad1ea.

[2] D.-R. W. Yost, M. E. Schwartz, J. Mallek, D. Rosenberg, C. Stull, J. L. Yoder, G. Calusine, M. Cook, R. Das, A. L. Day, E. B. Golden, D. K. Kim, A. Melville, B. M. Niedzielski, W. Woods, A. J. Kerman, and W. D. Oliver, "Solid-state qubits integrated with superconducting through-silicon vias," 2019, *arXiv:1912.10942*. [Online]. Available: http://arxiv.org/abs/1912.10942

[3] J. M. Gambetta, J. M. Chow, and M. Steffen, "Building logical qubits in a superconducting quantum computing system," *npj Quantum Inf.*, vol. 3, no. 1, Dec. 2017, doi: 10.1038/s41534-016-0004-0.

[4] J. S. Clarke, "Quantum computing and the importance of interconnects," in *Proc. IEEE Int. Interconnect Technol. Conf. (IITC)*, Jun. 2018, p. 1, doi: 10.1109/IITC.2018.8430479.

[5] R. N. Das, W. D. Oliver, J. L. Yoder, D. Rosenberg, D. K. Kim, D. Yost, J. Mallek, D. Hover, V. Bolkhovsky, and A. J. Kerman, "Cryogenic qubit integration for quantum computing," in *Proc. IEEE 68th Electron. Compon. Technol. Conf. (ECTC)*, May 2018, pp. 504–514, doi: 10.1109/ECTC.2018.00080.

[6] C. Song, Z. Wang, Q. Chen, J. Cai, and L. Liu, "High aspect ratio copper through-silicon-vias for 3D integration," *Microelectron. Eng.*, vol. 85, no. 10, pp. 1952–1956, Oct. 2008, doi: 10.1016/j.mee.2008.05.017.

[7] E. Clarke, *Circuit Analysis of AC Power Systems*, vol. 1. New York, NY, USA: Wiley, 1950, p. 81.

[8] M. Vahidpour, W. O'Brien, J. Tyler Whyland, J. Angeles, J. Marshall, D. Scarabelli, G. Crossman, K. Yadav, Y. Mohan, C. Bui, V. Rawat, R. Renzas, N. Vodrahalli, A. Bestwick, and C. Rigetti, "Superconducting through-silicon vias for quantum integrated circuits," 2017, *arXiv:1708.02226*. [Online]. Available: http://arxiv.org/abs/1708.02226

[9] B. Foxen, J. Y. Mutus, E. Lucero, R. Graff, A. Megrant, Y. Chen, C. Quintana, B. Burkett, J. Kelly, E. Jeffrey, Y. Yang, A. Yu, K. Arya, R. Barends, Z. Chen, B. Chiaro, A. Dunsworth, A. Fowler, C. Gidney, M. Giustina, T. Huang, P. Klimov, M. Neeley, C. Neill, P. Roushan, D. Sank, A. Vainsencher, J. Wenner, T. C. White, and J. M. Martinis, "Qubit compatible superconducting interconnects," *Quantum Sci. Technol.*, vol. 3, no. 1, Jan. 2018, Art. no. 014005, doi: 10.1088/2058-9565/aa94fc.

[10] K. Grigoras, S. Simbierowicz, L. Gronberg, J. Govenius, V. Vesterinen, M. Prunnila, and J. Hassel, "Superconducting TiN through-silicon-vias for quantum technology," in *Proc. IEEE 21st Electron. Packag. Technol. Conf. (EPTC)*, Dec. 2019, pp. 81–82, doi: 10.1109/EPTC47984.2019.9026646.

[11] H. Garbacz, P. Wieciński, B. Adamczyk-Cieślak, J. Mizera, and K. J. Kurzydłowski, "Studies of aluminium coatings deposited by vacuum evaporation and magnetron sputtering," *J. Microsc.*, vol. 237, no. 3, pp. 475–480, Mar. 2010, doi: 10.1111/j.1365-2818.2009.03297.x.

[12] A. Baptista, F. Silva, J. Porteiro, J. Míguez, and G. Pinto, "Sputtering physical vapour deposition (PVD) coatings: A critical review on process improvement and market trend demands," *Coatings*, vol. 8, no. 11, p. 402, Nov. 2018, doi: 10.3390/coatings8110402.

[13] F. Santagata, C. Farriciello, G. Fiorentino, H. W. van Zeijl, C. Silvestri, G. Q. Zhang, and P. M. Sarro, "Fully back-end TSV process by cu electro-less plating for 3D smart sensor systems," *J. Micromech. Microeng.*, vol. 23, no. 5, May 2013, Art. no. 055014, doi: 10.1088/0960-1317/23/5/055014.

[14] N. Stavitski, J. H. Klootwijk, H. W. van Zeijl, A. Y. Kovalgin, and R. A. M. Wolters, "Cross-bridge kelvin resistor (CBKR) structures for measurement of low contact resistances," in *Proc. 10th Annu. Workshop Semiconductor Adv. Future Electron. and Sensors (SAFE)*, vol. 22, Nov. 2007, pp. 551–554.

[15] Y. Ivry, C.-S. Kim, A. E. Dane, D. De Fazio, A. N. McCaughan, K. A. Sunter, Q. Zhao, and K. K. Berggren, "Universal scaling of the critical temperature for thin films near the superconducting-to-insulating transition," *Phys. Rev. B, Condens. Matter*, vol. 90, no. 21, pp. 1–8, Dec. 2014, doi: 10.1103/PhysRevB.90.214515.

[16] R. W. Cohen and B. Abeles, "Superconductivity in granular aluminum films," *Phys. Rev.*, vol. 168, no. 2, pp. 444–450, Apr. 1968, doi: 10.1103/PhysRev.168.444.