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PAVEL PURGAT

BUILDING BLOCKS FOR MESHED LVDC SYSTEMS

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DISSERTATION

for the purpose of obtaining the degree of doctor
at Delft University of Technology,
by the authority of the Rector Magnificus, Prof. dr. ir. T.H.J.J. van der Hagen,
chair of the Board for Doctorates,
to be defended publicly on *Friday* 20, November 2020 at 10:00 o'clock.

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To Mum & Dad.

Pravda a láska musí zvítězit nad lží a nenávistí!
— Václav Havel

SUMMARY

Low voltage direct current (LVDC) became a viable option for electric energy distribution in the early years of the twenty-first century. The upturn in the use of LVDC is fuelled by advances in power electronics and the growing use of renewable energy sources (RES) and electric storage. This work focuses on the power electronic devices for the LVDC systems as the primary instruments that implement the system functionalities.
The primary function of any power distribution system is to efficiently and safely deliver power from the sources to the loads. As is also discussed in this thesis, LVDC is exceptionally well suited to fulfill this goal in systems with bidirectional power flow that consist of multiple sources and multiple loads. Secondly, the system must be able to identify, isolate, and clear system failures that inevitably occur during the operation. Therefore this thesis focuses on the role of power electronics in two main application areas - power flow control and short-circuit protection.

POWER FLOW CONTROL

In this thesis, the attention is given to the meshed system topologies. In the meshed system, multiple paths for the current to flow exist. The current always follows the path of the least resistance. If the current is unregulated, the most efficient operation with regards to the joule losses is achieved. However, such unregulated operation can lead to local overloads. The local overloads are manifested for example by reaching the thermal limits of the connecting cables. Therefore, an efficient solution that can control the currents is studied in this thesis.
The proposed solution is based on the differential power processing concept. The concept of differential power processing originated in early sixties for battery cell balancing. It was also applied to ac systems for which the unified power flow controller (UPFC) was developed. In this thesis, a dc counterpart to the UPFC is proposed and studied. It is shown that the proposed converter can achieve above 99 % efficiency and significant material savings in different applications.

EFFICIENT CONVERTER CONTROL

For applications with the larger power rating, bipolar LVDC systems are desirable. The concept of a partially rated power flow control converter is generalized in this thesis for the use in bipolar systems. In the core of the proposed power flow control converter for the bipolar system is a triple active bridge converter (TAB). Using TAB topology, several semiconductor and passive components can be saved when the application has multiple input and output ports. However, the efficient operation of this topology is not guaranteed for all operating points. Therefore, in this thesis, the zero voltage switching areas of TAB are derived and a simple modulation improvement that minimizes the losses related to the TAB circulating power and increases the ZVS area.
TAB converters have typically two controllable ports. However, the control variables are coupled. The coupling of the control variables makes independent control of the two outputs difficult and even impossible. In this thesis, a decoupling controller that uses transformer currents is derived and experimentally verified.

SHORT-CIRCUIT PROTECTION

The ability of the system to protect people and equipment during abnormal operating conditions is of the utmost importance to its success in the market. The physical nature of dc systems makes the interruption and clearing of short-circuit more challenging than a comparable ac system. The typical LVDC system has small system inductances, and due to the use of voltage source converters, the system capacitances are relatively high. Therefore, the transients currents during the short circuits reach hundreds of amperes within microseconds. The semiconductor components are sensitive to overcurrents and can tolerate less than ten times the nominal current only for microseconds. Therefore, the identification of the faults and the following interruption are bounded in the microseconds range. However, fast interruption of the fault current creates overvoltage on the interrupting devices.
The design of the semiconductor-based circuit breaker must take the above constraints into account. The detection of the fault needs to recognize the fault early; therefore, in this thesis, both the rate-of-change-of-the-current and the current amplitude are investigated. The circuit breaker must be able to interrupt the current flow in a short period and withstand the resulting overvoltage. Therefore special attention in this work is placed on analyzing

the relationship between the overvoltage suppression circuits and different short-circuit detection methods. The trade-offs between the peak short-circuit currents, peak overvoltages, and both system and circuit breaker parameters are also analyzed and experimentally verified.

LVDC APPLICATIONS

LVDC systems are a technology with a low level of market readiness. A short survey of potential applications is provided in the last chapter of this thesis. Three promising applications were chosen from the market survey - street lighting, dc charging, and meshed city grids. The chosen application are used as case studies to demonstrate the benefits of the solutions proposed in this thesis- power flow control converter and solid-state circuit breakers. For street lighting system the possibility to extend the line length by fifty percent is demonstrated. For dc charging a converter that only needs to be rated for one third of the charging power is demonstrated. And lastly, over twenty percent increase in power capacity of a meshed city grid is demonstrated. All these benefits are achieved using the solutions proposed in this thesis.

SAMENVATTING

Laagspanningsgelijkstroom ("Low Voltage Direct Current" of LVDC) werd in het begin van de eenentwintigste eeuw een realistische optie voor de distributie van elektrische energie. De toename van het gebruik van LVDC wordt gevoed door de vooruitgang in vermogenselektronica en het toenemend gebruik van duurzame energiebronnen en elektrische opslag. Dit proefschrift concentreert zich op de vermogenselektronica voor de LVDC-systemen die als primaire instrumenten de beoogde systeemfunctionaliteiten implementeren.
De primaire functie van elk stroomdistributiesysteem is om efficiënt en veilig stroom te transporteren van de bronnen naar de belastingen. Zoals ook in dit proefschrift wordt besproken, is LVDC bijzonder geschikt om dit doel te bereiken in systemen met bidrectionele stromen, en meerdere bronnen en belastingen. Ten tweede moet het systeem in staat zijn om kortsluitingen, die onvermijdelijk optreden tijdens de operatie, te identificeren, te isoleren en te verhelpen. Daarom concentreert dit proefschrift zich op de rol van vermogenselektronica in twee belangrijke toepassingsgebieden: vermogensstroomregeling en kortsluitbeveiliging.

VERMOGENSSTROOMREGELING

In dit proefschrift wordt aandacht besteed aan de gemaasde systeemtopologieën. In vermaasde systemen bestaan er meerdere paden voor het vermogen om te stromen. De stroom volgt altijd het pad van de minste weerstand. Als de stroom niet gereguleerd is, wordt de meest efficiënte werking met betrekking tot de joule-verliezen bereikt. Een dergelijke ongereguleerde werking kan echter leiden tot lokale overbelasting. Een mogelijk resultaat van lokale overbelastingen is bijvoorbeeld het overschreiden van de thermische limieten van de verbindingskabels. Daarom wordt in dit proefschrift een efficiënte oplossing bestudeerd die de stromen kan beheersen.
De voorgestelde oplossing is gebaseerd op het differentiële vermogensverwerkingsconcept. Het concept van differentiële vermogensverwerking ontstond begin jaren zestig voor het balanceren van batterijcellen. Het werd ook toegepast op wisselstroomsystemen waarvoor de Unified Power Flow Controller (UPFC) werd ontwikkeld. In dit proefschrift

wordt een gelijkstroom-tegenhanger van de UPFC voorgesteld en bestudeerd. Het is aangetoond dat de voorgestelde converter een efficiëntie van meer dan 99 % en aanzienlijke materiaalbesparingen in verschillende toepassingen kan behalen.

EFFICIENTE BEHEERSING VAN VERMOGENSELEKTRONICA

Voor hoogvermogens toepassingen zijn bipolaire LVDC-systemen wenselijk. Het concept van een Partially Rated Power Flow Controller wordt in dit proefschrift onderzocht voor gebruik in bipolaire systemen. In de kern van de voorgestelde vermogenselektronica voor het bipolaire systeem bevindt zich een Triple Active Bridge (TAB). Met behulp van TAB-topologie kunnen verschillende halfgeleider- en passieve componenten worden gebruikt wanneer de applicatie meerdere invoer- en uitvoerpoorten heeft. De efficiënte werking van deze topologie is echter niet voor alle bedieningspunten gegarandeerd. Daarom zijn in dit proefschrift de gebieden voor Zero Voltage Switching (ZVS) van de TAB afgeleid, en een eenvoudige modulatieverbetering is gepresenteerd die de verliezen gerelateerd aan het TAB-circulerend vermogen minimaliseert en het ZVS-gebied vergroot. TAB-converters hebben doorgaans twee bestuurbare poorten. De controlevariabelen zijn echter gekoppeld. De koppeling van de regelvariabelen maakt onafhankelijke aansturing van de twee uitgangen moeilijk of zelfs onmogelijk. In dit proefschrift wordt een ontkoppelingsregelaar die gebruikmaakt van transformatorstromen afgeleid en experimenteel geverifieerd.

KORTSLUITINGSBEVEILIGING

Het vermogen van het systeem om mensen en apparatuur te beschermen tijdens abnormale omstandigheden is van het grootste belang voor het succes van LVDC op de markt. De fysieke aard van gelijkstroomsystemen maakt het onderbreken en verhelpen van kortsluitingen uitdagender dan een vergelijkbare wisselstroomsystemen. Het typische LVDC-systeem heeft kleine systeeminductanties en door het gebruik van spanningsbronomvormers zijn de systeemcondesatoren relatief hoog. Daarom bereiken de transiënte stromen tijdens kortsluitingen honderden ampères binnen microseconden. De halfgeleidercomponenten zijn gevoelig voor hoge stromen en kunnen slechts gedurende microseconden minder dan tien keer de nominale stroom verdragen. Daarom worden de identificatie en onderberkingen van de kortsluitingen plaatsvinden binnen microseconden. Een snelle onderbreking

van de foutstroom veroorzaakt echter overspanning over de apparaten die ze onderbreken.
Bij het ontwerp van een op halfgeleider gebaseerde stroomonderbreker moet rekening worden gehouden met de bovenstaande beperkingen. De detectie van de fout moet vroegtijdig plaatsvinden; daarom worden in dit proefschrift zowel de snelheid van de verandering van de stroom alsmede de stroomamplitude onderzocht. De vermogenschakelaar moet de stroom in korte tijd kunnen onderbreken en de resulterende overspanning kunnen weerstaan. Daarom wordt in dit werk speciale aandacht besteed aan het analyseren van de relatie tussen de overspanningsonderdrukkingscircuits en verschillende kortsluitingsdetectiemethoden. De afwegingen tussen de piekkortsluitstromen, piekoverspanningen en zowel systeem- als stroomonderbreker parameters worden ook geanalyseerd en experimenteel geverifieerd.

LVDC-TOEPASSINGEN

LVDC-systemen zijn een technologie met een lage marktbereidheid. Een kort overzicht van mogelijke toepassingen wordt gegeven in het laatste hoofdstuk van dit proefschrift. Uit het marktonderzoek zijn drie veelbelovende toepassingen gekozen: straatverlichting, gelijkstroomladen en vermaasde stadsnetwerken. De gekozen toepassing wordt gebruikt als casestudies om de voordelen van de oplossingen die in dit proefschrift worden voorgesteld aan te tonen: de vermogensstroomregelaar en haflgeleider gebaseerde stroomonderbrekers. Voor straatverlichtingssystemen wordt de mogelijkheid gedemonstreerd om de lijnlengte met vijftig procent te verlengen. Voor het opladen met gelijkstroom wordt een omvormer gedemonstreerd die slechts een derde van het laadvermogen hoeft te verwerken. En tot slot wordt een toename van meer dan twintig procent in stroomcapaciteit van een vermaasd stadsnet aangetoond. Al deze voordelen worden bereikt met behulp van de oplossingen die in dit proefschrift worden voorgesteld.

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NOMENCLATURE

N	Nodes in the dc distribution grid.
l	Distribution lines in dc distribution grid.
o	Phase conductors in dc distribution grid.
m	Loads in dc distribution grid.
$\boldsymbol{\Gamma}$	Incidence matrix describing the connectivity of dc distribution grids.
$\boldsymbol{C}_N$	Diagonal capacitance matrix of dc distribution grid.
$\boldsymbol{G}_N$	Conductance matrix of dc distribution grid.
$\boldsymbol{V}_N$	Matrix of the node voltages in dc distribution grid.
$\boldsymbol{I}_N$	Matrix of the currents flowing into each node in dc distribution grid.
$\boldsymbol{I}_{\text{LINE}}$	Matrix of the line currents in dc distribution grid.
$\boldsymbol{L}_l$	Diagonal inductance matrix of dc distribution grid.
$\boldsymbol{R}_l$	Diagonal resistance matrix of dc distribution grid.
$V_1, V_2, \ldots, V_i$	Node Voltages in the dc distribution grid.
$I_{\text{LINE},1}, \ldots, I_{\text{LINE},i}$	Line currents flowing on the positive rail in the dc distribution grid.
T_s	Switching period of the power flow control converter (PFCC).
f_s	Switching frequency.
f_c	Corner (cutoff) frequency.
t	Time.
Δt_i	Time interval.
τ	Time variable during switching period.

s	Complex number frequency parameter.
$\langle x \rangle_k$	The $k-th$ coefficient of the Fourier series.
ω_s	Angular frequency.
$s_1(\tau)$	Switching function of the high voltage side full bridge of the PFCC.
$s_2(\tau)$	Switching function of the low voltage side full bridge of the PFCC.
$s_3(\tau)$	Switching function of the unfolder bridge of the PFCC.
φ	Phase-shift of the dual active bridge (DAB) converter inside PFCC
d_1	Averaged control signal of the dual active bridge inside PFCC.
d_2''	Duty cycle of the unfolding bridge inside PFCC.
d_2'	Averaged duty cycle of the unfolding bridge inside PFCC.
d_2	Averaged duty cycle of the unfolding bridge inside PFCC rewritten as $d_2 = 2d_2' - 1$.
v_{IN}	Input voltage of the PFCC.
v_{DC}	Middle dc-link voltage of PFCC.
v_{SERIES}	Output voltage of the PFCC.
i_{IN}	Input current of PFCC.
i_σ	Leakage inductor current of the dual active bridge inside PFCC.
$i_{\sigma,1R}$	Real part of the 1st coefficient of the Fourier series representing DAB leakage current.
$i_{\sigma,1I}$	Imaginary part of the 1st coefficient of the Fourier series representing DAB leakage current.
i_f	Inductor current of the unfolding bridge inside PFCC.
n	Transformer ratio of the DAB inside PFCC.

C_{IN}	Input capacitor of the dual active bridge inside PFCC.
L_{IN}	Input inductor of the dual active bridge inside PFCC.
R_{IN}	Parasitic input resistor of the dual active bridge inside PFCC.
L_σ	Leakege inductor of the dual active bridge inside PFCC.
R_σ	Parasitic leakege resistor of the dual active bridge inside PFCC.
C_{DC}	Output capacitor of the dual active bridge inside PFCC.
$L_{f,1}, L_{f,2}$	Filter inductors of the unfolding bridge inside PFCC.
L_f	Sum of filter inductors $L_{f,1}$ and $L_{f,2}$.
C_{SERIES}	Output capacitor of the unfolding bridge inside PFCC.
R_f	Parasitic resistor of the unfolding bridge inside PFCC.
R_{PFC}	Parasitic resistor in the main current path of the PFCC.
L_{PFC}	Parasitic inductance in the main current path of the PFCC.
$\boldsymbol{A}, \boldsymbol{B}, \boldsymbol{C}, \boldsymbol{D}, \boldsymbol{N}$	Matrices of the state-space representation.
$\bar{x}$	Vector of state-space variables describing the PFCC in state-space representation.
$\bar{u}$	Vector of the PFCC inputs in the state-space representation.
$\bar{w}$	Vector of the disturbances in the state-space representation.
$\boldsymbol{E}$	Identity matrix.
$\boldsymbol{G}$	Matrix of transfer functions of small signal model of PFCC.
$G_{1,1} - G_{2,4}$	Transfer functions of small signal model of PFCC.
V^*_{DC}	Reference value for PFCC dc link voltage.
V^*_{SERIES}	Reference value for PFCC series voltage.
ζ	Relative damping.
$K_{\text{DC},1}$	Proportional gain of the dc link voltage PI controller.

$K_{\mathrm{DC},2}$	Integral gain of the dc link voltage PI controller.
$K_{\mathrm{UNF},1}$	Proportional gain of the series voltage PI controller.
$K_{\mathrm{UNF},2}$	Integral gain of the series voltage PI controller.
$Z_{\mathrm{LINE},\mathrm{I}}$	Impedance of distribution line i modeled with lumped element π model.
$R_{\mathrm{LINE},\mathrm{I}}$	Resistance of distribution line i.
L_{LINE}	Inductance of distribution lines.
C_{LINE}	Capacitance of distribution lines.
C_{NODE}	Node capacitance on the dc grid side.
$P_{\mathrm{LINE},i}$	Power transferred in the line i.
$P_{\mathrm{NODE},i}$	Power supplied or sunk in the node i.
$V_{\mathrm{DAB,HV}}$	Mid-point voltage of the high voltage bridge in the DAB.
$V_{\mathrm{DAB,LV}}$	Mid-point voltage of the low voltage bridge in the DAB.
V_{UNF}	Mid-point voltage of the unfolder bridge.

1

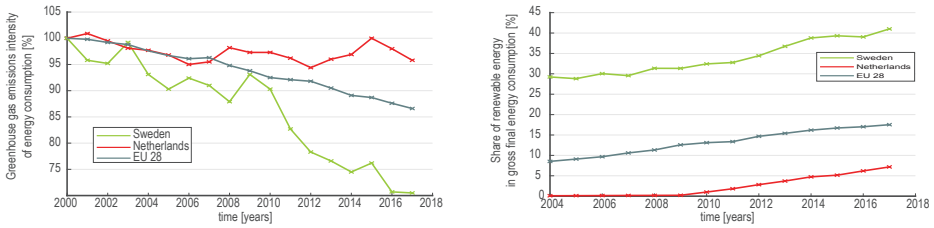
INTRODUCTION

1.1 BACKGROUND & MOTIVATION

Anthropogenic climate change triggered abrupt and irreversible changes in ecosystems across Earth. A major force driving the climate change is the rise of greenhouse gasses (GHG) in the atmosphere. The production and use of energy is by far the most significant contributor to the GHG emissions. Globally, two-thirds of GHG emissions originate in the burning of fossil fuels for energy [2]. The reduction of GHG emissions from energy can be achieved in two ways: cleaner energy sources (e.g. replacing fossil fuels with non-combustible renewable sources (RES)) and by reducing the overall energy consumption via efficiency gains. However, the later, historically speaking, always lead to an increase of energy consumption, as the efficiency gains, make the energy use cheaper.

The debate about how to meet our present energy needs and not compromise the prospects of the future generations for a decent life in the process brought forward a push for decarbonization of the energy mix and further electrification of the world economy. Figure 1.1a shows greenhouse gas emissions intensity of energy consumption in European Union (EU) and two chosen member countries. The indicator is calculated as the ratio between energy-related greenhouse gas emissions and gross inland consumption of energy. It expresses how many tonnes CO2 equivalents of energy-related greenhouse gases are being emitted in a specific economy per unit of energy that is being consumed. The share of RES in the energy mix is shown in Fig. 1.1b. The data shows that EU is slowly reducing the CO2 intensity of its economy as well as increasing the share of RES in its energy mix. It is however also clear, that some countries such as the Netherlands struggle to meet their commitments. Further motivation for member countries to accelerate the decarbonization is introduced with *European Green Deal* which sets out a framework for potential carbon tariffs, for countries that do not curtail their GHG emissions at the required rate [3].

As a result of growing urbanisation, the energy consumption concentration increases [4]. Thus the energy transition especially in countries with high population density becomes a spatial question as well. Moreover, the nature of electricity consumption is also evolving [5]. In effect that means that most of the new loads in the modern urban areas are of capacitive and non-linear



(a) (b)

FIGURE 1.1: European union energy indicators. Source: [1].

nature [5, 6]. One example for all of the new type of electrical devices in the urbanised areas is the growing number of the electric vehicles [7].

Higher penetration of RES into the electric energy distribution system brings forth new challenges. It exposes the existing infrastructure not just to the intermittent and diffuse nature of these sources but also to various power electronic-based components [8]. The existing infrastructure was however designed for well-planned, centralised energy production and mostly resistive and inductive components. Thus the traditional top-down approach to the design and operation of the distribution systems is under scrutiny [6, 9]. These developments incentivised re-evaluation of the low voltage direct current (LVDC) role in the electric energy distribution [10, 11].

1.2 LVDC VISION & STATE-OF-THE-ART

1.2.1 *Why DC?*

Several studies show potential energy savings when LVDC is adopted instead of low voltage alternating current (LVAC) [12–15]. Depending on the type of the study, the projected efficiency savings vary between two percent to eighteen percent for modelling based studies [12]. However, for the experimentally based studies the efficiency gains vary only between two percent to eight percent [14, 15]. The reported efficiency gains are heavily depended on the presence of energy storage, if energy storage is not present the efficiency gains are reduced [12]. Further, a strong dependency is on the match of RES with the load profile. In case of utility building, the most prominent RES is photovoltaics (PV). When RES production and load consumption coincide in time, the LVDC system does not utilize the active front end converter (AFE) connected to the AC grid. Bypassing AFE increases the energy efficiency [16]. Further, strong dependence arises from the assumed component efficiencies [12, 17]. It has to be noted, that the component efficiency increase with the increase

of the component power rating. While, the converters with power rating less than 1 kW achieve average efficiencies around 90 %, for converters with power rating between 1 to 5 kW the average efficiencies are around 97.5 % [16]. The converter efficiencies are also dependent on the operating conditions and unbalanced load conditions reduce the efficiency of components [17]. Moreover, the system efficiency gains can be greatly influenced by the voltage level chosen and the system configuration. The systems with higher voltage tend to have higher operating efficiencies [18]. The systems that do not have typical top down power consumption structure, but have bidirectional power flow have higher efficiency when LVDC is used compared to LVAC [12, 16].

The core advantages of LVDC compared to LVAC are the ease of integration of RES and energy storage. The underlying reasons are the dc nature of both energy storage and most of the RES. And, the absence of phase and frequency synchronization, or in other terms no need for AFE with power factor correction. The lack of AFE, leads to increase in operating efficiency, flexibility, resiliency and reduction of carbon footprint. Further benefits include a possibility of reduced upfront cost of the LVDC system. However, at the early stage of LVDC adaptation the upfront cost is increased due to lack of economies of scale and specific protection requirements for LVDC [16, 19]. A significant advantage that is often discussed in literature is the ability of the LVDC system to work at the grid edge. The LVDC systems are decopuled from the ac grid, thus these system have the ability to mitigate the effects of main grid voltage sags or frequency disturbances. High resiliency is a key benefit in applications that require extremely high availability, such as data centers or some critical production lines.

1.2.2 *Microgrids*

Microgrids are electricity distribution systems containing loads and distributed energy resources, (such as distributed generators, storage devices, or controllable loads) that can be operated in a controlled, coordinated way either while connected to the main power network or while islanded[1] [20, 21]. In other words, the term microgrid can be used to describe a conceptual solution for the integration of renewable energy sources, energy storage in such way that it minimizes the architectural changes and operational disruptions to the existing power grid [22]. The concept of the microgrid has several other distinguishing features than those encompassed in the above definition from CIGRE. Microgrids are often interfaced to the higher-level system through bidirectional

[1] CIGRE C6.22 Working Group, Microgrid Evolution Roadmap.

electronic power converter(s), all energy sources and storage are connected through electronic power converters and most loads are connected through electronic power converters. Furthermore, microgrids have extensive communication and control capabilities and protection and reconfiguration functions are provided without the use of thermal-magnetic switchgears [19, 23].

There are different approaches toward topological organization of LVDC microgrids. Originating from the centralized solid-state transformer enabled microgrids [24], LVDC systems with point-of-load-like structure [10] or highly modular decentralized LVDC multi-terminal systems [19, 25]. All of these structures can employ either a monopolar dc bus, a unipolar dc bus (i.e. single voltage level), bipolar dc bus (i.e. two voltage levels) or multiple regulated dc buses [8].

Grater flexibility and higher availability can be attained when reconfigurable topologies are used. Especially in highly utilized networks in densely populated areas with electric vehicles, distributed sources and energy storage devices, it would be preferable to use meshed connections. Meshing of the grid allows usage of neighbouring connections and substations in case of congestions, faults or maintenance work. In a meshed network, each dc distribution unit is connected to at least two dc buses. These two buses form a redundant configuration, that can ensure continuous operation of the DC distribution unit in case of a fault on one of the dc buses.

1.3 PROBLEM DEFINITION

1.3.1 *System Integration*

Future LVDC meshed microgrids that are consisting of semi-independent prosumers, utility buildings and autonomous energy storage with the "smart" functionalities are true systems-of-systems. These are systems that pool their capabilities together to create new systems that offer superb performance and functionality than the mere sum of the constituents units. In the complex architectures of the system-of-systems, the constituents systems must be able to usefully operate independently [26]. Moreover, the constituents are acquired and integrated independently, so they not only *can* but *do* operate independently [26].

From the definition, the constituent systems are often developed independently, the system-of-system behaviour emerges only through the interaction of the components. Therefore, the design of the interfaces is crucial. The systems can and normally have power and communication interfaces [26]. It is important to note, that in the envisioned meshed LVDC microgrids, the components

(even those used by the end users) actively react to the system parameters and status. Therefore, both the communications and power interfaces are crucial.

In order to work with well-defined interfaces, the concept of building blocks is introduced. The constituent systems are built from building blocks (or their collections). A building block is a well-defined functionality block that is well recognizable by the domain experts. It evolves with the technology and standards, and it can be assembled from other building blocks, it may be a subassembly of other building blocks and is reusable and replaceable. A right choice of a building block can lead to improvements in legacy system integration, interoperability, and flexibility in the creation of new systems and applications [27].

Following definitions are derived from TOGAF standard developed by the Open Group [28]. Two types of building blocks can be distinguished- system building blocks (SBB) and function building blocks (FBB). SBBs are the highest level of abstraction and define what function will be implemented, specify the power and communication interface as well as the market requirements. An example of SBB in LVDC microgrid can be a power flow controlling block, a voltage level interfacing block or a protection block.The electric devices used by the end customers also fall into the category of system building blocks. As the what function is implemented as well as the interfaces are clearly defined.

The function building blocks, on the other hand, define how the functions are implemented. That means which technologies and components will implement the functionality of SBB. An example of FBB can be a dual-active bridge converter, a full-bridge inverter or some solid-state circuit breaker topology. It should be noted that per the general characteristic of the building block an integrated half-bridge module is an FBB. As described above, it can be assembled from other building blocks (e.g. gate driver building block), it may be a subassembly of other building blocks (e.g. in a full-bridge inverter) and is reusable and replaceable.

In this thesis, the constituents parts of microgrids and nanogrids will be treated as building blocks. The challenges solved through the thesis will be either on the level of FBB, where the goal is to ensure that the FBB can perform its defined function efficiently. Alternatively, the challenges will be solved on the level of SBB. In such a case, the solutions will show well-defined building blocks as abstractions for systems design, and prove that these definitions are realizable in practice.

1.3.2 *Modeling and Control of Power Flow*

The ability to efficiently and cost-effectively control power flow in meshed dc systems will be crucial for the success of the technology. The primary function of all distribution systems is to safely, reliably and cost-effectively deliver electricity from the generators to the loads. However, the moment when multiple generation points and multiple paths for the current to flow exists a problem with overloading of some network parts arises. The local overloads, can occur in both dc and ac system. However, the solution options are different.

In ac systems, besides the voltage level, both frequency and phase angle can be be used to balance the flows of active and reactive powers. In dc systems, however, only the node voltage and the line resistance are left to control the power flow. Flexible alternating current transmission systems (FACTS) were proposed for ac systems to increase controllability and increase power transfer capability. FACTS grew very popular in system were power flow control is challenging. These networks are characterised by a high level of urbanisation and generation points that are distributed further away from load points.

In dc system only the node voltage and line resistance can be used to control the power flow. Different approaches were introduced for the power flow control in LVDC grids. The most basic method is based on changing the line resistance with a variable resistor and was described for both the HVDC and LVDC [29–31]. A second option is to dedicate a dc-dc converter rated for the full system power for a power flow control such as [32, 33]. The main advantages of the second approach are the versatility and robustness. Fully rated dc-dc converters are capable of controlling voltage and current. However, the assumption that the fully rated converter can always isolate a short-circuit does not hold. And despite the advances in the power electronics the cost and losses can for some applications be prohibitive. The losses and the investment cost from the system perspective can be reduced with a concept of a partially rated power flow control converters (PFCC) which were explored in [31, 34–36].

1.3.3 *Protection*

Protection of dc systems compared to corresponding ac systems is more challenging for electromechanical devices. The most obvious reason is the physical nature of dc - lack of natural zero-current crossings. The lack of zero-current poses a challenge for the mechanical parts of the breaker. Moreover, there are some typical characteristics of the LVDC systems that make the protection more difficult. The LVDC systems are usually highly capacitive and have comparably small line inductances, as a result of using predominantly voltage source

converters [37]. Consequently, in a low impedance grounded LVDC system during the short-circuit fault, the voltage on the fault drops rapidly, and the short-circuit current rises rapidly. This leads to fast and violent short-circuit transient behaviour.

Generally speaking, the protection challenges in meshed LVDC microgrids can be divided on system challenges and the protection device challenges. On the system level, the problem of paramount importance is achieving selectivity in fault clearing. Zonal protection schemes that are used in ac systems cannot be readily adopted. These schemes were designed for radial systems with unidirectional current flow. A unit based protection achieves selectivity using communication. A unit-based protection was proposed for LVDC systems in [37] and [38]. The communication however takes several milliseconds, unless fiberoptic connections are used [39]. An interlocking signals between the circuit breakers using fibreoptics ensured selective operation [40]. However, normal powerline communication introduces delays that are acceptable for high power systems, it is likely that in LVDC microgrids unit-based protection would have several unwanted consequences. Firstly, the system needs to be able to supply the short-circuit current for a prolonged period. Secondly, all components including cables, source converters and circuit breakers would need to be rated for higher short-circuit currents. The resulting oversizing would make the system less efficient and more expensive. Therefore, approaches not relying on communications are of more interest. A non-unit based protection using $\frac{\mathrm{d}i}{\mathrm{d}t}$ was proposed in [41] and [42]. In both cases, the protection scheme is tested only with simulation and under the assumption of very high ADC sampling speeds, which increases the cost of the solid-state circuit breaker (SSCB). Other non-unit based protection approaches rely on over-current or under-voltage threshold [43, 44].

On the device level, the research converges to two solutions: hybrid circuit breakers (HCB) [45] and SSCBs [46, 47]. The reason is that power electronic converters can not always implement short-circuit protection [48]. And the inadequacy of purely mechanical devices for the protection of dc systems. However, extensive use of semiconductor devices in protection brings forth new challenges. Firstly, the semiconductor devices due to their smaller size can withstand overcurrents only in the range of hundreds of μs[2]. Further operating limits are in the voltage withstand capability and the rate-of-change of current during turn-off. Since the solid-state based circuit breakers can interrupt fault current within tens of μs, the detection time becomes a significant period in the entire clearing process. Therefore, the design of the short-circuit detection must

[2]The comment has illustrative purpose. The topic is elaborated in more detail in Chapter 5.

ensure that the SSCB always meets the system requirements, ensure that the SSCB always operates within its safe operating area and meets the cost criteria.

1.4 RESEARCH AIM & OBJECTIVES

The main research aim of this thesis can be formulated as follows

Develop power electronics building blocks that offer power flow control and short-circuit protection for meshed LVDC microgrids with high avaialbility. The power electronics building blocks design aims for scalability and high efficiency.

The broad research objective is addressed via answering to following research questions

1. How differential power processing concept can be utilized in design of a power flow control converter for LVDC systems? How to create an efficient mathematical tool to study the behaviour of the power flow control converter in meshed LVDC microgrids?
2. How a three-port converter should be controlled such that power flow in bipolar meshed LVDC microgrid is efficiently regulated?
3. How a power flow control function block can be protected against grid short-circuits and become an efficient system building block of meshed LVDC microgrids?
4. What are the design criteria of a solid-state circuit breaker?

1.5 CONTRIBUTIONS

The key contributions of this work can be summarized as follows

- Proposal, modelling and validation of power flow control converter with partial power rating for unipolar and bipolar LVDC systems.
- Conceptualization and demonstration of a system building block with integrated short-circuit protection and power flow control.
- Complete analysis of zero-voltage switching conditions and reactive power losses of triple active bridge converter.

- Proposal and validation of power flow decoupling controller for triple active bridge converter.
- Derivation and analysis of design criteria for solid-state circuit breakers in LVDC systems.

1.6 THESIS OUTLINE & METHODS

Figure 1.2 shows the outline of this thesis. The thesis is divided into several parts based on the main problems and challenges that are addressed. The introduction chapter, together with chapter 6, elaborate system-level definitions and discuss associated challenges from the LVDC system perspective. Chapters 2,3 and 4 describe in detail different solutions that are needed to implement the proposed power flow control concept. Chapter 5 investigates the short-circuit protection challenges in LVDC.

Chapter 2 constitutes the modeling part of this thesis. In this chapter, a concept of partially rated power flow control converter (PFCC) is introduced. In this part, continuous-time, full-order large- and small-signal models of the PFCC are derived for the first time. The PFCC large-signal model is combined with the state-space model of the LVDC grid. Thus, they are creating a useful tool for studying and optimizing scalable LVDC systems with decentralized power flow control based on the PFCC. The models are experimentally validated, and the functionality of the PFCC is demonstrated in a laboratory-scale microgrid.

Chapter 3 together with chapter 4 form the part dealing with converter control-related challenges. Chapter 3 discusses the use of multi-port topology to facilitate different functions in the LVDC distribution system. Triple active bridge (TAB) converter is chosen from the multi-port topologies as a base for partially rated power flow control converter for bipolar LVDC grids. Since the TAB topology is known to suffer from coupled control variables, a novel decoupling controller is proposed. The controller is based on the Fourier series expansion. The state-space variables are decomposed into two components, which represent the active power and reactive power. The controller uses the transformer currents' active power components to decouple the active power flows between converter ports. The decoupling performance of the proposed controller is experimentally validated.

Since the efficiency of the multi-port topologies is of paramount importance for their deployment in LVDC systems, chapter 4 discusses the efficient operation boundaries of TAB. Using Fourier series expansion, a closed-form solution for soft-switching conditions is derived, taking into account different practical

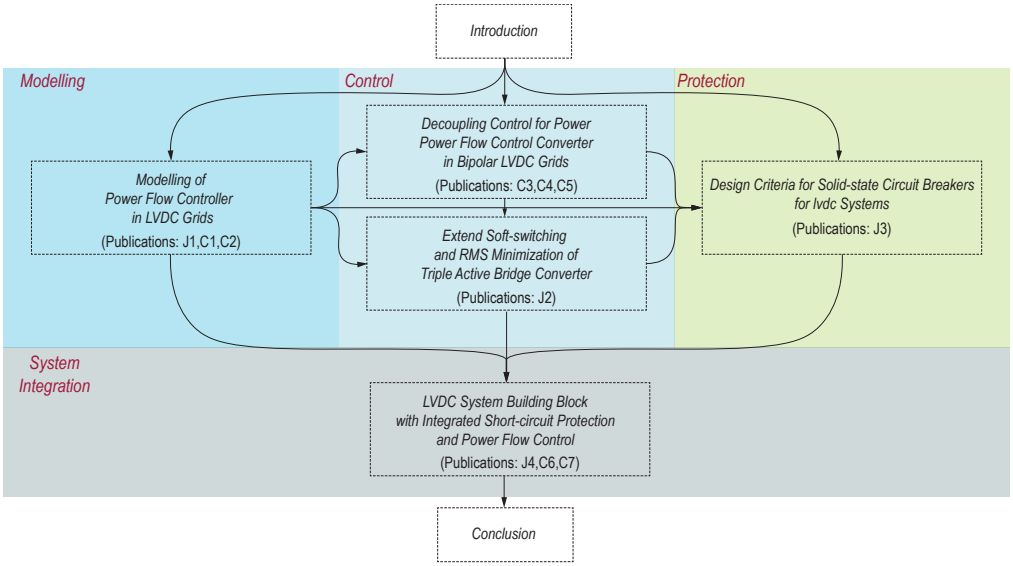


FIGURE 1.2: Thesis outline.

design aspects. The Fourier series model is further used to explore options for improving the TAB operation efficiency. A simple modulation improvement is proposed, which uses port voltages to reduce the RMS of transformer currents. A detailed loss model is used to show that the proposed modulation reduces switching, conduction, and magnetic losses. The analyses are validated with experimental results.

This thesis also addresses the protection challenges in LVDC systems. The protection part consists of chapter 5. Chapter 5 derives SSCB design criteria that consider the effect of different detection methods with varying delays of detection under variable system constraints. The design space is investigated in a sensitivity analysis, which provides insights into the operation boundaries of SSCB and explains how a combination of fault detection methods can reduce the SSCB size. SSCB prototype is developed and tested in different scenarios under nominal grid voltage and current. The derived design constraints can be used not only for efficient SSCB design but also to evaluate the effects of varying protection schemes on the required SSCBs.

In the last chapter of this thesis, chapter 6 returns to the definition of system building blocks. Chapter 6 presents a cost-effective system building block consisting of an SSCB and a PFCC with a partial power rating. The proposed system building block's primary functions are power flow control, overload currents limiting and increasing line power transfer capacity in a meshed LVDC grid while being capable of interrupting grid short-circuit currents. The

proposed building block enables a flexible solution for power flow control and short-circuits protection while maintaining high efficiency and low costs in meshed LVDC grids. The operation of the proposed system building block is validated with experiments.

Part I

MODELLING

2

MODELLING OF POWER FLOW CONTROL CONTROLLER IN LVDC GRIDS

This chapter introduces the concept of partially rated power flow control converter (PFCC). The main goal of PFCC is to support flexible and efficient power flow control in meshed LVDC microgrids. The continuous-time full-order large- and small-signal models of the PFCC are derived with the generalized averaging method. The PFCC models provide insights into controller design and stability analysis. The models are experimentally validated, and the functionality of the PFCC is demonstrated in a laboratory-scale microgrid.

This chapter is based on:

J1 P. Purgat, N. van der Blij, Z. Qin, P. Bauer-*"Partially Rated Power Flow Control Converter Modeling for Low Voltage DC Grids", IEEE Journal of Emerging and Selected Topics in Power Electronics*

C1 P. Purgat, R. A. Prakoso, L, Mackay, Z. Qin, P. Bauer-*"A partially rated DC-DC converter for power flow control in meshed LVDC distribution grids", 2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*

C2 P. Purgat, R. A. Prakoso, L, Mackay, L. Ramirez-Elizondo , P. Bauer-*"Power flow control converter for meshed LVDC distribution grids", 2017 IEEE Second International Conference on DC Microgrids (ICDCM)*

2.1 INTRODUCTION

2.1.1 *Power Flow Control Problem*

In any dc system, a challenge is to achieve efficient load sharing [49]. This challenge is inherent for multi-terminal (meshed) or ring topologies and is referred to as current limiting or power flow control [8], [31]. In the Fig. 2.1 is a basic meshed LVDC grid on which the principle of the power flow control and the voltage stepping can be explained. For the sake of simplicity, it is assumed that the nodes are connected by the cables of equal lengths and equal electrical characteristics. The grid is assumed to be in the steady state and the line impedances $Z_{\text{Line},1}$-$Z_{\text{Line},3}$ are only represented by the series resistances $R_1 = R_2 = R_3 = R$. During the operation node N_3 is disconnected. In such a case the equations of the line currents I_{Line_x} in the grid are

$$I_{\text{Line},2} = I_{\text{Line},3} = \frac{V_{1,2}}{2R} = \frac{V_1 - V_2}{2R}, \tag{2.1}$$

and

$$I_{\text{Line},1} = \frac{V_{1,2}}{R}, \tag{2.2}$$

where V_i is the voltage at the node N_i. In case that a significant amount of power from node 1 to node 2 needs to be transferred, the voltage difference $V_{1,2}$ between the two nodes will be increasing to a point where the current in the line 1 will reach the maximum rated value. In this special case, the current in the lines 2 and 3 will be only half the current in the line 1.

2.1.2 *Power Flow Control Options*

Different approaches were already introduced for the power flow control, both for the high voltage dc and the LVDC grids. Therefore, in this thesis only a short-literature

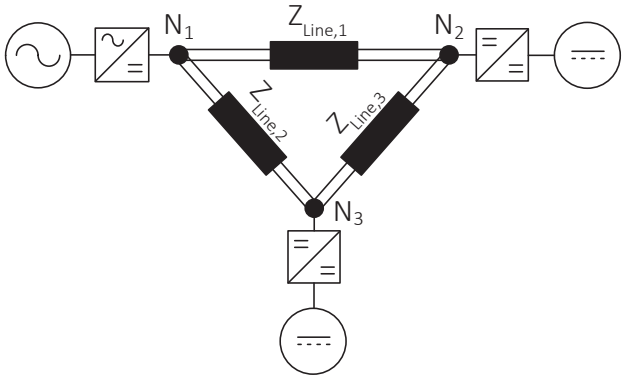


FIGURE 2.1: A simple meshed LVDC grid.

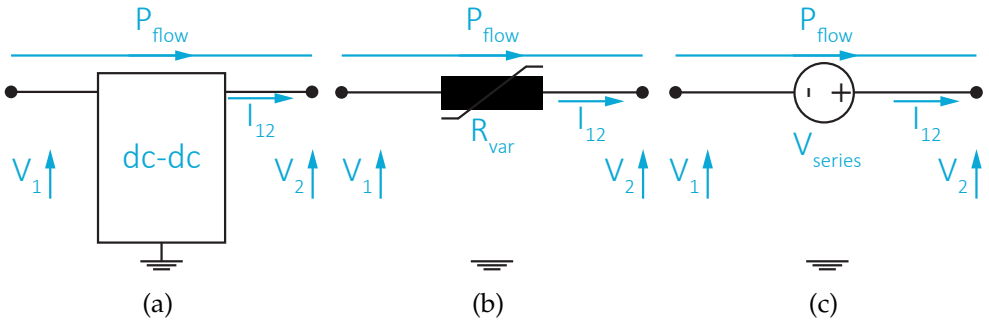


FIGURE 2.2: Power flow controller options. (a) represents fully rated dc-dc converter, (b) is the option employing variable resistance and in (c) is the series voltage injection power flow controller.

survey is provided. The first method is based on changing the line resistance with a variable resistor and was described for both the HVDC and LVDC [29–31]. Naturally, such an approach is inherently inefficient. The second approach to be found in the available literature is to dedicate a dc-dc converter rated for the maximum power transferred through the network such as [32, 33]. The main advantages of the fully rated converter are the versatility and robustness. However, the fully rated converter might not always be able to control the dc bus voltage. Moreover, the assumption that the fully rated converter can always isolate a short-circuit does not hold. Despite the advances in the power electronics the cost and losses can for some applications be prohibitive. The losses and the investment cost from the system perspective can be reduced with a concept of a partially rated power flow control converters (PFCC) which were explored in [31, 34] and [C1,C2].

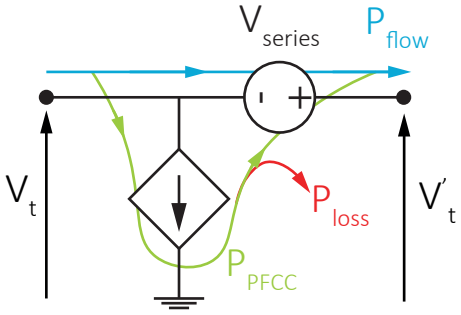


FIGURE 2.3: Partially rated power flow control converter- concept.

The core idea behind the PFCC can be illustrated using the example grid in Fig. 2.1 and Fig. 2.2. The power flow control is achieved by introducing a voltage drop in one of the lines. If the voltage drop is introduced in line 1, then the current in line 1 will be

$$I_{\text{Line},1} = \frac{V_{1,2} - V_{\text{series}}}{R}. \tag{2.3}$$

With proper control of V_{series} all lines can be forced into carrying the same current.

2.1.3 *Partially Rated Power Flow Control Converter*

The partially rated power flow control converter is in Fig. 2.4. The partial power rating arises from its series-parallel connection with the grid, as shown in Fig. 2.3. On one side the converter is connected to the full grid voltage, but only a fraction of the nominal grid current is flowing inside the converter. On the other side of the step-down transformer, the converter is connected in series with a line. Thus the current flowing on this side is the full network current. However, the operating voltage is a small fraction of the bus voltage. Achieving PFCC's partial power rating is straightforward with isolated topology. The transformer inside of the PFCC provides the voltage step down and the galvanic isolation. The transformer is essential to create a floating voltage V_{series} and allows the use of voltage derated components on the low voltage side of the PFCC. The isolation of the transformer needs to withstand the full grid voltage. A similar concept can be used in HVDC systems; however, the transformer manufacture complexity and cost would increase. The DAB topology is preferred due to its symmetry which offers easy implementation of bidirectional power flow, and further advantages are a low number of passive components and high power efficiency resulting from zero voltage switching. The DAB is connected to the line via unfolder full bridge. The unfolder bridge expands the operation of the PFCC into all four regions and extends the soft-switching operating area of the DAB by ensuring that the DAB operates with the unity of the voltage ratio. The operating range of V_{series} is dependent on the operating range of the bus voltage in the LVDC grid. Furthermore, the power that is processed by the PFCC is dependent on the maximum line current and the line impedance of the LVDC grid. The concrete minimum and maximum power rating of the PFCC, therefore, arise from the parameters of the grid in which it is installed. A similar concept was proposed for ac networks in 1995 [50]. The unified power flow controller (UPFC) was presented as a generalization of the static synchronous compensator devices. The UPFC is connected to the network via 50 Hz transformers on both sides. The UPFC uses common dc-link between the series and parallel connection to control the reactive and active power in the ac network. The heart of the UPFC and PFCC is the concept of differential power processing [51]. This concept, however, is more interesting for LVDC, as there is no need for bulky 50 Hz transformers, and the protection scheme can be simplified [C7]. The effect of series-parallel power flow control converters on the hvdc grid was studied in [52] and [53]. Both [52] and [53] focus on the grid level effects and formulation of the power flow control problem. The series-parallel converter is modeled as a general dc-dc converter, represented by controlled voltage and current sources. It was not the

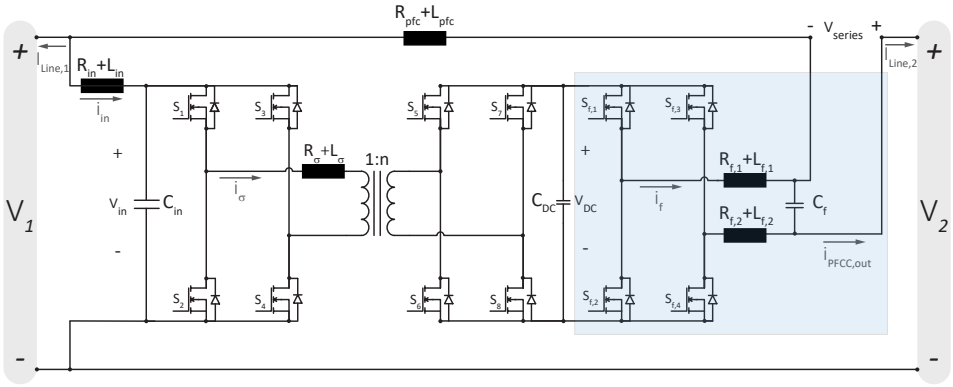


FIGURE 2.4: The power flow control converter for LVDC grids.

goal in this earlier work to consider and model the peculiarities of different topologies that are applicable for power flow control in hvdc or LVDC.

2.1.4 *Modelling*

Modeling of LVDC microgrids has been studied mostly to obtain insights into the control design [9], or stability [54]. Most of the models used for the LVDC microgrids use different state-space approaches to modeling of LVDC grids and are limited to the monopolar systems [55], [56]. Recently a generalized approach to modeling of the LVDC grids was introduced in [57], which allows for easy algorithmization in Python or Matlab/Simulink as well as the incorporation of the bipolar topologies.

Two basic approaches to modeling of the power electronic converters are switching models and average models. The switching models due to computational burden are too inefficient to be used as part of large systems such as microgrids. Average models can be obtained via an average switch, average inductor current or average state-space model. If the converter topology does not violate the small-signal ripple condition, then the use of various simplified average models such as [58] are appropriate. However, when the topology such as dual active bridge (DAB) violates the condition, one needs to resort to reduced-order models neglecting the current dynamics such as [59] or full-order discrete-time models such as [60] or [61]. However, to gain the insights into control and stability of the converter, it is often desirable to have continuous-time full order model [62]. The generalized average modeling technique was applied to the DAB in [62]. Recently it was improved to limit the small steady-state error in the closed-loop control signal of the DAB in [63] and even reformulated for the use with dc grid models in [64].

The main contributions of this chapter are the derivation and experimental verification of the average full-order large-signal and small-signal models of the PFCC. Furthermore, the large-signal model of the PFCC is coupled with the LVDC grid model

from [57]. This combination allows for easy simulation algorithmization, controller design and stability analysis of the PFCC controlled LVDC grids in Python or Matlab/Simulink, even for very complex systems. The PFCC models are validated by measuring the magnitude of the small-signal transfer functions. Furthermore, the models are validated via comparison of the dynamic performance in the laboratory-scaled microgrid. Additionally, the functionality of the PFCC in the meshed microgrid is demonstrated both in experiment and simulation.

2.2 MODELLING & CONTROL

2.2.1 *LVDC Grid Model*

An example of a dc distribution system consisting of three nodes is shown in Fig. 2.1. Any dc distribution system can be described by its N nodes, l distribution lines, o phase conductors, and m loads and sources (which are connected to the nodes via power electronic converters).

To describe the connectivity of dc distribution systems a so-called incidence matrix $\mathbf{\Gamma}$ is used.

$$\mathbf{\Gamma}(j,i) = \begin{cases} 1 & \text{if } \mathrm{I}_{\mathrm{Line},j} \text{ is flowing from node } i \\ -1 & \text{if } \mathrm{I}_{\mathrm{Line},j} \text{ is flowing into node } i \\ 0 & \text{otherwise} \end{cases}, \tag{2.4}$$

where i and j are the indices for each node and distribution line respectively. Therefore, $I_{\mathrm{Line},j}$ indicates the current flowing in the distribution line j. Furthermore, the boldface of variables indicates that they are vectors or matrices.

A lumped element π model is used for modelling the system's distribution lines. This lumped element model is valid when the length of the line is much shorter than the wavelength of the signals [65, 66]. Consequently, the dynamic behavior of dc distribution systems can be described by the differential equations of their node voltages and line currents.

The differential equations that describe the node voltages in the system are given by

$$\boldsymbol{C}_N \frac{\mathrm{d}}{\mathrm{d}t} \boldsymbol{V}_N = \boldsymbol{I}_N - \mathbf{\Gamma}^T \boldsymbol{I}_{\mathrm{Line}} - \boldsymbol{G}_N \boldsymbol{V}_N, \tag{2.5}$$

where $\boldsymbol{C}_N$ is the (diagonal) capacitance matrix, $\boldsymbol{G}_N$ is the conductance matrix, $\boldsymbol{V}_N$ are the node voltages, $\boldsymbol{I}_N$ are the currents flowing into each node (from the connected converters), and $\boldsymbol{I}_{\mathrm{Line}}$ are the line currents.

The currents of the distribution lines are described by the differential equations

$$\boldsymbol{L}_l \frac{\mathrm{d}}{\mathrm{d}t} \boldsymbol{I}_{\mathrm{Line}} = \mathbf{\Gamma} \boldsymbol{V}_N - \boldsymbol{R}_l \boldsymbol{I}_{\mathrm{Line}}, \tag{2.6}$$

where $\boldsymbol{L}_l$ and $\boldsymbol{R}_l$ are the (diagonal) inductance and resistance matrices respectively.

Subsequently, a state-space model of the whole dc distribution system can be derived. The voltages at the nodes and the currents in the lines are chosen as the state variables. The complete state space formulation is then given by

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} \boldsymbol{V}_N \\ \boldsymbol{I}_{\mathrm{Line}} \end{bmatrix} = \begin{bmatrix} -\boldsymbol{C}_N^{-1}\boldsymbol{G}_N & -\boldsymbol{C}_N^{-1}\boldsymbol{\Gamma}^{\boldsymbol{T}} \\ \boldsymbol{L}_l^{-1}\boldsymbol{\Gamma} & -\boldsymbol{L}_l^{-1}\boldsymbol{R}_l \end{bmatrix} \begin{bmatrix} \boldsymbol{V}_N \\ \boldsymbol{I}_{\mathrm{Line}} \end{bmatrix} + \begin{bmatrix} \boldsymbol{C}_N^{-1} \\ \emptyset \end{bmatrix} \boldsymbol{I}_N. \tag{2.7}$$

State-space models, like the one, presented in 2.7, can be efficiently applied for stability studies by inspecting the eigenvalues. Moreover, stability can be analyzed analytically or by using a root-locus method. This state-space dc distribution system model outputs the line currents and node voltages as a function of the currents flowing into each node ($\boldsymbol{I_N}$). Consequently, this system model can interface with any converter model that outputs a current as a function of the node voltage.

2.2.2 *Bipolar Systems*

For simplicity's sake, the model derived in this section is using a system that has a single phase conductor (i.e., a monopolar system). However, the models presented in this section can readily be extended to multiple phase conductors [65]. If the derived models are to be used for bipolar systems, the matrices $\boldsymbol{C}_N$, $\boldsymbol{G}_N$, and $\boldsymbol{L}_l$ are no longer diagonal only, but contain the mutual coupling between the phases. Moreover, the voltages and currents at each node are now specified for each polarity. The rest of the models derived in this chapter can be readily used in bipolar systems.

2.2.3 *Power Flow Control Converter Model*

The PFCC shown in Fig. 2.4 consists of two stages. The first stage is a DAB converter and the second is a full bridge converter. The DAB converter consists of two full bridges connected via transformer. Most of the power transferred through the DAB covnerter is in the fundamental ac component with the switching frequency of the converter. Modelling of the ac current of DAB prohibits usage of simple averaging method. To arrive to the full-order continuous-time model of the PFCC, generalized average modelling technique is reviewed and then the model is deployed.

2.2.3.1 *Recapitulation of Generalized Average Modelling*

The generalized average modeling method was derived in [67], motivated by the switching circuits that did not fulfill the small ripple condition. The generalized average modeling method was applied to the dual active bridge in [62]. These models were used to connect full bridge inverter and dual active bridge back-to-back in [68]. A considerable advantage of the generalized averaging method is that the standard state-space averaging is just a special case [67]. Thus one method can be applied for all variables in PFCC.

Because in the case of the dual active bridge the ac ripple in the current is far from being negligible, the generalized average modeling method needs to be applied.

The core idea is to represent the state-space variable during the switching interval $t - T_s \leq \tau < t$ using Fourier series approximation

$$x(\tau) = \sum_{k=-\infty}^{\infty} \langle x \rangle_k(t) e^{-jk\omega_s \tau}, \tag{2.8}$$

where $\langle x \rangle_k$ is the $k-th$ coefficient of the Fourier series and can be expressed as

$$\begin{aligned} \langle x \rangle_k(t) &= \frac{1}{T_s} \int_{t-T_s}^{t} x(\tau) e^{-jk\omega_s \tau} \mathrm{d}\tau \\ &= \frac{1}{T_s} \int_{t-T_s}^{t} x(\tau) \cos(k\omega_s \tau) \mathrm{d}\tau \\ &- \frac{j}{T_s} \int_{t-T_s}^{t} x(\tau) \sin(k\omega_s \tau) \mathrm{d}\tau. \end{aligned} \tag{2.9}$$

As shown for example in [67] or [62] using $\left\langle \frac{\mathrm{d}}{\mathrm{d}t} x \right\rangle_k (t)$ as representative of the average of the differential state variable, the derivative of the state-space variable is derived as

$$\frac{\mathrm{d}}{\mathrm{d}t} \langle x \rangle_k(t) = \left\langle \frac{\mathrm{d}}{\mathrm{d}t} x \right\rangle_k (t) - jk\omega_s \langle x \rangle_k(t). \tag{2.10}$$

The k-th coefficient of the product of the two variables x and y is

$$\langle xy \rangle_k = \sum_{i=-\infty}^{\infty} \langle x \rangle_{k-i} \langle y \rangle_i. \tag{2.11}$$

If the 1st and -1st coefficient of the the Fourier series are complex conjugates than the product of the zero-th coefficients becomes

$$\langle xy \rangle_0 = \langle x \rangle_0 \langle y \rangle_0 + 2 \left(\langle x \rangle_{1R} \langle y \rangle_{1R} + \langle x \rangle_{1I} \langle y \rangle_{1I} \right). \tag{2.12}$$

For the first coefficients the products become

$$\langle xy \rangle_{1R} = \langle x \rangle_0 \langle y \rangle_{1R} + \langle x \rangle_{1R} \langle y \rangle_{1I}, \tag{2.13}$$

$$\langle xy \rangle_{1I} = \langle x \rangle_0 \langle y \rangle_{1I} + \langle x \rangle_{1I} \langle y \rangle_{1I}. \tag{2.14}$$

The subscripts 'R'and 'I' represent the real and the imaginary parts of the complex numbers, respectively. These are necessary preliminaries to deploy the PFCC models in the next subsections.

2.2.3.2 *Large-signal Model*

The generalized average modeling approach that was summarized in the previous subsection will be applied to the circuit from Fig. 2.4. The model of the PFCC in this paper is derived under the assumption that the magnetizing current in the transformer is negligible. For all mosfets in the PFCC, it is assumed that the voltage drop across

the mosfets' diodes is insignificant and that the mosfets' switching transients are insignificant. The voltages in the PFCC are referred to the low voltage side and where appropriate are divided by n - turns ratio of the transformer. The parasitic resistances of the mosfets and the transformer of the DAB are all lumped into one parasitic element referred to as R_σ, while the parasitic resistances of the mosfets and the filter inductors of the unfolder bridge are lumped into R_f.

When using the phase-shift modulation for control of the DAB the voltage on the high voltage $v_{hv}(\tau) = s_1(\tau)v_{c_1}(\tau)$ is achieved through the switching action which is defined as

$$s_1(\tau) = \begin{cases} 1 & \text{in} \quad 0 \leq \tau < \frac{T_s}{2} \\ -1 & \text{in} \quad \frac{T_s}{2} < \tau < T_s \end{cases}. \tag{2.15}$$

On the low voltage side the voltage $v_{lv}(\tau) = s_2(\tau)v_{\text{dc}}(\tau)$ is achieved through the switching action which is defined as

$$s_2(\tau) = \begin{cases} 1 & \text{in} \quad \frac{\varphi T_s}{2} \leq \tau < \frac{T_s}{2} + \frac{\varphi T_s}{2} \\ -1 & \text{in} \quad 0 \leq \tau < \frac{\varphi T_s}{2} \quad \text{and} \quad \frac{T_s}{2} + \frac{\varphi T_s}{2} \leq \tau < T_s \end{cases}. \tag{2.16}$$

The voltage between midpoints of the unfolder bridge is defined as a product of the switching coefficient $s_3(\tau)$ and the voltage v_{dc}. The switching coefficient is defined as

$$s_3(\tau) = \begin{cases} 1 & \text{in} \quad 0 \leq \tau < d_2'' T_s \\ -1 & \text{in} \quad d_2'' T_s < \tau < T_s \end{cases}. \tag{2.17}$$

The operation of the PFCC can be described with the following equations

$$L_{\text{in}} \frac{\text{d}}{\text{d}\tau} i_{\text{in}}(\tau) = v_1(\tau) - v_{\text{in}}(\tau) - R_{\text{in}} i_{\text{in}}(\tau), \tag{2.18}$$

$$C_{\text{in}} \frac{\text{d}}{\text{d}\tau} v_{\text{in}}(\tau) = i_{\text{in}}(\tau) - s_1(\tau) i_\sigma(\tau), \tag{2.19}$$

$$L_\sigma \frac{\text{d}}{\text{d}\tau} i_\sigma(\tau) = - R_\sigma i_\sigma(\tau) + v_{hv}(\tau) - n v_{lv}(\tau), \tag{2.20}$$

$$C_{\text{dc}} \frac{\text{d}}{\text{d}\tau} v_{\text{dc}}(\tau) = s_2(\tau) n i_\sigma(\tau) + s_3(\tau) i_f, \tag{2.21}$$

$$L_{\text{f}} \frac{\text{d}}{\text{d}\tau} i_f(\tau) = - R_f i_f(\tau) + v_{\text{dc}}(\tau) s_3(\tau) - v_{\text{series}}(\tau), \tag{2.22}$$

$$C_{\text{f}} \frac{\text{d}}{\text{d}\tau} v_{\text{series}}(\tau) = \frac{1}{R_{\text{pfc}}} \left[v_2(\tau) - v_1(\tau) + v_{\text{series}}(\tau) \right] + i_f(\tau). \tag{2.23}$$

In (2.18)-(2.23) the role of L_{pfc} is neglected. The reason is that the connection is short, and is separated by the capacitors on each side. Therefore, to keep the number of state-space variables low, it is not used explicitly. The derivation of the average large-signal model of the PFCC is completed with the introduction of the Fourier coefficients of the switching signals $s_1(\tau)$, $s_2(\tau)$ and $s_3(\tau)$. For the coefficients of $s_1(\tau)$

and $s_2(\tau)$ it is assumed as in [62], that the duty ratio is fixed at 50%. Consequently, the coefficients are

$$\langle s_1 \rangle_0 = \langle s_1 \rangle_{1R} = \langle s_2 \rangle_0 = 0, \tag{2.24}$$

and

$$\langle s_1 \rangle_{1I} = -\frac{2}{\pi}, \tag{2.25}$$

$$\langle s_2 \rangle_{1R} = -\frac{2\sin(d_1\pi)}{\pi}, \tag{2.26}$$

$$\langle s_2 \rangle_{1I} = -\frac{2\cos(d_1\pi)}{\pi}. \tag{2.27}$$

For the unfolder bridge the Fourier coefficients are

$$\langle s_3 \rangle_0 = 2d_2' - 1, \tag{2.28}$$

$$\langle s_3 \rangle_{1R} = \frac{\sin(2\pi d_2')}{\pi}, \tag{2.29}$$

$$\langle s_3 \rangle_{1I} = -\frac{2}{\pi}\sin^2\left(\pi d_2'\right). \tag{2.30}$$

Applying the generalized average modeling method on the PFCC is somewhat cumbersome. Therefore the equations are not presented herein detail to keep the description concise. The average model of the PFCC is simplified by assuming that besides the DAB transformer current i_σ, it is appropriate to represent the variables by their zero-order terms, as was done for example in the [62]. The main difference between the DAB transformer current and other currents in the model is that in the DAB it is only ac components that transfer power, while its dc component is equal to zero. The precision of the modeling can be improved by including the ac components of other variables. However, that would make the model unnecessarily complicated and as is argued in [62] with limited gains in precision.

In the following equations the control signal of the unfolder bridge is rewritten as $d_2 = 2d_2' - 1$. The PFCC is described in the matrix form

$$\frac{\mathrm{d}}{\mathrm{d}t}\bar{x} = \boldsymbol{A}\bar{x} + \boldsymbol{B}\bar{u},$$

where

$$\bar{x} = \begin{bmatrix} i_{\text{in}} & v_{\text{in}} & v_{\text{dc}} & i_{\sigma,1R} & i_{\sigma,1I} & i_f & v_{\text{series}} \end{bmatrix},$$
$$\bar{u} = \begin{bmatrix} v_1 & v_2 \end{bmatrix}.$$

In vectors $\bar{x}$ and $\bar{u}$, only the DAB inductor current is modeled with ac components $i_{\sigma,1R}$, $i_{\sigma,1I}$. The rest of the variables is represented by the zero-th order coefficient which is dominant. The matrices $\boldsymbol{A}$ and $\boldsymbol{B}$ are in eq. (2.31).

$$
\boldsymbol{A} = \begin{bmatrix}
-\frac{R_{\text{in}}}{L_{\text{in}}} & -\frac{1}{L_{\text{in}}} & 0 & 0 & 0 & 0 & 0 \\
\frac{1}{C_{\text{in}}} & 0 & 0 & 0 & \frac{4}{\pi C_{\text{in}}} & 0 & 0 \\
0 & 0 & 0 & -\frac{4n\sin(d_1\pi)}{\pi C_{\text{dc}}} & -\frac{4n\cos(d_1\pi)}{\pi C_{\text{dc}}} & \frac{d_2}{C_{dc}} & 0 \\
0 & 0 & \frac{2n\sin(d_1\pi)}{\pi L_\sigma} & \frac{-R_\sigma}{L_\sigma} & \omega_s & 0 & 0 \\
0 & -\frac{2}{\pi L_\sigma} & -\frac{2n\cos(d_1\pi)}{\pi L_\sigma} & -\omega_s & \frac{-R_\sigma}{L_\sigma} & 0 & 0 \\
0 & 0 & \frac{d_2}{L_f} & 0 & 0 & -\frac{R_f}{L_f} & \frac{1}{L_f} \\
0 & 0 & 0 & 0 & 0 & \frac{1}{C_f} & -\frac{1}{R_{\text{pfc}}C_f}
\end{bmatrix},
$$

$$
\boldsymbol{B} = \begin{bmatrix}
\frac{1}{L_{\text{in}}} & 0 \\
0 & 0 \\
0 & 0 \\
0 & 0 \\
0 & 0 \\
0 & 0 \\
-\frac{1}{R_{\text{pfc}}C_{\text{f}}} & \frac{1}{R_{\text{pfc}}C_{\text{f}}}
\end{bmatrix}. \tag{2.31}
$$

2.2.3.3 *Large-signal PFCC and Grid Model*

As was explained in the second section of this paper the converter models in the grid need to use node voltages as their inputs and node currents as their output to the dc grid model. From the Fig. 6.2 and Fig. 2.5 it should be clear that the voltages V_1, V_2, highlighted in blue, are the inputs from the dc grid model to the PFCC model. The currents flowing out of the PFCC, highlighted in green, are the outputs of the large signal PFCC model to the grid model. These currents can be specified from the derived large signal PFCC model. For the current $I_{\text{Line},2}$ we can write

$$
I_{\text{Line},2} = \frac{1}{R_{\text{pfc}}}\left(V_2 - V_1 + v_{\text{series}}\right), \tag{2.32}
$$

and for the current in the line 1 we can write

$$
I_{\text{Line},1} = I_{\text{Line},2} - i_{\text{in}}. \tag{2.33}
$$

Using (2.32) and (2.33) we can efficiently couple the PFCC large signal model with the LVDC grid model.

2.2.3.4 *Small-signal Model*

To derive the small-signal average model of the converter, we first define the small-signal deviations as $\Delta d_1 = d_1 - D_1, \Delta d_2 = d_2 - D_2, \Delta v_{in} = v_{\text{in}} - V_{\text{in}}, \Delta i_{in} = i_{\text{in}} - I_{\text{in}}, \Delta v_{\text{dc}} = v_{\text{dc}} - V_{\text{dc}}, \Delta i_{\sigma,1R} = i_{\sigma,1R} - I_{\sigma,1R}, \Delta i_{\sigma,1I} = i_{\sigma,1I} - I_{\sigma,1I}, \Delta i_f = i_f - I_f, \Delta v_{\text{series}} = v_{\text{series}} - V_{\text{series}}, \Delta v_1 = v_1 - V_1, \Delta v_2 = v_2 - V_2,$

where Δ defines the small signal state, the upper case letters represent the dc terms and the lower case letters the large signal states.

Since the PFCC's mathematical description contains multiplication of the two state variables, it is necessary to define the following

$$\begin{aligned}\sin(\pi d_1)v_{\text{dc}} = &\sin(\pi D_1)\Delta v_{\text{dc}} + V_{\text{dc}}\sin(\pi D_1) \\ &+ V_{\text{dc}}\cos(\pi D_1)(\pi\Delta d_1).\end{aligned} \tag{2.34}$$

The small signal model of the PFCC is given in the matrix form

$$\frac{\mathrm{d}}{\mathrm{d}t}\Delta\bar{x} = \boldsymbol{A}\Delta\bar{x} + \boldsymbol{B}\Delta\bar{u} + \boldsymbol{N}\Delta\bar{w}, \tag{2.35}$$

where

$$\begin{aligned}\Delta\bar{x} &= \begin{bmatrix}\Delta i_{\text{in}} & \Delta v_{\text{in}} & \Delta v_{\text{dc}} & \Delta i_{\sigma,1R} & \Delta i_{\sigma,1I} & \Delta i_f & \Delta v_{\text{series}}\end{bmatrix}, \\ \Delta\bar{u} &= \begin{bmatrix}\Delta d_1 & \Delta d_2\end{bmatrix}, \\ \Delta\bar{w} &= \begin{bmatrix}\Delta v_1 & \Delta v_2\end{bmatrix},\end{aligned}$$

and the matrices $\boldsymbol{A}$, $\boldsymbol{B}$ and $\boldsymbol{N}$ are in eq. (2.36).

The transfer functions between control inputs and output voltages when the disturbances on voltages V_1 and V_2 are neglected are obtained using the well-known relation for the transfer function matrices

$$\boldsymbol{G}(s) = \boldsymbol{C}\left(\boldsymbol{E}s - \boldsymbol{A}\right)^{-1}\boldsymbol{B}, \tag{2.37}$$

where s is the complex variable in Laplace domain.

In order to measure the ratio between controlled voltages and the control signals the matrix $\boldsymbol{C}$ is defined as

$$\boldsymbol{C} = \begin{bmatrix}0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1\end{bmatrix},$$

then the transfer function matrix becomes

$$\boldsymbol{G}(s) = \begin{bmatrix}G_{1,1}(s) & G_{1,2}(s) \\ G_{2,1}(s) & G_{2,2}(s)\end{bmatrix} = \begin{bmatrix}\frac{\Delta v_{\text{dc}}}{\Delta d_1} & \frac{\Delta v_{\text{dc}}}{\Delta d_2} \\ \frac{\Delta v_{\text{series}}}{\Delta d_1} & \frac{\Delta v_{\text{series}}}{\Delta d_2}\end{bmatrix}. \tag{2.38}$$

$$
\boldsymbol{A} = \begin{bmatrix}
-\frac{R_{\text{in}}}{L_{\text{in}}} & -\frac{1}{L_{\text{in}}} & 0 & 0 & 0 & 0 & 0 \\
\frac{1}{C_{\text{in}}} & 0 & 0 & 0 & \frac{4}{\pi C_{\text{in}}} & 0 & 0 \\
0 & 0 & 0 & -\frac{4n\sin(D_1\pi)}{\pi C_{\text{dc}}} & -\frac{4n\cos(D_1\pi)}{\pi C_{\text{dc}}} & \frac{D_2}{C_{dc}} & 0 \\
0 & 0 & \frac{2n\sin(D_1\pi)}{\pi L_\sigma} & \frac{-R_\sigma}{L_\sigma} & \omega_s & 0 & 0 \\
0 & -\frac{2}{\pi L_\sigma} & -\frac{2n\cos(D_1\pi)}{\pi L_\sigma} & -\omega_s & \frac{-R_\sigma}{L_\sigma} & 0 & 0 \\
0 & 0 & \frac{D_2}{L_f} & 0 & 0 & -\frac{R_f}{L_f} & \frac{1}{L_f} \\
0 & 0 & 0 & 0 & 0 & \frac{1}{C_f} & -\frac{1}{R_{\text{pfc}}C_f}
\end{bmatrix},
$$

$$
\boldsymbol{B} = \begin{bmatrix}
0 & 0 \\
0 & 0 \\
-\frac{4n}{\pi C_{\text{dc}}}\left(I_{\sigma,1I}\sin(\pi D_1) - I_{\sigma,1R}\cos(\pi D_1)\right) & \frac{I_{\text{f}}}{C_{\text{dc}}} \\
\frac{2n}{L_\sigma}V_{\text{dc}}\cos(\pi D_1) & 0 \\
-\frac{2n}{L_\sigma}V_{\text{dc}}\sin(\pi D_1) & 0 \\
0 & \frac{V_{\text{dc}}}{L_f} \\
0 & 0
\end{bmatrix}, \boldsymbol{N} = \begin{bmatrix}
\frac{1}{L_{\text{in}}} & 0 \\
0 & 0 \\
0 & 0 \\
0 & 0 \\
0 & 0 \\
0 & 0 \\
-\frac{1}{R_{\text{pfc}}C_{\text{f}}} & \frac{1}{R_{\text{pfc}}C_{\text{f}}}
\end{bmatrix}. \tag{2.36}
$$

2.2.4 *PFCC Control*

The averaged small-signal models derived in Section 2 are used here to choose closed-loop controllers for the PFCC. The PFCC has a middle-link dc voltage, which is the output of the DAB. The DAB implements a simple phase-shift modulation. Figure 2.9a depicts the DAB converter control-to-output transfer function. Increasing the switching frequency f_s of the DAB results in decreasing the leakage inductance L_σ needed to transfer the amount of power. Thus, changes in the switching frequency and leakage inductance cancel each other out. As is visible from the transfer function $G_{1,1}(s)$ in Fig. 2.9a, DAB has one significant pole, which is dominated by the output capacitance. Increasing the size of the output capacitor C_{dc} limits the bandwidth of DAB even further. The fact that DAB has only one significant pole means that a PI controller is a good starting candidate for the control of voltage V_{dc}. The developed models allow to investigate the influence of other parameters on the voltage V_{dc} such as Δd_2, Δv_1 and Δv_2. A short design procedure based on [69] follows. The equation of PI controller for V_{dc} is

$$
C_{\text{PI,dc}}(s) = K_{\text{dc},1} + \frac{K_{\text{dc},2}}{s}. \tag{2.39}
$$

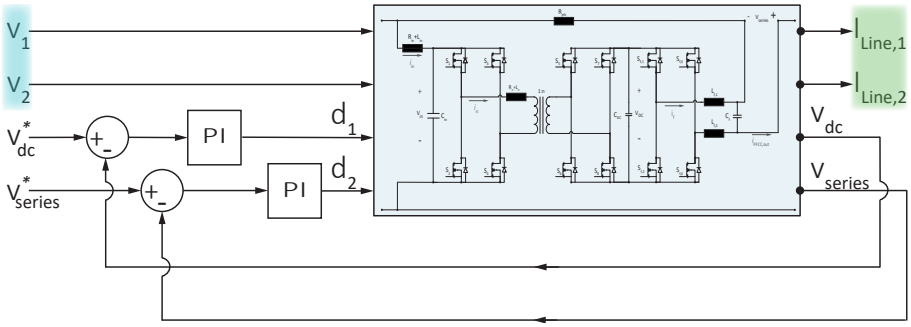


FIGURE 2.5: The PFCC with the closed-loop control of the dc link voltage V_{dc} and floating voltage V_{series}. The inputs to the PFCC large signal model from the dc grid model are highlighted in the blue rectangle. The outputs of the PFCC large signal model that are returned to the dc grid model are highlighted in the green rectangle.

Figure 2.9a exhibits one significant pole, and the corner frequency can be found in the point for which the magnitude falls by -3 dB. The design procedure in [69] can be simplified and the proportional gain $K_{\text{dc},1}$ can be written

$$K_{\text{dc},1} = \frac{f_c \zeta}{2\pi f_o}, \tag{2.40}$$

where ζ is the relative damping and typically is chosen to be $\frac{1}{\sqrt{2}}$, f_o stands for natural system frequency and f_c stands for the corner frequency. The integral gain is then

$$K_{\text{dc},2} = \frac{1}{\pi f_o} \left(\frac{\pi}{2} f_c\right)^2. \tag{2.41}$$

The full bridge converter in the presented power flow control converter can operate in three different modes:

1. *Unfolder Mode*: The amplitude of the series voltage V_{series} is controlled by the DC-DC isolated converter, the polarity of the voltage is given by the full bridge converter which unfolds the output of the DAB converter. In this mode the switching losses of the full bridge converter are eliminated.

2. *Buck Mode*: When the series voltage is too small, and the DAB would loose the ZVS on the LV side. The full bridge converter enters the buck mode to keep the minimum voltage for the ZVS on DAB and simultaneously meet the control objective.

3. *Bypass Mode*: When no intervention of the power flow control converter is required, the full bridge enters the bypass mode. In this mode switches $S_{f,1}$ and $S_{f,3}$(or $S_{f,2}$ and $S_{f,4}$) are ON. This mode reduces the stand-by losses of the PFCC.

The unfolder bridge in the buck mode operates with bipolar modulation. Inspecting Fig. 2.9b, unfolder bridge exhibits one significant pole which is dominated by the

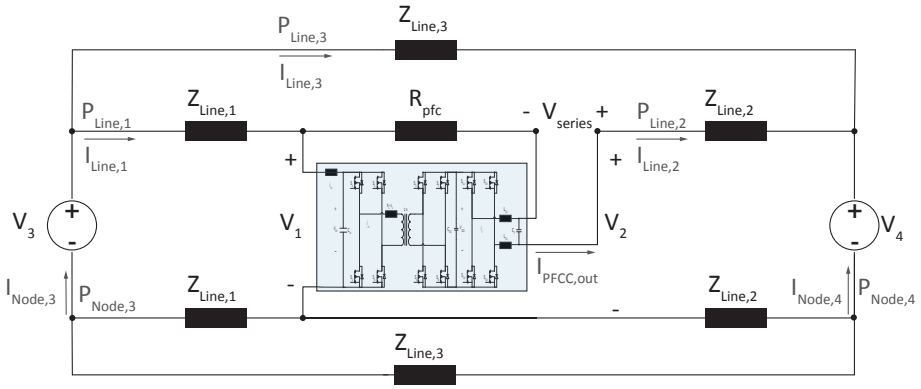


FIGURE 2.6: The basic meshed grid, for simulation and experiment. In the simulation, node 3 is holding voltage V_3 constant, while node 4 works as a constant power load, i.e., voltage V_4 is not held constant. In the experiment, the nodes 3 and 4 are emulated with laboratory power supplies SM15K.

output capacitance. The influence of the filter inductor is attenuated by parasitic resistance. To control voltage V_{series} it sufficient to use a PI controller. The procedure outlined in equations 2.40 and 2.41 or algebra-on-the-graph method can be used to choose $K_{\text{unf},1}$ and $K_{\text{unf},2}$. The PI controllers can be prone to high-frequency disturbances. In this chapter, it is assumed that the LVDC grid is strongly capacitive, and there are no high-frequency disturbances. The control loops used in this paper are kept simple since the PFCC control is not the primary focus of the paper.

2.3 SIMULATION & SENSITIVITY ANALYSIS

In the previous section a model of dc grid and a large-signal model of PFCC were developed. In this section, the dc grid model is used together with the PFCC large-signal model to demonstrate the usefulness of the derived models. The models are used to simulate multi-terminal LVDC grid with the PFCC, in which the functionality of the PFCC can be studied. The section closes with a brief discussion on the sensitivity of the models to the line parameters.

2.3.1 *Meshed Grid*

In this subsection, the derived PFCC large signal model is used together with the dc grid model to simulate a simple case, which can be to a large extent reproduced in the laboratory. The schematic of the grid used in the simulation is shown in 2.6. The case study is based on the ring/meshed grid topology and allows the power to circulate in the grid. The grid consists of four nodes, where node 1 and 2 are the output and input of the PFCC respectively. Nodes 3 and 4 are supplying or sinking the power in the grid. The power flows in the lines $P_{\text{Line},2}$ and $P_{\text{Line},3}$ are coupled as the nodes are not

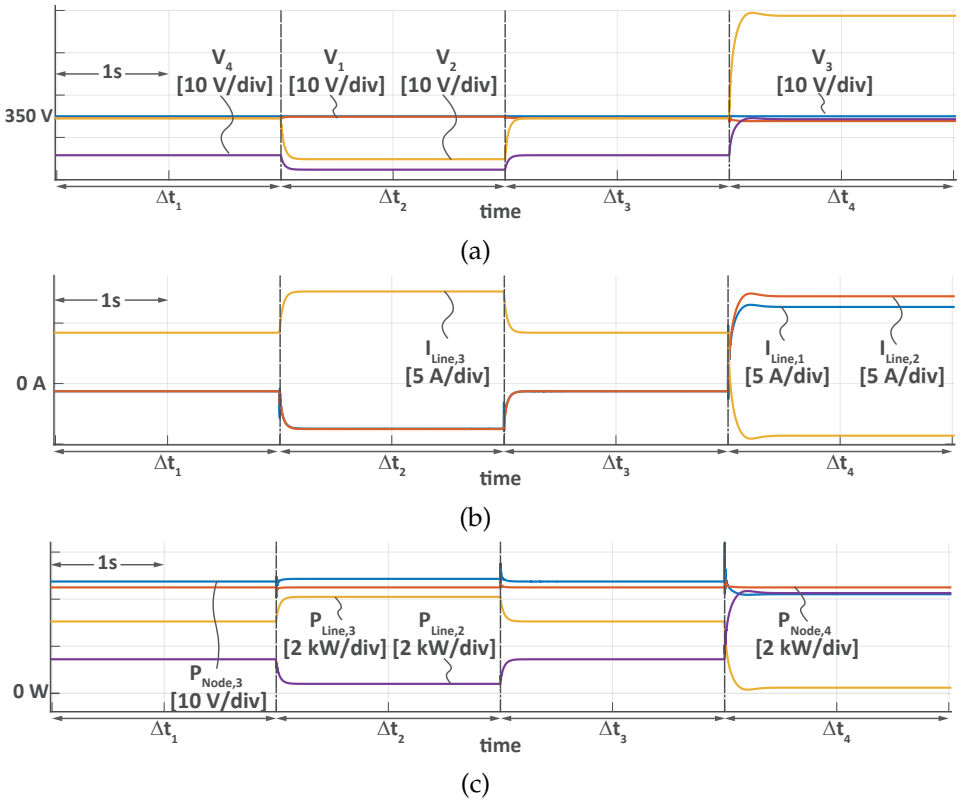


FIGURE 2.7: At the start of the simulation, the injected voltage is zero, and the line resistances give the ratio between the currents in the lines. During the simulation, the power flow in the lines is altered by the PFCC. The grid voltages are in (a), the currents in (b) and the powers are in (c).

ideal voltage sources. The PFCC is used to inject the voltage in series with the line to change the amount of power flowing through different lines, as well as to change the direction of power in lines.

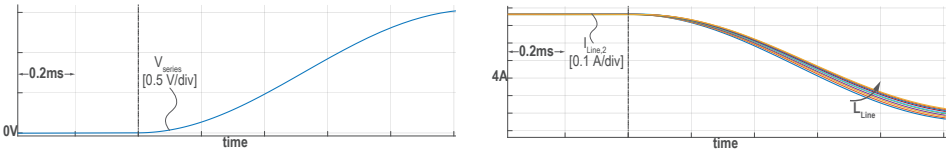
In the simulation, node 3 is modeled as a voltage source converter with dc grid side capacitance C_{Node}. Node 3 holds the voltage V_3 constant at 350 V. Node 4 is modeled as a constant power load, which is set to sink 4.5 kW and has the capacitance C_{Node} on the dc grid side. The rest of the parameters is shown in the Table 2.1.

In Fig. 2.7a the voltages in the simulated grid are shown. The voltage V_3 remains stable during the simulation. The voltage V_4 is changing as the node is programmed to behave as a constant power load. The voltages V_1 and V_2 are the voltages at the input and output of the PFCC respectively. In Fig. 2.7b the currents flowing in the grid are shown. Figure 2.7c shows the powers flowing in the grid. The current direction defines the direction of the power flow. Arrows in Fig. 2.6 represent the direction convention.

The simulation starts with 0 V being injected in series with the line, during time interval Δt_1. The current flowing in line three $I_{\text{Line},3}$ is higher than the current flowing

TABLE 2.1: The parameters of the grid used for simulation

Parameter	Acronym	Value
Line resistance 1	$R_{Line,1}$	100 mΩ
Line resistance 2	$R_{Line,2}$	1 Ω
Line resistance 3	$R_{Line,3}$	2 Ω
Line inductance 1,2,3	L_{Line}	1 µH
Line capacitance 1,2,3	C_{Line}	10 nF
Node capacitance	C_{Node}	1 mF
Inner pfcc resistance	R_{pfc}	1 Ω
Nominal Node 3 Voltage	V_3	350 V
Nominal Node 4 Voltage	V_4	350 V



(a) (b)

FIGURE 2.8: The line inductance in each line was varied from 1 μH to 100 μH, and the different system response to a disturbance was observed. The disturbance is the change of the injected series voltage. The series voltage is shown in (a) and the current flowing out of the PFCC in line 2 is shown in (b).

in the line containing the PFCC. During second time interval Δt_2, -10 V is injected in series with line 2. The series voltage increases the current flowing in line 3. The power flow in line 3 is reversed during fourth time interval Δt_4, when the PFCC injects 25 V. At this point, almost all the power between the nodes is flowing through line two, $P_{Line,2}$. The power flowing through line three is close to zero. Coincidently, in this case, the reduction of the power flow in line three makes the system more efficient as can be seen by the reduced power $P_{Node,3}$.

2.3.2 *Sensitivity of the model to the line parameters*

In the section 2 of this paper a modeling approach was described which allows to model the line inductance, line capacitance, line resistance, and even line conductance. It is interesting to investigate the influence of the line parameters on the operation of the PFCC due to several reasons. Firstly, the PFCC must be designed to operate reliably under a range of line parameters, not just a single value. Secondly, the line

parameters and impedances as discussed in the introduction influence the power rating of the PFCC. Lastly, the grid parameters influence the experiments. Therefore, before the simulation results are compared with the experimental data, it is vital to consider which parameters influence the results of the experiment significantly. The line conductance has virtually no influence in the small monopolar system on the system itself or the PFCC operation. Therefore, it can be disregarded. However, the other line parameters might influence the operation of both the grid and the PFCC.

Line resistance is a series parasitic. The influence of this parameter is straightforward to asses. The higher the line resistance, the higher the voltage drop across it and less current can be pushed through for the same power level. In the experiments, this parameter can be controlled with precision up to hundredths of milliohm.

The influence of the line capacitance and line inductance is more difficult to asses. The influence of the line capacitance on the operation of the PFCC can be overshadowed by the size of the nodes' capacitances and the capacitances of the PFCC. During the experiments the node and PFCC capacitances were much higher than the line capacitances, $C_{\text{node}} >> C_{\text{line}}$. The small line capacitance is the result of small cable cross-sections and very short cable connections. Therefore it can be concluded that the line capacitances have negligible influence on the overall dynamics of the experiment.

The influence of the line inductances on the dynamics of the PFCC is analyzed via simulation of the system from the previous subsection. Figure 2.8 shows the influence of the changing line inductance on the output current of the PFCC $I_{\text{Line},2}$. The increase in the line inductances slows down the change of the output current. In Fig. 2.8b the variation of the output current of the PFCC is evident. It is critical to address as, during the experimental measurements, the line inductances are frequency dependent parasitic elements and as such challenging to measure precisely, and their influence can be in the range of tens of milliamperes.

2.4 EXPERIMENT & DISCUSSION

The closed-loop control of the PFCC is implemented in a *C2000 Delfino LaunchPad*. The parameters of the prototype are summarised in Table 2.2, and the grid parameters are the same as in Table 2.1.

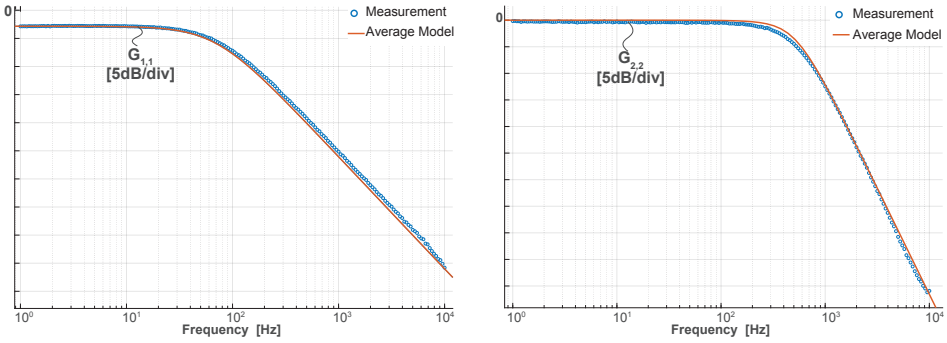
During all experiments in this paper, Delta Elektronika SM-15K power supplies are used to emulate the nodes. Since in a real meshed LVDC grid, there are typically more lines than voltage controlling converters the resulting power flows are coupled. To mimic the meshed LVDC grid the power flows in lines $P_{\text{Line},2}$ and $P_{\text{Line},3}$ are coupled.

2.4.1 *Models Validation*

Figure 2.9 shows the comparison of calculated and measured control-to-output gains of the PFCC. Since it is impractical to measure transfer functions of the PFCC with open-loop, the transfer function of the DAB and unfolder are measured separately. The transfer functions were measured using the Bode 100 vector analyzer. The measurement of the transfer functions with Bode 100 is described for example in [70]. The comparison of the measured and simulated transfer functions is shown in Fig. 2.9. It is clear from

TABLE 2.2: The design parameters of the PFCC prototype

Parameter	Acronym	Value
Nominal Input Voltage	$V_{in,nom}$	350 [V]
Nominal DC-link Voltage	V_{dc}	50 [V]
Transformer ratio	n	7 [-]
Switching Frequency	f_s	83 [kHz]
Parasitic Inductance	L_σ	78 [μH]
Input DC Capacitor	C_{in}	16 [μF]
DC-link Capacitor	C_{DC}	1.22 [mF]
Unfolder Bridge Inductor	$L_{f,i}$	31 [μH]
Unfolder Bridge Capacitor	C_f	1.22 [mF]



(a) (b)

FIGURE 2.9: Small-signal model verification. In (a) is the measured and the calculated transfer function between the control signal d_1 and the voltage v_{dc} of the DAB. In (b) is the measured and the calculated transfer function between the control signal d_2 and the voltage v_{series} of the unfolder bridge.

the figures that the measurement and simulation show very good match. The somewhat low cross-over frequency is caused by the considerable size of the capacitor bank of the prototype PFCC.

The small signal model derived in section 2 was validated via measurement of the transfer functions. The dc grid model with the large signal PFCC model is validated in this subsection in the time domain. The laboratory-scale microgrid is schematically shown in Fig. 2.6. The voltages V_3 and V_4 are programmed for the same initial voltage of 350 V. The voltage reference V^*_{series} is stepped from 0 V to 5 V at the time instance t_{step}. The experiment is repeated with a different V_{series} PI controller parameters.

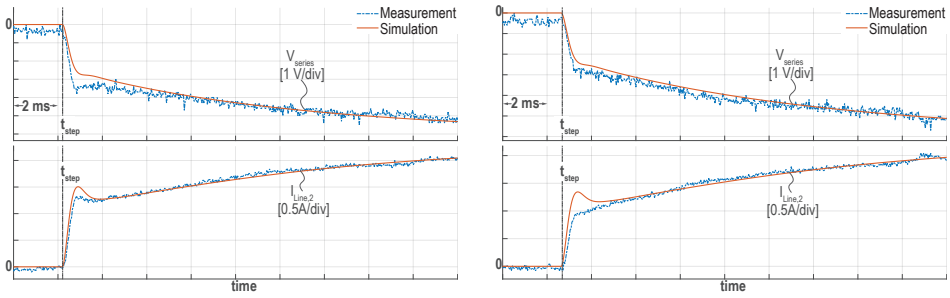


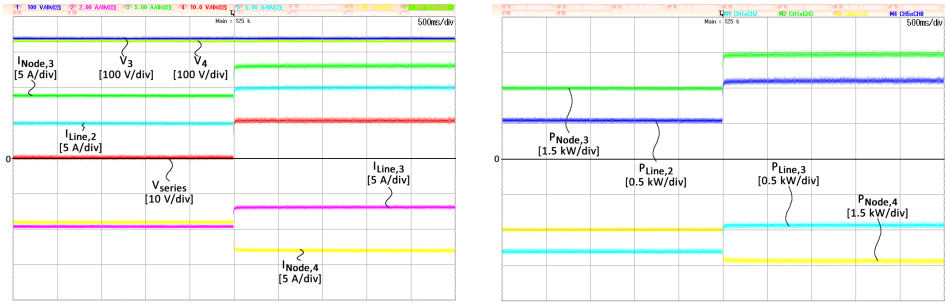
FIGURE 2.10: Large-signal model comparison. The results when the PI parameters of the unfolder bridge $K_{\text{unf},1} = 1$ p.u. and $K_{\text{unf},2} = 1$ p.u. are in (a). The results the PI parameters of the unfolder bridge $K_{\text{unf},1} = 0.8$ p.u. and $K_{\text{unf},2} = 0.8$ p.u. are in (b). In both cases the series voltage and current flowing in out of the PFCC (in line 2) are compared.

Figure 2.10 shows a comparison between the prototype and the simulation reacting to the step change in the V^*_{series} value from 0 V to 5 V at time instance t_{step}. The experiment and simulation were repeated with different PI controller values for the unfolder bridge control loop. The faster controller is shown in Fig. 2.10a. The controller with the coefficients reduced by one fourth is shown in Fig. 2.10b. Overall, the match between the simulation and the measurement in Fig. 2.10 is excellent. Figure 2.10a and Fig. 2.10b show only small variations in the peak values during transients. The models obtained with the generalized averaging method are known to be precise up to one-third of the switching frequency [62]. The slight difference between the measured current and simulated current can be attributed to the fact that the line inductance influences the current dynamics as was studied in the previous section. Secondly, the differences partially arise from the measurement method itself. The current was measured with a clamp-on probe, for which the repeatability error up to 100 mA is common [71].

The small differences in voltage comparison can, besides the error stemming from repeatability of the measurement, be attributed to the fact that the equivalent series resistance of the capacitor is not modeled [62] and slight variations of the output capacitance. The output capacitor is made of parallel connected ceramic capacitors, which capacitance is dependent on voltage, frequency, and temperature. Lastly, the Delta Elektronika output capacitance and their internal control parameters are virtually unknown, and it is reasonable to assume that there is a small discrepancy due to these differences.

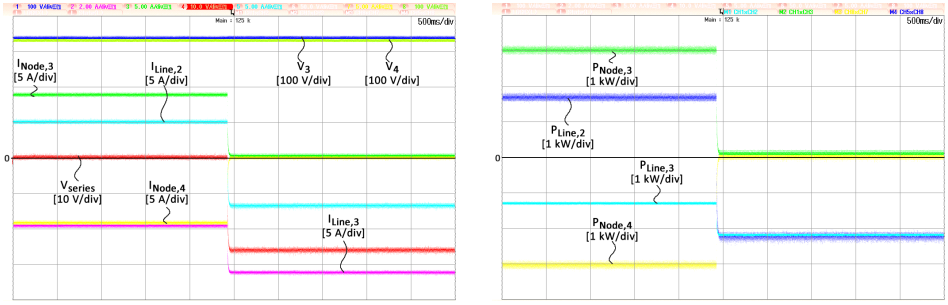
In summary, the match between the measurements and simulation in Fig. 2.9a and in Fig. 2.9b give confidence in the models presented in Section 2. The comparison exhibits only small discrepancies of the peak values during transients, which can have several origins due to the complexity of the measured system.

2.4.2 *Test in Meshed Grid*



(a) (b)

FIGURE 2.11: Operation of the pfcc in a meshed microgrid demonstrating step-up of the power flow in the grid. In (a) are the voltages and currents of the microgrid while (b) shows the powers.

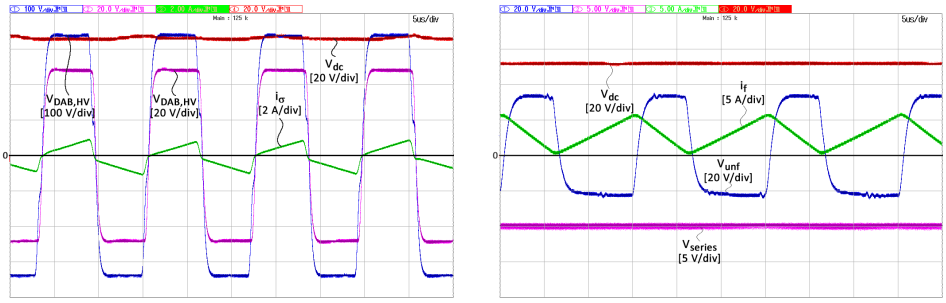


(a) (b)

FIGURE 2.12: Operation of the pfcc in a meshed microgrid demonstrating step-down of the power flow in the grid. (a) shows the voltages and currents of the microgrid while (b) shows the powers.

The experiment in this section will demonstrate the functionality of the PFCC in the laboratory-scale microgrid. The schematic from Fig. 2.6 is recreated in the laboratory. During the experiment one power supply is programmed with initial voltage V_3 of 350 V while the second power supply is programmed with an initial voltage V_4 of 335 V. Contrary to the simulation, the Delta Elektronika power supplies do not behave as ideal constant power loads or sources. Therefore, some change in the operation can be observed. Nevertheless, they do allow to study the dynamics of the modeled PFCC and demonstrate its functionality.

In Fig. 2.11, Fig. 2.12, Fig. 2.13 are the voltages and the currents flowing in the laboratory microgrid and inside the PFCC during the experiment. The experiment is separated in two main steps. First, the power flow in the grid is increased by the PFCC. In Fig. 2.11a the currents and voltages are shown while in Fig. 2.11b the powers



(a) (b)

FIGURE 2.13: Operational waveforms of the dab and unfolder bridge are shown in (a) and (b) respectively.

during the increase of the power flow are depicted. The power supplied by source one during this experiment is 4.5 kW. From Fig. 2.11a it is observable that the injected voltage V_{series} is 10 V, while the current flowing out of the PFCC $I_{\text{Line},2}$ is 10 A. This implies that the power processed by the PFCC is around 100 W. Figure 2.11b explicitly shows that after injection of the series voltage, the power supplied by source one is increased by 1500 W. Clearly, the PFCC is capable of controlling significant power flow while processing only a fraction of the total system power.

The power supplied to the grid is 45 times higher than the power processed by the PFCC prototype. The difference in power flow in line 2 after the PFCC injects 10 V is 15 times higher than the power processed by the PFCC prototype. These ratios show that partially rated PFCC can control grid power flow in a wide range. It is likely that the PFCC will operate below its nominal power rating for a significant part of its service life. Therefore, it is advantageous to employ a DAB which can achieve a flat efficiency curve across a wide power range.

In the second experiment, the PFCC reduces the circulating power. The currents and voltages are shown in Fig. 2.12a and the powers are depicted in Fig. 2.12b. It is notable that the current flowing in line 2 $I_{\text{Line},2}$ is reversed during this experiment.

The measurement section is completed with the operating waveforms of the DAB, and the unfolder bridge which are provided in Fig. 2.13a and Fig. 2.13b respectively.

2.5 CONCLUDING REMARKS

The chapter presents the derivation of the large- and small-signal models of the partially rated power flow control converter (PFCC) coupled with the low voltage direct current (LVDC) distribution grid model. The PFCC model can be easily combined with the LVDC grid model and allows for fast algorithmization and easy simulation of the LVDC systems based on the decentralized power generation with the power flow controlled by the PFCC. Using the derived PFCC small-signal model a simple controller was designed, in which specifics of the chosen topology were considered. The PFCC large-signal model was coupled with the LVDC network model to study the power flow control with a partially rated converter. The small-signal model was validated

by measuring the control-to-output transfer functions. PFCC large-signal model with dc grid model was validated via time-domain measurements. The experiments also demonstrated the functionality of the PFCC in a LVDC grid. The proposed continuous full-order models are insightful and allow for controller design which takes into account the characteristics of the LVDC network, as well as the peculiarities of the PFCC operation.

Due to the nature of the multi-terminal LVDC grids the power flows are coupled. Therefore, tools to study modeling and control of the power flows are necessary to further the applicability of the LVDC for the electric energy distribution. The effects of the PFCC on the LVDC grid dynamics and the effects of the LVDC grid dynamics on the PFCC can be easily studied with the presented models. Furthermore, the models can be used for the design of novel power flow control algorithms based on a partially rated power flow control converter, which can further increase the appeal of multi-terminal LVDC grids. The models can serve as a basis for studying truly decentralized grid topologies that allow for the integration of microgrids with significant numbers of cheap and efficient power flow control units.

Part II

CONTROL

3

DECOUPLING CONTROL FOR POWER FLOW CONTROL CONVERTER IN BIPOLAR LVDC GRIDS

In this chapter first the potential of multi-port topologies to facilitate different functions in LVDC distribution system is discussed. The triple active bridge (TAB) converter is chosen from the multi-port topologies to implement power flow control in bipolar LVDC grids. In this chapter a decoupling controller for the triple active bridge converter is proposed. The controller is based on a full-order continuous-time model of the TAB converter derived using the generalized average modelling (GAM) technique. GAM uses the Fourier series expansion to decompose the state-space variables into two components, which represent the active power and the reactive power. The controller uses the active power components of the transformer currents to decouple the active power flows between converter ports. The decoupling performance of the proposed controller is validated in a hardware experiment.

This chapter is based on:

C3 P. Purgat, S. Bandyopadhyay, Z. Qin, P. Bauer-*"Power Flow Decoupling Controller for Triple Active Bridge Based on Fourier Decomposition of Transformer Currents", 2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*

C4 P. Purgat, S. Bandyopadhyay, Z. Qin, P. Bauer-*"Continuous Full Order Model of Triple Active Bridge Converter",2019 21st European Conference on Power Electronics and Applications (EPE)*

C5 P. Purgat, L. Mackay, M. Schulz, Y. Han, L. Ramirez-Elizondo, M. März, P. Bauer-*"Design of a Power Flow Control Converter for Bipolar Meshed LVDC Distribution Grids",2018 IEEE 18th International Power Electronics and Motion Control Conference (PEMC)*

3.1 INTRODUCTION

Previous chapter identified a solution to efficiently control power flow and extend the power capacity of a meshed LVDC system. The power flow control converter (PFCC) proposed in Chapter2 can be used in bipolar networks as well. However, if a multi-port topology is used several passive and active components can be saved. The proposed partially rated power flow control converter for bipolar LVDC is in Fig. 3.1. The converter consists of the triple active bridge (TAB) and two unfolding bridges. The TAB is connected on the primary side between the positive and negative pole of the bipolar network. Therefore, the voltage on the primary side of the triple active bridge is two times the nominal grid voltage. The two outputs on the secondary side of the TAB are connected to the unfolding bridges. The role of the unfolding bridges is to keep the voltage on the TAB DC links always positive and help to increase the flexibility of the PFCC. The unfolding bridges are connected through an LC filter to the line of the network. The unfolding bridges are connected such that they insert a series voltage in the network as is demonstrated in Fig. 3.1. The figure also illustrates how the partial rating is achieved. Primary side of the PFCC is connected to double the grid voltage. However, only a fraction of the grid current flows in. On the secondary side of the transformer, full grid current flows. However, the operating voltage is only a fraction of the grid nominal voltage.

PFCC shown in Fig. 3.1 can control the power flow and limit the currents as its counterpart that was presented in the previous chapter. The use of TAB is only an expansion of the application, and the underlying operational concepts are the same. A natural question arises when the proposed converter is used in bipolar grids, whether it is capable to control load unbalances between the phases. The most critical unbalance is when one phase is fully loaded while the other phase is unloaded. Clearly, due to the partial power rating the proposed PFCC is not suited for grid balancing. The PFCC can only deal with unbalances that are as high as its power rating.

In recent years, TAB converters have gained research attention as a potential solution for versatile energy management systems able to integrate diverse renewable energy sources or conventional energy sources, storage systems, and loads [72]. The main advantages of TABs include lower component count compared to standalone converters, higher efficiency, the possibility of centralized control, and potentially higher power density. Potential applications for the TABs range from electric vehicles [73], more-electric aircrafts [74,75] to smart grids [76].

The primary purpose of multi-port converters is to integrate multiple sources, storages, and loads with varied voltage and current ratings into a single power stage allowing bi-directional power flow between each port. Apart from bi-directional power flow, specific applications like EV charging also require galvanic isolation between the different ports for safety reasons [77]. Hence, a multi-winding high-frequency (HF) transformer is used. The TAB converter belongs to a larger family of multi-port converters. Its name arises from three inverter bridges (half-bridge or full-bridge), which are connected via a high frequency (HF) multi-winding transformer [77,78]. Derived from the dual-active bridge (DAB) converter family [79], the TAB converter not only integrates and exchanges the energy from/to all ports, but also provides full

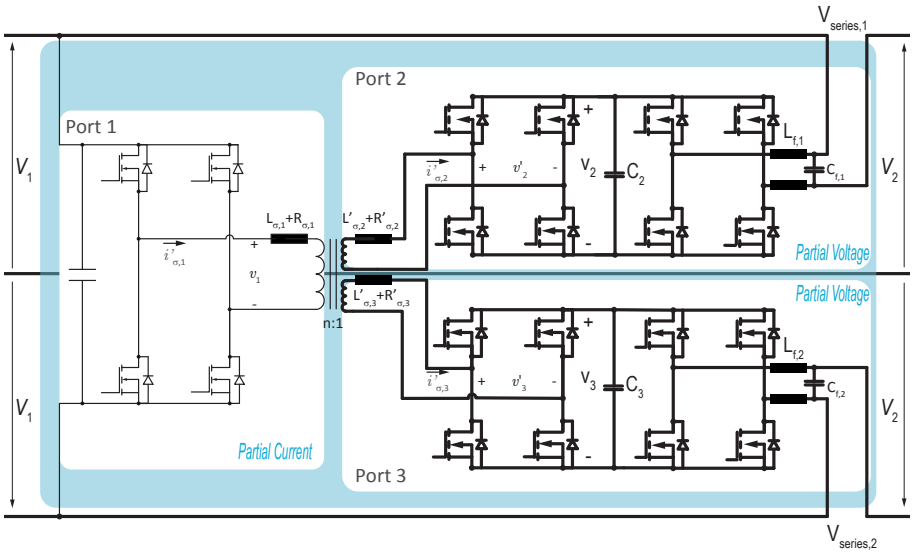


FIGURE 3.1: Triple active bridge converter connected as partailly rated power flow controller for bipolar LVDC.

isolation among all ports and matches the different port voltage levels. Additionally, the TAB converter can operate with soft-switching conditions across a broad operating range [80].

3.1.1 *TAB Operation Challenges*

A key challenge of TAB converter design and control is the inherent cross-coupling of the power flows between the ports due to the multi-winding transformer. Therefore, the TAB converter behaves as a multi-input multi-output (MIMO) system with coupled control loops. In literature, three control techniques to decouple the power flows are reported. A feedforward compensator based control method is proposed in [81], which decouples the control loops dynamically with pre-calculated gains stored as a look-up table in the controller. This approach is improved with feedforward control in [82] or reformulated using conjugated variables in [83]. Another control technique decouples the control loops by choosing different bandwidths for the single-input single-output (SISO) loops [84]. Therefore, the loop with the highest bandwidth determines the phase-shift direction during transients and acts as the slack bus. Recently, a time-sharing control is reported in [78], which decouples the power flows by operating the MAB converter as a DAB converter with only two active ports and other ports deactivated as diode rectifiers at any particular period. Currently, all approaches to decouple the control variables are based on the first order simplified model [85, 86].

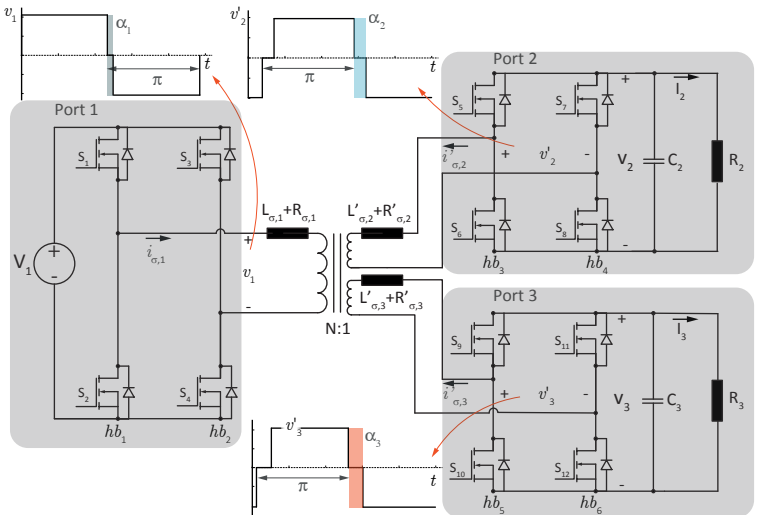


FIGURE 3.2: Triple active bridge converter.

3.1.2 *Contribution*

The main contributions of this chapter are the derivation and the experimental verification of the small-signal model and the active power decoupling controller for the phase-shifted TAB. The controller is derived, and its implementation in the digital domain is proposed. The proposed controller is validated by an experimental study on a TAB laboratory prototype.

The rest of this chapter is organized as follows. Section 2 recapitulates GAM and explains the state-space model of the TAB converter. In section 3, the active current based decoupling controller is proposed. The implementation of the proposed controller in the digital domain is explained in section 4. Section 4 further provides experimental verification of the proposed controller. Section 5 summarizes the chapter and provides an outlook on the application.

3.2 OPERATION & MODELLING PRINCIPLES

Triple active bridge (TAB) converter is derived from the dual active bridge (DAB) converter family. Figure 3.2 shows the schematic of the TAB converter. The TAB converter consists of three ac generating cells connected to a transformer with three windings. The power is transferred across the leakage inductances that can be inserted as separate components, or the transformer leakage inductances can be used. The zero-voltage switching (ZVS) is achieved utilizing the parasitic capacitance of full bridges MOSFETs.

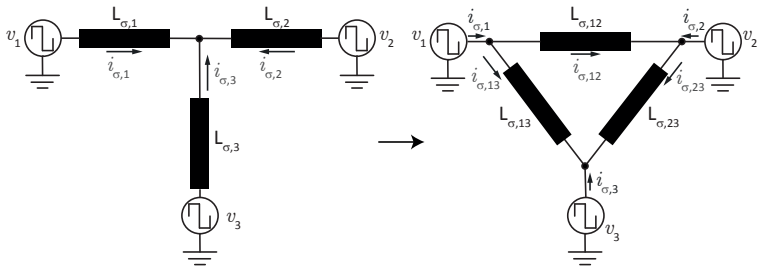


FIGURE 3.3: Simplified schematic of TAB in star and delta connection.

The equation derived for the DAB cycle-by-cycle average (CCA) power in [79] can be extended to a TAB converter. Thus, the CCA power transferred (P_{ij}) from port j into port k of a TAB converter is given by

$$P_{ij} = \frac{V_i^{'} V_j^{'}}{2\pi f_s L_{\sigma,ij}} \varphi_{ij} \left(1 - \frac{|\varphi_{ij}|}{\pi}\right), \qquad \varphi_{ij} = \varphi_i - \varphi_j, \tag{3.1}$$

where $L_{\sigma,ij}$ is the equivalent inductance between ports i and j, φ_i and φ_j are the corresponding phase shift angles, $V_i^{'}$ and $V_j^{'}$ are the corresponding dc port voltages. Therefore, the power flow at each port of TAB converter can be controlled in three ways: (a) phase-shift (φ_{ij}) control between the full bridges, (b) duty-cycle control of the full bridges, and (c) switching frequency (f_s) control. This chapter focuses only on the phase shift control. For the phase-shift control, the duty cycle on the full bridges is kept at 50%, and the power transfer is controlled by the phase shifts between the full bridges. To analyze the power transfer between the ports, the equivalent inductance between the ports needs to computed/estimated. Therefore, it is beneficial to convert the schematic in Fig. 3.2 into a delta equivalent circuit.

The transformation from star to delta equivalent circuit of the TAB converter is shown in Fig. 3.3. The transformer is described as a Δ connection. The current waveforms of the converter are shown in Fig. 3.3. As was done in [77], the link inductances in Δ connection can be computed based on the individual leakage inductances of the transformer windings

$$L_{\sigma,12} = L_{\sigma,1} + N^2 L_{\sigma,2} + \frac{L_{\sigma,1} L_{\sigma,2}}{L_{\sigma,3}}, \tag{3.2}$$

$$L_{\sigma,13} = L_{\sigma,1} + N^2 L_{\sigma,3} + \frac{L_{\sigma,1} L_{\sigma,3}}{L_{\sigma,2}}, \tag{3.3}$$

$$L_{\sigma,32} = N^2 L_{\sigma,3} + N^2 L_{\sigma,2} + N^4 \frac{L_{\sigma,3} L_{\sigma,2}}{L_{\sigma,1}}, \tag{3.4}$$

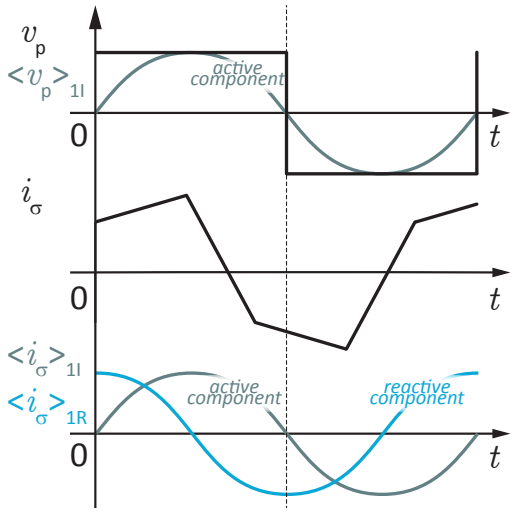


FIGURE 3.4: Active and circulating power components.

where N is the transformer ratio and $L_{\sigma,1}$, $L_{\sigma,2}$ and $L_{\sigma,3}$ are the transformer leakage inductances and the transformer ratio is accounted as $L'_{\sigma,2} = N^2 L_{\sigma,2}$ and $L'_{\sigma,3} = N^2 L_{\sigma,3}$. Similarly, the transformer currents of the TAB converter after transformation are

$$i_{\sigma,1} = -i_{\sigma,12} - i_{\sigma,13}, \tag{3.5}$$
$$i'_{\sigma,2} = i_{\sigma,12} - i_{\sigma,23}, \tag{3.6}$$
$$i'_{\sigma,3} = i_{\sigma,13} + i_{\sigma,23}, \tag{3.7}$$

where $i_{\sigma,1}$ is the primary side transformer current and $i'_{\sigma,2}$ and $i'_{\sigma,3}$ are the secondary side transformer currents. The transformer ratio is accounted as $i'_{\sigma,2} = N i_{\sigma,2}$ and $i'_{\sigma,3} = N i_{\sigma,3}$.

3.2.1 *Generalized Average Modelling - Control Perspective*

The generalized averaging method (GAM) was derived in [67], motivated by the switching circuits that did not fulfill the small-ripple condition. MPC that are derived from DAB fall into this category; therefore, when the transformer harmonics are to be captured, GAM must be applied. The generalized averaging method was applied to the DAB in [62]. GAM is based on the fact that any waveform $x(t)$ can be represented to arbitrary accuracy by a Fourier series on a given interval $t - T_s \leq \tau < t$. For periodic signals, this property can be represented as

$$x(\tau) = \sum_{l=-\infty}^{\infty} \langle x \rangle_l (t) e^{-jl\omega_s \tau}, \tag{3.8}$$

where $\omega_s = 2\pi f_s$, the sum is over all integers l and $\langle x \rangle_l$ is the $l-th$ coefficient of the Fourier series. These coefficients are functions of time and can be expressed as

$$\begin{aligned}\langle x \rangle_l(t) &= \frac{1}{T}\int_{t-T+s}^{t} x(\tau)e^{-jl\omega_s\tau}\mathrm{d}\tau \\ &= \frac{1}{T}\int_{t-T+s}^{t} x(\tau)\cos(l\omega_s\tau)\mathrm{d}\tau \\ &- \frac{j}{T}\int_{t-T+s}^{t} x(\tau)\sin(l\omega_s\tau)\mathrm{d}\tau.\end{aligned} \tag{3.9}$$

In eq. (3.9) the *sine* component is in phase with the ac voltage and it is the active power component while the *cosine* component represents the reactive power as shown in Fig. 3.4. This convention is adopted here to keep the derived equations in line with the preceding works [62, 67, 87].

3.2.2 *Large-signal Model*

The equations describing the operation of TAB converter using delta convention shown in Fig.3.3 are

$$C_2\frac{\mathrm{d}}{\mathrm{d}\tau}v_2(\tau) = -\frac{v_2(\tau)}{R_2} + s_2(\tau)i'_{\sigma,2}(\tau), \tag{3.10}$$

$$C_3\frac{\mathrm{d}}{\mathrm{d}\tau}v_3(\tau) = -\frac{v_3(\tau)}{R_3} + s_3(\tau)i'_{\sigma,3}(\tau), \tag{3.11}$$

$$L_{\sigma,12}\frac{\mathrm{d}}{\mathrm{d}\tau}i_{\sigma,12}(\tau) = -R_{\sigma,12}i_{\sigma,12}(\tau) + v_1(\tau) - v'_2(\tau), \tag{3.12}$$

$$L_{\sigma,13}\frac{\mathrm{d}}{\mathrm{d}\tau}i_{\sigma,13}(\tau) = -R_{\sigma,13}i_{\sigma,13}(\tau) + v_1(\tau) - v'_3(\tau), \tag{3.13}$$

$$L_{\sigma,23}\frac{\mathrm{d}}{\mathrm{d}\tau}i_{\sigma,23}(\tau) = -R_{\sigma,23}i_{\sigma,23}(\tau) + v'_2(\tau) - v'_3(\tau), \tag{3.14}$$

where C_2, C_3 are the output capacitances, R_2 and R_3 are the output resistances and $R_{\sigma,12}$, $R_{\sigma,13}$ and $R_{\sigma,23}$ are the parasitic resistances in the delta type equivalent circuit of the TAB, transformed the same way as the leakage inductances.

In (3.10)(3.14), it is assumed that the transformer magnetization current is insignificant. Further, the MOSFET switching transients are neglected as well as the voltage drop across the MOSFET body diode. The input capacitance is coupled in the ideal voltage source V_1, and the reason is twofold. First, the input capacitance is normally large enough to minimize any voltage ripple. Secondly, in most applications, it is desired to control the voltages on the secondary side of the converter; therefore, output capacitors C_2 and C_3 and their respective dynamics are modeled. The parasitic resistances $R_{\sigma,12}$, $R_{\sigma,13}$ and $R_{\sigma,23}$ represent both the ohmic losses in the magnetic circuit as well as in the semiconductors. The large-signal model can be derived by applying GAM (3.9) on the converter model in (3.10)-(3.14). Further, it is assumed that the dynamics of the input voltage source and the voltages on the output capacitors C_2 and C_3 are much slower than that of the TAB transformer. Therefore the capacitor voltages $V_2(\tau)$ and $V_3(\tau)$ are

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} V_2 \\ V_3 \\ i_{\sigma,12R} \\ i_{\sigma,12I} \\ i_{\sigma,13R} \\ i_{\sigma,13I} \\ i_{\sigma,23R} \\ i_{\sigma,23I} \end{bmatrix} = \begin{bmatrix} \frac{-1}{R_2C_2} & 0 & \frac{-4N\sin(d_1\pi)}{\pi C_2} & \frac{-4N\cos(d_1\pi)}{\pi C_2} & 0 \\ 0 & \frac{-1}{R_3C_3} & 0 & 0 & \frac{-4N\sin(d_2\pi)}{\pi C_3} \\ \frac{2N\sin(d\pi)}{\pi L_{\sigma,12}} & 0 & \frac{-R_{\sigma,12}}{L_{\sigma,12}} & \omega_s & 0 \\ \frac{2N\cos(d\pi)}{\pi L_{\sigma,12}} & 0 & -\omega_s & \frac{-R_{\sigma,12}}{L_{\sigma,12}} & 0 \\ 0 & \frac{2N\sin(d_2\pi)}{\pi L_{\sigma,13}} & 0 & 0 & \frac{-R_{\sigma,13}}{L_{\sigma,13}} \\ 0 & \frac{2N\cos(d_2\pi)}{\pi L_{\sigma,13}} & 0 & 0 & -\omega_s \\ \frac{2N\sin(d_1\pi)}{\pi L_{\sigma,23}} & \frac{-2N\sin(d_2\pi)}{\pi L_{\sigma,23}} & 0 & 0 & 0 \\ \frac{-2N\cos(d_1\pi)}{\pi L_{\sigma,23}} & \frac{2N\cos(d_2\pi)}{\pi L_{\sigma,23}} & 0 & 0 & 0 \end{bmatrix} \times \begin{bmatrix} V_2 \\ V_3 \\ i_{\sigma,12R} \\ i_{\sigma,12I} \\ i_{\sigma,13R} \\ i_{\sigma,13I} \\ i_{\sigma,23R} \\ i_{\sigma,23I} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ \frac{-2}{\pi L_{\sigma,12}} \\ 0 \\ \frac{-2}{\pi L_{\sigma,13}} \\ 0 \\ 0 \end{bmatrix} \left[V_{\text{in}}\right] \begin{bmatrix} 0 & \frac{4N\sin(d_1\pi)}{\pi C_2} & \frac{4N\cos(d_1\pi)}{\pi C_2} \\ \frac{-4N\cos(d_2\pi)}{\pi C_3} & -\frac{4N\sin(d_2\pi)}{\pi C_3} & -\frac{4N\cos(d_2\pi)}{\pi C_3} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ \omega_s & 0 & 0 \\ \frac{-R_{\sigma,13}}{L_{\sigma,13}} & 0 & 0 \\ 0 & \frac{-R_{\sigma,23}}{L_{\sigma,23}} & \omega_s \\ 0 & -\omega_s & \frac{-R_{\sigma,23}}{L_{\sigma,23}} \end{bmatrix} \tag{3.15}$$

described only by the zero-order component of the Fourier series, while the inductor currents are described with the fundamental component i.e., the switching frequency component.

The generalized averaging method will not be applied explicitly here to eq. (3.10)-(3.14) as modeling is not the primary goal of this chapter. However, the generalized averaging method was explicitly applied to TAB equations in [88]. The large-signal model of the TAB can be written in the state-space form, as shown in eq. (3.15).

3.2.3 *Small-signal Model*

To derive the small-signal average model of the converter, we first define the small-signal deviations as $\Delta d_1 = d_1 - D_1, \Delta d_2 = d_2 - D_2, \Delta v_{\text{out},1} = v_{\text{out},1} - V_{\text{out},1}, \Delta v_{\text{out},2} = v_{\text{out},2} - V_{\text{out},2}, \Delta i_{\sigma,12R} = i_{\sigma,12R} - I_{\sigma,12R}, \Delta i_{\sigma,12I} = i_{\sigma,12I} - I_{\sigma,12I}, \Delta i_{\sigma,13R} = i_{\sigma,13R} - I_{\sigma,13R}, \Delta i_{\sigma,13I} = i_{\sigma,13I} - I_{\sigma,13I}, \Delta i_{\sigma,23R} = i_{\sigma,23R} - I_{\sigma,23R}, \Delta i_{\sigma,23I} = i_{\sigma,23I} - I_{\sigma,23I}$. where Δ defines the small-signal state, the upper case letters represent the dc terms and the lower case letters the large-signal states.

Equation (3.15) contains nonlinear terms such as multiplication of the control input and state variables. For small δd_1, the nonlinear term can be written as

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix}\Delta v_{\mathrm{out},1}\\ \Delta v_{\mathrm{out},2}\\ \Delta i_{\sigma,12R}\\ \Delta i_{\sigma,12I}\\ \Delta i_{\sigma,13R}\\ \Delta i_{\sigma,13I}\\ \Delta i_{\sigma,23R}\\ \Delta i_{\sigma,23I}\end{bmatrix} = \begin{bmatrix} \frac{-1}{R_{\mathrm{out},1}C_{\mathrm{out},1}} & 0 & \frac{-4n\sin(D_1\pi)}{\pi C_{\mathrm{out},1}} & \frac{-4n\cos(D_1\pi)}{\pi C_{\mathrm{out},1}} & 0 \\ 0 & \frac{-1}{R_{\mathrm{out},2}C_{\mathrm{out},2}} & 0 & 0 & \frac{-4n\sin(D_2\pi)}{\pi C_{\mathrm{out},2}} \\ \frac{2n\sin(D_1\pi)}{\pi L_{\sigma,12}} & 0 & \frac{-R_\sigma}{L_{\sigma,12}} & \omega & 0 \\ \frac{2n\cos(D_1\pi)}{\pi L_{\sigma,12}} & 0 & -\omega & \frac{-R_\sigma}{L_{\sigma,12}} & 0 \\ 0 & \frac{2n\sin(D_2\pi)}{\pi L_{\sigma,13}} & 0 & 0 & \frac{-R_\sigma}{L_{\sigma,13}} \\ 0 & \frac{2n\cos(D_2\pi)}{\pi L_{\sigma,13}} & 0 & 0 & -\omega \\ \frac{2n\sin(D_1\pi)}{\pi L_{\sigma,23}} & \frac{-2n\sin(D_2\pi)}{\pi L_{\sigma,23}} & 0 & 0 & \\ \frac{-2n\cos(D_1\pi)}{\pi L_{\sigma,23}} & \frac{2n\cos(D_2\pi)}{\pi L_{\sigma,23}} & 0 & 0 & \end{bmatrix}$$

$$\begin{bmatrix} 0 & \frac{4n\sin(D_1\pi)}{\pi C_{\mathrm{out},1}} & \frac{4n\cos(D_1\pi)}{\pi C_{\mathrm{out},1}} & \\ \frac{-4n\cos(D_2\pi)}{\pi C_{\mathrm{out},2}} & \frac{4n\sin(D_2\pi)}{\pi C_{\mathrm{out},2}} & \frac{4n\cos(D_2\pi)}{\pi C_{\mathrm{out},2}} & \\ 0 & 0 & 0 & \\ 0 & 0 & 0 & \\ \omega & 0 & 0 & \\ \frac{-R_\sigma}{L_{\sigma,13}} & 0 & 0 & \\ 0 & 0 & \frac{-R_\sigma}{L_{\sigma,23}} & \omega \\ 0 & 0 & -\omega & \frac{-R_\sigma}{L_{\sigma,23}} \end{bmatrix} \times \begin{bmatrix}\Delta v_{\mathrm{out},1}\\ \Delta v_{\mathrm{out},2}\\ \Delta i_{\sigma,12R}\\ \Delta i_{\sigma,12I}\\ \Delta i_{\sigma,13R}\\ \Delta i_{\sigma,13I}\\ \Delta i_{\sigma,23R}\\ \Delta i_{\sigma,23I}\end{bmatrix}$$

$$+ \begin{bmatrix} 0 & -4n\left[I_{3R,0}\cos\left(\pi D_2\right) - I_{3I,0}\sin\left(\pi D_2\right)\right] \\ 2nV_{\mathrm{out},1,0}\cos\left(\pi D_1\right) & 0 \\ -2nV_{\mathrm{out},1,0}\sin\left(\pi D_1\right) & 0 \\ 0 & 2nV_{\mathrm{out},2,0}\cos\left(\pi D_2\right) \\ 0 & -2nV_{\mathrm{out},2,0}\sin\left(\pi D_2\right) \\ 2nV_{\mathrm{out},1,0}\cos\left(\pi D_1\right) & -2nV_{\mathrm{out},2,0}\cos\left(\pi D_2\right) \\ -2nV_{\mathrm{out},1,0}\sin\left(\pi D_1\right) & -2nV_{\mathrm{out},2,0}\sin\left(\pi D_2\right) \end{bmatrix} \begin{bmatrix}\Delta d_1\\ \Delta d_2\end{bmatrix}. \tag{3.17}$$

$$\sin(\pi d_1)v_{\mathrm{out},1_0} = \sin(\pi D_1)\Delta v_{\mathrm{out},1_0} + V_{\mathrm{out},1_0}\sin(\pi D_1) + V_{\mathrm{out},1_0}\cos(\pi D_1)(\pi D_1). \tag{3.16}$$

The small signal model of the TAB converter is written in eq. (3.17).

3.3 DECOUPLING CONTROLLER

The instantaneous powers of the converter ports connected in delta convention shown in Fig. 3.3 can be written as

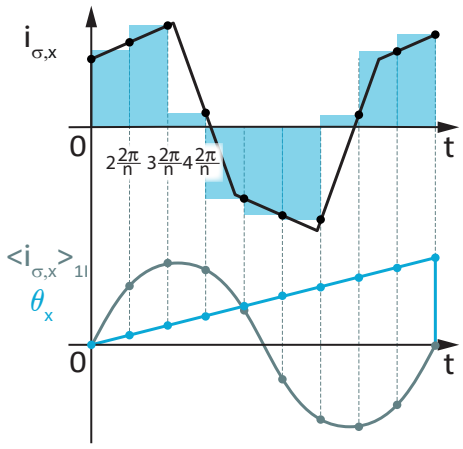


FIGURE 3.5: Extraction of the active component of the measured variable in discrete time.

$$\begin{aligned}\left\langle P_{\mathrm{p},1}\right\rangle_{1I}(t) &= \left\langle v_1\right\rangle_{1I}(t)\left\langle i_{\sigma,1}\right\rangle_{1I}(t)\\ &= \left\langle v_1\right\rangle_{1I}(t)\left(\left\langle i_{\sigma,12}\right\rangle_{1I}(t)+\left\langle i_{\sigma,13}\right\rangle_{1I}(t)\right),\end{aligned} \tag{3.18}$$

$$\begin{aligned}\left\langle P_{\mathrm{p},2}\right\rangle_{1I}(t) &= \left\langle v_2\right\rangle_{1I}(t)\left\langle i_{\sigma,2}\right\rangle_{1I}(t)\\ &= \left\langle v_2\right\rangle_{1I}(t)\left(-\left\langle i_{\sigma,12}\right\rangle_{1I}(t)+\left\langle i_{\sigma,23}\right\rangle_{1I}(t)\right),\end{aligned} \tag{3.19}$$

$$\begin{aligned}\left\langle P_{\mathrm{p},3}\right\rangle_{1I}(t) &= \left\langle v_3\right\rangle_{1I}(t)\left\langle i_{\sigma,3}\right\rangle_{1I}(t)\\ &= \left\langle v_3\right\rangle_{1I}(t)\left(-\left\langle i_{\sigma,13}\right\rangle_{1I}(t)-\left\langle i_{\sigma,23}\right\rangle_{1I}(t)\right),\end{aligned} \tag{3.20}$$

where $\langle x\rangle_{1I}(t)$ is the first coefficient in the Fourier series representing active power as shown in Fig. 3.4.

It is clear from eq. (3.20) that the port powers of TAB can be decoupled by compensating for the influence of the current $\langle i_{\sigma,23}\rangle_{1I}$ in the control loops of the ports two and three. In [87], a controller for DAB was proposed that uses the active power component of the transformer current. In [87] it was shown that using the active power component reduces the transient DC component, thereby reduces the peak flux density. The controller proposed in this work uses the active power components of the transformer currents extracted from the raw data and calculated in a DSP.

3.3.1 *Active Current Component Extraction*

In the derivation of the extraction of the active current component, it is assumed that the signals are periodic. The Fourier series coefficient corresponding to the active component in the time domain can be written as

$$\langle x\rangle_k(t) = -\frac{1}{T_s}\int_{T_s} x(\tau)\sin(k\omega_s\tau)\mathrm{d}\tau. \tag{3.21}$$

The extraction of the active component is measured periodically n times across the switching period T_s. The integration is substituted by dividing the integration to intervals with defined length of $k\frac{T_s}{n}$. In period $\frac{T_s}{n} \leq \tau < (k+1)\frac{T_s}{n}$, the integrand $x(\tau)\sin(k\omega_s\tau)$ is approximated by $\tau = k\frac{T_s}{n}$ which means

$$x\left(k\frac{T_s}{n}\right)\sin\left(\frac{2\pi}{T_s}k\frac{T_s}{n}\right) = x\left(k\frac{T_s}{n}\right)\sin\left(\frac{2\pi}{n}k\right).$$

Therefore the integration over the specified period is approximated by the area of the rectangle with the height of $x\left(k\frac{T_s}{n}\right)\sin\left(\frac{2\pi}{n}k\right)$ and width of $\frac{T_s}{n}$. When the rectangle area is substituted to (3.21) then the discrete approximation can be written as

$$\langle x\rangle_k(t) \approx \langle x\rangle_k^{(n)} = -\frac{1}{T_s}\sum_{k=0}^{n-1}\frac{T_s}{n}x\left(\frac{T_s}{n}k\right)\sin\left(\frac{2\pi}{n}k\right) = \tag{3.22}$$

$$-\frac{1}{n}\sum_{k=0}^{n-1}x\left(\frac{T_s}{n}k\right)\sin\left(\frac{2\pi}{n}k\right). \tag{3.23}$$

Equation (3.23) can be rewritten in the form corresponding with the one shown in [87] if the PWM carrier period $\theta_x = \frac{2\pi}{T_s}$ and $x[n-k] = x\left(\frac{T_s}{n}k\right)$, then it can be written

$$\langle i_{\sigma,x}\rangle_{1I}[n] = -\frac{1}{n}\sum_{k=0}^{n-1}\left(i_{\sigma,x}\left[n-k\right]\sin\left(\theta_x\left[n-k\right]\right)\right), \tag{3.24}$$

where the x in θ_x and $i_{\sigma,x}$ denotes the number of the corresponding full-bridge in the TAB. This is because the extraction of the fundamental component of the ac currents must be done at a position referred to the corresponding ac port voltage. Therefore, the extraction is synchronized via the reference angle θ_x, which is the carrier wave of the corresponding PWM, i.e., PWM 2 or PWM 3. Equation (3.24) is the complete expression describing the extraction of the active component. The timing diagram of the active power components extraction subroutine is shown in Fig. 3.5.

3.3.2 *Coupling Current Estimation Using Transformer Voltages*

To apply the proposed decoupling control, current $i_{\sigma,23}(t)$ needs to be estimated. The current between the ports two and three is given by the voltage difference across the inductor $L_{\sigma,23}$. When $R_{\sigma,23}$ is assumed to be negligible, (3.14) can be written as

$$L_{\sigma,23}\frac{\mathrm{d}}{\mathrm{d}\tau}i_{\sigma,23}(\tau) = v_2'(\tau) - v_3'(\tau). \tag{3.25}$$

In integral form (5.3) can be written as

$$i_{\sigma,23}(t) = \frac{1}{L_{\sigma,23}}\int_{t_1}^{t_2} v_2'(\tau) - v_3'(\tau)\mathrm{d}\tau. \tag{3.26}$$

Using the trapezoidal rule, (3.26) can be estimated as

$$i_{\sigma,23}(t) = \frac{1}{L_{\sigma,23}} \int_{t_1}^{t_2} v_2'(\tau) - v_3'(\tau) \mathrm{d}\tau \tag{3.27}$$

$$\approx \frac{t_2 - t_1}{2L_{\sigma,23}} \left(v_2'(t_2) - v_3'(t_2) + v_2'(t_1) - v_3'(t_1) \right). \tag{3.28}$$

Equation (3.28) can be rewritten in terms of sampling speed f_n and written as

$$i_{\sigma,23}[n] = \frac{f_n}{2L_{\sigma,23}} \left(\Delta v'[n] + \Delta v'[n-1] \right), \tag{3.29}$$

where $\Delta v'[n] = v_2'(t_2) - v_3'(t_2)$ and $\Delta v'[n-1] = v_2'(t_1) - v_3'(t_1)$. Extraction of the active component can be easily performed combining (3.29) and (3.24) obtaining

$$\langle i_{\sigma,23} \rangle_{1I}^{(\theta_2)}[n] = -\frac{1}{n} \sum_{k=0}^{n-1} i_{\sigma,23}[n-k] \sin\left(\theta_2 [n-k]\right), \tag{3.30}$$

$$\langle i_{\sigma,23} \rangle_{1I}^{(\theta_3)}[n] = -\frac{1}{n} \sum_{k=0}^{n-1} i_{\sigma,23}[n-k] \sin\left(\theta_3 [n-k]\right), \tag{3.31}$$

for port two and port three, respectively. Result of (3.30) and (3.31) can be used as the decoupling current for their respective ports as explained at the beginning of this section and described with (3.19)-(3.20).

3.3.3 *Coupling Current Estimation Using DC Capacitor Voltages*

The disadvantage of the method derived in the previous subsection is the measurement of the high-frequency voltages. These voltages have different potentials, and the measurements must be galvanically isolated. If isolated amplifiers are used to measure these voltages, the induced delays by the measurements are $1\mu s$ to $3\mu s$. These delays can be significant, especially when the phase angles are small.

The large-signal model matrix offers a solution to avoid the measurement of the high-frequency voltages. The equations describing the coupling current $i_{\sigma,23}$ can be rewritten in integral form as

$$\begin{aligned} \langle i_{\sigma,23} \rangle_{1R} = \int_{t_1}^{t_2} & \frac{2n \sin(d_1 \pi) V_2}{\pi L_{\sigma,23}} - \frac{2n \sin(d_2 \pi) V_3}{\pi L_{\sigma,23}} \\ & - \frac{R_{\sigma,23} \langle i_{\sigma,23} \rangle_{1R}}{L_{\sigma,23}} + \omega_s \langle i_{\sigma,23} \rangle_{1I} \quad \mathrm{d}t, \end{aligned} \tag{3.32}$$

$$\begin{aligned} \langle i_{\sigma,23} \rangle_{1I} = \int_{t_1}^{t_2} & -\frac{2n \cos(d_1 \pi) V_2}{\pi L_{\sigma,23}} + \frac{2n \cos(d_2 \pi) V_3}{\pi L_{\sigma,23}} \\ & - \frac{R_{\sigma,23} \langle i_{\sigma,23} \rangle_{1I}}{L_{\sigma,23}} - \omega_s \langle i_{\sigma,23} \rangle_{1R} \quad \mathrm{d}t. \end{aligned} \tag{3.33}$$

Using trapezoidal rule (3.32)-(3.33) can be rewritten for the discrete domain as

$$\begin{aligned}
&\langle i_{\sigma,23}\rangle_{1R}[n] \approx \frac{f_n}{2L_{\sigma,23}}\,(\\
&\frac{2N}{\pi}\left(\sin(d_1[n]\pi)V_2[n] - \sin(d_1[n-1]\pi)V_2[n-1]\right) \\
&-\frac{2N}{\pi}\left(\sin(d_2[n]\pi)V_3[n] - \sin(d_2[n-1]\pi)V_3[n-1]\right) \\
&-R_{\sigma,23}\left(\langle i_{\sigma,23}\rangle_{1R}[n] - \langle i_{\sigma,23}\rangle_{1R}[n-1]\right) \\
&+\frac{\omega_s}{L_{\sigma,23}}\left(\langle i_{\sigma,23}\rangle_{1I}[n] - \langle i_{\sigma,23}\rangle_{1I}[n-1]\right)\Big),
\end{aligned} \tag{3.34}$$

and

$$\begin{aligned}
&\langle i_{\sigma,23}\rangle_{1I}[n] \approx \frac{f_n}{2L_{\sigma,23}}\,(\\
&\frac{2N}{\pi}\left(\cos(d_1[n]\pi)V_2[n] - \cos(d_1[n-1]\pi)V_2[n-1]\right) \\
&-\frac{2N}{\pi}\left(\cos(d_2[n]\pi)V_3[n] - \cos(d_2[n-1]\pi)V_3[n-1]\right) \\
&-R_{\sigma,23}\left(\langle i_{\sigma,23}\rangle_{1I}[n] - \langle i_{\sigma,23}\rangle_{1I}[n-1]\right) \\
&-\frac{\omega_s}{L_{\sigma,23}}\left(\langle i_{\sigma,23}\rangle_{1R}[n] - \langle i_{\sigma,23}\rangle_{1R}[n-1]\right)\Big).
\end{aligned} \tag{3.35}$$

Result of (3.35) can be used as the decoupling current as explain at the beginning of this section and described in equations (3.19)-(3.20).

3.4 IMPLEMENTATION & EXPERIMENT

3.4.1 *Controller Implementation*

The overall structure of the proposed controller and its implementation in the digital domain is shown in Fig. 3.6. The controller is implemented on *TMS320F28379D* digital signal processor (DSP). The used DSP is equipped with an independent 32-bit floating-point math processor referred to as Control Law Accelerator (CLA) [89]. CLA helps with concurrent-loop execution and is capable of reading ADC samples just after ADC finishes reading. Therefore CLA is used to implement time-critical mathematical tasks, i.e., extraction of the active current component. The used DSP is equipped with two CPUs. CPU 1 implements the controller and sends control signals over the inter-processor communication (IPC) link to CPU 2. CPU 2 communicates with the laboratory computer.

The secondary transformer currents and secondary transformer voltages are sampled ten times per switching period. The sampling of currents and voltages is synchronized with the respective PWMs as shown by $(10f_{s,1} + \varphi_x)$ in Fig. 3.6. The ADC signals are scaled and sent via a double buffer to CLA. The double buffer is necessary

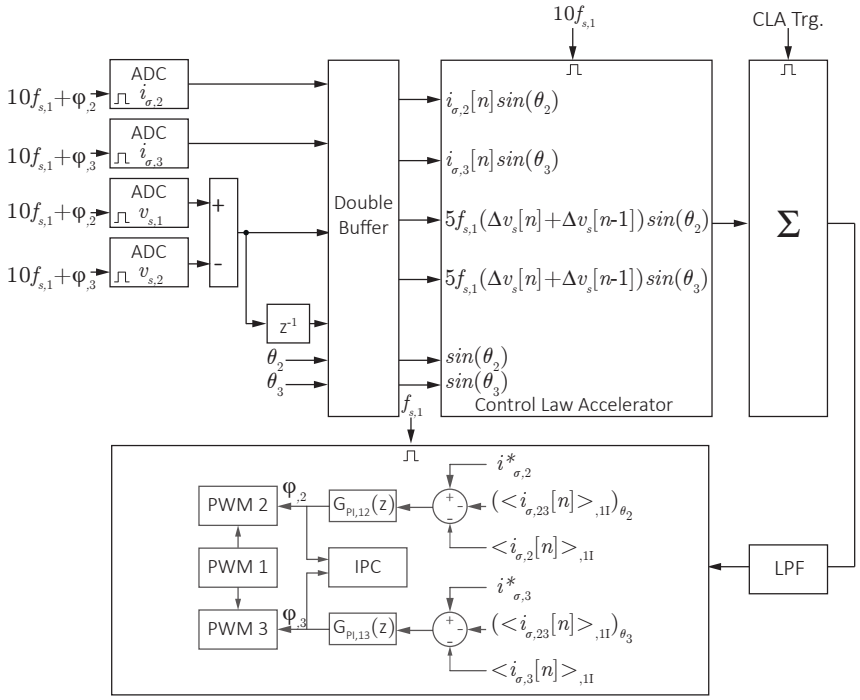


FIGURE 3.6: Proposed implementaion of the decoupling controller in the digital domain.

as the CLA task is executed asynchronously with the CPU clock. The CLA also receives the time base periods θ_2 and θ_3 of PWM 2 and PWM 3. The time base periods of the respective PWMs are used to calculate the corresponding trigonometric functions for active component extraction. Inside the CLA, sines of the two driving periods, θ_2 and θ_3 are calculated as well as the multiplication of different signals, as shown in Fig. 3.4. After completion of each CLA task, a buffer is triggered. The results of the CLA task are read, and the summation of the results is performed once per switching period in a separate task on CPU 1. In every period, a controller subroutine is called. In the controller subroutine, the calculated active components of currents are used to close the loop, and corresponding phase-shifts are calculated with PI controllers. The phase-shifts are communicated via IPC to CPU 2.

3.4.2 *Experiment*

The ADCs measuring currents and voltages are triggered ten times faster than the driving PWMs - PWM1, PWM2, and PWM 3. The ADCs are synchronized with PWM 2, and PWM 3 and correspondingly phase shifted with respect to PWM 1. From the measured raw data, the active power components are extracted as described in Fig. 3.5 and further fed to the PI blocks that regulate the converter operation as shown in Fig. 3.6.

TABLE 3.1: Prototype Parameters

Parameter	Acronym	Value
Transformer ratio	N	7 [-]
Primary Inductance	$L_{\sigma,1}$	70 [μH]
Secondary Inductance	$L_{\sigma,x}$	1.5 [μH]
Output Capacitance	$C_{out,x,x}$	1.22 [mF]
Primary Resistance	$R_{\sigma,1}$	20 [mΩ]
Secondary Resistance	$R_{\sigma,x}$	.4 [mΩ]

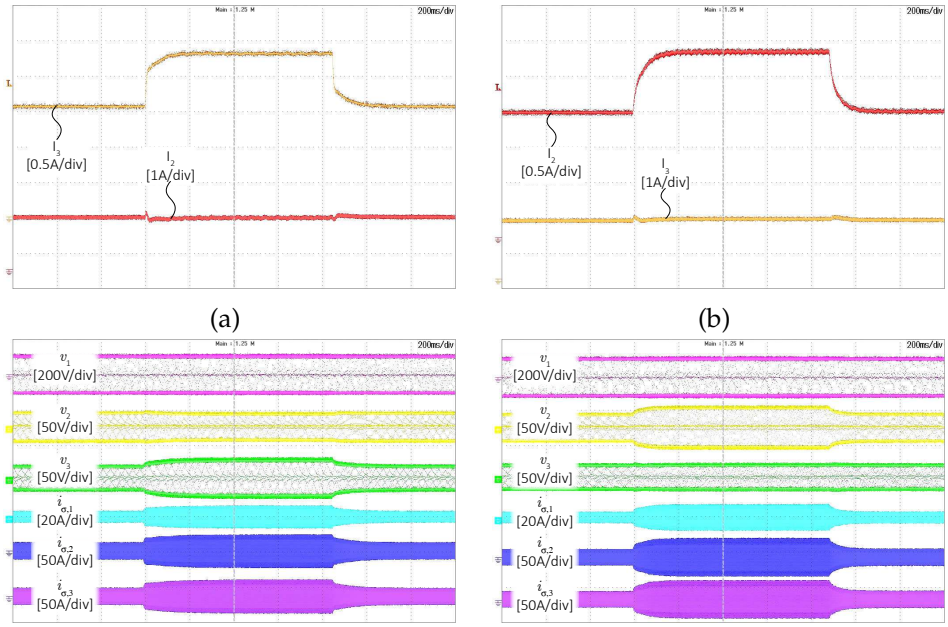


FIGURE 3.7: Step response of the proposed controller using dc capacitor voltage based coupling estimator. In (a) are the load currents response to change in reference of $i^*_{\sigma,2}$, in (b) are the load currents response to change in reference of $i^*_{\sigma,3}$. In (c) and (d) are the transformer currents and voltages.

The operation of the proposed controller is verified in the hardware experiments. The prototype parameters are summarized in Table 4.15. The converter switching frequency is 20 kHz. The load resistances R_2 and R_3 were 10Ω. The main goal of the experiment is to demonstrate the decoupling of the power flow P_{12} and P_{13} inside of

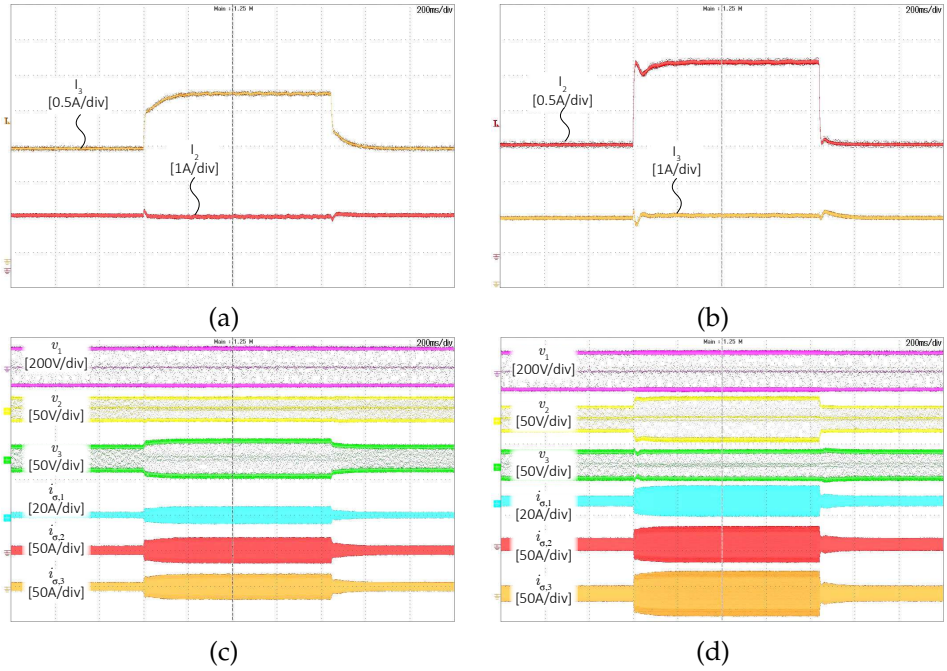


FIGURE 3.8: Step response of the proposed controller using transformer voltage based coupling estimator. In (a) are the load currents response to change in reference of $i^*_{\sigma,2}$, in (b) are the load currents response to change in reference of $i^*_{\sigma,3}$. In (c) and (d) are the transformer currents and voltages.

the TAB converter. To this end, each port of the converter is stepped separately up and down. The results are shown in Fig. 3.7 and Fig. 3.8.

The response of the load currents to step in the reference of port two is shown in Fig. 3.7a. The load current $i_{\text{load},1}$ changes and tracks the reference. The load current I_3 is only slightly disturbed. The same step change is repeated with port three. Figures 3.8b show similar performance and good disturbance rejection. The results show the operation of the controller when the dc capacitor voltages are used for coupling current estimation. The high-frequency signals during steps are shown in Fig. 3.7c and Fig. 3.7d showing smooth envelopes and good disturbance rejection on the transformer state-space variables as well.

The response of the load currents to step in the reference for ports two and three when the estimator based on the transformer voltages is used are shown in Fig. 3.8. As can be seen, the controller decouples the power flows very fast. Moreover, a faster step can be achieved when the PI controllers bandwidth is increased. The high-frequency signals during steps using the transformer voltage based estimator are shown in Fig. 3.8d and Fig. 3.8c showing smooth envelopes and good disturbance rejection on the transformer state-space variables as well.

3.5 CONCLUDING REMARKS

In this chapter, a new approach to the decoupling control of the triple active bridge (TAB) is derived and verified in hardware experiments. The main difference between the proposed controller and previous works is the use of the ac transformer current dynamics to achieve the decoupling of the control variables. The chapter analyses the physical origin of the power flow coupling. A coupling current component is defined using the delta convention. Two estimators of the coupling current component are derived. The implementation of the decoupling controller in the digital domain is thoroughly analyzed and described.

The proposed decoupling control belongs to the family of model-based controllers and uses high-frequency variables. The implementation of the controller is somewhat complicated, however, the derivations and analysis provide valuable insights into the operation of the TAB converter. The main limitation of the controller is the use of high-frequency currents. The measurement and computing delays must be significantly smaller than the shortest phase-shifts employed. Therefore, the controller is suitable for converters with larger power ratings that operate with lower switching frequencies.

4

EXTENDED SOFT-SWITCHING AND RMS MINIMIZATION OF TRIPLE ACTIVE BRIDGE CONVERTER

This chapter explores the operating efficiency limits of the triple active bridge (TAB) converter. First Fourier series is used to model the operation of the TAB converter. Using Fourier series expansion, a closed form solution for soft-switching conditions are derived that take into account practical design aspects. The Fourier series model is further used to explore options how to improve the efficiency of operation of the TAB. A simple modulation improvement is proposed, which uses port voltages to reduce the rms of transformer currents. A detailed loss model is used to show that the proposed modulation reduces switching, conduction and magnetic losses. The analyses are validated with experimental results.

This chapter is based on:

J2 P. Purgat, S. Bandyopadhyay, Z. Qin, P. Bauer-*"Zero Voltage Switching Criteria of Triple Active Bridge Converter", IEEE Transactions on Power Electronics*

4.1 INTRODUCTION

Previous chapter introduced multi-port converters (MPC) as a system capable of integrating multiple sources, storages and loads with varied voltage and current ratings into a single power stage allowing bi-directional power flow between each port. The triple active bridge converter was chosen from this family to be used as a block to build a PFCC optimal for bipolar LVDC grids.

The basic TAB modulation, that was used in the previous chapter, uses 50% duty cycles on all three full bridges and uses the phase-shifts across the three leakage inductors to transfer power between the ports [77,78,85,90]. However, operating with only two independent degrees of freedom leads to loss of soft-switching and high circulating currents in the HF link [85,86]. Similarly, in DAB converters operating with a single phase-shift leads to loss of softswitching and higher current stress. Different dual phaseshifts modulations [91–93] and triple phase-shift modulations [94–96] were proposed for DAB to increase the operating efficiency. The soft-switching areas of DAB converters operated with all three degrees of freedom were identified using various approaches [97–103]. Firstly, many approaches use steady-state time-domain analysis or small-signal statespace modelling techniques [103,104]. Using the time domain analysis DAB operation was characterised into twelve operating modes in [105] and later simplified into five operating modes using graphical method in [106]. Furthermore, computationally intensive numerical approaches that incorporate the effect of parasitic capacitances were used to derive ZVS boundaries [101]. Lastly, the effect of parasitic capacitance was taken into account using energy balance equations [102]. However, the TAB converters due to the higher number of degrees of freedom and superpositions of port voltages applied to a transformer have several tens of operating modes. The complexity makes the use of graphical methods such as [106] or computational intensive methods such as [101] impractical.

For TAB converters the work rigorously deriving and analysing the soft-switching boundaries is virtually nonexistent. A derivation of soft-switching boundaries for threeport converter without considering the effect of parasitic capacitors and only considering the basic phase-shifts are described in [107]. Moreover, due to not considering the superposition of voltages on the transformer, the listed conditions in [107] are not complete. Derivation of ZVS for a three-port topology made of half-bridges is in [86]. Again, the effect of parasitic capacitances is not considered. The soft-switching conditions under all five independent degrees of freedom and taking into account the effect of parasitic capacitances were not yet derived and analysed.

The ZVS condition analysis includes two steps: the first step is to express the transformer currents as a function of the port voltages, phase shift angles, switching frequency, and leakage inductance. The second step is to identify all the commutation modes of the converters. In each commutation mode, calculate the minimum current that is sufficient to discharge the output capacitor of the switch that is going to turn on. In the available literature, two approaches for the first step can be found: piece-wise expression or harmonic form expression of transformer currents. A piece-wise expression is easy to understand [105]; however, to implement it in a digital controller is a bit complicated, since the expression changes in each switching pattern. The

implementation becomes even more involved with an increasing number of switching patterns when the modulation changes from a single-phase shift to a dual-phase shift or further to triple-phase shift. Thank to [100], harmonic form expression is a kind of unified interpretation of the transformer current no matter which switching pattern it is in or which modulation is used. It, therefore, makes expression more concise and the implementation in digital controller much more straightforward.

Yet, from the dual active bridge to triple active bridge, there is a gap. Since one more port is added, there are three more parameters as the input of the transformer current expressions, including the port voltage, duty cycle, and phase shift angle. Moreover, adding the third port is not an extension of a dual active bridge in terms of the transformer currents or ZVS conditions. Since the third port is highly coupled with the initial two ports, the transformer current expressions and ZVS conditions of even the initial two ports are entirely changed. Thus, the ZVS condition analysis in triple active bridge converters can hardly be found in the literature. As a result, this paper demonstrates a concise and clear approach to analyze the ZVS criteria of TAB: firstly all the operation scenarios are categorized into four commutation modes; then in each mode Thevenin Equivalence is applied to effectively address the minimum discharging current for each port meanwhile taking into account the coupling between the port voltages and leakage inductances; eventually, by the harmonic form expression of the transformer currents, the ZVS conditions can be calculated. Experimental results are obtained under various voltage ratios, and phase shift angles to validate the analysis.

4.1.1 *Contribution*

The main contribution of this chapter is the derivation, analysis and experimental verification of the zero-voltage switching boundaries, analytical investigation of losses occuring due to circulating power that gives insight into the operation and operating limits of the triple active bridge converter while improving it's overall operating efficiency. Experimental results are obtained under various voltage and load conditions to validate the analysis.

4.2 TRIPLE ACTIVE BRIDGE MODELLING

4.2.1 *Fourier Series Model*

The port ac voltages v_1, v_2 and v_3 can be described using Fourier series. The infinite sums describing the port voltages are

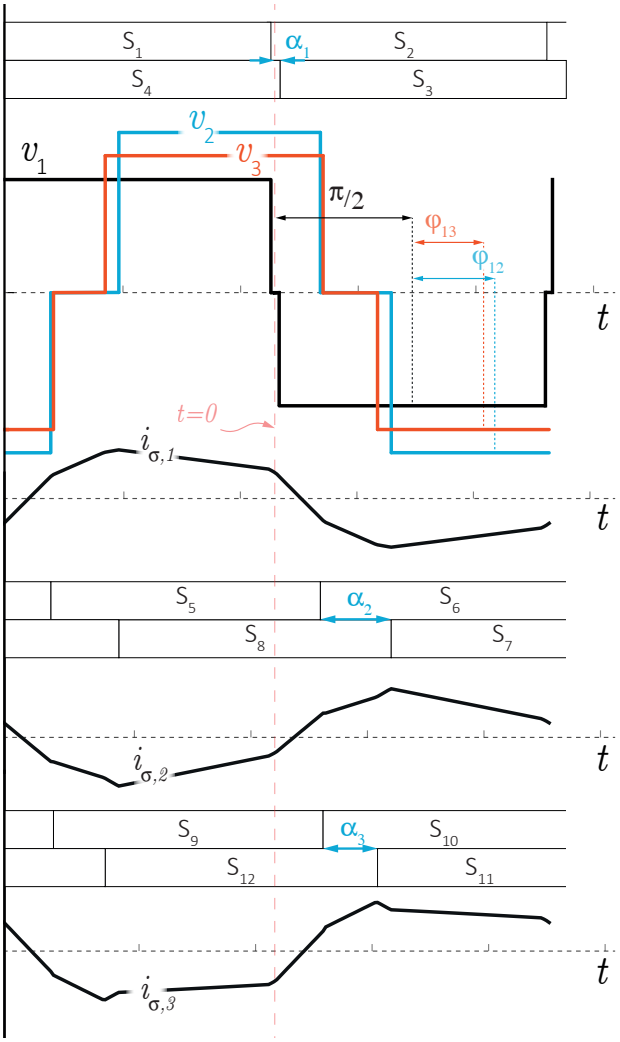


FIGURE 4.1: Phase leg switched voltages and port currents during commutation.

$$v_1(t) = \sum_{\substack{1 \le n < \infty \\ n \text{ odd}}} \left[V_1 d_{1,r} \frac{\sin(nt\omega_s)}{n} \right], \tag{4.1}$$

$$v_2(t) = \sum_{\substack{1 \le n < \infty \\ n \text{ odd}}} \left[V_2 d_{2,i} \frac{\cos(nt\omega_s)}{n} + V_2 d_{2,r} \frac{\sin(nt\omega_s)}{n} \right], \tag{4.2}$$

$$v_3(t) = \sum_{\substack{1 \le n < \infty \\ n \text{ odd}}} \left[V_3 d_{3,i} \frac{\cos(nt\omega_s)}{n} + V_3 d_{3,r} \frac{\sin(nt\omega_s)}{n} \right], \tag{4.3}$$

where

$$d_{1,r} = \frac{4}{\pi} \cos\left(\frac{n\alpha_1}{2}\right), \tag{4.4}$$

$$d_{2,r} = \frac{4}{\pi} \cos\left(\frac{n\alpha_2}{2}\right) \cos\left(n\varphi_{12}\right), \tag{4.5}$$

$$d_{2,i} = \frac{4}{\pi} \cos\left(\frac{n\alpha_2}{2}\right) \sin\left(n\varphi_{12}\right), \tag{4.6}$$

$$d_{3,r} = \frac{4}{\pi} \cos\left(\frac{n\alpha_3}{2}\right) \cos\left(n\varphi_{13}\right), \tag{4.7}$$

$$d_{3,i} = \frac{4}{\pi} \cos\left(\frac{n\alpha_3}{2}\right) \sin\left(n\varphi_{13}\right). \tag{4.8}$$

The definition of φ_{12}, φ_{13} and α_1, α_2, α_3 is graphically demonstrated in Fig. 4.1.

The inductor currents in the circuit described in delta convention can be calculated as

$$i_{\sigma,xy}(t) - i_{\sigma,xy}(0) = \frac{1}{L_{\sigma,xy}} \int_0^t \left[v_x(\tau) - v_y(\tau)\right] \mathrm{d}\tau, \tag{4.9}$$

considering the switching symmetry across the switching cycle it is clear that current at $t = 0$ is the same as the current at $t = \frac{\pi}{2\omega_s}$, i.e. $i_{\sigma,xy}(\frac{\pi}{2\omega_s}) = i_{\sigma,xy}(0)$. The transformer current in delta circuit can be written as

$$\begin{aligned} i_{\sigma,12}(t) = &\frac{-V_2}{L_{\sigma,12}\omega_s} \sum_{\substack{1 \le n < \infty \\ n \text{ odd}}} \left[m_{12} d_{1,r} \frac{\cos\left(nt\omega_s\right)}{n^2} \right. \\ &\left. - d_{2,r} \frac{\cos\left(nt\omega_s\right)}{n^2} + d_{2,i} \frac{\sin\left(nt\omega_s\right)}{n^2} \right], \end{aligned} \tag{4.10}$$

$$\begin{aligned} i_{\sigma,13}(t) = &\frac{-V_3}{L_{\sigma,13}\omega_s} \sum_{\substack{1 \le n < \infty \\ n \text{ odd}}} \left[m_{13} d_{1,r} \frac{\cos\left(nt\omega_s\right)}{n^2} \right. \\ &\left. - d_{3,r} \frac{\cos\left(nt\omega_s\right)}{n^2} + d_{3,i} \frac{\sin\left(nt\omega_s\right)}{n^2} \right], \end{aligned} \tag{4.11}$$

$$\begin{aligned} i_{\sigma,23}(t) = &\frac{-V_3}{L_{\sigma,23}\omega_s} \sum_{\substack{1 \le n < \infty \\ n \text{ odd}}} \left[m_{23} \left(d_{2,r} \frac{\cos\left(nt\omega_s\right)}{n^2} \right. \right. \\ &\left. - d_{2,i} \frac{\sin\left(nt\omega_s\right)}{n^2} \right) - d_{3,r} \frac{\cos\left(nt\omega_s\right)}{n^2} \\ &\left. + d_{3,i} \frac{\sin\left(nt\omega_s\right)}{n^2} \right], \end{aligned} \tag{4.12}$$

where $m_{12} = \frac{V_1}{V_2}$, $m_{13} = \frac{V_1}{V_3}$ and $m_{23} = \frac{V_2}{V_3}$.

TABLE 4.1: Closed-form solution of the port ac currents

Current	Closed-form solution
$i_{\sigma,1}(\tau_j)$	$-\frac{\pi V_2}{2\omega_s L_{\sigma,12}}\left[1+m_1\left(\frac{\left\lvert\frac{\alpha_1}{2}+\tau_j\right\rvert+\left\lvert\frac{-\alpha_1}{2}+\tau_j\right\rvert}{\pi}-1\right)-\frac{\left(\left\lvert\frac{\alpha_2}{2}+\tau_j-\varphi_{12}\right\rvert+\left\lvert-\frac{\alpha_2}{2}+\tau_j-\varphi_{12}\right\rvert\right)}{\pi}\right]+$ $\frac{-\pi V_3}{2\omega_s L_{\sigma,13}}\left[1+m_2\left(\frac{\left\lvert\frac{\alpha_1}{2}+\tau_j\right\rvert+\left\lvert\frac{-\alpha_1}{2}+\tau_j\right\rvert}{\pi}-1\right)-\frac{\left(\left\lvert\frac{\alpha_3}{2}+\tau_j-\varphi_{13}\right\rvert+\left\lvert-\frac{\alpha_3}{2}+\tau_j-\varphi_{13}\right\rvert\right)}{\pi}\right]$
$i_{\sigma,2}(\tau_j)$	$\frac{\pi V_2}{2\omega_s}\left[\frac{1}{L_{\sigma,12}}\left[1+m_1\left(\frac{\left\lvert\frac{\alpha_1}{2}+\tau_j\right\rvert+\left\lvert\frac{-\alpha_1}{2}+\tau_j\right\rvert}{\pi}-1\right)-\frac{\left(\left\lvert\frac{\alpha_2}{2}+\tau_j-\varphi_{12}\right\rvert+\left\lvert-\frac{\alpha_2}{2}+\tau_j-\varphi_{12}\right\rvert\right)}{\pi}\right]+\right.$ $\left.\frac{-1}{L_{\sigma,23}}\left[\frac{1}{m_3}\left(1-\frac{\left\lvert\frac{\alpha_3}{2}+\tau_j-\varphi_{13}\right\rvert+\left\lvert\frac{\alpha_3}{2}-\tau_j+\varphi_{13}\right\rvert}{\pi}\right)+\frac{\left\lvert\frac{\alpha_2}{2}+\tau_j-\varphi_{12}\right\rvert+\left\lvert\frac{\alpha_3}{2}-\tau_j+\varphi_{12}\right\rvert}{\pi}-1\right]\right]$
$i_{\sigma,3}(\tau_j)$	$\frac{\pi V_3}{2\omega_s}\left[\frac{1}{L_{\sigma,13}}\left[1+m_2\left(\frac{\left\lvert\frac{\alpha_1}{2}+\tau_j\right\rvert+\left\lvert\frac{-\alpha_1}{2}+\tau_j\right\rvert}{\pi}-1\right)-\frac{\left(\left\lvert\frac{\alpha_3}{2}+\tau_j-\varphi_{13}\right\rvert+\left\lvert-\frac{\alpha_3}{2}+\tau_j-\varphi_{13}\right\rvert\right)}{\pi}\right]+\right.$ $\left.\frac{1}{L_{\sigma,23}}\left[m_3\left(\frac{\left\lvert\frac{\alpha_2}{2}+\tau_j-\varphi_{12}\right\rvert+\left\lvert\frac{\alpha_2}{2}-\tau_j+\varphi_{12}\right\rvert}{\pi}-1\right)-\frac{\left(\left\lvert\frac{\alpha_3}{2}+\tau_j-\varphi_{13}\right\rvert+\left\lvert\frac{\alpha_3}{2}-\tau_j+\varphi_{13}\right\rvert\right)}{\pi}-1\right]\right]$

4.2.2 *Closed Form Solution*

By substituting the harmonic form expression of the duty cycle in (4.4)-(4.8) and the delta circuit currents in (4.10)-(4.12), into the port currents in (3.5)-(3.7), the closed-form solution of the port current $i_{\sigma,1}(\tau_j)$, $i_{\sigma,2}(\tau_j)$ and $i_{\sigma,3}(\tau_j)$ at the events of switching transitions τ_j can be obtained, and they are summarized in Table 4.5. The times of switching event τ_j are defined in Tables 4.7 and 4.9. Note that in the derivation procedure of the closed form solution of the port currents from harmonic form expression, following properties of infinite series of odd components are used

$$\sum_{\substack{1\leq n<\infty \\ n \text{ odd}}} \frac{1}{n^2} = \frac{\pi^2}{8}, \tag{4.13}$$

$$\sum_{\substack{1\leq n<\infty \\ n \text{ odd}}} \frac{\cos(n\beta)}{n^2} = \frac{\pi(\pi - |2\beta|)}{8}, \tag{4.14}$$

where β is any angle in radians. The closed form solutions of the port currents are summarized in Table 4.4. The times of switching event τ_j are defined in Tables 4.7 and 4.9.

4.3 ZERO VOLTAGE SWITCHING

The full-bridge ac voltages and the corresponding currents are shown in Fig. 4.1. In an ideal case, the energy stored in the MOSFETs parasitic capacitors is ignored, and the magnetising inductance of the transformer is considered to be infinite. In this ideal case, the ZVS operation of the converter switches is only dependent on the direction of the output bridge current during the state transition. ZVS occurs when the output current of a bridge is flowing through the active switch of corresponding half-bridge as the half-bridges opposing transistor becomes active, in such a case the current will naturally commute to the opposing switch anti-parallel diode after the active switched is turned off.

The parasitic capacitance of MOSFET adds a soft-switching condition, in the form of minimal current in the leakage inductance that is required to complete the ZVS commutation. In order to derive the ZVS conditions for the TAB converter, it is assumed that the converter operates in steady-state, i.e. only one phase leg commutates at each switching event.

TAB can be operated with five phase-shifts. Two phase-shifts between ports φ_{12}, φ_{13}, and three phase-shifts that are defined between phase legs of each port α_1, α_2 and α_3. The phase-shifts φ_{12}, φ_{13} as marked in Fig.4.1 are defined as the difference between the middle points of the switching cycles. These five degrees of freedom can create tens of different operating modes, and examination of each with graphical tools is impractical. Therefore to analyse ZVS of a TAB converter, first, a comprehensive investigation of ZVS conditions for generic full-bridge operated with phase-shifts φ_x and α_x is presented. In the generic full-bridge, four separate switching modes are

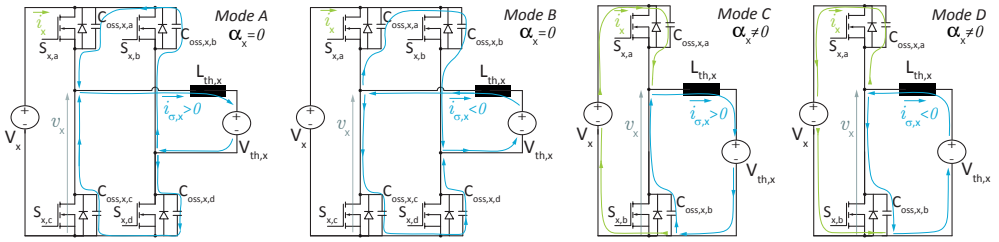


FIGURE 4.2: Port schematics during four possible commutation modes.

identified. These four modes encompass all unique commutations, i.e. the remaining commutations are always symmetrical counter-parts of described commutations. The four commutation modes can be divided into two groups based on the phase leg phase shift α_x, and further subdivided by the direction of the port current $i_{\sigma,x}$. In second step, values of inductor $L_{\text{th},x}$ and amplitude of voltage source $v_{\text{th},x}$ in the generic full bridge are derived.

The need for the second step stems from the fact that the inductor as well as the voltage source in TAB converter are not simple constants (unlike in DAB), but are superpositions of each ports state at the given time instant. Therefore, Thevenin equivalents of these voltages are derived in the second step. The third step consists of synthesis of the conditions from the first step, Thevenin equivalents impedances and voltage sources and the respective sequences of switching instances τ_j. These three steps establish conditions for ZVS in TAB converter.

4.3.1 *Mode A:* $\alpha_x = 0$, $i_{\sigma,x}(\tau_j) > 0$

In mode A all four switches are commutating, $S_{x,a}$ and $S_{x,d}$ have been turned off, while $S_{x,b}$ and $S_{x,c}$ are going to be turned on. From Fig. 4.2a following current equations can be written

$$i_{\sigma,x}\left(\tau_j\right) = -2C_{\text{oss},x}\frac{\mathrm{d}v_x}{\mathrm{d}t}, \tag{4.15}$$

$$i_x\left(\tau_j\right) = 0. \tag{4.16}$$

The minimum current requirement for ZVS is obtained from the energy absorbed by $V_{\text{th},x}$, which can be calculated as follows

$$E_{\text{absorbed}} = \int_{T_{\text{com}}} V_{\text{th},x} i_{\sigma,x}(\tau_j)\mathrm{d}t. \tag{4.17}$$

Combining (4.15), (4.16) and assuming the voltage v_x is changing from V_x to 0 in (4.17), following is obtained

$$E_{\text{absorbed}} = 2C_{\text{oss},x}V_{\text{th},x}V_x. \tag{4.18}$$

The sum of energy stored in the parasitic capacitors does not change during commutation. To find the minimum current amplitude requirement, an energy inequality can be written as

$$\frac{1}{2}L_{\mathrm{th},x}i^2_{\sigma,x}(\tau_j) \geq 2C_{\mathrm{oss},x}V_{\mathrm{th},x}V_x. \tag{4.19}$$

The polarity of the voltage $V_{\mathrm{th},x}$ is assumed to be positive in (4.19). If the voltage $V_{th,x}$ is negative, then ZVS is always achieved. The minimal current condition for Mode A, when $V_{\mathrm{th},x} > 0$ can be written as

$$\left|i_{\sigma,x}(\tau_j)\right| \geq 2V_x\sqrt{\frac{C_{\mathrm{oss},x}}{L_{\mathrm{th},x}}\frac{V_{\mathrm{th},x}}{V_x}}. \tag{4.20}$$

4.3.2 *Mode B:* $\alpha_x = 0$, $i_{\sigma,x}(\tau_j) < 0$

As shown in Fig. 4.2b, in mode B, all four switches are commutating, where $S_{x,b}$ and $S_{x,c}$ have been turned off while $S_{x,a}$ and $S_{x,d}$ are going to be turned on. The inductor current is flowing into the full bridge, which is in reverse compared to mode A. The current equations from Fig. 4.2b can be written as

$$i_{\sigma,x}(\tau_j) = -2C_{\mathrm{oss},x}\frac{\mathrm{d}v_x}{\mathrm{d}t}, \tag{4.21}$$

$$i_x(\tau_j) = 0. \tag{4.22}$$

Similarly as in mode A, following energy inequality can be derived

$$\frac{1}{2}L_{\mathrm{th},x}i^2_{\sigma,x}(\tau_j) \geq -2C_{\mathrm{oss},x}V_{\mathrm{th},x}V_x. \tag{4.23}$$

In (4.23) it is assumed that $V_{\mathrm{th},x}$ is negative, otherwise ZVS is assured. The minimal current requirement for mode B can be written as

$$\left|i_{\sigma,x}(\tau_j)\right| \geq 2V_x\sqrt{-\frac{C_{\mathrm{oss},x}}{L_{\mathrm{th},x}}\frac{V_{\mathrm{th},x}}{V_x}}. \tag{4.24}$$

The inequality (4.24) is derived for switches $S_{\mathrm{x},a}$ and $S_{\mathrm{x},d}$ turning on.

4.3.3 *Mode C:* $\alpha_x \neq 0$, $i_{\sigma,x}(\tau_j) > 0$

Mode C commutation is shown in Fig. 4.2c. Mode C occurs when the phase-shift α_x is non-zero. The soft-switching conditions for leading and lagging phase-leg become different. According to Fig. 4.2c the currents are

$$i_{\sigma,x}(\tau_j) = -2C_{\mathrm{oss},x}\frac{\mathrm{d}v_x}{\mathrm{d}t}, \tag{4.25}$$

TABLE 4.3: ZVS Conditions of TAB Converter

Mode	Switches turned-on	Conditions
A	S_c and S_b	if $V_{\text{th},x} > 0$ the ZVS condition is $\left\|i_{\sigma,x}\left(\tau_j\right)\right\| \geq 2V_x\sqrt{\frac{C_{\text{oss},x}}{L_{\text{th},x}}\frac{V_{\text{th},x}}{V_x}}$
		if $V_{\text{th},x} < 0$, the ZVS is assured
B	S_a and S_d	if $V_{\text{th},x} < 0$ the ZVS condition is $\left\|i_{\sigma,x}\left(\tau_j\right)\right\| \geq 2V_x\sqrt{-\frac{C_{\text{oss},x}}{L_{\text{th},x}}\frac{V_{\text{th},x}}{V_x}}$
		if $V_{\text{th},x} > 0$, the ZVS is assured
C	S_b	if $V_{\text{th},x} > \frac{V_x}{2}$, the ZVS condition is $\left\|i_{\sigma,x}\left(\tau_j\right)\right\| \geq 2V_x\sqrt{\frac{C_{\text{oss},x}}{L_{\text{th},x}}\frac{V_{\text{th},x}}{V_x} - \frac{C_{\text{oss},x}}{2L_{\text{th},x}}}$
		if $V_{\text{th},x} < \frac{V_x}{2}$, the ZVS is assured
D	S_a	if $V_{\text{th},x} < \frac{V_x}{2}$, the ZVS condition is $\left\|i_{\sigma,x}\left(\tau_j\right)\right\| \geq 2V_x\sqrt{-\frac{C_{\text{oss},x}}{L_{\text{th},x}}\frac{V_{\text{th},x}}{V_x} + \frac{C_{\text{oss},x}}{2L_{\text{th},x}}}$
		if $V_{\text{th},x} > \frac{V_x}{2}$, the ZVS is assured

$$i_x(\tau_j) = -C_{\text{oss},x}\frac{\mathrm{d}v_x}{\mathrm{d}t}. \tag{4.26}$$

As was done for modes A and B, calculating the absorbed energy by source $v_{th,x}$ leads to calculation of the minimum current amplitude requirement. Energy absorbed by the sources can be calculated as

$$E_{\text{absorbed}} = \int_{T_{\text{com}}} V_{\text{th},x} i_{\sigma,x}(\tau_j)\mathrm{d}t - \int_{T_{\text{com}}} V_x i_x(\tau_j)\mathrm{d}t. \tag{4.27}$$

Combining to (4.25), (4.26) and assuming the voltage v_x to change from V_x to 0 in (4.27) following is obtained

$$E_{\text{absorbed}} = 2C_{\text{oss},x}V_{\text{th},x}V_x - C_{\text{oss},x}V_x^2. \tag{4.28}$$

Similarly as for modes A and B, minimum current requirement can be obtained from

$$\frac{1}{2}L_{\text{th}}i_{\sigma,x}^2(\tau_j) \geq 2C_{\text{oss},x}V_{\text{th},x}V_x - C_{\text{oss},x}V_x^2, \tag{4.29}$$

From (4.29) a ZVS condition can be obtained

$$\left|i_{\sigma,x}(\tau_j)\right| \geq 2V_x\sqrt{\frac{C_{\text{oss},x}}{L_{\text{th},x}}\frac{V_{\text{th},x}}{V_x} - \frac{C_{\text{oss},x}}{2L_{\text{th},x}}}, \tag{4.30}$$

where $V_{\text{th},x} > \frac{V_x}{2}$ otherwise ZVS is assured for switch S_b.

4.3.4 *Mode D- $\alpha_x \neq 0$, $i_{\sigma,x}(\tau_j) < 0$*

The counter part of mode C is mode D which occurs when the inductor current has opposite polarity. Circuit describing mode D is shown in Fig. 4.2d. The current equations can be written as

$$i_{\sigma,x}(\tau_j) = -2C_{\text{oss},x}\frac{\mathrm{d}v_x}{\mathrm{d}t}, \tag{4.31}$$

$$i_x(\tau_j) = -C_{\text{oss},x}\frac{\mathrm{d}v_x}{\mathrm{d}t}. \tag{4.32}$$

Similarly as for mode C, energy absorbed and supplied can be derived. The notable difference is the change of voltage v_x from 0 to V_x. Using the inductor and capacitances energies, minimum current amplitude requirement can be written as

$$\frac{1}{2}L_{\text{th},x}i_{\sigma,x}^2(\tau_j) \geq -2C_{\text{oss},x}V_{\text{th},x}V_x + C_{\text{oss},x}V_x^2. \tag{4.33}$$

From (4.33) the minimum amplitude current requirement can be obtained as

$$\left|i_{\sigma,x}(\tau_j)\right| \geq 2V_x\sqrt{-\frac{C_{\text{oss},x}}{L_{th,x}}\frac{V_{\text{th},x}}{V_x} + \frac{C_{\text{oss},x}}{2L_{\text{th},x}}}. \tag{4.34}$$

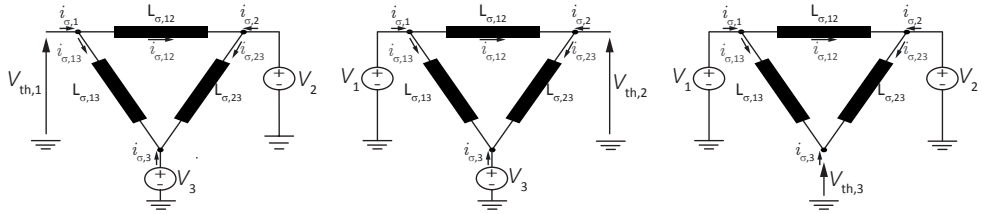


FIGURE 4.3: Equivalent Thevenin circuits.

Condition (4.34) is derived for turn on of switch S_a when voltage $V_{\text{th},x}$ is smaller than $\frac{V_x}{2}$, otherwise ZVS is assured for S_a.

The ZVS conditions for all modes are summarized in Table 4.3. The parameters like $V_{\text{th},x}$, $L_{\text{th},x}$ and $i_{\sigma,x}$ for the conditions are then derived as follows in Table 4.5.

4.3.5 *Thevenin Equivalent Circuits*

The delta circuit from Fig. 3.3 is simplified into three Thevenin equivalent circuits as shown in Fig. 4.3. During commutation, the port voltage either remains the same or has already changed to new value, and thereby they are considered as constant voltage and expressed with uppercase letters. For illustration, the Thevenin equivalent impedance during commutation of port one can be derived from circuit in Fig. 4.3a. The equivalent impedance is calculated by short-circuiting V_2 and V_3 and equals

$$L_{\text{th},1} = \frac{L_{\sigma,12}L_{\sigma,13}}{L_{\sigma,12} + L_{\sigma,13}}. \tag{4.35}$$

The Thevenin equivalent voltage for the same circuit is a superposition of the two voltage dividers at time instant τ_1 and can be written as

$$V_{\text{th},1}(\tau_1) = V_2(\tau_1)\frac{L_{\sigma,13}}{L_{\sigma,12} + L_{\sigma,13}} + V_3(\tau_1)\frac{L_{\sigma,12}}{L_{\sigma,12} + L_{\sigma,13}}. \tag{4.36}$$

Thevenin equivalent impedances and voltages can be derived for other ports in similar manner, and are summarized in Table 4.5.

4.3.5.1 *Non-Linear Parasitic Capacitance $C_{oss,x}$*

The C_{oss} is not constant, and it varies with drain-source voltage Vds of the switch in a nonlinear way. As a nonlinear function of V_{ds}, the C_{oss} is usually provided in the datasheet of the power switches. Based on it, the equivalent output capacitance of the switch can be calculated. The derivation of (4.18) is shown here to demonstrate how the nonlinearity is considered. (4.18) is obtained by substituting (4.15) and (4.16) into (4.17), which then becomes

$$E_{\text{absorbed}} = 2V_{th,x}\int_0^{V_x} C_{oss,x}(v_x)\mathrm{d}v_x = 2V_{th,x}\bar{C}_{oss,x}(V_x)V_x \tag{4.37}$$

where V_x is the dc link voltage of the port where the transistor operates, v_x is the instant voltage of the C_{oss}, $V_{th,x}$ is contant in the discharging procedure. $C_{oss,x}(v_x)$ is provided in the datasheet. The only thing is that the datasheet usually doesn not

TABLE 4.5: Port Characteristics for ZVS Conditions of TAB Converter

Port no.	$L_{\mathrm{th},x}$	Half-bridge	$V_{\mathrm{th},x}$	$i_{\sigma,x}$
1	$\frac{L_{\sigma,13}L_{\sigma,12}}{L_{\sigma,13}+L_{\sigma,12}}$	Leading	$V_2(\tau_1)\frac{L_{\sigma,13}}{L_{\sigma,13}+L_{\sigma,12}} + V_3(\tau_1)\frac{L_{\sigma,12}}{L_{\sigma,13}+L_{\sigma,12}}$	$i_{\sigma,1}$
		Lagging	$-V_2(\tau_2)\frac{L_{\sigma,13}}{L_{\sigma,13}+L_{\sigma,12}} - V_3(\tau_2)\frac{L_{\sigma,12}}{L_{\sigma,13}+L_{\sigma,12}}$	$-i_{\sigma,1}$
2	$\frac{L_{\sigma,23}L_{\sigma,12}}{L_{\sigma,23}+L_{\sigma,12}}$	Leading	$V_1(\tau_3)\frac{L_{\sigma,23}}{L_{\sigma,23}+L_{\sigma,12}} + V_3(\tau_3)\frac{L_{\sigma,12}}{L_{\sigma,23}+L_{\sigma,12}}$	$i_{\sigma,2}$
		Lagging	$-V_1(\tau_4)\frac{L_{\sigma,23}}{L_{\sigma,23}+L_{\sigma,12}} - V_3(\tau_4)\frac{L_{\sigma,12}}{L_{\sigma,23}+L_{\sigma,12}}$	$-i_{\sigma,2}$
3	$\frac{L_{\sigma,13}L_{\sigma,23}}{L_{\sigma,13}+L_{\sigma,23}}$	Leading	$V_1(\tau_5)\frac{L_{\sigma,23}}{L_{\sigma,23}+L_{\sigma,13}} + V_2(\tau_5)\frac{L_{\sigma,13}}{L_{\sigma,23}+L_{\sigma,13}}$	$i_{\sigma,3}$
		Lagging	$-V_1(\tau_6)\frac{L_{\sigma,23}}{L_{\sigma,23}+L_{\sigma,13}} - V_2(\tau_6)\frac{L_{\sigma,13}}{L_{\sigma,23}+L_{\sigma,13}}$	$-i_{\sigma,3}$

TABLE 4.7: Switching sequences for selection of $V_{\mathrm{th},x}$. (Part I)

Port no.	Half-bridge	Voltages for Thevenin Circuit		τ_j
1	Leading	$V_2(\tau_1) = \begin{cases} V_2 & \text{if } \tau_1 < \tau_3, \\ 0 & \text{if } \tau_3 < \tau_1 < \tau_4, \\ -V_2 & \text{if } \tau_4 < \tau_1, \end{cases}$	$V_3(\tau_1) = \begin{cases} V_3 & \text{if } \tau_1 < \tau_5, \\ 0 & \text{if } \tau_5 < \tau_1 < \tau_6, \\ -V_3 & \text{if } \tau_6 < \tau_1, \end{cases}$	$\tau_1 = -\frac{\alpha_1}{2}$
	Lagging	$V_2(\tau_2) = \begin{cases} V_2 & \text{if } \tau_2 < \tau_3, \\ 0 & \text{if } \tau_3 < \tau_2 < \tau_4, \\ -V_2 & \text{if } \tau_4 < \tau_2, \end{cases}$	$V_3(\tau_2) = \begin{cases} V_3 & \text{if } \tau_2 < \tau_5, \\ 0 & \text{if } \tau_5 < \tau_2 < \tau_6, \\ -V_3 & \text{if } \tau_6 < \tau_2, \end{cases}$	$\tau_2 = \frac{\alpha_1}{2}$
2	Leading	$V_1(\tau_3) = \begin{cases} V_1 & \text{if } \tau_3 < \tau_1, \\ 0 & \text{if } \tau_1 < \tau_3 < \tau_2, \\ -V_1 & \text{if } \tau_2 < \tau_3, \end{cases}$	$V_3(\tau_3) = \begin{cases} V_3 & \text{if } \tau_3 < \tau_5, \\ 0 & \text{if } \tau_5 < \tau_3 < \tau_6, \\ -V_3 & \text{if } \tau_6 < \tau_3, \end{cases}$	$\tau_3 = \varphi_{12} - \frac{\alpha_2}{2}$
	Lagging	$V_1(\tau_4) = \begin{cases} V_1 & \text{if } \tau_4 < \tau_1, \\ 0 & \text{if } \tau_1 < \tau_4 < \tau_2, \\ -V_1 & \text{if } \tau_2 < \tau_4, \end{cases}$	$V_3(\tau_4) = \begin{cases} V_3 & \text{if } \tau_4 < \tau_5, \\ 0 & \text{if } \tau_5 < \tau_4 < \tau_6, \\ -V_3 & \text{if } \tau_6 < \tau_4, \end{cases}$	$\tau_4 = \varphi_{12} + \frac{\alpha_2}{2}$

TABLE 4.9: Switching sequences for selection of $V_{\mathrm{th},x}$. (Part II)

Port no.	Half-bridge	Voltages for Thevenin Circuit		τ_j
3	Leading	$V_1(\tau_5) = \begin{cases} V_1 & \text{if } \tau_5 < \tau_1, \\ 0 & \text{if } \tau_1 < \tau_5 < \tau_2, \\ -V_1 & \text{if } \tau_2 < \tau_5, \end{cases}$	$V_2(\tau_5) = \begin{cases} V_2 & \text{if } \tau_5 < \tau_3, \\ 0 & \text{if } \tau_3 < \tau_5 < \tau_4, \\ -V_2 & \text{if } \tau_4 < \tau_5, \end{cases}$	$\tau_5 = \varphi_{13} - \frac{\alpha_3}{2}$
	Lagging	$V_1(\tau_6) = \begin{cases} V_1 & \text{if } \tau_6 < \tau_1, \\ 0 & \text{if } \tau_1 < \tau_6 < \tau_2, \\ -V_1 & \text{if } \tau_2 < \tau_6, \end{cases}$	$V_2(\tau_6) = \begin{cases} V_2 & \text{if } \tau_6 < \tau_3, \\ 0 & \text{if } \tau_3 < \tau_6 < \tau_4, \\ -V_2 & \text{if } \tau_4 < \tau_6, \end{cases}$	$\tau_6 = \varphi_{13} + \frac{\alpha_3}{2}$

As seen, if V_x does not change or have an only slight change, $\bar{C}_{oss,x}(V_x)$ can be considered as constant. In case V_x varies a lot, $\bar{C}_{oss,x}(V_x)$ at different V_x can be calculated beforehand, and a look-up table based on it can be used for online ZVS analysis.

4.3.5.2 *Dead-Time*

The dead time can influence the ZVS from two aspects: 1. the rising edge or falling edge of the port ac voltage may get delayed due to deadtime. Which edge is going to be delayed depends on the polarity of the port current at the moment of related leg commutation. This effect will be significant when deadtime is comparable with the switching cycle; 2. ZVS is a procedure of LC resonance. Assuming the converter operates on the boundary of ZVS before the switch turns on, its drain-source voltage will first drop to zero and increase again. So the deadtime must match the resonance time to turn on the switch at the exact time when its drain-source voltage drops to zero. Earlier or later, ZVS can not be achieved. However, this is only valid when the converter is on the boundary of ZVS. If the port current is much larger than the minimum current for ZVS, as long as deadtime is longer than discharging time of the switch, ZVS can be achieved.

4.3.6 *Complete ZVS Expressions*

Complete ZVS conditions of TAB depend on the sequence of the switching, as the Thevenin voltage can change in the condition depending on the sequence. This dependence can be illustrated using Fig. 4.1. It is clear that when calculating the Thevenin equivalent voltage for port one, both V_2 and V_3 are positive. However, when calculating the Thevenin equivalent voltage, for example for port two, voltage v_1 already reversed. A similar situation can happen to any port, depending on the sequence. Therefore the voltages in the Thevenin equivalent are functions of the sequence of the switching events. Table **??** gives a complete overview of the sequences.

4.3.7 *Soft-switching Analysis*

The surfaces were calculated using parameters summarised in Table 4.15. Figure 4.4 shows the ZVS areas of all three ports as a function of voltage ratios m_{12} and m_{13} when phase-shifts φ_{12}, φ_{13} and α_1 are used while $\alpha_2 = \alpha_3 = 0$. In figures, 1-Lead and 1-Lagg are defined as the leading leg (composed of S_1 and S_2) and lagging leg (composed of S_3 and S_4) of port one; 2-Lead and 2-Lagg are defined as the leading leg (composed of S_5 and S_6) and lagging leg (composed of S_7 and S_8) of port two; 3-Lead and 3-Lagg are defined as the leading leg (composed of S_9 and S_{10}) and lagging leg (composed of S_{11} and S_{12}) of port three. In Fig. 4.4 phase-shifts φ_{12}, φ_{13} are equal and are varied in the vertical direction, going from 0.05π in the first row to 0.3π in the third row. Phase-shift α_1 is varied in the horizontal direction, i.e. in the first column $\alpha_1 = 0$, while in the third it is 0.3π.

A general observation is that ZVS is achieved at ports with higher voltage, while the ports that have smaller voltage do not achieve ZVS. Moreover, as is the case in the

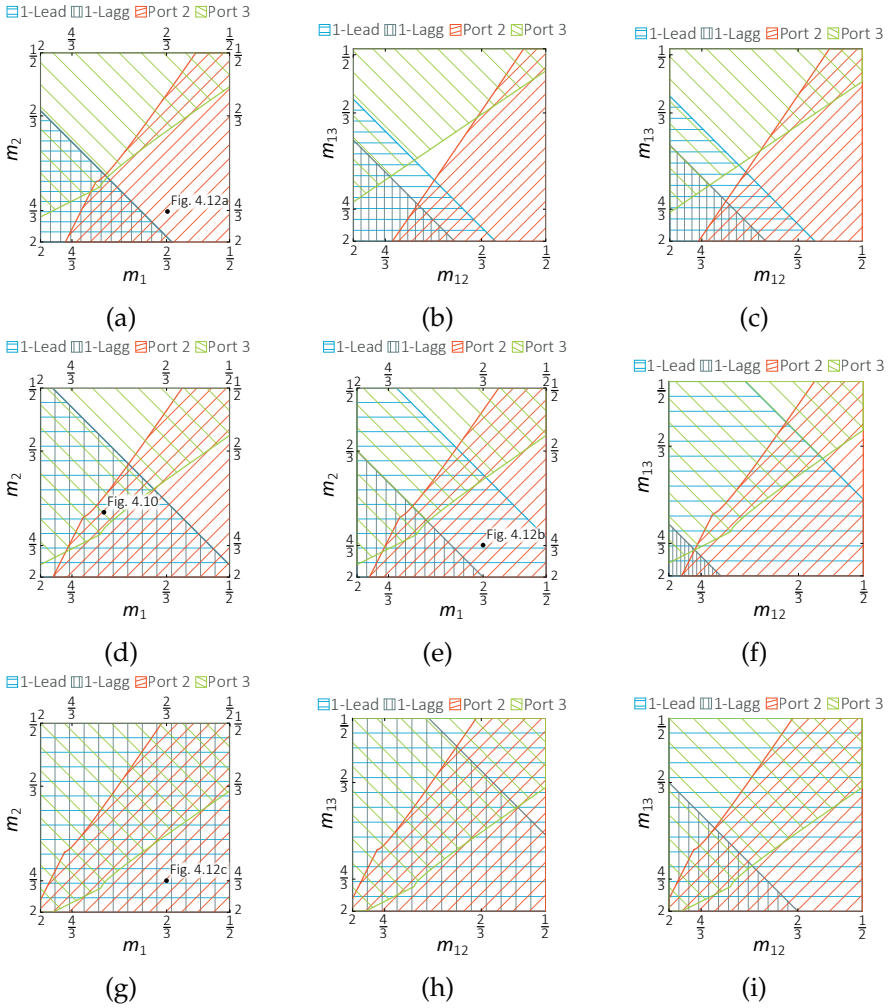


FIGURE 4.4: Zero voltage switching when port one uses phase-shift α_1. In (a)-(c) the phase-shifts are $\varphi_{12} = \varphi_{13} = 0.05\pi$, in (d)-(f) $\varphi_{12} = \varphi_{13} = 0.15\pi$ and in (g)-(i) $\varphi_{12} = \varphi_{13} = 0.3\pi$. In (a),(d) and (g) phase-shift $\alpha_1 = 0$, in (b),(e) and (h) phase-shift $\alpha_1 = 0.15\pi$ and in (c), (f) and (i) phase-shift $\alpha_1 = 0.45\pi$.

dual active bridge, increasing the phase-shifts φ_{12}, φ_{13} leads to ZVS across the large range of voltage ratios. However, large phase-shifts also mean larger losses due to increased circulating power. Secondly, it is clear that for port one, which is assumed to always lead in Fig. 4.4, it is, in general, easier to achieve ZVS for the leading phase-leg.

The ZVS areas of all three ports as a function of phase-shifts φ_{12} and φ_{13} when voltage ratios m_{12} and m_{13} are both equal to $\frac{4}{3}$ is shown in Fig. 4.5. Figure 4.5 also shows the effect of changing phase-shift α_1. As is clear from the figure, achieving ZVS on port one, which has the highest voltage is possible across the whole operating

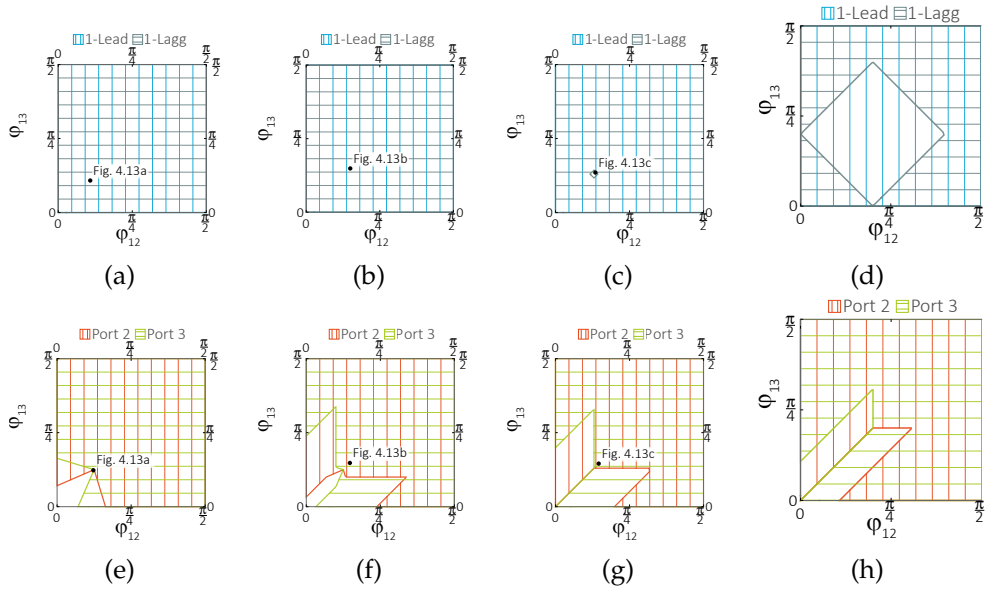


FIGURE 4.5: Calculated zero voltage switching areas when $m_{12} = m_{13}$ are $\frac{4}{3}$. In (a) and (e) $\alpha_1 = 0$. In (b) and (f) $\alpha_1 = 0.2\pi$. In (c) and (g) $\alpha_1 = 0.25\pi$ and in (d) and (h) $\alpha_1 = 0.4\pi$

region. However, for port two and three, the soft-switching areas are limited. Especially, at very light loads achieving ZVS on all phase-legs is difficult. Increasing phase-shift α_1 reduces the ZVS area of the lagging half-bridge in port one. It is interesting to observe the difference between Fig. 4.5b and Fig. 4.5c, when even a relatively small difference in phase-shift α_1 leads to loss of soft-switching on the lagging phase-leg of port one. When phase-shift α_1 is increased even further, then soft-switching can be achieved even for very small phase-shifts on port two and three. However, it leads to loss of soft-switching for lagging phase-leg on port one.

The ZVS areas of all three ports as a function of phase-shifts φ_{12} and φ_{13} when voltage ratios m_{12} and m_{13} are both equal to $\frac{2}{3}$ is shown in Fig. 4.6. Figure 4.6 shows the ZVS area for each port separately for better clarity as four out of five degrees of freedom are in use. ZVS is achieved on port one only for relatively large phase-shifts φ_{12} and φ_{13}. Increasing phase-shifts α_2 and α_3 leads to an increase of ZVS area of the port one. However, the cost of achieving ZVS transitions on port one is the loss of soft-switching on the leading phase-leg on ports two and three. The origin of this can be seen in Fig. 4.1. As is clear, the current needs time to reverse polarity before the lead half-bridge turns on. This time is reduced when phase-shifts α_2 and α_3 are larger than zero. On the contrary, for the lagging half-bridge, this time is increased, thus achieving ZVS for the lagging leg is easier. Moreover, it is clear that achieving ZVS on all ports and all phase-leg simultaneously becomes very difficult when the ports are not loaded equally or have highly unbalanced voltages.

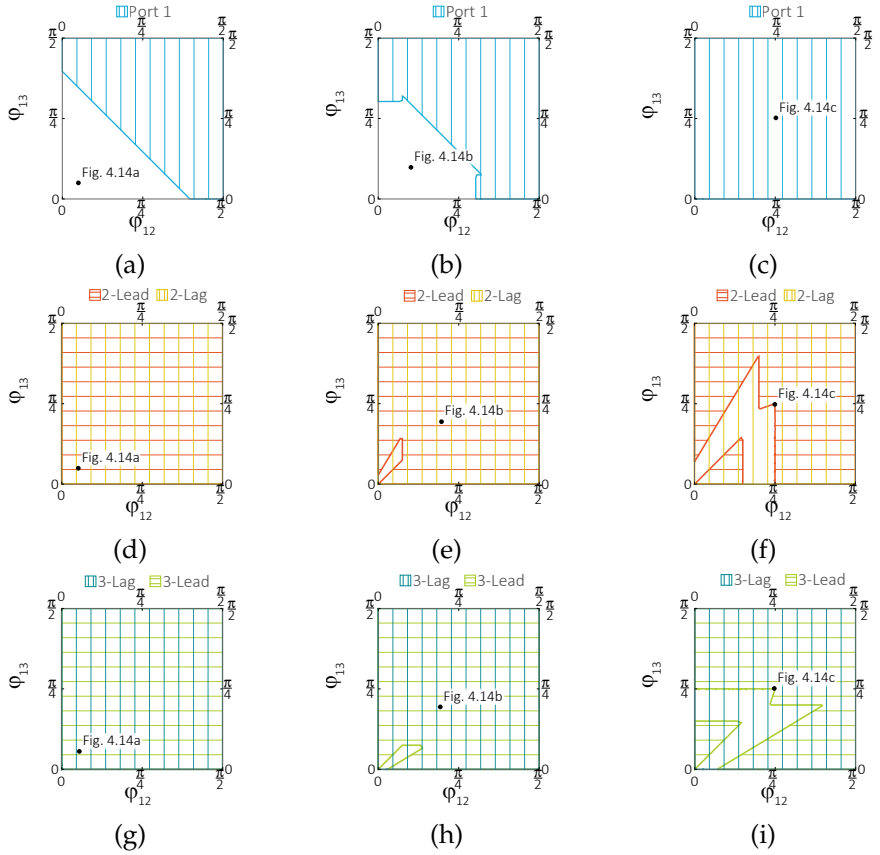


FIGURE 4.6: Calculated zero voltage switching areas when $m_{12} = m_{13}$ are $\frac{2}{3}$. In (a), (d) and (g) $\alpha_2 = \alpha_3 = 0$. In (b), (e) and (h) $\alpha_2 = \alpha_3 = 0.15\pi$. In (c), (f) and (i) $\alpha_2 = \alpha_3 = 0.4\pi$.

4.4 REACTIVE POWER MINIMIZATION

The main goal of the TAB converter is transfer of active power between the three ports. However, alongside the active power a certain amount of circulating power exists in the inductive link. The reactive power demonstrates itself as higher rms inductor current and as such has negative impact on the converter efficiency as it increases the conduction losses in both passive and active components. In this paper Fourier series is used to describe the TAB converter ZVS opeartion. One of the main advantages of this approach is that the same set of equations, used to derive the ZVS conditions can be used to analyse the reactive power in the high-frequency network.

In further text, given the complexity of TAB converter the analysis is constrained to fundamental components of the Fourier series. This is done to keep the equations insightful such that meaningful and applicable modulation laws can be derived. This

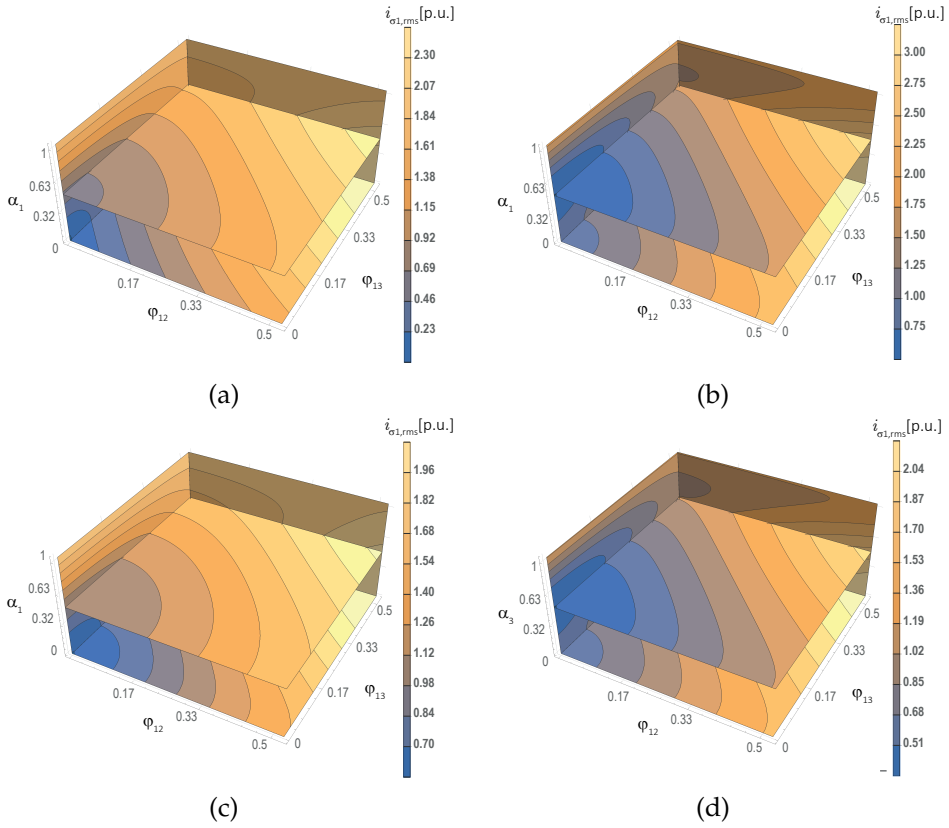


FIGURE 4.7: Calculated p.u. rms of the current at port one. In (a) the voltage ratios are at unity. In (b) both m_{12} and m_{13} are 0.8. In (c) both m_{12} and m_{13} are 1.2. In (c) both m_{12} and m_{13} are 1.2 but now α_3 and α_2 are varied together.

method yields some error, which is is illustrated in Fig. 4.8e-4.8f and will be discussed further in this section. The rms values in this paper are calculated as

$$x_{\mathrm{rms}} = \sqrt{\frac{\omega_s}{\pi} \int_0^{\frac{\pi}{\omega_s}} x^2(t)\, \mathrm{d}t}. \tag{4.39}$$

Using (4.39) rms values of voltages and currents are obtained, and are summarized in Table 4.11. In order to achieve more general conclusions the rms values in this section are normalized and the rms currents are shown in per unit. The normalization is done by dividing the rms current values with $\frac{V_1}{L_{\sigma,12}\omega_s}$.

The effect of variation of all five phase shifts on the rms current at port one is shown in Fig. 4.7. The rms values in Fig. 4.7 were calculated using seventh order coefficients of Fourier series to achieve higher precision for the analysis. It can be seen that the rms of the current at port one can be reduced when phase-shifts α_1, α_2 and α_3 are used

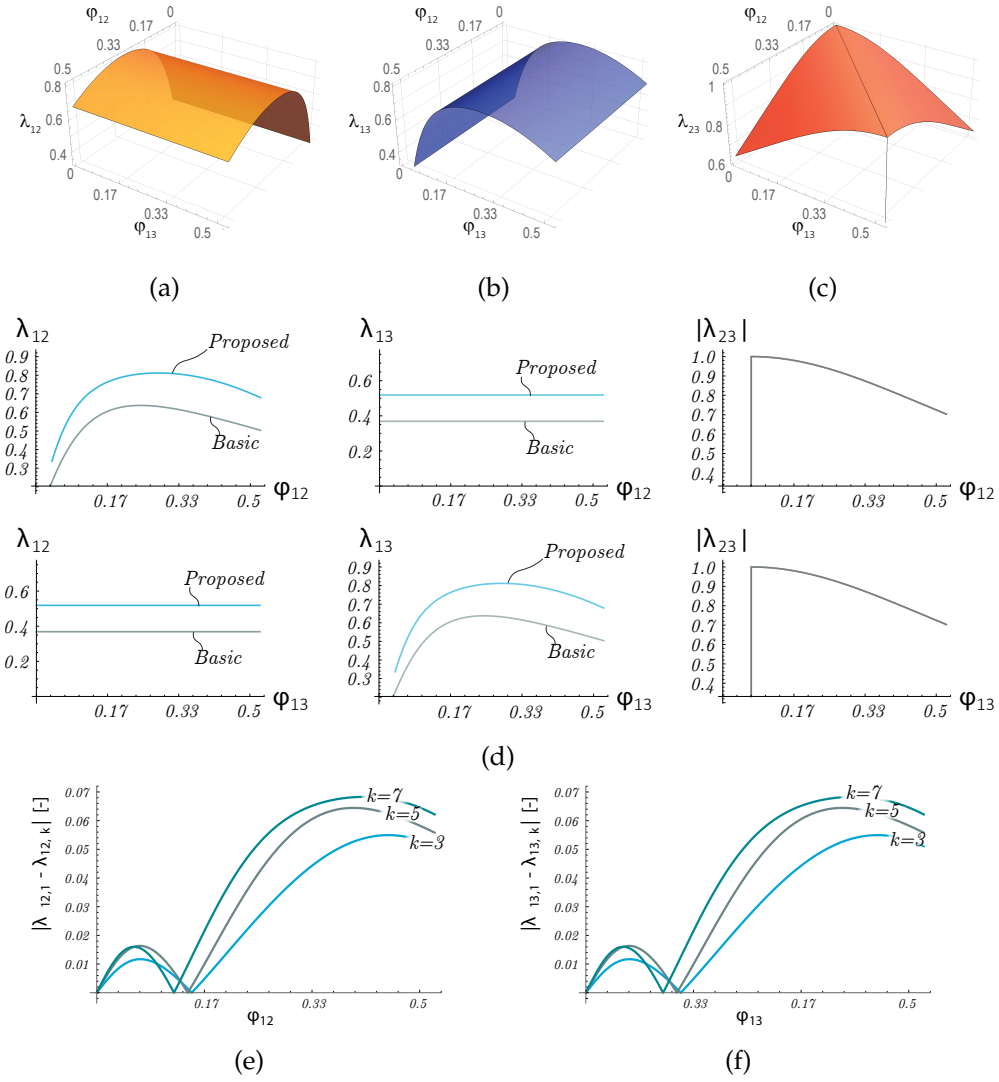


FIGURE 4.8: Power factors as function of outer phase-shift angles. The influence of the proposed modulation is shown in (d). The error introduced due to the use of fundamental only is shown in (e) and (f).

appropriately. As is visible in Fig. 4.7b when the voltage at port one is higher than voltage at ports two and three variation of α_1 leads to reduction of the rms current at port one. However, when the voltage at port one is smaller than the voltages at ports two and three then the same effect is achieved with variation of phase-shifts α_2 and α_3 as demonstrated by Fig. 4.7c and Fig. 4.7d.

TABLE 4.11: RMS values of port voltages and currents in delta convention.

Voltage	rms	Current	rms
v_1	$\sqrt{2}d_{1,r}V_1$	$i_{\sigma,12}$	$\frac{V_2}{L_{\sigma,12}\omega_s}\sqrt{\frac{d_{2,i}^2+(d_{2,r}-d_{1,r}m_{12})^2}{2}}$
v_2	$V_2^2\sqrt{\frac{\left(d_{2,i}^2+d_{2,r}^2\right)}{2}}$	$i_{\sigma,13}$	$\frac{V_3}{L_{\sigma,13}\omega_s}\sqrt{\frac{d_{3,i}^2+(d_{3,r}-d_{1,r}m_{13})^2}{2}}$
v_3	$V_3^2\sqrt{\frac{\left(d_{3,i}^2+d_{3,r}^2\right)}{2}}$	$i_{\sigma,23}$	$\frac{V_3}{L_{\sigma,23}\omega_s\sqrt{2}}\Big(d_{3,i}^2+d_{3,r}^2$ $+\left(d_{2,i}^2+d_{2,r}^2\right)V_2^2$ $+\left(d_{2,i}d_{3,i}+d_{2,r}d_{3,r}\right)m_{23}\Big)^{\frac{1}{2}}$

4.4.1 *Reactive Power Minimization*

As mentioned at the beginning of this section, too high rms current in the inductors does not only contribute to the active power transfer but largely contribute to the circulating power. Certain amount of reactive power is needed to meet the soft-switching conditions as presented in the previous section, however most of it contributes to conduction losses. Therefore, minimizing reactive power is important to achieve efficient operation. The reactive power is a combination of reactive power caused by voltage and current of the same frequency component and by the voltage and current of different frequency components. The ratio of active and apparent power can be a useful tool to describe the amount of reactive power that is circulating in the circuit alongside the active power. The closer the ratio is to 1, the less reactive power is in the circuit.

To calculate the power factor the active and apparent powers must be calculated. The fundamental active powers can be calculated as shown in (4.40)-(4.42). The apparent

power can be calculated from root-mean-square (rms) values of port voltages and corresponding currents. The fundamental power factors are then calculated as follows

$$\lambda_{12} = \frac{P_{12}}{v_{1,(rms)} i_{\sigma,12,(rms)}}, \tag{4.40}$$

$$\lambda_{13} = \frac{P_{13}}{v_{1,(rms)} i_{\sigma,13,(rms)}}, \tag{4.41}$$

$$\lambda_{23} = \frac{P_{12}}{v_{3,(rms)} i_{\sigma,23,(rms)}}. \tag{4.42}$$

The fundamental power factors are depicted in Fig. 4.8a, 4.8b and Fig. 4.8c. From the three surfaces it is clear that in delta-convention each power factor is only dependent on the respective phase-shift, i.e. λ_{12} is only a function of φ_{12}. Therefore the power factors are replotted in Fig. 4.8d. Figure 4.8d also shows the influence of varying the phases-shifts α_1,α_2 and α_3 on the power factors. The error that stems from using only the fundamental component for the analysis is shown in Fig. 4.8e and Fig. 4.8f. As Fig. 4.8d shows appropriate choice of phase-shifts α_1, α_2 and α_3 can increase the respective power factors and thus reduce the currents rms in the inductors.

In order to find the point with the smallest circulating power in the converter (4.40)-(4.42) need to be equated to 1. The equations than can be then solved for the voltage ratios resulting in following

$$m_{12} = \frac{d_{2,r}}{d_{1,r}}, \tag{4.43}$$

$$m_{13} = \frac{d_{3,r}}{d_{1,r}}, \tag{4.44}$$

$$m_{23} = \frac{d_{3,i}^2 + d_{3,r}^2}{d_{3,i} d_{2,i} + d_{3,r} d_{2,r}}. \tag{4.45}$$

The operation of TAB converter can be categorized based on the voltage ratios. The reactive power is minimized when the modulation ratios are chosen according to the smallest voltage in the system. The optimal duty cycles can be derived from (4.43)-(4.45) by assuming following

$$\cos(\varphi_{12}) \approx 1, \tag{4.46}$$

$$\cos(\varphi_{13}) \approx 1, \tag{4.47}$$

$$\cos(\varphi_{12} - \varphi_{13}) \approx 1. \tag{4.48}$$

The logic of assumptions (4.46)-(4.48) follows from the fact that the outer angles φ_{12} and φ_{13} after an inflection point reduce the power factor. Therefore, an optimal TAB design aims for small outer angles under rated conditions. The outer angles φ_{12} and φ_{13} are used to control transmission power while the duty ratios α_1, α_2 and α_3 are adjusted to decrease the circulating reactive power and increase the efficiency. Similar assumptions were used for DAB operation in [108].

TABLE 4.13: Near-optimal phase-shifts to minimize the reactive power.

Scenario	Optimal Duty Cycle
$V_1 < V_2 < V_3$, $V_1 < V_3 < V_2$	$\alpha_1 = 0$, $\alpha_2 = 2\arccos(m_{12})$, $\alpha_3 = 2\arccos(m_{13})$.
$V_2 < V_1 < V_3$, $V_2 < V_3 < V_1$	$\alpha_1 = 2\arccos\left(\frac{1}{m_{12}}\right)$, $\alpha_2 = 0$, $\alpha_3 = 2\arccos\left(\frac{1}{m_{13}}\right)$.
$V_3 < V_2 < V_1$, $V_3 < V_1 < V_2$	$\alpha_1 = 2\arccos\left(\frac{1}{m_{13}}\right)$, $\alpha_2 = 2\arccos(m_{23})$, $\alpha_3 = 0$.

It should be noted that the duty ratios as derived in Table 4.13 are not global optimums. Especially in the corner operating points when the power transfer is mostly consisting of higher frequency components the values can in fact increase the rms. However, as is visible from the Table 4.13 these expressions are easy to implement and give a good insight into operation of the converter. Moreover, no look-up tables or advanced co-processors are necessary to implement this type of control and the control as will be demonstrated give good overall performance.

4.4.2 *Rms reduction*

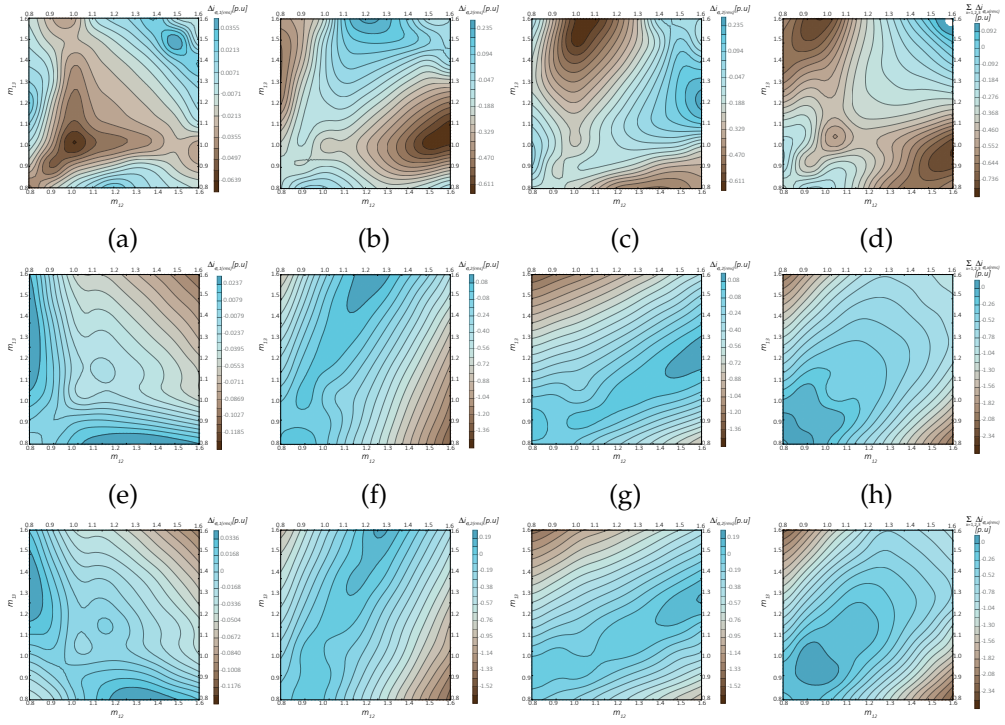


FIGURE 4.9: The simulated reduction of rms currents in p.u. The contour plots show the difference between the port rms currents when the proposed modulation is applied and when only phase-shifts φ_{12} and φ_{13} are used.

A detailed switching model was constructed in PLECS/Simulink. The influence of the proposed rms reduction control by modulating phase-shifts α_1, α_2 and α_3 is demonstrated in Fig. 4.9. The contour plots depict the difference in the rms values of the port currents when only phase-shifts φ_{12} and φ_{13} are used to control the converter

TABLE 4.15: Prototype Parameters

Parameter	Acronym	Value
HV MOSFET	S_{1-4}	C3M0030090K
LV MOSFET	S_{5-12}	IPB017N10N5
HV MOSFET Capacitance	$C_{oss,1-4}$	131 [pF]
LV MOSFET Capacitance	$C_{oss,5-12}$	1810 [pF]
Transformer ratio	N	7 [-]
Switching Frequency	f_{sw}	50 [kHz]
Primary Inductance	$L_{\sigma,1}$	106 [μH]
Secondary Inductance	$L_{\sigma,x}$	3 [μH]
Output Capacitance	$C_{out,x,x}$	1.22 [mF]
Primary Resistance	$R_{\sigma,1}$	206 [mΩ]
Secondary Resistance	$R_{\sigma,x}$	22 [mΩ]

and when all five degrees of freedom are used as proposed in Table 4.13. Expressed mathematically

$$\Delta i_{\sigma,x}^{(p.u)} = \frac{i_{\sigma,x}^{(proposed)} - i_{\sigma,x}^{(normal)}}{\frac{V_1}{L_{\sigma,12}\omega_s}}. \tag{4.49}$$

In each row are the results for one operating load point, i.e. in (a)-(d) the load is 0.9 p.u., in (e)-(h) the load is 0.45 p.u and in (i)-(j) the load is 0.3 p.u.. In the Fig. 4.9 the columns correspond to the ports, i.e. the first column from the left is port one, second column is port two and third column is port three. Fourth column from the left is the sum of all rms values $\Delta i_{\sigma,1}^{(p.u)} + \frac{\Delta i_{\sigma,2}^{(p.u)}}{N} + \frac{\Delta i_{\sigma,3}^{(p.u)}}{N}$. In all figures the output voltages are varied from 0.66 p.u. to 1.3 p.u. Clearly, the largest reduction of the rms current happens at small loads and when the port voltages are further away from unity. It can be observed that the results for port two and three are symmetrical as expected. An interesting observation can be made that while the total sum of rms currents is reduced, locally it can be slightly increased. This observation is in line with the comment about non-assurance of global optimum.

4.5 EXPERIMENT

4.5.1 *ZVS Analysis*

A prototype converter was assembled to confirm the analysis presented in the previous section. The prototype parameters are summarised in Table 4.15. Several operating

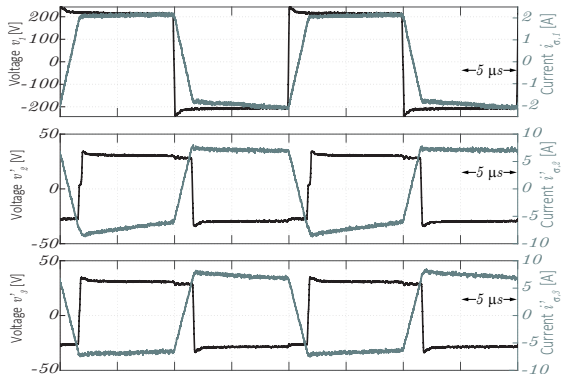


FIGURE 4.10: Operation of TAB converter at unity voltages and all halfbridges achieving ZVS. The phase-shifts φ_{12} and φ_{13} are 0.15π.

points were chosen to demonstrate ZVS and hard commutations. The chosen operating points are also highlighted in Fig. 4.4, Fig. 4.5 and Fig. 4.6. Figure 4.10 shows operation of TAB converter at unity port voltage ratios. In Fig. 4.10 all switches are soft-switched.

Since the three ports are symmetrical, showing the ZVS region for one port should be able to cover all the scenarios. Therefore, the analyzed ZVS regions for port one, shown in Fig. 4.12 (a)-(c) are verified, and the test results are shown in Fig.4.12 (d)-(f). The operating points of the test in Fig.4.12 (d)-(f) are marked in Fig. 4.12(a)-(c), respectively. The test results show MOSFET drain-source voltage, gate-source voltage, port ac voltage, and current, which can be used to identify whether the two legs of port one are in ZVS or not. For instance, the test in Fig. 4.12(e) shows that the leading leg (S2) is in ZVS, while the lagging leg (S4) is out of ZVS, which matches the analysis in Fig. 14(b) very well. Similarly, it can be seen the test results in Fig. 4.12(d) and (f) also match the analyzed ZVS region in Fig. 4.12(a) and (c) well.

First the ZVS operation of the converter when voltage ratios are $\frac{2}{3}$ and $\frac{4}{3}$ for m_{12} and m_{13} respectively are shown in Fig. 4.12. The operating point shown in Fig. 4.12a is also marked in Fig. 4.4a. It is clear that port with the smallest voltage does not have soft-switching transition as the current during the transition has the opposite polarity. Similarly, ZVS is not achieved at port one, as the current is just crossing zero during the commutation. Next operating point is shown in Fig. 4.12b marked in Fig. 4.6e. Port with the highest voltage is soft-switched, port with the smallest voltage is hard-switched as shown by the current polarity. At port one, the leading half-bridge achieves ZVS. However, the lagging half-bridge is hard switched as the current changes polarity during the time of phase-shift α_1. Last operating point shown for various voltage ratios is in Fig. 4.12c and shown in Fig. 4.4g. As expected when the phase-shifts are large even for significantly different voltages, a complete ZVS operation can be achieved on ports two and one. However, the current at port three is still too small to achieve soft-switching.

Figure 4.13 confirms the effect of phase-shift α_1 when voltage ratios $m_{12} = m_{13}$ are $\frac{4}{3}$. Figure 4.13a shows operating point marked in Fig. 4.5a and Fig. 4.5e. In the experimental results, the currents are already reversed on all three ports. Figures 4.5b

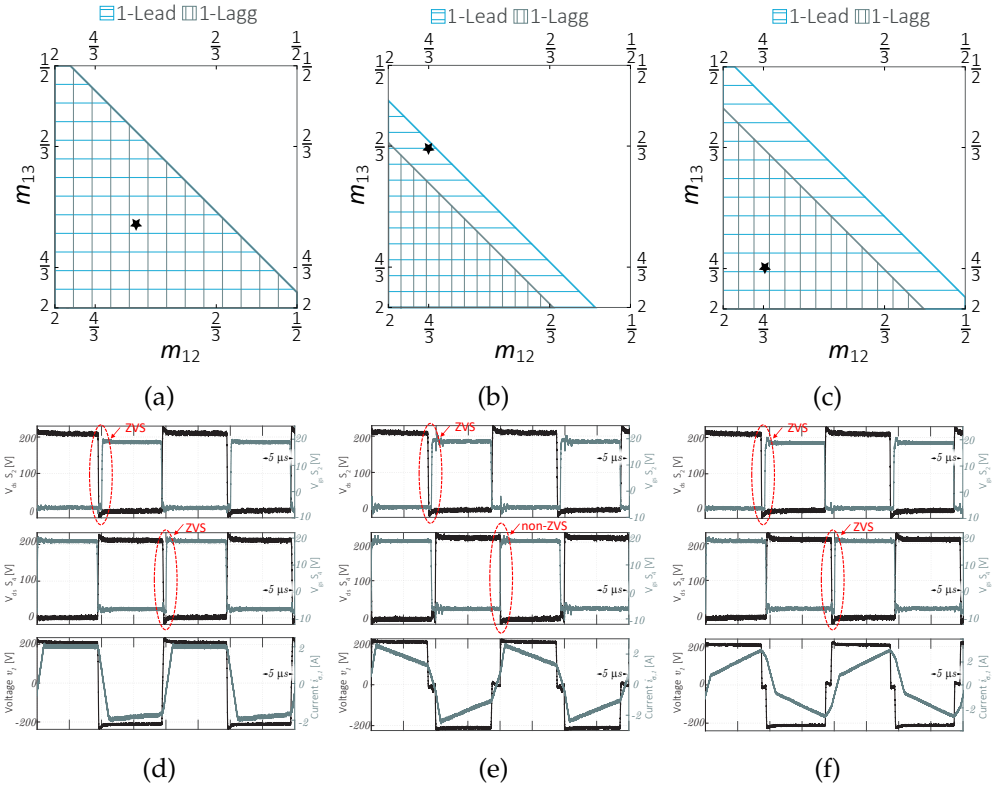
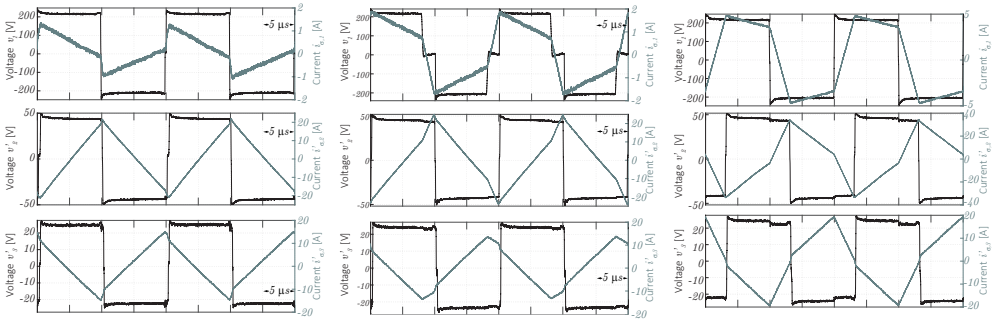


FIGURE 4.11: Calculated zero voltage switching areas of port 1 with: (a) $\alpha_1 = 0$ and $\varphi_{12} = \varphi_{13} = 0.15\pi$; (b) $\alpha_1 = 0.08\pi$ and $\varphi_{12} = \varphi_{13} = 0.1\pi$; and (c) $\alpha_1 = 0.08\pi$ and $\varphi_{12} = \varphi_{13} = 0.2\pi$. The ZVS areas are validated by testing shown in: (d) as a verification of (a); (e) as a verification of (b); (f) as a verification of (c). Note: The operation points of the test in (d) (e) (f) are marked as a star in (a) (b) (c), respectively.

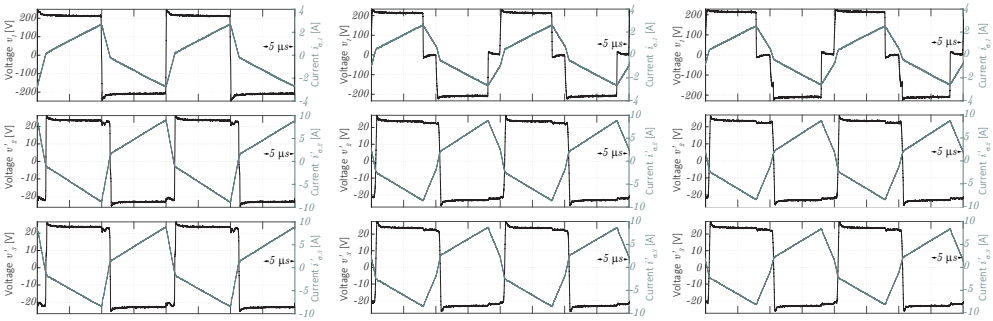
and 4.5f mark the operating point measured in Fig. 4.13b. Port one achieves ZVS, even at the lagging port. Port two and three show that the current had enough time to cross zero before the commutation and the current is higher at the end of commutation than it was in the previous case and ZVS transition is achieved. The last operating point marked in Fig. 4.5c and Fig. 4.5g is shown in Fig. 4.13c. At these operating points, the current at ports two and three had time to change polarity before commutation. However, the current at port one, when the lagging phase-leg commutates, changes polarity. This leads to a hard transition, thus increasing losses and electromagnetic interference.

Last operating point verified is shown in Fig. 4.14 when voltage ratios are $m_{12} = m_{13} = \frac{2}{3}$, in this set of experimental results the effect of phase-shifts α_2 and α_3 are verified. Starting with operating point marked in Fig. 4.6a, 4.6d, 4.6g is shown in Fig. 4.14a where port one does not achieve ZVS as clearly the current has opposite polarity as needed. However, ZVS is smoothly achieved on port two and three. The



(a) (b) (c)

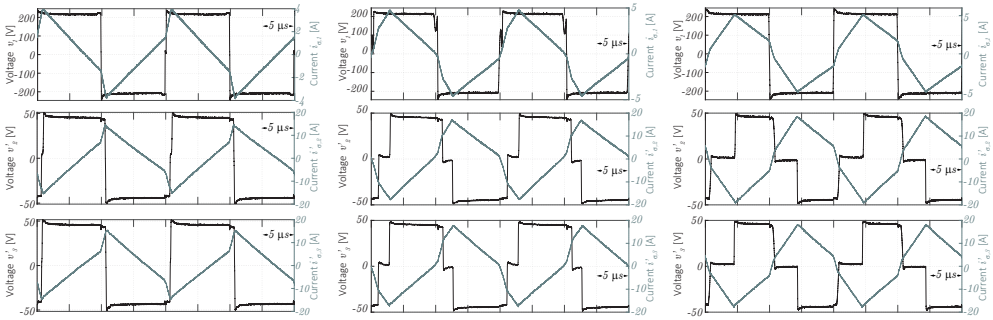
FIGURE 4.12: Measured commutations of ports when m_{12} is $\frac{2}{3}$ and m_{13} is $\frac{4}{3}$. In (a) φ_{12} and φ_{13} are 0.05π. In (b) φ_{12} and φ_{13} are 0.15π and α_1 is 0.15π. In (c) φ_{12} and φ_{13} are 0.3π



(a) (b) (c)

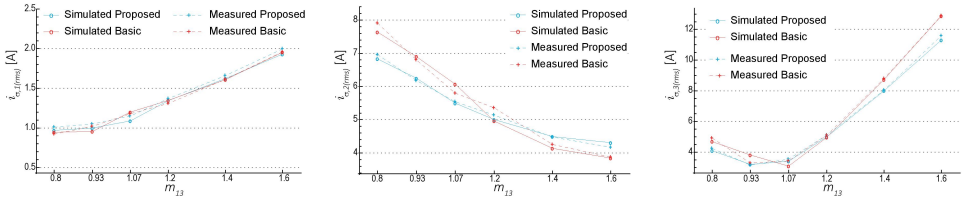
FIGURE 4.13: Measured commutations of ports when voltage ratios $m_{12} = m_{13}$ are $\frac{4}{3}$. In (a) φ_{12} and φ_{13} are 0.1π.In (b) φ_{12} and φ_{13} are 0.15π and α_1 is 0.2π. In (c) φ_{12} and φ_{13} are 0.15π and α_1 is 0.25π.

effect of introducing phase-shifts α_2 and α_3 is shown in Fig. 4.14b, this operating point is marked in Fig. 4.6b, 4.6e, 4.6h. It can be observed that current at port one is crossing zero during commutation; thus, double transitions are occurring. However, at these operating points, ZVS is kept on all switches on the secondary ports. It is clear why achieving ZVS for the lagging half-bridges on ports two and three are easier than for the leading half-bridges. The current has more time to rise. This effect is even stronger for the operating point shown in Fig. 4.14c which is marked in Fig. 4.6c, 4.6f, 4.6i. Clearly, at this operating point, it is possible to achieve ZVS at port one as the commutation occurs before the current reverses polarity and no hard commutations occur. However, at ports two and three, it is clear that the current during commutation of the leading half-bridges is still very small compared to other transitions. The small current amplitude leads to breaking of the energy condition and



(a) (b) (c)

FIGURE 4.14: Measured commutations of ports when voltage ratios $m_{12} = m_{13}$ are $\frac{2}{3}$. In (a) φ_{12} and φ_{13} are 0.1π. In (b) φ_{12} and φ_{13} are 0.2π and α_1 is 0.15π. In (c) φ_{12} and φ_{13} are 0.25π and α_1 is 0.4π



(a) (b) (c)

FIGURE 4.15: Measured and simulated rms transformer currents for operation at $f_s = 50$ kHz at load 0.45 p.u.. In (a) is the rms current of port one, in (b) is the rms current of port two and in (c) is the rms current of port three.

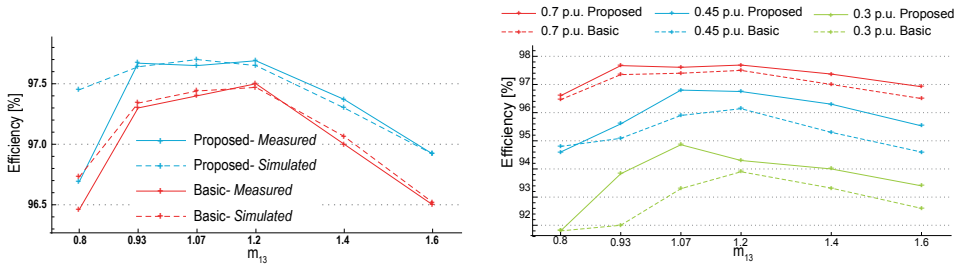
hard transition for the leading half-bridges. On the other hand, the lagging phase-legs undergo soft transitions as the current had enough time to rise.

4.5.2 *Reactive Power*

In this section the transformer current rms values are validated to strengthen the conclusions achieved in the previous section. These results also demonstrate the reduction of the rms. Efficiency of the prototype is also provided at different operating points. The efficiency measurements is meant as a case study demonstrating the positive effect of the proposed modulation. Moreover, a calculated loss breakdown is provided in this section to present where the operation is improved the most.

4.5.3 *RMS Current*

The rms values of transformer currents are compared in Fig. 4.15 measured at load 0.45 p.u.. The measurement was done when the voltage at port two was held constant



(a) (b)

FIGURE 4.16: In (a) is the comparison of calculated and measured efficiencies for the loss breakdown at load 0.7 p.u.. In (b) are the efficiencies of the prototype at different load points.

at 0.83 p.u. while the voltage at port three was varied from 0.625 p.u. to 1.2 p.u.. Figure 4.15a shows the rms values of the transformer current at port one. The blue curves mark the currents measured when the proposed modulation techniques is used, while the red when only basic phase-shift control is applied. The simulated curves are solid, while the measured are dashed. The points marked with "*o*" are simulated while those marked with "+" are measured. Figure 4.15b shows the rms values of current at port two and Fig. 4.15c are rms values of transformer current at port three. The figure shows good match in all operating points. The error seems to be slightly higher for current at port two. However, this is due to small amplitude and thus increase sensitivity to measurement error. Small mismatches occur around the unity voltage. This is due to the fact that in laboratory prototype, the effective turns ratio is never precise and the same can be said about the inductances, which can change due to small movement of the winding during manipulation.

4.5.4 *Efficiency & Loss Breakdown*

The proposed steady-state control which is designed to increase the inductor network power factor results in higher overall efficiency. The efficiency of the prototype was measured with the power analyser Yokogawa PWT-500. The efficiency measurement at different loads and voltage ratios are in Fig. 4.16b. It can be seen that the proposed modulation increases the efficiency by up to 2% depending on the operating point. The highest gains are achieved for highly unbalanced port voltages as expected from the analysis in previous section. There is a single point at which at light loads the efficiency is not increased and there is a discrepancy between the simulation and experiment. As mentioned earlier and shown in the measured waveforms, the double transition can occur when extra phase-shifts are introduced. The double transition leads to an increase of the losses especially on port one which has highest voltage. A comparison of measured and calculated efficiency at load 0.7 p.u. is in Fig. 4.16a.

At times, it can be interesting to observe how the losses are distributed in a converter. For this purpose detailed models of switches and magnetic components were

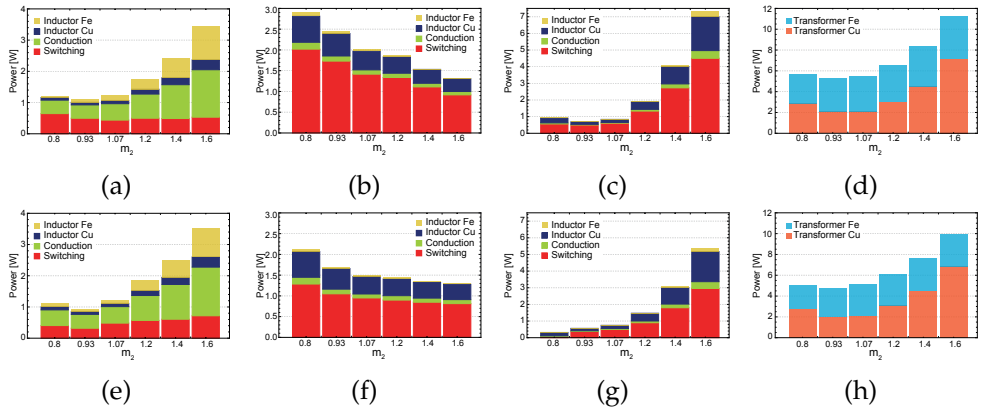


FIGURE 4.17: Loss breakdown comparison of the basic and the proposed modulation.

constructed in PLECS. The calculated loss breakdown is shown in Fig. 6.4c for the operating points at load 0.7 p.u. and m_{12} fixed at 1.2. The efficiency measurements were done for the voltage at port two held constant at 1.2 p.u. while the voltage at port three was varied from 0.8 p.u. to 1.6 p.u.. From Fig. 6.4c it can be observed that switching losses are minimized due to the soft-switching that is gained with the proposed modulation. The main contribution of losses is the transformer. However, comparing the losses with proposed modulation it can be observed that the losses in high-frequency transformer can be reduced. These losses drop significantly due to the reduction of the discrepancy between the voltages applied to the transformer. Furthermore, the switching and conduction losses are reduced on both port one and port three. The only port that slightly increases losses is port two. This is the case when the voltage at port three is much higher than that on port two. This is a logical consequence of the slight increase of the corresponding rms current at that port at these operating points. It should be noted however, that port two addition to the overall losses is small.

4.6 CONCLUDING REMARKS

The chapter derives the zero voltage switching (ZVS) criteria of the triple active bridge (TAB) converter using Fourier series expansion. Closed-form solutions are summarised and used to investigate the influence of different practical design aspects on the soft-switching regions, including the dc side voltage ratio, the phase shift between ports, and the internal phase shift of each port.

A significant advantage of the derived ZVS criteria is that the effect of parasitic capacitors is considered, ensuring complete commutation of each phase-leg. In general, the port with higher voltage can achieve ZVS easier. Phase shift inside the full bridge can be applied to the port with higher voltage so that the ZVS region of the ports with lower voltage will be enlarged. However, the cost is a reduction of the ZVS region of the port with non-zero internal phase shift, and to be more specific, the ZVS region

of its lagging leg if the port is sourcing power, or leading leg if the port is absorbing power. Experiments on a laboratory prototype then verify the closed-form solution of the ZVS and the theoretical analysis. The derived ZVS criteria present a powerful tool to study the operation of TAB converter and further optimisation of its operation. Moreover, the approach outlined in the paper can be generalised to any phase-shift operated n-port topology.

Secondly, in this chapter the losses that are caused by the circulating current in the high-frequency link of the TAB converter are investigated. A simple modulation that uses all five degrees of freedom is proposed and verified experimentally. A simulation study shows in which operating points the efficiency gains are highest. Moreover, a calculated loss breakdown provides an insight about converter loss distribution. The loss distribution reveals that significant part of the losses in the prototype are in the transformer, therefore reducing the rms of the transformer currents is an effective tool in achieving higher operating efficiency.

Part III

PROTECTION

5

SOLID-STATE CIRCUIT BREAKER: DESIGN CRITERIA

This chapter derives solid state circuit breaker (SSCB) design criteria that consider the effect of different detection methods with different detection delays under varying system constraints. The design space is investigated in a sensitivity analysis, which provides insights into the operation boundaries of SSCB and explains how a combination of fault detection methods can reduce the SSCB size. SSCB prototype is developed and tested in different scenarios under nominal grid voltage and current. The derived design constraints can be used not only for efficient SSCB design but also to evaluate the effects of different protection schemes on the required SSCBs.

This chapter is based on:

J3 P. Purgat, N. van der Blij, Z. Qin, P. Bauer-*"Design Criteria of Solid-state circuit breakers in LVDC Grids", IET Power Electronics (under review)*

5.1 INTRODUCTION

A conceptual LVDC microgrid relying on solid-state protection is shown in Fig. 5.1. The LVDC microgrid is connected to the medium voltage dc (mvdc) grid via a step-down isolated dc/dc converter such as as [109]. Using the solid-state circuit breaker (SSCB) on the low voltage side to protect the substation is favourable compared to implementing the protection on the mvdc side as the SSCBs do not have to be rated for very high overvoltages. The houses are connected to the microgrid via SSCBs; the power flow in the grid can be controlled with power flow control converters such as described in Chapter 2. Inside the house, several protection groups can be defined similarly as is done in the contemporary electric installations.

5.1.1 *Challenges & Requirements of LVDC System Protection*

The short-circuit protection of LVDC systems has several peculiarities compared to ac based counterparts. The dc networks are usually highly capacitive and have comparably small inductances, as a result of using predominantly voltage source converters [37]. Consequently, in a low impedance grounded LVDC system during the short-circuit fault, the voltage on the fault drops rapidly, and the short-circuit current rises rapidly. Furthermore, the short-circuit current in a dc system can be strengthened by the constant power source behaviour of some nodes [110]. Due to the fast and violent short-circuit transient behaviour and because the assumption that the converters can implement complete short-circuit isolation is not always true [48], the consensus for

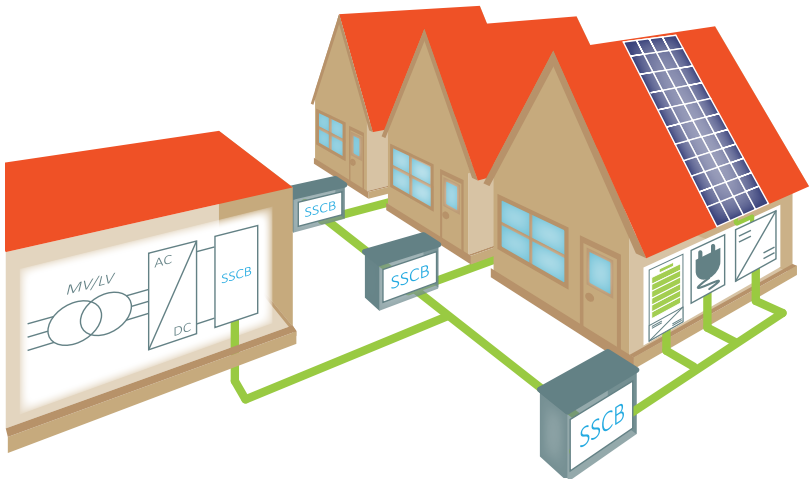
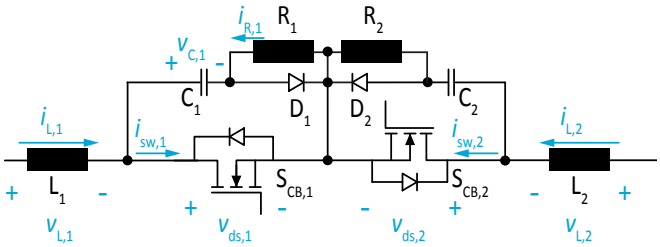


FIGURE 5.1: LVDC microgrid protection concept. Direct current houses can be connected to the network via SSCBs instead of fully rated dc/dc converters to make the system more efficient. The power flow in the grid can be controlled with power flow control converters as described in Chapter 2 of this thesis.



(a)

FIGURE 5.2: SSCB topology used in this thesis and investigated in this chapter.

LVDC protection converges to two solutions: hybrid circuit breakers (HCB) [45] and SSCBs [46], [47].

The main advantage of the HCBs are the small on-state losses; one of the main HCBs limitations is the reliability of the mechanical part caused by the mechanical contact erosion [45]. The HCBs open short-circuits in the range of milliseconds, which is significantly faster than the traditional circuit breakers. However, for low power microgrids with small nominal operating currents, the fault clearing periods in the range of milliseconds can result in short-circuit current peaks hundreds thousands of times higher than the nominal currents [111]. Peak current amplitudes then lead to significant oversizing of all the grid components [112]. Therefore, for small dc nanogrids or microgrids, fast SSCBs are preferred [C6].

One of the main challenges regarding the use of the SSCBs are the on-state losses [113], [114]. A popular choice for SSCBs are Si IGBTs [46], Si MOSFETs [C6] and their SiC counterparts. IGCT based solutions prove to be more efficient in systems with a nominal current in the range of kA [115]. MOSFETs have limited minimum voltage breakdown amplitude compared to the IGBTs.In case of SSCB, the conduction losses are of paramount importance. In MOSFETs, they are defined by a classical resistance; in IGBTs, there is a fixed conduction loss determinator in the form of a knee voltage plus a differential resistance of the output characteristic. Therefore, the conduction losses of an SSCB based on MOSFETs can be reduced almost arbitrarily by paralleling of MOSFETs. However, when IGBTs are used the conduction loss limit remains at the knee voltage regardless of the number of devices used. The use of MOSFETs can improve the efficiency of the SSCB in terms of energy and cost in systems with smaller operating voltages and currents [C6]. The emerging SiC MOSFETs are a promising technology for the use in SSCB. However, they are likely to suffer the highest short-circuit current relative to their chip size due to the intrinsic properties of the SiC BJT [116], [117]. Therefore, the short-circuit detection time is very crucial when SiC MOSFETs are used in SSCB. Furthermore, the higher the short-circuit current, the higher the voltage spike after the opening of the SSCB; as a result, snubber circuits size becomes significant [46], [118].

The time the SSCB requires to open a short-circuit is in the range of several μs. Therefore the short-circuit detection time becomes a significant part of the entire short-

circuit clearing time. Moreover, as discussed above the Si and especially SiC-based devices are sensitive to overcurrent and overvoltage. Therefore, the design of the short-circuit detection must ensure that the SSCB always meets the system requirements, ensure that the SSCB always operates within its safe operating area and meets the cost criteria. The SSCB topology used in this study is in Fig. 5.2a, with three distinct short-circuit detection mechanisms. The slowest mechanism is a thermal protection which is also used in today's electromechanical circuit breakers. The faster protection during short-circuits is provided by the overcurrent detection and a complementary rate of change of current (ROCOC) detection. The role of the overcurrent detection is to detect short-circuits that are further away from the SSCB and are characterised by higher fault inductance. The overcurrent detection is implemented via drain-source voltage measurement. The drain-source voltage monitoring was chosen as this method does not introduce any further losses and does not have a tight bandwidth limit. However, when the short-circuit occurs at the terminals of the SSCB, use of overcurrent detection only can result in destruction of SiC switches. Therefore a complementary ROCOC detection is implemented, that improves the SSCB performance in the cases with zero external inductance.

5.1.2 *Previous Work*

The main goals of protection systems are detection, location and isolation of faults [8]. To successfully meet these three goals, knowledge about the system and its behaviour is necessary. In [119], a simple short-circuit current calculation method based on the Laplace transform neglecting the node capacitor is proposed. A generalised approach, suitable for meshed dc systems, is presented in [120]. However, the matrices are not directly suitable for threshold selection. A model providing an insightful expression of the short-circuit currents was derived in [121], and another simple approach for LVDC was proposed in [119]. A unit-based protection was proposed for LVDC systems in [37] and [38]. The unit-based protection relies on communication and generally takes several milliseconds to detect a fault. While such delays are acceptable for high power systems, it is likely that in LVDC small power systems unit-based protection would have several unwanted consequences. Firstly, the system needs to be able to supply the short-circuit current for a prolonged period. Secondly, all components including cables, source converters and circuit breakers would need to be rated for higher short-circuit currents. The resulting oversizing would make the system less efficient and more expensive. Therefore, approaches not relying on communications are more interesting for small dc systems like the one shown in Fig. 5.1. Non-unit based protection using $\frac{\mathrm{d}i}{\mathrm{d}t}$ was proposed in [41] and [42]. In both cases, the protection scheme is tested only with simulation and under the assumption of very high ADC sampling speeds, which increases the cost of the SSCB. Other non-unit based protection approaches rely on over-current or under-voltage threshold [43, 44]. Combination with external circuitry that can inject known frequency to detect high impedance faults is proposed in [122]. The reported works do not consider the effect of the detection methods on the design of the protection devices and validate the results with simulation studies.

While on the system level, the research is focused on coordination and selectivity in complex network topologies, on the device level, the research is focused on the development of autonomous and cost-efficient topologies [123] and functionalities [124]. In [123] the design of a cost-efficient solution based SiC JFET is investigated. The main advantage is the combination of a detection circuit with an auxiliary power circuit, which enables self-powering of the SSCB during the fault. The circuit from [123] was studied to increase its blocking voltage capability in [125] and to increase its current carrying capability in [126]. However, the use of normally-on devices can be deemed dangerous in applications where humans can come into contact with the live circuit, and the touch potential is higher than the "*let go*" threshold. For systems with high nominal currents novel topologies that introduce fault current limiting are investigated [47, 127]. An essential aspect of SSCB design is overvoltage suppression. Different overvoltage snubbers are described in [46]. Further, SSCBs are equipped with extra functionalities such as fault location or adjustable trip curves. Depending on a system structure, the upstream and downstream position of an SSCB is relative to a fault location. An SSCB can be upstream at one fault location but downstream at another location. Therefore, the threshold of SSCB in such system should be adjustable and can be set to different values according to its sensed power flow direction [39]. The fault location functionality is usually achieved with current injection at a known frequency [128], [129]. However, the proposed fault location techniques introduce more components and make the clearing process longer.

5.1.3 *Contribution*

The main contributions of this chapter are the derivation of the design criteria of SSCB for LVDC grid that take into consideration the effects of different short-circuit detection methods, sensitivity analysis of SSCB design space and development of a SSCB prototype. The design space of the SSCB is analysed in a sensitivity study that highlights the limits and potential of the SSCB use in LVDC grid. A prototype SSCB is designed and developed. The SSCB prototype ability to effectively interrupt short-circuits with minimal delay time is validated in experiments with varying loop inductance. The SSCB prototype ability to avoid spurious tripping during large load steps is also validated. The experiments are not scaled down, i.e. the experiments are done at nominal grid voltage and current levels.

5.1.4 *Organization*

The rest of the chapter is organised as follows. Section 2 investigates the SSCB operation and derives the design criteria. Section 3 contains a sensitivity analysis of the SSCB design space, highlighting the effect of different detection methods and detection delay time. Section 4 presents experimental results. Section 5 closes the chapter with a summary and an outlook on future work.

5.2 SSCB OPERATION ANALYSIS

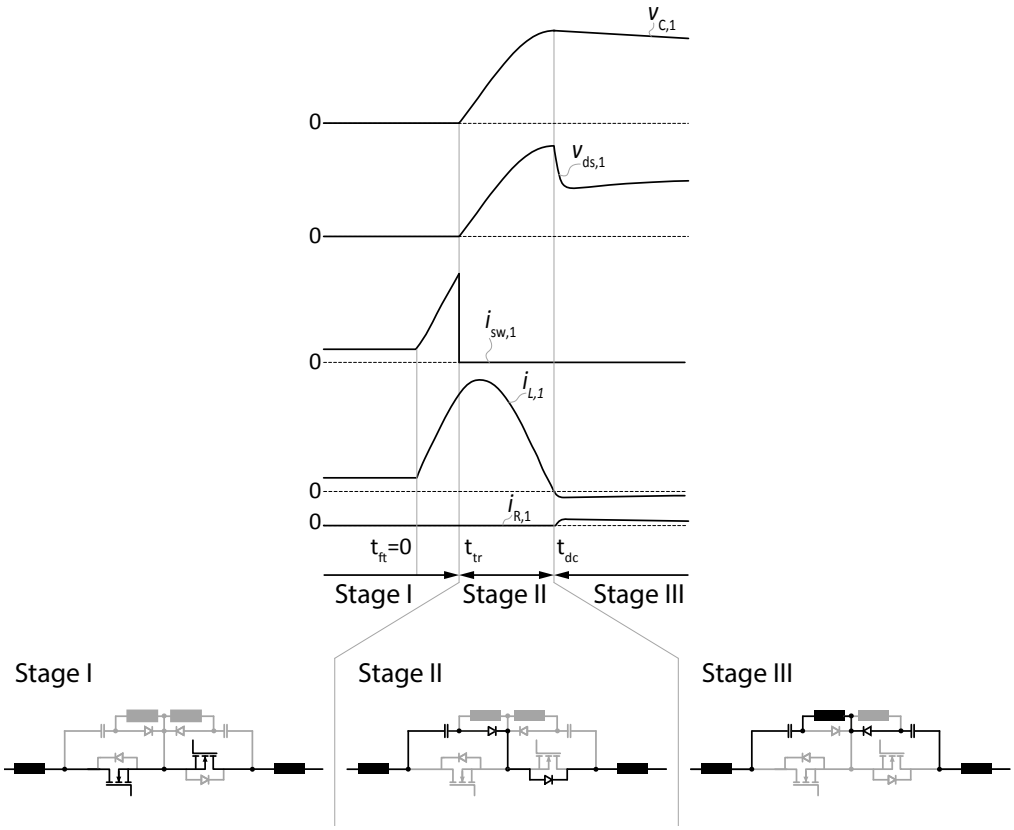


FIGURE 5.3: SSCB operation during the fault clearing. Stage 1 starts after the fault occurance and the circuit is dominated by the inductance. Stage 2 starts after the SSCB MOSFETs are opened and is characterized by charging of the snubber capacitor. The last stage is the discharge of the snubber capacitor.

The line-to-ground fault and line-to-line fault are the two main types of short-circuiting. The line-to-ground fault is formed when either the positive or negative phase touches the ground, while the line-to-line fault occurs when a low impedance connection between the phases of the system is formed. In the case of low resistance grounded systems, both faults have similar behaviour that is characterized by the large currents and fast $\frac{di}{dt}$; therefore both can be approximated by the bolted fault [130].

5.2.1 *SSCB Operation Analysis*

The operation of the SSCB during a bolted fault can be divided into three distinct stages shown in Fig. 5.3. In the operation analysis it is assumed that the capacitance

of the short-circuit current source is sufficiently large and during the short-circuit it appears as an ideal voltage source V_{DC}, the short-circuit current is characterized by the inductance between the source and the loop L_{total} and by the fault impedance R_{SC} (for bolted fault $R_{SC} \to 0$). The loop inductance L_{total} is a sum of the SSCB current limiting inductances L_1, L_2 and any additional inductance present in the loop $L_{ext.}$. The parasitic line capacitance in the LVDC systems is in general very low and is neglected.

Figure 5.3 shows that after the fault occurs in Stage 1 the current flows through the SSCB MOSFETs. The Stage 1 is bounded by the time of the fault $t_{ft} = 0$ and turn-off of the SSCB MOSFETs t_{tr}. In the first stage the circuit is described by a first-order differential equation

$$L_{total}\frac{d}{dt}i_{L,1}(t) = V_{DC} - \underbrace{R_{SC}i_{L,1}(t)}_{V_{SC}\to 0}, \tag{5.1}$$

where $i_{L,1}$ is the current through the inductor and equals the short-circuit current. The voltage across the capacitor C_1 in the first stage is assumed to be

$$v_{C,1} = v_{ds,1} \approx 0. \tag{5.2}$$

The solution of the first-order system in the time domain is

$$i_{L,1}(t) = I_{L,o} + \frac{V_{DC}}{L_{total}}t, \tag{5.3}$$

where $I_{L,1}(0) = i_{L,1}(t_{ft})$ is the current at the time of the fault occurrence.

After the short-circuit passes defined threshold, the SSCB turns-off the MOSFETs and Stage 2 starts. Stage 2 is bounded by the turn-off of the SSCB MOSFETs t_{tr} and the time when the snubber capacitor starts to discharge into the snubber resistor t_{dc}. As shown in Fig. 5.3, the current commutes to the snubber diode and starts charging the snubber capacitor C_1. In the analysis it is assumed that the diode is ideal and the commutation from MOSFET to snubber diode is instant. The circuit is described by two differential equations

$$L_{total}\frac{d}{dt}i_{L,1}(t) = V_{DC} - v_{C,1}(t) - \underbrace{R_{SC}i_{SC}(t)}_{V_{SC}\to 0}, \tag{5.4}$$

$$C_1\frac{d}{dt}v_{C,1} = i_{L,1}(t). \tag{5.5}$$

Moreover, the initial conditions are

$$\begin{aligned} i_{L,1}(t = t_{tr}) &= I_{L,o} + \frac{V_{DC}}{L_{total}}t_{tr}, \\ v_{C,1}(t = t_{tr}) &= 0. \end{aligned} \tag{5.6}$$

The current and voltage are a solution of the second-order system (5.4)-(5.5) and are

$$i_{L,1}(t) = A\cos\left(\omega\left(t - t_{tr}\right) + \varphi_1\right), \tag{5.7}$$
$$v_{C,1}(t) = B\sin\left(\omega\left(t - t_{tr}\right) + \varphi_1\right) + V_{DC}, \tag{5.8}$$

where

$$A = \sqrt{\left(I_{L,o} + \frac{V_{DC}}{L_{total}}t_{tr}\right)^2 + \frac{C_1}{L_{total}}V_{DC}^2} \quad \text{and} \quad B = \sqrt{\frac{L_{total}\left(I_{L,o} + \frac{V_{DC}}{L_{total}}t_{tr}\right)^2}{C_1} + V_{DC}^2},$$
$$\omega = \frac{1}{\sqrt{L_{total}C_1}} \quad \text{and} \quad \varphi_1 = -\arcsin\left(\sqrt{\frac{1}{1 + \frac{\left(I_{L,o} + \frac{V_{DC}}{L_{total}}t_{tr}\right)^2}{\omega^2 C_1^2 V_{DC}^2}}}\right). \tag{5.9}$$

During stage 3 the snubber capacitor is discharged via the snubber resistor, thus $v_{C,1}$ will decrease and $i_{L,1}$ will also be very small due to the snubber resistor dumping. Therefore, stage 3 is omitted in the analysis.

5.2.2 *Design Constraints*

Different detection methods have different time delays and have an influence on the design parameters. The main parameters of interest are the peak values of the short-circuit current, the peak overvoltage on the blocking MOSFET of the SSCB and the total fault clearing time.

5.2.2.1 *Overcurrent Dection*

Overcurrent dection uses threshold of the current I_{th} to detect fault. Once the measured current reaches the threshold, the MOSFET is turned-off. However, in reality there is always a delay T_d between the time the current reaches the threshold and the time the MOSFETs open t_{tr}. The delay effect can be taken into account by rewriting (5.3)

$$\underbrace{i_{L,1}(t_{tr})}_{I_{th.}} = I_{L,o} + \frac{V_{DC}}{L_{total}}t_{tr}, \tag{5.10}$$

and the actual time of SSCB MOSFET turn-off can be obtained from

$$t_{tr} = T_d + \frac{L_{total}}{V_{DC}}\left(I_{th} - I_{L,o}\right), \tag{5.11}$$

then the current at the trip time is

$$i_{L,1}(t_{tr}) = I_{th.} + \frac{V_{DC}}{L_{total}}T_d. \tag{5.12}$$

The time when the peak voltage is reached is the time when current passes zero for the first time can be found by investigating eq. (5.7) and is

$$t_{dc} = t_{\text{tr}} + \frac{1}{\omega}\left(\frac{\pi}{2} + \varphi_1\right). \tag{5.13}$$

During the short-circuit surge energy is supplied. This energy can be dissipated in components both in the SSCB and in the faulted system. Thus it is directly proportional to the self-hating of the system and system components during the fault. The energy that is dissipated during the fault is defined as

$$E_{\text{sg}} = r\int_{t_{\text{ft}}}^{t_{\text{dc}}} i_{\text{L},1}^2(\tau)\,\mathrm{d}t, \tag{5.14}$$

where r is a system-dependent parameter; it represents the equivalent resistance of the line and the line components. This parameter can be used as an abstract measure of the distance of the fault (or line length), as was done for example in [131]. The inductor current is chosen for the definition, as this current flows through the system, the semiconductors and the overvoltage surpassing circuit for the entire duration of the fault. Since r is component-specific, the design constraint can be obtained as a surge energy index, defined as

$$E_{\text{ds}} = \frac{E_{\text{sg}}}{r} = \int_{t_{\text{ft}}}^{t_{\text{dc}}} i_{\text{L},1}^2(\tau)\,\mathrm{d}t = \int_0^{t_{\text{tr}}} i_{\text{L},1}^2(\tau)\,\mathrm{d}t + \int_{t_{\text{tr}}}^{t_{\text{dc}}} i_{\text{L},1}^2(\tau)\,\mathrm{d}t. \tag{5.15}$$

Substituting (5.13), (5.11) and (5.12) into (5.15) the energy index is obtained as

$$E_{\text{ds}} = \frac{I_{\text{th.}}^2\tau_{\text{SSCB}}}{k_1^2}\left(\frac{k^3}{3} + \frac{\pi}{4}\left(1+k^2\right) + \frac{1}{2}\left(1+k^2\right)\arctan\left(\frac{1}{k}\right) - \frac{k}{2}\frac{\left(3k^2-1\right)}{1+k^2}\right). \tag{5.16}$$

where

$$\tau_{\text{SSCB}} = \sqrt{L_{\text{total}}C_1}, \tag{5.17}$$

$$k_1 = \frac{Z_{\text{SSCB}}}{Z_{\text{sys}}} = \frac{L_{\text{total}}}{C_1}\frac{I_{\text{th.}}}{V_{\text{DC}}}, \tag{5.18}$$

$$k_2 = \frac{T_d}{\tau_{\text{SSCB}}} = \frac{T_d}{\sqrt{L_{\text{total}}C_1}}, \tag{5.19}$$

$$k = k_1 + k_2. \tag{5.20}$$

The peak voltage for the overcurrent detection can be rewritten using (5.18)-(5.20) as

$$V_{\text{C},1,\text{max}} = V_{\text{ds},1,\text{max}} = V_{\text{DC}}\sqrt{1+k^2} + V_{\text{DC}}. \tag{5.21}$$

The maximum current can be found by substituting (5.12) into (5.7), and written using (5.18)-(5.20) as

$$I_{\text{L},1,\text{max}} = I_{\text{th.}}\frac{\sqrt{1+k^2}}{k_1}. \tag{5.22}$$

5.2.2.2 *Rate of change of current detection*

Rate of change of current detection is implemented by measuring the voltage drop $v_{L,1}$ on L_1. The peak voltage, peak current and surge energy constraints are different for this detection method compared to the threshold current detection. The condition for tripping of the detection is

$$v_{L,1}\left(t = t_{ft}\right) = V_{dc}\frac{L_1}{L_{total}} \geq V_{L,th}. \tag{5.23}$$

The condition for tripping of the rate of change current detection expressed in (5.23) does not require the current to rise to $I_{th.}$ instead it is tripped when the current is $I_{L,o}$. However, the detection circuit still introduces delay T_d, which is considered.Therefore, in the equations for the ROCOC detection the threshold current is replaced with $I_{L,o}$. The time when the capacitor discharge starts can be then written as

$$t_{dc} = T_d + \frac{1}{\omega}\left(\frac{\pi}{2} + \varphi_1\right). \tag{5.24}$$

The surge energy index can be defined as

$$E_{ds} = \frac{I_{th.}^2 \tau_{SSCB}}{k_1^2}\left(\frac{1}{3}k_0^3 + \frac{\pi}{4}\left(1 + k_0^2\right) + \frac{1}{2}\left(1 + k_0^2\right)\arctan\left(\frac{1}{k_0}\right) - \frac{k_0}{2}\frac{\left(3k_0^2 - 1\right)}{1 + k_0^2}\right), \tag{5.25}$$

where

$$k_0 = \frac{I_{L,o}}{I_{th}}k_1 + k_2. \tag{5.26}$$

The peak voltage can be then written as

$$V_{C,1,max} = V_{ds,1,max} = V_{DC}\sqrt{1 + k_0^2} + V_{DC}. \tag{5.27}$$

The peak current that will be reached when ROCOC detection is used is

$$I_{L,1,max} = \frac{I_{th.}}{k_1}\sqrt{1 + k_0^2}. \tag{5.28}$$

TABLE 5.1: Governing design constraints of solid state circuit breaker for LVDC grid protection.

Design Constraint	Overcurrent Detection	ROCOC Detection
Maximum Voltage	$V_{\text{DC}}\sqrt{1+k^2}+V_{\text{DC}}$	$V_{\text{DC}}\sqrt{1+k_0^2}+V_{\text{DC}}$
Maximum Current	$I_{\text{th.}}\dfrac{\sqrt{1+k^2}}{k_1}$	$\dfrac{I_{\text{th.}}}{k_1}\sqrt{1+k_0^2}$
Energy Index	$\dfrac{I_{\text{th.}}^2\tau_{\text{SSCB}}}{k_1^2}\left(\dfrac{k^3}{3}+\dfrac{\pi}{4}\left(1+k^2\right)+\dfrac{1}{2}\left(1+k^2\right)\arctan\left(\dfrac{1}{k}\right)-\dfrac{k}{2}\dfrac{\left(3k^2-1\right)}{1+k^2}\right)$	$\dfrac{I_{\text{th.}}^2\tau_{\text{SSCB}}}{k_1^2}\left(\dfrac{1}{3}k_0^3+\dfrac{\pi}{4}\left(1+k_0^2\right)+\dfrac{1}{2}\left(1+k_0^2\right)\arctan\left(\dfrac{1}{k_0}\right)-\dfrac{k_0}{2}\dfrac{\left(3k_0^2-1\right)}{1+k_0^2}\right)$
Discharge Time	$T_d+\dfrac{L_{\text{total}}}{V_{\text{DC}}}\left(I_{\text{th}}-I_{\text{L,o}}\right)+\dfrac{1}{\omega}\left(\dfrac{\pi}{2}+\varphi_1\right)$	$T_d+\dfrac{1}{\omega}\left(\dfrac{\pi}{2}+\varphi_1\right)$

TABLE 5.3: Sensitivity analysis parameters.

Parameter	Acronym	Value
Voltage	V_{DC}	350 [V]
Initial Current	$I_{L,o}$	8 [A]
Threshold Current	$I_{th.}$	32 [A]

5.3 DESIGN SENSITIVITY ANALYSIS

In the previous section, SSCBs operation stages and design constraints that takes into account the difference between the applied detection methods were described. This section provides a sensitivity analysis of the design space and design constraints. The parameters used in the sensitivity analysis are summarized in Table 5.3.

In the following analysis, the influence of the system on the SSCB operation is considered with the total inductance of the circuit. The current threshold values for which the SSCB needs to be rated can be calculated using IEC61660 standard. The influence of the meshed topology can be taken into account using a matrix approach presented in [120, 132]. The SSCB needs to be rated to be capable of carrying the short circuit currents and open them at given maximum inductance of the circuit. Similarly, the SSCB must be able to interrupt extremely fast-rising current at minimum inductance. The grid sources are assumed to behave as ideal voltage sources, as the operation of SSCB is in range of μs. The size of the fault inductance can be considered as a measure of fault distance, as the fault inductance increases with the fault distance from the SSCB.

A crucial design parameter for the SSCB design is the maximum voltage that appears across the blocking MOSFET after the opening of the faulted circuit. Figure 5.4 shows the peak voltage that is reached during the clearing process for both overcurrent and ROCOC detection method. By comparing Fig. 5.4a and Fig. 5.4b it is clear that the overcurrent detection method results in overvoltages above 800 V for all values of the total loop inductance when the snubber capacitor is smaller than 1 μF. However, the ROCOC detection is capable of limiting the overvoltages for minimal loop inductances even with snubber capacitance less than 500 nF.

The effect of increased detection delay T_d can be studied in Fig. 5.5 and Fig. 5.6. Figure 5.5 shows the effect of changing detection delay when L_{total} is fixed at 3 μs. For both methods, it can be observed that the longer the delay, the higher are the resulting overvoltages. Moreover, with the increased capacitor size, the difference caused by the delay diminishes as well as the difference between the detection methods. When the loop inductance is minimal, the ROCOC detection effectively reduces the maximum voltages provided that the detection delay is within 1 μs. Figure 5.6 shows the effect of different detection delay times when the loop inductance is fixed at 100 μH. For very large loop inductance, the ROCOC detection is never activated as the current change is very slow. Therefore the results for ROCOC are not shown. Figure 5.6 shows that even

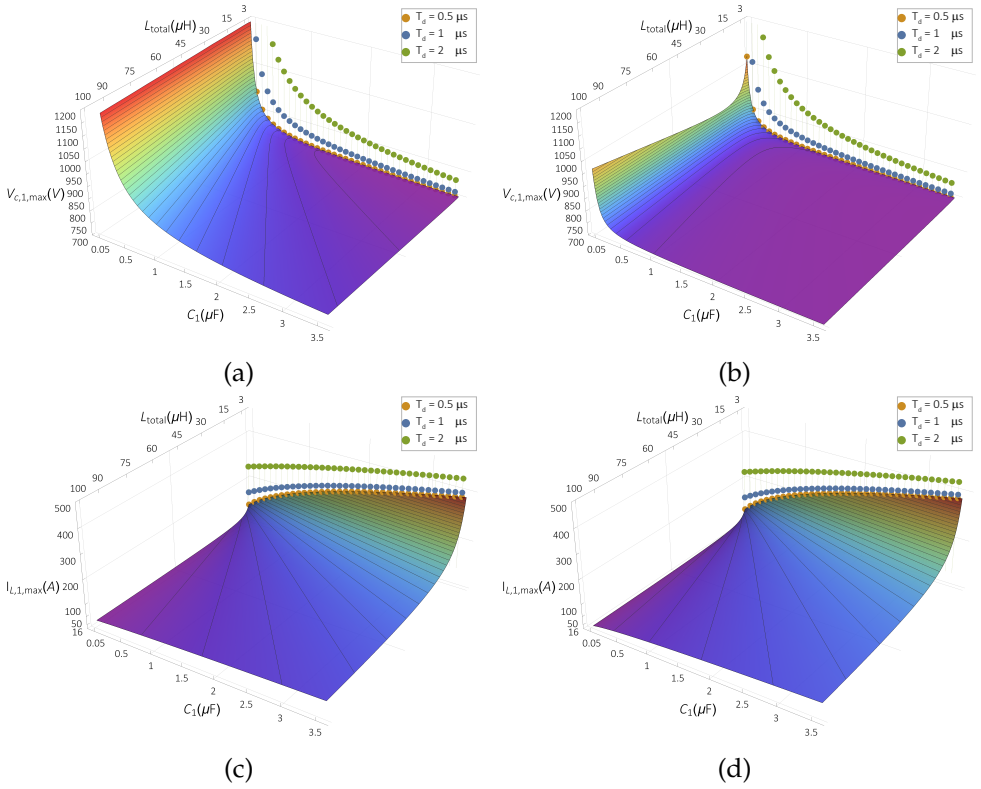


FIGURE 5.4: Peak current and voltage as a function L_{total} and C_1. In (a) is the peak voltage when overcurrent detection is used and in (b) is the peak voltage when ROCOC detection is used. (c) and (d) show the peak current when overcurrent detection and ROCOC detection are tripped respectively.

though the peak current is very low, the maximum voltage is very high. For highly inductive faults reducing the detection delay is ineffective and only increasing the size of the snubber capacitor can limit the maximum voltage.

The snubber capacitance should not be oversized as it directly increases the maximum value of current flowing in the circuit during short-circuit as is visible in Fig. 5.4c and Fig. 5.4d. From figures, it is also visible that for both methods for substantial capacitor sizes, the difference caused by different delay times is diminished. This effect can be explained by the fact that the clearing process is dominated by stage 2, i.e. the stage bounded by the time of MOSFET turn-off $t_{\text{tr.}}$ and time t_{dc} at which the short-circuit current crosses zero for the first time. The influence of different detection delays, however, is very strong for small snubber capacitors as can be seen in both Fig. 5.4c and Fig. 5.4d. The influence of the detection delay is stronger for ROCOC detection, which can limit the short-circuit current peak below hundred amperes for snubber capacitors smaller than 500 nF. The detail of the influence of different detection delays is shown in Fig. 5.5. Comparing peak currents in Fig. 5.5c and Fig. 5.5d it is clear

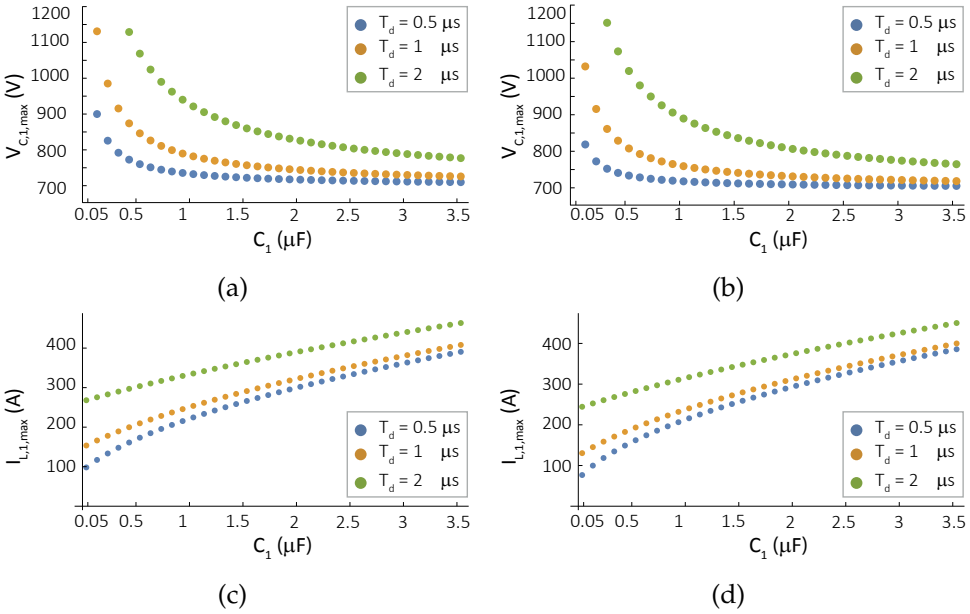


FIGURE 5.5: Peak current and voltage as a function of C_1 for different detection delay times T_d, when L_{total} is fixed at 3μH. In (a) is the peak voltage when overcurrent detection is used and in (b) are the peak voltages when ROCOC detection is used. (c) and (d) show the peak currents when overcurrent detection and ROCOC detection are tripped respectively.

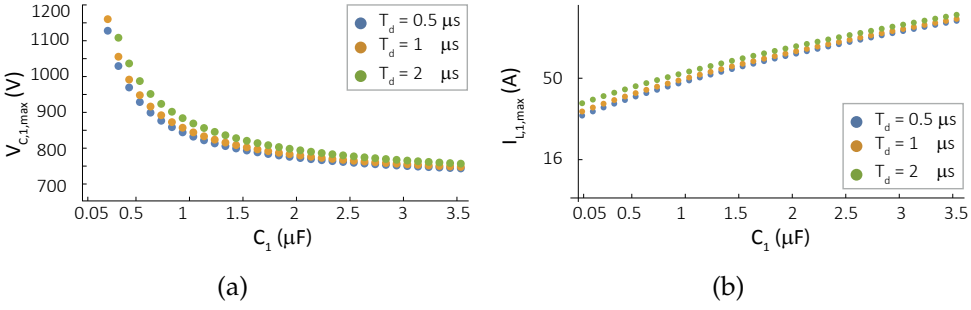


FIGURE 5.6: Peak current and voltage as a function of C_1 for different overcurrent detection delay times T_d, when L_{total} is fixed at 100μH. In (a) is the peak voltage when overcurrent detection is used and in (b) are the peak currents.

that fast ROCOC detection is capable of limiting the peak currents better than slower overcurrent detection when the circuit has minimal self-inductance inductance.

The increase of time t_{dc} and energy index E_{ds} caused by the increase of the snubber capacitor is further illustrated in Fig. 5.7. As is visible oversizing of the snubber

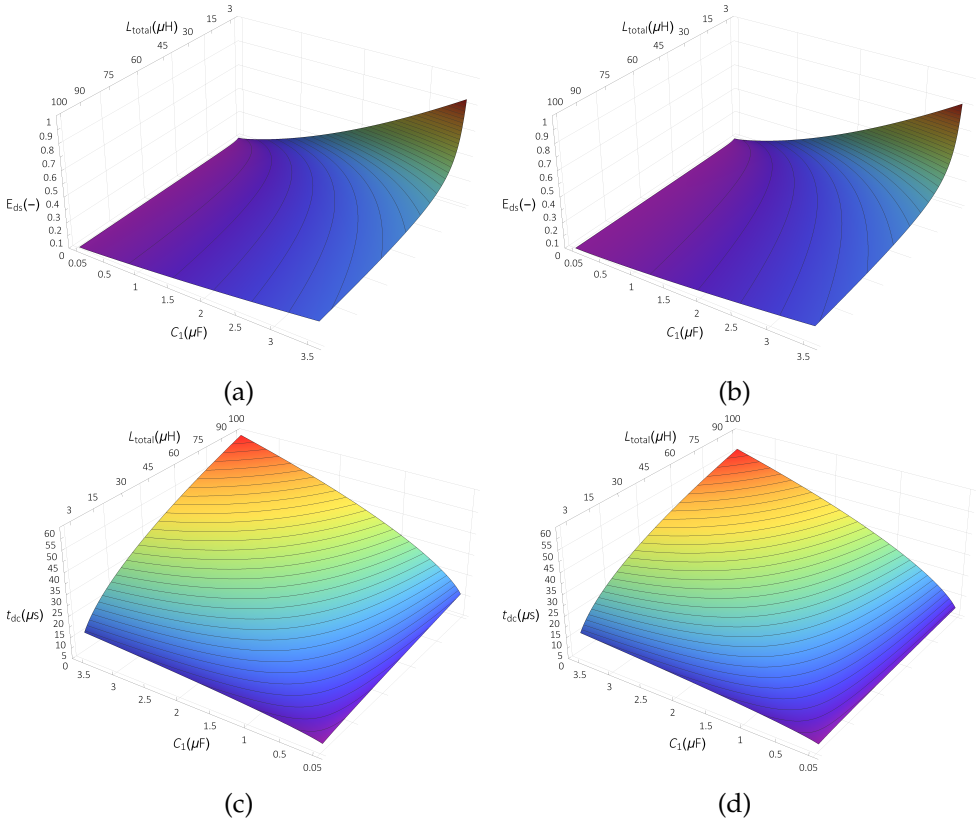


FIGURE 5.7: Energy index and time period $t_{dc} - t_{ft}$ as a function L_{total} and C_1 The results are obtained for detection delay T_d of 1 μs. In (a) is the energy index when overcurrent detection is used and in (b) is the energy index when ROCOC detection is used. (c) and (d) show the time period $t_{dc} - t_{ft}$ when overcurrent detection and ROCOC detection are tripped respectively.

capacitor results in a significant increase of the energy index, especially for minimal loop inductance. This can be explained by the fact that when the loop inductance is small, the current rises very fast, the large snubber capacitor causes prolongation of the entire clearing time, and that results in the high energy index. Further insights about clearing time can be gain by observing Fig. 5.7c and Fig. 5.7d. It is clear that the total clearing time is longer for overcurrent detection, and the difference is becoming more evident as the inductance of the circuit is increased. However, for large loop inductance, the ROCOC detection will not be activated as the current rise would be too small.

From the above discussion, it can be concluded that the overcurrent detection and the ROCOC can complement each other. The ROCOC detection is viable to reduce the voltage stress when the loop inductance is minimal, thus minimizing the requirement on the snubber capacitor. The overcurrent detection is viable when the current rise is

slower, and the ROCOC detection is not activated. Furthermore, it can be concluded that the SSCB must specify the maximum loop inductance it can safely open as the overvoltages can be very high even when the short-circuit currents are relatively small.

5.3.1 *Effect of Switch Parasitics*

The SSCBs peak current amplitude and its duration are limited by the semiconductor junction temperature. The peak voltage is limited by the semiconductor minimum breakdown voltage. The influence of the non-ideal behaviour of the devices on the peak voltage across the blocking semiconductor and the peak inductor current has three common parasitic sources: drain-source capacitance, drain path inductance and source path inductance.

Typical values of the drain-source capacitance of SiC MOSFETs are in the range of hundreds of picofarads. From the sensitivity analysis, it can be observed that practical snubber capacitances C_1 and C_2 are several hundred up to thousands of times larger than the parasitic capacitance. Therefore, the influence of the drain-source capacitance on the peak values will be minimal. The parasitic inductances occur in the drain and the source path and tend to influence high-speed switching circuits. If the parasitic inductances are not limited, they can have a harmful influence on the switching behaviour of the employed MOSFETs. However, in the case of SSCB, these parasitic inductances will have a relatively small influence on the peak fault current and peak overvoltage. The sensitivity analysis shows that practical minimum values of limiting inductances that are part of the SSCB start at hundreds of nanohenry. This value is significantly higher than the parasitic inductance of any semiconductor package.

The operation of MOSFETs, in general, is influenced by the junction temperature. One of the well-known impacts of varying junction temperature is the rise of drain-source on resistance and restriction of the safe-operating area of the semiconductor. The change of the drain-source resistance over a temperature range is not linear. The variation of on-resistance should be taken into account when using drain-source voltage as a fault indicator. During the fault clearing the difference of on-resistance on its own is not significant enough to notably influence the peak fault current or the overvoltage after interruption of the fault current.

5.4 EXPERIMENT

The SSCB prototype parameters are summarized in Table 5.4. The prototype is shown in Fig. 5.8. The prototype used in the experiments uses in total 4 SiC MOSFETs. On the prototype, the overcurrent detection is implemented using drain-source voltage measurement using method adopted from [133]. The ROCOC is based on the differential measurement of the voltage drop across the current limiting inductor L_1. The measured values are fed to analogue comparator modules on MCU. The use of analogue comparator modules significantly reduces the detection delay time compared to ADC modules.

The short-circuit was created with a mechanical switch. A complete test bench is shown in Fig. 5.9a. The prototype was tested in two test circuits shown in Fig. 5.9b and

TABLE 5.4: Prototype and test circuit parameters.

Parameter	Acronym	Value
Nominal Voltage	V_{DC}	350 [V]
Nominal Current	$I_{nom.}$	16 [A]
Threshold Current	$I_{th.}$	32 [A]
On Resistance	R_{on}	33 [mΩ]
Limiting Inductance	L_x	1.5 [μH]
Snubber Capacitance	C_x	0.32 [μF]
Snubber Resistance	R_x	39 [Ω]
Line Resistance	$R_{Line,x}$	2 [Ω]
External Capacitance	C_{DC}	1.2 [mF]
External Inductance	$L_{ext.}$	6 [μH]
Short Circuit Resistance	R_{SC}	1 [Ω]

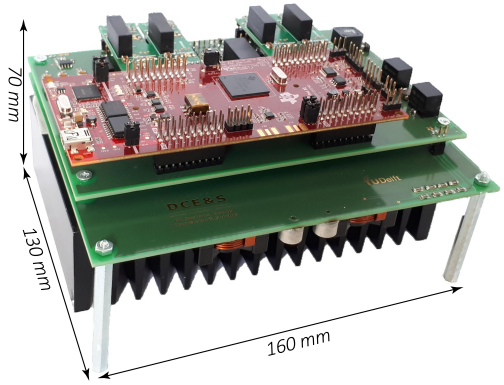


FIGURE 5.8: Prototype SSCB.

Fig. 5.9c. The circuit in Fig. 5.9b was used to test the short-circuit detection and clearing capabilities of the SSCB. During the short-circuit tests, an external capacitor was added to the source to emulate ideal voltage source behaviour better. The experiment was repeated with external inductance $L_{ext.}$ and without. As discussed with minimum loop inductance, the current rises faster, and the ROCOC detection is activated. When external inductance is added, the overcurrent detection is activated. The circuit in Fig. 5.9c was used to test the behaviour of the SSCB during large load steps. The current through the drain of the MOSFET was measured with Rogowski coil and the current through the SSCB during short-circuit detection with a Peterson coil.

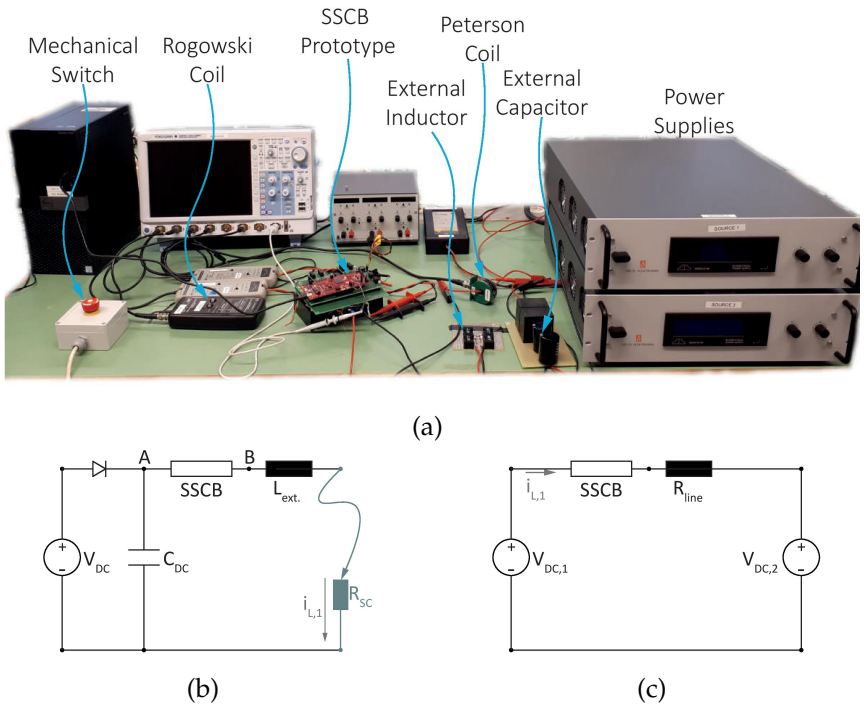
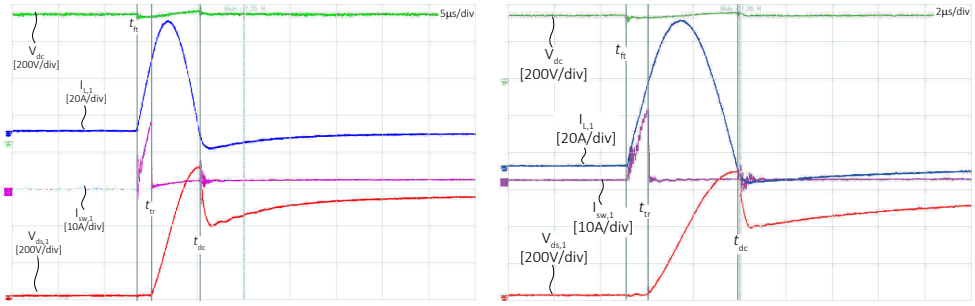


FIGURE 5.9: Evaluation Circuits. In (b) is the circuit used in the laboratory to evaluate the short-circut detection. In (c) is the circuit used to ensure the resistivity of the detection method to load steps.

5.4.1 *Overcurrent Detection Experiment*

The experimental results for the short circuit detection when the SSCB orientation is as in Fig. 5.9b are shown in Fig. 5.10. The detection based on measurement of the drain-source voltage $v_{ds,1}$ is shown in Fig. 5.10a. Figure 5.10a shows the power signals in the circuit - current through the SSCB $i_{L,1}$, current through the drain of the blocking MOSFET $i_{ds,1}$, the voltage on the external capacitor V_{DC}, and the voltage on the drain-source of the blocking MOSFET $v_{ds,1}$. As is shown in the figure, the total time after the fault inception to the turnoff is 2 μs. After the SSCB MOSFETs are turned off, the current continues to flow and charges the snubber capacitor. Because the external inductor is part of the circuit, the charging process takes up to 6 μs. After the capacitor is charged, the current reverses its direction, and the capacitor is discharging through the snubber resistance. During this stage, the MOSFET body diode is used. The transition to the MOSFET body diode is visible in Fig. 5.10a where the noise in the drain current marks the transition. The process ends when the capacitor is discharged, and the voltage is blocked as is visible from $v_{ds,1}$.

The experiment with added external inductance was repeated with the SSCB inverted compared to Fig. 5.9b, i.e. the short circuit is at the node A. The results are



(a) (b)

FIGURE 5.10: Experimental results for fault at node B.In (a) are the power waveforms of the SSCB with external inductance added to the circuit. In (b) are the power waveforms of the SSCB without the external inductance, when ROCOC detection is activated.

shown in Fig. 5.11a. The results show that the SSCB trips at the same thresholds for both locations of fault, and the differences between the signals are minimal. Confirming the bidirectional operation capabilities of the design SSCB.

5.4.2 *Rate of Change of Current Detection Experiment*

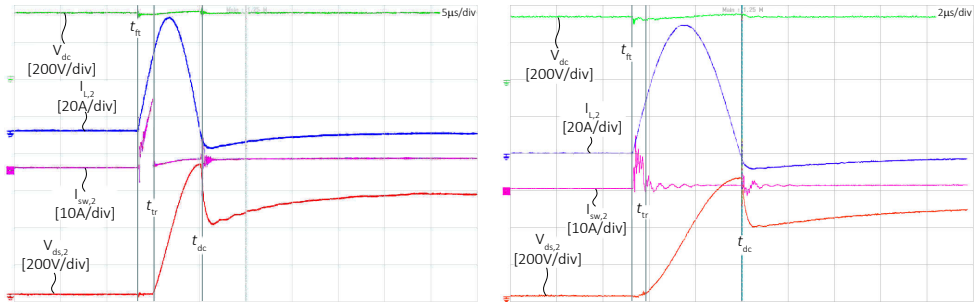
As was discussed when the short-circuit is located at the terminals of the SSCB, the overcurrent protection is not able to limit the overvoltages after opening. Therefore the experiment in Fig. 5.9b was repeated with zero external inductance. The current rises more than two times faster after the short circuit inception.

The experimental waveforms of the ROCOC detection are shown in Fig. 5.10b for the fault located at node B. On the power waveforms in Fig. 5.10b the fast current rise through the SSCB and the blocking MOSFET can be observed. The fault is detected within one microsecond as can be seen from the current through the drain $i_{ds,1}$. The current after opening continues to rise and reaches its peak faster than when the external inductance is in the circuit. When ROCOC detection is used, the total time from fault inception to discharge of the capacitor is 1 μs shorter than when overcurrent detection is used. The results show that the total clearing time is dominated by the time taken to charge the snubber capacitor.

The experiment was repeated with the fault located at the terminal A, and the results are shown in Fig. 5.11b. When the fault is located at terminal A, the time taken by the detection is 300 ns faster. The difference is caused by the fact that the fault is located closer to the inductor on which the voltage drop is measured.

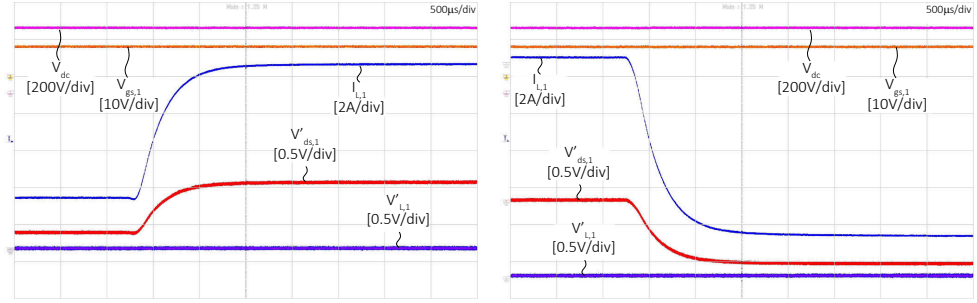
5.4.3 *Load Steps*

In SSCB prototype ROCOC detection is implemented. The ROCOC detection can be prone to be activated by fast load trips. Experiment with fast load step is executed,



(a) (b)

FIGURE 5.11: Experimental results for fault at node A. In (a) are the power waveforms of the SSCB with external inductance added to the circuit. In (b) are the power waveforms of the SSCB without the external inductance, when ROCOC detection is activated.



(a) (b)

FIGURE 5.12: Reaction of the SSCB to load steps.

to strengthen the confidence in the designed SSCB prototype. In [134] the load step was 1.6 A over 100 milliseconds. In [135] the load step was 1.5 A over 400 milliseconds. In [136] the load step was 2.3 A over 100 milliseconds. In [137] the load step was 5 A over 50 milliseconds. The load step is almost a hundred times faster than in the preceding works. Figure 5.12 shows the results of the experiments executed on the test circuit shown in Fig. 5.9c. The voltage source and load $V_{DC,1}$ and $V_{DC,2}$ were emulated with Delta Elektronika SM-15K. The results of step-up of the current through the SSCB and step-down are shown. As is visible, the current rises to five times the original value. In both Fig. 5.12a and Fig. 5.12b the measured voltage across the blocking switch $v'_{ds,1}$ follows the current through the SSCB. The voltage $v'_{L,1}$ is the trip signal of the ROCOC detection method. As is visible during the load steps, it remains zero and does not initiate spurious trips.

5.5 CONCLUDING REMARKS

Design criteria and constraints of a solid-state circuit breaker (SSCB) for a low voltage direct current (LVDC) microgrid protection were derived based on the SSCB operation analysis. The design criteria consider the effect of different system parameters, detection methods and detection delay times. The design space and the limitations of the SSCB with different detection methods are analysed via sensitivity analysis. SSCB prototype is developed, and its performance is evaluated in different operating scenarios under nominal grid voltage and current.

Sensitivity analysis presents the rate of change of current (ROCOC) detection as a useful tool to optimise the size of the snubber capacitors when the SSCB is expected to operate in grids with minimal self-inductances. The analysis demonstrates the vitality of the optimal size of the snubber capacitance as it is directly linked to the total clearing time and the peak short-circuit currents. Moreover, it is shown that the maximum loop inductance is an important design parameter that needs to be specified for every SSCB. As clarified in the analysis for maximum values of the loop inductance, the detection delay has minimal effect and only increasing the snubber capacitor can limit the maximum voltage on the blocking MOSFET.

Derived design constraints are a useful tool to optimise the size of the SSCB equipped with a combination of detection methods for different grid parameters. Moreover, the derived constraints are compact and can be used as an effective tool to evaluate the effect of different LVDC grid protection schemes on the size of the SSCB.

Part IV

SYSTEM INTEGRATION

6

PARTIALLY RATED PFCC & SSCB: ENABLING MESHED LVDC GRIDS

Previous chapters dealt with technical challenges of various function building blocks. In this chapter the function building blocks are integrated and a system building block for LVDC microgrids is proposed. The building block functionality is demonstrated in various applications using simple equivalent circuits. In the chapter the system gains when the proposed building block is used are demonstrated, e.g. doubling the line length of a street light system. The chapter experimentally validates the operation of the building block during normal operation and grid short-circuits.

This chapter is based on:

J4 P. Purgat, A. Shekhar, Z. Qin, P. Bauer-*"LVDC System Building Block with Integrated Power Flow Control and Short-Circuit Protection", IEEE Industrial Electronics Magazine (under review)*

C6 P. Purgat, Z. Qin, P. Bauer-*"Design of Solid-state Circuit Breaker for Partially Rated Power Flow Control Converter", 2019 IEEE Third International Conference on DC Microgrids (ICDCM)*

C7 P. Purgat, Z. Qin, , P. Bauer-*"On the Protection of the Power Flow Control Converter in Meshed Low Voltage DC Networks", 2018 IEEE Energy Conversion Congress and Exposition (ECCE)*

6.1 INTRODUCTION

Previous chapters focused on various technical challenges of function blocks used in LVDC microgrids. In this chapter firstly a short excursion into history of LVDC in secondary and tertiary energy distribution system is made. Then a short survey of current pilot projects and potential markets is provided to illustrate the LVDC future. Then a system building block for LVDC systems is presented which integrates power flow controller converter (PFCC) and solid state circuit breaker (SSCB). The functionality of the system building block is presented using a simple equivalent model. Three of the surveyed markets are chosen as case studies to demonstrate the potential benefits of the proposed building block. The chosen markets are - street light system, battery charging and meshed power distribution system. The chapter closes with an experimental section that validates the steady-state operation. Moreover, the ability of the building block to withstand bolted short-circuits on its terminals is also experimentally validated.

6.1.1 *A Very Short History of LVDC*

Low voltage direct current (LVDC) systems were the pioneer systems providing public lighting based on Edison's incandescent electric light. These LVDC systems were more efficient than the first single phase alternating current systems (ac). However, they were soon outperformed by Tesla's polyphase ac systems. While in 1887 in United States there were five times more LVDC central stations for light than ac central stations, in 1890 there were 30 % more ac central stations [138]. The efficiency and ability of ac systems outweighed any concerns about ac safety, that were amplified especially by Edison to help his systems commercial growth. Already at the end of nineteenth century it was clear that without a device to arbitrarily control the voltage level, LVDC systems will not outperform ac polyphase systems.

Power electronics in the past two decades, however, brought forth disruptive changes besides else to electric power distribution. Primarily, the rise in energy efficiency and cost-efficiency of power electronics lead to the increase of devices that internally utilise direct current (dc) and this trend is expected to continue. The increased economic competitiveness of the renewable energy sources (RES) such as photovoltaics (PV) leads to extensive use of these sources. PV and other RES either internally produce dc or are using power electronic converters to control their power output which have an internal dc link. Moreover, the emergence of prosumers and energy storage is fundamentally reshaping the landscape of both electric energy production and distribution. Under the new conditions LVDC became a viable option in many energy distribution markets.

6.2 LVDC PROMISE AND OUTLOOK

6.2.1 *LVDC Markets & Applications*

There are already numerous pilot projects and field demonstrators of LVDC systems. LVDC was successfully used by several municipalities to install street light

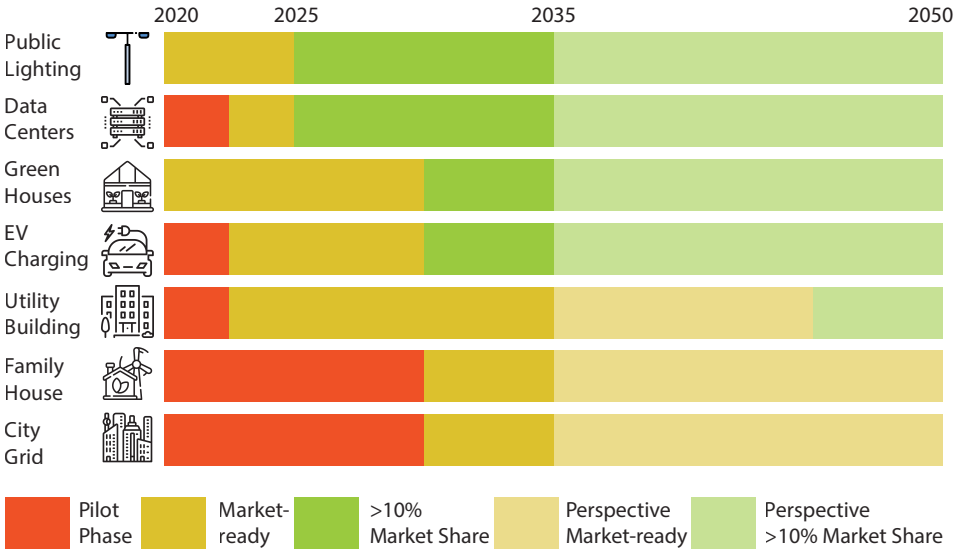


FIGURE 6.1: Dc markets current status and outlook.

systems [139] and even by the port of Amsterdam [140]. A PV-powered DC test bed with office LED lighting system showed potential electricity savings of up to 5 % [141]. Using LVDC in data centers can double mean-time-between-failure when a single uninterruptible power supply per path is used [142]. Moreover, pilot projects such as [143] and [144] exhibit efficiencies increased by 7 % to 10 %. LVDC shows energy savings in utility installations, as well. LVDC office building in [15] demonstrated up to 5.5 % energy savings compared to comparable ac system. Energy neutral teaching facility that uses LVDC distribution was also demonstrated [145]. Usability of LVDC for power distribution has been demonstrated in field for the first time in [146]. The installed bipolar system is capable of delivering 100 kW. The demonstrator showed that it is possible to continue to supply the end customers despite several medium voltage AC interruptions. A larger system with 160 kW installed PV, that integrates LEDs, air conditioning and even electric vehicle charging was demonstrated in [147].

Figure 6.1 shows an overview of the current status of LVDC adaptation in different power distribution markets [148]. Three technology readiness levels are defined in Fig. 6.1. First is the pilot phase in which the feasibility of LVDC for a given market is experimentally demonstrated on a small scale. After the pilot phase, the technology can enter a market-ready phase in which the first commercialised systems start to appear. The last phase is achieved when the technology carves-up a relevant piece of market, 10 % market share is selected as a threshold for the last phase. LVDC in these markets brings either cost-saving or system efficiency improvement or a combination of the two. LVDC at the present moment has a strong foothold in niche markets, especially in private owned energy distribution systems [148, 149]. Further LVDC market growth is expected especially in RES and energy storage systems, electromobility, data centers and utility buildings [149].

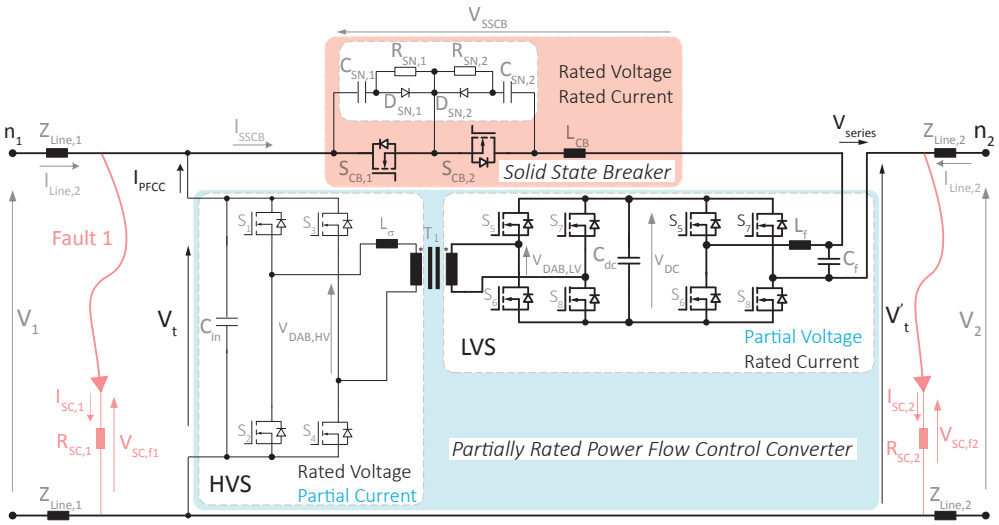


FIGURE 6.2: The power flow control converter for LVDC grids with integrated short circuit protection.

6.2.2 *LVDC Barriers & Challenges*

Further adoption of LVDC faces both technical and non-technical challenges. Main non-technical challenges are essentially typical characteristics of the nascent stage. Market surveys and technology readiness reports suggest that one of the major barriers is the lack of cost-competitive, market-ready components for dc systems. Lack of cost-competitive components creates a barrier for the use of LVDC in utility and office buildings as the cost of retrofitting is high. However, a strong incentive comes from the power over Ethernet and the new USB standards [149] to foster growth of LVDC in utility buildings. Other significant drawback is the lack of standards and good practices [16, 150]. The lack of knowledge at the early stage also means a lack of personnel for installation and maintenance of these systems [148].

Technological challenges stem from specific protection requirements of LVDC systems and efficient bi-directional power control. DC-DC converters can not always implement short-circuit current interruption, as the freewheeling diodes continue to conduct. Therefore, DC-DC converters that are used in LVDC systems need to have extra protection circuitry. Most prominent short-circuit protection solution are the solid-state circuit breakers (SSCB). DC-DC converters with galvanic isolation can implement the fault isolation, as well as the connection of different voltage levels and the bi-directional power flow control. However, DC-DC converters with galvanic isolation have considerable size and cost. Thus in many applications, it is desirable to implement the protection against short circuit, and voltage and current control in a way that saves material and increases system efficiency. For this reason, partially rated power flow control converters (PFCC) were independently proposed for high voltage DC [34] and LVDC systems [31] and [C2-C3]. The partial power rating and

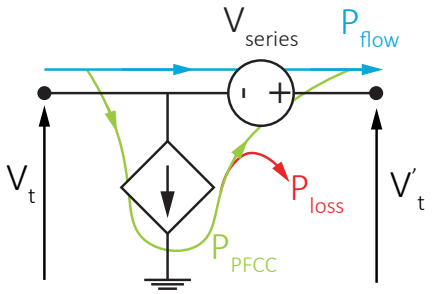


FIGURE 6.3: Equivalent circuit of the proposed building block.

processing ensures smaller size, cost and higher system efficiency than their fully rated counterparts.

6.3 SYSTEM BUILDING BLOCK

The schematic of the partially rated PFCC composed of power electronic switch based High and Low Voltage Side (HVS and LVS, respectively) is shown in Fig. 6.2. The purpose is to regulate the power flow (P_{flow}) between two nodes (n_1, n_2) with voltages V_1 and V_2 by injecting a relatively small controlled series voltage V_{series}. It will be shown that the power processed by the PFCC (P_{PFCC}) is a relatively small fraction of P_{flow}. Consequently, it can be inferred that components used for composing HVS and LVS can be derated in accordance to the respective partial current and voltage requirements during full load operation. A more detailed working principle as well as system protection during short-circuit faults at n_1 and n_2 is experimentally described in Section 6.5.

6.3.1 *Equivalent Circuit*

The equivalent circuit of the PFCC with integrated short circuit protection is shown in Fig. 6.3. The presented abstraction is used as the key building block for different system level applications proposed in this paper.

The current I_{PFCC} drawn by the building block is given by (6.1),

$$I_{\text{PFCC}} = \frac{P_{\text{PFCC}}}{V_t} = \frac{P_{\text{flow}} V_{\text{series}}}{\eta V_t V_t'}, \tag{6.1}$$

where, V_{series} is the control action that results in the desired P_{flow} between terminals with voltages V_t and V_t'. It must be noted that P_{flow} and V_t' are intimately related and govern the current flow I_{flow} between the two terminals. Therefore, the PFCC block can be used in different applications that require the functionality to regulate these three operating parameters in the system as a function of V_{series}.

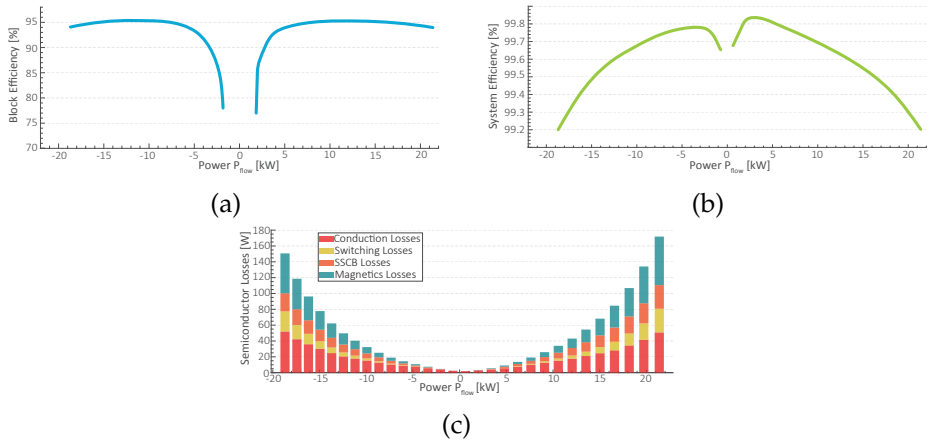


FIGURE 6.4: System building block efficiency. In (a) is the building block level efficiency η, in (b) is the system efficiency η_{sys} and in (c) is the loss breakdown.

6.3.2 *Operating Efficiency and Loss Breakdown*

The factor η in (6.1) is the efficiency of the PFCC building block that relates the block power loss P_{loss} to the processed PFCC power, including the component losses in HVS, LVS and the SSCB, as described by (6.2).

$$P_{\text{loss}} = (1-\eta)P_{\text{PFCC}}. \tag{6.2}$$

For defined system level efficiency η_{sys}, the equality described by (6.3) must be followed.

$$(1-\eta_{\text{sys}})P_{\text{flow}} = (1-\eta)P_{\text{PFCC}}. \tag{6.3}$$

Since $P_{\text{PFCC}} << P_{\text{flow}}$, it is inferred that $\eta_{\text{sys}} >> \eta$ as can be observed from the simulated efficiency curve shown in Fig. 6.4

The presented results are based on a detailed switch model developed in PLECS using the parameters from Table 6.1 and Table 6.2. The HV switches used in PFCC are C3M0030090K. and IPB017N10N5 for the low voltage part of the PFCC. While the shown results are representative and can be different depending on the design considerations, the highlighted principle is that system level efficiency for achieving the desired control objective is high even if the actual converter efficiency itself is relatively lower. The loss breakdown for different block components is shown in Fig. 6.4c.

In addition to the potential system level efficiency improvement, the material usage, size and inevitably the cost of the PFCC building block is lower compared to a fully rated dc-dc converter considering that the passive as well as active components in HVS and LVS are derated.

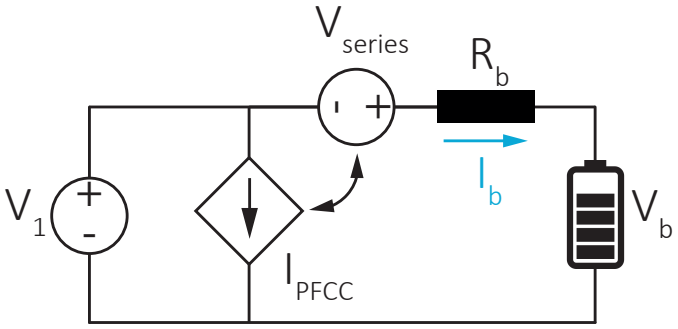


FIGURE 6.5: Simplified equivalent circuit representing dc charging with PFCC.

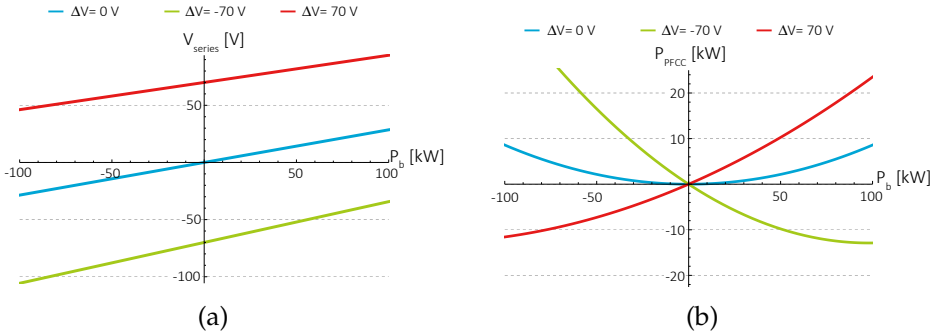


FIGURE 6.6: DC battery charging with PFCC. In (a) is the series voltage of the PFCC as a function of the battery power. In (b) is the power processed by PFCC as a function of the battery power.

6.4 APPLICATIONS

In the previous section, the key benefits and operation principle of the developed building block were presented. In this section, the equivalent circuit is used in three different applications, which are in different market adaptation levels. The applications were also chosen such that they represent three different control roles and have different sizing requirements. In each example new insights about the proposed building block are demonstrated, which are then summarized in conclusions.

6.4.1 *DC Charging*

Interfacing batteries with dc systems is often done via synchronous buck converters when galvanic isolation during normal operation is not required. The galvanic isolation during faults is provided by external circuit breakers and mechanical contactors. The proposed building block can interrupt faults, and only mechanical contactors are added to ensure galvanic isolation. Simplified circuit of battery charging with PFCC is

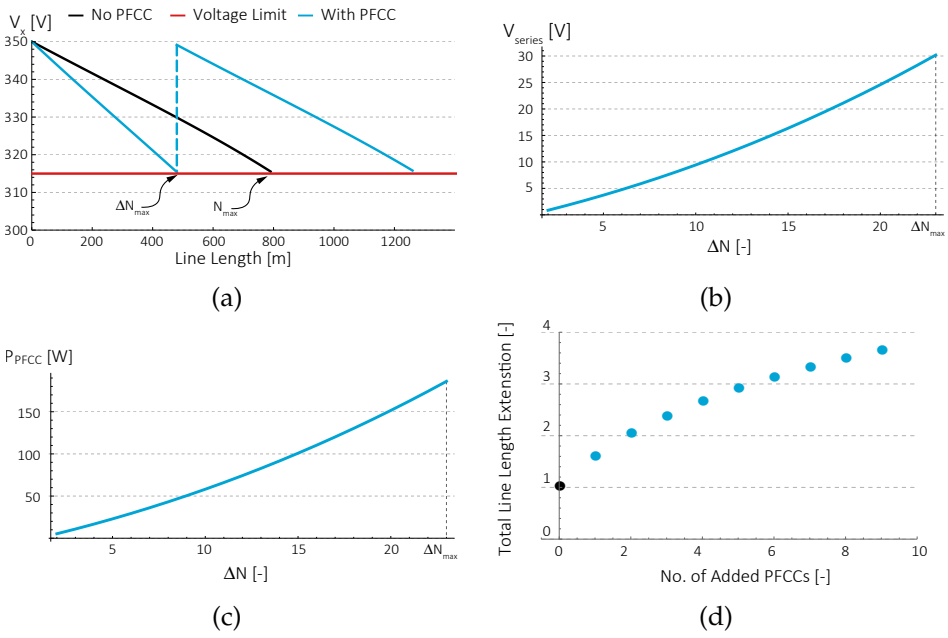


FIGURE 6.7: Voltage drop compensation in street lighting system. In (a) is the voltage profile of the system without PFCC (black) and with PFCC (cyan). In (b) is the series voltage of the PFCC and in (c) is the power processed by the PFCC, both shown as functions of the number of added lamps. In (d) is shown the possible line extension if multiple PFCC were used.

shown in Fig. 6.5. For simplicity sake, the battery is assumed to behave like a voltage source with small internal resistance. Further, no resistance between the source and PFCC is assumed. By analysing circuit in Fig. 6.5 following equations can be written

$$V_{\text{series}} = \frac{P_b R_b}{V_b} - \underbrace{(V_1 - V_b)}_{\Delta V}, \tag{6.4}$$

$$P_{PFCC} = \frac{P_b}{\eta V_b} V_{\text{series}}, \tag{6.5}$$

where P_b is the battery power and V_b is the battery terminal voltage.

Figure 6.6 shows the results of the simplified system when nominal dc voltage is $V_1 = 350V$ and the internal battery resistance is $R_b = 0.1\Omega$. Figure 6.6a shows the series voltage injected by PFCC during charging at different voltage drops. The voltage drop range is 40%, which is the maximum operating voltage drop of most batteries. The first observation from Fig. 6.6a is that the variation of series voltage is smaller than one-fifth of the nominal voltage. The total range of the series voltage is therefore within one-third of the nominal voltage, i.e. for the system used in this example the operating voltage of PFCC on the low voltage side is only $+/-100$ V. This small

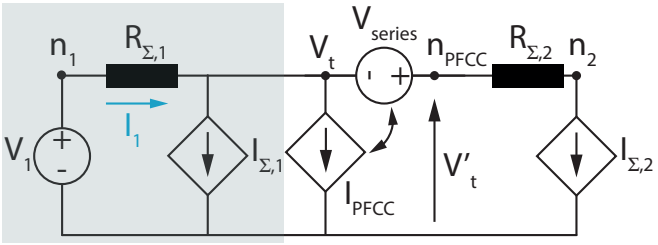


FIGURE 6.8: Equivalent circuit of street light system with PFCC. The shaded grey part can be considered as the equivalent circuit of a street light system without a PFCC installed.

processed voltage translates to small power processed. Figure 6.6b shows the power processed in PFCC as a function of the charging power. For the nominal case, when the battery voltage is the same as the source voltage, the power processed is ten times smaller than the charging power. This ratio is less favourable in extreme cases when the battery voltage is 20% higher or smaller than the grid voltage. However, even in extreme cases, PFCC processes only one-fifth of the total charging power. The PFCC maintains the advantage of partial processing. It should also be noted, that normally the batteries are operated with smaller voltage drops to prevent fast battery degrading.

6.4.2 *DC Street Light*

The street lighting was historically the first major application of electricity that brought major benefits in terms of increased life quality. Street lighting also seems to be the first major application opened for dc distribution. The motivation to use dc in street lighting stems from the decrease of use of incandescent and high-pressure sodium due to concerns about their negative impact on the environment. The municipalities are seeking to retrofit the lights with more energy-efficient light-emitting diodes (LED), install a remote monitoring and control system. Already existing dc pilot projects are in the port of Amsterdam or A4 highway in Delft, the Netherlands.

Consider only the shaded grey region of the equivalent circuit shown in Fig. 6.8. This is representative of a street lighting system of N poles equally spaced $d = 20\,\mathrm{m}$ apart without PFCC. The lumped power drawn by N lamps in such a system can be represented by a current sink $I_{\Sigma,1}$ and is given by (6.6).

$$I_{\Sigma,1} = \frac{NP_{\mathrm{lamp}}}{v_{\mathrm{t}}}. \tag{6.6}$$

Here, the rated power drawn by a single lamp is taken as $P_{\mathrm{lamp}} = 50\,\mathrm{W}$. The lumped resistance $R_{\Sigma,1} = NdR$ is estimated assuming a line resistance $R = 6.57\,\Omega/\mathrm{km}$. The voltage profile along the feeder line in the absence of PFCC based voltage regulation is shown with solid black line in Fig. 6.7a. It can be observed that the allowable drop in

line voltage (V_{min}, red line) limits the line length to approximately 800 m corresponding to $N = 40$ for the considered parameters as given by (6.7),

$$N \leq \underbrace{\sqrt{\frac{V_{\text{nom}} - V_{\text{min}}}{dRi_{\text{r,max}}}}}_{N_{\text{max}}}, \tag{6.7}$$

where $i_{\text{r,max}} = P_{\text{lamp}}/V_{\text{min}}$ is the maximum operating current of a single lamp. In case the PFCC element is added to regulate V_{t}' to nominal system voltage (V_{nom}) as shown in the Fig. 6.8, the number of series connected lamps can be extended to $N_{\text{ext}} = N_{\text{max}} + \Delta N$. It can be inferred that N_{max} lamps can be installed between the output terminal of the PFCC and the end-node n_2. Correspondingly, the lumped resistances in such a system are given by $R_{\Sigma,1} = \Delta N dR$ and $R_{\Sigma,2} = N_{\text{max}} dR$. The currents, $I_{\Sigma,1}$ and $I_{\Sigma,2}$ are related to the lumped power drawn by $N = \Delta N$ and $N = N_{\text{max}}$ lamps respectively, as described by (6.6). The maximum possible line extension corresponds to maximum lamps Δn_{max} between the source node n_1 and input terminal of the PFCC such that the limit $V_{\text{t}} \leq V_{\text{min}}$ is not breached. It can be seen from Fig. 6.7a (blue line) that the length can be increased by about 50 % to approximately 1260 m corresponding to $\Delta n_{\text{max}} = 23$ for the given operating conditions.

Assume that the voltage regulating PFCC is installed such that N_{max} lamps exist between its output node n'_{pfcc} and the end node n_2. The operating PFCC voltage (V_{series}) and processed power (P_{PFCC}) as a function of the extended number of lamps (Δn) in the system is shown in Fig. 6.7b and Fig. 6.7c respectively. For example, if the street light system is extended to power ten extra lamps ($\Delta n = 10$), the PFCC needs to inject a small $V_{\text{series}} \approx 10\,\text{V}$ such that $V_{\text{t}}' = V_{\text{nom}} = 350\,\text{V}$. The corresponding power processed $P_{\text{PFCC}} \approx 50\,\text{W}$ is one-tenth of the additional load power associated with the extra lamps installed. Consequently, it can be inferred that benefits in terms of installation cost and operating efficiency of the system can be attractive as compared to conventional solutions such as re-conductoring, multiple parallel paths or use of fully-rated converter. The limit for Δn_{max} can further be increased if $V_{\text{t}}' > V_{\text{nom}}$ is permissible. The discussed use of PFCC building block specifically for line voltage regulation can be similarly conceptualized for other dc applications, such as power distribution to residential buildings.

Figure 6.7d shows an outlook on the possible line extension when multiple PFCCs are used in the same system. The trend in the figure shows saturation after several PFCCs are added. However, it is worth to underline that in theory it is possible to extend the line length by 400 %.

6.4.3 *Meshed DC Networks*

Considering the potential benefits of DC technologies in markets like street light, charging stations, data-centers and utility buildings, it is anticipated that interconnecting such systems to form a dc distribution grid is plausible as illustrated in [151]. The possible advantage of this strategy is improved system availability and efficiency, particularly when meshed topology is employed. When several paths for current to

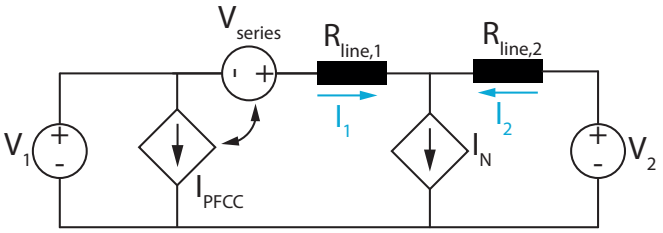


FIGURE 6.9: Equivalent circuit of a three-node meshed LVDC grid with a PFCC.

flow exists, extra care must be taken to ensure that no line is overloaded. PFCC can enhance the power capacity of the meshed system and ensure that the interconnecting lines are not overloaded.

Figure 6.9 shows a simplified schematic of a simple meshed network. If V_1 is assumed to be the same as V_2 two paths exist for the current to flow from the voltage source V_1 to the load, represented by power source $I_N = \frac{P_N}{V_N}$. The power source can both sink and source power. If the voltage V_{series} is zero, the current flow in the two paths is given by the resistance ratio $k = \frac{R_{\text{line},1}}{R_{\text{line},2}}$. For the sake of example, in the following analysis, the ratio is assumed to be equal to 2. Implying that the current flowing in line one will be two times as high as the current flowing in line two. The system further operates at nominal voltage $V_1 = V_2 = 350$ V, and the line resistance $R_{\text{line,x}} = 6.57 \quad \frac{\Omega}{\text{km}}$, line one is long 100 m. The maximum carrying capability of the line is $35A$. Figure 6.10a shows the currents in a network defined by the above parameters and assumptions.

As expected current in line, one in Fig. 6.10a has double the amplitude compared to the current in line two. The current in line one also reaches the maximum current carrying capability faster than the current in line two for both scenarios when the power source P_N is sourcing, i.e. $P_N > 0$, and when it sinks power, i.e. $P_N < 0$. The voltage of the series source is calculated as shown in (6.8). The series voltage is a function of line maximum current carrying capability, the ratio of the path resistances k, system voltage V_1 and power transferred P_N. The series voltage in (6.8) is derived by solving the Kirchoffs equations of the circuit in Fig. 6.9 for maximum current $I_{1,\max}$. The series voltage is zero, while the maximum current limit is not breached. The series voltage has a maximum limit that ensures that the current in line two is not breached either; the voltage limit is expressed in (6.8).

$$|V_{\text{series}}| = \begin{cases} \frac{1}{2}\left((2+k)\, I_{1,\max} R_{\text{line},1}\right. \\ \left. -V_1 + \sqrt{(kI_{1,\max}R_1 + V_1)^2 - 4kP_N R_1}\right) & \iff |I_1| \geq I_{1,\max} \\ 0 & I_{1,\min} \geq I_1 \geq I_{1,\max} \end{cases} .$$

$$|V_{\text{series,max}}| = R_1 \left(\frac{P_N}{V_1 - kI_{2,\max}R_1} - (1+k) I_{2,\max} \right). \tag{6.8}$$

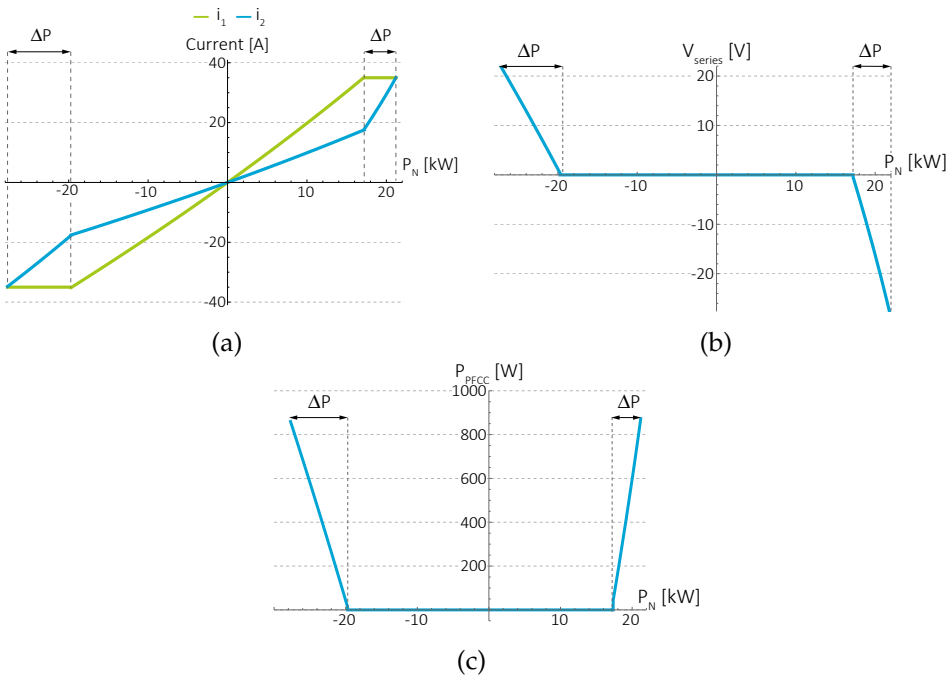


FIGURE 6.10: Current re-rounting in a meshed LVDC microgrid. In (a) are the line currents as a function of the transferred power. In (b) is the series voltage of the PFCC and in (c) is the PFCC processed power, both shown as function of the transferred power P_N.

Figure 6.10b shows voltage V_{series} as a function of power P_N, clearly the series voltage needed to ensure the current limit in both lines is less than 10% of the nominal grid voltage. Figure 6.10c shows the power processed by the PFCC. The power processed is less than 1 kW for both directions of power flow. The gain in power transfer capacity is 2.5 kW and 8 kW for power sinking and power sourcing by I_N respectively. The difference in the power enhancement capability in this particular case stems from the placement of the controlled current source I_{PFCC}. When power node P_N is sinking power, the current flows from the voltage source V_1. The current I_1 is a combination of the current supplied to the load and I_{PFCC}. If the current is supplied from V_1 than besides supplying I_N also I_{PFCC} has to be supplied. Thus reducing the net amount of power that can be supplied to power source P_N in via line 1. In the opposite direction, the effect is opposite. To gain the most power enhancement, the PFCC should be installed in both lines. Given that very low power rating of PFCC is sufficient, such installations are feasible.

6.5 EXPERIMENTS

The goal of the experiment is two-fold. One is to demonstrate the operation in a simple two-node connection, similar to *DC Charging* application. The second goal is to closely

TABLE 6.1: Power flow control converter parameters.

Parameter	Acronym	Value
Nominal Input Voltage	$V_{DAB,in}$	350 [V]
PFCC DC-link Voltage	V_{DC}	50 [V]
Switching Frequency	f_{sw}	62.5 [kHz]
Parasitic Inductance	L_{σ}	72 [μH]
Input DC Capacitor	C_{in}	16 [μF]
DC-link Capacitor	C_{dc}	1.22 [mF]
Unfolder Bridge Inductor	L_f	47 [μH]
Unfolder Bridge Capacitor	C_f	1.22 [mF]

TABLE 6.2: Solid state circuit breaker and lines parameters.

Parameter	Acronym	Value
Nominal Current	I_{SSCB}	36 [A]
On Resistance	R_{on}	8 [mΩ]
Maximum Pulse Current	$I_{SSCB,pulse}$	378 [A]
Limiting Inductance	L_{CB}	3 [μH]
Snubber Capacitance	$C_{SN,x}$	0.32 [μF]
Snubber Resistance	$R_{SN,x}$	10 [Ω]
Line Resistance	$R_{Line,x}$	1.3 [Ω]
Line Inductance	$L_{Line,x}$	1.4 [μH]

emulate the conditions during a bolted short circuit, i.e. almost zero fault resistance. The short-circuit emulation demonstrates the capability of the proposed combination to protect the derated components from failure during grid faults. The PFCC prototype electrical parameters are summarized in the Table 6.1. The electrical parameters of the SSCB and the line are summarized in the Table 6.2. A controllable short circuit is created with a MOSFET with $R_{ds,on}$ of 20 mΩ, which creates a good approximation of a bolted short-circuit. The nodes V_1 and V_2 are emulated using the Delta Elektronika SM15K series power supplies. The nominal voltage during all experiments is 350 V on both nodes.

6.5.1 *PFCC Operation*

Experimental results obtained during normal operation of the PFCC are shown in Fig. 6.11a and Fig. 6.11b. The PFCC controls the power flow between two nodes n_1 and

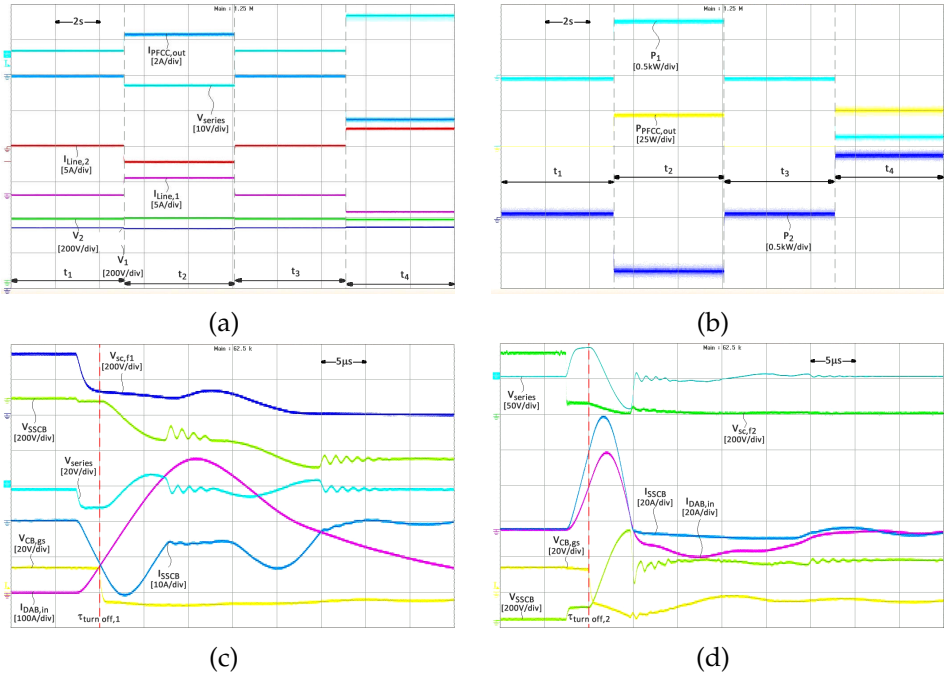


FIGURE 6.11: Operational waveforms of the PFCC and the SSCB. In (a) are the waveforms during power flow control by the PFCC and in (b) are the powers. In (c) are the variables during short circuit Fault 1. In (d) variables during short circuit *Fault 2*.

n_2 as illustrated in the schematic in the Fig. 6.2. During time intervals t_1 and t_3 PFCC controls the voltage V_{series} to be zero volt, therefore no current flows and no power is exchanged. During time interval t_2 the voltage V_{series} is controlled to be -10 V. From node V_1 current $I_{Line,1}$ starts to flow to node V_2. The power P_1 supplied by node n_1 is around 800 W, while the power P_{PFCC} injected by the PFFC is only around 25 W. During time interval t_4 the voltage V_{series} is regulated to be 10 V. Therefore, during the time interval t_4 it is the node V_2 supplying the power. During this experiment the SSCB is in conducting state, i.e. MOSFETs $S_{CB,1}$ and $S_{CB,1}$ are turned on.

6.5.2 *Fault 1*

Figure 6.11c shows the waveforms during the clearing of short circuit Fault 1. Immediately after the inception of Fault 1, it can be observed that the voltage $V_{sc,f1}$ drops. The capacitor C_{in} is quickly discharging into the short circuit as is demonstrated by the rise of the current I_{PFCC}. The short circuit current that is supplied from the capacitor C_{in} peaks at more than 400 A. The fact that this capacitor current is only limited by the impedance of the short-circuit path during Fault 1 is not problematic as there is no critical equipment in the pathway and the capacitor can supply high current only for a short period, i.e. the energy dissipated is small. The short-circuit current is also

supplied from the node n_2. The supplement is visible by the current I_{SSCB} that flows in the reverse direction. The rise of this current is slower compared to the current I_{PFCC} as it is limited by the line inductance $L_{Line,2}$ and SSCB limiting inductance L_{CB}.

The voltage $V_{CB,gs}$ is the gate source voltage on the MOSFET $S_{CB,2}$. This voltage marks the start of the clearing process $\tau_{turn\ off,1}$. After SSCB MOSFETs are turned-off, the current I_{SSCB} continues to rise for a short period defined by the size of the snubber capacitor $C_{SN,2}$. Figure 6.11c shows the rise of the voltage V_{series} as well. The notable sharp rise of V_{series} after the fault inception is also visible on the voltage across the SSCB - V_{SSCB}. The voltage V_{SSCB} continues to rise to negative values, until it reaches approximately 400 V, which is the difference between short circuit voltage $V_{sc,f1}$ and node voltage V_2.

6.5.3 *Fault 2*

Figure 6.11d shows the waveforms during the clearing of short circuit Fault 2. Fault 2 is located at the point of injection of V_{series}. During Fault 2 the capacitor C_{in} contributes to the short circuit current which is visible from the rise of the current I_{PFCC}. During Fault 2 the rise of the current I_{PFCC} and I_{SSCB} is slower than during the Fault 1. This is a consequence of using limiting inductance L_{CB}. The peak current amplitude reached by the I_{SSCB} is around 60 A. However, a bulk of short-circuit power is supplied from node n_2, but it does not flow through the building block.

During Fault 2 the voltage V_{series} rises sharply to 50 V before the time $\tau_{turn\ off,2}$ when MOSFETs $S_{CB,1}$ and $S_{CB,2}$ are turned off. This sharp rise is also visible on the voltage V_{SSCB}. After $\tau_{turn\ off}$ current I_{SSCB} continues to rise, as well as the voltage V_{SSCB}. When the current I_{SSCB} reverses, so thus the voltage V_{series}. It is notable however, that the voltage V_{series} stabilizes after 30 μs and the PFCC can return into stable operation.

6.6 CONCLUDING REMARKS

A building block that integrates essential functionalities such as current limiting, voltage stepping and short-circuit protection is proposed in this chapter. The building block consists of a fully-rated solid-state circuit breaker (SSCB) that can fulfil more traditional protection and monitoring functions and a partially rated power flow control converter (PFCC). PFCC expands the operating possibilities of the building blocks and brings added value in different applications.

A simple steady-state equivalent model of PFCC is used to demonstrate the role of the building block in three chosen applications. The chosen applications are in various stages of technology readiness - street lighting, battery charging and meshed LVDC grid. When used for battery charging the PFCC acts as a charge controller and has to operate in a relatively large voltage range compared to other applications. However, even when voltage swing is assumed to be 40 % of the nominal grid voltage, the PFCC processes less than one third of the charging power. The street lighting system accumulates voltage drop which limits segment length. The PFCC acts as a voltage compensator, which in the presented scenario extends the segment length by 50 %. Prolonging of lines can bring potential economic benefits through material savings

and easier installation. Meshed grids in which the current follows the path of least action can run into local congestions. The proposed building block enhances the power capacity of the grid and can prevent the local congenstions by re-routing the current. In all three applications, PFCC processes only a fraction of the total system power. The power derating is the key to the economic savings and efficiency gains.

The operation of the building block is experimentally demonstrated. Moreover, an experimental proof of the grid short-circuit withstand capability is provided.

7

CONCLUSION

This thesis's primary goal is to study the devices needed for highly modular, scalable, and flexible electric power distribution systems that are well suited for integrating renewable energy sources (RES) and storage. Therefore, in this thesis, the basics of power electronics building blocks for (meshed) low voltage direct current (LVDC) systems are outlined. Every power distribution system's general objective is to safely and efficiently transport energy from the source to the load. In this thesis, this objective is explicitly studied for meshed LVDC systems. A partially rated power flow control converter is proposed, designed, and tested to facilitate efficient power distribution even in systems with a meshed topology. A solid-state circuit breaker with fast short-circuit detection is developed and tested to improve the LVDC system's safety. In the following text, the observations and findings from these two core areas are summarized for each research question, and some recommendations for future research are given.

7.1 REGARDING KEY QUESTIONS

How differential power processing concept can be utilized in design of a power flow control converter for LVDC systems? How to create an efficient mathematical tool to study the behaviour of the power flow control converter in meshed LVDC microgrids?

In this thesis a partially rated power flow control converter (PFCC) is proposed. The topology is based on the differential power processing concept, in which the converter processes only a fraction of the power flowing in the system in which it operates. The differential power processing concept was successfully applied for ac systems and carries the name of Unified Power Flow Controller.

The main benefits of the proposed solution are high operating efficiency with respect to the system and a wide range of control functions that it can full-fill. In order to investigate these benefits and influence of the proposed topology on LVDC system an efficient mathematical tool that connects the LVDC grid model and PFCC model was developed in chapter 2. The developed models allow to study the effects of PFCC in LVDC grid holistically. The derived small-signal models of the PFCC are a useful tool to design the control loops, which was also briefly demonstrated. The small-signal model was validated in frequency domain by measuring the control-to-output transfer functions. The large-signal PFCC model coupled with LVDC grid model was validated in time-domain. The experiments in chapter 2 also demonstrated the functionality of the PFCC in a meshed LVDC grid.

How a three-port converter should be controlled such that power flow in bipolar meshed LVDC microgrid is efficiently regulated?

In chapter 3, the PFCC concept is generalized into a three-port topology for bipolar meshed LVDC systems using a triple-active bridge converter (TAB). The concept and models from chapter 2 can be used both in unipolar and bipolar systems. However, when a TAB based topology is used, the amount of semiconductor and passives components is reduced. In chapter 3, a decoupling controller for TAB is proposed based on the Fourier series of high-frequency transformer currents. The decoupling controller is transformed and implemented in the digital domain using a standard off-the-shelf microcontroller. The proposed controller and its capability to decouple the TAB control loops are experimentally verified.

In Chapter 4, the operation limits of the TAB converter are analysed. Starting with the Fourier series description of the converter variables, the converter's soft-switching operation areas are derived. These areas take into account the converter parasitics such as the MOSFETs parasitic capacitances and switching dead-time. Moreover, the derivation of the soft-switching limits also defines the converter's operation modes via simple tables. The calculated soft-switching areas are validated in experiments. In Chapter 4, the losses related to the circulating power in the converter's high-frequency link are analysed. The chapter continues with a proposition of a simple modulation that extends soft-switching operation and reduces the current stress in the high-frequency link of TAB. In chapter 4 it is experimentally validated that the proposed modulation increases the converter efficiency via reduction of both switching and conduction losses. Calculated loss breakdown is also presented in chapter 4.

How a power flow control function block can be protected against grid short-circuits and become an efficient system building block of meshed LVDC microgrids?

The PFCC relies on de-rated components in terms of both voltage and current to achieve high operating efficiencies. However, the use of de-rated components makes the converter prone to grid failures, such as short-circuits. Therefore in chapter 6, an integrated building block consisting of fully rated solid-state circuit breaker (SSCB) and a partially rated PFCC is proposed. The chapter shows that the proposed building block's efficiency on the system level is over 99%. Furthermore, the building block's ability to withstand a bolted short-circuit on its terminals is experimentally validated.

Based on the market and application survey in chapter 6, three applications are chosen in which the benefits and operation of the integrated building block are demonstrated. The first application is DC charging, in which it is shown that even when the voltage swing of the battery is 40 %, the PFCC can have three times smaller voltage rating than a fully rated converter. The second application is public lighting. In the studied case, the proposed building block can extend the line length by 50 %. The last application is power capacity enhancement in a meshed grid. It is shown that the PFCC can enhance the power capacity by more than 20 % in the studied case. The last case study is a valuable addition to the analyses from chapter 2.

What are the design criteria of a solid-state circuit breaker?

Solid-state circuit breaker design criteria that consider the effect of different system parameters, detection methods, and detection delay times are derived in chapter 5. The derivation of the design criteria is based on a sensitivity analysis of the design space. The limitations of the SSCB equipped with different detection methods are analysed in a sensitivity analysis. The design is verified with a SSCB prototype with ultra-fast short-circuit detection.

Sensitivity analysis presents the rate of change of current (ROCOC) detection as a useful tool to optimise the snubber capacitors' size when the SSCB is expected to operate in grids with minimal self-inductances. The analysis shows the vitality of the snubber capacitance's optimal size as it is directly linked to the total clearing time and the peak short-circuit currents. Moreover, it is shown that the maximum operating loop inductance is an important design parameter that needs to be specified for every SSCB. As clarified in the analysis for maximum loop inductance values, the detection delay has minimal effect. Increasing the snubber capacitor can limit the maximum voltage on the blocking MOSFET, however, for the cost of increased peak fault currents and prolonged clearing times.

7.2 ON THE FUTURE RESEARCH

Partially Rated Power Flow Control Converter

The benefits of the proposed PFCC topologies were investigated in several applications and demonstrated experimentally. However, the operating limits investigation, as well as the candidate topology survey is not exhaustive. A rigorous study of topologies that implement differential power processing concepts in LVDC systems can lead to the discovery of more efficient and flexible options. Furthermore, the rating of the constituent components of the PFCC for abnormal operating conditions (e.g., short-circuits) was only briefly investigated. Therefore, analysing different failure modes, both internal and external to the PFCC, would bring vital knowledge for the proposed converter's future applications.

Solid-state Circuit Breakers

Solid-state circuit breakers will be the key to the efficient roll-out of LVDC. In this thesis, only an analytical investigation of the design criteria is provided. However, there are many unanswered questions regarding the development of SSCB. Firstly, the SSCB competes in many applications with hybrid circuit breakers (HCB). There is no clear figure of merit (FOM), which shows when HCB is more cost and energy-efficient. Defining FOM for the protection devices in LVDC would constitute an essential tool for system designers.

Secondly, the SSCB in this thesis is build using MOSFETs. However, several different semiconductor devices are available IGBTs, MOSFETs, JFETs, and IGCTs. Each of these devices has respective advantages and disadvantages. Currently, there are no

clear selection criteria for the application of these devices in SSCB. Benchmarking and optimising the devices for the protection application would help increase system efficiency and reduce design times.

SSCBs face significant overvoltages after interruption of the short-circuit currents. Thus the overvoltage surpassing circuits are essential to every SSCB design. However, metal oxide varistors (MOV) have a relatively short mean-time-between-failure and show significant degradation when repeatedly exposed to large current peaks. The RCD based snubbers offer better transient performance and smaller performance variation over the lifetime than the MOV, but in general, are less cost- and space-efficient. The optimal overvoltage suppression circuits will vary depending on the application power and voltage level. However, finding the optimal solutions will be detrimental to the cost and lifetime of future SSCBs.

Triple Active Bridge Converter

In chapter 3, a TAB converter is used as a basis of PFCC. The three-port topology shows promise for bipolar systems. However, the internal control of the TAB converter remains difficult. Several solutions already exist at the time of writing this thesis, yet most are relatively complex, and their stability and robustness are not understood. Further study of efficient decoupling controllers and their stability for multi-port converters is still required.

TAB converters can maintain zero voltage switching (ZVS) operation only under small variations of ac port voltages. Therefore, the development of modulations capable of extending ZVS operation under unbalanced operating conditions is needed to minimize EMI filters' size and improve converter operating efficiency.

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PUBLICATIONS

JOURNAL AND MAGAZINE PUBLICATIONS

J1 P. Purgat, N. van der Blij, Z. Qin, P. Bauer-*"Partially Rated Power Flow Control Converter Modeling for Low Voltage DC Grids"*, IEEE Journal of Emerging and Selected Topics in Power Electronics

J2 P. Purgat, S. Bandyopadhyay, Z. Qin, P. Bauer-*"Zero Voltage Switching Criteria of Triple Active Bridge Converter"*, IEEE Transactions on Power Electronics

J3 P. Purgat, N. van der Blij, Z. Qin, P. Bauer-*"Design Criteria of Solid-state circuit breakers in LVDC Grids"*, IET Power Electronics (*udner review*)

J4 P. Purgat, A. Shekhar, Z. Qin, P. Bauer-*"LVDC System Building Block with Integrated Power Flow Control and Short-Circuit Protection"*, IEEE Industrial Electronics Magazine (*udner review*)

J5 S. Bandyopadhyay, P. Purgat, Z. Qin, P. Bauer-*"A Multi-Active Bridge Converter with Inherently Decoupled Power Flows"*, IEEE Transactions on Power Electronics

J6 N. van der Blij, P. Purgat, T. B. Soeiro , L. M. Ramirez-Elizondo , M. T. J. Spaan, P. Bauer-*"Decentralized Plug-and-Play Protection Scheme for Low Voltage DC Grids"*, Energies

CHOSEN CONFERENCE CONTRIBUTIONS

C1 P. Purgat, R. A. Prakoso, L, Mackay, Z. Qin, P. Bauer-*"A partially rated DC-DC converter for power flow control in meshed LVDC distribution grids"*, 2018 IEEE Applied Power Electronics Conference and Exposition (APEC)

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C4 P. Purgat, S. Bandyopadhyay, Z. Qin, P. Bauer-*"Continuous Full Order Model of Triple Active Bridge Converter"*,2019 21st European Conference on Power Electronics and Applications (EPE)

C5 P. Purgat, L. Mackay, M. Schulz, Y. Han, L. Ramirez-Elizondo, M. März, P. Bauer-*"Design of a Power Flow Control Converter for Bipolar Meshed LVDC Distribution Grids"*,2018 IEEE 18th International Power Electronics and Motion Control Conference (PEMC)

C6 P. Purgat, Z. Qin, P. Bauer-"*Design of Solid-state Circuit Breaker for Partially Rated Power Flow Control Converter*", 2019 IEEE Third International Conference on DC Microgrids (ICDCM)

C7 P. Purgat, Z. Qin, , P. Bauer-"*On the Protection of the Power Flow Control Converter in Meshed Low Voltage DC Networks*", 2018 IEEE Energy Conversion Congress and Exposition (ECCE)

C8 P. Purgat, J. Popović-Gerber, P. Bauer-"*Modularity in power electronics: Conceptualization, classification and outlook*", 2017 IEEE Industrial Electronics Society Conference (IECON)

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CURRICULUM VITAE

Pavel Purgat was born in Slovakia in 1991. In 2011 he finished with distinction Bilingual Grammar School of Milan Hodža, Sučany, Slovak Republic. He received BSc. from the Czech Technical University in Prague in 2014 and MSc. from the Delft University of Technology in 2016. He became a PhD. candidate at the Delft University of Technology in 2016. In 2017-2018 he was a visiting researcher at the Fraunhofer-IISB in Erlangen, Germany. In 2020 he joined Eaton Industries GmbH in Vienna, Austria.