Design and Fabrication of a Measurement Interface for Smart IoT sensors

Hardware design

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Bsc graduation thesis

TU Delft Delft University of Technology

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Abstract

At this time, sensor developers rely on their own circuit board designs to test new sensors. This means a lot of time and money is spent on designing the custom interface for every newly designed sensor. This report describes a way to have a configurable test bench for sensors. The system consists of a data acquisition unit and multiple circuit boards to be able to have a certain level of reconfigurability for the used pins. This system is also able to generate simple signals. It is therefore a replacement for certain instruments as well. The test bench has 9 configurable pins and a number of external connections. It is simple to use and can do its job automatically. This report focuses on the hardware part, where all the switching and amplification is done. We recommend to use the system on a trial basis, because it is not completely functional yet.

Preface

This thesis is written in the context of the Bachelor Graduation Project. The project proposal is given by the microelectronics part of the Electronic Components, Technology and Materials (ECTM) group at the TU Delft. The goal of the project is to design a measurement interface to test new sensors. This interface should be used to test the sensors, instead of needing to design a new test setup for every new sensor.

We would like to thank the thesis supervisors Sten Vollebregt and PhD student Joost Romijn, who guided us during our Bachelor Graduation Project. We would also like to thank the members of the defense committee Dr.ir. M.A.P. Pertijs as chair and Dr. C. GarcÃŋa Almudever as jury member.

Contents

Chapter 1

Introduction

The aim of the project is to design a reconfigurable measurement interface to test new sensors. This measurement interface should make testing these sensors easier, faster and cheaper.

This thesis is mainly focused on the hardware part. Figure 1-1 shows a global project overview.

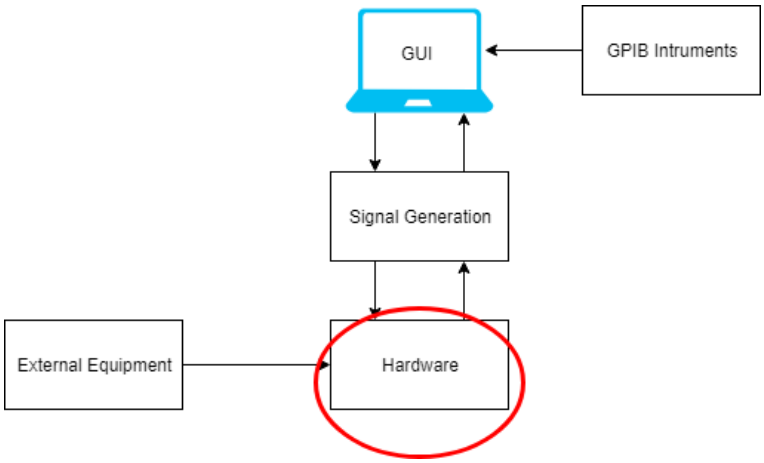


Figure 1-1: Global project overview

1-1 State-of-the-art analysis

Modern sensor testing is done on a chip by chip basis. For each different sensor produced, a custom interface with the chip is prepared. Within this interface accuracy is important, since accuracy is an important factor concerning the functionality of the sensor. To make testing simpler and more efficient, a reconfigurable measurement interface is desired. This will save chip developers time and money when testing a new sensor.

There are some reconfigurable test setups available, for example the run-time reconfigurable instrument working with an FPGA board [16]. However this is a different implementation, since an FPGA board does not have the same possibilities as a DAQ regarding the signal generation. This is one of the reasons why a DAQ is chosen instead of an FPGA board. The reasoning for choosing a DAQ can be found in Chapter 3.

Since high-accuracy is important for the testing of the sensors, an example circuit on a high accuracy A/D interface for capacitive sensors [3] is shown in Figure 1-2. For the circuit it is stated that it has a single path structure instead of cascaded, since this is less sensitive to non-ideal effects [3].

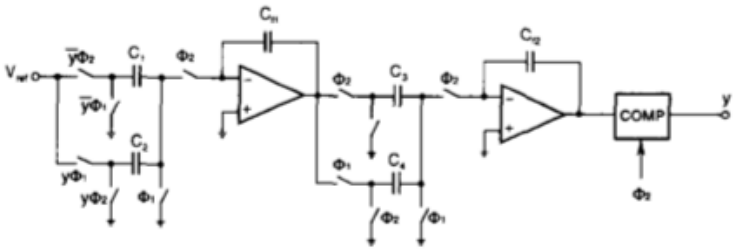


Figure 1-2: Second-order capacitor readout circuit

The testing circuits of these sensors are sometimes quite simple. The film sensor is a sensor of which the test setup is discussed in a paper [6]. It is a one purpose sensor with a simplistic test circuit, which can be seen in Figure 1-3, and a setup that is not reconfigurable. However this test setup is given as an example, but the measurement interface is not something like this read out circuit. Since it is an interface to connect the sensor which has to be tested to the needed test setup. If for every new sensor a new simple test setup, like with the film sensor, has to be designed and fabricated, it is eventually way more expensive then having one complicated setup.

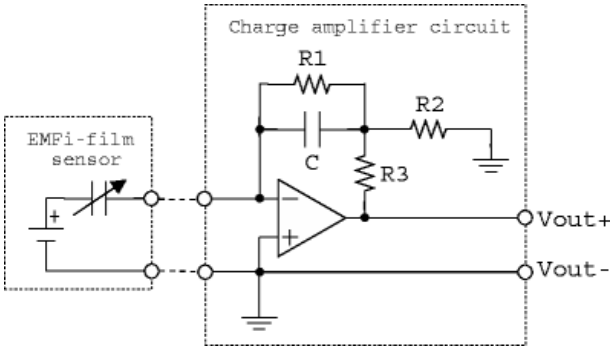


Figure 1-3: Circuit film sensor

1-2 Problem definition

Currently for every new sensor that is developed a new chip interface is designed, which means that at facilities such as universities, where a lot of different sensors are developed, a huge amount of different measurement interfaces are lying around. In general these old measurement interfaces are kept, but never used again. This is expensive as well as bad for the environment. Keeping all these unused old measurement interfaces means needing a lot of storage space, which could be used for other things. Even though there is no urgent need for such a measurement interface, it would have a lot of benefits, such as more storage space, less costs, less time consuming design process and it would be better for the environment.

When the measurement interface is developed it should be able act as an interface for most of the developed sensors at the department of the thesis supervisors. It will also reduce the amount of external devices needed to properly test the sensor, since several test signals are already generated by the measurement interface.

Chapter 2

Programme of requirements

In this chapter all requirements are stated. These requirements are meant to accomplish designing a measurement interface for internet of things sensors. The interface has as goal to act as a general interface for the test setup for the sensors which have to be tested. This interface, when finished, will be used by the microelectronics department of the TU Delft. This makes it extra important to keep the requirements in mind during the whole design process.

2-1 Requirements

1. Graphical User Interface (GUI) (not discussed in this thesis)
   - The GUI runs on the user's laptop
   - No additional software is required to run the GUI (university software such as Matlab, is accepted)
   - The GUI allows the user to assign roles to each pin of the chip under measurement, the different roles include; analog in, analog out, digital in, digital out, power supply+, power supply-, external power supply+, external measurement out
   - The GUI allows the user to specify his/her measurement in terms of the input signals (waveform generation), time, output handling and saving/visualizing the measured data
   - The GUI allows GPIB commands to use ICCAP for direct control of SMUs
   - The interface has a wired communication connection to the user's laptop
2. Input/output
   - The system allows the connection of three external measurement tools
   - The system has one 48p DIP socket (commonly used at EKL) for the chip under measurement
3. Structural and usage
   - The system dimensions are within 200x125x45mm
   - The system allows mounting in a future housing
4. External analog input/output signals
   - All pins are rated up to $\pm 100V$ and $100mA$
   - The system consists of 10 external analog input connections
   - The externally connected signals must be sent to the sensor directly
   - The system allows two additional external power connections rated up to $\pm 200V$ and $1A$
5. Internal signal generation
   - Up to 9 signals are generated
   - Up to 4 basic analog signals
   - The frequency of the analog signals is rated up to $100kHz$

- The amplitude of the analog signals is rated up to $\pm 10V$
- All nine signals can be used to generate bias voltages of $3.3V$ $5V$ $10V$ $12V$ or $24V$
- Current of generated signals has to be measured
- The current of the generated signals should be at least enough to drive the gate of a transistor
- The output voltage has an accuracy of tenths of volts

6. Power supply
   - External power connection of up to $\pm 30V$
   - The power supply is connected to 6 pins
7. Pin connections
   - All pins interfacing with the chip under measurement are fully reconfigurable
   - The system has one 48p connector to connect to an external smaller board
   - The external board is to ensure that the chip can also be tested at $2m$ from the test setup
8. Costs
   - The costs of all the hardware must be less than €1000

Chapter 3

Theoretical design

In this chapter all designs, except the final design, are discussed. The final design and the optimization of that design is discussed in Chapter 4. During the design phase the following requirements from Chapter 2 are kept in mind since they should be met with the implementation of the final design.

- Up to 9 signals have to be generated
- Up to 4 basic analog signals have to be generated
- The frequency of the analog signals is rated up to 100kHz
- All 9 signals must have the option to generate bias voltages at $3.3V$, $5V$, $10V$, $12V$, $24V$
- The power supply should be connected to power connections of up to $30V$

3-1 Research

At the begin of the research stage, almost all options concerning components were open. This meant that it had to be determined which requirements are the most important and what constraints these requirements gave. Since one of the requirements stated that there should be analog and digital inputs and outputs, there should be appropriate hardware for analog signals. An other requirement states that waveforms have to be generated. This means that in addition to just routing the signals, simple waveforms also have to be made.

During the research it became clear that generating analog signals without a digital to analog converter is not possible. This means that the generation of the analog signals would have to be done by for example an FPGA board. While researching the possibility of using an FPGA board, it became clear that a very expensive FPGA would have to be used to be able to achieve the desired level of freedom, because many output pins are needed. In addition, analog to digital converters are needed to generate analog signals, as well as digital to analog converters to measure signals. An other option would be to use a microcontroller. Microcontrollers are powerful, but in general these have very few pins. A lot of extension modules would be needed. This would result in high costs and difficulty. At the beginning of the project the thesis supervisors mentioned that a National Instruments Data acquisition unit (DAQ) was available to use. Quite soon it became clear that it was possible to generate analog signals with this DAQ, the PXI6229 [18], and to measure analog signals. These analog signals can be generated on 4 pins of the DAQ. The other pins are digital pins. This means that all pins can generate digital signals and only 4 can generate analog signals. The DAQ has 48 digital pins, which makes the driving of the relays easier. The other subgroups looked into LABVIEW, the program that is used to control the DAQ, and concluded it was realistic to use this program. Therefore the choice was made to use the DAQ.

3-2 Selection circuit

The selection of the correct voltage level can be implemented in several ways. Regardless of which implementation is chosen, it is necessary to implement some kind of switching mechanism. This can be implemented with reed relays, solid state relays (SSRs), electromechanical relays or transistors. There are several advantages and disadvantages for using either relays or transistors.

Using transistors would have the advantage of the small component size, 5 by 5 mm, compared to 10 by 20 mm for electromechanical relays, 5 by 20 mm for reed relays and 10 mm by 40 mm for a small package SSR relay. These are the approximate values of commonly used relays and transistors. However using transistors with the circuit design from Section 3-5, the transistors would be short circuited, which is a problem that cannot easily be fixed.

Using SSRs, reed relays or relays would have the advantage of having a simple drive circuit. Therefore using some kind of relay is a better option than using transistors. The following considerations about the advantages and disadvantages regarding the relays are based on a National Instruments article [20].

With reed relays and electromechanical relays there is a power consumption, because the components are made using a coil. The current going through this coil causes the power consumption, while with the SSRs it is the contact resistance. This means a higher resistance when closed and a lower resistance when open, which results in power consumption when closed and possible signal noise. There are a few important differences between these types of relays, but only the relevant ones are evaluated.

Using SSRs would have the advantage of a shorter switching time and a longer life time than the other relays, since there are no mechanical parts in SSRs. A disadvantage would be the size, which is at least twice that of electromechanical relays. Since a SSR is implemented with photo-sensitive MOSFET, the disadvantages of using transistors also apply to SSRs.

The disadvantages of using electromechanical relays are the large switching times, contact bounce and the large component size compared to the reed relays.

Reed relays have a smaller switching time and are smaller than electromechanical relays, but the contact bounce is still a disadvantage.

The contact bounce is a common problem with mechanical relays [1]. It is the bouncing apart of the spring like metals in the relays, which can happen once or several times. This problem influences the reliability of the system in which relays are used, but this is only for a short time after switching. This means that after some time the system is reliable again [12].

3-3 Concept

All possible options of the system are schematically shown in Table 3-1 and Table 3-2. In both tables the ● symbol is used if the suggested option is implemented and the ❍ symbol is used if the suggested option is partially implemented. If it is relevant how many times the option is implemented, this number is stated in the tables. Furthermore a blank space in the table means that it is not implemented for that part.

Table 3-1: Options of the system

Part	Current measurement	External bypass	Reconfigurable
4 A/D circuits	❍	●	●
5 D circuits	●	●	●

Table 3-2: Caption

Part	200V	Ext. bypass connections	Ext. connections
External PCB		9	13
Socket PCB	●	9	13

3-4 First design

A systematic overview of this design is shown in Appendix A-1 and Appendix A-2. The first design idea, would have used 17 multiplexers. These multiplexers are used to make sure that all digital and analog signals can be brought to 5 different voltages levels, since there are not enough output pins on the DAQ. The multiplexers would be used for all signals, the driver signals as well as the data signals. Since multiplexers introduce signal noise and signal decay, using multiplexers would mean that the data signals would be corrupted and the number of driver signals would be 51. To be able to drive these signals, four 16-bit IO expanders would be used. This would complicate the system a lot. To bring the voltage levels up and down, the saturation effect of opamps is used. By controlling the supplied voltage of the opamps, the maximum output voltage can be controlled relatively easily. However, the rail to rail voltage output swing has to be checked, because it is required that the opamp will output a signal with a voltage similar of that of the supply voltage.

This design is changed mainly because the corruption of the data signals is unacceptable for the purpose of the system.

3-5 Second design

The second design idea, would not have multiplexers. It would use transistors to control the voltage level to the opamps. To control these transistors, IO expanders would be used. These are necessary because there are not enough output pins on the DAQ. The amount of opamps is also decreased. Instead of using an opamp for every voltage level, and for every signal, one opamp is used for every signal, which is a factor five more effective. The voltage select part of the circuit can be found in Figure 3-1.

When this circuit is evaluated, it can be seen that there will always be a short between either the ground and the voltages, or between the voltages. For example, when CTRL 1 will be a '1', CTRL 2 will be a '1' and CTRL 3 will be a '0', there will be $5V$ on the output (from CTRL 3) as well as 2 times a GND. This will create a short. Something similar will happen for every combination.

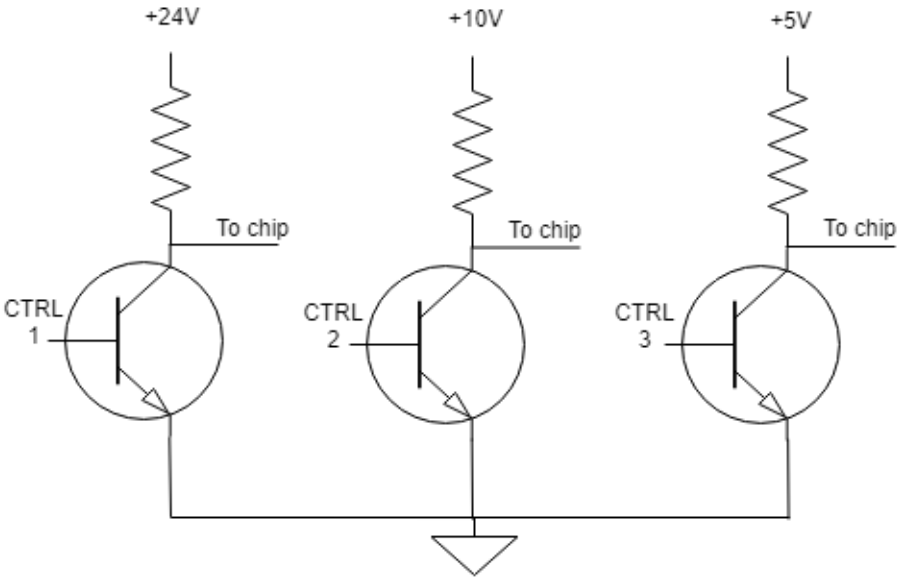


Figure 3-1: Transistor network for switching voltages

There is no easy way to avoid this without increasing the number of opamps with a factor five. Therefore it is preferred to change the transistors, rather than increasing the number of opamps while keeping the transistors in the design.

3-6 Third design

The third design idea, continues upon the idea of the second design, but instead of using transistors to switch the voltage levels, reed relays are used. These reed relays are a reliable way to switch a signal or power a path on or off. These relays still need a lot of output pins on the DAQ, so the IO expanders are still necessary. These expanders, however, still have to be controlled by the DAQ through I2C. During a meeting with the other subgroup, it became clear that I2C would be very complicated to use with LABVIEW and would take a lot of time.

Therefore a different design had to be made, with either no need to increase the number of output pins or increasing the number of output pins without using IO expanders.

3-7 Fourth design

The fourth design idea, is similar to the third idea, with the IO expanders exchanged for multiplexers and OR gates. With 9 multiplexers and 6 OR gates, all the different options can be made. The system with the multiplexers and OR gates is a part of another subgroup. Since this system is needed to control the reed relays via the OR gates, it is mentioned here. However the full explanation of this system can be found in the thesis of the signal generation subgroup.

Chapter 4

Final design

A systematic overview of this design is shown in Figure 4-1.

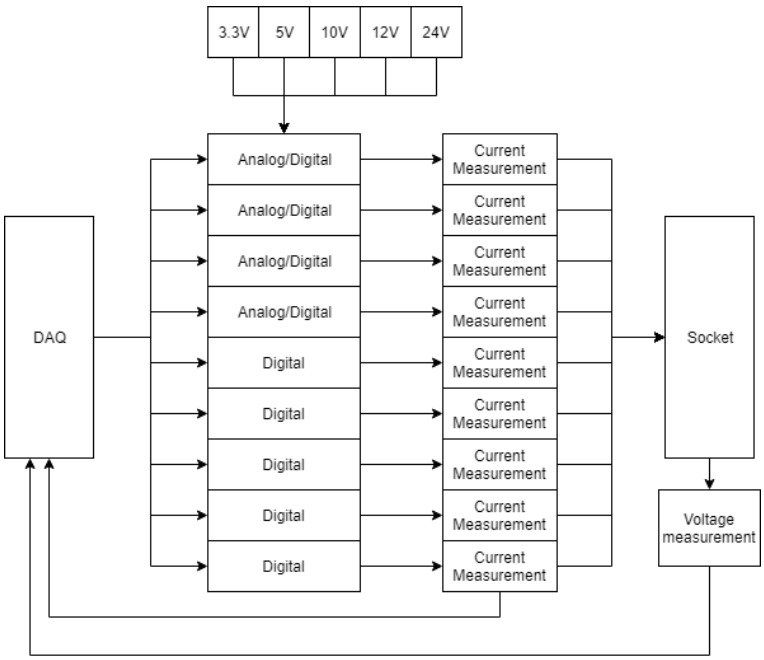


Figure 4-1: Global overview of the system

The final design consist of the following building blocks, that will be discussed in this chapter, namely an analog voltage follower circuit, a digital amplifying circuit and a current measuring circuit. It will have 55 reed relays to switch these voltage levels. These reed relays will need a lot of driver signals coming from the DAQ. Therefore 9 multiplexers and 6 OR gates are used, which are a part of the signal generation subgroup. This design is an optimized version of the fourth design in Section 3-7. In addition, there is also a power supply block. Since there are a lot of different signals which are generated in the total system, less external equipment will probably be needed.

4-1 Analog voltage follower

The DAQ can not supply enough power to the generated signals. There are multiple solutions to this problem. The first solution is to use a transistor, driven by the generated signal. However, this solution has a drop in output voltage. This drop has to be corrected in the

DAQ itself, a higher output voltage should be applied. This would limit the maximum output voltage of the analog signals. However, this would be able to generate a high current.

The second solution is to implement a voltage follower, which makes sure that enough current is available. The output voltage of this opamp is the same as the input voltage, but with a higher current. This method is chosen.

The opamp that is used for this is connected to the VDD and VSS planes, as shown in Figure 4-2. This opamp uses negative feedback to create a gain of 1. To stabilize the power supplied to the opamp, small capacitors are added from the power pins to the ground. Four of these circuits are used in the system, to make sure the requirements are met. The circuit, seen in Figure 4-2, is tested in Chapter 6.

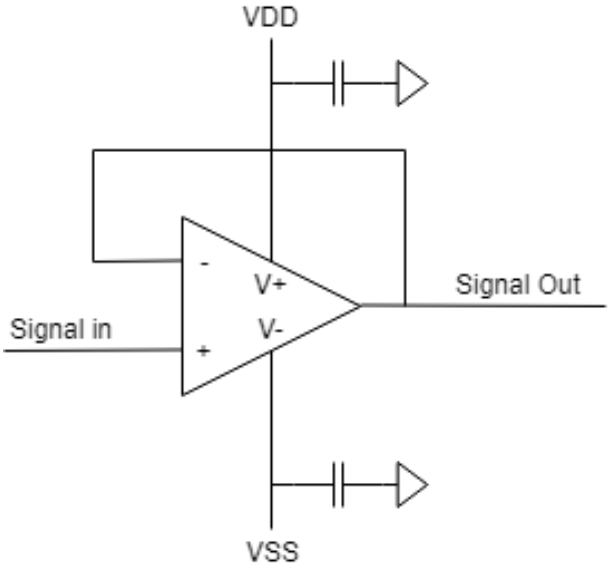


Figure 4-2: Analog voltage follower using the OPA445 opamp

4-2 Digital amplifier

To be able to have the possibility to amplify digital generated signals, another circuit is needed. Here two options are discussed. The first option uses a digitally controlled programmable gain amplifier. The gain of this amplifier can be controlled by setting a couple of bits. Every combination has a different amplification. However, these amplifications can not be changed. This makes the circuit not versatile enough. Thes econd circuit consists of an opamp that saturates at the desired voltage. To achieve this, different power supply voltages are connected at the V+ terminal. How this switching is done will be discussed in Section 4-6. The used circuit is shown in Figure 4-3.
This option is chosen because of the level of versatility. Nine of these blocks are used, to make sure the requirements are met. The output voltages are $3.3V$, $5V$, $10V$, $12V$ and $24V$, so this requirement is also met.

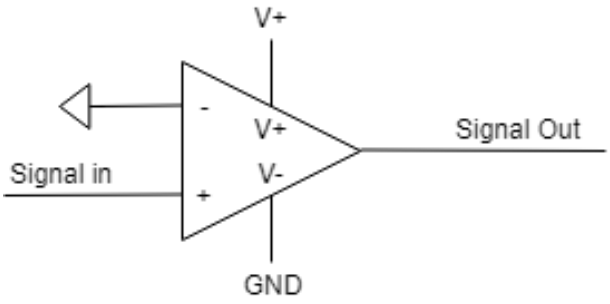


Figure 4-3: Amplifying circuit for digital signals

4-3 Current measuring

This design has the possibility to measure the current of the generated signal. Two options to do this are discussed. The first option involves measuring the voltage over a resistor in series with the signal path. The positive terminal and the negative terminal can then be measured by connecting them both to an analog in port of the DAQ. Using $I = \frac{U}{R}$, the current can then be calculated. However, this will also need voltage dividers, to control the maximum voltage that enters the DAQ. In addition, buffer amplifiers are needed, to make sure that the measurement does not interfere with the signal. This approach uses a lot of components, and because of the voltage divider, the accuracy is not very high. An other option is to use a current sensing amplifier, which senses the current through a 1Ω resistor in series with the signal path. The resulting signal will then be brought to a level between $0V$ and $10V$. In the datasheet of the INA169 [19] the circuit in Figure 4-4 is found.

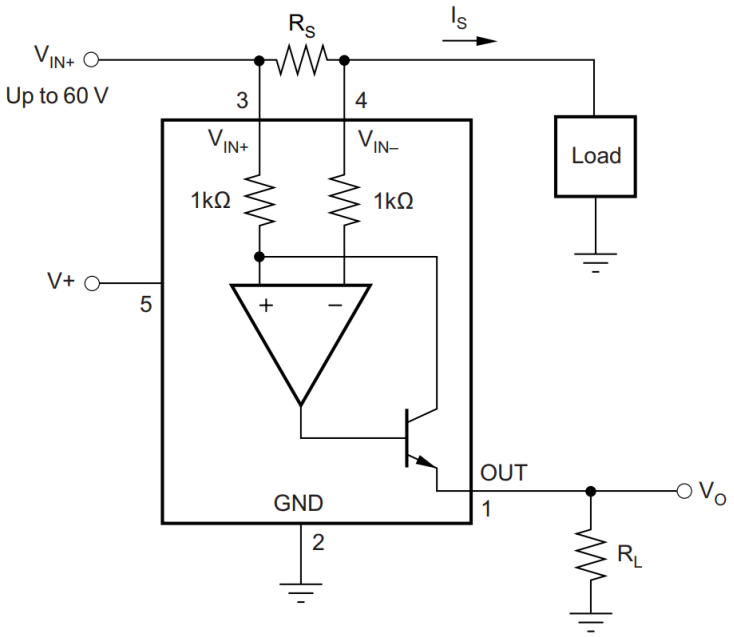


Figure 4-4: Current sensing circuit with the INA169

The values of R_s and V_o can be calculated using equation 4-1[19].

$$V_o = \frac{I_s R_s R_L}{1k} \tag{4-1}$$

To have a minimal signal distortion, an R_s value of 1Ω is used. Because the maximum output voltage has to be below $10V$, and the maximum current is $100mA$, a R_L value of $100k\Omega$ is used.

4-4 Output voltage measuring

Another possibility is to measure the output voltage of the analog and digital pins. When there is no signal generated at the DAQ, this can be measured. This is to make sure that the voltage divider that is used does not affect the generated signal. As stated, there is a voltage divider present that makes sure that the maximum voltage delivered to the input of the DAQ can not exceed $10V$. The divider has a division of 20:1, so that when there is $200V$ present (the maximum value for a pin), the voltage to the DAQ does not exceed $10V$. However, this does affect the accuracy of the measurement by a factor 20 as well. As can be found in [18], these analog inputs can withstand a voltage of $25V$, which translates to a voltage spike of $500V$. A relay can be found between the pin and the DAQ as well, so that when no measurements are taken, a voltage spike can not damage the DAQ.

4-5 Power supply design

In order to make the opamps saturate at a certain voltage level, there are two options: externally connect all required voltages, or generate them internally. The second option is chosen, to make sure that there is only one external power supply needed. This will make the setup easier to use. The choice for a simple circuit containing the LM317HV linear regulator is made, with an input voltage of $\pm 30V$.

Figure 4-5 shows the circuit, which is found in the datasheet of the LM317HV regulator [14]. This circuit is used four times to make $3.3V$, $10V$, $12V$ and $24V$. However the values of the resistors are changed. These values can be calculated by using Equation 4-2. I_{adj} has a typical value of $50\mu A$ with a maximum of $100\mu A$.

$$V_{out} = 1.25V \left(1 + \frac{R2}{R1}\right) + I_{adj}(R2) \tag{4-2}$$

Resistor R1 has to have a value of around 100Ω to 300Ω. Checking the parts cabinet at the Tellegen Hall, values of 100, 120, 150, 180, 220 and 270 Ω are found. By filling in these values in Equation 4-2, the values for R2 can be calculated for every voltage level. Then it can be checked if these values are available. However, the output voltage has to be tested to be sure it matches the desired voltages. This will be done in Section 6-3. The calculated values for R2 can be found in Table 4-1.

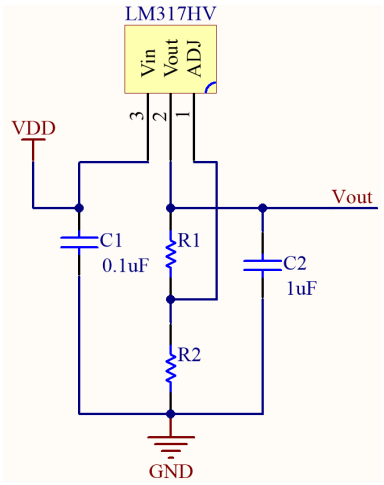


Figure 4-5: LM317HV circuit

Table 4-1: Calculated values for R1 and R2

Voltage	**R1** (Ω)	**R2** (Ω)
$3.3V$	100	163
$10V$	120	835
$12V$	120	856
$24V$	100	1812

These values are not available, but have the lowest deviation from the available values. Also filter capacitors are used, to make sure that the supplied (and therefore created) voltage is as clean as possible. The $5V$ power can be pulled straight out of the DAQ, which can supply $1A$ per $5V$ pin, which should be plenty. There is also the possibility to use protection diodes. However, no protection is used for voltages lower than $25V$ [14]. The maximum voltage generated in the system is $24V$.

4-6 Switching

To be able to switch between all the different modes, relays are used. These are controlled by signals coming from the multiplexers and OR gates, and are generated by the DAQ. These relays have a diode in parallel with the input, to make sure that the DAQ outputs do not suffer from the voltage spikes caused by the switching off of the coil [17].

All designed modes can be switched, but with this implementation not all pins interfacing with the chip are fully reconfigurable as stated in the requirements in Chapter 2. Only 9 pins are fully reconfigurable. This choice is made, because otherwise around 2000 reed relays would be needed instead of 55. This would mean a lot more driver signals and a lot bigger PCB. Since the price for a reed relays is about €1, see Table 5-1, using 2000 reed relays would cost twice the budget for all the hardware as stated in Chapter 2. Therefore full reconfigurability for all pins is not achieved.

4-7 Total design

Figure A-3 shows one complete analog/digital block. Here all connections can be seen. There are multiple of this blocks. The digital blocks are the same, but lack the analog bottom part. In addition they have more voltage options. The select signals are the selection signals, with which the different modes can be selected. The analog-in signals are the measurement signals, which send back the measurements to the DAQ. The $24V$ and $12V$, $10V$ and $5V$ for the digital blocks, can be connected or disconnected, to make sure that the correct amplification is present for the signals.

To protect the DAQ itself from high inrush currents, all inputs are shielded from the chip itself. This is done by either an opamp, a relay or both. The relays can hold off $250V$ DC signals, or $1500V$ AC signals with a current of $0.5A$ [8].

4-8 Optimization

The power traces on the PCB have a certain induction. This creates ripple in the power signal. To prevent this, a decoupling capacitor can be used, or decoupling power planes can be used [2]. Both options will be discussed in Chapter 7. The value of this decoupling capacitors can be calculated by Equation 4-3 [2].

$$C = \frac{dQ}{dV} = \frac{I}{2f_c \times Vdd \times n} \tag{4-3}$$

In this equation I is the maximum current through the power traces. There are 6 VDD pins and 6 VSS pins. The maximum current through the traces will then be $I = 6 \cdot 0.1A = 0.6A$. The maximum frequency is unknown, although the maximum generated frequency of the DAQ is $100kHz$. Therefore it is assumed that this frequency will be $100kHz$. The maximum value for VDD and VSS will be $30V$. However, it is possible to connect lower voltages, so the value of the capacitor is calculated with a VDD and VSS of 10V. One would not want to go lower than this, because there would be serious limitations to the output voltages of the circuit. In this equation, n is the amount of ripple that is allowed. There is no hard constraint on this, but the lower the better. The capacitance value is therefore calculated using 1% ripple. When plugging all of these values into Equation 4-3, it is found that the capacitor should have a value of $30\mu F$. Since the location of the different $+30V$ connections and $-30V$ connections are rather close together, within a couple of cm, only one capacitor for the three $+30V$ connections and one for the three $-30V$ connections is used. This capacitor is placed as close to the connections as possible. This minimizes the amount of line inductance.

Chapter 5

Component choices

In this chapter all components in Chapters 3 and 4 are discussed. A complete overview of how many pieces are used for all components can be found in Table 5-1.

5-1 Operational amplifiers

Four different types of operational amplifiers are used, since there are four types of things that need to be done. The first type is used to perform a current measurement. The second type is used to bring the signals to the desired voltage levels. The third type is used to generate the different voltage levels. The fourth type is used to increase the current level of the signals.

5-1-1 INA169

This opamp is used for the current measurement of the digital signals. It can measure the current without changing the voltage or current level of the measured signal. This specific opamp is chosen because the supply voltage has a maximum value of $60V$, as seen in the INA169 datasheet [19], which is higher than the highest voltage level, $24V$, and therefore sufficient. The reason that the maximum voltage is more than twice the highest needed voltage, is because there was a big jump in maximum voltages for current sensor devices. Therefore this was one of the few options.

5-1-2 LM6132

This opamp is used for the digital voltage amplification circuit, to bring the signals to the desired voltage level, as discussed in 4. At the V+ power supply terminal of this opamp the chosen voltage level is supplied. The V- terminal is connect to the ground. With this setup the opamp is used in saturation mode, which causes the V+ value to be on the output of the opamp. The absolute maximum value of the voltage difference between V+ and V- is $35V$, if this value is exceeded, damage may occur. However the recommended operating range of the supply voltage is $1.8V \leq V+ \leq 24V$. Both of these values can be found in the LM6132 datasheet [11]. Therefore the maximum value of $24V$ that is used is within the recommended range. The maximum offset for a supply voltage of $24V$ is $0.2V$, with lower values for the supply voltage the output swing can differ. So if the offset causes the signal to be $24.2V$, it is just outside the recommended range. But nowhere close to the absolute maximum value. Therefore this is an acceptable value. However the maximum offset voltage is always less than $0.5V$, as seen in the datasheet [11], this is in line with the tenths of volts accuracy in Chapter 2.

5-1-3 LM317HV

This regulator is used to generate the different voltage levels, which are used as a power supply for the multiple circuits that use the same voltage level. Since the input voltages are the positive power supplies, the maximum value for the output voltage is limited to this value. This means that the maximum output voltage of this opamp is $30V$, since this is the standard power supply value for the measurement interface. Since the opamps are used for several circuits it is important that they can deliver enough power, to make sure they give the correct voltage value. The LM317HV is chosen, because it has an output current of $1.5A$ and a maximum input to output voltage differential of $60V$, as can be seen in the datasheet [14]. Since the maximum differential voltage which is needed is $30V - 3.3V$, the $60V$ is clearly more than enough.

5-1-4 OPA445

The OPA445 is used for the analog voltage follower circuit. As stated in Chapter 2 the current level should be increased to at least be able to drive a transistor. A commonly used current value to drive a MOSFET is $10mA$. It is needed to increase the current value since, the analog signals which are generated on the DAQ have a really low current level, about $1mA$. The easiest way to increase the current level is with a non-inverting voltage follower.

This opamp is suitable to use as a voltage follower to increase the current level, since the output current of the OPA445 is $15mA$, which can be found in the datasheet [7]. However depending on the temperature this value may deviate, as can be seen in Figure 5-1 from the datasheet. As can be seen in the figure, as long as the temperature is under 100°C, the output current is more than $10mA$. Therefore this implementation is suitable to drive a transistor. The complete implementation of this voltage follower circuit is explained in Chapter 4.

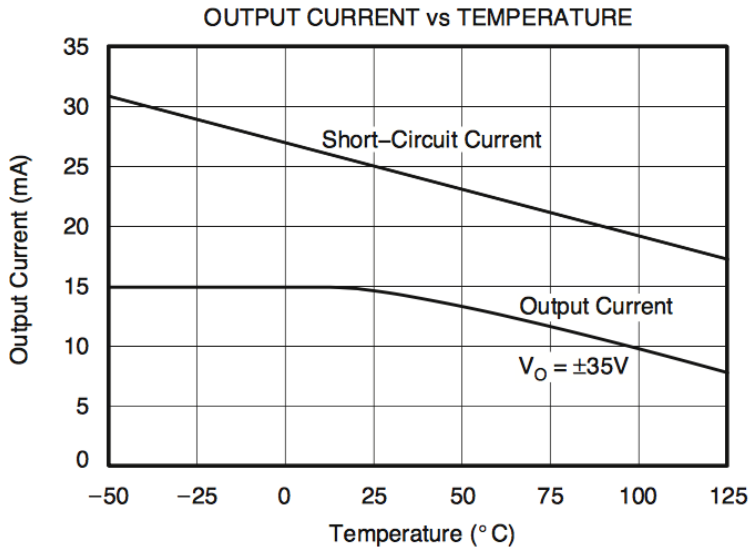


Figure 5-1: Output current vs temperature characteristic for the OPA445

5-2 Relays

Relays are used to select one of the several possible voltage levels and to choose which mode the total circuit is working in. These different modes are all controlled with relays to make sure that they are isolated. Using relays makes it possible to implement the design discussed in Chapter 4 in a simple way.

Reed relays are used, because they are a lot smaller than electromechanical relays, as discussed in Chapter 1. Since the PCB should be as small as possible, using a small relay is preferred. However this is not the main reason that the reed relays are chosen. Reed relays also have a longer life span and are faster than electromechanical relays [20], while the disadvantage of the contact bounce is not enough reason to not choose the reed relays. The different options concerning relays can also be read in Chapter 1.

The reason that the HE3621A0500 reed relay is chosen is, because it has a hold-off voltage of $250V$ and a maximum switching current of $0.5A$. This makes sure that the relay, and therefore the DAQ is safe from voltage spikes.

These relays are used with a diode in parallel as suggested in the datasheet [8], to protect the coil drive circuit.

5-3 Connectors

The 48 contacts socket is used for mounting the sensor. It is a universal test socket, which is why it is ideal to use for this measurement interface. There is a handle to ensure connection of the mounted device and easy removal. The pin layout and how it is implemented can be found in Section 7-3.

The 68 pin connectors are used to connect the DAQ PCB. This is done with two of these connector cables.

A high speed coaxial cable, the FCF8-30-01-L-75.00-S [21], is used to connect the external PCB to the socket PCB. This cable is bought since the costs of making the cable would be about the same as buying it. An already put together cable will be more accurate than making a cable, because the wires are micro coaxial cables and the size makes it more likely to make mistakes, and hand soldered connections can have more deviations than machine soldered connections.

The $\pm 30V$ power supply will be connected via three generic banana plugs, which are available at the Tellegen Hall.

5-4 Resistors

Resistors are used for voltage dividers in Section 4-4, the voltage regulator circuit in Section 4-5 and for current measurements in 8-3.

For the voltage regulator circuit generic resistors are used, which are available at the Tellegen Hall.

For the current measurement 1Ω resistors are used to measure the current, while keeping the voltage at the same level.

5-5 Multiplexers

Multiplexers are used for the driver signals. There are a lot of driver signals needed, way more than the number of output pins that are available on the DAQ. Therefore, it is necessary to increase the number of driver signals.

The disadvantage of using multiplexers is that noise is introduced and signal decay will occur. However this is not problematic, since the multiplexers are only used for driver signals. This means that it is only important that the difference between a '0' and a '1' should be clear, which is the case with the output signals of the multiplexers.

Why the SN74LV4051AN multiplexers [15] are used and how they are implemented can be read in the bachelor thesis of the signal generation subgroup.

5-6 Capacitors

Some capacitors are used for the decoupling of the power supply. How this is implemented is discussed in Section 4-8.

Some capacitors are used for the OPA445 circuit. This is discussed in Section 4-1.

Some capacitors are used for the LM317HV circuit, as can be seen in Section 4-5.

The used capacitors are available at the Tellegen Hall. This is preferred since this is cheaper and there is a large variety of capacitors available

5-7 Diodes

Diodes are used to protect the DAQ pins that power the coil from voltage spikes generated by the coil when deactivated [17]. A surface mounted device is chosen to minimize the needed space. The diode has a rating of $800V$ and $2A$, so the diode can withstand high voltage spikes. The maximum switching current is $0.5A$ [8]. The switching voltage is $5V$. To make sure that the diode acts fast, a Schottky diode is used [22].

5-8 Heat sinks

The heat sinks are not necessary, but are preferred to make sure that the high voltage regulators will not get too hot. The biggest determining factor for choosing the heat sinks is the size, because the PCB should be as small as possible. This results in using small and cheap heat sinks.

When the temperature exceeds 50°C the output voltage deviation increases more rapidly than the temperature, this can be seen in figure 5-2 from the LM317HV datasheet [14]. The

thermal resistance of the heat sinks is $R_w = 21°\text{C}/W$ [9]. To ensure a good conductivity a thermal grease is put between the heat sinks and the component. This thermal grease fills the air gaps, which improves the conductivity. Since four high voltage regulators are used, four heat sinks will be needed.

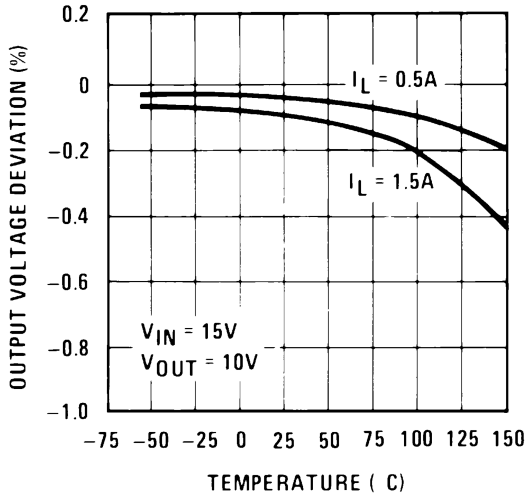


Figure 5-2: Voltage deviation characteristic for the LM317HV

5-9 PCBs

Most of the used components are soldered onto the designed PCBs, but for the fuses and operational amplifiers this is not the case. The fuses are put in to fuse holders to make sure that when a fuse breaks it can easily be replaced. For the same reason IC-sockets are used on the PCB. How the three PCBs are designed is discussed in Chapter 7.

5-10 Costs

Adding all the costs from Table 5-1 together results in about €800. Since the mandatory requirement involving costs in Chapter 2 states that the costs of the project must be less than €1000. It is clear that this requirement is met.

Table 5-1: Used components

Component type	Component	Used amount	Total cost (€)
Connector	68 pin connector	2	34,88
Capacitors	generic	18	0
Resistors	generic	52	4,97
Operational amplifiers	INA169	13	27,75
Operational amplifiers	LM6132	9	30,60
Operational amplifiers	LM317HV	4	12,36
Multiplexers	SN74LV4051AN	9	6,6
Operational amplifiers	OPA445	4	54,75
OR gates	SN74AC32N	6	2,64
Reed relays	HE3621A0500	55	56,36
Fuse holders	open design fuse holder	4	2,99
Fuses	ESKA522618	2	3,20
Fuses	ESKA522621	2	3,20
Socket	48 contacts	2	39,68
IC Sockets	8/14/16 pins	28	11,38
Connector	coax	24	28,75
Connector	inter-board	2	9,30
Cable	high-speed coax	1	156,00
Diodes	DO-214AA	55	8,10
PCB	2 layers	2	96,44
PCB	6 layers	1	204,76
Banana plugs	generic	3	0
Total costs			796,10

Chapter 6

Testing the circuits

Before ordering and soldering the PCBs, first the different circuits have to be tested to make sure that they work as designed. To do this, the total circuit is divided into different blocks. One block for digital signals, one block for analog and digital signals, one block for the power supplies and one block for the current measurements. In addition the switching of the relays has to be tested.

6-1 Digital signals

The digital signals block can be found in Figure 4-3. This block is mainly used for generating bias signals at voltage levels $3.3V$, $5V$, $10V$, $12V$ and $24V$. This is the main part to be tested.

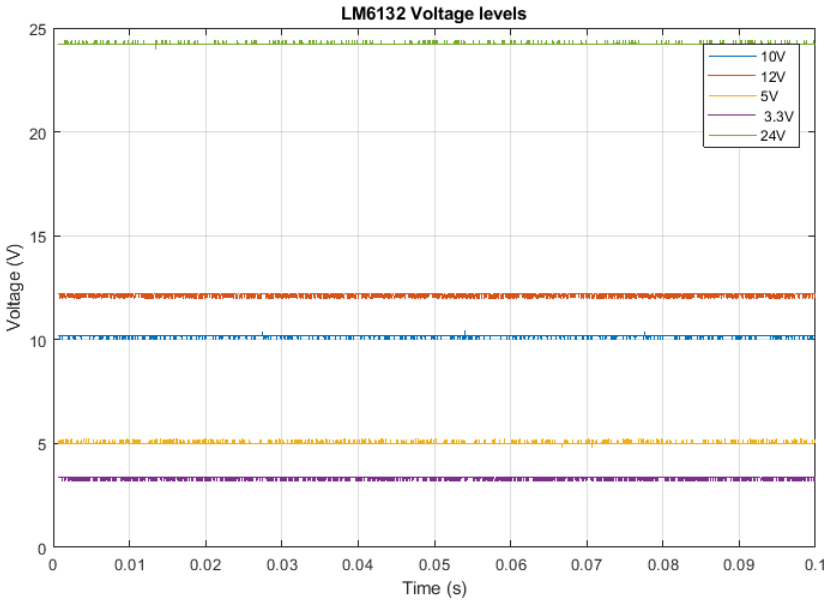


Figure 6-1: Bias levels at 3.3V, 5V, 10V, 12V and 24V

As can be seen in Figure 6-1, the signals are brought to the correct voltage level. There is about $0.2V$ to $0.4V$ of deviation from the ideal voltage. The exact minimum and maximum deviation can be found in Table 6-1. This is, although not ideal, within the specifications, which states that the signal has to be exact within tenths of volts. If a more precise bias voltage is needed, it is always possible to connect it externally.

Table 6-1: Deviation from ideal bias voltages

Voltage	Minimum	Maximum
$3.3V$	$3.2V$	$3.4V$
$5V$	$4.8V$	$5.2V$
$10V$	$10V$	$10.4V$
$12V$	$12V$	$12.2V$
$24V$	$24V$	$24.4V$

To test if the power supplies are capable of driving a load, a load is connected. The results of this measurement are found in Table 6-2.

Table 6-2: Load behaviour of the power supplies

$R(\Omega)$	**100**	**150**	**1k**	**100k**
$I_{3.3V}(mA)$	32.03	21.59	3.36	0.03
$V_{3.3V}(V)$	3.166	3.218	3.3	3.32
$I_{5V}(mA)$	47.25	31.9	5	0.05
$V_{5V}(V)$	4.66	4.75	4.9	4.945
$I_{10V}(mA)$	97.6	64.71	10.12	0.1
$V_{10V}(V)$	9.47	9.65	9.93	9.98
$I_{12V}(V)$	119.6	78.5	12.28	0.12
$V_{12V}(V)$	11.48	11.71	12.04	12.1
$I_{24V}(V)$	15.4	150	24.62	0.24
$V_{24V}(V)$	40	23.27	23.99	24.12

As can be seen, higher voltages can not drive lower loads. The voltage drops. However, from about 150Ω, all voltages and currents are within spec. The larger the load, the better the voltage. To achieve an even better performance at lower loads, a fan could be used to cool the LM317HV regulators. More power can then be outputted. An other option could be to add a larger heatsink to the regulators. This will make the components dissipate more heat, and will therefore achieve higher output power. One consideration to take into account when using the system, is that when connecting multiple loads at different pins, these will be seen as loads in parallel. This means that a lower load will be seen, which could result in a lower output voltage.

The second feature of this block is to amplify digitally generated square waves. While testing this, a flaw is found. Because the opamp is saturated, it cannot switch fast enough, so the output is not a square wave for frequencies higher than $10Hz$. The slew rate of the LM6132 is $12V/\mu s$ [11]. This means that for a voltage swing of $5V$, it should be able to do this $\frac{12V/\mu s}{5} = 2.4 \cdot 10^6$ times per second. This value turns out to be much lower when the saturation effect of the opamp is used. A way of compensating for this, is to first use a voltage divider, so the swing of the opamp does not have to be as large. This however, brings more noise to the circuit. To be able to amplify high frequencies of up to $100kHz$, this means that a voltage divider of about 10000:1 has to be implemented. The amplification of these square waves is tested with a 100:1 voltage divider to show that this approach would work. The results for a $100Hz$ and a $1kHz$ square wave are shown in Figure 6-2.

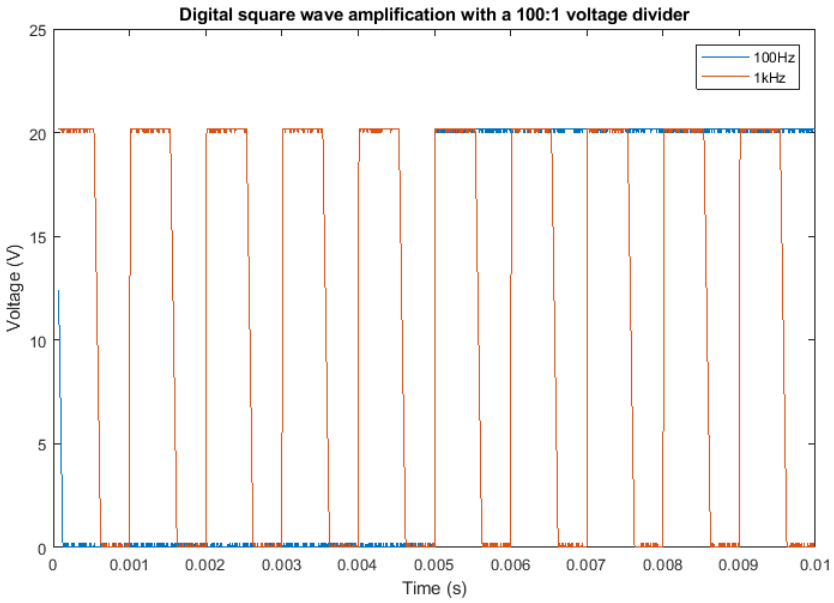


Figure 6-2: Square wave of $100Hz$ and $1kHz$ with a 100:1 voltage division

This is not implemented in the end, because it is not possible to implement these square waves in the DAQ. These can only be generated at the analog ports.

Therefore, the circuit could have been simpler. Because the only digital signals will be DC signals, it is possible to just switch between power supplies and use that signal, instead of letting the opamp saturate. This approach is taken in the end, because it is a more precise and more reliable option.

6-2 Analog and digital signals

The analog and digital signals block can be found in Figure 4-2 and Figure 4-3. Because the digital part of this block is the same as the one already tested in Section 6-1, only the analog part has to be verified. All voltages between $-10V$ and $10V$ have to be made. The analog part is responsible for giving more power to the generated DAQ signal and to separate the DAQ from the sensor itself. It is implemented by a voltage follower. To test this part of the system, a couple of different signals and amplitude combinations are tested. Square waves, ramp waves and sinus waves of $1kHz$, $50kHz$ and $100kHz$ and DC levels of $10V$, $5V$, $3.3V$ and $1V$. The maximum frequency that the system should achieve is $100kHz$.

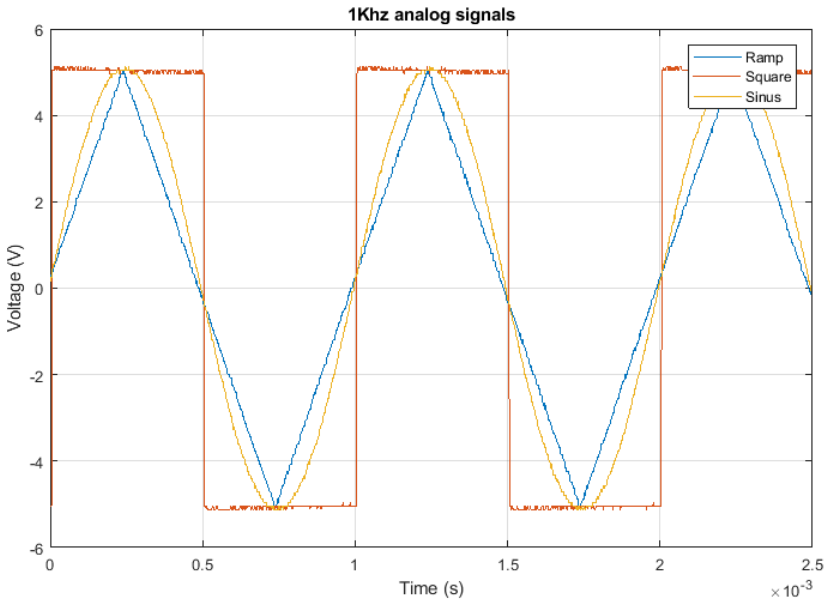


Figure 6-3: $1kHz$ analog signals

When observing the results in Figure 6-3, it can be seen that the signals have low noise. There is however a overshoot at first at the square waves, which will gradually level out to the applied voltage. This effect can be seen as the declining line at the square waves.

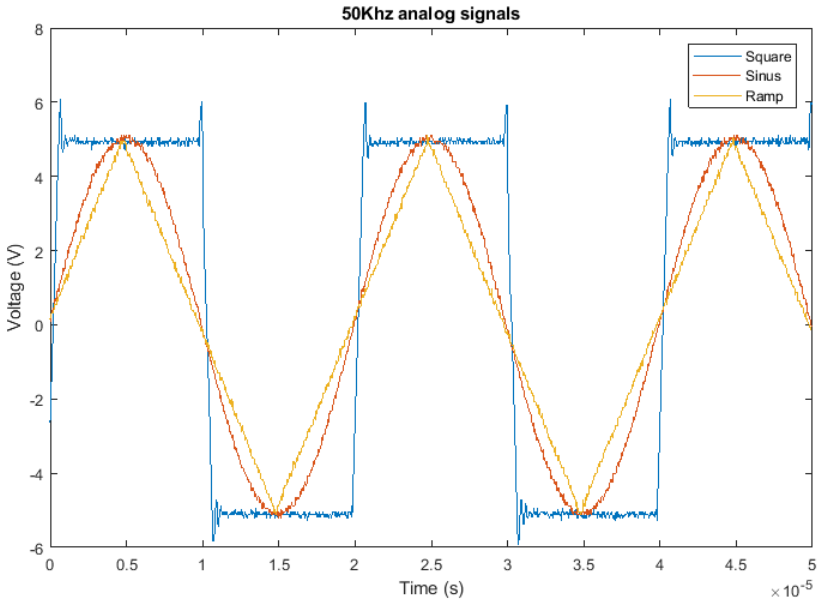


Figure 6-4: $50kHz$ analog signals

When observing the results in Figure 6-4, it can be seen that the signals have more noise than for $1kHz$ signals. For the square waves, there is an overshoot of about $1V$ at the tipping

points.

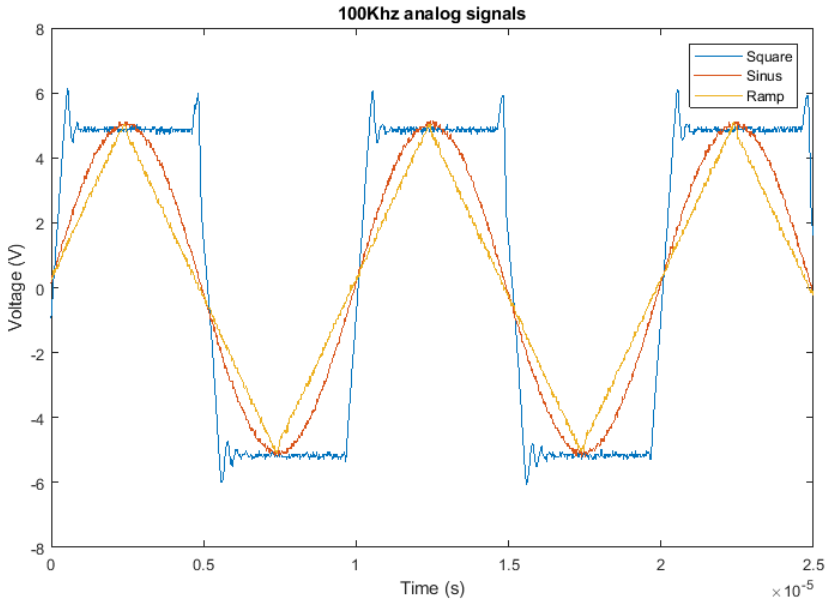


Figure 6-5: $100kHz$ analog signals

When observing the results in Figure 6-5, it can be seen that the signals have more noise than for $1kHz$ signals as well. For the square waves, there is an overshoot of about $1V$ at the tipping points. These also keep resonating more than at $50kHz$.

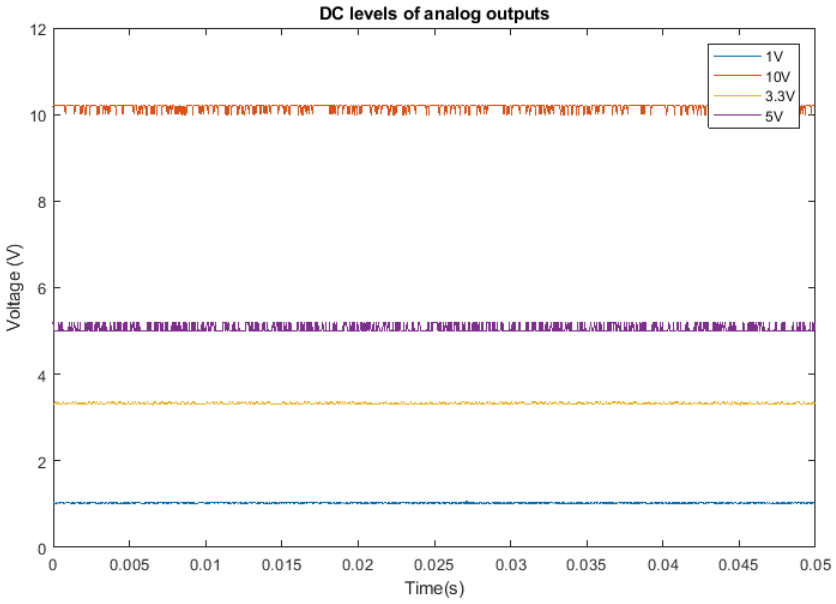


Figure 6-6: Various DC levels of analog signals

When observing the results for the DC signals in Figure 6-6, it can be seen that the circuit does what it should do. However, the lower the voltage level, the more noise is introduced. The deviations of this signal can be found in Table 6-3. The maximum deviation is 4.7% for a $3.3V$ signal, and only 0.9% for a $24V$ signal.

Table 6-3: Deviations from mean DC signal

Mean (V)	**Min (V)**	**Max (V)**	**Deviation (%)**
3.35	3.2	3.4	4.7
5.03	4.8	5.2	4.8
10.18	10	10.4	2.2
12.13	12	12.2	1.1
24.21	24	24.4	0.9

When observing all of the above results, it can be concluded that square waves have an overshoot at the tipping point. The lower the frequency, the less overshoot can be seen. One way to avoid this overshoot is to place a resistor in series with the output. However, this method is costly in terms of performance. The amplitude of the signal will change. One could also put a capacitor in parallel with the feedback network. However, the analog circuit design does not use a feedback network, because the gain is unity. The opamp itself is unity gain stable [7], so there is no need to stabilize it. A third method is to use a Snubber circuit. The idea is to put a series resistor and capacitor in parallel with the output of the opamp. The values of this resistor can be found by trial and error. The value of the capacitor can then be calculated with Equation 6-1 [10]. While testing, it is found that the square wave starts to overshoot at around $19kHz$.

$$C = \frac{3}{2\pi f R} \tag{6-1}$$

Multiple values for R and C were tested. These can be found in Table 6-4.

Table 6-4: Values for R and C for the snubber network

$R(\Omega)$	$C(nF)$
56	100
56	470
220	50
220	100

The results can be found in Figure 6-7. As can be seen, 220Ω does not produce a smooth output signal. The signal is damped too much, because of the high resistance. When moving down to 56Ω, the desired shape can be seen. The slope however, is much less steep than the original signal. The signal does have the right amplitude, so the value for R is not changed anymore. Changing the value of the capacitor does not change the plot by much. In addition, the overshoot is smaller, but not by much. The compromises in signal quality are not worth it. In the end, no measures were taken. As can be seen in Figure 6-7, the system does work with $100kHz$ signals, although it is not ideal for square waves.

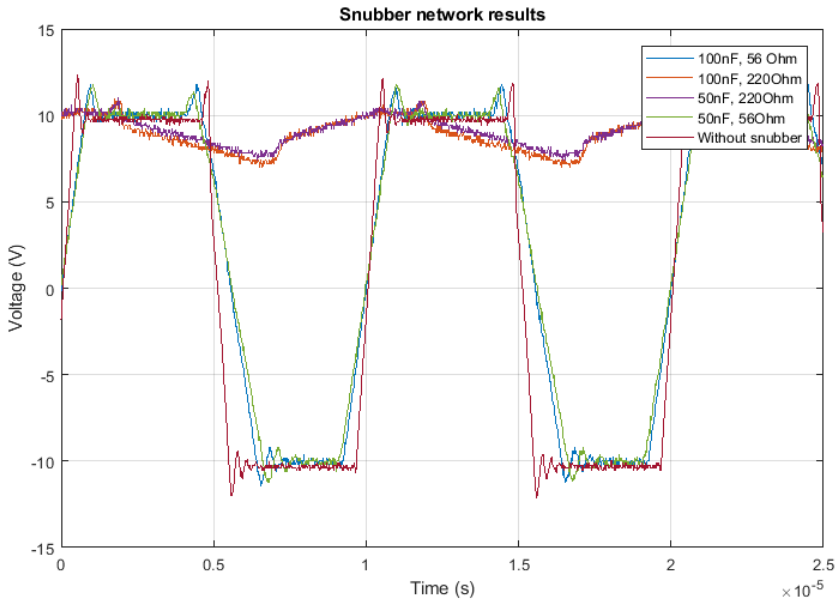


Figure 6-7: Results of a snubber network

6-3 Power supplies

The power supply block can be found in Figure 4-5. The precise calculated values for $R1$ and $R2$ are not available at the Tellegen Hall. To be able to have the correct output voltages, multiple resistors have to be used in series. The power supplies then have to be tested, to ensure the correct voltages. The results, including the minimum and maximum voltages, can be found in Table 6-5.

Table 6-5: Deviation from ideal voltages

Average	Minimum	Maximum
$3.3699V$	$3.32V$	$3.44V$
$5.0052V$	$4.9440V$	$5.0640V$
$10.1322V$	$10V$	$10.2V$
$12.2098V$	$12V$	$12.4V$
$24.3509V$	$24.2V$	$24.4V$

As can be seen in Table 6-5, the average value of the voltage is higher than the required voltage. This is done intentionally, because the opamps used for amplification have a certain voltage drop. However, in the end these opamps are not used anymore, so the resistor values could have changed as well.

The final values for the resistors can be found in Table 6-6.

Table 6-6: Final used values for the power supplies

Voltage (V)	**R1 (Ω)**	**R2 (Ω)**
3.3	99.9	164.5
10	119.7	833
12	120	1037
24	99.7	1818

6-4 Current measurement

The current measurement is the only part that can not be tested before completing the PCB. The INA169 current shunt monitor is supplied in a SMD package, which makes it impossible to connect to the oscilloscope. However, because the circuit from the datasheet [19] is used, the circuit is very likely to work.

Chapter 7

PCB design

There are three PCBs, namely the DAQ PCB, the socket PCB and the external PCB. This setup is chosen to make sure that the size requirements are met. This way all of the switching can be done on a large PCB, which will have no size constraints. The external PCB is needed to have an external smaller test setup at $2m$ from the original setup.

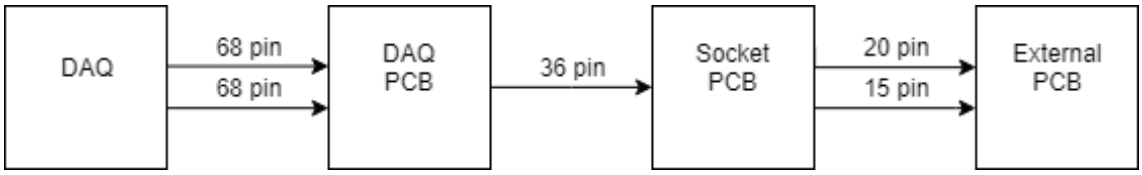


Figure 7-1: Interconnection of PCBs

Figure 7-1 shows the connections between the DAQ and between the PCBs. Between the DAQ and the DAQ PCB two cables are used. These are proprietary for the used DAQ. Both of these cables come with connectors of 68 pins. Between the DAQ PCB and the socket PCB, a cable is used that comes with 36 pins connectors. Between the socket PCB and the external PCB, two cables of $2m$ are connected. One cable consists of 20 coax cables, to transport the coaxial signals with as little noise as possible. The other cable has 15 pins connectors, and is custom made. This cable transports the digital signals and the VDD, VSS and grounds.

7-1 General design rules

When designing a PCB, there are several design rules to keep into account. The rules from the IPC-2221A standard [5] are used. This is a widely used standard for the design of PCBs.

7-1-1 Track widths

To ensure that enough current can flow through the traces on the PCB, the tracks should have a certain width. These widths can be calculated by first calculating the area of the track with Equation 7-1. Then the widths can be calculated by Equation 7-2.

$$Area[mils^2] = \frac{Current[ampere]}{(k * (TempRise[^\circ C])^{0.44})}^{\frac{1}{0.725}} \tag{7-1}$$

$$Widths[mils] = \frac{Area[mils^2]}{Thickness[oz] * 1/378[mils/oz]} \tag{7-2}$$

For internal layers: k=0.024. For external layers: k=0.048. The temperature rise is the maximum allowed temperature rise of the trace. This temperature is set at 10°C, to make sure that the board does not heat up too much. The thickness of the traces is $0.036mm$. One mil is $0.0254mm$. One oz is equal to 29573 mm^3. For $0.1A$ traces (the maximum the board is rated for), the width has to be $0.0714mm$ for external layers, and $0.0274mm$ for internal layers. For $1A$ traces (used by the $200V$ signals), the widths should be $0.657mm$.

7-1-2 Spacing between tracks

To make sure that there is as little interference from the different signals, there should be enough spacing between the tracks on the PCB. For $16 - 30V$, Table 6.1 of the IPC-221A standard [5] states a minimum spacing of $0.1mm$, as can be seen in Appendix A-4. For the 200V power signals, a spacing of $0.2mm$ should be present. All PCBs use a spacing of $0.2mm$ to make sure that there is as little interference as possible.

7-1-3 Capacitance

To be able to route all of the components on the PCB, multiple layers are used. When using multiple layer PCB designs, there is the possibility to have planes and signal layers. Routing can happen through signal layers, while planes are used for DC power and ground planes. The layout of these planes and signals has to be thought of carefully. When using DC power planes, the signal layers should be symmetrical about the ground or voltage plane [5].

7-1-4 Shielding

To have as little noise as possible on the signal lines, the signals have to be shielded as much as possible. To achieve this, critical signal traces have to be buried between power and ground planes [4]. If this is not possible, the alternative is to bury these traces between ground traces as much as possible.

7-2 DAQ PCB

The DAQ PCB is the main PCB for this system. It houses:

- The power supplies
- The relays
- The $\pm 30V$ connections
- Fuses for the $\pm 30V$ connections
- The amplifiers for the digital and analog signals
- The OR gates and multiplexers
- The current measurement amplifiers

The DAQ is directly connected to this, using two 68-pin connectors. It also features a connector that connects directly to the socket PCB. As a final feature, it houses two fuses for the $\pm 30V$ connections. This PCB consists of 6 layers, of which three are power planes. There

is a VDD plane, a VSS plane and a ground plane. These planes have a suboptimal layout, because there is a VSS plane, which means that the signals cannot be symmetrical about the ground and voltage planes. However, without this VSS plane, the routing of the board would be impossible, which would result in even more layers. The final layer layout can be found in Table 7-1.

Table 7-1: PCB layer layout

Name	Type	Thickness
Component side	Signal layer	$0.036mm$
VSS	Plane	$0.036mm$
GND	Plane	$0.036mm$
Inner layer	Signal layer	$0.036mm$
VDD	Plane	$0.036mm$
Solder side	Signal layer	$0.036mm$

The traces all have a width of $0.254mm$ and the $\pm 30V$ input connections have a trace width of $0.5mm$. These traces go to the fuses, after which they go in to the power planes. These are wide enough as calculated in Section 7-1-1. The power traces in this PCB are decoupled by using a VDD, a ground and a VSS plane.

7-3 Socket PCB

The socket PCB is the input for all coax connections. It consists of 9 external bypass connections, 13 normal external connections and two $\pm 200V$ connections. These bypass connections are there to be able to connect more external signals. Bypassing these signals is also necessary, since this is stated in the requirements in Chapter 2. This PCB also houses the mount for the chip to be tested. In addition, fuses for the $\pm 200V$ connections are implemented, with a rating of $1.25A$. The maximum current of these pins should not exceed $1A$, which makes these fuses sufficient. Therefore in the case of a short circuit the components on the PCB will not be damaged. This board also houses the connections to the external PCB.

This PCB uses two layers to keep it affordable. This however means that not all signals are shielded as well as they could have been. To compensate for this, an effort is made to shield the external coax signals between two ground traces. Because of the limited space on the PCB, this is not possible everywhere. All traces on the PCBs have a width of $0.254mm$, which is within the required specifications as stated in Section 7-1-1. But there is an exception, namely the $200V$ connections, which have a trace width of $1mm$. This PCB uses two decoupling capacitors to decouple the power traces.

The pin layout of the system can be found in Figure 7-2. This pinout is made in consultation with the supervisor and with external members from the EKL, during a consultation session. In this figure the I/O pins are externally connected. The D pins are the digital pins that can be generated internally and the A/D pins are the analog/digital pins that can be generated internally. There are also 6 VDD pins and 6 VSS pins, to be able to meet the requirement of 6 power supply connections.

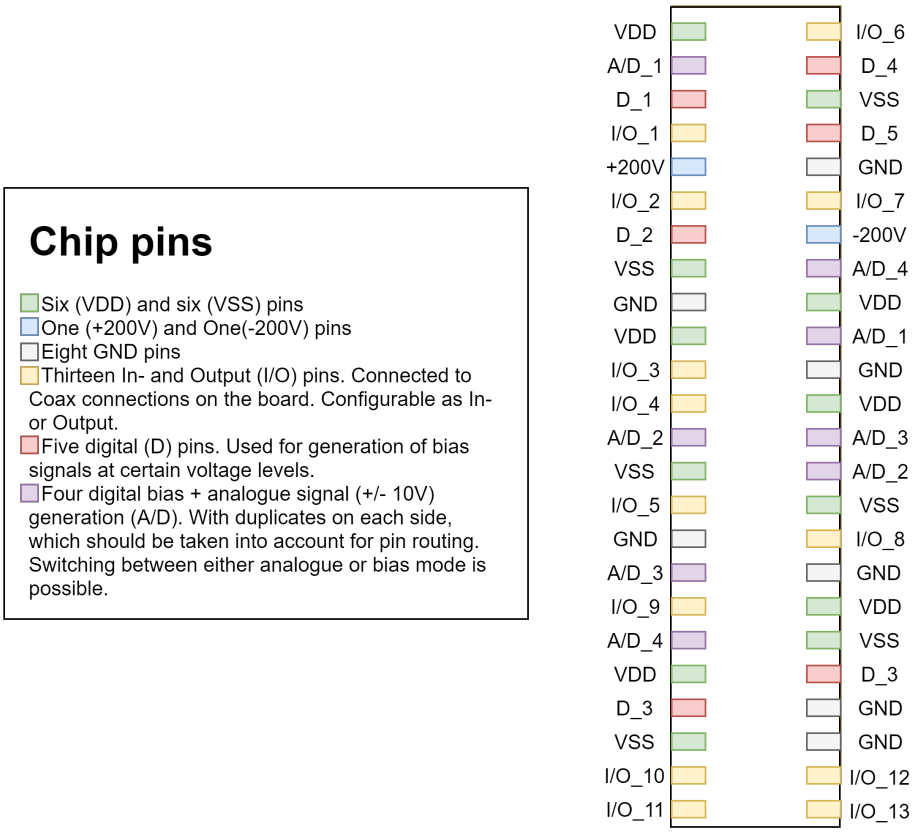


Figure 7-2: Pinout for the socket on the PCB

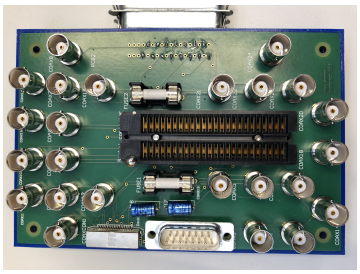
This PCB can be found in Figure 7-3a. The dimensions of this PCB are $100mm$ by $150mm$ and it is mounted into a simple holder with a height of $23mm$.

7-4 External PCB

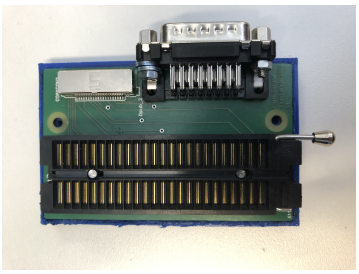
This PCB uses two layers as well. This is the smallest PCB of the three. Its only purpose is to have a smaller test board, for smaller measurement setups. This board has the same socket as the socket PCB and the same pinout as Figure 7-2. This board lacks the possibility to connect $200V$ power connections. These two connections are connected to the ground. All traces on this board have a width of $0.254mm$. This is enough according to Section 7-1-1. This PCB can be found in Figure 7-3b. The PCB has a format of $50mm$ by $81mm$ and is mounted into a simple holder with a height of $8mm$.

7-5 Interconnects

For the external PCB, a cable has to be found that is shielded. This is to make sure that there is little interference. In the end, the choice is made to use two cables, one coaxial assembly and one d-sub assembly. The coaxial assembly is used for all of the I/O signals. These signals



(a) The finished socket PCB



(b) The finished external PCB

Figure 7-3: Two completed PCBs

are generated outside the system and come in at the coaxial connections. These signals have to have as little distortion as possible. The analog signals go through coaxial cables as well. The digital signals are generated at the DAQ, and will just be bias voltages. These signals already went through a cable and through a complete PCB, so there is no need to shield these as well. In addition, the used coaxial cable assembly [21], is not made for DC voltages.

Chapter 8

Prototype Results

First all the components have to be soldered into the system. The DIP packages are not inserted into the sockets yet. Then the system has to be tested. After first making sure that there are no shorts, the power supply part can be tested. The correct pins on the PCB can then be probed to check if the correct voltages are present at the correct pins. After this, the system can be connected to the DAQ. At first, no power supply is connected. This is to make sure that the DAQ will not break down if an error is made. Signals are then generated at the DAQ, after which the pins on the PCB can be probed to see if the correct waveform or voltage is present. If all is well, the components can be inserted and the total system can be tested. In this chapter, the testing of all of the separate parts will be discussed.

8-1 Analog outputs

First the analog outputs are tested. A sine wave is generated at the DAQ, which can then be measured at the socket. However, when measuring the pins on the socket, it became clear that there was no output signal present. After evaluating all of the parts of the PCB, it became clear that the relays were to blame. This will be discussed in Section 8-6. To be able to still test the circuit, the pin directly on the opamp was probed. However, while testing this part of the circuit, it became clear that there was a certain amount of negative clipping. The sine wave would be perfect, until it reached about $-2V$, after which it would clip. After this, all of the circuit was verified again on a test board. The relay was also included, to make sure that that was not what caused the issue. The test circuit however, was working as expected. Eventually the issue was found. It had to do with the current measuring of the signal. This will be discussed in detail in Section 8-3.

After solving the issue, three measurements are taken. A sine and a square wave at $1kHz$, at $50kHz$ and at $100kHz$.

Figure 8-1 shows the result for the $1kHz$ signal. The expected sine and square wave are found. However, the voltage is higher than is set in the GUI. This is a result of overshoot of the opamp.

Figure 8-2 shows the results for the $50kHZ$ signal. The signal has more distortion than the $1kHz$ signal. This is because of the limited sampling frequency of the used DAQ. This can also be seen in Figure 8-3. The higher the frequency, the more distortion. A signal of $100kHz$ is therefore not recommended, although possible. As more channels of the DAQ are one, the maximum sample rate will go down, so the maximum frequency will go down as well.

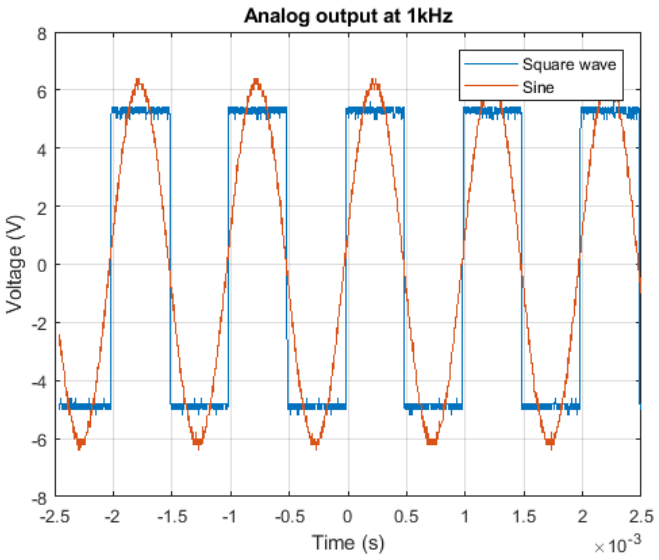


Figure 8-1: Analog outputs at 1kHz

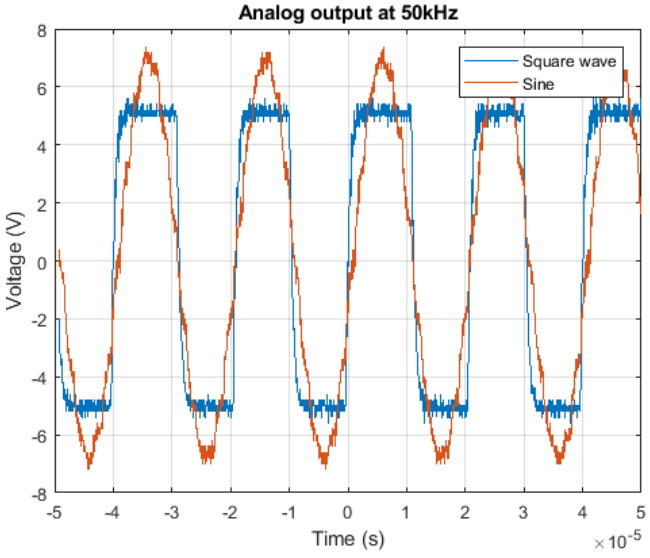


Figure 8-2: Analog outputs at 50kHz

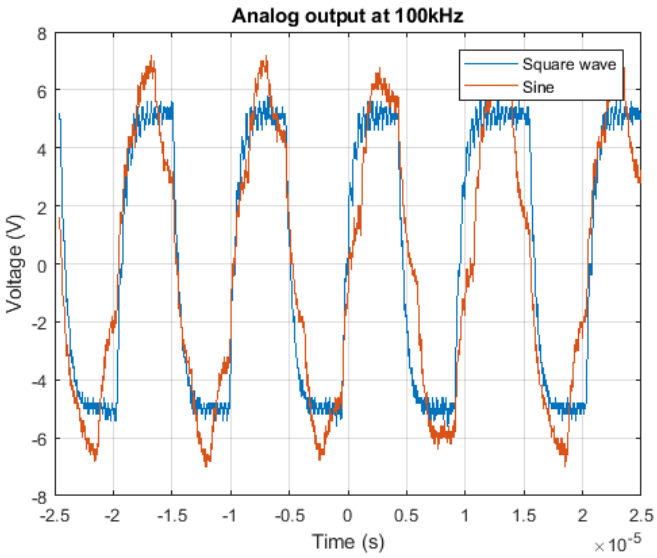


Figure 8-3: Analog outputs at 100kHz

8-2 Digital outputs

To measure the digital outputs, a $12V$ DC signal is put on one of the channels. Two places are then measured: on the output of the opamp, and on the socket. This way any distortion or abnormalities in the cable and PCB traces can be detected. The results of this measurement can be found in Figure 8-4.

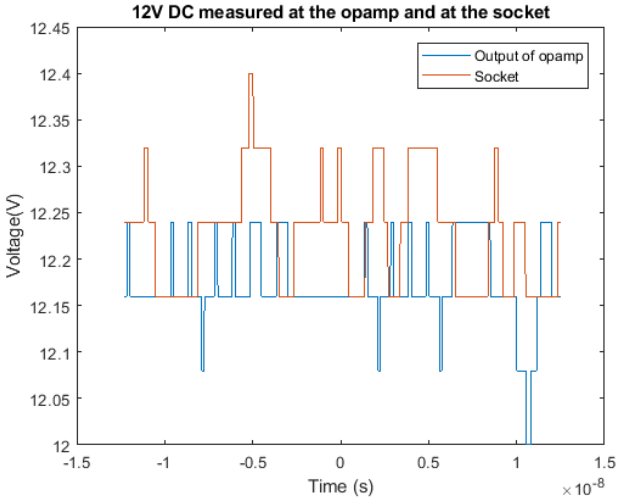


Figure 8-4: 12V DC measured at the socket and at the opamp

When evaluating this figure, it can be seen that the signals are not completely equal, but still have roughly the same properties. The mean of the opamp voltage is $12.17V$, and the mean of the socket voltage is $12.22V$. This is such a small deviation, that this can be partly contributed to the used oscilloscope. The signal on the socket has a maximum value of $12.4V$

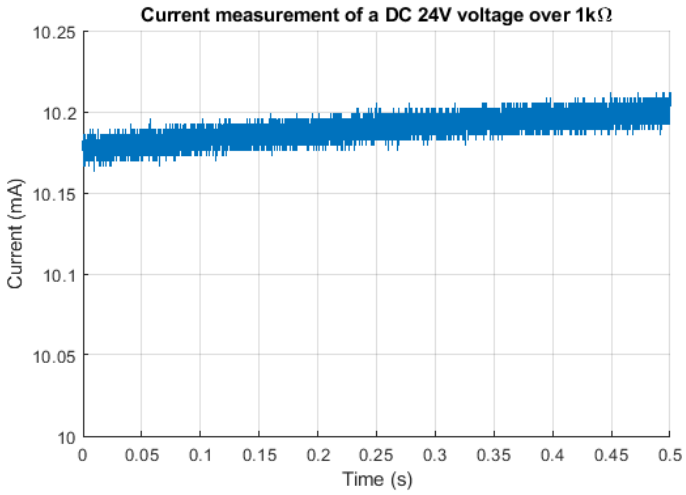


Figure 8-5: Measuring of the current of a 24V DC signal through a $1k\Omega$ resistor

and a minimum value of $12.16V$. This means a deviation from the mean value of $0.18V$ and $-0.06V$. This is within the requirements of Chapter 2, that state that the outputs have to be precise up to tenths of volts.

The other signals have also been tested. The output voltages of these signals can be found in Table 8-1. These voltages are all measured without a load.

Table 8-1: Output voltages for DC signals

Required Voltage (V)	Output voltage (V)
3.3	3.31
5	4.94
10	10.1
12	12.2
24	24.4

8-3 Current measurement

As stated in Section 8-1, the current measuring circuit for the analog system influenced the analog output waveforms. After closely inspecting the datasheet of the current shunt monitor [19], it is found that it can not measure negative currents. The solution is to remove these components from the PCB for the analog parts. The possibility to measure the current of analog waveforms is thereby removed. Searching for another component with the possibility to measure negative currents as well did not bring up any results (the power supply voltage that is connected through the PCB is too high for most of these small components).

The current of the digital signals can be measured. To test this, a DC voltage of $24V$ is selected in the GUI. A $10k\Omega$ resistor is connected at the output. The results of this measurement can be found in Figure 8-5.

Using Ohm's law, $U = IR$, the expected current can be calculated. This current should be

$I = \frac{U}{R} = 24mA$. When looking at Figure 8-5, it can be concluded that the current is lower than expected. To check if this is a measurement flaw, or a design flaw, other voltages are measured as well. Figure 8-6 shows the same measurement for a $3.3V$ bias voltage.

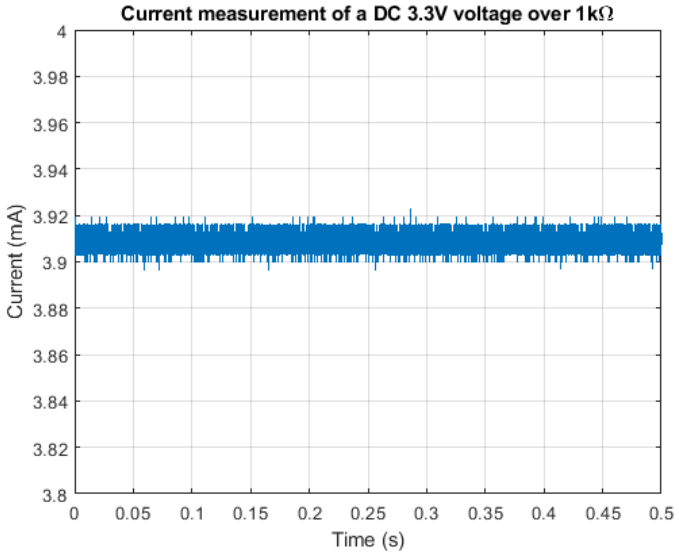


Figure 8-6: Measuring of the current of a 3.3V DC signal through a $1k\Omega$ resistor

The expected current of this signal is $I = \frac{U}{R} = 3.3mA$. However, when checking Figure 8-6, the current shows a value of around $3.9mA$. To check this, a multimeter was used as well to measure this current. This showed a value of $3mA$. After extensive research, the reason is found to be the voltage drop over the 1Ω resistor. This voltage drop, with a load of $1k\Omega$, can be calculated by using a voltage divider equation. This voltage divider can be found in Figure 8-7.

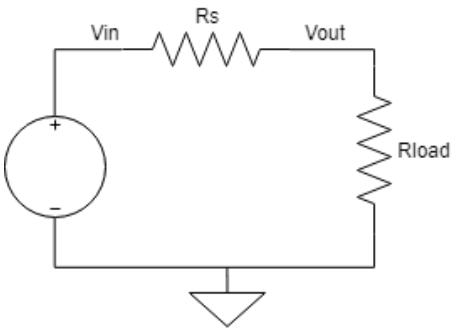


Figure 8-7: Voltage divider for current measurement

The output voltage at a certain input voltage can then be found using Equation 8-1.

$$Vout = \frac{Rload \cdot Vin}{Rload + Rs} \tag{8-1}$$

When filling in a value of $3.3V$ for the input voltage, a output voltage is $3.2967V$. The voltage drop is then $3.3 - 3.2967 = 3.3mV$. When checking the datasheet of the INA169, a voltage drop of around $50mV$ is recommended. To solve this problem, a higher Rs has to be chosen. However, a higher resistor value will give more losses at higher voltages. For other resistances of the load, this value also has to change. For a $3.3V$ signal and a load of $1k\Omega$, the required resistor, for a voltage drop of $50mV$, has to be 15Ω. However, for a $24V$ signal, this same resistor has to have a value of only 2Ω. The right balance has to be found. A Matlab script is made to plot values for Rs against the load resistance of chips. For a load of $100k\Omega$, a Rs of over $1.5k\Omega$ has to be used for a voltage of $3.3V$. This is not achievable, because the losses at low load resistances will simply be too high. To test the above theory, a Rs value of 180Ω is chosen, which is suitable for load resistances in the range of $10k\Omega$ up to $50k\Omega$. The value for Rl can then be calculated using Equation 4-1. This turns out to be 555Ω. However, when trying out these values, strange behaviour can be observed. The measurements are completely off. Therefore the choise is made to keep the original values for Rs and Rl.

When a new PCB could be ordered, an other solution could be made. The output voltage and input voltage could first be buffered, before going through the current shunt monitor. This way, it would be independent of the load.

It could also be concluded that the reason that the current at a $24V$ signal is lower than expected, is that the used opamp can not output enough current. When desired, this opamp could be exchanged for an opamp with a higher current output. When a higher load is connected however, the system works as expected. However, as stated in Section 6-1, the LM6132 opamp is not necessary in the end, so this problem does not have to be solved in a future version. This problem is solved at this time, by connecting the positive supply terminal of the LM6132 socket directly to the output. This way, the LM6132 opamp is not used anymore. There is still a limitation to the load resistor, to keep a stable voltage. It is stable from around 100Ω. Any lower load will result in a lower output voltage, due to the inability of the power circuit to deliver enough current. An extra bonus is the fact that the digital outputs are now completely disconnected from the DAQ pins, so there is no possibility to damage the DAQ. It would be advisable to implement for example an optocoupler at all channels from the DAQ, to be extra sure the DAQ does not receive voltage spikes.

The new digital output voltages can be found in Table 6-5.

8-4 Output voltage measurement

The voltage output measurement can be tested by using the GUI to select the voltage measurement mode. A power supply can then be connected to the socket, and the voltage can then be checked in the GUI. A $5V$ sine wave is generated by a function generator at $1kHz$, $50kHz$ and at $100kHz$. This sine wave is then connected through a coaxial connector. The results of this measurement can be found in Figure 8-8, Figure 8-9 and Figure 8-10.

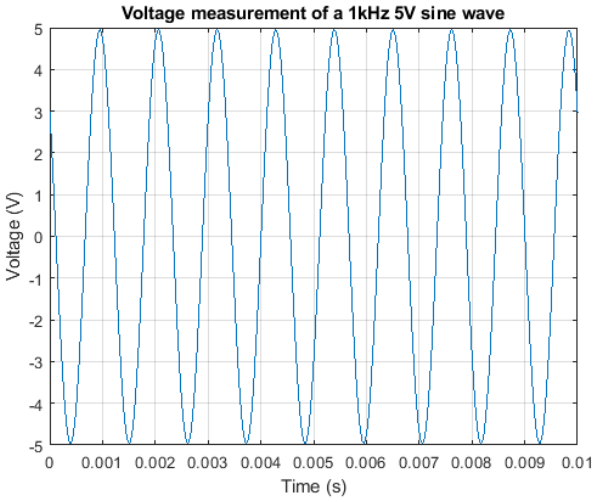


Figure 8-8: Voltage measurement of a $1kHz$, $5V$ sine wave

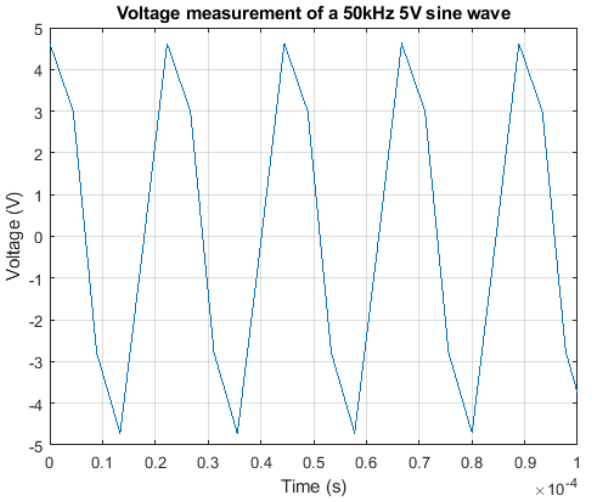


Figure 8-9: Voltage measurement of a $50kHz$, $5V$ sine wave

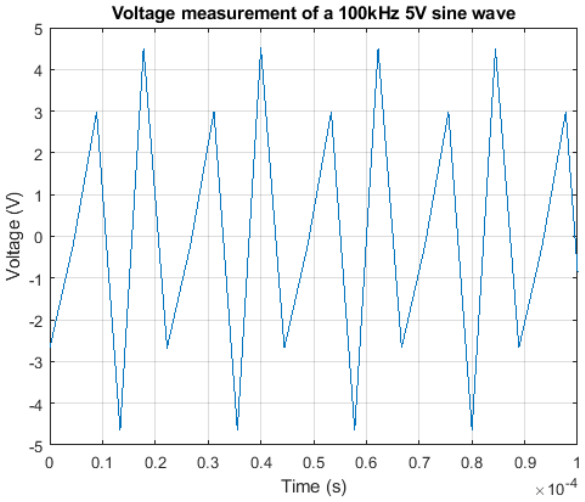


Figure 8-10: Voltage measurement of a $100kHz$, $5V$ sine wave

As can be seen, the voltage is accurate for lower frequencies. However, when the frequency gets higher, the accuracy drops significantly. This is because of the limited sampling frequency of the used DAQ card. The voltage measurement function will be usable up to around $50kHz$.

8-5 Power supply

Because the same resistors from Section 6-3 are used to create the voltage with the LM317HV regulator, the results are the same. This means that the voltages have the same values as in Table 6-5.

8-6 Switching

As stated in Section 8-1, the relays did not do the job. They were not triggered. After extensive testing, it became clear that the problem was the OR gates. They could not deliver enough current to trigger the relays. Testing the relays showed a minimum current necessary of about $3mA$. The OR gates could only deliver $1.5mA$. Therefore the choice is made to switch out the OR gates for others that can deliver the required current. However, they have a different pinout. Therefore an external board is necessary to house them. After switching out the OR gates, the relays work.

8-7 External board

To make sure that the external board does not add any more noise to the signal, it is tested as well. A function generator is connected to the socket PCB as well as to an oscilloscope. At the same time, the output from the external PCB is connected to the oscilloscope. The results in Figure 8-11 can then be compared, where no noticeable differences are found.

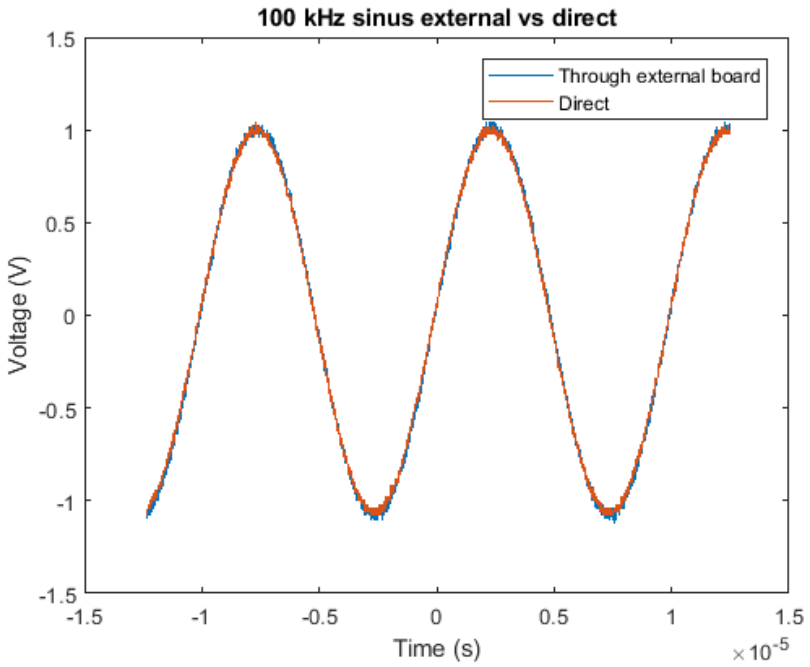


Figure 8-11: Testing of the external board

8-8 Driving a transistor

As stated in the requirements in Chapter 2, the current of the generated signals has to be enough to drive a transistor. To test this requirement, a simple circuit is build. This circuit can be found in Figure 8-12.

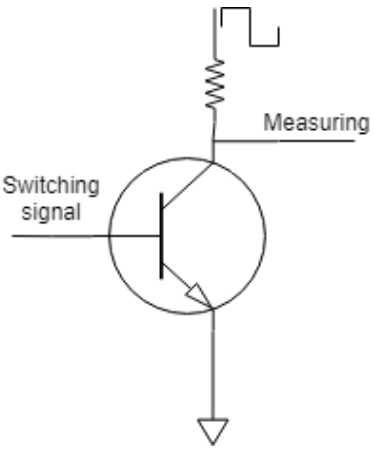


Figure 8-12: Testing circuit for a transistor circuit

A square wave is put onto the collector of the transistor through a resistor. The emitter is connected to the ground. When a voltage is applied at the switching signal terminal, measuring should be zero. When a zero is applied at the switching signal terminal, a square

wave should be measured. By connecting the switching signal pin to a pin on the DAQ, it can be verified if the generated signals can deliver enough current to drive the gate of a transistor. When applying a $5V$ signal through an analog channel, the transistor is closed, and $0V$ is found on the measuring port. This means that the transistor has switched. When a $0V$ signal is applied, the square wave can be found on the output. The same goes for the digital channels. This means this requirement is also verified and met.

8-9 200V testing

To test if the $200V$ connections also work, a HPSMU is used to measure two different resistors. The HPMSU can deliver a current of $1A$ at $20V$ or $50mA$ at $100V$. When using Ohm's law, $U = IR$, the current through a resistor can be calculated at a certain voltage. Two resistors are tested, namely a resistor of 37.5Ω and a resistor of $200k\Omega$. The First resistor is used to generate a high current at $20V$. This current will be $I = \frac{U}{R} = 0.53A$. The test results can be found in Figure 8-13. The resistance can then be calculated by Equation 8-2.

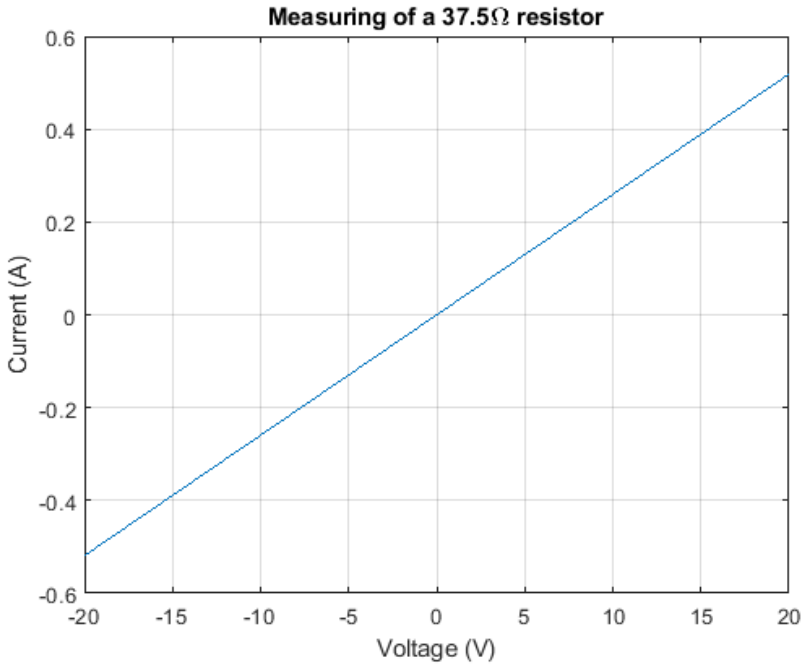


Figure 8-13: Test results for a $20V$ voltage over a 37.5Ω resistor

$$R = \frac{max(V) - min(V)}{max(I) - min(I)} \tag{8-2}$$

When evaluating Figure 8-13, it can be seen that the system measures a resistance of 38.53Ω. This is what is expected, so no clipping occurs, and no shorts are found.

The second resistor is used to generate a low current at a high voltage. The current at this voltage will be $I = \frac{U}{R} = 1mA$. The results of this measurement can be found in Figure 8-14. When evaluating this figure using Equation 8-2, it can be calculated that the system measures

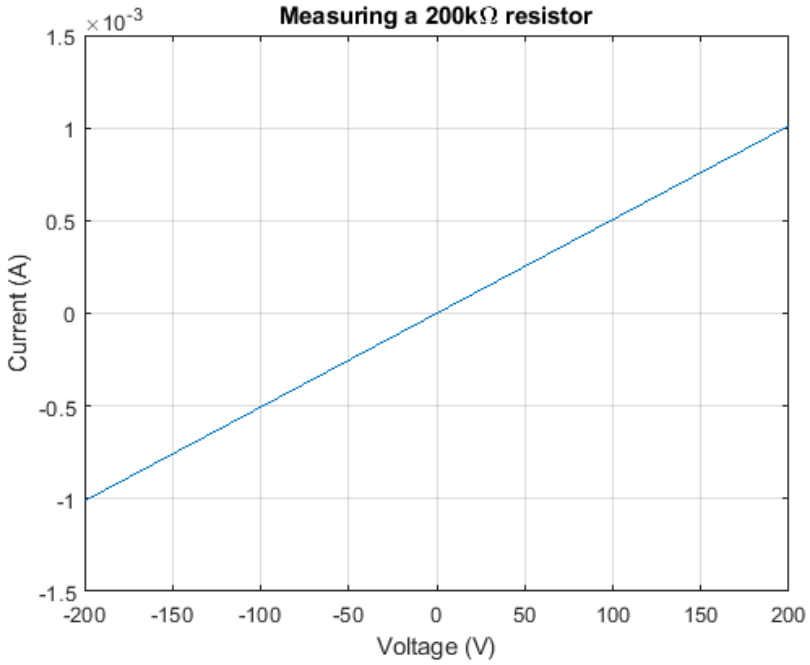


Figure 8-14: Test results for a $200V$ voltage over a $200k\Omega$ resistor

a resistance of $197.6k\Omega$. This is the expected value, therefore no clipping occurs and no shorts are found.

Chapter 9

Discussion of the results

In this chapter, all relevant requirements from Chapter 2 will be verified. Which means that only the requirements that are discussed in this thesis, are discussed in this chapter. The other requirements will be discussed in the theses of the other subgroups.

9-1 Input/output requirements

The first requirement states that the system should allow the connection of three external measurement tools. This requirement is met. All digital and analog/digital pins also have the possibility to connect externally as an input or output. In addition, all the I/O connections can also be connected externally (7-3), which adds up to 22 external connections.

The second requirement states that the system has one 48p DIP socket for the chip under measurement. This requirement is also met (7-3).

9-2 Structural and usage requirements

There are two structural and usage requirements, both are met. The socket PCB has dimensions of $100mm$ by $150mm$, within a case with a height of $23mm$. This is within the required specifications. The housing is already made, so the second requirement is also met.

9-2-1 External analog input/output signals requirements

The first requirement that is discussed here states that all pins are rated at $\pm 100V$ and $100mA$. This requirement is also met. They are rated even higher, because of the used reed relays. These are rated at $250V$ and $0.5A$ as stated in Section 4-7. All connections to the DAQ go through these relays. When there is a direct connection to the DAQ after the relay, an opamp or voltage divider is present as an extra safety measure. The digital connections have no direct connection to the DAQ whatsoever.

The second requirement states that there should be ten analog input connections. This requirement is met, because there are 13 I/O connections. In addition, there are bypasses available for the digital and analog/digital connections. In total, 22 connections can be made externally.

The third requirement states that the externally connected signals have to be sent to the sensor directly, to have as little distortion as possible. This requirement is also met. The

externally connected signals do not travel through any components, and are largely shielded on the PCB as stated in Section 7-3.

The fourth requirement states that the system allows two additional external power connections rated up to $\pm 200V$ and $1A$. This requirement is also met. This can be connected to the socket PCB (7-3). The traces are designed with this $200V$ and $1A$ in mind, and are tested in Section 8-9, so this requirement is also met.

9-3 Internal signal generation requirements

The first two internal signal generation requirements state that up to 9 signals should be generated, of which 4 are basic analog signals. This requirement is met. This can be read in Chapter 4.

The requirement that states that the frequency of the analog signals is rated up to $100kHz$ is partly met. The system works for signals with this frequency, but for square waves there is an overshoot at the output as can be read in Section 6-2. Also, because of limitations of the DAQ, the higher the frequency, the lower the sampling rate, which results in distortion.

The amplitude of the analog signals can be adjusted from $-10V$ to $10V$. This can be read in Section 6-2 as well.

The next requirement for the internal signal generation states that all nine signals can be used to generate bias voltages at $3.3V$, $5V$, $10V$, $12V$ and $24V$. This requirement is also met, as can be read in Section 6-1.

The sixth requirement states that the current of the generated signals has to be measured. This is partly met. Because of the problems with the current shunt monitor in Section 8-3, the current measurement of the analog signals is not possible. There are no components available that fit on the PCB, so a whole new PCB would have to be designed. The current of the digital signals however, can be measured. There is an issue however, with the accuracy at low voltages.

The next requirement states that the current of the generated signals has to be enough to drive the gate of a transistor. This requirement is also met, as can be read in Section 8-8.

The last requirement states that the output voltage has an accuracy of tenths of volts. This requirement is met. In Section 8-2, it can be seen that the outputs are within tenths of volts accurate. The maximum deviation from an ideal signal is $0.4V$ for a $24V$ DC signal. This could be compensated by changing the values of the resistors of the $24V$ power supply.

9-4 Power supply requirements

There are two requirements concerning the power supply. External power of $\pm 30V$ can be connected, and the power supply is connected to 6 pins on the socket. Both requirements are met. As can be read in Section 4-5, the input voltage for the total system has a maximum value of $\pm 30V$. In Section 7-3 it can be seen that there are 6 VDD connections and 6 VSS connections available.

9-5 Pin connections requirements

The first requirement states that all pins interfacing with the chip under measurement are fully reconfigurable. This requirement is not met, because only nine pins are. The reason for this, is that the project would otherwise be too large. Instead of using 55 reed relays, about 2000 would be needed. Also more driving signals would be needed. This is not achievable with the budget that is available, as discussed in Section 4-6, and within the time span of the project. The system would also be way too large. The last reason is that the coaxial signals have to be as precise as possible, which would be impossible when they have to go through the relays.

The second pin connections requirement states that the system also has one 48p connector to connect to an external smaller board. This requirement is also met. There is an external smaller board available. Although the connection between them is not by a 48p connector, there is a 48p connector available on the external PCB (7-4).

The last requirement has to do with the external board. All socket pins can be found on the external board as well, and the external board has to have a cable of at least $2m$. This requirement is met. There is a side note, because the $200V$ connections are not found on the external board. However, the cable between the two PCBs has a length of $2m$.

9-6 Cost requirement

The last requirement states that the costs of all the hardware has to be less than €1000. This requirement is met, as can be seen in Section 5-10

Chapter 10

Conclusions and recommendations

This chapter includes reflection on what works and what could have been implemented better. How certain subsystems could have been implemented better is discussed in the recommendations.

10-1 Conclusions

The developed measurement interface can internally generate simple DC and AC testing signals. It can measure output voltages and can measure the current of the generated DC signals.

This kind of measurement interface is new in the field of chip testing, as stated in the state-of-the-art analysis in Section 1-1. Even though it has limitations regarding the generated test signals, it will reduce the workload of sensor developers.

The interface is not fully reconfigurable, as discussed in Section 4-6, namely the pin layout is not fully reconfigurable. This design choice is made to make it possible to complete the measurement interface during the Bachelor Graduation Project, while following the budget. Therefore it is important to keep the layout in mind when the sensor is developed. The advantage of not needing to develop a specific test setup is a lot greater than the disadvantage of the set pin layout.

The complete system gives a few benefits. The sensor can be mounted directly on the measurement interface or $2m$ from the measurement interface, making it suitable for large as well as small test setups. There is no need to develop a test setup for every developed sensor. When needed $\pm 200V$ signals can be connected, as discussed in Chapter 7. Several different test signals are internally generated, which can reduce the number of needed externally connected measurement devices.

10-2 Recommendations

For future development, it is recommended to use a different current measurement circuit. The currently used current measurement circuit is not suitable for the analog signals, because this causes clipping for the negative voltages of the sine wave, as discussed in Section 8-1. It is also not suitable, because the current measurement for the digital signals is dependent on the load, as discussed in Section 8-3. In a next version of the measurement interface, the INA193 [13] component should be used for the analog circuit, since that makes it possible to measure the current of the analog circuit without clipping. This component can measure

negative as well as positive voltages. However, this component uses a different supply voltage, which means that it will not work at this PCB.

To avoid the dependence on the load, in a next version of the measurement interface, a buffer should be used. This should be done for both analog and digital circuits.

Since the measurement setup is developed while making sure it would be suitable for digitally generated square wave forms, sine waves and bias signals, some components are used to ensure functionality which eventually was not needed. It became clear that generating square wave forms on the digital pins is not a possibility with the DAQ, which can be read in the thesis of the signal generation subgroup. Without needing to process square waves, the digital circuit became simpler.

In a next version of the measurement interface it is recommended to use larger heat sinks. Using larger heat sinks would make it possible to drive smaller loads. This is now not possible since this would increase the amount of power in the LM317HV which has to be dissipated. Since the small heat sinks that are used cannot do this clipping of the signal can happen at low loads, as discussed in Section 6-1.

As an extra precaution, optocouplers could also be integrated in the signal paths from the DAQ. This would completely disconnect the DAQ from the chip, so there could be no voltage spikes that could damage the DAQ.

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Appendix A

Appendix

A-1 Figures

Figures A-1 an A-2 show the systematic overview of the first design idea.

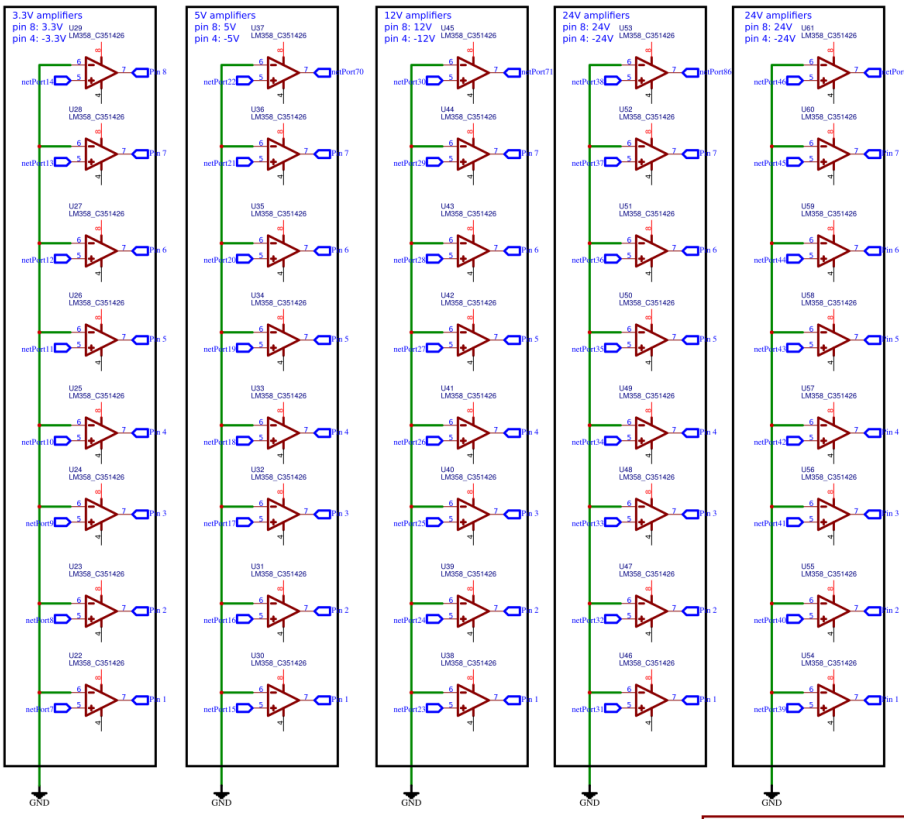

Figure A-1: Opamp circuit of the first design

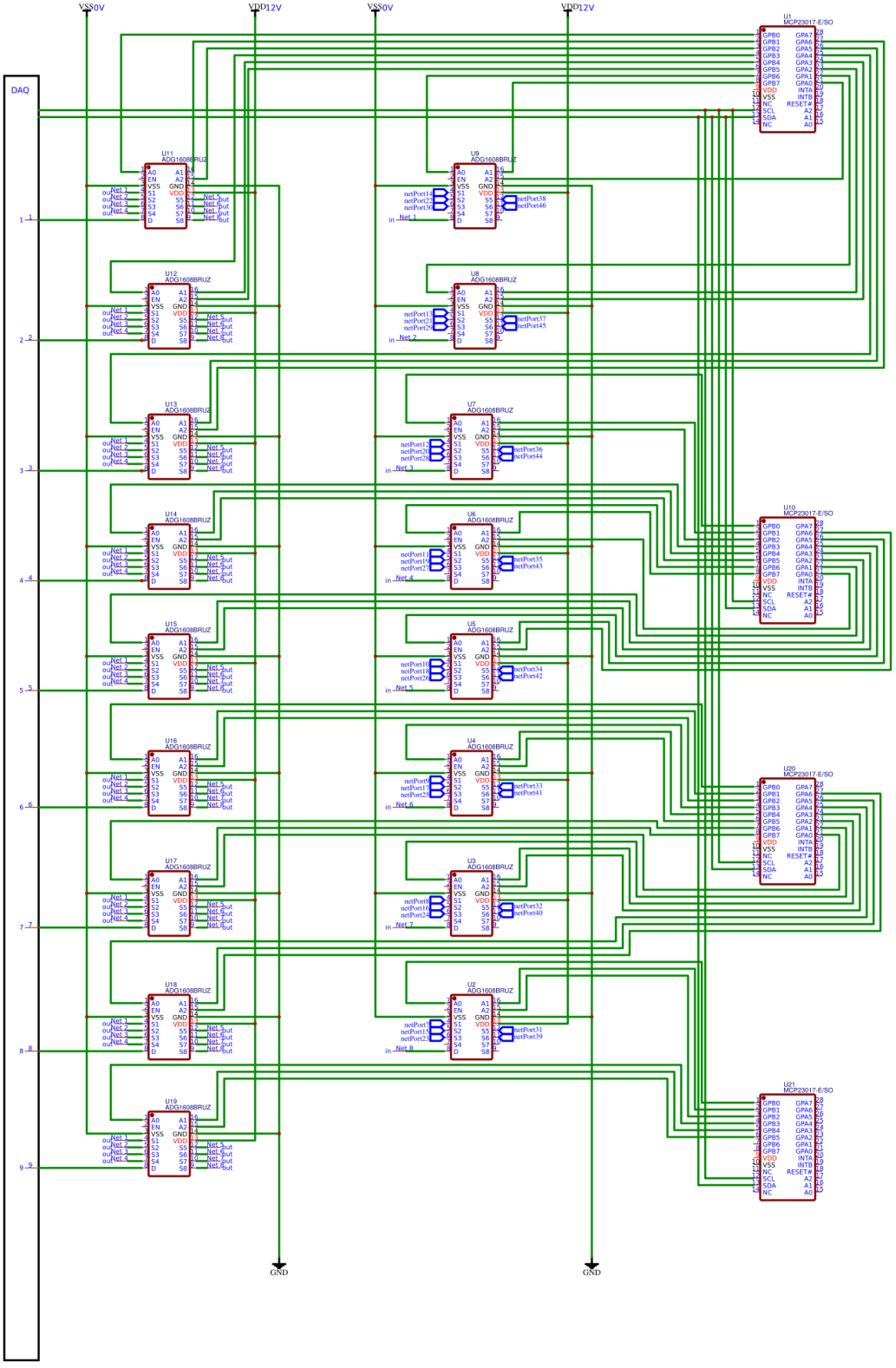

Figure A-2: Multiplexer circuit of the first design

Figure A-3 shows one building block of the final design.

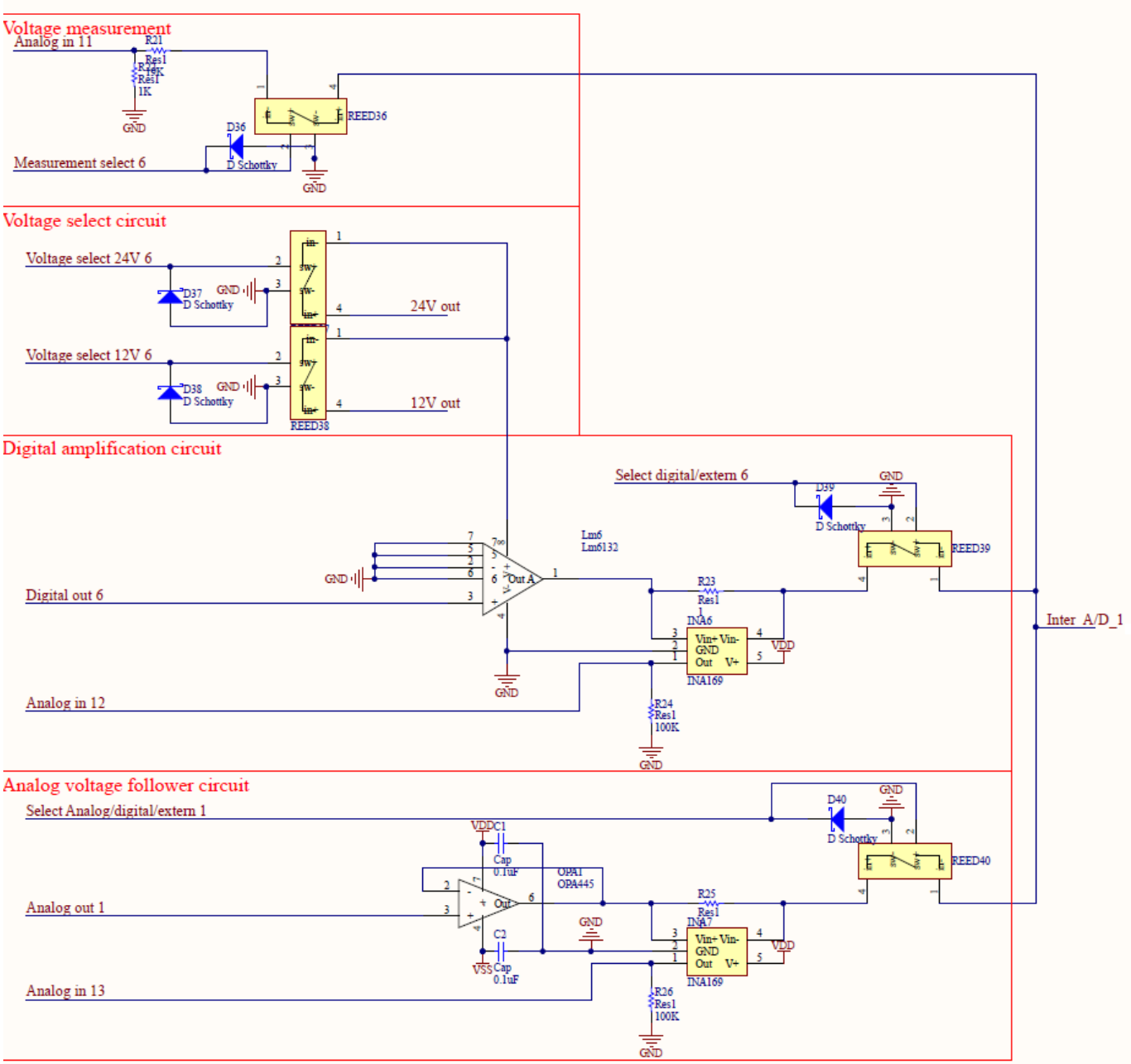

Figure A-3: One building block of the complete system

A-2 Tables

Figure A-4 shows the table from the IPC-2221A standard [5].

Figure A-4: Table 6.1 From the IPC-2221A standard

Table 6-1 Electrical Conductor Spacing

Voltage Between Conductors (DC or AC Peaks)	Minimum Spacing						
	Bare Board				Assembly		
	B1	B2	B3	B4	A5	A6	A7
0-15	0.05 mm [0.00197 in]	0.1 mm [0.0039 in]	0.1 mm [0.0039 in]	0.05 mm [0.00197 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]
16-30	0.05 mm [0.00197 in]	0.1 mm [0.0039 in]	0.1 mm [0.0039 in]	0.05 mm [0.00197 in]	0.13 mm [0.00512 in]	0.25 mm [0.00984 in]	0.13 mm [0.00512 in]
31-50	0.1 mm [0.0039 in]	0.6 mm [0.024 in]	0.6 mm [0.024 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.4 mm [0.016 in]	0.13 mm [0.00512 in]
51-100	0.1 mm [0.0039 in]	0.6 mm [0.024 in]	1.5 mm [0.0591 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.5 mm [0.020 in]	0.13 mm [0.00512 in]
101-150	0.2 mm [0.0079 in]	0.6 mm [0.024 in]	3.2 mm [0.126 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
151-170	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	3.2 mm [0.126 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
171-250	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	6.4 mm [0.252 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
251-300	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	12.5 mm [0.4921 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.8 mm [0.031 in]
301-500	0.25 mm [0.00984 in]	2.5 mm [0.0984 in]	12.5 mm [0.4921 in]	0.8 mm [0.031 in]	0.8 mm [0.031 in]	1.5 mm [0.0591 in]	0.8 mm [0.031 in]
> 500 See para. 6.3 for calc.	0.0025 mm /volt	0.005 mm /volt	0.025 mm /volt	0.00305 mm /volt	0.00305 mm /volt	0.00305 mm /volt	0.00305 mm /volt

B1 - Internal Conductors
B2 - External Conductors, uncoated, sea level to 3050 m [10,007 feet]
B3 - External Conductors, uncoated, over 3050 m [10,007 feet]
B4 - External Conductors, with permanent polymer coating (any elevation)
A5 - External Conductors, with conformal coating over assembly (any elevation)
A6 - External Component lead/termination, uncoated, sea level to 3050 m [10,007 feet]
A7 - External Component lead termination, with conformal coating (any elevation)