19.9 A 2.15W 120V/230Vac to 5-to-12Vdc Offline Power Converter with Full-Duty-Cycle Input-Series Dual-Branch Converter Achieving 1088mW/cm³ and 87.2% Peak Efficiency

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Abstract

This paper presents a 120V/230Vac to 5-to-12Vdc offline power converter consisting of a capacitor-drop AC-DC rectifier and a full-duty-cycle input-series dual-branch DC-DC converter for IoT devices. The proposed converter operates at full-duty-cycle with VCR of D/2 and reduces both the C_{REC} volume and the voltage stress on components, while achieving high efficiency across a broad input and output voltage range. 87.2% peak efficiency, 2.15W output power, and 1088mW/cm³ power density are achieved.

The rapid growth of Internet of Things (IoT) devices and sensors in smart home systems has increased the demand for efficient and compact offline power converters that transfer power from the AC mains to low DC voltages. Traditional offline power converters are typically implemented with isolated flyback [1] or forward [2] topologies, which require bulky transformers to step down the AC voltage (120/230V_{RMS}), limiting the power density to typically less than ~500mW/cm³ [1]. In recent years, non-isolated AC-DC converters [3-15] are gaining popularity due to their compact form factor. Direct AC-DC converters [3-5] use high-voltage (HV) low-dropout regulators (LDOs) [3] or DC-DC converters [4,5] to step down the rectified high voltage (>325V) to a low DC voltage of 3.3-to-12V. These extremely high voltage conversion ratios (VCRs) lead to low efficiency and bulky volume. The capacitor-drop AC-DC converter [6-9] uses an X-capacitor as a buffer to withstand most of the high voltage and reduce the rectifiers' input and output voltages. It offers a higher integration level [6], a reduced VCR for the DC-DC stage [7], and higher system efficiency [8,9]; however, it struggles with limited output power, large filtering capacitor (C_{REC}) volume, and low light-load efficiency.

As shown in Fig. 19.9.1, the theoretical output power P_{REC} of a capacitor-drop AC-DC rectifier is $P_{REC} = 4f_{LINE}V_{REC}C_X(\sqrt{2}V_{LINE}-V_{REC})$. The frequency and voltage of the AC mains (f_{LINE} and V_{LINE}) are fixed, and increasing C_X brings more idle power loss. Thus, increasing P_{REC} requires raising the rectifier's output voltage V_{REC}, as demonstrated by prior arts increasing it from 23V [7] to 60V [8] and 70V [9] to achieve up to 1.52W of output power P_{OUT}. However, this necessitates a higher VCR in the subsequent DC-DC stage. In [8] and [9], switched-capacitor (SC) converters with 1/10× and 1/14× VCRs are utilized. The SC converters can only achieve high efficiency within a narrow voltage range near their ideal VCRs. As such, a large-volume filtering capacitor C_{REC} (aluminum electrolytic, 47μF@63V/80V) is required to suppress the ripple voltage of V_{REC}, severely limiting power density. Furthermore, the complex SC structures required for high VCRs result in higher output resistance and switching loss, limiting the maximum output power and light-load efficiency. Consequently, the P_{OUT} in [8] and [9] reached only 33% and 48% of the 3.18W theoretical P_{REC}, respectively. In summary, SC stages with high VCRs have the drawbacks of a narrow voltage range and a large output resistance, which constrains their output power, voltage range, power density, and peak efficiency.

To resolve these issues, we propose an architecture, shown in Fig. 19.9.1, that integrates two key components: 1) a three-mode capacitor-drop AC-DC rectifier [8] to mitigate bridge voltage stress, reduce idle power, and enhance light-load efficiency; and 2) a full-duty-cycle, input-series dual-branch (ISDB) DC-DC converter. The ISDB converter replaces the traditional SC converter and yields a reduced C_{REC} volume, enhanced load capability, and higher efficiency. This architecture leverages the fact that the AC-DC rectifier's output voltage (V_{REC}) and the DC-DC converter's ground are not required to share the same reference. Two series-connected capacitors (C_H and C_L) are placed across V_{REC}, with the DC-DC converter's ground defined at their mid-point. This splits the high V_{REC} voltage domain into two symmetric lower-voltage domains: a positive domain ($V_{REC}/2$) across C_H and a negative domain ($-V_{REC}/2$) across C_L. A buck converter regulates the positive voltage, yielding $V_{OUT} = D\times V_{REC}/2$, while an inverting buck converter regulates the negative voltage with $V_{OUT} = -D\times -V_{REC}/2$. The output currents from both inductors are combined to supply the load. Critically, as each branch now handles only $V_{REC}/2$, the required voltage rating for all components, including filtering capacitors, flying capacitor, power transistors, and isolation rings, is halved. Furthermore, this dual-branch configuration, operating at a full duty cycle with a conversion ratio of D/2, supports a significantly wider input voltage range than a fixed-ratio SC converter. This inherent voltage flexibility relaxes the V_{REC} ripple requirement, allowing the total capacitance (C_H and C_L) to be reduced by approximately 30%. The total inductor plus capacitors' volume in the ISDB converter is nearly identical to that of the prior SC converters. Thereby, the overall converter volume is reduced. Compared to the SC converter, the ISDB converter also sustains much higher efficiency across broad voltage and load ranges, increasing P_{OUT} under the same V_{REC}. To ensure equal voltage allocation between C_H and C_L, a voltage balance scheme is proposed, which guarantees the reliability of the converter and simultaneously balances the inductor currents in the two branches. Finally, a discontinuous conduction mode (DCM) calibration loop is implemented to reduce inductor losses further and improve light-load efficiency.

As shown in Fig. 19.9.2, the ISDB converter can be simplified into two branches: Branch P comprises C_H, S_1, S_2, and L_1, while branch N includes C_L, S_3, S_4, S_5, and L_2. The inputs of the two branches are in series, and the outputs are in parallel. Consequently, both the switches and capacitors withstand only $V_{REC}/2$. Both branches have the same V_{OUT} and can be controlled independently without mutual interference. The ISDB converter extends the duty cycle to 1 while achieving a VCR of D/2. Figure 19.9.2 then shows the operating principle. In the steady state, the voltages across C_H and C_L are typically $V_{REC}/2$ = 30V and $-V_{REC}/2$ = –30V. In Φ_1, S_1 is turned on and V_{SW1} = 30V. S_3 and S_4 are also turned on. The flying capacitor C_F is connected in parallel with C_L, resulting in V_{CF} = –30V and V_{SW2} = 0. In Φ_2, S_2 and S_5 are on, V_{SW1} = 0 and $V_{SW2} = -V_{CF}$ = 30V. In Φ_3, S_2, S_3, and S_4 are on, resulting in $V_{SW1} = V_{SW2}$ = 0. In Φ_4, S_1 and S_5 are on, so $V_{SW1} = V_{SW2}$ = 30V. To keep two voltages of C_H and C_L equal, a V_{CH} and V_{CL} balance loop is shown in Fig. 19.9.2. The concept is to adjust the duty cycles to control the powers in each branch. When $V_{CH}>V_{CL}$ due to disturbances, the loop makes $D_1>D_2$, and more current is delivered from branch P to the load, reducing V_{CH} and raising V_{CL}, until $V_{CH} = V_{CL}$. Owing to the characteristics of the input-series output-parallel topology [16], the output currents of both branches, which are the inductor currents in the ISDB converter, are proportional to the input voltages, so $I_{L1}/I_{L2} = V_{CH}/V_{CL}$. In this way, the V_{CH} and V_{CL} balance loop also ensures I_{L1} and I_{L2} balance, thus improving efficiency while eliminating complex current-sensing and regulation circuitries.

Figure 19.9.3 shows the system diagram. The power stage of the AC-DC rectifier consists of four 70V-LDMOS ($M_{1\text{-}4}$), two 70V-diodes ($D_{1\text{-}2}$), and five off-chip capacitors C_X, $C_{P1,\,P2}$, and $C_{H,\,L}$. C_X is a 310V_{AC} film capacitor and carries most of the AC voltage. C_{P1} and C_{P2} reduce idle power, and 70V low-profile ceramic capacitors are used. Low and high-side transistors in the rectifier bridge are realized with NMOS devises and diodes, respectively. The hysteresis controller generates the gate signals $V_{GM1\text{-}4}$ of $M_{1\text{-}4}$. C_H and C_L are implemented using 35V-rated aluminum electrolytic capacitors. For the ISDB DC-DC converter, the switches $S_{1\text{-}5}$ are implemented with 40V-LDMOSs. $S_{2,3,4}$ are implemented using NMOSs to reduce on-resistance, and $S_{1,3}$ are PMOS transistors for easy driving. C_F is a 35V-rated ceramic capacitor. A type-III compensation is used for the voltage regulation loop. The V_{CH} and V_{CL} balance loop first senses the mismatch between the voltage of $V_{REC\_P} + V_{REC\_N}$ and GND and then gets the error voltage V_{EA_B} from the error amplifier. V_{EA_B} is used to modify the magnitude of $Ramp_1$ and $Ramp_2$ to modulate the duty cycles of D_1 and D_2 until the balance is achieved. A DCM calibration loop is also designed to enhance the light-load efficiency. Before turning off S_2, the V_{SW1} node and GND voltages are both sampled and then processed by a type-I compensator to generate the error signal V_{EA_DCM}. As illustrated in Fig. 19.9.3, the reverse inductor current reduces V_{EA_DCM}, which advances the turning-off point of S_2, and in this way, negative inductor current is gradually eliminated. Measurement results verify that under light-load DCM conditions with V_{REC} = 50V and V_{OUT} = 5V, the efficiency of the ISDB converter is improved by up to 14%. This approach enhances the light-load efficiency of the AC-DC converter from 51% [8] to 78%.

The AC-DC rectifier was fabricated in a 180nm HV SOI process with an area of 1.45mm×0.6mm. To lower the cost, the ISDB converter was implemented in a 180nm BCD process, with an area of 3.03mm×0.55mm. Figure 19.9.4 presents the measured waveforms when V_{LINE} = 230V@50Hz and V_{OUT} = 5V. Although V_{REC} varies between ~30V and ~54V, the converter maintains a regulated 5V output, indicating a relaxed V_{REC} ripple requirement. Figure 19.9.4 also shows the measured steady-state waveforms of the ISDB converter under various input and output voltages. At V_{REC} = 30V, V_{OUT} = 5V, and I_{OUT} = 0.05A, the converter operates in DCM. It was observed that the DCM calibration loop effectively eliminates negative currents in I_{L1} and I_{L2}. When the input voltage and output current increase to 60V and 0.4A, the ISDB converter operates in continuous condition mode (CCM). As expected, when duty cycle D = 0.8>0.5, overlapping occurs at V_{REC} = 30V and V_{OUT} = 12V, demonstrating support for a wide range of input and output voltages.

Figure 19.9.5 illustrates the measured load transient response waveforms of the ISDB converter for V_{OUT} = 5V. When the load current is switched between 50-to-500mA with ~30ns edges, the under- and over-shoots are 400mV and 200mV, respectively. It can be observed that the currents are well equalized by the V_{CH} and V_{CL} balance loop. The reverse inductor currents after transients are eliminated by the DCM calibration loop. Figure 19.9.5 also shows the measured efficiencies of the ISDB converter and the overall AC-DC converter

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under different AC input and DC output voltages. When V_{LINE} = 230V_{RMS}@50Hz and V_{OUT} = 12V, an 87.2% peak efficiency is achieved. The maximum output power is 2.15W. This work also maintains high efficiency across various output voltages and load currents.

Figure 19.9.6 benchmarks the performance in terms of power density, output power, and efficiency. Figure 19.9.6 also presents the comparison with the state-of-the-art designs. Among the compared designs in Fig. 19.9.6, this work achieves the highest maximum output power of 2.15W, and the highest efficiency of 86.7% at maximum output power. The highest power density of 1088W/cm³ is also achieved. Additionally, the light-load efficiency is improved by at least 18% compared to the prior art in Fig. 19.9.6. Figure 19.9.7 shows the chip micrograph and PCB photos.

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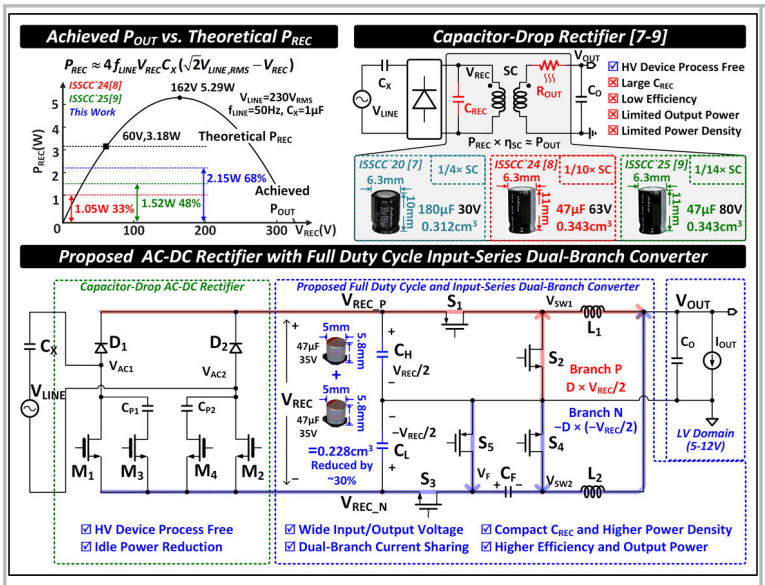


Figure 19.9.1: System diagrams of prior art and the proposed AC-DC converter.

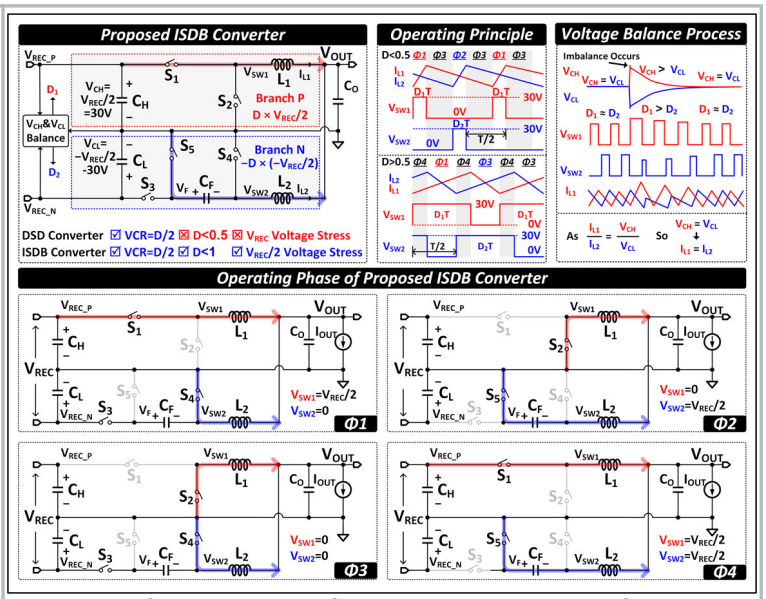


Figure 19.9.2: Comparison of the DSD converter and the proposed ISDB converter, voltage balance process, and the operating principle and phase of the ISDB converter.

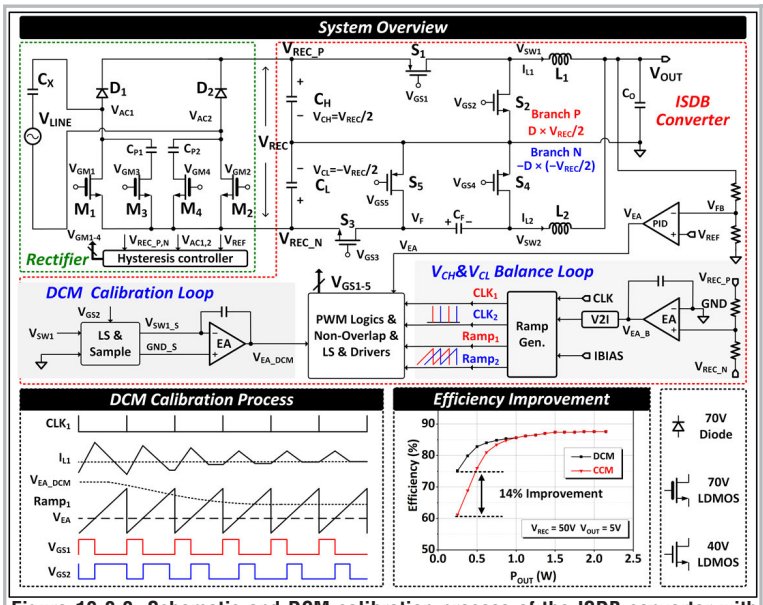


Figure 19.9.3: Schematic and DCM calibration process of the ISDB converter with measurement results of efficiency improvement in DCM.

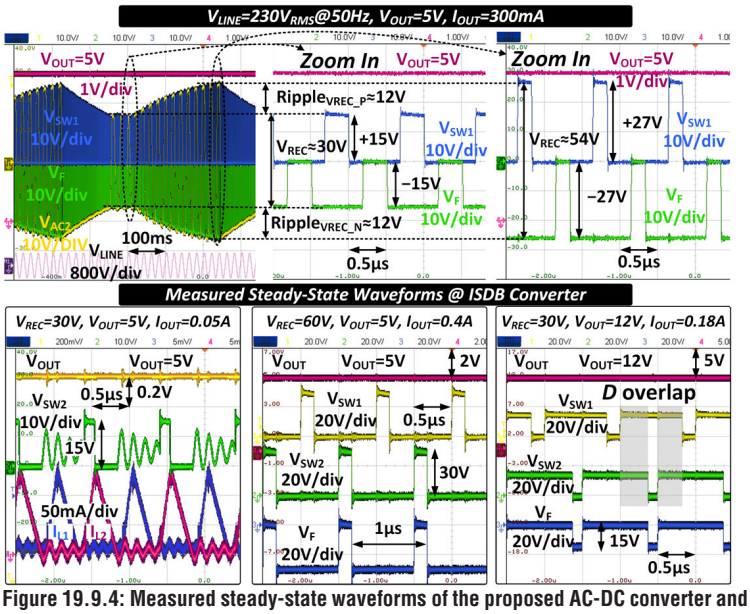


Figure 19.9.4: Measured steady-state waveforms of the proposed AC-DC converter and the ISDB converter.

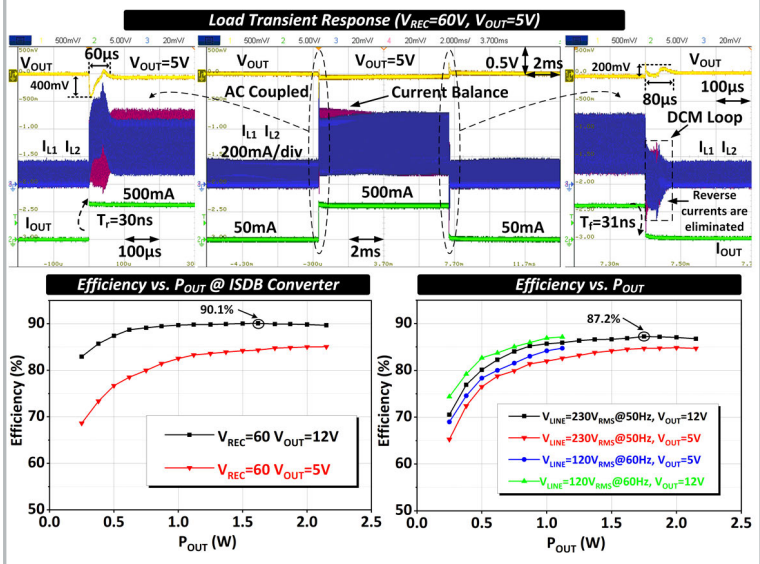
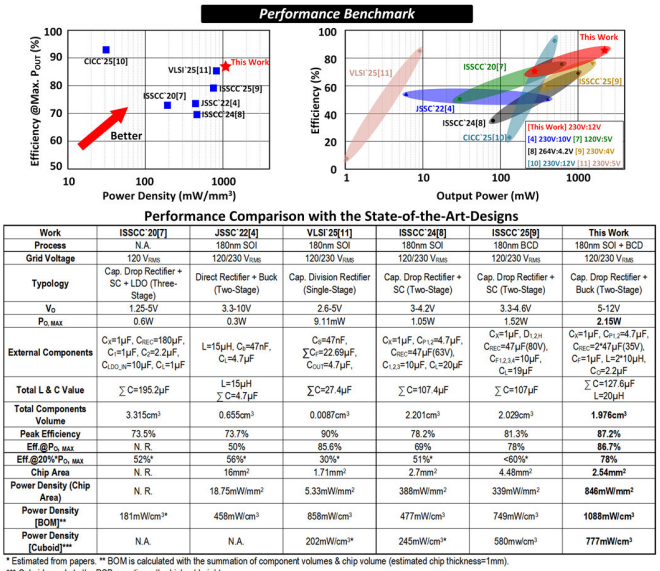


Figure 19.9.5: Measured load transient response, efficiency vs. P_{OUT} under different AC input and DC output voltages.

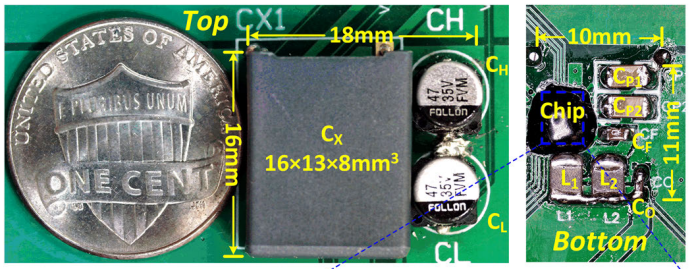


Performance Comparison with the State-of-the-Art-Designs

Work	ISSCC'20[7]	JSSC'22[4]	VLSI'25[11]	ISSCC'24[8]	ISSCC'25[9]	This Work
Process	N.A.	180nm SOI	180nm SOI	180nm SOI	180nm BCD	180nm SOI + BCD
Grid Voltage	120 V_{RMS}	120/230 V_{RMS}	120/230 V_{RMS}	120/230 V_{RMS}	120/230 V_{RMS}	120/230 V_{RMS}
Typology	Cap. Drop Rectifier + SC + LDO (Three-Stage)	Direct Rectifier + Buck (Two-Stage)	Cap. Division Rectifier (Single-Stage)	Cap. Drop Rectifier + SC (Two-Stage)	Cap. Drop Rectifier + SC (Two-Stage)	Cap. Drop Rectifier + Buck (Two-Stage)
V_O	1.25-5V	3.3-10V	2.6-5V	3-4.2V	3.3-4.6V	5-12V
$P_{O,MAX}$	0.6W	0.3W	9.11mW	1.05W	1.52W	**2.15W**
External Components	C_X=1μF, C_{REC}=180μF, C_F=1μF, C_P=2.2μF, C_{LDO_IN}=10μF, C_L=1μF	L=15μH, C_X=47nF, C_L=4.7μF	C_X=1μF, C_{REC}=47μF(63V), $C_{1,2,3}$=10μF, C_L=20μF	C_X=47nF, $\sum C_I$=22.69μF, C_{OUT}=4.7μF,	C_X=1μF, $C_{P1,2}$=4.7μF, C_{REC}=47μF(80V), $C_{F1,2,3,4}$=10μF, C_L=19μF	C_X=1μF, $C_{P1,2}$=4.7μF, C_{REC}=2*47μF(35V), C_F=1μF, L=2*10μH, C_O=2.2μF
Total L & C Value	$\sum$C=195.2μF	L=15μH $\sum$C=4.7μF	$\sum$C=27.4μF	$\sum$C=107.4μF	$\sum$C=107μF	$\sum$C=127.6μF L=20μH
Total Components Volume	3.315cm³	0.655cm³	0.0087cm³	2.201cm³	2.029cm³	**1.976cm³**
Peak Effciency	73.5%	73.7%	90%	78.2%	81.3%	**87.2%**
Eff.@$P_{O,MAX}$	N. R.	50%	85.6%	69%	78%	**86.7%**
Eff.@20%*$P_{O,MAX}$	52%*	56%*	30%*	51%*	<60%*	**78%**
Chip Area	N. R.	16mm²	1.71mm²	2.7mm²	4.48mm²	**2.54mm²**
Power Density (Chip Area)	N. R.	18.75mW/mm²	5.33mW/mm²	388mW/mm²	339mW/mm²	**846mW/mm²**
Power Density [BOM]**	181mW/cm³*	458mW/cm³	858mW/cm³	477mW/cm³	749mW/cm³	**1088mW/cm³**
Power Density [Cuboid]***	N.A.	N.A.	202mW/cm³*	245mW/cm³*	580mW/cm³	**777mW/cm³**

* Estimated from papers. ** BOM is calculated with the summation of component volumes & chip volume (estimated chip thickness=1mm).
*** Cuboid equals to the PCB area times the highest height.

Figure 19.9.6: Performance benchmark and comparison with the state-of-the-art-designs.



Component	Value	Volume
C_X	1μF(310V_{AC})	16×13×8mm³
$C_{P1,P2}$	4.7μF(100V)	3.2×1.6×1.6mm³(1206)
$C_{H,L}$	47μF(35V)	D=5mm, H=5.8mm
C_F	1μF(35V)	1.6×0.8×0.8mm³(0603)
$L_{1,2}$	10μH(DCR=324mΩ)	3.2×2.5×1.2mm³(1210)
C_O	2.2μF(16V)	1×0.5×0.5mm³(0402)

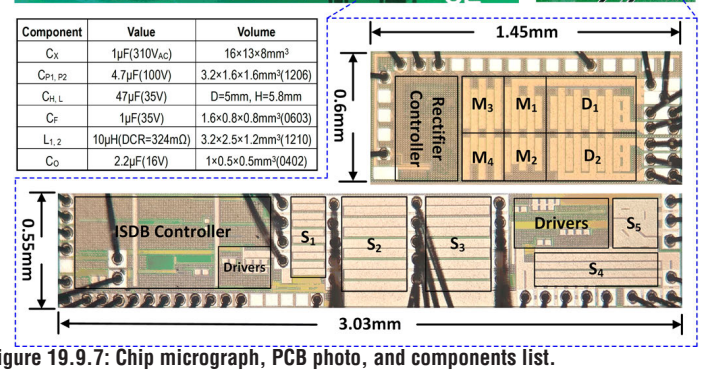


Figure 19.9.7: Chip micrograph, PCB photo, and components list.

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