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Operation and Control of a Grid-Connected Asymmetrical Cascaded Multilevel Inverter

Ali Isazadeh, Jafar Adabi, Mohammad Rezanejad, and M. Ebrahim Adabi

Abstract— **This article presented a new structure for the grid-connected multilevel inverters (MLIs) circuit with the ability of the cascaded connection. The proposed inverter is capable of transformerless connection of distributed generation resources to the network. The control system manages the power injection to the grid by minimizing the output current harmonics as well as exchanging reactive power with the grid. The self-balancing state of the capacitors' voltage is occurred only with the switching technique without any measurement sensors. An enhanced phase-locked loop (EPLL) and a proportional resonant (PR) controller are employed for the proposed asymmetric MLI. An important feature of the proposed inverter is the ability of stable performance and fast dynamics of the control system to the changes of the reference values. Simulation and experimental results are presented in order to validate the performance accuracy of the proposed MLI.**

Index Terms— **Enhanced phase-locked loop (EPLL), grid connected, multilevel inverter (MLI), proportional resonant (PR), self-balancing, transformerless.**

I. Introduction

MULTILEVEL inverters (MLIs) have attracted a great deal of attention in many industrial applications. The main advantages of these converters are high output power quality, lower harmonic content, better electromagnetic compatibility, lower switching losses, lower voltage stress, and higher efficiency [1]–[6]. Three main structures of the MLIs include neutral point clamped (NPC) [7], flying capacitors (FCs) [8], and cascaded H-bridge (CHB) [9]. Asymmetric MLIs are capable of maximizing the number of output voltage levels with lower equipment. Moreover, due to the less use of components, the cost reduces drastically [10], [11]. The main disadvantages of the mentioned topologies are the complicated control for capacitors' voltage balancing (CVB) in NPC and FC and also require multiple isolated dc sources for CHB.

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Switched-capacitor MLIs (SCMLIs) are introduced as another type of MLIs, especially for applications with low input dc sources. Voltage boosting without the use of any transformers or bulky inductors is the most important feature of these multilevel converters [12]–[14]. These structures drop behind from full industrialization and grid connection due to the problems, such as current spikes, voltage drop, and high capacitance. To avoid the mentioned issues, the structures based on active NPC (ANPC) and packed U-cell (PUC) are the best solution. Voltage and current measurement sensors also have to be eliminated to reduce the cost of the system.

Grid-connected MLIs are increasingly employed for power transferring of distributed power generation systems. The main concerns regarding these converters are proper structures for obtaining the highest voltage levels with fewer elements along with increasing system efficiency [15]–[19]. In general, the current control loop and phase-locked loop (PLL) are needed to connect the inverter the grid, which both have a direct impact on the stability of the grid-connected inverter [20]–[23].

Grid-connected single-phase inverters are investigated in [24]–[32]. A structure involving a controller for connecting a solar cell to the grid is presented in [24]. An amorphous alloy magnetic-bus-based NPC converter is investigated in [25], which reduces the control complexity for voltage balancing of the common-mode point in a grid-connected mode. A modified ANPC model is examined in [26], where a lookup table-based CVB strategy is used to simplify the control. The application of a specific type of filter in the MLI output is investigated in [27] without using an additional controller for CVB. Its advantage is the significant reduction of the common-mode voltage, which is discussed in [28]. An asymmetric CHB inverter is employed in [29], in which a PLL, *LCL* filter, and a control method are used for better stability and performance for a distorted network.

A five-level packed U-cell (PUC5) is introduced in [30], which does not need a voltage sensor for CVB due to its switching strategy. Its control section only involves PLL and a proportional–integral (PI) controller. Model-predictive control of a grid-connected seven-level packed U-cell (PUC7) inverter is discussed in [31] and [32], in which voltage sensor is used for capacitors voltage measurement. Makhamreh *et al.* [32] presented a Lyapunov-based control strategy for mentioned PUC7.

Du *et al.* [34] presented a cascaded MLI with a higher number of levels where higher voltage dc link and higher

amount capacitors are required. A detailed review on the module structure of modular multilevel converter (MMC) is presented in [35], which can be selected for other applications of grid-connected MLIs. Note that the main issue of MMC structure is its control complexity and difficult CVB.

This article aims at presenting a modular structure of a transformerless grid-connected MLI. Also, a proper controller has been addressed to reduce the control complexity. A grid-connected controller with the capability of capacitors voltage's self-balancing is presented to achieve a fast dynamic response. The control section is based on active power transmission and reactive power exchange with the grid. In addition, nonideal proportional resonant (PR) controller with harmonic compensators is used. The proposed circuit is able to generate a high number of voltage levels by cascading different modules without using any sensors for the voltage balance of the capacitors. Capacitors' current spike are eliminated due to series charging and discharging of the capacitors in the load path. This inherently bipolar converter is able to operate as a bidirectional converter with high efficiency.

In Section II, the main 5-level module and cascade connection of two modules (to achieve an11-level inverter) are discussed. Circuit control strategy at the grid-connected mode, enhanced phase-locked loop (EPLL), PR controller, phase disposition (PD) modulation technique, the capacitor's energy calculation, and the technique applied for the capacitor's balancing are all discussed in Section III. Simulation and experimental results are shown in IV. A general summary of the results of this article is presented in V.

II. Proposed Module

The proposed MLI structure is based on the cascaded connection of five-level modules. Each module includes six switches, a dc source, and a capacitor [see Fig. 1(a)].

The capacitors in each module are balanced at half of the dc-link voltage. Therefore, the module with the dc-link voltage of V_{dc} has five output levels of $\pm V_{dc}$, $\pm V_{dc}/2$, and 0. Fig. 1(b) shows a two-module grid-connected asymmetrical system (with dc-link voltages of V_{dc} and $2V_{dc}$), which can generate 11 output voltage levels. Table I displays the switching states, adjacent states of each level, output voltage of each module, output voltage of the circuit, and condition of capacitors C_1 and C_2 [charging (C), discharging (D), and no change (N) state].

III. Operating Principals and Control

Fig. 2 shows the grid-connected inverter and its control. V_i is the output voltage of the proposed inverter, i_g is the current of the grid-connected inverter, L_f is the interface inductor filter between grid and converter, Z_g is the grid impedance, and V_g is the grid voltage. Due to the use of 11-level inverter, switching frequency and size of the interface inductor will be much lower, and there would be no need for a particular compensator in the output. In this article, due to the small amount of Zg, it is considered to be zero. Grid voltage and current are as follows:

$$v_g(t) = V_m \sin \omega t \quad (1)$$

$$i_g(t) = I_m \sin(\omega t + \theta) \quad (2)$$

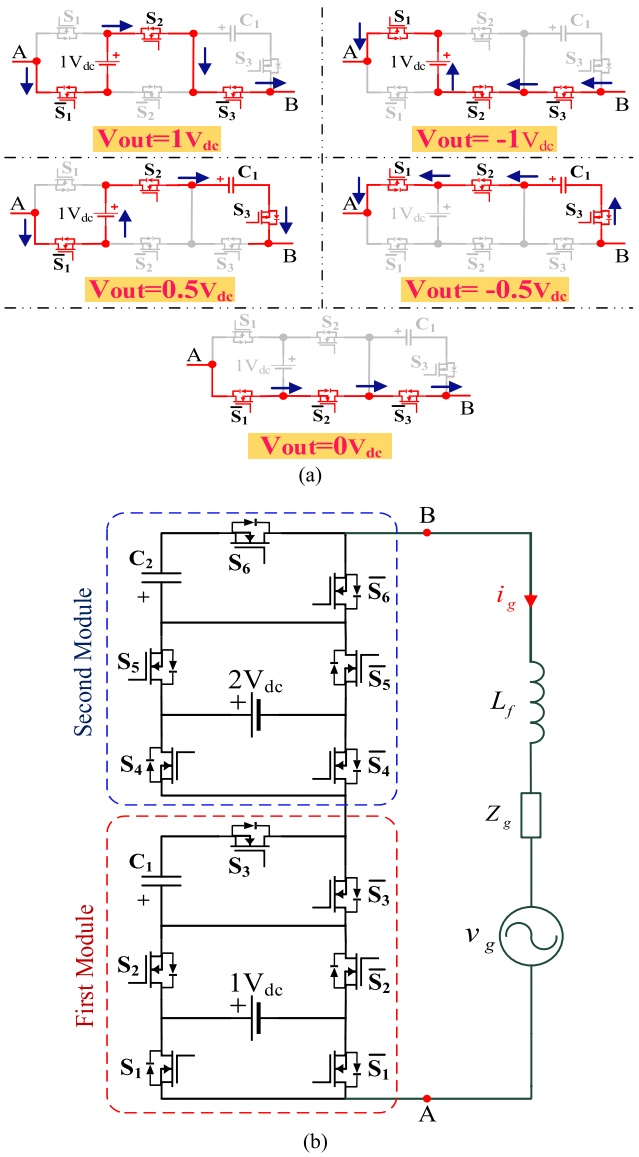

Fig. 1. (a) Different voltage levels of the proposed module. (b) Proposed two-module 11-level MLI.

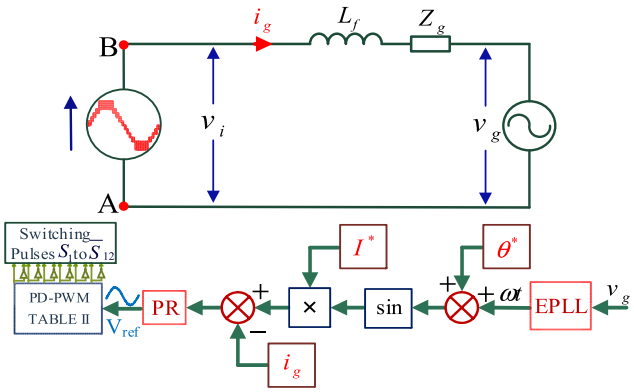

Fig. 2. Block diagram of the grid-connected single-phase MLI proposed with a closed-loop control algorithm.

where V_m, I_m, and θ are the value of the voltage magnitude, current magnitude, and the angle difference value between voltage and current of the grid, respectively. For exchanging

the reactive power of the inverter with the grid, the angle difference value between the voltage and the current of the grid is significant. Therefore, in the control design section of the proposed grid-connected inverter based on (2), I^* reference value is replaced by I_m and θ^* reference value is replaced by θ.

The EPLL block is the synchronous system for detecting the phase and frequency of the grid, which would have a proper response in case of balanced or unbalanced states of the grid voltage. ωt is the output of the EPLL block, and by adding to θ^*, reactive power injection can also be achieved. For $\theta^* = 0$, the exchanged reactive power with the grid is zero and only the active power transfer with a unity power factor is obtained for the MLI. Also, the control structure is in a way that the amount of transmitted active power to the grid can be regulated by changing I^*. PR current control is among the conventional controllers, which sets the error of the measured reference current to zero. The output of this current control will determine the magnitude of sinusoidal reference voltage (V_{ref}). It enters the phase disposition PWM (PD-PWM) modulator and provides the switching model for current injection, which leads to power transfer to the grid. The control circuit and the self-balancing feature of the capacitors' voltage are synchronized and improved the dynamic capability of the 11-level grid-connected inverter system.

A. Enhanced Phase-Locked Loop

EPLL is PLL is a simple and effective tool with a nonlinear structure that can synthesize a signal whose phase angle is locked to that of a given input signal. The input signal is an alternative signal with a reference frequency, but it might be distorted due to the presence of nonlinear loads in the grid and the reference frequency changes. PLL has two major drawbacks in the power and control systems applications: 1) the loop a double-frequency ripple even in the most ideal case where the input signal is pure sinusoidal and 2) the output signal value has no relation to its input signal. EPLL has resolved these two problems, and it is particularly powerful in power electronics and power quality systems. The general structure of an EPLL is shown in Fig. 3, where u is the voltage sensor value (V_g), ωt is the output signal, ω_0 indicates system frequency, and A and ωt indicate the magnitude and angle, respectively. μ_1, μ_2, and μ_3 are constant and positive numbers. In fact, EPLL has an internal PLL that is made by adding other control loops. In addition, it eliminates ripples [21], [22].

B. PR Controller

The ideal PR controller with the ability to produce a zero steady-state error for the sinusoidal reference signal can eliminate disturbances. However, due to the very low bandwidth, the smallest frequency variation will cause the error not to be detected. This controller has infinite gain and also needs a grid with infinite quality factor. The nonideal PR control has been more resistant to variations due to the increased bandwidth of the controller. In addition, easy implementation and harmonic compensation for low-order harmonics, with no effects on the system dynamics and overall bandwidth, has turned this controller into an efficient system for connecting distributed power sources to the power grid [33].

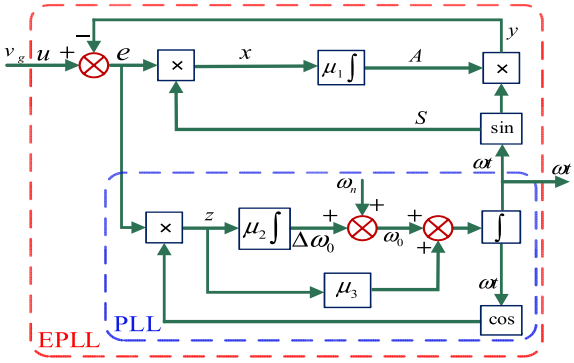

Fig. 3. EPLL structure.

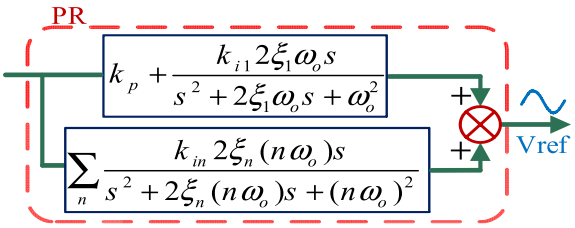

Fig. 4. Block diagram of the PR controller and the harmonic compensator.

In some conditions, the injected current to the grid includes some major harmonics; to this end, the PR controller is applied to the harmonic compensator. This controller will be achieved by parallelizing the resonance compensators, which are adjusted with the relevant harmonic frequency, with the PR controller block. PR controller along with the harmonic compensators is shown in Fig. 4. The bandwidth selection would be possible in these relations. The larger ζ, the broader the controller's bandwidth. The interesting capability of the compensator is that it does not affect the controller's dynamic. The PR controller method is an appropriate one for injecting unbalanced current in the distorted or unbalanced grid. It is accurate and its computational complexity is low [17], [20].

C. Pulsewidth Modulation Technique

PD-PWM is applied for the switching strategy of the proposed grid-connected inverter. Less total harmonic distortion (THD) and easy implementation are the most important features of this technique [12], [27]. According to Fig. 5, in the proposed 11-level inverter, a sinusoidal wave (V_{ref}) made from the PR controller output is compared with ten triangular carrier waves (V_{t1}–V_{t10}) for generating switches' gate pulse. The triangular carrier waves have the same frequency (f_t) and magnitude but different offset voltages. As it can be observed, Fig. 5 shows the switches' gate pulse. Switches $\bar{S}_4.S_4.\bar{S}_1.S_1$ work at grid frequency which is a very lower frequency. Table II illustrates the PD-PWM algorithm for generating each voltage level. This table is selected based on the best switching states of Table I so that all switches equally involve in turning on/off and switching loss distributed among all switches.

D. Calculation of Capacitance

In this section, the mathematical proof of self-balancing state of the capacitors' voltages is provided. The significance

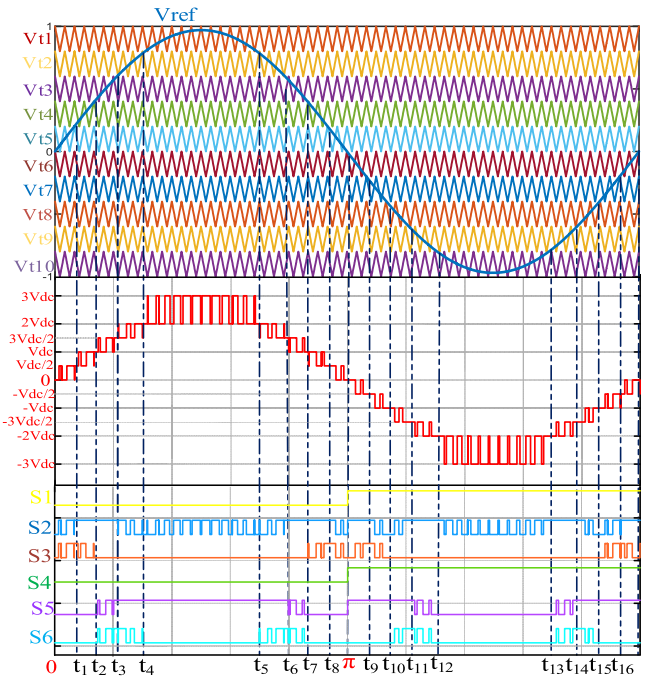

Fig. 5. PD-PWM modulation for the proposed converter.

TABLE I

SWITCHING PATTERNS AND STATES OF THE CAPACITORS AT EACH VOLTAGE LEVEL FOR PROPOSED 11-LEVEL MLI

Level	S_1	S_2	S_3	S_4	S_5	S_6	V_{M1}	V_{M2}	V_{out}	C_1	C_2
+5	0	1	0	0	1	0	$1V_{dc}$	$2V_{dc}$	$3V_{dc}$	N	N
+4	0	0	0	0	1	0	0	$2V_{dc}$	$2V_{dc}$	N	N
	1	1	0	0	1	0					
+3	0	1	0	0	1	1	V_{dc}	$V_{dc}/2$	$3V_{dc}/2$	N	C
+2	0	1	0	0	0	0	V_{dc}	0	V_{dc}	N	N
	0	1	0	1	1	0					
+1	0	1	1	0	0	0	$V_{dc}/2$	0	$V_{dc}/2$	C	N
	0	1	1	1	1	0					
0	0	0	0	0	0	0	0	0	0	N	N
	0	0	0	1	1	0					
	1	1	0	0	0	0					
	1	1	0	1	1	0					
-1	1	1	1	1	1	0	$-V_{dc}/2$	0	$-V_{dc}/2$	D	N
	1	1	1	0	0	0					
	0	0	1	0	0	0					
	0	0	1	1	1	0					
-2	1	0	0	1	1	0	$-V_{dc}$	0	$-V_{dc}$	N	N
	1	0	0	0	0	0					
-3	1	1	0	1	1	1	0	$-3V_{dc}/2$	$-3V_{dc}/2$	N	D
	0	0	0	0	0	1					
	1	1	0	0	0	1					
	0	0	0	1	1	1					
-4	1	1	0	1	0	0	0	$-2V_{dc}$	$-2V_{dc}$	N	N
	0	0	0	1	0	0					
-5	1	0	0	1	0	0	$-1V_{dc}$	$-2V_{dc}$	$-3V_{dc}$	N	N

of being self-balanced even when the grid is not balanced is among the proposed inverter's feature. The voltage on the C_1 and C_2 capacitors, by considering $\Delta\%$ capacitor's voltage ripple, is approximately kept at $(V_{dc}/2)$ and $(3V_{dc}/2)$,

TABLE II

LIST OF THE ON-STATE SWITCHES IN EACH LEVEL

Relationship between V_{ref} and V_{ti}	On-state switches	Output Voltage
$V_{ref} > V_{t1}$	$\bar{S}_1, S_2, \bar{S}_3, \bar{S}_4, S_5, \bar{S}_6$	$+3V_{dc}$
$V_{t2} < V_{ref} < V_{t1}$	$\bar{S}_1, \bar{S}_2, \bar{S}_3, \bar{S}_4, S_5, \bar{S}_6$	$+2V_{dc}$
$V_{t3} < V_{ref} < V_{t2}$	$\bar{S}_1, S_2, \bar{S}_3, \bar{S}_4, S_5, S_6$	$+3V_{dc}/2$
$V_{t4} < V_{ref} < V_{t3}$	$\bar{S}_1, S_2, \bar{S}_3, \bar{S}_4, \bar{S}_5, \bar{S}_6$	$+V_{dc}$
$V_{t5} < V_{ref} < V_{t4}$	$\bar{S}_1, S_2, S_3, \bar{S}_4, \bar{S}_5, \bar{S}_6$	$+V_{dc}/2$
$V_{t6} < V_{ref} < V_{t5}$	$\bar{S}_1, \bar{S}_2, \bar{S}_3, \bar{S}_4, \bar{S}_5, \bar{S}_6$	0
	$S_1, S_2, \bar{S}_3, S_4, S_5, \bar{S}_6$	
$V_{t7} < V_{ref} < V_{t6}$	$S_1, S_2, S_3, S_4, S_5, \bar{S}_6$	$-V_{dc}/2$
$V_{t8} < V_{ref} < V_{t7}$	$S_1, \bar{S}_2, \bar{S}_3, S_4, S_5, \bar{S}_6$	$-V_{dc}$
$V_{t9} < V_{ref} < V_{t8}$	$S_1, S_2, \bar{S}_3, S_4, S_5, S_6$	$-3V_{dc}/2$
$V_{t10} < V_{ref} < V_{t9}$	$S_1, S_2, \bar{S}_3, S_4, \bar{S}_5, \bar{S}_6$	$-2V_{dc}$
$V_{ref} < V_{t10}$	$S_1, \bar{S}_2, \bar{S}_3, S_4, \bar{S}_5, \bar{S}_6$	$-3V_{dc}$

respectively. Fig. 6 shows the diagram of the voltage waveform and the inverter's output current along with the capacitors' voltage. Grid current can be written as

$$i_g(t) = I_m \sin(\omega t - \phi) \tag{3}$$

where ϕ is the angle between inverter voltage and current.

As the absorbed or delivered energy to the output load is through C_1 and C_2, the following equation is obtained:

$$I = \frac{dq}{dt} \rightarrow dU = V dq = V I dt \rightarrow U = \int V I dt \tag{4}$$

where I, q, and U are the capacitors current, charge, and energy, respectively. According to Fig. 5 and by inserting (3) into (4), absorbing energy of C_1 in positive half-cycle can be calculated as (5), shown at the bottom of the next page.

Similarly, absorbing energy of C_2 is achieved as follows:

$$U_{c2}^{+} = 1.5\ V_{\mathrm{DC}} I_m \begin{pmatrix} \cos(\alpha_3 - \phi) - \cos(\alpha_4 - \phi) \\ +\cos(\alpha_5 - \phi) - \cos(\alpha_6 - \phi) \end{pmatrix}. \tag{6}$$

With the same procedure, delivering energy of C_1 and C_2 in negative half-cycle can be achieved as

$$U_{c1}^{-} = 0.5\ V_{\mathrm{DC}} I_m \begin{pmatrix} \cos(\alpha_9 - \phi) - \cos(\alpha_{10} - \phi) \\ +\cos(\alpha_{15} - \phi) - \cos(\alpha_{16} - \phi) \end{pmatrix} \tag{7}$$

$$U_{c2}^{-} = 1.5\ V_{\mathrm{DC}} I_m \begin{pmatrix} \cos(\alpha_{11} - \phi) - \cos(\alpha_{12} - \phi) \\ +\cos(\alpha_{13} - \phi) - \cos(\alpha_{14} - \phi) \end{pmatrix}. \tag{8}$$

Considering symmetrical switching angles, one can have

$$\begin{cases} \alpha_9 = \pi + \alpha_1,\ \alpha_{10} = \pi + \alpha_2,\ \alpha_{15} = \pi + \alpha_7,\ \alpha_{16} = \pi + \alpha_8 \\ \alpha_{11} = \pi + \alpha_3,\ \alpha_{12} = \pi + \alpha_4,\ \alpha_{13} = \pi + \alpha_5,\ \alpha_{14} = \pi + \alpha_6. \end{cases} \tag{9}$$

Having the abovementioned symmetry in the switching pattern, the capacitors' energy in the negative and positive half-cycles is equal

$$U_{c1}^{+} = -U_{c1}^{-},\ U_{c2}^{+} = -U_{c2}^{-}. \tag{10}$$

Therefore, the self-balancing performance of the capacitors is guaranteed, which eliminates the application of sensor in the balancing control system [30].

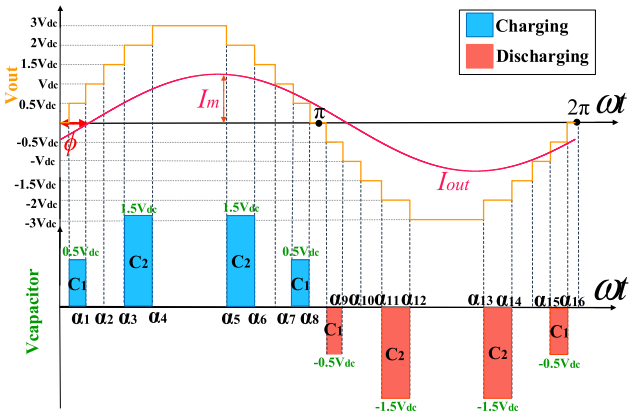

Fig. 6. Typical output voltage and current of the proposed inverter.

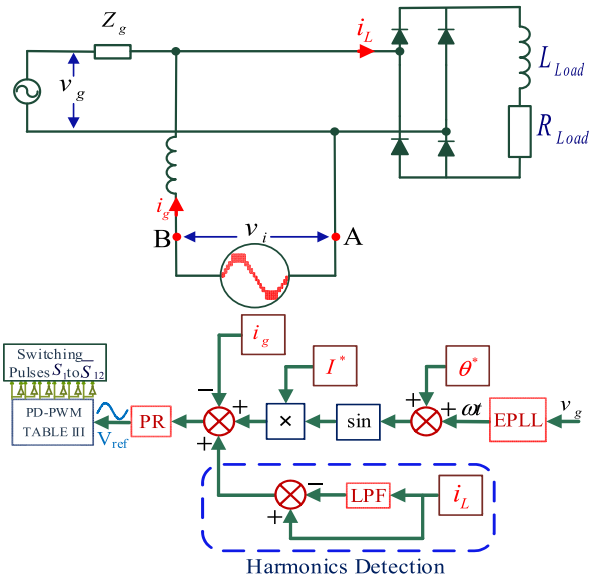

Fig. 7. Harmonic compensation of a nonlinear load with the proposed converter structure.

E. Harmonic Compensation

The proposed converter is also capable of harmonic compensation without any problems for the CVB. Fig. 7 shows the structure of the proposed converter in compensation of a nonlinear load. A low-pass filter is used to obtain the nonlinear load harmonic orders in the control system to build the proper reference current [36].

TABLE III

COMPARISON OF THE PROPOSED 11-LEVEL MLI WITH OTHER GRID-CONNECTED INVERTER TOPOLOGIES

	[26]	[27]	[28]	[29]	[31]	[32]	**Proposed**
Levels	9	9	9	17	7	7	**11**
DC Sources	1	1	1	3	1	1	**2**
Active switches	10	10	8	12	6	6	**12**
Capacitors	3	3	1	0	1	1	**2**
Diodes	10	10	8	12	6	6	**12**
TSV ($\times V_{dc}$)	5	4	6	36	4	4	**16**
control	PI	PR	PI	SRF-PI	PI - Predictive Control	Lyapunov-Predictive Control	**PR/EPLL**
Filter	L	L	LC	LCL	L	L	**L**
Self-balanced capability	no	yes	no	-	no	no	**yes**

F. Comparison Study

Table III compares some famous grid-connected inverter topologies in terms of a number of components and requirements of capacitor balancer. It should be noted that each topology has its own performance and conditions (with regard to the number of output voltage levels and control requirements). Therefore, a fair comparison cannot be made, but some main factors are listed to show that the proposed converter is a compromise of different design considerations. According to this table, [26], [28], [31], and [32] need measurements' sensors for the CVB. It leads to the control complexity of the converter, while the capacitors of the proposed topology and [27] are self-balanced. In [29], three dc sources are used without any capacitors. Synchronous reference frame PLL with PI control (SRF-PI) is used. The mentioned system uses a third-order output filter (*LCL*) with many sensors, which leads to a complex control system. Total standing voltage (TSV) of switches in structures [2]6, [27], [28], [31], [32] may have lower TSVs, but they need higher voltage dc sources.

$$
\begin{aligned}
U_{c1}^{+} &= \int_0^{\pi} V_m I_m \sin(\omega t-\phi)d(\omega t) = I_m \int_0^{\pi} V_m \sin(\omega t-\phi)d(\omega t) \\
&= I_m \left(\begin{array}{c} \int_0^{\alpha_1} 0\times\sin(\omega t-\phi)d(\omega t) + \int_{\alpha_1}^{\alpha_2} 0.5\ V_{\mathrm{DC}}\times\sin(\omega t-\phi)d(\omega t) + \\ \int_{\alpha_2}^{\alpha_7} 0\times\sin(\omega t-\phi)d(\omega t) + \int_{\alpha_7}^{\alpha_8} 0.5\ V_{\mathrm{DC}}\times\sin(\omega t-\phi)d(\omega t) + \\ \int_{\alpha_8}^{\pi} 0\times\sin(\omega t-\phi)d(\omega t) \end{array} \right) \\
&= -0.5\ V_{\mathrm{DC}} I_m \cos(\omega t-\phi)\Big|_{\alpha_1}^{\alpha_2} - 0.5\ V_{\mathrm{DC}} I_m \cos(\omega t-\phi)\Big|_{\alpha_7}^{\alpha_8} \\
&= 0.5\ V_{\mathrm{DC}} I_m \left(\begin{array}{c} \cos(\alpha_1-\phi) - \cos(\alpha_2-\phi) \\ +\cos(\alpha_7-\phi) - \cos(\alpha_8-\phi) \end{array} \right)
\end{aligned} \tag{5}
$$

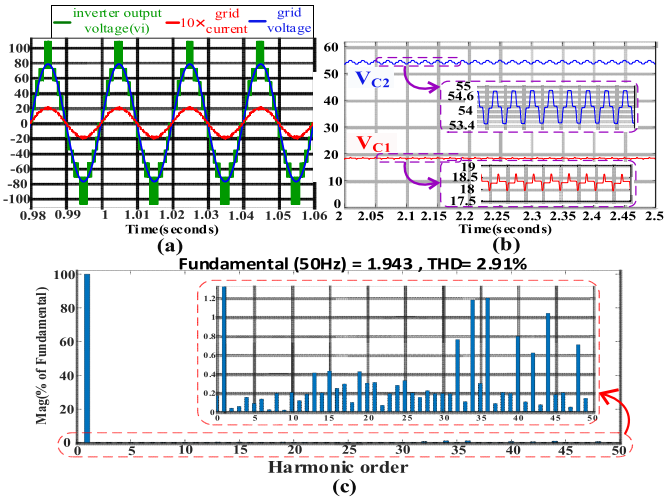

Fig. 8. Simulation results. (a) Injection of active power into the grid. (b) Capacitors' voltages. (c) Harmonic spectrum of grid current.

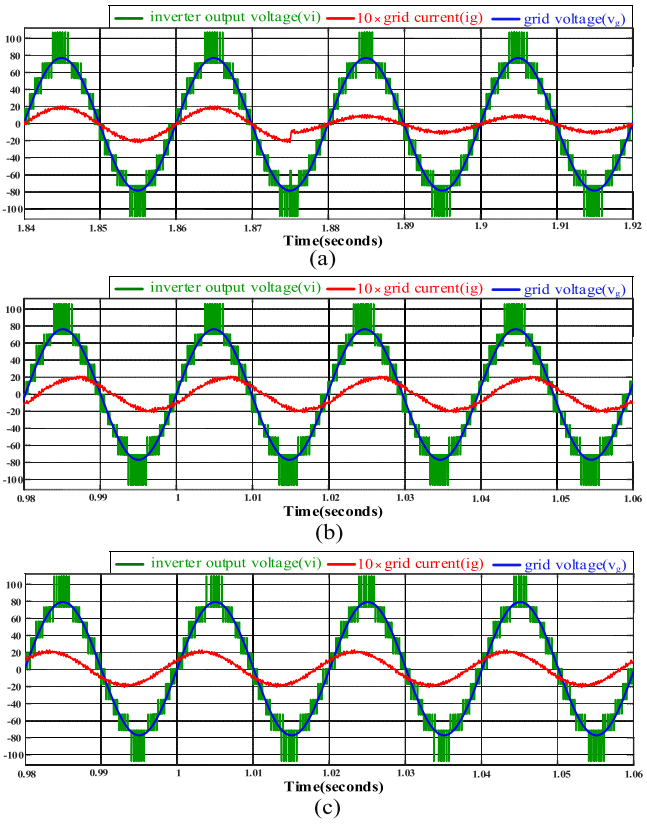

Fig. 9. Simulation results—the transient for the case of (a) changing current reference amplitude (I^*) 2–1-A inverter and grid voltages, with grid current (b) lagging by $\theta^* = -30°$ and (c) leading by $\theta^* = +30°$.

IV. Simulation and Experimental Results

A. Simulation Results

MATLAB simulation results are presented for the mentioned 11-level inverter (with the system parameters of Table IV) to validate the accurate circuit performance. Fig. 8 shows the waveform of the inverter voltage, grid voltage, and grid current.

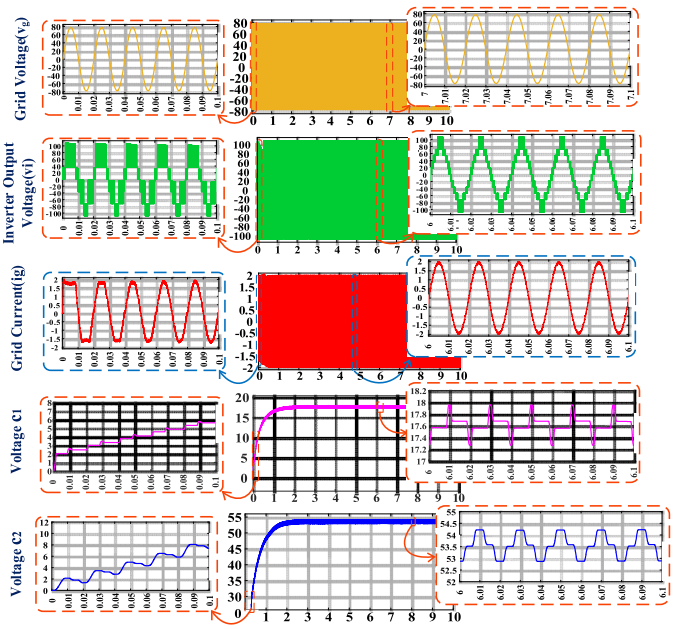

Fig. 10. Simulation results for grid and inverter voltages, and grid current and capacitors voltages waveforms during start-up of the proposed inverter.

TABLE IV
Simulation and Experimental Parameters

Parameters	Symbol	Value
Grid Voltage	V_g	55Vrms
Grid Frequency	f_g	50Hz
Carrier Frequency	f_t	3kHz
Grid Link Inductor	L_f	3.2mH
Capacitors	C_1, C_2	1000μF , 2200μF
DC link voltages	V_{dc1}, V_{dc2}	36V , 72V
Grid Resistance	Z_g	0.06Ω

Moreover, by selecting proper reference current and angle ($\theta^* = 0$ and $I^* = 2$A) for the controller, its accurate performance in injecting active power to the grid by the proposed inverter can be observed. The capacitors' voltage ripple is shown too. The THD value of the grid current is 2.91%. Fig. 9 shows the fast dynamic response of the controller system in the power injection mode by changing the reference current. Figs. 10 and 11 show the grid voltage, inverter output voltage, grid current, and the voltage waveforms of capacitors C_1 and C_2 for circuit startup (from zero to steady state) and grid voltage changes, respectively. In the case of startup, the capacitors' voltage will naturally converge on the required values. Also, for the case of grid voltage transitions, the results show that capacitors' voltages will reach the required values after a change in grid voltage. Fig. 12 shows the grid, converter, and nonlinear load currents. Three different scenarios are considered. At the first step, the proposed inverter is transferring power to the grid, and at the second step, a nonlinear load is connecting to the point of common coupling and compensates for the current harmonics in order to make the grid current sinusoidal. At the third step,

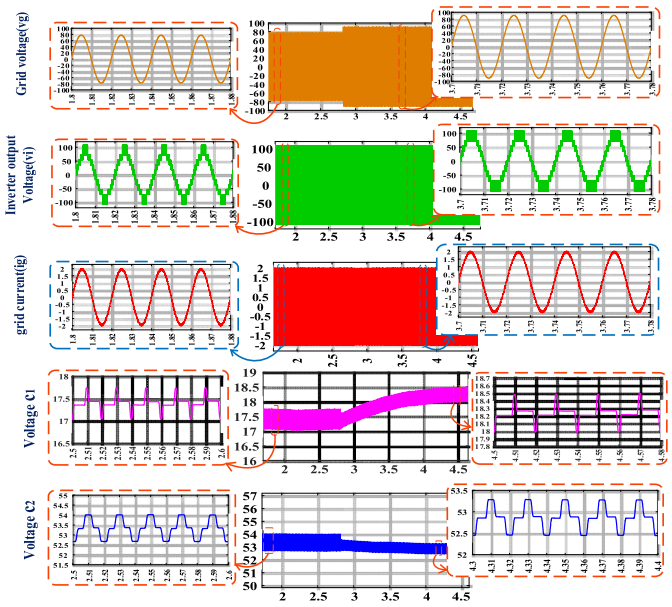

Fig. 11. Simulation results for grid and inverter voltages, and grid current and capacitors voltages waveforms for grid voltage changes.

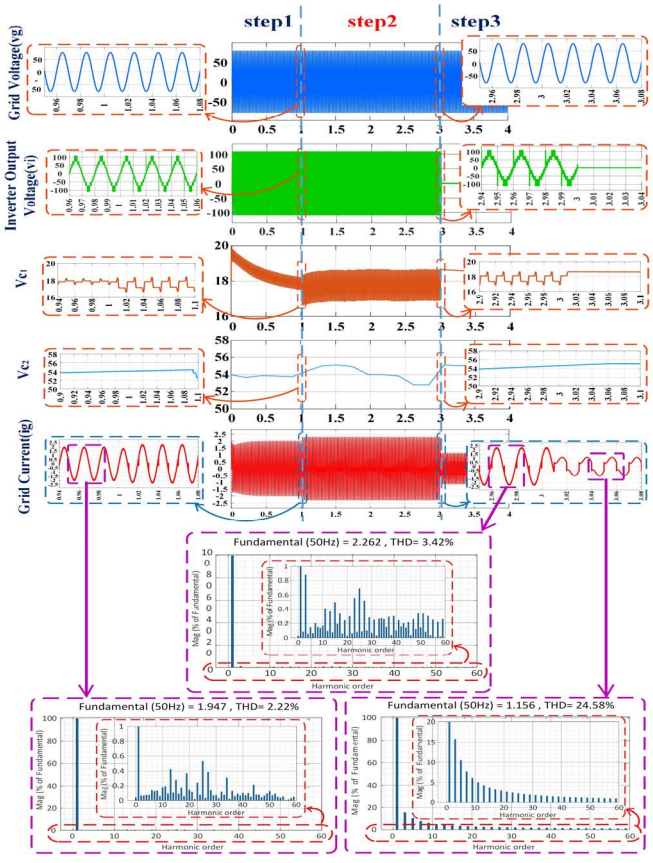

Fig. 12. Simulation results for the proposed converter as harmonic compensator. Grid voltage, inverter voltage, grid current, and capacitors voltages for three steps. Step 1—only inverter is connected to the grid. Step 2—nonlinear load is also connected to the point of common coupling. Step 3—inverter is disconnected and the grid supplies the load.

an inverter is disconnected and the load is supplied from the network, which includes different harmonic orders. As shown in this figure, the capacitors' voltage is self-balanced.

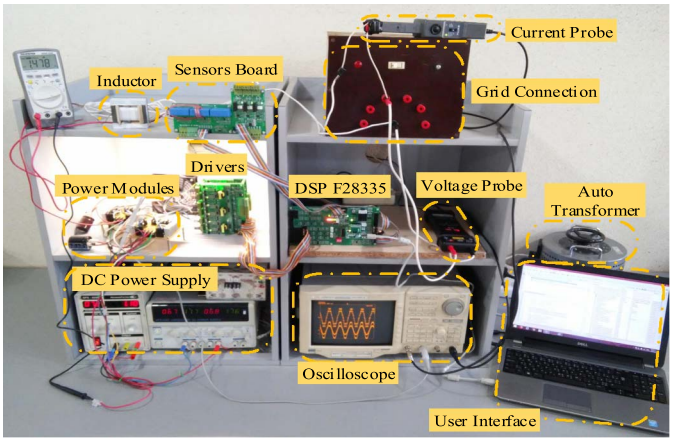

Fig. 13. Experimental setup.

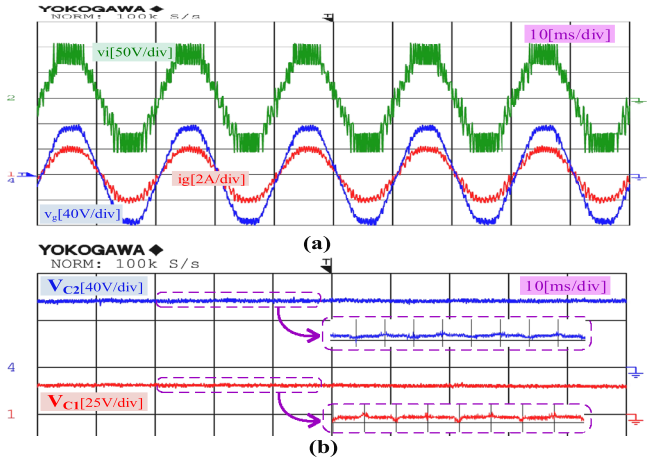

Fig. 14. Experimental results. (a) Injection of active power into the grid. (b) Capacitors' voltages.

B. Experimental Results

To validate the accuracy of the proposed module, an 11-level sample of the proposed inverter was implemented at the power-electronics laboratory and its overall picture is brought in Fig. 13. In this implemented sample, MOSFET switch (IRFP 460), (HCPL-316J) for the optocoupler driver section, LEM LA 55-P for the current sensor, and DSP TMS320F28335 for the processor are applied. Other information is provided in Table III. In this sample, all parts of the control loops, along with the PD-PWM switching technique, are implemented. Fig. 14 shows the inverter's voltage waveform, grid, grid current, and the capacitors' voltage ripple. Also, the accurate performance of the controller of the proposed inverter in injecting active power to the grid is proved by selecting reference angle and current ($\theta^* = 0$ and $I^* = 2$ A). The THD value of the grid current in the implemented practical sample is 3.71%, which is compliant with (IEEE519) standard for the grid-connected inverter. The power injection mode by changing the reference current and fast dynamic response of the controller system is shown in Fig. 15. Also, by changing the reference angle, the reactive power exchange with the grid is possible for the proposed inverter. The achieved

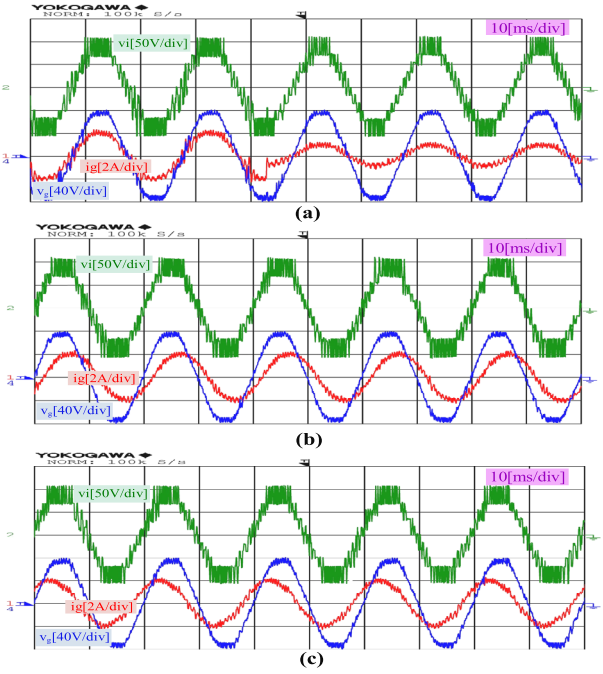

Fig. 15. Experimental results—the transient for the case of (a) changing current reference amplitude (I^*) 2–1-A inverter and grid voltages, with grid current (b) lagging by $\theta^* = -30°$ and (c) leading by $\theta^* = +30°$.

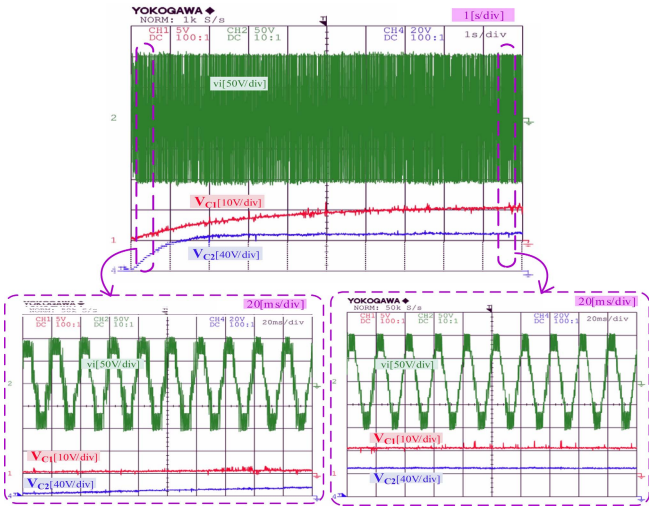

Fig. 16. Experimental results for inverter output and capacitors voltages waveforms during startup of the proposed inverter.

results are exactly equal to the simulation values, and this is indicative of the performance accuracy of the proposed inverter. Fig. 16 shows the experimental results' inverter output voltage and capacitors' voltage for a circuit startup where the capacitors' voltage reaches its predetermined values.

Fig. 17 shows the grid current and voltages as well as capacitors' voltage for the case of grid voltage changes. It is noticeable that capacitors' voltages reach its desired value. Finally, harmonic compensation capability of the proposed converter is shown in Fig. 18 where the grid and load currents are shown when the nonlinear load is not connected—inverter transfers the power to the grid (step 1) and inverter injects

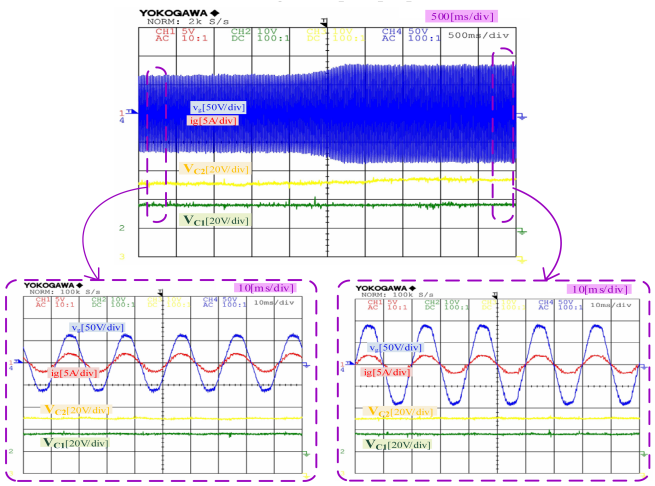

Fig. 17. Experimental results for grid voltage changes: grid voltage (V_g), grid current (I_g), and capacitors voltages.

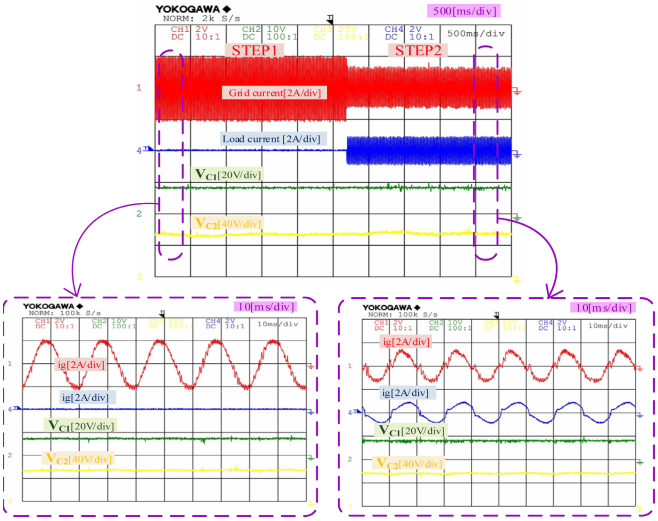

Fig. 18. Experimental results for grid and load currents at (step 1)—inverter is only connected to the grid—and (step 2)—a nonlinear load is connected and the inverter transfers the power to the grid as well as compensates for the load current harmonics.

power to the grid and also compensate the nonlinear load harmonics (step 2).

V. Conclusion

This article investigates the new structure of the single-phase grid-connected transformerless MLI with the cascaded connection. By combining the appropriate controller system for grid connection and the self-balancing feature of the capacitors' voltage, the proposed inverter has significantly reduced the number of sensors and the complexity of the control system. Along with the high dynamics of the control system, the proposed inverter is capable of current and power injection to the grid and reactive power exchange with the grid. In the control system, EPLL is applied for synchronization and in-phase of the grid, which is capable of functioning at the nonbalanced condition of the grid voltage. Moreover, the

nonideal PR controller with the harmonic compensator is used in the current control. PD-PWM modulation state applied for the proposed inverter, along with the mathematical calculation of the capacitors' energy for balancing state, is investigated. A significant advantage of the proposed grid-connected MLI is cost reduction and increased efficiency of the system for the industrialization of these types of inverters. In the end, simulation and experimental results are carried out, which are indicative of the performance accuracy of the proposed inverter along with the IEEE519 standard.

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