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A Hybrid Modulation Scheme for Efficiency Optimization and Ripple Reduction in Secondary-Side Controlled Wireless Power Transfer Systems

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***Abstract*— This article presents a hybrid modulation (HM) scheme to facilitate secondary-side control (SSC) in wireless power transfer (WPT) systems. To achieve broad power regulation in WPT systems, the conventional pulsewidth modulation (PWM) exhibits a significant efficiency drop under light loads, while the existing pulse density modulations (PDMs) lead to considerable current and voltage ripples. To address this issue, an optimal discrete PDM (D-PDM) is proposed for active rectifier modulation. By symmetrically and uniformly distributing pulses, the proposed optimal D-PDM eliminates even-subharmonics in rectifier input voltage, thereby reducing the current distortions and output voltage ripple while removing the capacitor dc blocking voltages. Moreover, pulsewidth regulation is incorporated into the optimal D-PDM, enabling continuous output tuning and further minimizing subharmonics in the voltage. Based on a WPT prototype, the proposed HM is benchmarked with the existing PWM and PDMs. The experimental results show that the proposed HM significantly mitigates current and voltage ripples while facilitating continuous tuning when compared with the existing PDMs. In addition, when compared with the PWM, the proposed HM demonstrates notable efficiency improvements within the 10%–60% power range, achieving a maximum efficiency enhancement of up to 5.5%.**

***Index Terms*— Hybrid modulation (HM), secondary-side control (SSC), wireless power transfer (WPT).**

I. Introduction

WIRELESS power transfer (WPT) enables convenient, automated, and weather-proof charging for electromobility [1]. In wireless charging of electromobility, achieving wide output power regulation is essential to accommodate considerable battery load variations during the charging process [2]. Recently, extensive work has been done to enable wide power regulation for WPT systems. These research activities are mainly carried out from two perspectives: one involves using additional dc/dc converters, while the other focuses on optimizing modulation for the inverter and rectifier.

An intuitive approach for expanding the power tuning range is to introduce extra dc/dc converters at the front- and/or back-end of the system [3]. However, the adoption of additional dc/dc converters results in extra losses, higher costs, and decreased power density [4].

Another well-known method for wide-range power regulation is to optimize modulation techniques for the inverter and rectifier, where the phase shift modulation (PSM), also known as pulsewidth modulation (PWM), is the most commonly used one. Nevertheless, the PWM results in hard switching under load variations [5]. To address this issue, a triple-phase shift (TPS) control was proposed in [6], where the phase difference between the primary and secondary ac voltages is adjusted to realize wide-range zero-voltage switching (ZVS). The cost of this method is that considerable reactive power is introduced in the resonant circuits, resulting in a significant efficiency drop under light loads. Based on TPS control, the half-bridge (HB) mode was further introduced to improve the light-load efficiency [7], [8]. However, due to the limited regulation range of the HB mode, the reactive power is still notable at some power points. In addition, implementation of the HB mode results in the dc blocking voltage across the compensation capacitors, thereby increasing their voltage stresses. In addition to TPS control, other control variables can also be incorporated to realize wide ZVS. In [9], a variable-frequency-based PWM was proposed, where the switching frequency is dynamically adjusted based on load conditions. However, significant frequency deviations are observed in this method under light loads, leading to severe system detuning and considerable reactive power. Moreover, it is noteworthy that the process of varying frequency is susceptible to the bifurcation phenomenon [10], [11]. In [12], a switched-controlled capacitor (SCC) was introduced into the PWM to implement wide ZVS. Nevertheless, this approach still exhibits remarkable reactive power under light loads. In addition, the implementation of SCC results in increased power losses and component costs.

Recently, pulse density modulation (PDM) has been extensively investigated for the power regulation in WPT

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systems [13], [14], [15], [16], [17], [18], [19], [20]. In [13], PDM was adopted for the HB converters to achieve output power regulation and efficiency optimization. Furthermore, the application of PDM was extended to the FB converters in [14]. In addition, in [15], the PDM technique was applied to a semi-active rectifier (SAR). However, the conventional PDM in [13], [14], and [15] results in significant current distortions and output voltage ripple. To deal with this issue, several improved PDM (iPDM) techniques were proposed. Sheng and Shi [16] proposed an iPDM technique using harmonic analysis. Moreover, Wu et al. presented an iPDM method in [17] based on efficiency analysis and iterative calculation. However, the harmonic analysis in [16] is complicated, while the iterative calculation in [17] requires substantial computational effort. On the other hand, in [18] and [19], the semi-active mode was introduced to optimize the pulse distribution within the iPDM methods. Through evenly distributing the active and semi-active modes, the current and voltage ripples are reduced in [18] and [19]. Although the existing iPDMs effectively mitigate current distortions and output voltage ripple compared with the conventional PDM, notable current and voltage ripples still exist due to irregular pulse distributions. Moreover, it is challenging to achieve continuous tuning in iPDMs as there are a tremendous number of densities that should be optimized in continuous PDM. Consequently, the tuning resolution of the existing iPDMs is limited. In [20], a conditional PDM strategy was proposed to achieve ripple reduction. However, it requires real-time detection of high-frequency coil currents, which notably increases the hardware complexity.

In addition to the PWM and PDM techniques, pulse frequency modulation (PFM) [21], [22] and on–off keying (OOK) modulation [23] have been applied in WPT systems for power regulation. Nonetheless, the PFM also leads to notable current distortions and output voltage ripple, while the OOK results in significant surge currents during the on–off transients and large output voltage ripple due to the long duration of the "OFF" state.

Apart from wide output regulation, another challenge in WPT systems is the implementation of wireless communication. In WPT systems, the primary-side converters cannot acquire load information through a wired feedback system. Consequently, wireless communication is commonly adopted. Nevertheless, the implementation of wireless communication encounters the challenges of communication latency and potential data loss. Therefore, it is preferable to eliminate the wireless communication link in WPT systems [19]. Implementing secondary-side control (SSC) is an effective method to eliminate wireless communication, and this control can be achieved based on an active rectifier. However, since only one active power conversion stage, i.e., the rectifier, is adopted for wide power tuning, the rectifier modulation ratio needs to be adjusted in a large range. As the modulation ratio decreases, the PWM results in considerable reactive power and decreased efficiency, while the PDMs lead to significant output voltage ripple and current distortions.

To enable efficient, communication-less, and wide-range power regulation for WPT systems, this article proposes a hybrid modulation-based SSC (HM-SSC) approach. In the proposed HM, the PWM and the optimal discrete PDM (D-PDM) are integrated to regulate the output power in a broad range. The concept of integrating PWM and optimal D-PDM for wide output tuning in WPT systems, to the best of our knowledge, has not yet been reported in previous studies. Moreover, the main contributions of the proposed HM-SSC method are summarized as follows.

1) The proposed HM-SSC scheme enables communication-less wide output regulation without introducing extra components and dc/dc converters.
2) An optimal D-PDM strategy is proposed. By symmetrically and uniformly distributing pulses, the proposed optimal D-PDM eliminates even-subharmonics in the voltage, thereby significantly reducing current distortions and output voltage ripple. Moreover, the symmetrical pulse distribution eliminates the capacitor dc blocking voltages, thus minimizing the capacitor voltage stresses.
3) An HM technique, which integrates PWM and optimal D-PDM, is further proposed. Compared with the existing PDMs, the proposed HM facilitates continuous tuning by introducing the pulsewidth regulation, while minimizing the voltage and current ripples through optimized discrete pulse distributions. On the other hand, when compared with the PWM, the proposed HM diminishes rectifier switching times and minimizes the reactive power under load variations, thereby achieving a notable efficiency enhancement across a broad power range.

The remainder of this article is outlined as follows. Section II illustrates typical modulation techniques for secondary-side controlled WPT systems. Subsequently, the proposed HM-SSC method is elaborated in Section III, while experimental results are shown in Section IV. Finally, Section V demonstrates the conclusions.

II. Typical Modulation Techniques for Secondary-Side Controlled WPT Systems

Fig. 1 presents the circuit diagram of the investigated active-rectifier-based WPT system. Within Fig. 1, the dc input and output voltages are denoted by U_{in} and U_{out}, while the dc output current is indicated by I_{out}. Moreover, v_{ab} and v_{cd} are the ac voltages of the inverter and rectifier; i_P and i_S are the primary and secondary coil currents; L_P and L_S are the self-inductances of the primary and secondary coils, while M indicates their mutual inductance; C_P and C_S are the compensation capacitors; R_P and R_S are the equivalent loss resistances; and R_L is the equivalent load resistance.

Based on the fundamental harmonic approximation (FHA) method, the ac equivalent model of the system is demonstrated in Fig. 2(a), where $\dot{V}_P$, $\dot{V}_S$, $\dot{I}_P$, and $\dot{I}_S$ represent the phasor forms of the fundamental components in v_{ab}, v_{cd}, i_P, and i_S, respectively. Based on the ac equivalent model shown in Fig. 2(a), basic circuit equations of the system are given by

$$\begin{cases} \dot{V}_P = (R_P + jX_P)\dot{I}_P - j\omega_s M\dot{I}_S \\ \dot{V}_S = j\omega_s M\dot{I}_P - (R_S + jX_S)\dot{I}_S \end{cases} \tag{1}$$

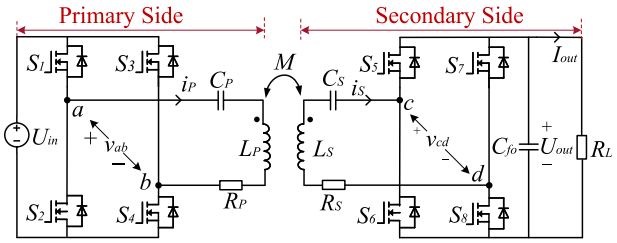


Fig. 1. Circuit diagram of the active-rectifier-based WPT system.

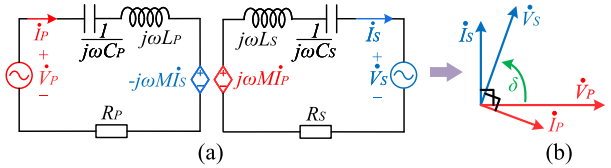


Fig. 2. (a) Equivalent circuit model and (b) phase diagram of the system based on the FHA method.

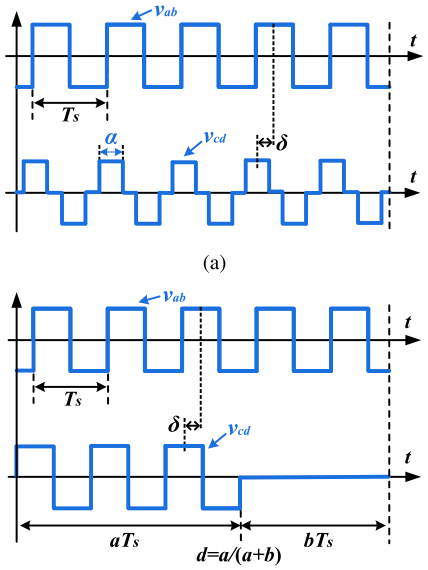


Fig. 3. Illustration of typical modulation techniques for secondary-side controlled WPT systems. (a) PWM technique, where α ($\alpha \in [0, \pi]$) indicates the pulsewidth angle of v_{cd}. (b) PDM technique, where aT_s and bT_s denote the time durations of pulse and nonpulse periods within v_{cd}, respectively, and d ($d \in [0, 1]$) represents the pulse density of v_{cd}. Here, T_s denotes the switching cycle, while δ ($\delta \in [0, \pi/2]$) is the phase difference between v_{ab} and v_{cd}.

where $X_P = \omega_s L_P - 1/(\omega_s C_P)$; $X_S = \omega_s L_S - 1/(\omega_s C_S)$; and ω_s is the switching frequency.

There are two prevalent modulation techniques for output power regulation in WPT systems. Fig. 3(a) demonstrates typical operating waveforms of the secondary-side controlled WPT systems using the PWM method. As illustrated in Fig. 3(a), in the secondary-side controlled WPT systems, the inverter output voltage is a full-duty-cycle square wave. Based on the FHA method, the rms value of $\dot{V}_P$ is given by

$$|\dot{V}_P| = 2\sqrt{2}U_{\text{in}}/\pi. \tag{2}$$

Moreover, the rms value of $\dot{V}_S$ under the PWM is derived as

$$|\dot{V}_S| = 2\sqrt{2}U_{\text{out}}/\pi \times \sin(\alpha/2) \tag{3}$$

where α is the pulsewidth angle of v_{cd}.

On the other hand, typical operating waveforms of the PDM method are demonstrated in Fig. 3(b). In this scenario, the rms value of $\dot{V}_P$ can be expressed by (2) as well. In addition, the rms value of $\dot{V}_S$ under the PDM is expressed as

$$|\dot{V}_S| = 2\sqrt{2}U_{\text{out}}/\pi \times d \tag{4}$$

where d is the pulse density of v_{cd}.

Assuming the primary and secondary resonant circuits are properly compensated and ignoring the loss resistances, the phase diagram of the system is further shown in Fig. 2(b). Moreover, the output power P_{out} of the system is derived as

$$P_{\text{out}} = \text{Re}\{\dot{V}_S \dot{I}_S^*\} = \frac{8U_{\text{in}}U_{\text{out}}}{\pi^2 \omega_s M} \times m_S \times \sin(\delta) \tag{5}$$

where δ is the phase difference between v_{ab} and v_{cd}, and m_S ($m_S \in [0, 1]$) is defined as the modulation ratio of the rectifier. Specifically, m_S corresponds to $\sin(\alpha/2)$ within the PWM, whereas it corresponds to d under the PDM.

In the secondary-side controlled WPT systems, the rectifier modulation ratio m_S is dynamically adjusted between 0 and 1 for output power regulation. Since the inverter does not actively participate in the power tuning, the SSC imposes greater demands on the rectifier modulation range. Nevertheless, as the value of m_S decreases, the conventional PWM results in remarkable reactive power for ZVS, while the existing PDMs lead to significant current distortions and output voltage ripple.

III. Proposed HM-SSC

To address the above-mentioned challenge, this article proposes an HM-SSC approach for wide power regulation in WPT systems. To enable a broad rectifier modulation range, a HM technique, which integrates PWM and optimal D-PDM, is introduced. Moreover, an optimal ZVS trajectory under the HM is established. Consequently, wide ZVS is achieved with minimal reactive power. The implementation details of the proposed HM-SSC method are elaborated as follows.

A. Existing PDMs

To regulate the output power in the secondary-side controlled WPT systems, the conventional PDM adjusts the pulse density of the rectifier input voltage (v_{cd}). Fig. 4 illustrates typical operating waveforms of the conventional PDM. Here, T_s indicates the switching cycle, while T_{PDM} represents the PDM control cycle. As shown in Fig. 4, there are two operating modes in the conventional PDM, i.e., the active and passive modes. With N_A and N_P representing the number of active and passive modes in one PDM cycle, the pulse density of v_{cd} is given by

$$d = \frac{N_A}{N_A + N_P} = \frac{N_A}{N} \tag{6}$$

where $N = N_A + N_P$ is the total number of T_s in one PDM cycle ($T_{\text{PDM}} = NT_s$). As evident from (4) to (6), power regulation of the system can be achieved by tuning the value of d in the conventional PDM. However, in this method, the number of passive modes N_P increases as the

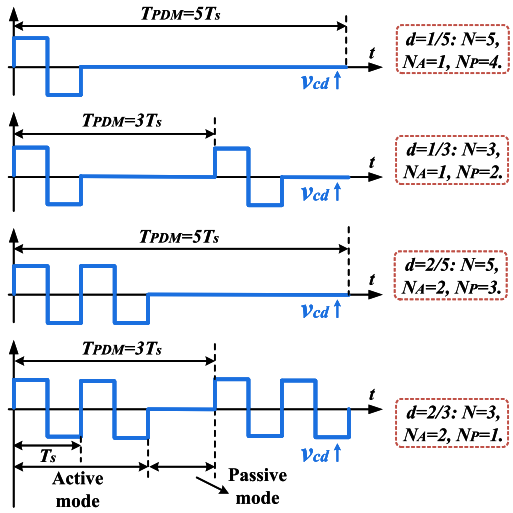


Fig. 4. Typical operating waveforms of v_{cd} when using the conventional PDM for the secondary-side controlled WPT systems.

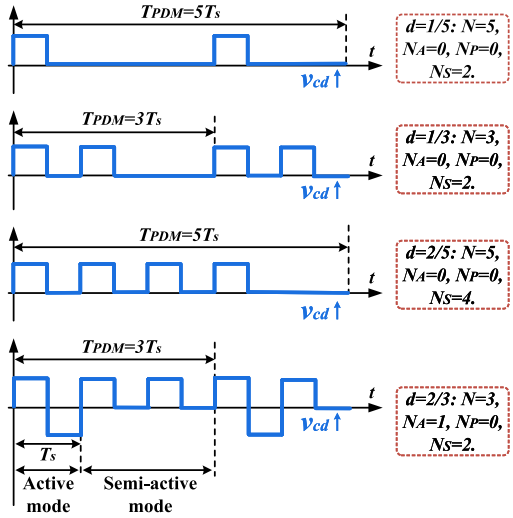


Fig. 5. Typical operating waveforms of v_{cd} when using the iPDM for the secondary-side controlled WPT systems.

value of d decreases, resulting in a long duration time of passive modes. Consequently, significant output voltage ripple and current distortions occur in the conventional PDM under light loads.

To mitigate the voltage and current ripples, the semi-active mode was introduced into the PDM, which is known as iPDM [18], [19]. Fig. 5 demonstrates typical operating waveforms of the iPDM. As shown in Fig. 5, by evenly distributing three operating modes, i.e., the active, semi-active, and passive modes, within a PDM cycle, the iPDM lowers the time duration of passive modes, thereby decreasing the voltage and current ripples. In the iPDM, the pulse density d of v_{cd} is

$$d = \frac{2N_A + N_S}{2N} \tag{7}$$

where N_S is the number of semi-active modes in a PDM cycle.

B. Proposed Optimal D-PDM

Although the iPDM reduces the voltage and current ripples by introducing the semi-active mode, it leads to the

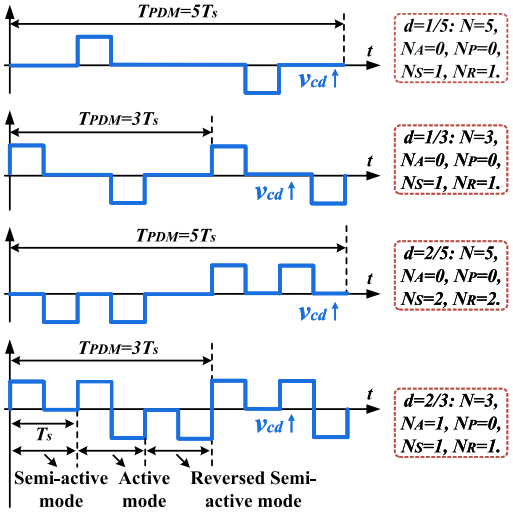


Fig. 6. Typical operating waveforms of v_{cd} when using the proposed optimal D-PDM for the secondary-side controlled WPT systems.

dc component and even-subharmonics in the voltage. The dc blocking voltage across the capacitors enlarges their voltage stresses, while the even-subharmonics exacerbate the current distortions and output voltage ripple. To minimize subharmonics in the currents and remove the capacitor dc blocking voltage, this article introduces the reversed semi-active mode into the iPDM. Since only optimal discrete pulse densities are considered, this method is also called optimal D-PDM. The basic principle of the optimal D-PDM is to evenly distribute four different operating modes, i.e., the active, semi-active, reversed semi-mode, and passive modes, in a PDM cycle, as demonstrated in Fig. 6. The key guidelines for designing the proposed optimal D-PDM are as follows.

First, to remove the dc component and even-subharmonics in the voltage, the semi-active and reversed semi-active modes should be symmetrically distributed, and the numbers of these two modes in one PDM cycle need to be identical. Hence, the pulse density d of v_{cd} under the proposed optimal D-PDM is derived as

$$d = \frac{2N_A + N_S + N_R}{2N} = \frac{N_A + N_S}{N}, \quad N_S = N_R \tag{8}$$

where N_R denotes the number of reversed semi-active modes in one PDM cycle.

Second, the total number of T_s in one PDM cycle, i.e., N, needs to be an odd number. According to the Fourier series expansion, the time-domain expression of $v_{cd}(t)$ under the proposed optimal D-PDM is derived as

$$v_{cd}(t) = \sum_k a_k \sin\left(\frac{k}{N}\omega_s t + \varphi_k\right), \quad k = 1, 3, 5, \ldots \tag{9}$$

where a_k and φ_k represent the amplitude and phase of the kth-order subharmonic, respectively, and ω_s is the resonant switching frequency. Due to the symmetrical pulse distribution, the even-subharmonics in v_{cd} are canceled, and k is any positive odd number. To excite the series–series (SS) compensated resonant circuits, the fundamental component at the resonant frequency is essential. As evident from (9), to obtain

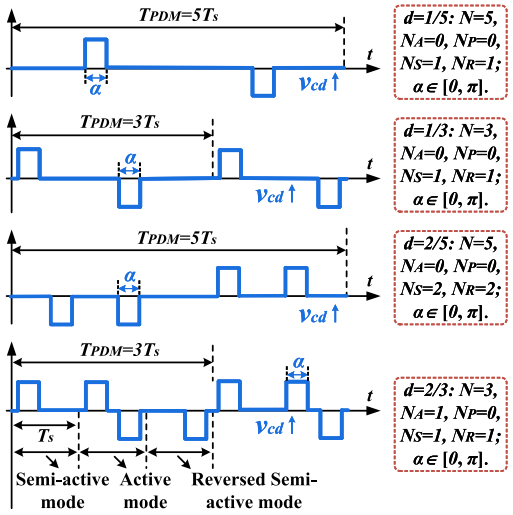


Fig. 7. Typical operating waveforms of v_{cd} when using the proposed HM for the secondary-side controlled WPT systems. Here, α ($\alpha \in [0, \pi]$) is the pulsewidth angle of v_{cd}, while d ($d \in [0, 1]$) is the pulse density of v_{cd}.

the fundamental component at the resonant frequency, there should be a value of k that is exactly equal to N. Since k is odd, N should also be an odd number accordingly.

Third, it is recommended to design N as small as possible to minimize subharmonics near the resonant frequency. According to (9), as the value of N rises, the subharmonics near the resonant frequency are increased accordingly. Considering the bandpass filtering characteristics of the SS compensation network, the voltage subharmonics near the resonant frequency cannot be effectively attenuated. Therefore, as shown in Fig. 6, N is selected as 3 or 5 in the proposed optimal D-PDM for minimizing subharmonics near the resonant frequency.

C. Proposed HM

Based on the above analysis, there is a common issue for the PDMs. As evident from (6) to (8), the minimum tuning step $d_{\min}$ for the conventional PDM and the optimal D-PDM is $1/N$, while it is $1/(2N)$ for the iPDM. As the value of N increases, the pulse density modulated rectifier is able to achieve a wider modulation range and finer tuning resolution. Nevertheless, a higher value of N results in increased subharmonics in the voltage. As the subharmonics around the resonant frequency cannot be effectively attenuated, this further leads to significant distortions in the currents.

To address this issue, an HM technique, which combines the PWM and the optimal D-PDM, is proposed, as shown in Fig. 7. Based on the optimal D-PDM, the proposed HM further adjusts the pulsewidth to achieve output regulation. As demonstrated in Fig. 7, the width of each pulse is identical, and it is represented by the pulsewidth angle α ($\alpha \in [0, \pi]$). The corresponding time duration of each pulse is given by $\alpha T_s/(2\pi)$. According to the Fourier series expansion, the rms value of $\dot{V}_S$ under the proposed HM is derived as

$$|\dot{V}_S| = 2\sqrt{2}U_{\text{out}}/\pi \times d \times \sin(\alpha/2). \tag{10}$$

As shown in (10), the rectifier modulation ratio m_S can be regulated by varying the pulse density d ($d \in [0, 1]$) and the pulsewidth angle α simultaneously. In this article, to achieve precise and wide-range power regulation with minimized subharmonics, the optimal d is selected as 1, 2/3, 2/5, 1/3, and 1/5, while α is adjusted between 0 and π.

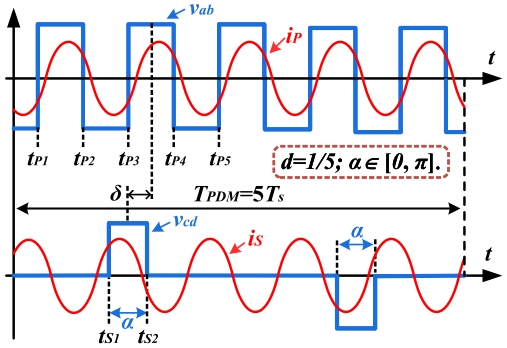


Fig. 8. Implementation of ZVS when the pulse density d of the rectifier input voltage v_{cd} is configured as 0.2.

D. Optimal ZVS Trajectory Under HM

In WPT systems, the ZVS of the power switches is of great importance. According to the analysis in [7], ZVS can be achieved by tuning the phase difference angle δ ($\delta \in [0, \pi/2]$). Specifically, as the output power decreases, the pulsewidth angle α diminishes to obtain the required power, and δ can be decreased accordingly to enable ZVS. By reducing δ from $\pi/2$, more reactive power is introduced into the resonant circuits, facilitating ZVS for both the inverter and rectifier. To minimize the reactive power, the optimal relationship between α and δ should be derived under varying power levels. Moreover, as the proposed HM technique introduces subharmonics into the coil currents, it is important to consider the subharmonics when deriving the optimal ZVS trajectory. The detailed derivation of the optimal ZVS trajectory under the proposed HM is elaborated as follows.

Based on the analysis in [6], to guarantee ZVS, a sufficient ZVS current is required to charge or discharge the equivalent output capacitance C_{oss} of the power switches within the dead time. Specifically, as shown in Fig. 8, when the pulse density d of the rectifier input voltage v_{cd} is configured as 0.2, the following equations should be satisfied for the inverter and rectifier ZVS:

$$\begin{cases} \min\{|i_P(t_{Pi})|\} \geq I_{\text{th}}, & i = 1, 2, 3, 4, 5 \\ \min\{|i_S(t_{Sj})|\} \geq I_{\text{th}}, & j = 1, 2 \end{cases} \tag{11}$$

where I_{th} is the threshold ZVS current to charge or discharge C_{oss}. It is noteworthy that in (11), only half of the PDM cycle needs to be considered due to symmetrical pulse distribution. Furthermore, based on (11), the critical ZVS condition for both the inverter and rectifier is obtained as

$$\min\{|i_P(t_{Pi})|, |i_S(t_{Sj})|\} = I_{\text{th}}. \tag{12}$$

To derive the above ZVS boundary accurately, subharmonics within $i_P(t)$ and $i_S(t)$ should be considered. Therefore, the harmonic-considered equivalent circuit model is established in Fig. 9. Based on the Fourier series expansion, the

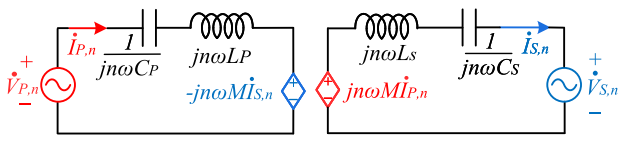


Fig. 9. Harmonic-considered equivalent circuit model.

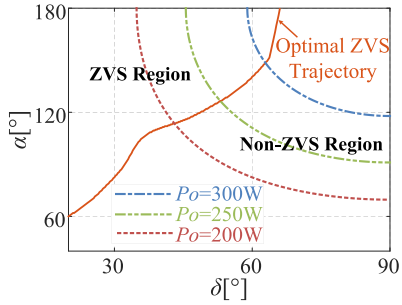


Fig. 10. Optimal ZVS trajectory and power boundary when the pulse density d of v_{cd} is set as 0.2.

time-domain expressions of $v_{ab}(t)$ and $v_{cd}(t)$ are given by

$$v_{ab}(t) = \sum_{n=1,3,\ldots} \frac{4U_{\text{in}}\sin^2(n\pi/2)}{n\pi}\sin(n\omega_s t) \tag{13}$$

$$v_{cd}(t) = \sum_{n=\frac{1}{5},\frac{3}{5},\ldots} \frac{4U_{\text{out}}\sin(n\pi/2)\sin(n\alpha/2)}{n\pi}\sin[n(\omega_s t+\delta)]. \tag{14}$$

Since the PDM control cycle is set as $T_{\text{PDM}} = 5T_s$ in the case of $d = 0.2$, subharmonic at the frequency of $\omega_s/5$ and its odd-integral multiples are considered (n is configured as 1/5, 3/5, ...), as shown in (14). Moreover, regarding $\dot{V}_{P,n}$ and $\dot{V}_{S,n}$ as two individual excitation voltage sources and applying the superposition theorem, the phasor-domain expressions of the harmonic-considered coil currents are derived as

$$\begin{cases} \dot{I}_{P\_\text{tot}} = \sum\limits_{n=\frac{1}{5},\frac{3}{5},\ldots} \dfrac{j(n-1/n)\hat{X}_S\dot{V}_{P,n} - jn\omega_s M\dot{V}_{S,n}}{n^2\omega_s^2M^2 - (n-1/n)^2\hat{X}_P\hat{X}_S} \\ \dot{I}_{S\_\text{tot}} = \sum\limits_{n=\frac{1}{5},\frac{3}{5},\ldots} \dfrac{jn\omega_s M\dot{V}_{P,n} - j(n-1/n)\hat{X}_S\dot{V}_{S,n}}{n^2\omega_s^2M^2 - (n-1/n)^2\hat{X}_P\hat{X}_S} \end{cases} \tag{15}$$

where $\hat{X}_P = \omega_s L_P = 1/(\omega_s C_P)$; $\hat{X}_S = \omega_s L_S = 1/(\omega_s C_S)$; $\dot{I}_{P\_\text{tot}}$; and $\dot{I}_{S\_\text{tot}}$ are the harmonic-considered coil currents. Combining (13)–(15), the time-domain expressions of $i_{P\_\text{tot}}(t)$ and $i_{S\_\text{tot}}(t)$ can be derived. Furthermore, substituting $i_{P\_\text{tot}}(t)$ and $i_{S\_\text{tot}}(t)$ into (12) yields the optimal ZVS trajectory, as shown in Fig. 10. In addition, the power boundary is also demonstrated in Fig. 10 based on the calculation of (5). As indicated by Fig. 10, the intersection point of the power boundary and optimal ZVS trajectory represents the optimal operating point, where the required ZVS can be achieved with minimal reactive power under this power level. In practice, to determine the optimal relationship between α and δ, a lookup table can be established and stored in the microcontrollers.

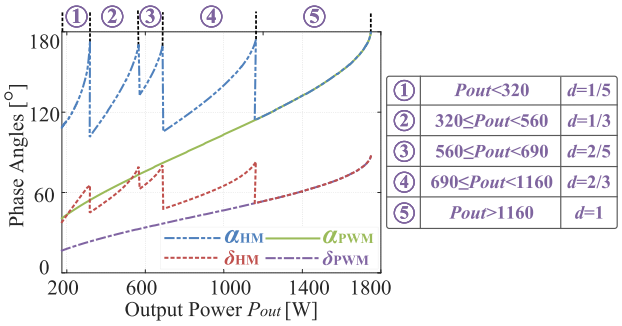


Fig. 11. Variations in δ, α, and d in the whole power range.

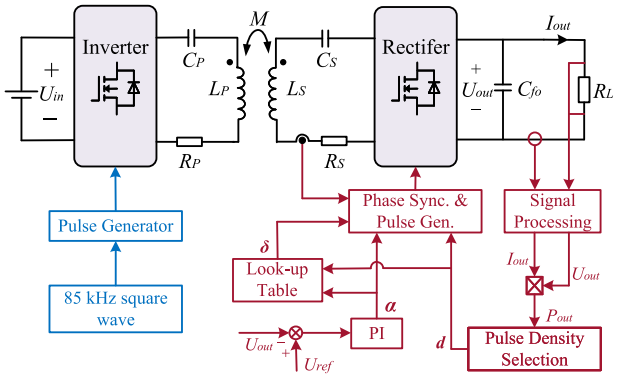


Fig. 12. Control block diagram of the proposed HM-SSC method.

The above analysis demonstrates the derivation of optimal ZVS trajectory for the case of $d = 0.2$. Similarly, the optimal $\alpha - \delta$ relationship under other discrete values of d can be obtained by following the same procedure. The variations in δ, α, and d in the whole power range are further demonstrated in Fig. 11. As illustrated in Fig. 11, the proposed HM introduces the optimal D-PDM for power regulation. As the output power decreases, the proposed HM reduces the pulse density d accordingly, thereby significantly reducing the tuning ranges of δ and α. Consequently, the value of δ in the proposed HM is significantly higher than that of the PWM across a wide power range. Based on [7], a higher value of δ results in reduced reactive power, thereby achieving improved efficiency.

E. Control Strategy

The control block diagram of the proposed HM-SSC approach is shown in Fig. 12. As illustrated in Fig. 12, the dc output voltage U_{out} and current I_{out} are first measured. By multiplying the measured U_{out} and I_{out}, the output power P_{out} is obtained. Subsequently, P_{out} is fed to the pulse density selection module to determine the optimal pulse density value d. As P_{out} decreases during the charging process, d is required to be reduced accordingly, as demonstrated in Fig. 11. Moreover, a PI controller is used for reference tracking, and the controller output is the pulsewidth angle α. Afterward, according to the optimal $\alpha - \delta$ relationship illustrated in Fig. 11, the phase angle δ is obtained by the lookup table. Finally, based on the control outputs d, α, and δ, the corresponding driving signals for the rectifier are generated by the pulse generator. On the other hand, the pulse generator of the inverter uses an 85-kHz full-duty-cycle square wave

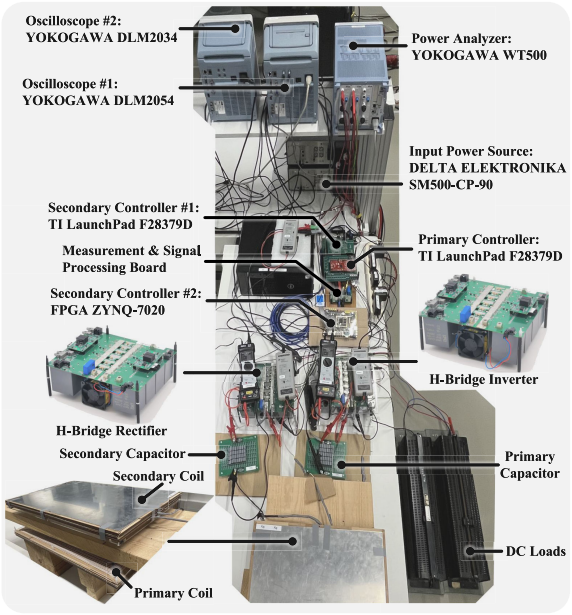


Fig. 13. Experimental prototype.

TABLE I
SYSTEM PARAMETERS OF THE INVESTIGATED WPT SYSTEM

Symbol	Parameters	Value	Unit
M	Mutual inductance	78	μH
L_P, L_S	Self-inductances	335.8, 220.0	μH
C_P, C_S	Compensation capacitances	10.6, 16.1	nF
U_{in}, U_{out}	DC input and output voltages	300, 300	V
R_P, R_S	Equivalent loss resistances	0.70, 0.46	Ω
K_p, K_i	Control gains of the PI controller	0.12, 1.00	/
f_s	Resonant switching frequency	85	kHz
P_R	Rated power	1.7	kW

as the modulation signal, and there is no need for wireless communication between the primary and secondary sides.

IV. EXPERIMENTAL RESULTS

A. Experimental Prototype

To evaluate the performance of the proposed HM-SSC method, experiments were carried out based on a WPT prototype, as illustrated in Fig. 13. Within this prototype, two H-bridge converters are used as the inverter and rectifier, respectively. The power film capacitors (KEMET R76 series capacitors) are adopted as the compensation capacitors, where the primary and secondary capacitors are configured as 5 × 8 and 4 × 10 capacitor arrays, respectively. A dc power source is used to provide the required power, while rheostats are adopted as the dc load. To compare the proposed HM with other existing modulation schemes, the HM, PWM, and iPDM methods were implemented. The control algorithm and pulse generation for the proposed HM and the conventional PWM were executed based on TI Launchpads F28379D. The iPDM, on the other hand, was implemented using a field-programmable gate array (FPGA, Xilinx ZYNQ-7020). Further details about the prototype can be found in Table I.

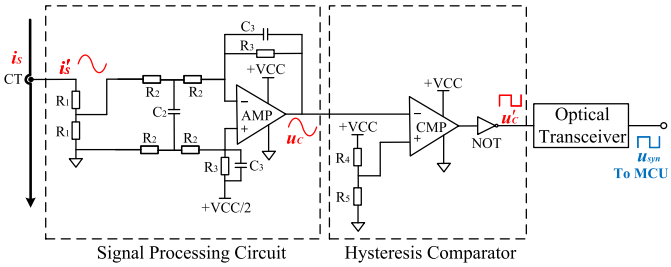


Fig. 14. Schematic of the zero-crossing-detection circuits for synchronization.

Notably, as the secondary-side control is implemented in the proposed method, synchronization between the primary and secondary driving signals is important. Within the experimental prototype, synchronization is realized by detecting the zero-crossing points of the secondary coil current (i_S). Fig. 14 demonstrates the schematic of the zero-crossing-detection circuits. As shown in Fig. 14, a current transducer (CT) is used to measure i_S. Subsequently, the output current signal of the CT is converted into a voltage signal by the signal processing circuit. To suppress the noise at the zero-crossing points, a hysteresis comparator is used. Finally, the output of the hysteresis comparator is sent to the microcontroller unit (MCU) through the optical transceiver module. It is important to note that in the proposed method, since the inverter output voltage is unchanged, the amplitude of the secondary coil current remains nearly constant despite variations in output power. This contributes to the accuracy of zero-crossing detection. However, in scenarios with significant noise disturbances or substantial variations in current amplitude, alternative synchronization techniques, such as phase-locked loop (PLL), should be considered for enhanced noise filtering and synchronization accuracy.

B. Steady-State Waveforms and ZVS Implementation

Fig. 15 demonstrates the steady-state operating waveforms of the proposed HM-SSC method. In the proposed HM-SSC method, the inverter output voltage is maintained as an 85-kHz full-duty-cycle square wave, while output regulation is accomplished through the secondary-side active rectifier. As shown in Fig. 15, both the pulsewidth (α) and density (d) of the rectifier input voltage (v_{cd}) are adjusted as the output power varies. With decreasing power, the selected pulse density diminishes accordingly. Specifically, the optimal pulse density d is configured as 1/5, 1/3, 2/5, and 2/3 when delivering 300-W, 500-W, 650-W, and 1-kW power, respectively. Meanwhile, the pulsewidth angle α is adjusted simultaneously to achieve precise power regulation.

Moreover, according to the analysis in Section III-D, the proposed HM-SSC method implements ZVS through dynamically tuning the phase difference δ. Following the analysis in [24], there are two important criteria for achieving ZVS. First, the directional requirement of the coil currents should be guaranteed. Second, the ZVS currents at the switching moments should be sufficiently large to charge or discharge the equivalent output capacitors (C_{oss}) of the power switches within the dead time. In the developed WPT prototype, the

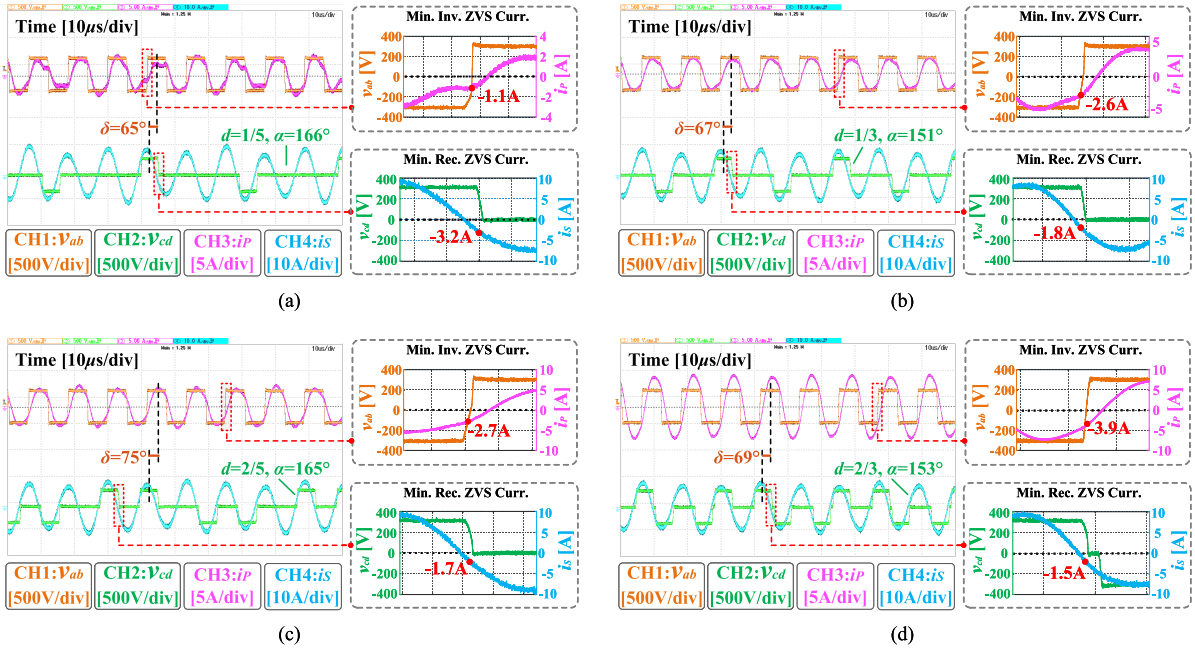


Fig. 15. Measured operating waveforms of the proposed HM-SSC method when delivering (a) 300-W power at $d = 1/5$, (b) 500-W power at $d = 1/3$, (c) 650-W power at $d = 2/5$, and (d) 1.0-kW power at $d = 2/3$. Herein, the operating waveforms at the switching moments are zoomed in, and the minimum ZVS currents for the inverter and rectifier are demonstrated.

MOSFETs IMZ120R030M1H are used as the power switches for both the inverter and rectifier. According to the datasheet of the adopted MOSFETs and considering sufficient margins, the threshold ZVS current (I_{th}) for the power switches is configured as 1.0 A in the experiments. In Fig. 15, the operating waveforms at the switching moments are zoomed in to highlight ZVS implementation, where the minimum ZVS currents for the inverter and rectifier are demonstrated. As can be observed in Fig. 15, the direction of currents at all switching moments conforms to the ZVS criteria. In addition, the minimum ZVS currents consistently exceed the threshold ZVS current (1.0 A). Consequently, by satisfying both the directional and amplitude criteria, ZVS is achieved for all power switches at different power levels. It is important to note that this article investigates ZVS analysis for steady-state operations, but this analysis is not applicable to guarantee ZVS during load transients.

Notably, due to the bandpass filtering characteristics of the SS compensated resonant tank, the harmonic components within the coil currents are considerably small at frequencies above 150 kHz. Since the noise sources of the electromagnetic interference (EMI) arise from frequencies above 150 kHz [25], the proposed method does not exacerbate the EMI issues.

C. Benchmark With Existing Modulation Schemes

To benchmark the proposed HM with other existing modulation techniques, experiments were carried out with the HM, PWM, and iPDM methods. Notably, as iPDM has demonstrated superiority over the conventional PDM in [19], only the iPDM was implemented and compared. The detailed comparisons are elaborated as follows.

1) Current Ripple: Fig. 16 illustrates the measured current ripple when delivering 40% rated power using both the proposed HM and the existing iPDM. In the iPDM, the semi-active mode is incorporated to achieve a modulation ratio of 0.4. However, this approach leads to significant current ripple, as evident in Fig. 16(a). Conversely, the proposed HM introduces both semi-active and reversed semi-active modes. Moreover, through evenly and symmetrically distributing these modes, the HM minimizes the ripple of both the primary and secondary currents, as demonstrated in Fig. 16(b).

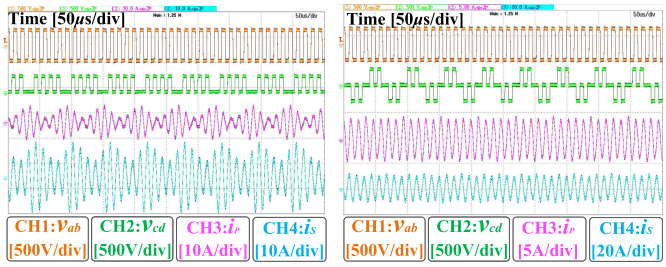


Fig. 16. Measured current ripple when delivering 40% rated power under (a) iPDM and (b) proposed HM in the experiments.

To investigate the cause of current ripple, the fast Fourier transform (FFT) analysis of the above experiments is further presented in Fig. 17. Notably, since the PDM control cycle is set as $T_{\text{PDM}} = 5T_s$ when delivering 40% rated power, the 17-kHz frequency and its integer harmonics are considered. As shown in Fig. 17, implementation of the iPDM introduces notable subharmonics near the resonant frequency (85-kHz) into v_{cd}. Due to the bandpass characteristics of SS compensation, these subharmonics cannot be effectively mitigated. Consequently, in the iPDM, significant subharmonics are observed at 68 and 102 kHz in both the primary and secondary coil currents (i_P and i_S). In contrast, through

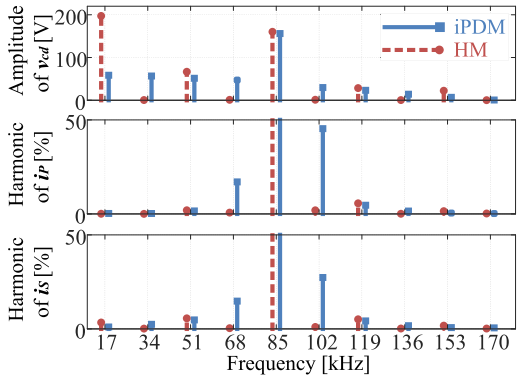


Fig. 17. FFT analysis of the measured rectifier input voltage (v_{ab}) and the coil currents (i_P and i_S) for the experiments shown in Fig. 16.

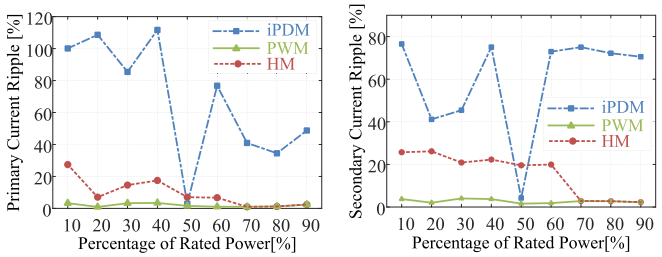


Fig. 18. Measured (a) primary current ripple and (b) secondary current ripple under different power levels and modulation schemes in the experiments. Here, the current ripple (I_{ripp}) is quantified as $I_{\text{ripp}} = [(I_{\text{peak\_max}} - I_{\text{peak\_min}})/I_{\text{peak\_avg}}] \times 100\%$, where $I_{\text{peak\_max}}$ and $I_{\text{peak\_min}}$ represent the maximum and minimum peak currents, respectively, while $I_{\text{peak\_avg}}$ indicates the average peak current within one PDM cycle. Notably, the average peak current ($I_{\text{peak\_avg}}$) can be calculated as $I_{\text{peak\_avg}} = \sqrt{2} I_{\text{rms\_avg}}$, where $I_{\text{rms\_avg}}$ is the average rms current within one PDM cycle.

symmetrically distributing the pulses, the proposed HM eliminates the even-subharmonics in v_{cd}, thereby remarkably reducing the current ripple.

In Fig. 18, a comparison of measured current ripple under various power levels in the experiments is presented. As indicated in Fig. 18, the PWM leads to minimal current ripple. Moreover, under the proposed HM, the maximum primary current ripple is 27.4%, while the maximum secondary current ripple is 26.1%. Nevertheless, in the iPDM, the primary current ripple reaches up to 111.7% at 40% rated power, while the secondary current ripple reaches 76.5% at 10% rated power. It is noteworthy that when delivering 50% rated power, the rectifier operates at HB mode in the iPDM, resulting in only integer harmonics of 85-kHz frequency in v_{cd}. This leads to decreased current ripple. However, excluding this specific power point, the current ripple of iPDM is significantly higher than that of the proposed HM.

The presence of current ripple leads to an increase in maximum current stress. As illustrated in Fig. 19, compared with the PWM, the proposed HM does not increase the maximum primary current stress, while it is increased by 26.5% in iPDM. On the other hand, the proposed HM increases the maximum secondary current stress by 13.5%, whereas this figure significantly rises to 49.1% in the iPDM.

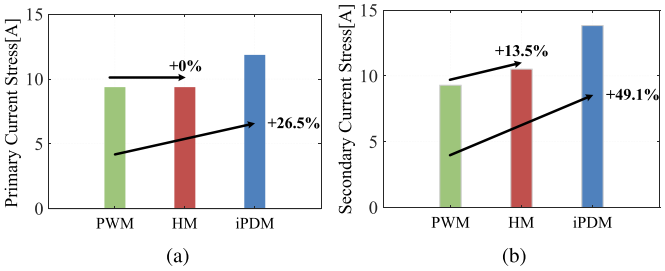


Fig. 19. Measured maximum (a) primary current stress and (b) secondary current stress under different modulation schemes in the experiments.

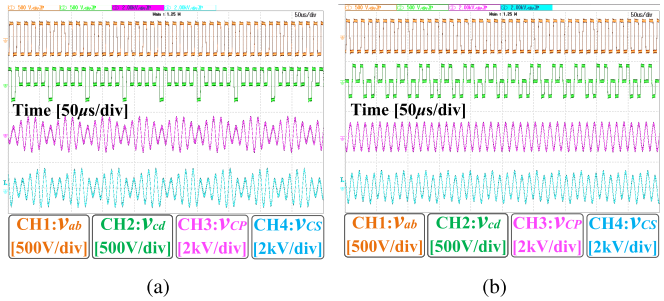


Fig. 20. Measured capacitor voltage when delivering 60% rated power under (a) iPDM and (b) proposed HM in the experiments.

2) Capacitor Voltage Stress: Fig. 20 presents the measured capacitor voltage when delivering 60% rated power. At this power level, the iPDM uses both the active and semi-active modes to obtain the required power. Conversely, the proposed HM simultaneously incorporates the active, semi-active, and reversed semi-active modes to evenly and symmetrically distribute the voltage pulses. This approach not only mitigates current ripple but also reduces capacitor voltage ripple accordingly. As depicted in Fig. 20, the capacitor voltage ripple is diminished in the proposed HM.

The reduced capacitor voltage ripple contributes to lower capacitor voltage stress. The measured capacitor voltage stress under different power levels in the experiments is shown in Fig. 21. As shown in Fig. 21(a), compared with the PWM and HM methods, the iPDM significantly increases the primary capacitor voltage stress at 90% rated power, with the primary capacitor voltage stress increased from 1764 to 2194 V. This increase is more pronounced in the secondary capacitor voltage stress, as shown in Fig. 21(b). Compared with the PWM, the iPDM substantially exacerbates the secondary capacitor voltage stress due to the capacitor voltage ripple and the dc blocking voltage. In contrast, the proposed HM eliminates the capacitor dc blocking voltage through symmetrical pulse distributions. Consequently, with reduced capacitor voltage ripple and the absence of dc blocking voltage, the secondary capacitor voltage stress in the proposed HM is markedly diminished compared with that of the iPDM.

Fig. 22 further demonstrates the measured maximum capacitor voltage stress when using different modulation techniques in the experiments. As shown in Fig. 22, the proposed HM does not increase the maximum primary capacitor voltage stress compared with the PWM, while the iPDM raises it by 19.1%. In addition, the proposed HM increases the maximum secondary capacitor voltage stress by 18.4%, whereas this number substantially rises to 53.5% within the iPDM.

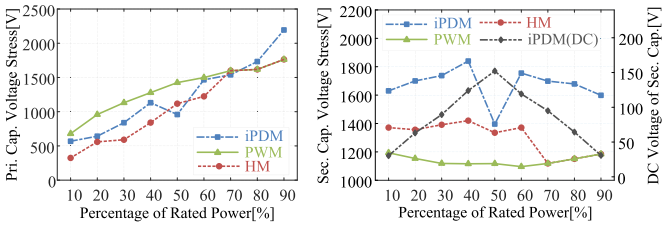


Fig. 21. Measured (a) primary capacitor voltage stress and (b) secondary capacitor voltage stress under different power levels and modulation schemes in the experiments.

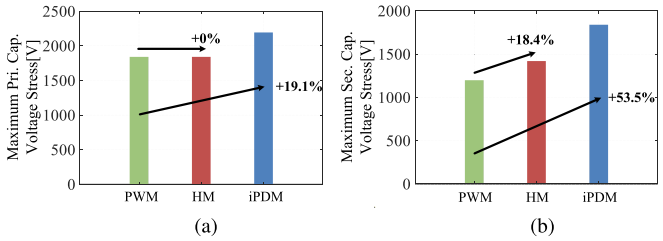


Fig. 22. Measured maximum (a) primary and (b) secondary capacitor voltage stress under different modulation schemes in the experiments.

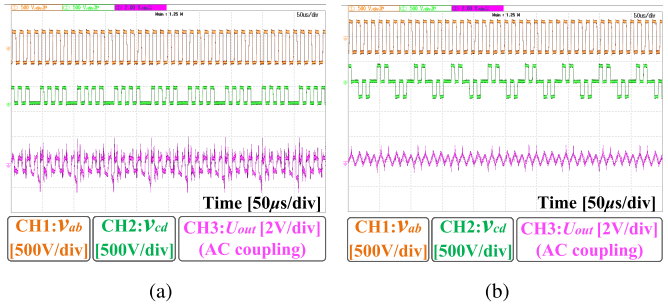


Fig. 23. Measured output voltage ripple when delivering 40% rated power under (a) iPDM and (b) proposed HM.

3) Output Voltage Ripple: Fig. 23 demonstrates the measured output voltage ripple when delivering 40% rated power under the HM and iPDM methods.

Notably, to measure the voltage ripple of U_{out} within Fig. 23, the oscilloscope channel was set to ac coupling (2 V/div). As shown in Fig. 23, the output voltage ripple of U_{out} looks distorted due to measurement noise. To mitigate measurement noise, the data measured by the voltage probe were exported from the oscilloscope and processed by the signal smoothing function in MATLAB.

As evident from Fig. 23, when compared with iPDM, the proposed HM notably diminishes the output ripple from 3.14 to 1.78 V. Moreover, the output voltage ripple under various power levels in the experiments is further presented in Fig. 24. As indicated in Fig. 24, the proposed HM increases the output ripple compared with the PWM. Nevertheless, when compared with the iPDM, the proposed HM achieves a notable reduction in the output voltage ripple.

4) Efficiency: Fig. 25 presents the measured operating waveforms and the dc-to-dc efficiency when delivering 20% rated power under different modulation techniques. Furthermore, Fig. 26 illustrates the power loss analysis for the experimental results shown in Fig. 25.

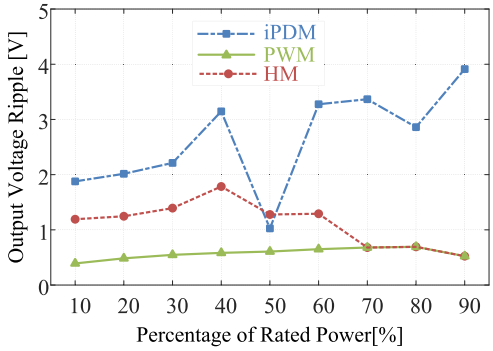


Fig. 24. Measured output voltage ripple under different power levels and modulation techniques in the experiments.

As indicated in Fig. 25(a) and (b), by satisfying the directional and amplitude requirements, ZVS is achieved in both the proposed HM and the PWM methods. However, compared with the PWM, the proposed HM method notably decreases the primary current. This reduction is attributed to the introduction of optimal D-PDM, which enables a greater value of δ and reduced reactive power under light loads. As evident from Fig. 26, the diminished primary current significantly decreases the power losses within the inverter, the primary coil, and the primary capacitor. Moreover, as shown in Fig. 25(a) and (b), the equivalent switching times of the rectifier are also reduced in the proposed HM. This, in turn, contributes to reduced rectifier switching losses, as illustrated in Fig. 26. Consequently, when compared with PWM, the proposed HM notably improves the efficiency from 87.2% to 91.4%, with the efficiency improvement up to 4.2%.

On the other hand, when comparing the proposed HM with the iPDM, as depicted in Fig. 25(a) and (c), the rms values of the currents are comparable in both the methods. Nevertheless, notable current distortions are observed in the iPDM, leading to hard switching at some switching points. As evident from Fig. 25(c), at the hard switching point-A, the flowing direction of i_P is positive at the turn-on moment of the power switches S_1 and S_4. This does not conform to the ZVS criteria, resulting in hard switching of S_1 and S_4. Similarly, at the hard switching point-B, the flowing direction of i_P is negative at the turn-on moment of the power switches S_2 and S_3. This also fails to satisfy the ZVS criteria and leads to hard switching of S_2 and S_3. As can be observed from Fig. 26, hard switching results in substantially increased losses within the power converters. Consequently, the dc-to-dc efficiency of the iPDM was only 84.2%, which is 7.2% lower than the proposed HM.

Fig. 27 further demonstrates the efficiency comparisons under various power levels in the experiments. Compared with the PWM, the proposed HM achieves remarkable efficiency improvement in the 10%–60% power range, with the maximum improvement reaching up to 5.5%. Notably, within the 70%–100% power range, the proposed HM shares the same pulse pattern as PWM, and the transmission efficiencies are identical in both the methods. For wide-range power delivery applications, the significant efficiency improvement within the 10%–60% power range is beneficial for saving energy and mitigating thermal stress.

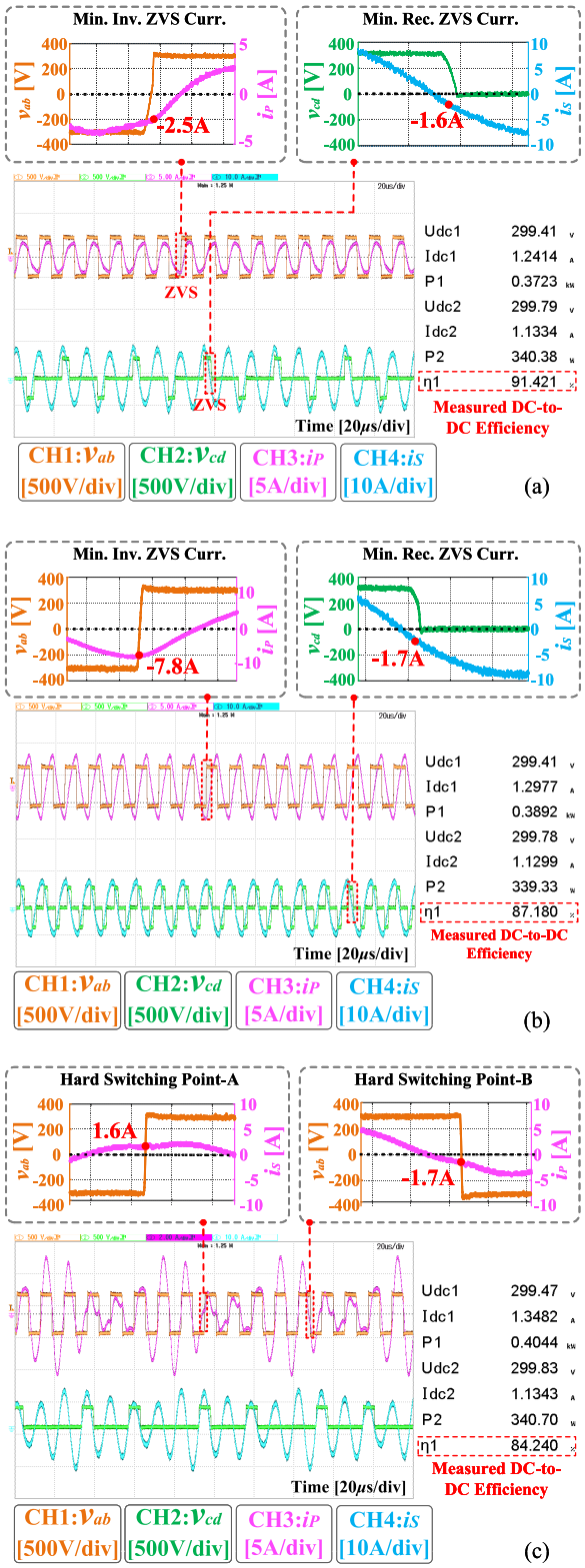


Fig. 25. Measured waveforms and dc-to-dc efficiency when delivering 20% rated power in (a) proposed HM, (b) PWM, and (c) iPDM. Herein, the operating waveforms at the switching moments are zoomed in to highlight ZVS and hard switching.

On the other hand, when compared with the iPDM method, the proposed HM method enhances efficiency at 10% (+14.6%), 20%(+7.2%), 30%(+3.6%), 40%(+1.7%), 60%(+0.9%), and 90%(+0.5%) rated power, while slightly reducing the efficiency at 50%(−0.3%), 70%(−0.5%), and 80%(−0.2%) rated power. Overall, the proposed HM excels the iPDM in terms of efficiency.

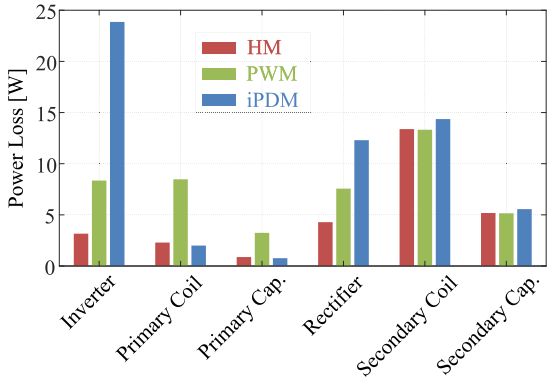


Fig. 26. Power loss analysis when delivering 20% rated power under different modulation techniques.

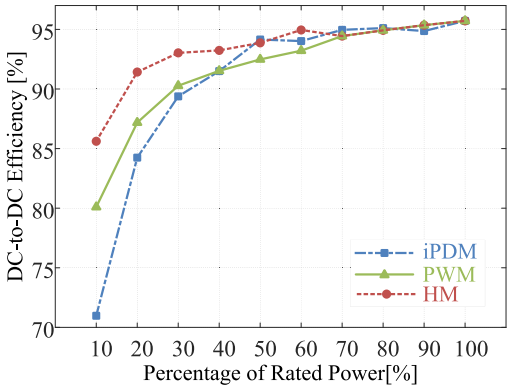


Fig. 27. Measured dc-to-dc efficiency under different power levels and modulation schemes in the experiments.

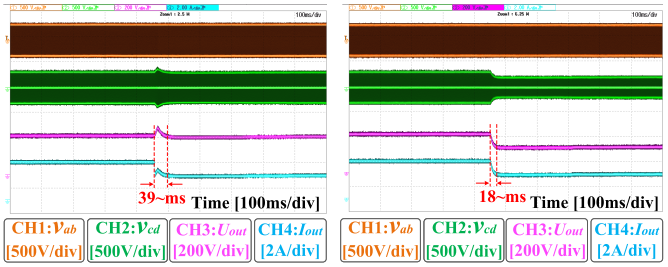
TABLE II
MINIMUM TUNING STEP OF DIFFERENT MODULATION SCHEMES

Modulation scheme	iPDM	iPDM	iPDM
Minimum tuning step	0.125 [16]	0.065 [18], [19]	0.05 [17]
Modulation scheme	PWM	Proposed HM	
Minimum tuning step	Continuous[1]	Continuous[1]	

1 The minimum tuning step of pulse width regulation is technically constrained by the ePWM clock frequency of the microcontrollers. For an 85 kHz system operating with 100 MHz ePWM clock frequency, the minimum tuning step is 0.00085. This step is significantly small, which is regarded as continuous tuning in this paper.

5) Tuning Resolution: Table II shows comparison of the minimum tuning step of different modulation methods. A smaller tuning step indicates higher tuning resolution, allowing for finer power regulation. As shown in Table II, the tuning resolution of the existing iPDMs is not continuous. This is attributed to the imperative of iPDMs to optimize pulse distribution for each density value. Enhancing tuning resolution necessitates consideration of a greater number of density values, which significantly increases the difficulty of analysis and implementation. Although the incorporation of a Delta–Sigma modulator enables continuous tuning for PDM methods [13], optimizing pulse distribution for each density is still challenging as there are a tremendous number of densities that should be considered in continuous PDM methods.

Conversely, the PWM enables continuous tuning through pulsewidth adjustment. By incorporating pulsewidth tuning



(a) (b)

Fig. 28. Dynamic performance of the proposed HM-SSC method: (a) when the load is changed from 100 to 150 Ω and (b) when the reference voltage is changed from 300 to 200 V ($R_L = 100$ Ω).

into the optimal D-PDM, the proposed HM completely leverages the advantages of the PWM in terms of continuous tuning. Since only a limited number of density values are considered, the analysis and implementation of the proposed HM method are much more straightforward than that of the iPDM.

6) Summary: After a comparative analysis of the proposed HM with the existing PWM and iPDM methods, a summary is presented as follows.

In comparison to PWM, the proposed HM leads to increased component stress and output voltage ripple. Fortunately, through optimizing pulse distributions for the adopted discrete pulse densities, this increase is effectively minimized. On the other hand, the proposed HM notably enhances efficiency across a broad power range, with a maximum efficiency improvement of up to 5.5%. This enhancement contributes to the overall efficiency improvement of the system, enabling efficient power transfer under wide load variations. In practical design, a tradeoff between efficiency improvements and increased output voltage ripple should be considered when evaluating the proposed HM against the PWM. Although applications with stringent requirements for output voltage ripple may necessitate a larger output capacitor to leverage the efficiency enhancement of the proposed method, it is important to note that for applications prioritizing energy transfer efficiency, the proposed method offers significant advantages.

When compared with the iPDM, the proposed HM achieves a substantial reduction in the component stresses and output voltage ripple. In addition, the proposed HM facilitates continuous tuning by integrating pulsewidth regulation. In terms of overall efficiency, the proposed HM outperforms the iPDM as well.

D. Transient Response

To test the dynamic capability of the proposed HM-SSC method, a signal measurement and processing system was used to sample the dc output voltage and current, while a PI controller was implemented to enable reference tracking.

Fig. 28 demonstrates the dynamic performance of the HM-SSC method. As shown in Fig. 28(a), when the load is suddenly altered from 100 to 150 Ω, the HM-SSC method restores the output voltage to 300 V within 39 ms. Furthermore, Fig. 28(b) shows that the HM-SSC approach effectively tracks the reference voltage when it is abruptly modified from 300 to 200 V, with the dynamic settling time at 18 ms.

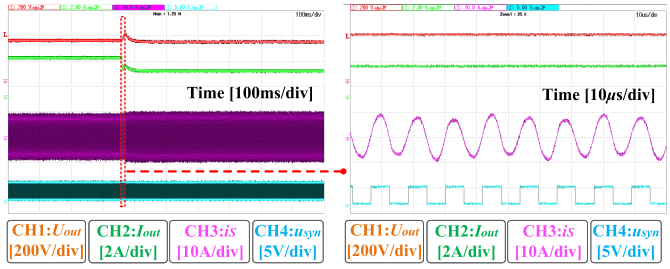
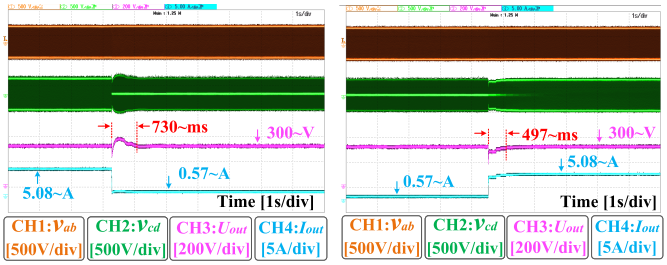


Fig. 29. Synchronization performance of the proposed method when the load is changed from 100 to 150 Ω.



(a) (b)

Fig. 30. Dynamic performance of the proposed HM-SSC method: (a) when the output power is decreased from 90% to 10% rated power and (b) when the output power is increased from 10% to 90% rated power.

Fig. 29 further illustrates the synchronization performance of the proposed method when the load is changed from 100 to 150 Ω. As shown in Fig. 29, the zero-crossing points of the secondary current (i_S) are detected, and the corresponding synchronization signal (u_{syn}) is generated. This confirms the effectiveness of the proposed method in maintaining synchronization during the transient period.

Fig. 30 illustrates the transient performance of the HM-SSC method when the system's output power is changed between 10% and 90% rated power. As shown in Fig. 30(a), when the load is suddenly changed from 59 to 530 Ω, the dc output current drops from 5.08 to 0.57 A, and the system's output power decreases from 90% to 10% rated power. The experimental results reveal that the HM-SSC method restores the dc output voltage back to 300 V within 730 ms. Similarly, as demonstrated in Fig. 30(b), when the load abruptly shifts from 530 to 59 Ω, increasing the system's output power from 10% to 90% rated power, the HM-SSC method effectively tracks the reference voltage, with the dynamic settling time at 497 ms.

E. Comparisons to Other Reported Works

Table III shows comparison of the proposed method with other existing methods. As demonstrated in Table III, when compared with [7] and [8], the proposed approach achieves minimized reactive power across wide power levels. Although the introduction of HB modes in [7] and [8] decreases the reactive power, the tuning range of the HB mode is constrained. Conversely, the proposed HM introduces optimal D-PDM, which notably decreases the reactive power across a wider power range. Furthermore, the proposed approach implements SSC for output power regulation, eliminating the need for communication links. Notably, compared with the dual-side control in [7] and [8], the SSC requires a broader modulation range for the active rectifier. In this context, the introduction

TABLE III
COMPARISONS TO OTHER REPORTED WORKS

References	[7]	[8]	[9]	[12]	[16]	[17]	[18]	[19]	This work
Rated Power	1.8 kW	10 kW	2.2 kW	1.6 kW	20 kW	1.0 kW	30 kW	1.05 kW	1.7 kW
Compensation Topology	SS	SS	LCC-S	LCC-LCC	SS	SS	SS	LCC-S	SS
Modulation Scheme	PWM	PWM	PWM	PWM	iPDM	iPDM	iPDM	iPDM	Proposed HM
No Extra SCC Circuits	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes
Bifurcation Free	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes
Minimized Reactive Power across Wide Power Levels	No	No	No	No	Yes	Yes	Yes	Yes	Yes
No Need for Communication Links	No	No	No	No	No	Yes	Yes	Yes	Yes
Continuous Power Tuning	Yes	Yes	Yes	Yes	No	No	No	No	Yes
Minimized Output Voltage Ripple and Current Distortions	Yes	Yes	Yes	Yes	No	No	No	No	Yes
Robust ZVS Operations across Wide Power Levels	Yes	Yes	Yes	Yes	No	No	No	No	Yes

Note: The shaded areas indicate the desirable performances.

of optimal D-PDM becomes exceedingly important to further minimize the reactive power at lower modulation ratios. In contrast to the HB mode, which only delivers half the output of the FB mode, the proposed optimal D-PDM method enables fractional outputs of 1/5, 1/3, 2/5, and 2/3 of the FB mode. This considerably extends the modulation range, facilitating minimized reactive power across wide power levels.

Moreover, when compared with the variable frequency-based PWM technique in [9], the proposed approach maintains constant-frequency operation, thereby avoiding the bifurcation phenomenon. In addition, compared with the SCC-based PWM approach in [12], the proposed technique presents notable advantages by eliminating the need for additional SCC circuits.

In comparison to the iPDM methods in [16], [17], [18], and [19], the proposed method demonstrates notable advantages across multiple aspects. First, the proposed optimal D-PDM evenly and symmetrically distributes voltage pulses. This eliminates the even-subharmonics in the rectifier input voltage, achieving significantly reduced current distortions and output voltage ripple. Second, since only five discrete pulse densities are considered, the optimal ZVS conditions at each pulse density can be easily investigated. By analyzing the optimal ZVS trajectory, the proposed method enables robust ZVS for all power switches throughout the entire power range. Third, by integrating pulsewidth regulation, the proposed strategy offers continuous power regulation capability for the system.

V. CONCLUSION

In this article, an HM technique is proposed to enable efficient, communication-less, and wide-range output regulation for the WPT systems. Through optimizing the pulse distributions and incorporating pulsewidth regulation, the proposed HM achieves continuous output tuning, minimized voltage and current ripples, as well as improved efficiency. The overall performance of the proposed HM is benchmarked with the existing PWM and iPDM methods in terms of current ripple, capacitor voltage stress, output voltage ripple, efficiency, and tuning resolution. The experimental results demonstrate that the proposed HM substantially reduces the component stresses and output voltage ripple while facilitating continuous tuning when compared with the iPDM. On the other hand, when compared with the PWM, the proposed HM notably enhances efficiency, enabling efficient power transfer under wide-range load conditions.

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