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Design of CMOS active pixels based on finger-shaped PPD

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Abstract: To improve the full-well capacity and linear dynamic range of CMOS image sensor, a special finger-shaped pinned photodiode (PPD) is designed. In terms of process, the first N-type ion implantation of the PPD N buried layer is extended under the transfer gate, thereby increasing the PPD capacitance. Based on TCAD simulation, the width and spacing of PPD were precisely adjusted. A high full-well capacity pixel design with a pixel size of 6×6 μm^2 is realized based on the 0.18 μm CMOS process. The simulation results indicate that the pixel with the above structure and process has a depletion depth of 2.8 μm and a charge transfer efficiency of 100%. The measurement results of the test chip show that the full-well capacity can reach 68650e$^-$. Compared with the conventional structure, the proposed PPD structure can effectively improve the full well capacity of the pixel.

Key words: CMOS active pixel; full well capacity; full depletion

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1. Introduction

As a key technology for recording image information, solid-state image sensors have received much attention. Solid-state image sensors are divided into charge coupled device (CCD) image sensors and complementary metal oxide semiconductor image sensors (CISs). Early on, CISs had problems such as high noise, low sensitivity, and severe image lag due to process level limitations, which made their application range narrower than CCD[1]. With the continuous development of CMOS technology, CIS has gradually overtaken CCD image sensor[2, 3]. At present, CISs are widely used in consumer electronics, biomedicine, security monitoring, automotive electronics, and industrial imaging due to their low power consumption, low cost, and easy integration[4–6]. However, with the growing requirements of various application, especially in the high-end imaging field, the requirements for wide dynamic range (DR) have become the main difficulties and challenges to be overcome at present[7–9].

DR is an important indicator of CIS, which reflects the range of the maximum light intensity signal and the minimum light intensity signal that CIS can detect[10]. DR can be calculated as:

$$\mathrm{DR} = 20 \lg \frac{N_{\mathrm{FWC}}}{N_{\mathrm{noise}}}, \tag{1}$$

where N_{FWC} and N_{noise} are the full well capacity (FWC) and read noise, respectively. According to Eq. (1), the FWC is one of the decisive factors in determining the CIS DR. The linear dynamic range can be further improved by increasing the FWC. The FWC can be increased by enlarging the PPD photosensitive area. However, the ratio of PN junction contact area to PPD volume in the traditional cube pinned photodiode (PPD) is relatively low, which will cause the pinned voltage V_{pin} to be relatively high. A large V_{pin} will cause incomplete transfer of photo-generated electrons in the PPD, resulting in image lag[11–13] and increasing charge transfer noise[14], which ultimately limits the expansion of the dynamic range. Therefore, a special finger-shaped PPD structure is designed in this paper to ensure a large FWC and PPD complete depletion, thereby effectively improving the linear dynamic range of the CIS. Meanwhile, to reduce the deviation between TCAD simulation results and chip measurement results, the process calibration was performed by using secondary ion mass spectroscopy (SIMS) data[15] and TCAD tools. The device simulations in this paper are based on process calibration.

2. Theory analysis of PPD design

To enhance the longitudinal electric field strength of the PPD and achieve a deeper depletion region depth, four times N-type ion implantations as shown in Fig. 1 are used to form the N buried layer of the PPD. TG and FD represent transfer gate and floating diffusion node, respectively. The four times N-type ion implantations are completed by self-alignment technology[16], and the implantation dose and implantation energy determine the charge transfer speed, charge transfer efficiency, and full well capacity in the pixel. Therefore, the optimal N-type ion implantation dose and implantation energy must be obtained through TCAD device simulation according to specific requirements and CMOS processes when designing a pixel.

For a traditional large-area cube-shaped PPD, it is difficult to achieve full depletion of the PPD region even with four times N-type ion implantations. Fig. 2 is the TCAD two-dimensional simulation result using the traditional cubic PPD structure, where the white curve is the depletion region

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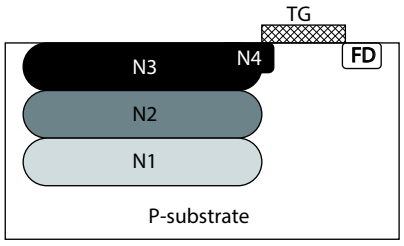

Fig. 1. N buried layer structure of PPD.

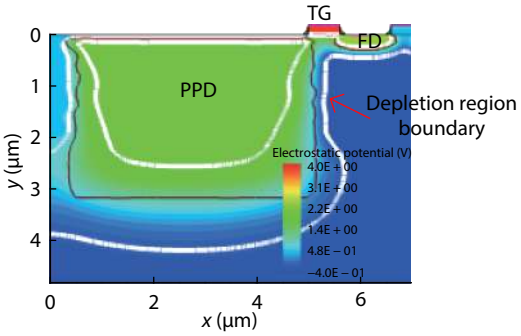

Fig. 2. (Color online) 2D TCAD simulation of depletion region in traditional cubic PPD.

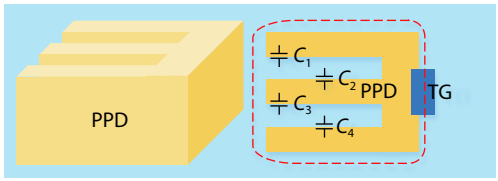

Fig. 3. (Color online) The finger-shaped PPD and its top view.

boundary. It can be seen from Fig. 2 that the central area of the PPD cannot always be fully depleted, which will cause incomplete photo-generated charges transfer and image lag. There is a certain fluctuation in the amount of charges in the undepleted region, which will deteriorate the noise performance of the CIS and eventually affect the imaging quality of the CIS.

In this paper, the finger-shaped PPD structure is used to solve the problem that the large-sized cube-shaped PPD is difficult to achieve full depletion. Fig. 3 shows the three-finger PPD structure used in this paper and its top view. The finger-shaped PPD design can increase the lateral electric field strength of the PPD, thereby ensuring the large-sized PPDs are fully depleted. Moreover, compared with the traditional cube-shaped PPD structure, this structure increases the contact area of the PN junction (including capacitors C_1, C_2, C_3, and C_4), thereby increasing the unit-area capacitance of the PPD[17, 18]. According to the expression of FWC:

$$N_{\mathrm{FWC}} = A_{\mathrm{PPD}} C_{\mathrm{PPD}} \left(V_{\mathrm{pin}} - V_{\mathrm{int}}\right)/q, \tag{2}$$

where A_{PPD} is the total area of PPD, C_{PPD} is the unit-area capacitance of PPD, V_{pin} and V_{int} are the pinned voltage of PPD and the initial voltage value when the pixel is saturated, respectively. It can be obtained from this formula that when the unit-area capacitance of the PPD increases, the full well capacity of the CMOS image sensor is increased, thereby improving the dynamic range of the CIS.

Although the TCAD 2D simulation results have certain errors with the actual chip measurement results, the corresponding trends and effects are consistent. In addition, the process calibration by SIMS can greatly improve the consistency between the simulation results and the measurement results. In this paper, a 2D simulation of the finger-shaped PPD is performed, and the following processing is performed:

a) When designing ion implantation conditions of finger-shaped PPD, the depletion region range, FWC and V_{pin} of a single-finger PPD are first confirmed. Then, the corresponding parameters of the entire finger-shaped structure are estimated.

b) When designing the width and spacing of a finger-shaped PPD, the depletion region range, FWC and V_{pin} are calculated and evaluated by two adjacent single-finger PPDs.

The following simulations and designs are based on the above simulation flow and process calibration.

3. Schematic design of the high FWC CMOS active pixel

3.1. Basic process design

After several TCAD simulation experiments, this paper pre-determined a basic version of ion implantation process conditions. The four graphs in Fig. 4 are the potential distribution diagrams of finger-shaped PPD in the initial stage, after light irradiation, during transfer, and after transfer (based on the above basic process conditions). Figs. 5(a) and 5(b) are the potential distributions during the charge transfer process and the potential curve along the charge transfer path under the basic process conditions, respectively. It can be seen that there are no potential barriers or potential wells on the charge transfer path, and the signal charges can be transferred from the PPD to the floating diffusion node (FD) without hindrance, thereby achieving the complete transfer of signal charges.

3.2. Finger-shaped PPD width simulation design

In a pixel, the pinned voltage V_{pin} of the PPD determines the ability of the PPD to store charge and the rate of charge transfer. A larger V_{pin} means a larger FWC of the PPD and a slower charge transfer rate. V_{pin} can be expressed as[19]:

$$V_{\mathrm{pin}} = \frac{qN_{\mathrm{D}}d^2}{2\varepsilon} + \frac{E_{\mathrm{g}}}{2q} - \frac{kT}{q}\ln\frac{N_{\mathrm{C}}}{N_{\mathrm{D}}}, \tag{3}$$

where N_{D} is the doping concentration of the N-type region, N_{C} is the effective state density of the conduction band, d is the depth of the PPD (the width of the short side), ε is the dielectric constant of the silicon material, E_{g} is the band gap width, k is the Boltzmann constant, and T is the absolute temperature. It can be seen from this formula that V_{pin} is mainly related to the depth of finger-shaped PPD. Therefore, based on the above-mentioned basic process conditions, this paper uses 0.1 μm as the step size to perform device simulation on different finger-shaped PPDs with widths between 0.6 and 1.0 μm. The simulation results are shown in Figs. 6(a)–6(e). Table 1 shows the V_{pin}, N_{FWC}, and depletion region depth W of PPDs with different finger widths d.

Table 1 shows that the N_{FWC} and V_{pin} of the PPD will increase as the width of finger-shaped PPD increases. Nevertheless, the design of d is not the larger the better. Because, the depletion width of PPD is:

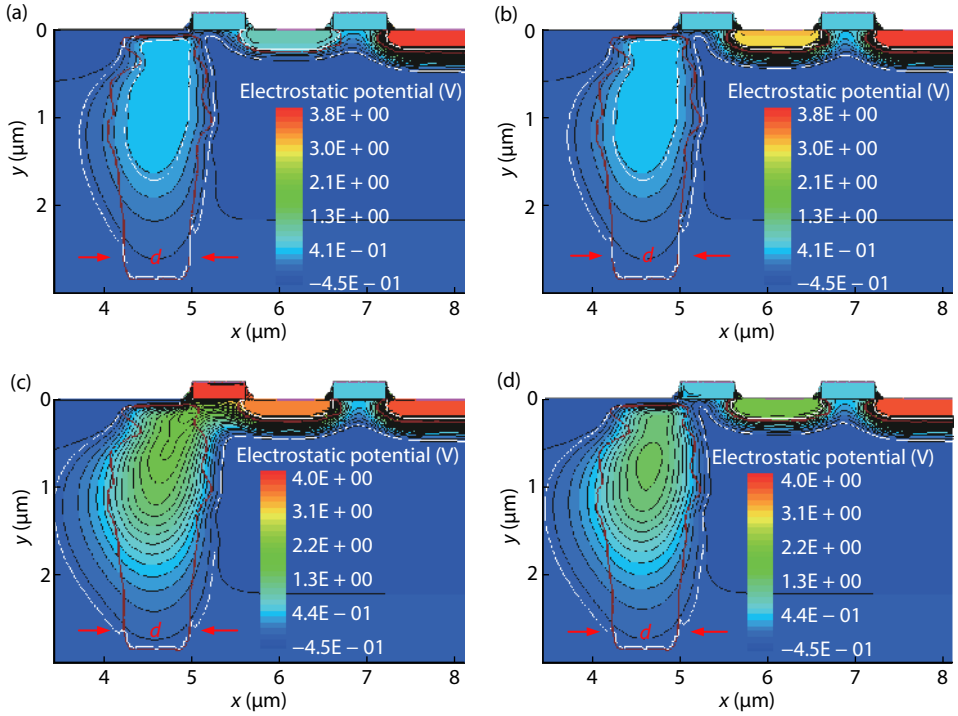

Fig. 4. (Color online) Under the basic ion implantation process conditions, the potential distribution in (a) initial phase, (b) after illumination phase, (c) transfer phase, (d) post-transition phase.

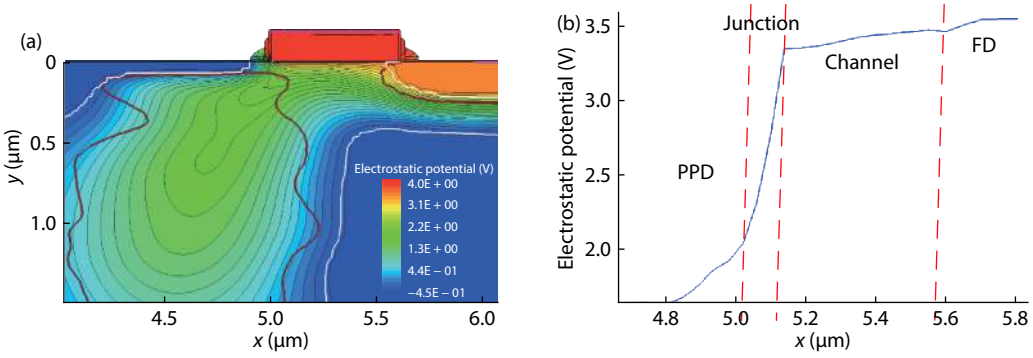

Fig. 5. (Color online) Under the basic ion implantation process conditions: (a) the potential distribution in transfer phase, (b) the potential curve on the charge transfer path.

$$W_{\text{dep}} = \sqrt{\frac{2\varepsilon_r\varepsilon_0 (N_A + N_D)(V_b - V_s)}{qN_AN_D}}, \tag{4}$$

where ε_r and ε_0 are the relative dielectric constant of silicon and vacuum dielectric constant, N_A is the doping concentration of the P-type region, V_b is the built-in potential in the PPD equilibrium state, and V_S is the external voltage. This formula shows that the depletion region width of PPD is mainly related to the doping concentration of PPD and the applied bias voltage. Therefore, increasing d without changing V_S, N_A, and N_D will affect the depletion state of PPD. When $d > W_{\text{dep}}$, PPD will not be fully depleted, resulting in image lag. Thus, the design value of d must be selected in a compromise. Fig. 6(f) shows the potential distribution of PPD under different d. The simulation results indicate that the potential barrier and potential well on the PPD charge transfer path are relatively small when d is 0.8 μm (within the range where the electron thermal motion can pass). Therefore, 0.8 μm is the optimal choice for the finger-shaped PPD width.

Fig. 7 shows the change in the number of electrons in the PPD (in Fig. 6(c)) over time. As can be seen from the figure, the number of electrons in PPD when saturated is:

$$\begin{aligned} N_{\text{PPD}} &= \text{eDensity}\left(\mu\text{m}^2/\text{cm}^3\right) \times W\,(\mu\text{m}) \times 10^{-12} \\ &= 6.3857 \times 10^{15} \times 1 \times 10^{-12} \approx 6385, \end{aligned} \tag{5}$$

where eDensity is the number of electrons in the PPD obtained by TCAD 2D simulation, and W is the width of the PPD. Similarly, the number of electrons in the PPD after the charge transfer can be calculated to be zero. Therefore, the charge transfer efficiency of PPD is [(6385 – 0) / 6385] × 100% = 100%.

3.3. The simulation design of PPD finger spacing

Similar to the design of the finger-shaped PPD width, the design of the PPD spacing also needs to be compromised.

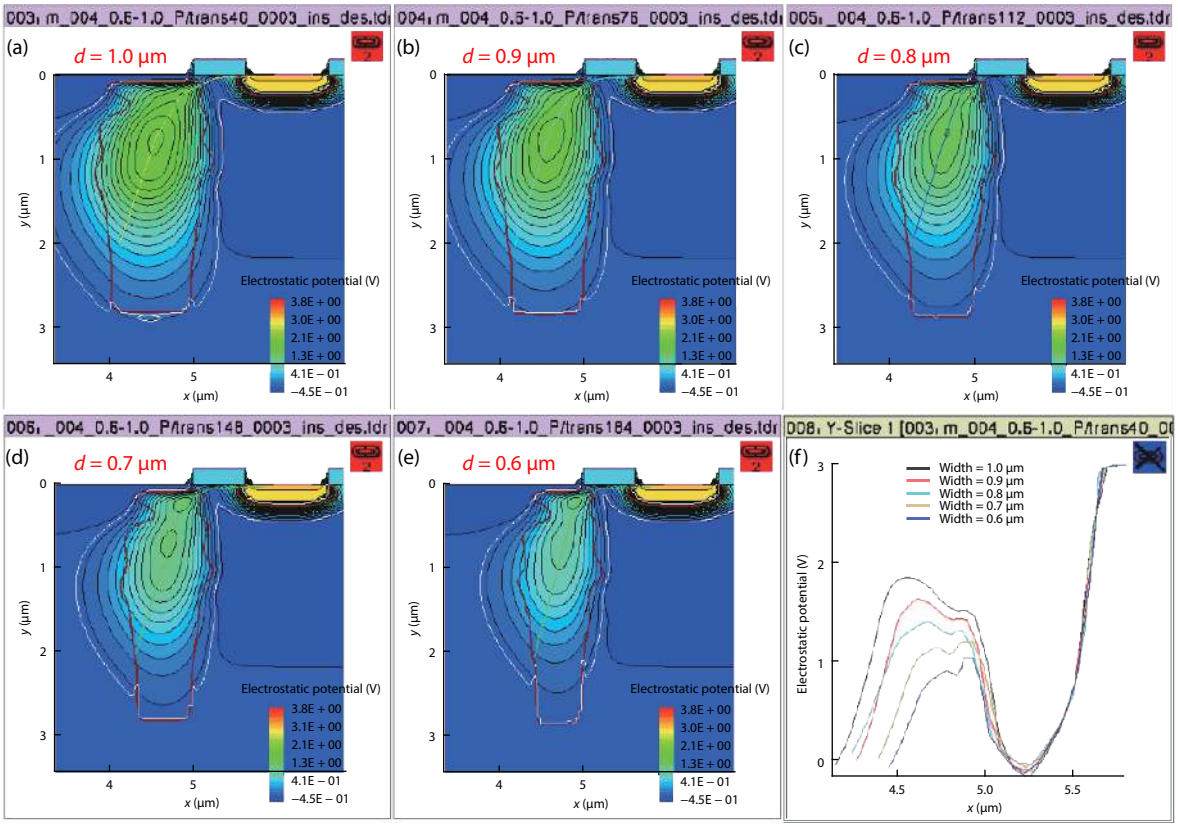

Fig. 6. (Color online) Potential and depletion region distribution with different single-finger PPD widths.

Table 1. V_{pin}, N_{FWC} and depletion depth (W) with different d.

d (μm)	0.6	0.7	0.8	0.9	1.0
V_{pin} (V)	1.057	1.215	1.408	1.646	1.863
N_{FWC} (e^-)	3094	4335	5516	6725	7966
W (μm)	2.842	2.792	2.845	2.845	2.845

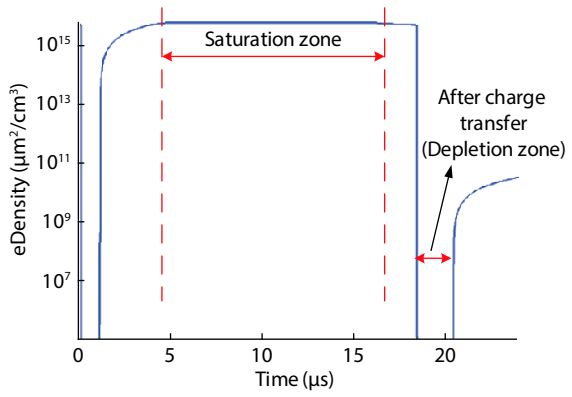

Fig. 7. (Color online) The number of electrons in PPD based on TCAD 2D simulation.

Based on the PPD width of 0.8 μm and the step size of 0.1 μm, the simulation results were obtained when the PPD spacing is 0.9–1.4 μm. Fig. 8 shows the depletion region zone and potential distribution after charge transfer at different spacings.

The simulation diagrams indicate that the smaller the PPD spacing, the more complete the depletion zone of the adjacent single-finger PPD. However, if the spacing is too small, then the overall doping concentration of the PPD will be higher, which will cause the V_{pin} to be higher. When $V_{pin} \geqslant V_{resert} - V_{drop}$, it will seriously affect the signal charge transfer speed, and even lead to partial depletion of PPD. V_{resert} is the reset level of the FD, V_{drop} is the voltage drop of the FD after the signal charge is completely transferred from the PPD to the FD. Table 2 extracts the V_{pin} results under the above-mentioned different PPD spacing. When the spacing is less than 1.1 μm, V_{pin} will increase significantly. The PPD will not be fully depleted when it is smaller than 0.9 μm, which is consistent with the above analysis. Hence, it is necessary to compromise to select the size of the PPD when designing the PPD, that is, to ensure that the PPD spacing is about 1.1 μm.

Figs. 9(a) and 9(b) show the changes in the number of electrons in the PPD over time before and after pixel optimization, respectively. These two pictures were obtained under the same simulation conditions. From Fig. 9(a), the number of electrons before and after charge transfer in PPD is 60912 and 14427, respectively. In other words, the charge transfer efficiency of the cubic PPD is 76.315%. From Fig. 9(b), the number of electrons before and after charge transfer in PPD is 15901 and 0, respectively. Hence, the proposed pixel structure can achieve a good charge transfer efficiency, that is, a charge transfer efficiency of 100%.

3.4. Further optimization of FWC

To further improve the pixel full well capacity, this paper proposes a PPD structure as shown in Fig. 10. Fig. 10(b) is a sectional structural view of the PPD taken along the AA' direction in Fig. 10(a). Fig. 10(c) is a TCAD device simulation diagram corresponding to Fig. 10(b). Except that the implanta-

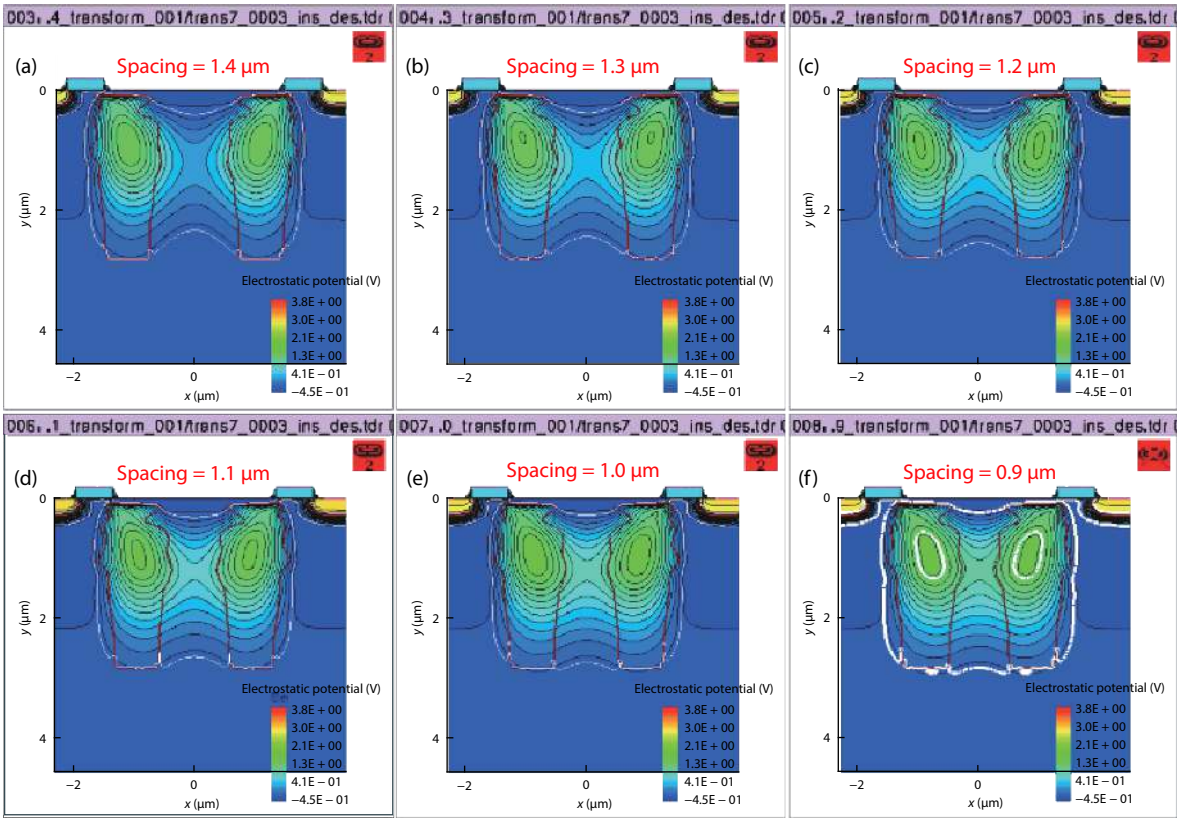

Fig. 8. (Color online) Depletion zone and potential distribution with different PPD spacing.

Table 2. V_{pin} with different PPD spacing.

Spacing (μm)	1.4	1.3	1.2	1.1	1.0	0.9
V_{pin} (V)	1.382	1.415	1.424	1.438	1.506	Not fully depleted

tion zone of the first N-type ion implantation N1 is extended to the right, the remaining process conditions are the same as the foregoing. Compared with before the improvement, this structure not only increased the capacitance value of the PPD, but also collected photons incident at a certain angle into the PPD, thereby greatly improving the full well capacity of the pixel.

4. Measurement results and analysis

In this paper, a front-illuminated CIS made in 0.18 μm CMOS process is designed and measured. The pixel design of this CIS uses the process parameters obtained through the TCAD device simulation described above. Based on the limitation of the pixel size and the area consumption of other transistors in the pixel, the final designed photodiode area is 4.6 × 4.6 μm^2, the gate length of the transfer transistor is 0.6 μm, the single-finger PPD width is 0.8 μm and the spacing is 1.1 μm. To further improve the signal-to-noise ratio of CIS, binning technology is used in this paper to realize the accumulation of the output signals of two pixels. At the same time, so as to ensure the uniformity of the pixel array in the CIS, a 2 × 2 pixel unit is finally designed as shown in Fig. 11(a). As shown in Fig. 11(b), the structure diagram of PPD, transmission gate (TG), and FD in one pixel is shown.

With a gain of 1.125 times and an exposure time of 124.6 ms, the output of the test chip under uniform illumination with different irradiances was measured in this paper. The measurement data was processed and analyzed with MATLAB and photon transfer theory. The photoresponse and FWC of pixels with different PPD spacings were obtained, as shown in Figs. 12 and 13, respectively. Fig. 12 shows the output of the test chip, the dimension of the output is ADU. The relationship of 'ADU' equivalent to 'e$^-$' is:

$$\mathrm{FWC}\left(\mathrm{e}^-\right) = \frac{\mathrm{FWC}\left(\mathrm{ADU}\right)}{K\left(\mathrm{ADU}/\mathrm{e}^-\right)}, \tag{6}$$

where K represents the system gain of the image sensor, FWC (ADU) and FWC (e$^-$) are the test chip output when the pixel is saturated. K is also expressed as the slope of the linear region of the photon transmission curve (PTC) during the rising phase. The measurement results are consistent with the simulation results in Table 2, that is, the number of signal charges (full well capacity) collected when the PPD is saturated will decrease with the increase of spacing. When the spacing is closest to 1.1 μm, it has the best FWC performance.

Based on these measurement conditions, the photoresponse and PTC of the special finger-shaped PPD structure (shown in Fig. 10(a)) is shown in Figs. 14(a) and 14(b), respectively. From the photoresponse, the FWC (ADU) is 11772 ADU. And, by linear fitting of the PTC curve, K is calculated to be 0.17148 ADU/e$^-$. Therefore, FWC (e$^-$) is also 68650e$^-$ according to Eq. (6), which is an increase of 8845e$^-$ compared to the FWC (59805e$^-$) before the further improvement. Therefore, the proposed PPD structure can effectively improve the full well capacity of a pixel.

Table 3 summarizes the FWC performance comparison

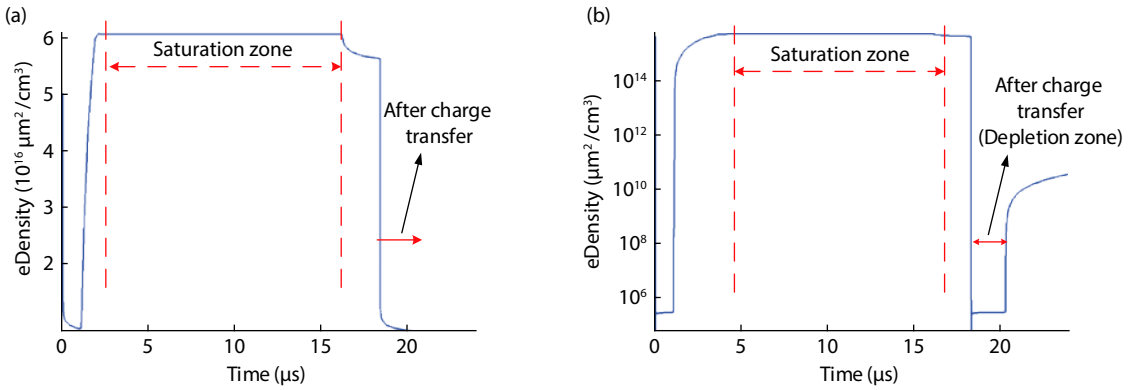

Fig. 9. (Color online) The number of electrons in PPD based on TCAD 2D simulation. (a) Using the process conditions of Fig. 2. (b) Using the process conditions of Fig. 8(d).

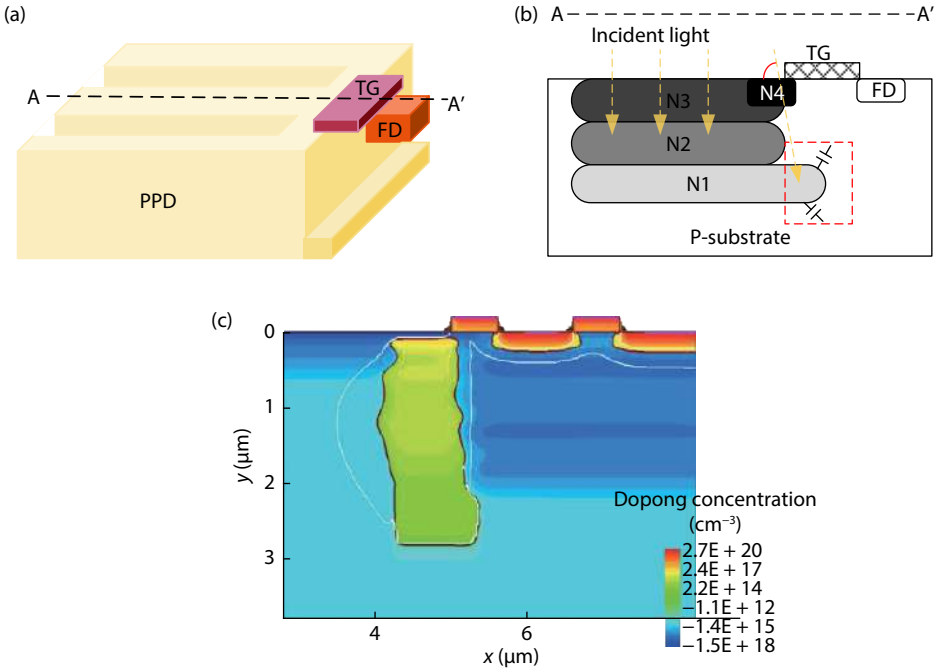

Fig. 10. (Color online) The special finger-shaped PPD structure proposed in this paper: (a) three-dimensional structure, (b) sectional structural view, (c) 2D device simulation diagram.

Table 3. Performance comparison between the pixel test results with a PPD of finger shape and related literature.

Parameter	This work	Ref. [20]	Ref. [21]	Ref. [22]	Ref. [23]
Technology	0.18 μm CMOS	90 nm CMOS	0.13 μm CMOS	0.18 μm CMOS	0.18 μm CMOS
Pixel size (μm^2)	6.00 × 6.00	5.86 × 5.86	5.60 × 5.60	5.60 × 5.60	6.50 × 6.50
FWC (e$^-$)	68650	30450	23000	47450	6400

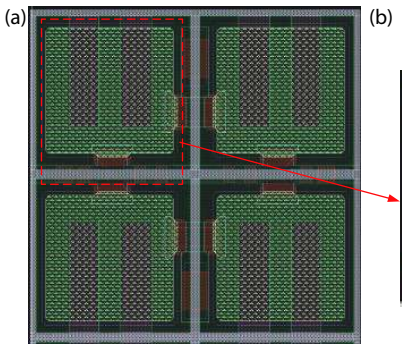

Fig. 11. (Color online) Pixel layout and the main layout level of PPD-TG-FD. (a) 2 × 2 pixel unit. (b) Layout of PPD-TG-FD.

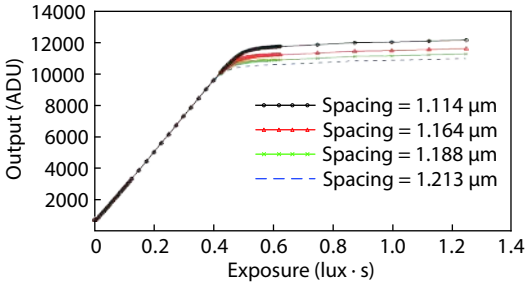

Fig. 12. Photoresponse with different single-finger spacing.

with other imaging devices in Refs. [20–23]. It shows that the PPD structure proposed in this paper effectively improves the full well capacity of CIS.

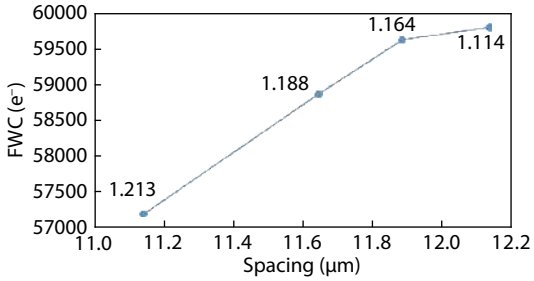

Fig. 13. (Color online) FWC with different spacing (Before widening N1).

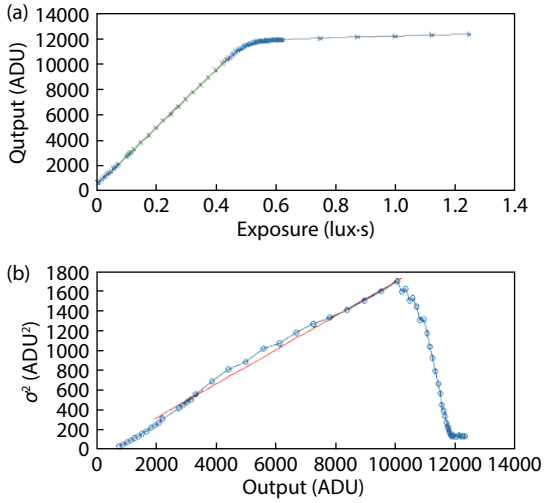

Fig. 14. (Color online) The measurement results of test chip: (a) photoresponse of the pixel using the proposed PPD structure, (b) PTC of the pixel using the proposed PPD structure.

5. Conclusion

This paper designs a CMOS image sensor with high full-well capacity based on 0.18 μm CMOS process. The finger-shaped PPD structure and the additional N-type ion implantation are used to increase the contact area of the PN junction and the unit-area capacitance of the PPD region, thereby improving the full well capacity of the CIS. Through simulation analysis, the pixel with this structure and process conditions has a depletion region depth of 2.8 μm and a charge transfer efficiency of 100%. The measurement results show that the full well capacity can reach 68650e⁻. Compared with the conventional structure, the proposed PPD structure can effectively improve the full well capacity of the pixel.

Acknowledgments

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References

[1] Bigas M, Cabruja E, Forest J, et al. Review of CMOS image sensor. Microelectron J, 2006, 37(5), 433
[2] Luo B, Yang F X, Yan L. Key technologies and research development of CMOS image sensors. IITA International Conference on Geoscience and Remote Sensing, 2010, 322
[3] Fontaine R. Innovative technology elements for large and small pixel CIS devices. Proc International Image Sensor Workshop (IISW), 2013, 1
[4] Wang X D, Ye T. Comparative research and future tendency between CMOS and CCD image sensor. Electron Des Eng, 2010, 18(11), 184
[5] Jan B, Erik J M, Wilco K, et al. Recent developments on large-area CCDs for professional applications. International image sensor workshop. Proc International Image Sensor Workshop (IISW), 2015, 1
[6] Velichko S, Hynecek J, Johnson R, et al. CMOS global shutter charge storage pixels with improved performance. IEEE Trans Electron Devices, 2015, 63(1), 1
[7] Solhusvik J, Kuang J, Lin Z, et al. A comparison of high dynamic range CIS technologies for automotive applications. Proc International Image Sensor Workshop, 2013, 1
[8] Freedman S D, Boussaid F. A high dynamic range CMOS image sensor with a novel pixel-level logarithmic counter memory. IEEE International Conference on Knowledge-Based Engineering and Innovation (KBEI), 2015, 14
[9] Takayanagi I, Yoshimura N, Mori K, et al. An 87 dB single exposure dynamic range CMOS image sensor with a 3.0 μm triple conversion gain pixel. Proc International Image Sensor Workshop (IISW), 2017, 30
[10] Wang R G, Yin Y X, Liang L, et al. A high dynamic range CMOS image sensor with dual charge transfer phase. IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), 2016, 1369
[11] Yu J T, Li B Q, Yu P P, et al. Two-dimensional pixel image lag simulation and optimization in a 4-T CMOS image sensor. J Semicond, 2010, 31(9), 094011
[12] Lofthouse-Smith D D, Soman M R, Allanwood E A H, et al. Image lag optimisation in a 4T CMOS image sensor for the JANUS camera on ESA's JUICE mission to Jupiter. Int Soc Opt Photonics, 2018, 10709, 107091J
[13] Rizzolo S, Goiffon V, Estribeau M, et al. Influence of pixel design on charge transfer performances in CMOS image sensors. IEEE Trans Electron Devices, 2018, 65(3), 1048
[14] Orly Y P, Ran G, Yosi S D. A random access photodiode array for intelligent image capture. IEEE Trans Electron Devices, 1991, 38(8), 1772
[15] Iltgen K, Bendel C, Benninghoven A. Optimized time-of-flight secondary ion mass spectroscopy depth profiling with a dual beam technique. J Vac Sci Technol A, 1997, 15(3), 460
[16] Park Y H. Image sensor having self-aligned and overlapped photodiode and method of making same. US Patent 7180151, 2007
[17] Li Z H. Research on image sensor with ultra wide dynamic range. PhD Thesis, Jilin University, 2016
[18] Cao X, Gäbler D, Lee C, et al. Design and optimisation of large 4T pixel. Proc Int Image Sensor Workshop (IISW), 2015, 112
[19] Han L Q. Study on the charge transfer mechanism and noise of CMOS active pixel. PhD Thesis, Tianjin University, 2016
[20] Oike Y, Akiyama K, Hung L D, et al. An 8.3M-pixel 480 fps global-shutter CMOS image sensor with gain-adaptive column ADCs and 2-on-1 stacked device structure. IEEE Symposium on VLSI Circuits, 2016, 1
[21] Lim W, Hwang J, Kim D, et al. A low noise CMOS image sensor with a 14-bit two-step single-slope ADC and a column self-calibration technique. IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2015, 51
[22] Yeh S, Hsieh C. Novel single-slope ADC design for full well capacity expansion of CMOS image sensor. IEEE Sens J, 2013, 13(3), 1012
[23] Xu R, Ng W C, Yuan J, et al. A 1/2.5 inch VGA 400 fps CMOS image sensor with high sensitivity for machine vision. IEEE J Solid-State Circuits, 2014, 49(10), 2342