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An Accurate BJT-Based CMOS Temperature Sensor with Duty-Cycle-Modulated Output

Guijie Wang, Ali Heidari, Kofi A.A. Makinwa, *Fellow Member IEEE,*
and Gerard C.M. Meijer, *Senior Member IEEE*

***Abstract*—This paper describes the design of a precision BJT-based temperature sensor implemented in standard 0.7μm CMOS technology. It employs substrate PNPs as sensing elements, which makes it insensitive to the effects of mechanical (packaging) stress and facilitates the use of low-cost packaging technologies. The sensor outputs a duty-cycle-modulated signal, which can easily be interfaced to the digital world and, after low-pass filtering, to the analog world. In order to eliminate errors caused by component mismatch, chopping and Dynamic Element Matching (DEM) techniques have been applied. The required component shuffling was done concurrently rather than sequentially, resulting in a fast DEM scheme that saves energy without degrading accuracy. After a single-temperature trim, the sensor's inaccuracy is ±0.1°C (-20°C to 60°C) and ±0.3°C (-45°C to 130°C), respectively. Measurements of sensors in different packages show that the package-induced shift is less than 0.1°C. Measurements of 8 sensors over 367 days show that their output drift is less than 6mK. While dissipating only 200μW, the sensor achieves a resolution of 3mK (rms) in a 1.8ms measurement time, and a state-of-the-art resolution Figure of Merit (FoM) of 3.2pJK^2. This combination of high accuracy, high resolution, high speed and low energy consumption makes this sensor suited for commercial and industrial applications.**

***Index Terms* – CMOS Temperature Tensor, Chopping, Dynamic Element Matching (DEM), Duty-Cycle-Modulation, One-Point Trim.**

I. INTRODUCTION

ONE of the first smart sensors that could be read out by simple microcontrollers was a temperature sensor that generated a duty-cycle modulated output signal [1], and which was implemented in BICMOS technology. Nowadays, a wide range of smart temperature sensors are available in low-cost CMOS technology [2] – [5]. However, it still make sense to design sensors with duty-cycle modulated outputs, because such signals have a number of useful and important features:

a) *Usability in both analog and digital systems*: Compared to the more widely used sigma-delta modulators, an attractive feature of duty-cycle modulators is that they can be easily and robustly connected to digital systems, such as microcontrollers, as well as to analog systems, such as thermostats ([6], chapter 10).

b) *Low energy consumption*: Often, the interface circuitry of a smart temperature sensor consumes more energy than the actual sensor itself. It then makes sense to perform the required signal processing in an external microcontroller as much as possible, so that the sensor's energy consumption (and self-heating) is minimized.

Recently, a CMOS smart temperature sensor with a duty-cycle-modulated-output signal has been presented [10]. In this paper, more details are disclosed together with the results of extensive measurements, which were done to characterize the new sensor for industrial applications. Compared to an earlier design with a duty-cycle-modulated-output [1], the main performance objectives of the new design are as follows:

a. Better accuracy and lower sensitivity to packaging shift.
b. More resolution at even higher acquisition rates.
c. Lower energy consumption per measurement.
d. Better long-term stability.

Early temperature sensors with duty-cycle-modulated outputs [1], [11], achieved good accuracy by exploiting the benefits of bipolar or BiCMOS technology, e.g. good component matching and the availability of high-performance Bipolar Junction Transistors (BJTs). Compared to CMOS technology, however, these benefits came at the expense of higher manufacturing cost. Although the analog performance of CMOS technology is arguably poorer, later work has demonstrated that it can also be used to realize accurate temperature sensors [12] – [16]. These sensors employ dynamic error-correction techniques, such as chopping, correlated-double sampling and Dynamic Element Matching (DEM) to mitigate the effects of component mismatch, and employ compensation schemes to reduce the effects of the low current gain of the available substrate PNPs [12], [16]. Straightforward implementation of such techniques would require complex circuitry and thus too much chip area. Furthermore, the required signal processing would then require hundreds of periods of the output signal, leading to a low data rate and high energy consumption. In this paper, it will be shown, how the required signal processing can be sped

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up, so that data rate and energy consumption can be minimized without losing performance.

In CMOS technology, the temperature-sensing elements can be BJTs [12] – [16], MOSFETs [17] – [18] or resistors [19] – [22]. The best accuracy has been achieved with BJTs after a one-point trim [12] – [16]. On the other hand, sensors based on MOSFETs or resistors can operate from low supply voltages, even below 1 V, but achieve lower accuracy, and sometimes even require multi-point trimming [21] – [22], thus significantly increasing calibration costs. Furthermore, the substrate PNPs available in CMOS technology, turn out to be quite insensitive to the mechanical stress induced by low-cost plastic packaging [23] – [25]. Consequently, excellent long-term stability and robustness to extreme thermal cycling can be achieved.

The sensor employs a continuous-time duty-cycle modulator whose system-level design is described in Section II. This is followed, in Section III, by a description of a self-clocked chopping and DEM scheme that averages component mismatch over several periods of the modulator's output. Straightforward application of this scheme would require 256 periods. However, it will be shown how this can be reduced to just eight without significant loss of accuracy. Details about the circuit implementation and signal processing are presented in Section IV and V, respectively. Measurement results are described in Section VI.

II. BASIC DESIGN

For reasons of simplicity, small chip size, low energy consumption and compatibility, the basic operation of the CMOS temperature sensor (Fig. 1) is chosen to be the same as that of previous designs [1], [11]. Under the control of a Schmitt trigger (ST), a capacitor C is periodically charged by a current I_1 up to a threshold voltage V_2 and then discharged by a current I_2 down to a threshold voltage V_1 (Fig. 1 (a)). As can be deduced from the timing diagram shown in Fig. 1 (b), the duty-cycle D of the resulting output signal equals:

$$D = \frac{t_H}{t_L + t_H} = \frac{\frac{(V_2 - V_1)C}{I_2}}{\frac{(V_2 - V_1)C}{I_1} + \frac{(V_2 - V_1)C}{I_2}} = \frac{I_1}{I_1 + I_2} \quad (1)$$

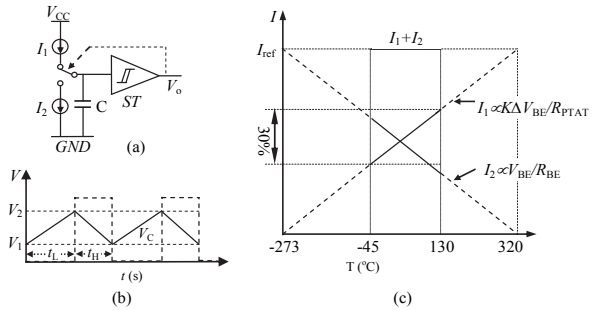

Fig. 1. The operation principle of the temperature sensor. (a) Basic principle; (b) the voltage across the capacitor C; (c) various (extrapolated) currents as a function of temperature.

It should be noted that the value of D is independent of the exact value of the ST's threshold voltages V_1 and V_2 and of the capacitance C. The two currents I_1 and I_2 are designed to be temperature dependent: In its simplest implementation, I_1 is linearly proportional to absolute temperature (PTAT), while I_2 is complementary-to-absolute-temperature (CTAT) (Fig. 1 (c)). Furthermore, if the sum $I_{ref} = I_1+I_2$ is designed to be temperature independent (as indicated in Fig. 1 (c)), then D will be a linear function of temperature.

In a CMOS process, the CTAT current I_2 can be derived from the base-emitter voltage V_{BE} of a substrate PNP, while I_1 can be derived from the difference ΔV_{BE} between the base-emitter voltages of two appropriately biased PNPs. However, as shown in Fig. 1 (c), the resulting duty-cycle D will then vary by only about 30% over the desired temperature range: -45ºC to 130ºC.

To increase the dynamic range of D, the currents I_1 and I_2 can be implemented as the combination of a PTAT current I_{PTAT} and a CTAT current I_{CTAT} [11], such that

$$I_1 = 3I_{PTAT} - 0.5I_{CTAT} \quad (2)$$
$$I_2 = I_{CTAT} - I_{PTAT}$$

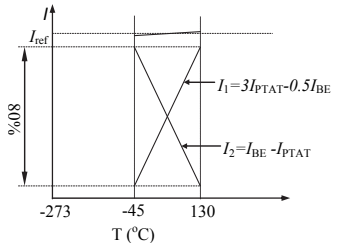

Fig. 2. The charge and discharge current in this design.

As in [11], the sum I_{ref} of the charging and discharging currents, i.e. $2I_{PTAT}+0.5I_{CTAT}$, was designed to have a slightly positive temperature coefficient, which effectively compensates the curvature in V_{BE}. As shown in Fig. 2, this scheme ensures that D now varies from about 10% to 90% over the desired temperature range: –45ºC to 130ºC.

Fig. 3 shows a simplified block diagram of the actual CMOS sensor. Substrate bipolar PNP transistors Q_1 and Q_2 are biased at a 1:9 current-density ratio, and an Op-amp (OP_1) forces the resulting voltage $\Delta V_{BE}=(kT/q)\ln(9)$ across a resistor R_{PTAT} to generate a PTAT current $I_{PTAT}=\Delta V_{BE}/R_{PTAT}$ (~1μA at room temperature). Similarly, OP_2 and resistor R_{BE} convert the base-emitter voltage V_{BE3} of Q_3 into a CTAT current $I_{CTAT}=V_{BE3}/R_{BE}$ (when both switches S_{BE1} and S_{BE2} are ON) . Next, these currents are linearly combined such that the capacitor C is charged by a current $I_1=3I_{PTAT}-0.5I_{CTAT}$ (S_1 is ON, one of S_{BE1} and S_{BE2} is ON) and is discharged by a current $I_2=I_{CTAT}-I_{PTAT}$ (S_1 is OFF, both S_{BE1} and S_{BE2} are ON).

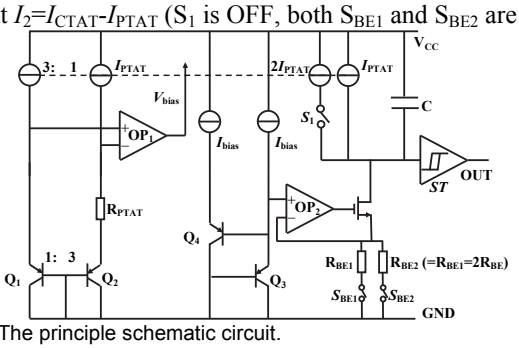

Fig. 3. The principle schematic circuit.

By properly choosing the values of R_{PTAT} and R_{BE}, as well as the nominal value of V_{BE3}, a linear duty-cycle versus temperature characteristic can be realized:

$$D = a_0 + a_1 \vartheta \quad (3)$$

where ϑ is the temperature in degree Celsius.

For compatibility with the previous design [1], the sensor was designed such that a_0 = 0.32 and a_1 = 0.0047(ºC)$^{-1}$. In BICMOS technology, a straightforward implementation of the Fig. 3 circuit resulted in good accuracy. This was because the current mirrors and other precision circuits could be implemented with well-matched bipolar transistors, while MOSFETs were only used as switches and digital logic. In CMOS technology, however, a straightforward implantation would result in very poor accuracy, because of the much large mismatch of MOSFETs. Fortunately, by applying chopping and DEM, this problem can be solved and, as will be shown in the next paragraphs, the resulting accuracy exceeds that of previous designs in bipolar or BICMOS technology.

III. Design For Accuracy

In the circuit shown in Fig. 3, the main sources of systematic error are:

- Component mismatch, which induces output spread.
- Process spread in the base-emitter voltage V_{BE3}.
- Limited current gain β of the substrate PNPs,
- Non-linearity of V_{BE} versus temperature.

In this section we will discuss ways to reduce the effects of these error sources one by one. The effects of noise will be discussed in section VI together with the experimental results.

A. Component mismatches

When designing precision sensors in CMOS technology, component mismatch is the main non-ideality to be taken into account. In our design, this will, for instance, give rise to errors in the gain of the various current mirrors, thus causing the ratios between the various charging and discharging currents to spread. Moreover, mismatch will cause offset voltages in the op-amps OP_1 and OP_2. These offset voltages are connected in series with our basic signals ΔV_{BE} and V_{BE} and thus directly reduce sensor accuracy. In order to prevent this, the effects of op-amp offset and 1/*f* noise are mitigated by the use of chopping. In addition, errors in current-mirror gain, as well as in the ratio of resistances and in the emitter areas of the substrate PNPs are mitigated by applying DEM. Since some ill-defined voltages will be dropped across the DEM switches in block S_{B2} (Fig.4), which are used to interchange Q_1 and Q_2, Kelvin connections are used to accurately sense ΔV_{BE} [14], [26]. The DEM and chopping-state machines are self-clocked (by the output of the Schmitt trigger ST), and so no external clock is required. The ratio R_{BE}/R_{PTAT} is made accurate by using large devices and careful layout.

As shown in Fig. 4, seven identical PTAT current sources are used to bias Q_1 and Q_2, as well as to charge and discharge the capacitor C. Therefore, a DEM cycle with at least seven states is required. Furthermore, four identical PNP transistors Q_1 and Q_2 were used to realize an emitter ratio of three. A complete DEM cycle of these transistors thus requires four steps. Lastly, the op-amps need to be chopped and the nominally identical R_{BE} resistors need to be swapped. To satisfy all these requirements, an extra dummy current source was added to the circuit (not shown in Fig. 4) and a DEM cycle with eight states was chosen. During each DEM cycle the following actions take place:

- the current sources are rotated once,
- the four BJTs are rotated twice,
- the R_{BE} resistors are swapped four times,
- the Op-amps are chopped four times.

Rotating all four groups of components one by one, so that each possible permutation would occur, would require 256 periods. This would be quite time and energy consuming, and the temperature of interest could vary quite significantly during such a long procedure. As one of the main innovations presented in this paper, all four groups of components are rotated concurrently, which significantly reduces the required number of DEM states. This means that not all possible permutations of component configurations are implemented. However, detailed analysis shows that rotating all four groups of components simultaneously is enough to cancel all first-order mismatch errors, leaving only the much smaller second-order errors.

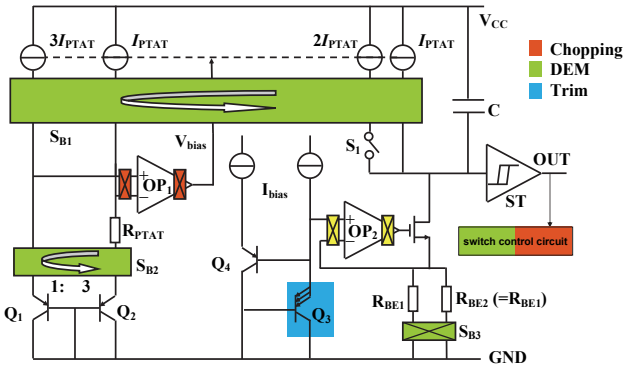

Fig. 4. Circuit modifications for reaching a higher accuracy.

B. Process spread in V_{BE3}

The second most important error source is the effect of process spread on the base-emitter voltage V_{BE3} [11] of Q_3. In the selected CMOS technology, the maximum deviation in this voltage amounts to about ±15mV, resulting in an unacceptable temperature error of about ±4K. This deviation can be corrected by trimming both the bias current and the emitter area of Q_3. When resistor spread is also taken into account, the required peak-to-peak trimming range is about 10K. To correct for this, a trimming scheme with a worst-case (largest) trimming step of about 50mK (see section IV) has been implemented.

C. Limited current gain

Another source of error and spread is the finite current gain β of the substrate PNPs (about 25 at room temperature). To reduce this error, an extra current source (Fig. 4), which is not included in the DEM scheme, and a substrate PNP (Q_4) are used to implement a simple beta-compensation scheme.

D. Non-linearity of V_{BE}

In order to partially compensate for the nonlinearity of V_{BE} versus temperature, the current sum (I_1+I_2) has been designed to be slightly proportional to temperature [11] [26].

IV. Circuit Design

In this section, key aspects of the circuit-level implementation of the CMOS temperature sensor are presented.

A. Current mirrors and current sources

To generate the PTAT currents ((Fig. 4), a wide-swing cascoded current mirror [27] has been used. Its large output impedance ensures that I_{PTAT} remains constant during the charging and discharging of the modulator's timing capacitor C. This ensures that the sensor has a low supply-voltage sensitivity.

B. Op-amps

The finite gain of the amplifiers OP_1 and OP_2 causes errors in I_{PTAT} and I_{CTAT}, respectively. In order to keep the resulting temperature-sensor errors below, for instance, 50mK, the gains of OP_1 and OP_2, must be larger than 90dB and 70dB, respectively. Moreover, the amplifiers must be able to handle input voltages (V_{BE}) down to about 0.3V at 130ºC. Both requirements are met by implementing OP_1 and OP_2 as folded-cascode amplifiers with PMOS input pairs [28].

C. Schmitt trigger

The Schmitt Trigger (ST) is based on the use of two inverters in series, with a positive feedback path that controls the threshold voltages of the first inverter [29]. In order to make the swing range as large as possible, the threshold voltage V_1 and V_2 (see Fig. 1 (b)) are chosen as close as possible to the corresponding rail voltages, which are:

$$\begin{aligned} V_1 &= V_{\text{TH\_N}} \\ V_2 &= V_{CC} - \left|V_{\text{TH\_P}}\right| \end{aligned} \tag{4}$$

where $V_{\text{TH N}}$ and $V_{\text{TH P}}$ are the threshold voltages of the input invertor of, an NMOS transistor and a PMOS transistor, respectively. The large voltage swing range (about $V_{CC} - 2$V) at the input of the ST ensures that its input-referred noise has negligible impact on the duty-cycle. By using a large capacitor (C ~150pF), the modulator's oscillation frequency is designed to be low enough (less than 7kHz) to ensure that the error caused by the ST's own switching time (a few nanoseconds) is less than 10mK.

D. Calibration

An 8-bit trimming network, consisting of a switchable array of PNPs, was used to adjust the base-emitter voltage of Q_3 (in Fig. 4) and to compensate for process spread. The base-emitter voltage can be trimmed, starting from its minimum value, with increments in a range of 0mV to 40mV, with a worst-case (largest) step size of about 50mK. After calibration, the trim code is stored by zapping Zener diodes that form a reliable and low-cost on-chip memory.

V. Signal Averaging

Due to the application of DEM and chopping in the circuit, the presence of component mismatch means that the duty-cycle of the sensor's output will vary from period to period. However, the output signal repeats every eight periods, which is the period of a full DEM cycle. In order to achieve an accurate temperature measurement, the sensor's output must be properly processed, as will be discussed in this section.

Fig. 5 shows the output signal of the temperature sensor over a full DEM cycle. A microcontroller can measure the time intervals t_{L1}, t_{H1}; t_{L2}, t_{H2} etc. relative to its own clock frequency. As discussed in Section III-A, systematic errors due to component mismatch and offset are compensated by averaging them over eight successive periods of the duty-cycle modulator. This signal-processing step is performed by the user, who must, therefore, be aware that the use of incomplete DEM cycles will result in a significant loss of accuracy. However, there are various ways in which the sensor's output can be averaged, as will be discussed below.

A. First type of averaging

A first type of averaging involves computing the duty-cycle of each period and then averaging the results. This yields the average value D_{avg1} as:

$$D_{avg1} = \sum_{i=1}^{8} (t_{Hi} / (t_{Hi} + t_{Li})) / 8 \tag{5}$$

where i is the order of the period in one DEM cycle (Fig. 5).

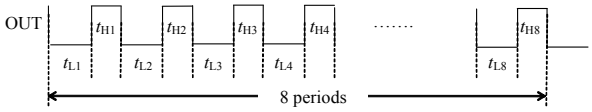

Fig. 5. The output signal of the temperature sensor.

B. Second type of averaging

A simpler method is to first sum the "High" and "Low" time intervals and then compute the average D_{avg2} with a single division as follows:

$$D_{avg2} = \sum_{i=1}^{8} t_{Hi} / \sum_{i=1}^{8} (t_{Hi} + t_{Li}) \tag{6}$$

This second type of averaging is equivalent to using an analog low-pass filter to convert the sensor's duty-cycle-modulated output into a DC voltage, which can then be read out by, for instance, a multi-meter. It can also be used in very simple analog temperature-control systems ([6], chapter 7). However, this type of averaging does not completely cancel the mismatch-induced errors, because in the calculation of (6), each period has a different weight: The longer periods will have larger weights than the shorter ones, and thus will contribute more error to the final "averaged" result. Fig. 6 shows the simulated residual temperature errors caused by 1mV offset in OP_1 (Fig. 4) for the two averages D_{avg1} and D_{avg2}, respectively. Here, both residual errors have been normalized to 0 at 27ºC. Note that the average D_{avg2} results in much more error, especially at low temperatures. However, for the limited range of −10ºC to +110ºC, the error is still less than 0.1ºC, which is acceptable in many applications.

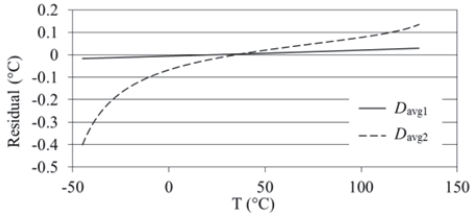

Fig. 6. Simulated residual errors obtained with D_{avg1} and D_{avg2} for an offset voltage V_{os1} = 1mV of OP_1.

C. Third method of averaging

Better temperature-sensing resolution can be obtained by averaging the sensor's output over more than one DEM cycle, because this will reduce the noise bandwidth (see section VI). If this is desired, a third type of averaging can be used to reduce the number of divisions required, while still obtaining high accuracy. This involves calculating the duty-cycle D_{avg3} as follows:

a) Suppose that the numbers N_{L1}, N_{H1}, N_{L2}, N_{H2}, … N_{L8}, N_{H8}, represent the 16 time intervals t_{L1}, t_{H1}; … t_{L8}, t_{H8} of the sensor's output over one DEM cycle.
b) For the first 8 periods, the values of N_{L1} to N_{H8} are stored in separate registers.
c) For the 9th period (= the first period of the second DEM cycle), the number N_{L9} is added to N_{L1}, while the number N_{H9} is added to N_{H1}. In a similar manner, this is done for the other 14 time intervals of the second DEM cycle.
d) Step c) is repeated for all other DEM cycles.
e) Next, the duty cycle D_{avg3} is calculated with an equation similar to (6):

$$D_{avg3} = \sum_{i=1}^{8} (N_{Hi} / (N_{Hi} + N_{Li})) / 8 \qquad (7)$$

Note that for M DEM cycles only eight divisions are required. So, as compared to using D_{avg1}, this approach reduces the calculation time by roughly a factor M, while its accuracy is as good as when using D_{avg1}.

VI. Fabrication and Test Results

The temperature sensor is fabricated in standard 0.7µm CMOS technology of On Semiconductor. The die size is 1.7mm x1.3mm (Fig. 7). In total, the chip has 13 pads. Nine of them are used to store the trimming code determined by wafer-level calibration at room temperature. The other four pads are available to the user and are: V_{CC}, GND, OUT and PD (an optional pad for POWER DOWN). The sensors have been packaged in TO18, TO92, TO220, SOT223 and SOIC-8.

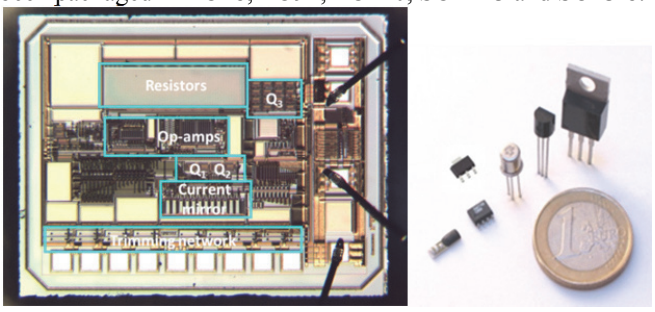

Fig. 7. Chip photo and packages of the temperature sensor.

The sensor has been trimmed at wafer level to counteract the effects of process spread. This is significantly less expensive than trimming individually packaged devices, but relies on the sensor being insensitive to packaging-shift. Without trimming the sensor exhibits about ±5K error, which is not acceptable.

A. Test set up

To characterize the duty cycle versus temperature accurately, the sensor's output is compared with that of a reference sensor. In our case, a Pt100 platinum resistor with an inaccuracy of less than ±20mK over the full temperature range of -45ºC to 130ºC, was used as the reference sensor. To ensure that the sensor temperatures were as close as possible to that of the reference sensor, a special set-up was built, as shown in Fig. 8. An ARM processor (STM32F103CBT6) with a 72MHz counter was used to digitize the time intervals of the sensor output and to calculate the average duty cycle.

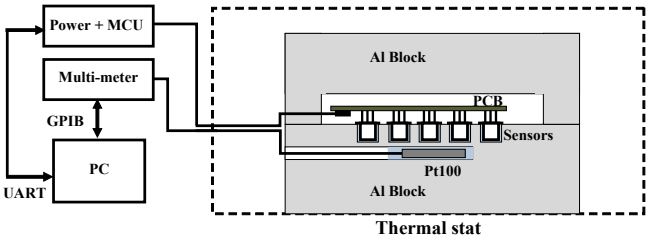

Fig. 8. Measurement set-up for the temperature characterization of the sensors.

B. DEM and averaging

The sensor's output is a rail-to-rail square-wave voltage. The frequency varies from about 500Hz to 7kHz, depending on the supply voltage and temperature, although the exact variation is subject to process spread. Only the duty cycle contains accurate temperature information.

As explained in section III, DEM and Chopping have been applied to achieve an accurate result. To benefit from this, the sensor's duty-cycle should be averaged over eight successive periods in one of the ways described in section V. Finally, the temperature is calculated using (3).

To show the importance of averaging over complete groups of 8 periods, Fig. 9 shows a typical real-time measurement result for each period (dashed line) without any averaging, and the moving average, using (5) over eight periods (solid line). Note that with the dashed line, the results repeat every eight readings, corresponding to the eight states of one DEM cycle, where errors induced by component mismatch are still present. The temperature error of each single period varies from –2.9K to 3.2K, and these values vary from sample to sample, depending on the specific mismatch. In contrast, averaging over eight periods reduces mismatch-induced errors significantly, to –0.018K.

It can be shown that the measurement can be started at an arbitrary transient (up-going or down-going) in a DEM cycle. So, no synchronization is required because any series of eight periods will cover a full DEM cycle. The measurement results discussed in the following text are all based on using the average over eight periods or integer numbers of eight periods.

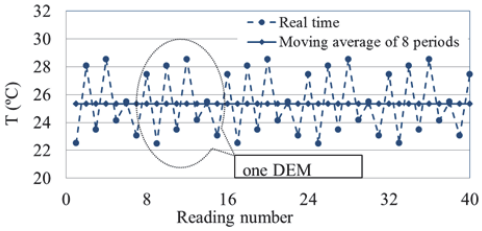

Fig. 9. Measured temperature reading at room temperature (T_{ref}=25.356°C).

C. *Accuracy versus temperature*

To characterize device spread, 36 calibrated samples in (metal) TO-18 packages were tested over the temperature range from -45ºC to 130ºC. As an example, Fig. 10 (a) shows the measured temperature errors of 70 samples from two batches after computing the average duty cycle according to (5) or (7) (D_{avg1} or D_{avg3}). This figure shows clearly the remaining systematic nonlinearity, which is mainly due to incomplete curvature correction and to the exponential increase of leakage currents at high temperatures.

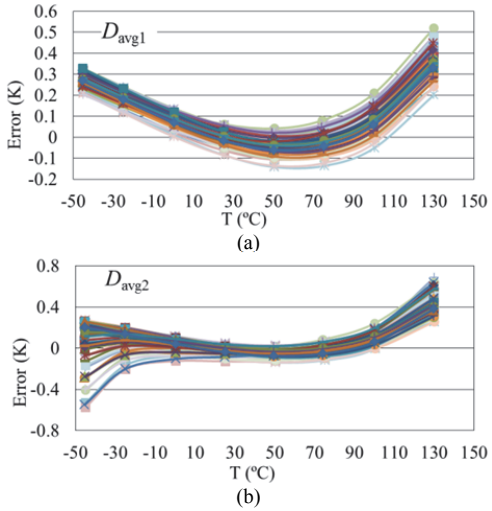

Fig. 10. Systematic error versus temperature for 70 samples from two batches when the duty cycle is calculated (a) with (5) or (7) (D_{avg1} or D_{avg3}, V_{CC} =5V) and (b) with (6) (D_{avg2}).

Fig. 10 (b) shows the measured total error for the case when, with the same measurement data, the average duty cycle is calculated with the simpler (6) (D_{avg2}). In agreement with Fig. 6, there is significantly more error at low temperatures. However, for the temperature range from 0ºC to 110ºC, this error is still less than 0.2ºC. Note that this error is larger than the simulated error shown in Fig. 6 and varies from sample to sample, depending on the specific amounts and combinations of offset and component mismatch that are present.

The measurement results depicted in Fig. 10 (a) show that the spread between the samples is very small. Therefore, the systematic non-linearity can further be reduced by fitting the sensor's residual nonlinearity with a higher-order polynomial. After a least-squares fit on the measurement results shown in Fig. 10 (a), the relationship between the average duty cycle D and temperature ϑ, is found to satisfy the following third-order polynomial:

$$D = a_0 + a_1\vartheta + a_2\vartheta^2 + a_3\vartheta^3 \tag{8}$$

where $a_0 = 0.32$; $a_1 = 4.68 \times 10^{-3}/(^{\circ}\mathrm{C})$; $a_2 = 7.03 \times 10^{-8}/(^{\circ}\mathrm{C})^2$; $a_3 = 1.10 \times 10^{-9}/(^{\circ}\mathrm{C})^3$ and ϑ = temperature in ºC.

Fig. 11 shows that the residual inaccuracy after computing D_{avg1} and applying (8) is less than ±0.2ºC from −45ºC to 130ºC.

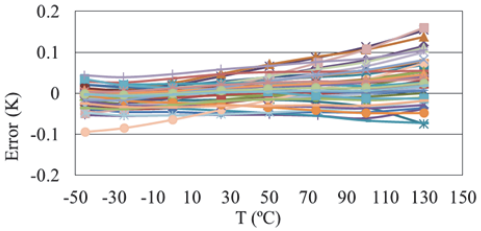

Fig. 11 Same data as depicted in Fig.10 (a), but when using a third-order correction of the results, according to (8).

D. *Noise*

At a stable temperature of about 25ºC, the sensor's noise was measured by logging the results of 360000 measurements, where each measurement is based on averaging over eight periods. A microcontroller with a 72MHz sampling frequency was used to digitize the time intervals. As shown in Fig. 12, for the minimum measurement time t_m of 1.8ms (8 periods), the resolution is about 3mK (rms). The sensor's energy efficiency can be benchmarked with the help of the resolution Figure of Merit (FoM) F, which is defined as follows [30]:

$$F = E \cdot s^2 \tag{9}$$

where E is the energy consumed during one complete measurement (one DEM cycle) and s is the sensor's resolution (standard deviation). For a supply voltage of 3.3V, a supply current of 60µA, and a measurement time t_m of 1.8ms (8 periods), the energy E for one measurement is only 356nJ. The sensor's resolution FoM is 3.2pJK^2, which is much smaller than that of other products in the market (see table II). Even including recent research results, this FoM represents the state of the art for BJT-based temperature sensors [10], [30].

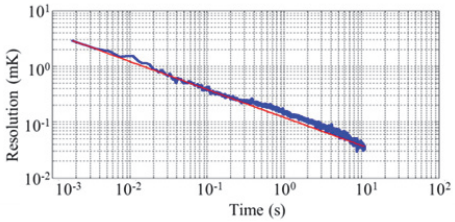

Fig. 12. Measured resolution (standard deviation) versus measurement time (72MHz sampling frequency).

In sensor systems where a slower microprocessor is used to digitize the time intervals, the quantization noise due to the limited sampling speed should also be taken into account. For this, the reader is referred to [30].

E. *DC Supply-voltage sensitivity*

Fig. 13 shows the change of the sensor's error versus the DC supply voltage for three temperatures, referred to the errors at V_{CC} = 5V. Over the whole temperature range, the output varies by less than 0.1ºC over the supply-voltage range from 2.5V to 5.5V.

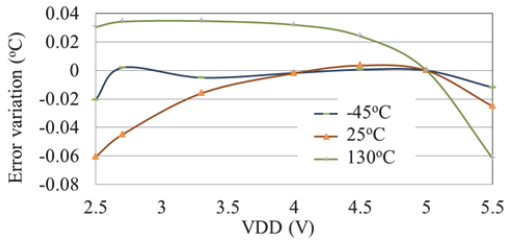

Fig. 13. Variation of sensor output with change of DC supply voltage, relative to its output with a 5V supply.

F. *Packaging and packaging shift*

To meet different market requirements, the new temperature sensor has been packaged in various types of packages (Fig. 8). Due to differences in the thermal expansion coefficients of the various materials involved (silicon die, die attachment and metal substrate), some mechanical stress remains after the high-temperature packaging process. Plastic packages induce much more mechanical stress than metal-can packages (i.e. TO-18) because they use an epoxy resin that completely covers the chip [24], [25]. Due to the piezo-junction effect, this packaging-induced stress will change the base-emitter voltage V_{BE3} (Fig. 4) and thus induce extra error in the sensor's output. As shown in [23] and [25], vertical PNPs are much less stress sensitive than vertical NPNs. So, the sensor presented here should exhibit less packaging shift and better stability than the one described in [11]. Packaging shift, as due to mechanical stress, has been investigated for the five different packages. The average values of this shift at room temperature for TO-18, TO-92, TO-220 are listed in Table I, together with values for a previous BiCMOS design in TO-18 and TO-92 packages [1].

Test results for other plastic packages (SOT223 and SOIC) are similar to those for TO92 and TO220 in Table I. These results show that the room temperature error induced by the metal-can package (TO-18) is almost negligible. The plastic packages induce a positive shift, which is much smaller than that of a previous product [1]. These results demonstrate the remarkable improvement that can be achieved when vertical PNPs rather than NPNs are used as sensing elements.

TABLE I
MEASURED PACKAGING SHIFT FOR THREE TYPES OF PACKAGES COMPARED WITH THE SHIFT IN THE PRODUCTS DESCRIBED IN **ERROR! REFERENCE SOURCE NOT FOUND.**]

	TO-18 this work	TO-92[1] this work	TO-220[1] this work	TO-18 [1]	TO-92[1] [1]
Number of sensors	36	18	9	18	18
Mean error (ºC)	0.004	0.044	0.053	-0.026	0.38
Spread (3σ) (ºC)	0.06	0.13	0.06	0.31	0.35

[1]: The plastic packages employ a stress-relieving die coating.

G. *Stability*

Long-term stability tests have been performed by a certified qualification company (Tempcontrol I.E.P. B.V.). Eight sensors (never powered-on after wafer calibration) were inserted in a metal tube, filled with thermal conductive compound. This tube was put in a water bath, whose temperature was regulated at 22ºC with an inaccuracy <0.5mK. Over 367 days, as shown in Fig. 14, the sensor's output drift was found to be less than ±6mK.

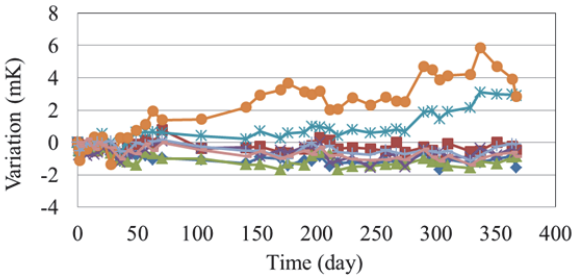

Fig. 14 Variation of temperature output over 367 days for 8 samples at 22ºC.

H. *Performance summary and comparison with other products*

Table II summarizes the main features of this design compared to existing products with similar accuracy or with a similar number of pins. A full list of specifications of the final product can be found in [31]. It can be seen that it achieves better accuracy, resolution and resolution FoM, as well as higher speed. One of the main reasons for its excellent resolution FoM is that it outputs a quasi-analog signal, whose time intervals are then digitized by a microcontroller. Thanks to this feature, the sensor's energy consumption, and hence, any self-heating effects are extremely low.

TABLE II
COMPARISON WITH OTHER STATE-OF-THE-ART TEMPERATURE SENSORS.

	This design	SMT160 [1]	D18B20 [2]	LMT01 [3]	TMP107 [4]	ADT7320 [5]
Supply voltage (V)	2.7 to 5.5	4.75 to 7.2	3.0 to 5.5	2.0 to 5.5	1.7 to 5.5	2.7 to 5.5
Supply current (μA)	42 to 75	180	1000 to 1500 (at 5V)	34 to 125	200 to 400	210 to 300
Number of pins	3 or 4	3	3	2	8	12
Temperature range (ºC)	-45 to 130	-45 to 130	-55 to 125	-50 to 150	-55 to 125	-40 to 125
Output signal	DCM	DCM	digital	digital	digital	digital
Measurement time (ms)	1 to 22	0.25 to 2	94 to 750	100	12 to 18	240
Supply voltage Sensitivity(ºC/V)	0.1	0.1	0.1	0.13	0.1	0.1
Best Accuracy (ºC) (Temperature range (ºC))	0.1[1] (-20 to 60)	0.7 (-10 to 100)	0.5 (-10 to 85)	0.5 (-20 to 90)	0.4 (-20 to70)	0.5 (-10 to 105)
	0.3[1] (-45 to 130)	1.2 (-45 to 130)	2 (-55 to 125)	0.7 (-50 to 150)	0.7 (-55 to 125)	0.66 (-40 to 125)
Resolution (ºC) Measurement time (ms)	0.003 1.8	0.005 20	0.0625 750	0.0625 100	0.0156 15	0.0078 240
Resolution FoM (pJK^2)	3.2	430	$1.46\text{x}10^7$	$4.38\ \text{x}10^4$	$2.42\ \text{x}10^3$	$8.28\text{x}10^3$

[1]: The accuracy in these cells is the result using (8) and D_{avg1} or D_{avg3}.

VII. CONCLUSIONS

The details of a BJT-based temperature sensor designed and fabricated in 0.7µm CMOS technology have been discussed. The use of a duty-cycle-modulated output signal enables easy interfacing with both digital and analog systems. Its high output data rate makes this sensor well suited to both temperature monitoring and controlling. A high accuracy is achieved by applying DEM and chopping, which significantly reduces the errors caused by CMOS component mismatching. Simultaneously rotating all the component groups during the DEM process, instead of rotating them one after one, reduces the number of DEM periods significantly, making the measurement speed much faster. By applying DEM, the mismatch-induced errors from the various groups of components can be reduced to the second order. To achieve this result, the results of a complete DEM cycle must be averaged. Three different types of averaging have been discussed. They provide different trade-offs between computational speed/complexity and sensing accuracy. Applying substrate PNPs instead of NPNs reduces errors caused by package-induced stress. As a result, the presented sensor has a much better long-term stability than earlier designs. It also facilitates the use of low-cost packaging technologies, which compared to metal-can packaging, typically induce large amounts of mechanical stress.

Measurement results show that this temperature sensor achieves a state of art resolution Figure of Merit, which is better than (3.2pJK^2). This makes this sensor highly suited for low-energy applications. After wafer calibration at room temperature, the sensor's accuracy is better than 0.1°C (-20°C to 60°C) and 0.3°C (-45°C to 130°C), respectively. Package-induced errors were found to be less than 0.1°C at room temperature. Measurements over 367 days show a long-term drift less than 6mK.

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