Negative Offset Operation of Four-Transistor CMOS Image Pixels for Increased Well Capacity and Suppressed Dark Current

Bongki Mheen, *Member, IEEE*, Young-Joo Song, and Albert J. P. Theuwissen, *Fellow, IEEE*

***Abstract*—This letter presents an electrical method to reduce dark current as well as increase well capacity of four-transistor pixels in a CMOS image sensor, utilizing a small negative offset voltage to the gate of the transfer (TX) transistor particularly only when the TX transistor is off. As a result, using a commercial pixel in a 0.18 μm CMOS process, the voltage drop due to dark current of the pinned photodiode (PPD) is reduced by 6.1 dB and the well capacity is enhanced by 4.4 dB, which is attributed to the accumulated holes and the increased potential barrier near the PPD, respectively.**

***Index Terms*—CMOS image sensor (CIS), dark current, four–transistor pixel, hole accumulation diode, imager, pinned photodiode (PPD), well capacity.**

I. Introduction

RECENTLY, the CMOS image sensor (CIS) has gained lots of interest based on its strong superiority of the CIS pixel's scalability [1], [2], even though it has a limit which is set by the diffraction of the camera lens [2]. Because the pixel scaling generally results in cost reduction and performance gain even at complex pixel structures, a four-transistor pixel structure, where higher sensitivity and better noise reduction has been achieved, is being extensively used in versatile commercial products [3]–[7]. However, the lowered operation voltage resulting from this device scaling is one of the main limiting factors for the stable and excellent performance of the pixel.

One of the main obstacles in lowering supply voltage at a pixel is the insufficient suppression of the potential barrier between the pinned photodiode (PPD) and the channel of transfer (TX) transistor when the TX transistor is on [5]–[7]. Therefore, some efforts such as using a reduced gate length of the TX transistor with optimized PPD profile and a new photodiode structure with a 0.25 μm CMOS process [6], [7] were tried to make the complete reset (RX) of the PPD and prevent noise increase due to image lag. This problematic barrier normally happens because of two reasons. One is the increased surface boron implant dose for sufficient surface pinning and dark (noise) current reduction. The other is the out-diffusion phenomena of boron itself, which is easily diffused at the subsequent thermal processes.

Since the dark current is normally increased with device scaling due to severe implant conditions and low thermal budget, a higher surface implantation concentration is normally required for the dark current reduction. On the other hand, it is also required that the potential barrier that is formed by such additional implants should be suppressed sufficiently when the TX transistor is on, while it can sustain a sufficiently high potential barrier when the TX transistor is off during the light integration to have a required well capacity. Therefore, it is important to enhance both contradicting conditions, particularly under a low supply voltage process such as the sub-0.18 μm CMOS process.

In this letter, we propose an electrical method to reduce the dark current and increase well capacity simultaneously under low supply voltages. This proposed method was experimentally verified by using a four-transistor pixel in a commercial CIS fabricated by 0.18 μm CMOS technology with a supply voltage of 2.5 V for pixel driving.

II. Proposed Driving Method and Experiments

Increased doping concentration at the top of the PPD normally reduces the dark current flowing into the PPD in Fig. 1(a) because the holes from the top area of the PPD play a key role to fill the traps at the Si-SiO_2 surface and make the surface potential pinned at ground level [8]. However, because of the aforementioned reasons, increasing the boron concentration in this structure is normally restricted when a sub-0.18 μm CMOS process is used.

Under the condition using a conventional TX pulse (TX1) as shown in Fig. 1(b) with an RX signal for the RX transistor, the hole concentration of the "region A" during light integration is determined by both doping profile and gate potential. On the other hand, in the proposed method, to keep the "region A" electrically in a hole accumulation condition during light integration, a different TX pulse (TX2) with a negative off-potential voltage $(V_{\mathrm{TX},G(\mathrm{off})})$ is applied to the gate of the TX transistor as shown in Fig. 1(b) (negative offset operation) [9].

Meanwhile, even under the negative offset operation, most of the channels of the TX transistor is sustained to be depleted (OFF-state) because the doping level of the channel is much lower than that of "region A." In the case where this part of the channel is also accumulated by the holelike "region A," it will increase the electrical field of the depletion region of floating diffusion (FD) node toward the TX transistor and result in

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B. Mheen is with the Electronic Instrumentation Laboratory, Technical University of Delft, 2628 CN Delft, The Netherlands and also with the IT Convergence and Components Laboratory, Electronics and Telecommunications Research Institute, Daejeon 305-350, Korea (e-mail: mheen@ieee.org).

Y.-J. Song is with the Industrial Technology Development Laboratory, Korea–China Semiconductor IT Association, Kunming, Yunnan Province, China.

A. J. P. Theuwissen is with the Electronic Instrumentation Laboratory, Technical University of Delft, 2628 CN Delft, The Netherlands.

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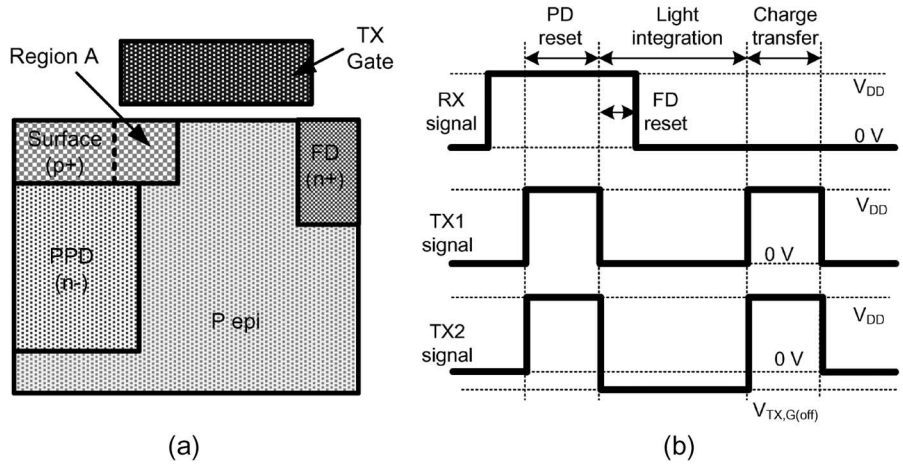

Fig. 1. (a) Cross section of the TX transistor consisting of a PPD and an FD node as source and drain, respectively. (b) Comparison of the signals applied to the gate of the RX and the TX transistor for conventional and negative offset operation.

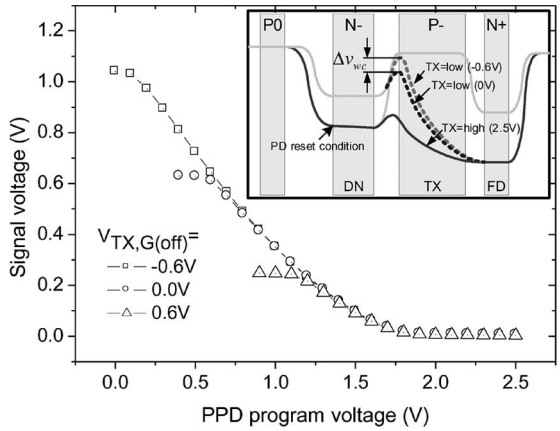

Fig. 2. Charge TX curves at the $V_{\mathrm{TX},G(\mathrm{off})}$ voltages of -0.6, 0, and $+0.6$ V, with an energy band diagram comparison showing well capacity offset (Δv_{wc}) between $V_{\mathrm{TX},G(\mathrm{off})}$ values of 0 and -0.6 V.

higher leakage current of the FD node, which will be discussed later.

The used pixel size is 3.2 μm $\times$ 3.2 μm in a 1.0 megapixel commercial CIS. The minimum feature size and supply voltage to the pixel array are 0.18 μm and 2.5 V, respectively, which means that the pixel is supposed to be suffering from insufficient barrier suppression due to lowered operational voltage.

III. Results and Discussion

For the measurement of well capacities for the three different $V_{\mathrm{TX},G(\mathrm{off})}$ voltages (-0.6 V, 0 V, 0.6 V) of the TX transistor, three charge TX curves were obtained as shown in Fig. 2. It shows similar charge TX curves near the RX voltage, but the full well capacities were differently measured as 1.04 V, 0.629 V, 0.248 V at the $V_{\mathrm{TX},G(\mathrm{off})}$ of -0.6, 0, and 0.6 V, respectively. The energy band diagrams between the PPD and the FD when the TX transistor is on (2.5 V) and off (0 V, -0.6 V) are shown, respectively, in the inset of Fig. 2. Consequently, it can be concluded that the proposed method increases the barrier between the PPD and TX gate during the light integration time and makes it possible to provide a pixel with additional well capacity in addition to other various optimization efforts.

Normally, the threshold voltage of the TX transistor is designed to be kept low to make the PPD fully depleted when the TX transistor is on. This effort normally sacrifices the well capacity due to an insufficient barrier when the TX transistor is off. Therefore, it is generally required to adjust the potential barrier to an optimum operating condition. By using the proposed method ($V_{\mathrm{TX},G(\mathrm{off})} = -0.6$ V), the potential barrier height can be increased electrically and selectively only when the TX transistor is off, i.e., during light integration, while the potential profile when the TX transistor is on is sustained to be unchanged. Consequently, this method gives an additional freedom to increase the well capacity in a pixel design while sustaining the same degree of resetting the PPD.

To inspect the well capacity variation in more detail, $V_{\mathrm{TX},G(\mathrm{off})}$ was swept from -1.4 to 0 V while keeping the other parameters the same. As shown in Fig. 3(a), the well capacity was increased as $V_{\mathrm{TX},G(\mathrm{off})}$ was decreased and it saturated nearly at the $V_{\mathrm{TX},G(\mathrm{off})}$ of -0.6 V where the surface potential under the TX gate was sufficiently increased to the level comparable to other potential barriers surrounding the PPD. Beyond this negative bias offset voltage, the photogenerated electrons in this PPD cannot be stored because they can flow through other boundaries around the PPD except for the boundary abutting to the TX transistor.

Similarly, the effect of negative offset operation on the dark current was also investigated, As previously described, the negative $V_{\mathrm{TX},G(\mathrm{off})}$ also forces the "region A" in the hole accumulation condition during light integration and the channel of the TX transistor in depletion mode (OFF-state) simultaneously due to different doping concentrations. The generated holes in "region A" recombine with dark electrons generated from defects at the Si-SiO_2 surface and/or fill the traps around this area. To verify the effect of $V_{\mathrm{TX},G(\mathrm{off})}$ on the dark current reduction, the $V_{\mathrm{TX},G(\mathrm{off})}$ was swept from -1.0 to 0 V. The RX voltage for the PPD through the RX and TX transistors is kept at 2.5 V, which is the conventional operating condition of this pixel in a commercial product.

As shown in Fig. 3(b), by changing the $V_{\mathrm{TX},G(\mathrm{off})}$ from 0 to -0.6 V, the voltage drop at the FD node due to dark current is reduced from 3.77 to 1.87 mV (about 50% reduction). The reduction of the dark current at the PPD node is attributed to the sufficiently accumulated holes near the boron implant

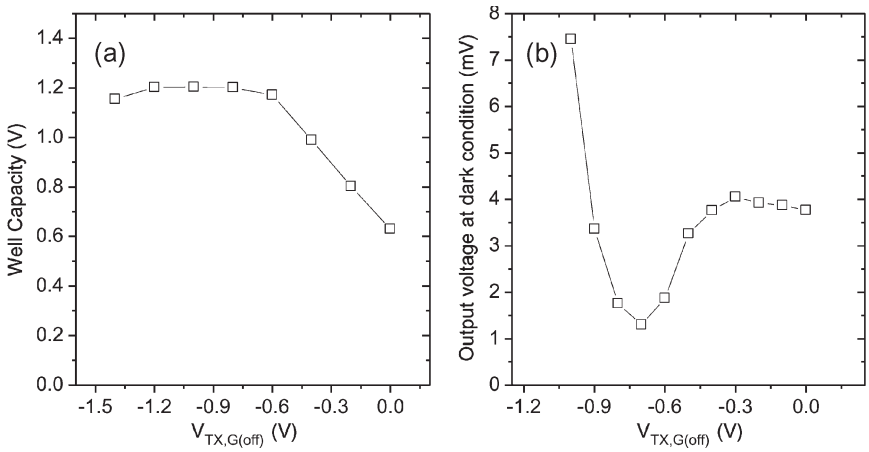

Fig. 3. (a) Well capacity under various $V_{\mathrm{TX},G(\mathrm{off})}$ voltages from -1.0 to 0 V. (b) Output voltage due to dark current under various $V_{\mathrm{TX},G(\mathrm{off})}$ voltages from -1.0 to 0 V.

TABLE I
ENHANCEMENT RESULTS USING THE PROPOSED NEGATIVE OFFSET OPERATION

Property	Unit	Used method		Enhancement
		Conventional	Proposed	(Unit: dB)
Full Well capacity	V	0.629	1.04	4.4
	e-	8986	14857	
Output signal due to dark current	MV	3.77	1.87	6.1
	e-	54	27	

surface under the TX transistor gate area [region A in Fig. 1(a)]. Considering that the region is relatively smaller than the other surrounding areas of the PPD, this region is believed to be more likely to generate dark current than other regions of the PPD for the given image sensor product due to the higher electrical field and process boundary.

For a lower $V_{\mathrm{TX},G(\mathrm{off})}$ than -0.6 V, the dark current increases sharply. It is caused by the direct conducting path formed by the decreased gate potential. At a larger negative gate bias of the TX transistor (< -0.6 V), the channel of the TX transistor also starts to be accumulated by the hole, making a direct conducting path from the p^+ surface layer up to the depletion region of the FD node. It increases the electric field in the depletion region of the FD node toward the TX transistor, and induces a large FD reverse leakage current.

The experimental results for both well capacity and dark current are summarized in Table I where the numbers of electrons are also shown from the derived capacitance (2.3 fF in this pixel) of the FD node while keeping all other conditions the same.

This technique can be used in any other site where a dark current can be found within a pixel [9]. Compared with the similar effort to accumulate holes near the STI where traps can be found using an additional metal line with an offset voltage [10], this method has another merit wherein it does not require such an additional metal line in a pixel array, because it can use the existing address line for the TX transistor. Therefore, it helps to sustain the same quantum efficiency without being affected by increased height and complexity of the metal stack.

IV. CONCLUSION

To increase the well capacity and decrease the dark current in a four-transistor CMOS image pixel, an electrical method was proposed and experimentally evaluated. In this negative offset operation method, the negative potential of the TX transistor (-0.6 V) was applied only when the TX transistor is off. The well capacity was increased from 0.629 to 1.04 V (4.4 dB) due to potential barrier height enhancement. In addition, the dark current was also reduced from 3.77 to 1.87 mV (6.1 dB) because of the reduction in generated dark electrons flowing to the PPD by accumulated holes at the top of the PPD. However, a further decrease in the negative bias abruptly increases the dark current because of the activated direct conducting path from the p^+ area up to the FD node, which gives the optimum negative offset voltage of -0.6 V in this experiment. As a result, the proposed method was proven to be useful and can be utilized in low-voltage four-transistor pixel designs without significant changes in pixel structure and operation.

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