Carbon Nanotubes as Vertical Interconnects in 3D Integrated Circuits

Sten Vollebregt

Carbon Nanotubes as Vertical Interconnects in 3D Integrated Circuits

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To my parents

Contents

1

Introduction

This chapter serves as introduction to this thesis. First, current state-of-the-art interconnect technology and some of its limitations are discussed. This is followed by a discussion on 3D integration, which has been identified as potential solution to many problems in current interconnect technology. Challenges in the 3D integration are identified, and carbon nanotubes (CNT) are presented as potential interconnect material to solve these challenges. Requirements for successful integration of CNT into semiconductor technology, and an overview of previous work from literature are presented. The chapter concludes with the definition of the research problem, and an outline of this thesis.

1.1 The interconnect era

The continued downscaling of transistor dimensions as dictated by Moore's Law has been the driving force of the semiconductor industry for many decades. Each new generation of transistors is roughly 1.4 times smaller, which doubles the number of transistors which can be put in the same area, and is released to large-volume manufacturing about every 18 months. While downscaling the transistor generally improves delay, power consumption and price per transistor, the same is not true for downscaling the interconnects.

Already in the mid-90's it was predicted that interconnect RC-delay, the time it takes to charge up a line with a resistance R and capacitance C, would become a serious performance issue. Indeed, it surpassed gate delay at the end of the decade, as shown in fig. 1.1. This forced the industry to shift to Cu as interconnect material, lowering R. Furthermore, so-called low-k dielectrics (where k is the dielectric constant, thus lowering C) were introduced instead of SiO_2 for the electrical and mechanical separation of the individual lines [1,2]. However, in 1995 it was already predicted that this change of materials would "reach practical limits in just a few generations" [1].

Indeed, current interconnect technology suffers from many issues. The further reduction in wire dimensions introduces grain and surface boundary scattering, and poor scaling of barrier layers (required against Cu diffusion), which increase the resistivity of the line [3]. Furthermore, the pursue of materials with an even lower dielectric constant results in many mechanical stability issues in the resulting interconnects.

Besides the electrical performance expressed by the interconnect delay and power dissipation, the electrical reliability is becoming an issue. A decade ago the International Technology Roadmap for Semiconductors (ITRS) predicted that by now the current density in metal lines would have surpassed the maximum current density (J_{max}) of bulk Cu for high-end Very-Large-Scale Integration (VLSI) circuits. A shift from aggressive clock-scaling to multi-core designs alleviated this issue, but still the most recent 2012 update of the roadmap predicts problems 10 years from now [4].

Thus, interconnects are becoming increasingly important for the performance of future Integrated Circuit (IC), which requires the introduction of new materials and concepts, as the current materials are reaching their physical limitations. One of the most promising new concepts, 3D integration, will be discussed in the next section.

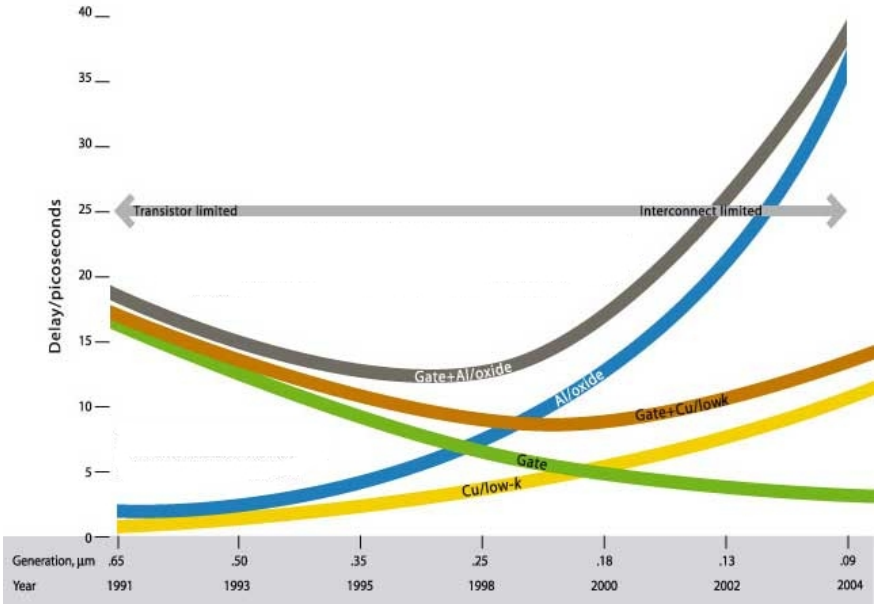


Figure 1.1: Gate and interconnect delay for different technology nodes, source [2]

1.2 3D integration and vertical interconnects

One way of reducing the RC-delay of interconnects is simply by reducing their total length. In planar VLSI technology this is rather difficult to achieve, as chip sizes remain large due to an increase of the number of transistors, while the transistors become smaller. However, a radical change in interconnect length could be obtained by stacking layers of transistors on top of each other and using many vertical interconnects (vias) to connect individual transistors, as shown by fig. 1.2a-b [5]. Due to the added dimension of wiring, the total interconnect length can be reduced. Several approaches exist for 3D integration: chip stacking (fig. 1.2b), wafer stacking, or direct stacking of transistor layers on a single wafer (fig. 1.2d, dubbed monolithic integration) [5–7].

Chip stacking is a technique which recently became mature enough for mass production. In this technique (thinned) chips are stacked on top of each other after testing. State-of-the-art chip stacking uses Through Silicon Vias (TSV) to connect the different device layers. Through silicon means that the vias go through the entire bulk Si, reaching the next chip as shown

in fig. 1.2b. Still, even when the stacked chips are thinned down to tens of μm, quite some performance will be lost in these relative long TSV. As the maximum achievable aspect ratio for Cu plating is limited, the TSV take up considerable space, which otherwise would have been available for transistors. Moreover, this limits the density of vias, expressed as number of vias per unit area. Increasing the aspect ratio from 5-10 to 10-20 will reduce the wasted area, but in turn will give problems with Cu filling. Finally, the use of Cu for TSV introduces all kind of reliability problems due to Cu diffusion into the transistor area, and mismatch between the thermal expansion coefficients of Si and Cu.

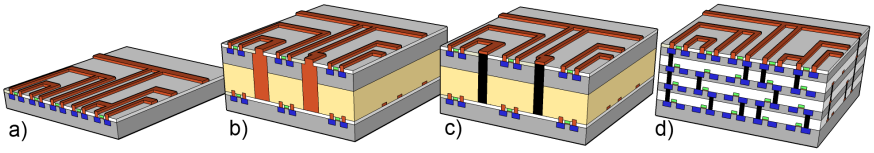


Figure 1.2: Overview of current and future interconnect technology: (a) traditional planar technology, all metal layers are routed on top of the transistors; (b) current 3D IC technology using Cu TSV to connect chip or wafer stacked layers of transistors; (c) 3D IC TSV technology with CNT TSV; (d) monolithic 3D IC with high aspect ratio CNT vias

The highest via density can be obtained by using monolithic integration, in which the layers of transistors are just a few μm apart separated by a dielectric layer, as shown in fig. 1.2d. Several challenges have to be resolved in order for monolithic integration to reach mass volume production. One of these challenges, the creation of a layer of transistors on top of an existing layer has been investigated previously in our group by using so-called Single-Grain Thin-Film Transistors (SG-TFT) fabricated by the μ-Czochralski process [8, 9].

Fabricating vias with a sufficient high aspect ratio (> 2.5) to achieve the high via density for monolithic integration, up to a billion vias per cm^2 [7], will be another challenge. Cu is likely unable to reach high enough aspect ratios: already in planar IC technology it is reaching its practical limit. Beside that contamination issues will become even more severe as the vias have to be placed much closer to the transistors.

Another challenge for 3D integration is thermal management. Current VLSI chips already operate several tens of degrees above room temperature, with power densities being reached which are comparable with that of a nuclear reactor (> 100 W/cm^2). Stacking multiple layers of transistors on top of each other will increase the amount of transistors per unit area

beyond that of traditional scaling. The heat of the transistors has to be transported efficiently to the surface, through all the interconnect layers. As the dielectrics surrounding the interconnect normally have a thermal conductivity of just a few W/mK, most heat will go through the interconnect lines. While Cu is a good thermal conductor (401 W/mK), new materials like graphene and Carbon Nanotubes (CNT) have recently been shown to be able to transport up to ten times more heat [10].

1.3 Carbon nanotubes for interconnects

As discussed in the previous section Cu is reaching its physical limits and will likely not be able to reach the desired aspect ratios required to create 3D IC with a high enough via density. Beside that it suffers from reliability issues due to the high current density, contamination issues, thermal expansion mismatch and an increase in resistance due to the continued down-scaling.

Much effort has been put in finding alternatives for Cu as interconnect material. One material which gained particular interest are CNT, especially for vias as they can easily be fabricated vertically [11, 12]. CNT are an allotrope of sp^2 hybridized carbon, and can be visualized as rolled up sheets of graphene (in which graphene is a single atom thick layer of graphite). Nanotubes consisting of one sheet of graphene are called a Single-Walled Carbon Nanotubes (SWCNT), and tubes consisting of multiple sheets are dubbed Multi-Walled Carbon Nanotubes (MWCNT), see also fig. 1.3 for a graphic overview.

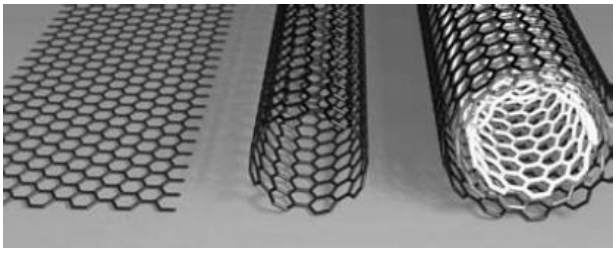


Figure 1.3: Schematic representation of (from left to right): graphene, SWCNT, and MWCNT.

One of the biggest advantages of CNT as interconnect material is their current carrying capacity due to the strong sp^2 bonds, which has been demonstrated to be in the order of 10^9 A/cm^2, even at elevated temperature [13]. In comparison, the maximum current density of Cu is in the

order of 10^6 A/cm^2. Besides being able to withstand a large current density, CNT are in general good electrical conductors. Simulations have shown that potentially CNT are able to outperform Cu as interconnect material [14,15].

Beside their electrical properties, CNT have two more characteristics which makes them attractive as future via material. One of them is the high thermal conductivity, up to 3500 W/mK as shown by measurements [10], which is almost 9 times higher than that of Cu. Finally, it has been demonstrated that CNT can be fabricated at High Aspect Ratio (HAR) [16], which is caused by their bottom-up nature of fabrication. Those features make CNT very attractive for use as CNT TSV, as shown if fig. 1.2c, and future monolithic 3D IC as displayed in fig. 1.2d.

1.3.1 Requirements for CNT integration

In the previous section the potential advantages of CNT were discussed. To introduce a new material into existing semiconductor technology several boundary conditions will have to be met in order to successfully integrate the material, and make it an attractive candidate to replace current materials:

- Electrical and thermal performance: similar or better than that of Cu.
- Deposition temperature: to prevent thermal damage to the transistors deposition temperature should be no higher than 500 °C, and preferable below 400 °C for future generations and low-k dielectrics.
- Materials: only materials which are considered compatible with VLSI technology.
- Equipment: equipment and techniques which are similar to existing equipment is recommended.

1.3.2 Previous work on CNT vias

Due to their potential, it is no surprise many different groups have been working on vias consisting of CNT. Already in 2002 Infineon Technologies displayed interest in CNT as interconnect and demonstrated some first integration results [11,17]. Being the first their growth temperature of 700 °C, and electrical resistance (see fig. 1.4) were both high. Not much later Fujitsu Ltd. started working on fabricating CNT vias [18–20]. Beside Infineon and Fujitsu also Samsung displayed some interest in CNT vias [21,22], but again the reported resistance and growth temperature (600 °C) are too high.

The research of Fujitsu resulted in many break-troughs towards high-density low temperature integration with a low electrical resistance. For

instance, they identified ways of decreasing contact resistance by using Ti or TiN as contact material [23] and Chemical Mechanical Polishing (CMP) to improve the electrical contact and allow conduction through multiple MWCNT shells [24–26]. In order to increase bundle density a technique was developed to directly deposit metal nanoparticles on top of the substrate [27]. Later ballistic transport for 60 nm high vias was demonstrated [28]. In 2008 the current record holding via in terms of electrical resistivity was fabricated, at a growth temperature of just 390 °C [29]. Still its resistivity of 0.69 mΩ-cm is two orders of magnitude higher than that of bulk Cu. Unfortunately, the equipment Fujitsu employed for catalyst deposition and growth are considered non-standard and can have potential scaling issues to full wafer sizes, which makes it unattractive for large scale manufacturing.

Several research groups at universities have also investigated the use of CNT for via application. The group of Robertson at Cambridge University investigated methods to obtain ultra high density growth (expressed in tubes/cm^2) [30, 31] and growth on $CoSi_2$ (an often used material for source/drain contacts in transistor) [32]. Unfortunately, most high density growth is obtained on non-conductive Al_2O_3 layers, although tunnelling through a thin Al_2O_3 layer to CNT was demonstrated [33]. Furthermore, the growth temperature is too high (650 °C), and no electrical measurements performed on actual vias are reported. Recently a reduction of growth temperature to 450 °C was demonstrated, but unfortunately no electrical measurements were shown [34]. A cooperation between Cambridge and CEA-LETI resulted in the demonstration of vias with ultra high density ($2.5 \cdot 10^{12}$ tubes/cm^2) grown at 590 °C [35]. Their measured resistance of 10 kΩ was very high, though, likely due to bad electrical contacts to the CNT.

KU Leuven/Imec investigated the use of CNT grown at 470 °C as via in future sub-32 nm nodes and provided full electrical characterization, although the resulting resistivity were initially still high [36–38]. Recently, they have demonstrated growth at temperatures as low as 400 °C [39], and an improved 540 °C process which resulted in a resistivity of 5 mΩ-cm [40, 41].

For TSV, which are relative new, only a few integration results using CNT TSV have been shown. The first attempt was done by Xu et al. [42]. Although growth in deep silicon holes was demonstrated, no complete vias were fabricated. The first complete TSV were demonstrated by Wang et al. [43, 44], although the growth temperature used (700 °C) and resistance are still too high for practical applications. Recently, some work by the group of Robertson has been published about CNT grown on Al_2O_3 at 650 °C for TSV [45].

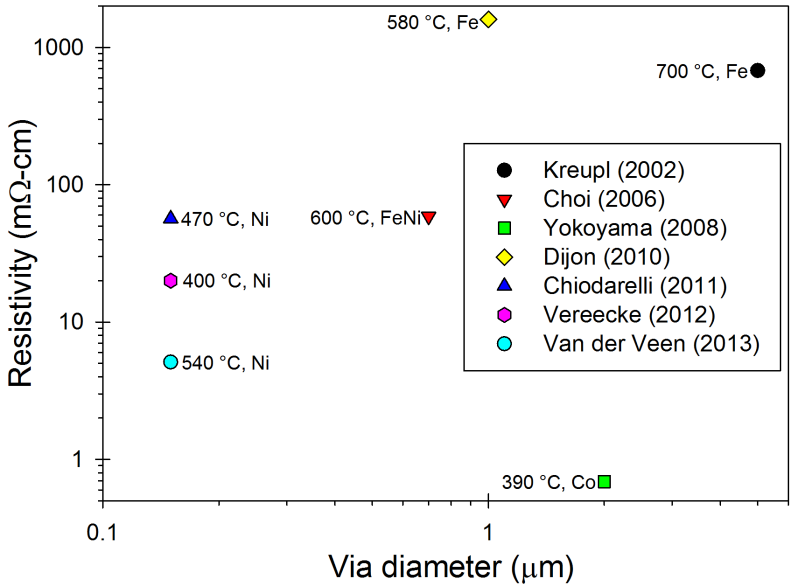


Figure 1.4: Overview of reported electrical performance of fully integrated CNT vias from literature.

The reported electrical measurements expressed in electrical resistivity from the groups mentioned above are shown in fig. 1.4. Only results obtained from fully integrated vias are considered (i.e. not from direct probing the bundle). A large spread of values is observed, due to the difference in quality of the CNT material, and the sometimes very high contact resistance. Overall, all values are considerably higher than that of bulk Cu which has a resistivity of 1.68 $\mu\Omega$-cm.

Beside the poor overall electrical performance and often high deposition temperature, several other things are lacking in the available work on CNT vias. Very little is know about the magnitude of the electrical contact resistance, electrical reliability, and thermal performance of these vias. Furthermore, there have so far been no attempts to integrate the vias into any actual electronic circuits, often due to the too high deposition temperature.

1.4 Outline of this thesis

The goal of this research is to investigate and demonstrate that CNT can be used as vias in 3D IC. The focus will mostly be on monolithic 3D IC,

however the growth of CNT for TSV has also been investigated. In the case of monolithic 3D IC the vias which are desired to replaced by CNT are the ones interconnecting subsequent device layers. As a relative thick (for the 3D IC process using SG-TFT ~ 2.5 μm) oxide is required, the aspect ratio of the vias will be around 2.5 iff minimal sized vias (1 μm^2) are used. This is an aspect ratio unachievable using Al metallization by sputtering.

My initial research problem, *can CNT be used as vertical interconnects in 3D IC*, can be split into several parts:

- What would be the required tube densities to achieve similar electrical performance as Al or Cu? (*Chapter 2*)
- How can the quality of the grown CNT be determined? (*Chapter 3*)
- How can the CNT be fabricated at conditions compatible with integration into the 3D-IC process? (*Chapter 4*)
- What is the electrical performance and reliability of these CNT? (*Chapter 5*)
- What is the thermal performance of these CNT? (*Chapter 6*)
- Does the integration of CNT in electronics have an impact on the transistor performance? (*Chapter 7*)

The research questions from the previous section are discussed in the different chapters of this thesis in the same order they were stated. Chapter 2 provides a background on the electrical and thermal properties of CNT, together with a background on fabricating CNT. In chapter 3 Raman spectroscopy is presented as method to investigate CNT quality, and this method is used on two different kind of samples (low and high crystal ordering). Chapter 4 discusses several catalysts and support layers used in this work for growing the CNT, and the properties of the resulting growth. Finally, some details are given on fabrication approaches which can be used to integrate CNT in semiconductor technology.

The electrical characterization of test vias fabricated on TiN using the methods described in chapter 4 are discussed in chapter 5, this includes resistance measurements, characterization of the Temperature Coefficient of Resistance (TCR), and reliability measurements. Next, the thermal properties of the fabricated vias are discussed in chapter 6 using a novel vertical 3ω-method. Chapter 7 discusses the integration of CNT vias into a SG-TFT monolithic 3D processes, together with the electrical performance of the fabricated circuits. Finally, a conclusion and future prospect are provided in chapter 8.

2

Properties and growth of carbon nanotubes

This chapter provides some background on carbon nanotubes and their electrical and thermal properties, and growth methods. First the electrical modelling is discussed, resulting in an equivalent circuit model of a via consisting of a CNT bundle. After that, the influence of the bundle density on the electrical resistivity is discussed and theoretical minimum densities are calculated. This is followed by a discussion and literature overview of the thermal conductivity and thermal boundary resistance of CNT. Finally, chemical vapour deposition is discussed as method to fabricate CNT, and the impact of process parameters is given together with the standard recipes used throughout most of this work.

2.1 Terminology

As mentioned in the previous chapter a CNT can be visualized as a rolled-up sheet(s) of graphene, which itself is a single-atom thick layer of sp^2 hybridized carbon. Depending on the number of walls CNT are dubbed SWCNT, Double-Walled Carbon Nanotubes (DWCNT), or MWCNT. Defective MWCNT with graphene sheets crossing the tube axis along its length, but still with graphene sheets parallel to the axis, are often called bamboo MWCNT. Very defective tubes without any apparent graphene sheets along their tube axis are dubbed Carbon Nanofibres (CNF). Beside the number of walls, other parameters of interest are the tube diameter, chirality, length, quality and for bundles the density (section 2.2.5).

Of these parameters chirality and quality are the least unambiguous and will be specified in more detail. The chirality, defined by the so-called chiral vector C_h and its indexes (n, m), is the way the graphene sheet is rolled-up compared to the unit vectors of the graphene unit cell. This is visualized in fig. 2.1. The rolling up of the graphene sheet changes the band structure of the CNT, influencing it electrical properties [46]. In case a shell of a CNT has chiral indexes $n = m$ (dubbed armchair) the shell is metallic. When $n - m = 3i$, in which i is a non-zero integer, the shell is semi-metallic with a bandgap of a few meV. In all other cases the shell will be semiconducting, with a bandgap that depends on its diameter. For a random chirality distribution this will results in $1/3$ of the tubes being (semi-)metallic.

Quality denotes the crystallinity of a CNT. Generally, no number is associated with this property and simply the definition low or high quality is employed. Quality can be investigated using Transmission Electron Microscope (TEM), but this is generally expensive, time consuming and the outcome depends heavily on the viewed area. Another approach is Raman spectroscopy, which is fast (measurements generally take just tens of seconds to a few minutes), non-destructive and relatively inexpensive. It also allows for a more quantitative approach as information from the obtained spectrum can be translated in numbers and compared. Raman spectroscopy will be discussed in more detail in chapter 3.

In this chapter some background on CNT is provided. First the electrical properties and an equivalent circuit model will be discussed. This model will be used to investigate the required bundle density to achieve a resistivity comparable to Al and Cu. This will be followed by a discussion on the thermal properties of CNT. The chapter concludes with an introduction into CNT fabrication.

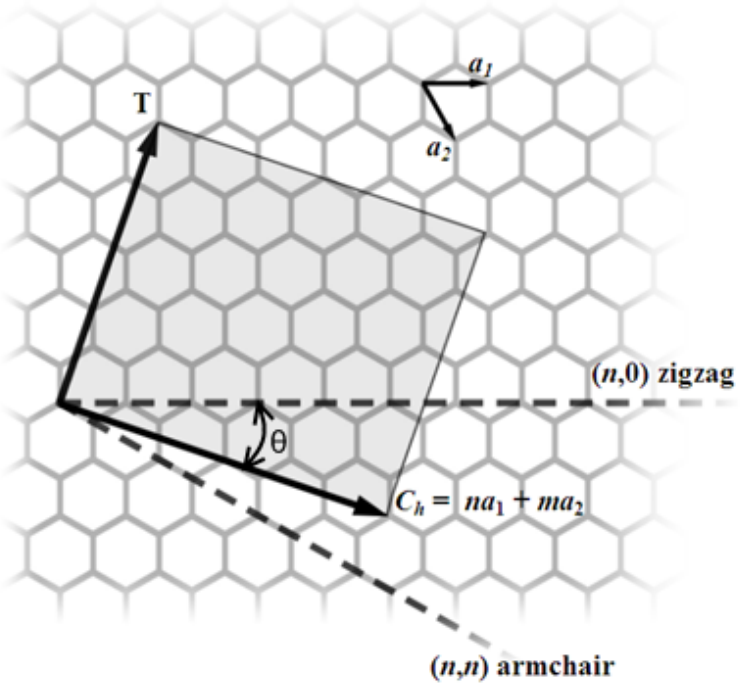


Figure 2.1: Definition of the chiral vector C_h and its indexes (n, m). T denotes the tube axis, and a_1 and a_2 are the vectors of the graphene unit cell in real space.

2.2 Electrical properties

2.2.1 Resistance of a CNT

A high quality CNT can exhibit ballistic conduction up to a length of several μm [47]. Although this implies that the resistance is independent of length, this does not mean that a CNT has no resistance. As CNT are an 1D material, they have only limited amount of conduction bands available. Once a contact is formed between a system consisting of many conduction bands (e.g. a metal) and a material with limited states, a mismatch is formed between the conduction bands resulting in a quantum conductance which can be described by the Landauer Formula [46]:

$$G = \frac{e^2}{h} M T_i(E_F) \tag{2.1}$$

in which e is the electron charge, h Planck's constant, M the amount of available conduction channels in the few-states system, and $T_i(E_F)$ the reflection probability at the contacts.

The next step is to determine the amount of available conduction bands for a specific CNT. This number depends heavily on both the chirality, and the diameter of a tube. For a metallic SWCNT there are 2 channels which are both spin-degenerate, thus $M = 4$ which results in a quantum resistance $R_Q = 6.45$ kΩ in case of ideal contacts ($T_i(E_F) = 1$). For semiconducting SWCNT there are no conduction bands available at room temperature and zero bias, and a bandgap (E_g) exist given by equation 2.2, in which a_{cc} is the C-C bond length (0.142 nm), γ_0 the C-C hopping constant (2.5-3.2 eV), and d the tube diameter [48]. As the diameter of a SWCNT is generally smaller than 2 nm the contribution of semiconducting SWCNT to conduction at room temperature is neglectable.

$$E_g = \frac{2a_{cc}\gamma_0}{d} \approx \frac{0.84}{d\ [\text{nm}]}\ [\text{eV}] \tag{2.2}$$

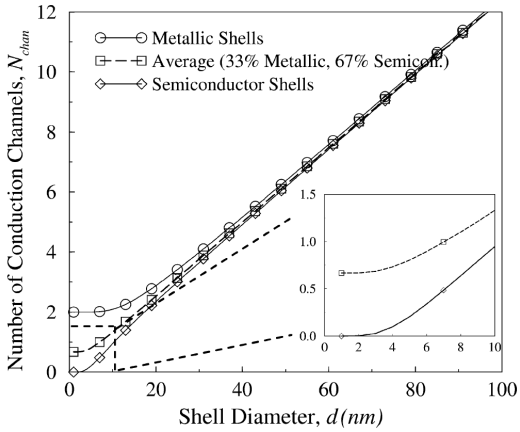


Figure 2.2: Number of conductive channels per wall vs. diameter ($T = 300$ K), from [49]

For MWCNT the situation is slightly more complex. Not only are there multiple shells available, due to the increase in diameter more conduction bands become available per shell [14]. Moreover, due to the large diameters semiconducting shells only have a small bandgap, which can be overtaken by charge carriers at elevated temperatures. These effects, assuming that a third of the channels are metallic for a random chirality distribution, are

shown in eq. 2.3, while fig. 2.2 displays the diameter dependency of the conduction channels at room temperature.

$$\begin{array}{rcll} N_{conductive}(d,T) & \approx & aTd+b, & d > d_T/T \\ & \approx & 2/3, & d < d_T/T \end{array} \tag{2.3}$$

Here a is 4.67×10^{-4} $\text{nm}^{-1}\text{K}^{-1}$, b is 0.2, d the diameter of the shell, T the temperature in Kelvin, and d_T equals 1300 nm·K. The total number of conductive shells for a MWCNT can now be expressed as [15]:

$$\begin{array}{rcl} N_{channels} & = & \sum_{N_{shells}} N_{conductive} \\ N_{shells} & = & 1 + \left\lfloor \frac{d_{out}-d_{in}}{2\delta} \right\rfloor \end{array} \tag{2.4}$$

Where d_{out} and d_{in} are the outer and inner tube diameter of the MWCNT, respectively, and δ is the spacing between walls, which is normally 0.34 nm. Equations 2.3 and 2.4 can be combined to [49]:

$$N_{channels} = \frac{2}{3}\left(1 + \left\lfloor \frac{(d_{out}-d_{in})}{2\delta} \right\rfloor\right), d_{out} < 6 \text{ nm} \tag{2.5}$$

$$= \left(1 + \left\lfloor \frac{(d_{out}-d_{in})}{2\delta} \right\rfloor\right)\left(\frac{1}{2}aT(d_{out}+d_{in})+b\right) \tag{2.6}$$

For a bundle it is normally assumed that interactions between individual CNT are weak [49,50] and the total bundle quantum resistance (R_Q) is the sum of all quantum resistances per conductive channel in parallel, here N_{tubes} is the number of tubes in the bundle:

$$R_Q = \frac{1}{N_{channels}N_{tubes}}\frac{h}{2e^2} \tag{2.7}$$

In case the tube is ballistic this quantum resistance drops only over the contacts and not the tube itself. When the tube length exceeds the Mean Free Path (MFP) of the CNT ($l > \lambda_{CNT}$), the tube operates outside the ballistic regime and the resistance becomes length dependent. This MFP can be as large as several μm for SWCNT [47], while for multi-walled CNT (MWCNT) a length of 25 μm has been reported [51]. The MFP of a tube depends heavily on its quality. The additional resistance R_L due to the limited MFP is per unit length:

$$R_L = R_Q\frac{1}{\lambda_{CNT}} \tag{2.8}$$

The CNT resistance can also be bias dependent, but it has been concluded that this influence can be ignored in interconnects as the potential drop over an interconnect is generally small [49,50].

As final resistive component the contact resistance between the CNT and its (metal) contact has to be included as R_C for both contacts, as normally $T_i(E_F) < 1$. This resistance can be rather large in the order of hundred kΩ [37], and should thus not be omitted when comparing simulations to measurements. Metals like Ti, Au and Pd have been demonstrated to allow for a good contact [25,47,52,53], where R_C has been found to have the same order of magnitude as R_Q. The total CNT bundle resistance can now be expressed by (assuming R_C is defined as each individual metal-CNT contact resistance to the bundle, and l is the length of the tube):

$$R_{CNT} = 2R_C + R_Q + R_L = 2R_C + R_Q(1 + \frac{l}{\lambda_{CNT}}) \tag{2.9}$$

2.2.2 Capacitance of a CNT

A nanotube not only has a quantum resistance, but also a quantum capacitance caused by the low dimensionality of the system and the limited charge carriers and states. Burke [54,55] gives a derivation for both, which will be shortly treated here.

A SWCNT can be seen as a 1D quantized electron gas consisting of four non spin-degenerate parallel channels. The Pauli exclusion principle states that two electrons cannot occupy the same quantum state simultaneously. All quantum states till the Fermi energy (E_F) are already occupied (at low temperature), thus the electron should be added above E_F. As electrons travel at E_F through metals, energy should be added to the electron to put it in the available quantum state above E_F. For a 1D quantum wire of length L the energy difference (δ) between quantum levels is given by equation 2.10, where k is the wave number, E the energy, $v_F = 8 \cdot 10^5$ m/s the Fermi velocity in graphene [56], and $\hbar = h/2\pi$.

$$\delta = \frac{dE}{dk}\delta k = \hbar v_F \frac{2\pi}{L} \tag{2.10}$$

The quantum capacitance per unit length can now be calculated using equation 2.11, which is the relation between the quantum capacitance and the required energy. As a SWCNT consists of four parallel channels the total quantum capacitance should be four times the quantum capacitance of a single 1D wire (hence the factor four in equation 2.12).

$$\frac{e^2}{C_Q} = \delta \tag{2.11}$$

$$C_{Q,CNT} = 4\frac{2e^2}{hv_F} \tag{2.12}$$

$$C_{Q,CNT} = 400 \text{ aF}/\mu\text{m}$$

For MWCNT with perfect contacts each conducting wall simply contributes $C_{Q,CNT}$ in parallel, therefore increasing the quantum capacitance [57,58]. Rossi et al. [58] introduced a coupling capacitance between adjacent walls (the capacitance between non adjacent walls is shielded by the walls in-between). This capacitance is derived from the coupling between two cylinders in a traditional coaxial cable. If the walls carry the same signal, which should be the case for interconnects this coupling capacitance can be neglected.

Now the equations describing the capacitance of a generic CNT bundle can be formulated. Every conductive shell of every tube in the bundle adds a quantum capacitance of 200 aF per μm length. As these capacitances are all in parallel they add, giving the following expressions for the quantum capacitance of a bundle per unit length:

$$C_Q = N_{channels} N_{tubes} \times 200 \text{ aF}/\mu\text{m} \tag{2.13}$$

From this it follows that the value of C_Q rapidly increases when bundle width or length increase.

Besides a quantum capacitance a CNT also has an electrostatic capacitance C_E. The electrostatic capacitance for an individual tube depends on it position within the bundle. Generally the outer tubes display the largest capacitance, while the inner tubes of a bundle are shielded by their neighbours [49,50]. For accurate simulations the capacitance per outer tube should be calculated [50], although as a first approximation the electrostatic capacitance of traditional metal lines can be used [49]. The coupling capacitance between tubes are normally ignored as the tubes are assumed to be equipotential [50]. Finally, the electrostatic capacitance is in series with the quantum capacitance. As capacitances in series add like resistors in parallel the smallest capacitance dominates, which in most practical applications will be the electrostatic capacitance [49].

2.2.3 Inductance of a CNT

Due to the low density of current carriers in nanotubes there is a large kinetic energy stored in the current flow. Therefore a CNT has a dominant kinetic inductance, the magnetic inductance can even be neglected as it is many orders of magnitude smaller [54, 56]. The kinetic energy per unit length in a 1D wire is the sum of the kinetic energies of the particles moving left and right. In case of a net current one of the particle streams dominates. If, for instance, the particles moving to the left dominate and their Fermi energy is raised by $e\Delta\mu/2$ (where $\Delta\mu$ is the change in mobility, which depends on the effective mass, which in turn depends on k), and the E_F of the particles

moving to the right is decreased by the same amount, the net current in the 1D wire will be:

$$I = (e^2/h)\Delta\mu \tag{2.14}$$

The increase in kinetic energy is the amount of excess electrons times their added energy and is given by (δ is the same as in equation 2.10):

$$N_{exec}\Delta E_{elec} = \left(\frac{e\Delta\mu}{2\delta}\right)\left(\frac{e\Delta\mu}{2}\right) = \frac{(e\Delta\mu)^2}{4\delta} \tag{2.15}$$

Combining equation 2.14 and 2.15 and taking into account that the kinetic (or inductive) energy equals $^1/_2LI^2$ an expression for the kinetic inductance per unit length can be derived (equation 2.16). Again care has to be taken that the CNT consists of four parallel channels, and the total inductance should be divided by a factor four.

$$\begin{aligned} L_{K,CNT} &= \frac{1}{4}\frac{h}{2e^2 v_F} \\ L_{K,CNT} &= 4 \text{ nH}/\mu\text{m} \end{aligned} \tag{2.16}$$

For a MWCNT and a bundle the same reasoning holds as for the quantum resistance and capacitance and thus the kinetic inductance of a bundle per unit length (L_K) becomes:

$$L_K = \frac{1}{N_{channels}N_{tubes}} \times 8 \text{ nH}/\mu\text{m} \tag{2.17}$$

For current VLSI technology the inductance can in all cases be ignored when performing simulations [50], but might become important for giga and terrahertz applications.

2.2.4 Equivalent circuit model

With all individual components identified, an equivalent circuit for a CNT bundle can be made, as shown in fig. 2.3. As can be clearly seen the circuit consists of constant and length dependent part. In this model it is assumed that the quantum resistance drops equally over both contacts, while the contact resistance (R_C) is defined as the total resistance between the macroscopic (metal) contacts and the bundle. For most practical applications (i.e. dense bundles) the kinetic inductance and quantum capacitance can be neglected, as discussed before.

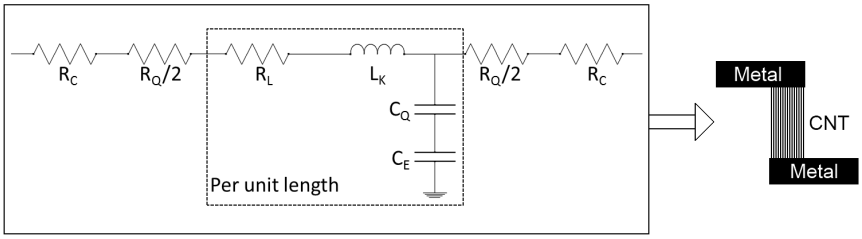


Figure 2.3: Equivalent circuit of a CNT bundle

2.2.5 The density of a bundle

A common reported value for grown bundles of CNT is the density of such a bundle, given in tubes/cm^2. This density can be determined by simply counting the number of tubes from a SEM cross-section, or by determining the fill-factor using liquid densification [35]. A simple model to evaluate the theoretical maximum density of a bundle with hexagonal packing was developed, as shown in fig. 2.4. Here d is the diameter of the tubes, s the spacing, and h and w the dimensions of the bundle. The number of CNT for a given bundle size (h, w) can now be determined by:

$$N_W = \left\lfloor \frac{w+s}{x} \right\rfloor \tag{2.18}$$

$$N_H = \left\lfloor \frac{h-d}{\sqrt{3}/2x} \right\rfloor + 1 \tag{2.19}$$

$$x = d+s$$

$$N_{CNT} = N_W N_H \qquad \text{if } w+s-N_W x \geq \frac{x}{2} \tag{2.20}$$

$$= N_W N_H - \left\lfloor \frac{N_H}{2} \right\rfloor \qquad \text{otherwise} \tag{2.21}$$

In fig. 2.5 the CNT density as predicted by the model is displayed against the diameter (ranging from 0.3 to 100 nm) and separation (1 – 10 nm). As expected for zero separation the density decreases quadratic for increasing diameter, while for tubes with a large separation and small diameter the influence of the diameter is only small. For small diameter tubes the density decreases sharply when the separation is increased, as many tubes are being removed from the bundle. For large diameter tubes increasing the separation removes only a few tubes, resulting in a weak dependency on separation.

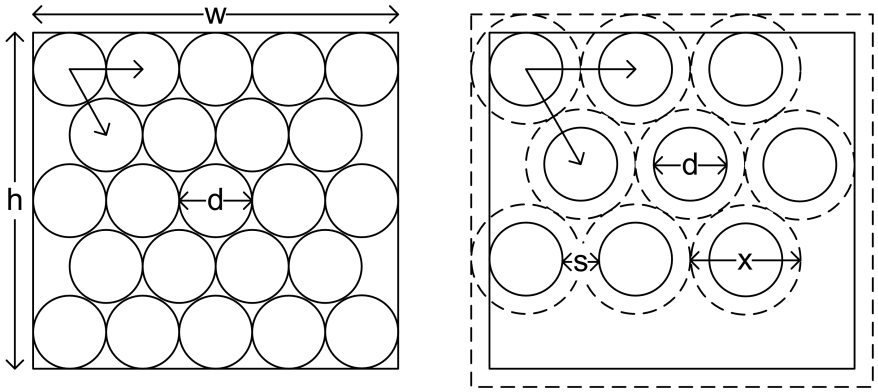


Figure 2.4: Model of ideal tight packed (left) and sparse packed (right) bundle

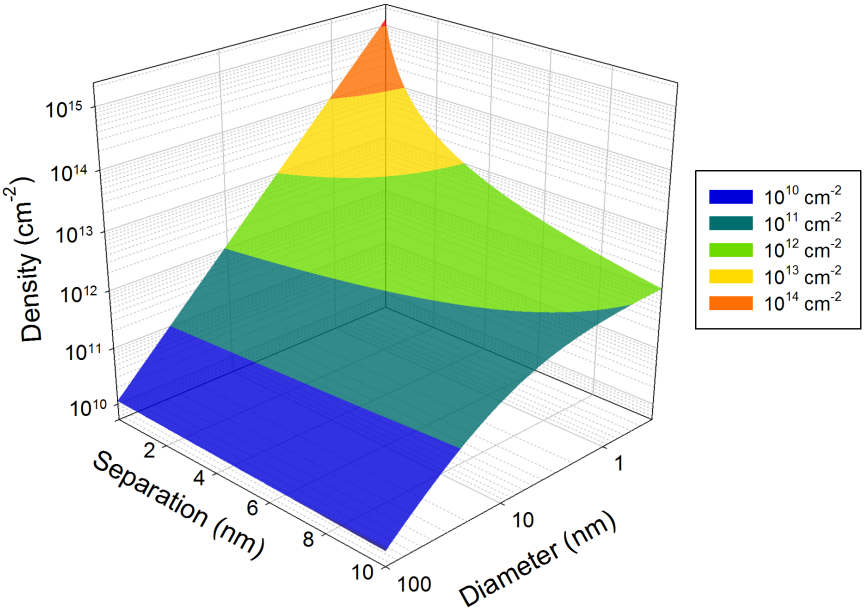


Figure 2.5: CNT density as predicted by the model against diameter and separation

However, the amount of tubes inside the bundle is not the most important value. As shown in the equations describing the quantum resistance, quantum capacitance and kinetic inductance of a bundle their value is determined by the product of the number of channels and the density. While the number of channels for a bundle of SWCNT would be $^2/_3$ on average (assuming a normal distribution of the chiral angle, resulting in $^1/_3$ of the tubes to be metallic), for MWCNT this number is dependent on the diameter of the tube and the number of walls, as shown in eqs. 2.5 and 2.6. The product of both, assuming $d_{in} = 0.5 d_{out}$, is shown in fig. 2.6. The amount of channels can be several orders of magnitude higher than the tube density for large MWCNT and flattens out around $7 \cdot 10^{12}$ channels/cm^2 for large diameter MWCNT.

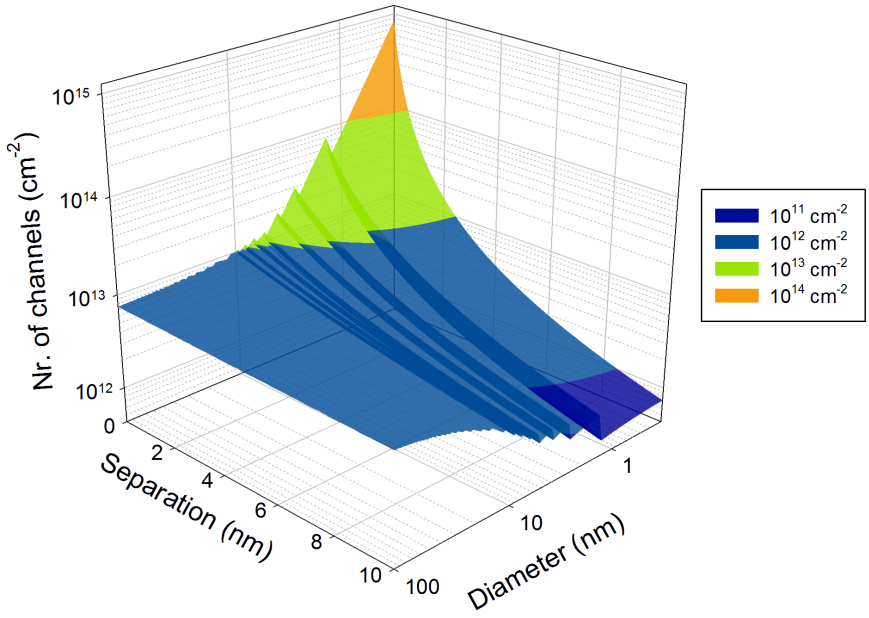


Figure 2.6: Calculated number of conductive channels of a CNT bundle as function of diameter and separation.

2.2.6 Minimum theoretical bundle resistivity

If CNT want to compete with current interconnect materials (e.g. Al, W, Cu) their resistivity should be within the same order of magnitude, preferably even lower. In fig. 2.7 the resistivity of a CNT bundle against its

number of channels per cm^2 is plotted using eq. 2.9, together with the bulk resistivity values of Cu, Al, and W. For these calculations it is assumed that the CNT are displaying ballistic conduction over their entire length, and have zero contact resistance. In this case the CNT resistivity will be length dependent due to its definition of $\rho = R \cdot A/l$, as longer tubes will have the same resistance as a short tube. Because of this the resistivity for a 0.1, 1 and, 10 μm long ballistic bundlea are shown in fig. 2.7.

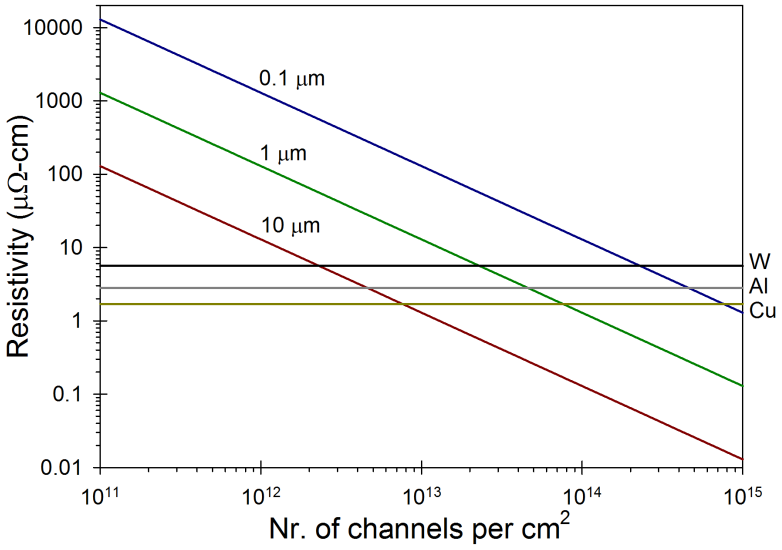


Figure 2.7: Minimum resistivity against nr. of channels for bundles with a different length. The MFP is assumed to be as long, or longer than, the bundle length.

From fig. 2.7 it can be concluded that for 100 nm bundles a channel density comparable to the maximum shown in fig. 2.6 would be required. For vertical interconnects in monolithic 3D ICs the length would be in the order of 2.5 μm. This means that in order to compete with Al, the currently used interconnect material, a channel density of at least $2 \cdot 10^{13}$ channels/cm^2 would be required. For SWCNT, which have on average $^2/_3$ channels, this would require a staggering density of $3 \cdot 10^{13}$ tubes/cm^2. DWCNT with $^4/_3$ channels, on the other hand, only require half of this density. For MWCNT it would be impossible to compete with Al for these lengths. Making the interconnects longer, while still remaining ballistic, relaxes the density requirement, but it is questionable if such long ballistic lengths could be achieved in practical situations. This clearly demonstrates that both density as quality

(MFP) will be key parameters in order to obtain a low via resistivity, and that it will be difficult to actually outperform current via metals in terms of electrical resistivity.

2.3 Thermal conductivity

As already mentioned in chapter 1 CNT have been shown to be excellent thermal conductors which is due to their strong sp^2 bonds. Heat in a material can be carried both by electrons and phonons, in metals the electron conduction normally dominates. In CNT, however, the phonon conduction dominates [59]. Just like graphite the in-plane conduction in CNT is about a thousand times larger than the out-of-plane conduction.

Simulations have shown that the theoretical (in-plane) thermal conductivity can be as high as 6,600 W/mK at room temperature for SWCNT [60]. Most data from measurements on the thermal conductivity of CNT is for individual single-walled or multi-walled tubes [10, 61–65], with reported values of over 3000 W/mK for both. For bundles of CNT on the other hand, which are required to obtain a low enough electrical and heat resistance [50], less data is available [66–70]. Moreover, the values for the thermal conductivity reported in the literature vary significantly, ranging from 50 to 5800 W/mK, and are generally one order of magnitude lower than those obtained from individual tubes.

The discrepancy between the different published values originates from differences in the Thermal Boundary Resistance (TBR), which can be high due to a difference between conduction mechanisms in the different materials (i.e. electron and phonon conduction of heat) [71]. Unfortunately, the TBR of CNT has so far been a hardly investigated subject, but the few publications available show that the impact of this resistance can be high and dominates the thermal performance [63, 71–73].

Defects can be another cause of the large spread in published values. Che et al. [74] calculated the influence of vacancies and so-called (5,7,7,5) or Stone-Wall defects where four hexagons are changed into two pentagons and two heptagons, which is a common defect in nanotubes. A vacancy concentration of 0.5 % already changed the thermal conductivity from 2980 W/mK to 700 W/mK. The effect of (5,7,7,5) is less severe. For a similar concentration of 0.5% the thermal conductivity becomes 800 W/mK. Yamamoto et al. [75] also mention the influence of defects and state that a vacancy concentration of 1% decreases the conductivity by 25%. Indeed, it has been shown that CNF, which are very defective, have a room temperature thermal conductivity of only 12 W/mk [63].

For CNT vias hardly any data on the thermal conductivity of such vias

is available. Simulations have shown that high thermal conductivity can be advantageous for the thermal management in IC [50]. Only work done by Horibe et al. [68] mentions the value of the thermal conductivity of CNT vias using the laser flash technique. They found it depended on the growth mode of the CNT (see also section 2.4.1), and reported a maximum value of 291 W/mK for base-growth CNT, and 49 W/mK for tip-growth CNT.

2.4 Depositing carbon nanotubes

2.4.1 Growth mechanism

Only growth by Chemical Vapour Deposition (CVD) is considered here, as laser ablation and arc-discharge are methods which operate at too high temperatures and don't allow direct integration on silicon substrates. CVD is a popular method in semiconductor industry to deposit all kind of layers from gas phase precursors. When growing CNT catalytic CVD is required, which implies that, besides the gas precursors and a form of energy, a catalyst nanoparticle is required. If those preconditions are met any kind of CVD, being plasma-enhanced, atmospheric pressure or low pressure, can potentially result in the growth of CNT.

As catalyst metals like Fe, Ni, Co, Pd, and Cu can be used. CNT can only nucleate from a nanoparticle. To form a dense array of nanoparticles usually a nm-thin catalyst film is deposited on a barrier layer, which breaks up into small particles upon heating by minimization of surface energy. It is also possible to deposit catalyst nanoparticles directly [76], or from a liquid or gas-phase [77, 78].

The catalyst particle will absorb the precursor (usually a hydrocarbon gas like CH_4 or C_2H_2) and dissociate the hydrogen. After this it is usually assumed that the carbon atoms diffuse by surface diffusion towards the CNT growth front [79], where it forms a CNT due to energy minimization. To prevent a surplus of carbon from poisoning the catalyst an etching gas like H_2 or NH_3 is added, which removes a-C [80]. After nucleation of the CNT has started, the catalyst can be either lifted from the surface by the CNT growing under it, dubbed tip growth, or remain at the surface due to strong interaction with the support layer, resulting in base growth.

The growth direction of the CNT is generally random, but can be altered by interactions of the tubes with their surrounding. Vertically aligned tubes are relatively easy to obtain when the density of the catalyst particles is sufficiently high to obtain self-alignment due to Van der Waals interaction between the tubes [81]. Another approach is to use an electric field (e.g. generated by a plasma) to force the CNT into (vertical) alignment [82].

Horizontal growth of CNT is generally more difficult. In literature several different approaches have been used including transfer techniques [83, 84], growth along crystal planes [85, 86], guidance by an electric field [87] and gas flow [88], and perpendicular growth on vertical surfaces [89, 90].

The different properties of CNT as mentioned in section 2.1 depend heavily on the fabrication conditions. The diameter of a CNT is strongly correlated with the catalyst nanoparticle, which in turns depends on the catalyst film thickness and support layer [91]. The length of the CNT depends generally on the growth time. For long growth times the catalyst can become inactive, which can be caused by covering of the catalyst with a-C, or a change to a chemically inactive state [92]. This results in a reduction in growth speed till the growth completely terminates.

The quality of a sample is generally strongly influenced by the growth temperature [93], with higher temperatures giving higher quality tubes. Plasmas usually have a negative impact on quality due to ion-bombardment [94]. Chirality control is at the time of writing still not achieved. A few publications exist in which a change from the usual $^2/_3$ semiconducting ratio was observed, but the mechanism behind this is still poorly understood [95–97].

A qualitative summary of the CNT properties and the influence of the growth parameters on them is displayed in table 2.1. The 'gas ratio' column shows the influence of the etching gas and the carbon feedstock. A '+' indicates that the properties are proportional, a '-' indicates the inverse. The 'O' indicates there is an optimum, 'X' for no influence, and an 'I' for inconclusive.

Table 2.1: Qualitative overview of properties vs. growth parameters, for an explanation of the symbols see the text

	Temperature	Pressure	Time	Gas ratio	Plasma power	Cat. thickness
Growth rate	+ [98] or O [99, 100]	+ [91]	+ [99]	O [99]	I [91, 101–103]	- [99]
Diameter	O [99, 104]	- [105]	O [104, 106]	- [100]	+ [107]	+ [91]
Quality	+ [93] or O [104]	O [108]	X or - [104]	+ [108] or O [91]	- [94, 103]	- [109]
Density	O [104, 110]	+ [105]	O [104, 106]	+ [100]	- [107, 111]	- [100]

2.4.2 Growth conditions

In this work CNT were grown using an AIXTRON Blackmagic CVD reactor. This reactor allows growth on samples with any size up to 100 mm wafers. The standard recipes available on this system proved to work for most process conditions required for CNT growth in this thesis. Unless otherwise specified the following recipes were used:

Low-Pressure Chemical Vapour Deposition (LPCVD)

Samples are loaded into the pre-heated chamber directly on the substrate holder. After this the system is pumped down to < 0.1 mbar. Once this pressure is reached 700 sccm of H_2 is allowed in the reactor, and the temperature and pressure are ramped to 500 °C and 80 mbar, respectively. Once these conditions have been met a 3 min pre-anneal is performed. Next the reactor is ramped to the growth temperature, after which 50 sccm of C_2H_2 is added. Once the selected growth time is reached, the gasses and heater are cut-off and the systems is pumped down. Finally, the reactor is cooled and purged using N_2 till the heater temperature is below 400 °C. In case the growth temperature is below 500 °C both pre-anneal and growth are performed at the same temperature, but the pre-anneal is extended to 5 min for 400 °C and 8 min for 350 °C.

Plasma-Enhanced Chemical Vapour Deposition (PECVD)
Similar loading conditions are used as with the LPCVD recipe. The sample is heated up to 550 °C at 9 mbar while 400 sccm H_2 is flowing. This is followed by the ignition of a 100 W pulsed-DC plasma, H_2 is increased to 700 sccm, and the temperature is ramped up to the growth temperature. After this temperature has been reached 20 sccm of C_2H_2 is added for the specific growth time. The remainder of the process is similar to that of the LPCVD recipe.

2.5 Conclusion

The electric model for a CNT bundle was discussed. Most quantum effects are neglectable for typical via applications, which results in only the quantum resistance, contact resistance and electrostatic capacitance influencing the CNT performance. Using hexagonal packing the density of a CNT bundle can be estimated from the diameter and spacing between the tubes. From this the resistivity of CNT bundles with different lengths was calculated. For practical monolithic 3D IC via applications with a length of 1 μm and equal MFP the required density to compete with Al was found to be in the order of $2 \cdot 10^{13}$ channels/cm^2, which can only be obtained by SWCNT or DWCNT with packing densities of respectively $3 \cdot 10^{13}$ tubes/cm^2 and $1.5 \cdot 10^{13}$ tubes/cm^2.

The thermal conductivity of CNT can theoretically be as high as 6600 W/mK, and values well over 3000 W/mK have been measured. There exists a large spread in values found in literature, caused by differences in the TBR between the interface and the CNT and the quality of the material. The chapter concluded with a short introduction into CNT growth, and the impact of growth parameters on the properties of CNT.

3

Investigating quality using Raman spectroscopy

In this chapter a systematic study on the impact of growth temperature on the crystallinity (quality) of multi-walled carbon nanotubes and carbon nanofibres is presented. First the growth results obtained using scanning electron and transmission electron microscopy are discussed. This is followed by an explanation of the different Raman active bands, and the procedures on fitting those bands to extract the data. The extracted data is plotted against temperature, and the response of the different intensity ratios and band widths are compared to results from literature. An empirical equation from literature is presented which relates the Raman spectra to the crystalline size. From the results recommendations are made on which bands can be used to determine the crystallinity of a CNT sample. Finally, a method to detect the growth method of the CNT from the Raman data is presented.

3.1 Introduction

As was discussed in chapter 2 the quality, or crystallinity, of a CNT is an important aspect which influences its electrical and thermal properties. TEM is often used to investigate the crystal structure of CNT, but is time-consuming and expensive. Another approach is the use of Raman spectroscopy, which relies on the inelastic scattering of monochromatic light (Raman scattering). The light (usually emitted by a laser) interacts with phonons or other excitations in the sample, which results in the photon energy of the laser to be shifted up or down. Using a filter to remove the laser energy and a detector the spectrum of the Raman scattered light can be obtained. The location of the peaks, and their Full Width at Half Maximum (FWHM) gives information on the vibrational modes in the sample.

Raman spectroscopy has become a popular tool to investigate all kind of properties of CNT. For SWCNT Raman spectroscopy has been used as an alternative method to assess the diameter and chirality of single-walled nanotubes [112,113]. Another often used application of Raman spectroscopy is to determine the quality of both SWCNT and MWCNT, as well as CNF [114]. The big advantages of Raman spectroscopy (over TEM) are that it is very fast (measurements generally take just tens of seconds to a few minutes), non-destructive and relatively inexpensive. For determining the quality another advantage is that it gives a quantitative outcome, while TEM is a more qualitative approach.

To determine the crystal quality using Raman spectroscopy the vast majority of publications simply use the intensity ratio between the so-called D-band (defect related, around 1350 cm^{-1}) and G-band (Raman active mode of graphitic materials at 1582 cm^{-1}), see fig. 3.4 for an example of a Raman spectrum. Already in 1970 Tuinstra and Koenig showed that this ratio is related to the graphite in-plane crystallite length L_a [115].

However, using only this specific quantity limits the reliability of the measurement. From research on the Raman spectra of disordered and amorphous carbon it is known that the I_D/I_G ratio can have an optimum when plotted against the crystalline length [116,117] or distance between defects for point-like defects [118]. For samples with small crystalline lengths an increasing crystallinity increases the probability of finding six-fold rings in the material, which are required together with defects for the D-band and thus increases the magnitude of this band. At a certain point the number of six-fold rings is roughly constant, and the number of defects per unit area decreases, which causes a reduction of the D band magnitude for increasing crystallinity. Care should thus be taken when only an I_D/I_G ratio is mentioned, without specifying the overall crystallinity of the samples.

From research on Raman spectra of graphite and carbon nanotubes it has been shown that several other Raman bands are sensitive to the crystallinity of the graphite layers [109, 119, 120]. Among these are the second defect related first-order band D', and the second-order overtones (i.e. 2D, D+G and 2D'). Unfortunately, not many publications investigate the second-order bands and most available research is on other graphite based materials beside CNT. Furthermore, most research performed on the crystallinity of graphitic materials with Raman spectroscopy is either on samples treated with high temperature thermal annealing in order to improve the crystallinity [117, 120–126] or introduce damage to lower it [116, 118, 122, 127]. Few publications exist in which CNT are grown using CVD at different temperatures and systematically investigated using Raman spectroscopy, and those that exist are fabricated at high temperatures (> 800 °C) [93, 104].

In this chapter the results of a systematic investigation on the first and second-order Raman bands of both MWCNT and CNF produced under the same CVD conditions, while only varying the relative low (500-750 °C) growth temperature are discussed. Both the different intensity ratios and band widths against temperature were investigated with two different laser wavelengths. From this it is determined which Raman bands are most suitable to analyse the crystal quality of CNT and CNF. This is followed by a discussion on how the crystallite length can be determined from the Raman spectrum. Finally, a way to use Raman spectroscopy to determine the growth method of the CNT is presented.

3.2 Sample preparation

As catalyst to create the CNT 3 nm thick Fe was used, and for the CNF 6 nm of Ni, both evaporated with an e-beam evaporator. As substrate p-type 100 mm Si (100) wafers were used. To prevent diffusion of the metal catalyst into the substrate an e-beam evaporated Ti barrier layer of 10 nm and thermal oxide of 100 nm were deposited on the substrate for Fe and Ni, respectively.

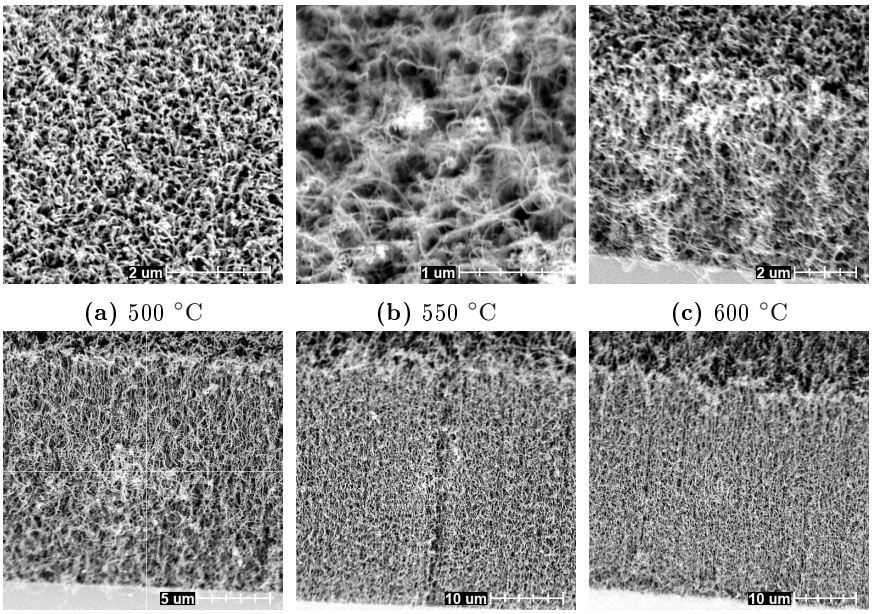
The samples with Fe as catalyst used the standard LPCVD recipe as discussed in section 2.4.2, with a growth time of 5 min, and a growth temperature ranging from 500 to 750 °C. The samples using Ni as catalyst were exposed to the standard PECVD recipe with a growth time of 20 min and temperature ranging from 550-750 °C.

For the Raman characterization the in-house Renishaw inVia system with two selectable lasers, one red HeNe laser of 633 nm and a green Ar^+ laser of 514 nm, was employed. Three measurements from each sample were

gathered under identical conditions and fitted using Matlab. The average of the resulting band data from the three separate measurements were used to gain accuracy. The fitting details will be discussed in section 3.4.

3.3 Measurement results

In LPCVD mode MWCNT could be grown at temperatures ranging from 500 to 750 °C, with steps of 50 °C. Fig. 3.1 displays the Scanning Electron Microscope (SEM) images taken from MWCNT grown with 3 nm Fe. The samples displayed random growth at 500 °C and 550 °C, and aligned growth at higher temperatures. The growth rate depends on the temperature, going from less than one μm/min at low temperature to several μm/min at 750 °C. For all aligned samples the density is in the order of $10^{10} - 10^{11}$ tubes/cm^2.



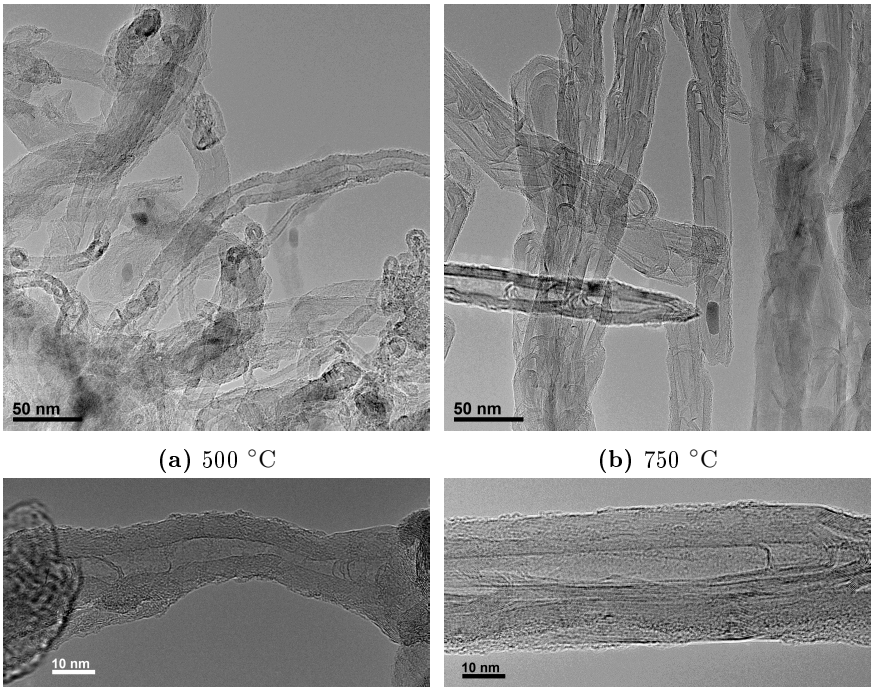
(a) 500 °C **(b)** 550 °C **(c)** 600 °C

(d) 650 °C **(e)** 700 °C **(f)** 750 °C

Figure 3.1: SEM images of MWCNT grown using 3 nm Fe at different temperatures

Using TEM the diameter of the tubes at different temperatures could more accurately be determined. At 500 °C most tubes have a diameter between 20-30 nm and some 10 nm tubes are observed. When tempera-

ture is increased to 650 °C the diameter of the tubes increases to 30-50 nm. Again some small 10 nm tubes were observed. At the highest temperature of 750 °C the diameter range doesn't differ from 650 °C. In fig. 3.2 TEM images taken from samples at 500 and 750 °C can be found. At low temperature the CNT walls display many bending and bamboo defects (fig. 3.2a-c). At higher temperature the bending disappears, suggesting an increase in graphite in-plane ordering, although still many bamboo defects are visible (fig. 3.2b-d).



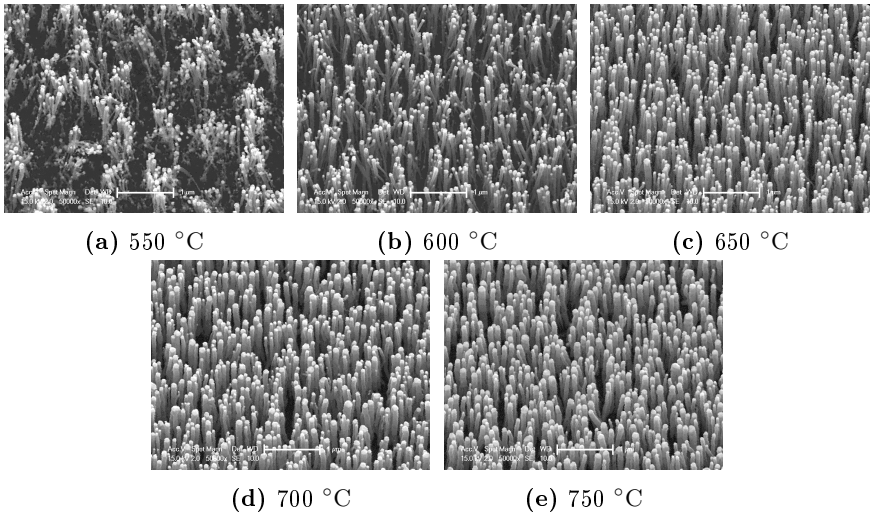
(a) 500 °C **(b)** 750 °C

(c) 500 °C, high magnification **(d)** 750 °C, high magnification

Figure 3.2: TEM images of MWCNT grown using 3 nm Fe at 500 and 750 °C

In PECVD mode CNF were deposited between 550-750 °C, again with steps of 50 °C. Fig. 3.3 displays the obtained SEM images for different temperatures. The vertical alignment and apparent quality of CNF are inferior at 550 °C, but improve when the growth temperature is increased. The diameter increases slightly with increasing growth temperature, from 30-90 nm at 550 °C to 60-140 nm at 750 °C. This is most likely caused

by Ni forming larger nanoparticles when the atoms become more mobile at higher temperature [99]. The length of the fibres is about 700 nm, while the maximum observed density is in the order of 10^9 fibres/cm^2.



(a) 550 °C **(b)** 600 °C **(c)** 650 °C

(d) 700 °C **(e)** 750 °C

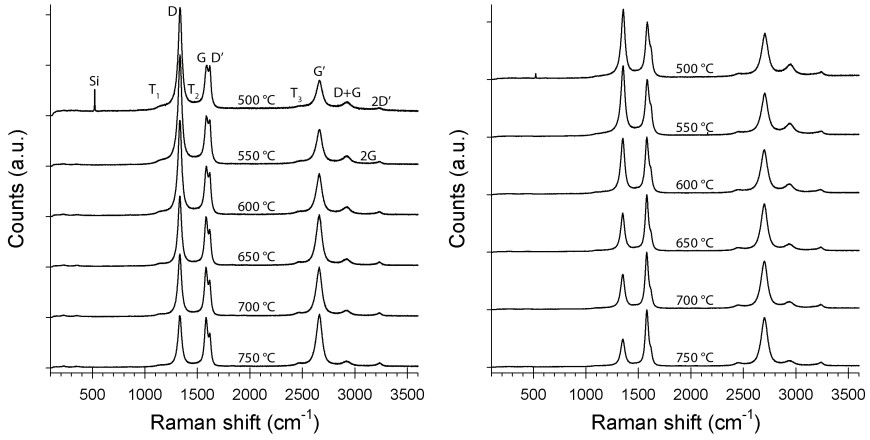
Figure 3.3: SEM images of CNF grown using 6 nm Ni at different temperatures, scale bar is 1 μm for all images

The Raman spectra obtained from MWCNT are shown in fig. 3.4. In the first-order region two strong bands can be observed for both laser wavelengths. The before mentioned D band is sited around 1330 and 1350 cm^{-1}, for respectively the red and green laser. The difference is caused by the dispersion of the D-band [113]. This band originates from inter-valley double resonance elastic phonon scattering with a defect, close to the K point of the Brillouin zone (BZ) [128, 129]. Around 1582 cm^{-1} the G-band can be found, which in contrast to the D-band has no dispersive behaviour. Finally a third weaker band can be observed, which is named D'. For the spectra obtained with the red laser this peak is clearly visible at 1617 cm^{-1}, when a green laser is used the band is visible as a shoulder of the G-band. This band is also disorder induced, but this time by a intra-valley double resonance elastic phonon scattering process around the Γ point in the BZ [128]. The band is reported to be weakly dispersive ($\sim$ 10 cm^{-1}eV^{-1}) [124], but due to the small difference in laser energy and the appearance as shoulder this is difficult to observe for these samples.

In the second-order region a single sharp band, and several weaker ones can be observed. The strong dispersive band around 2660/2700 cm^{-1}

(red/green laser) is designated as the G' band (sometimes called 2D). This band is caused by a double resonance effect similar to the D band, but now caused by two inelastic phonon scattering processes [129]. Thus, no defects are necessary for this band: it is also observed in high-quality graphitic materials [113].

Weak second-order bands around 2469/2452 cm^{-1}, 2920/2940 cm^{-1}, 3180 cm^{-1} (too weak to accurately measure dispersion, see fig. 3.6b for a magnification) and 3233/3237 cm^{-1} can be observed. The exact origin of the peak around 2450 cm^{-1} is still unknown. According to Shimada et al. [130] this band is related to 2LO second-order scattering, showing no dispersion. Tan et al. explain the origin of the band to be a combined overtone of the D band and the modulation around 1100 cm^{-1}, displaying a negative dispersion [131, 132]. From now on this band will be referred to as T_3. The strongest weak band at 2920/2940 cm^{-1} is the combined overtone of the D and G band, called D+G (or D") [120, 122, 133]. The band around 3180 cm^{-1} is attributed to the overtone of the G band (2G) [113, 133]. Finally, the band around 3233 cm^{-1} is explained as being an overtone of the D' band (2D') [120, 122, 133].



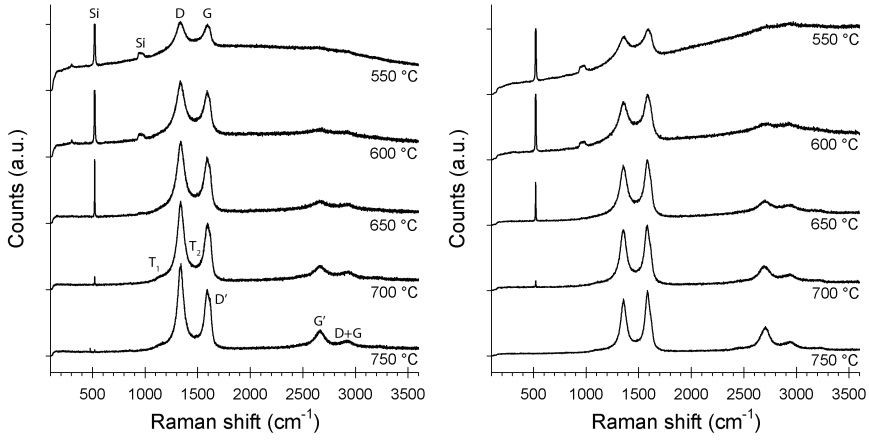
(a) 633 nm laser **(b)** 514 nm laser

Figure 3.4: Raman spectra of MWCNT grown with 3 nm Fe, normalized to the G band intensity

Fig. 3.5 shows the Raman spectra obtained for the CNF. A strong baseline is present in the low temperature spectra, which is more profound when the 514 nm laser is used. Furthermore, wide D and G bands are visible, which become sharper for higher temperatures. The G-band is sited around

1590 and 1600 cm^{-1} for the red and green wavelength laser, respectively. Normally this band is expected at 1582 cm^{-1}, the reason for this apparent shift is the strong influence of the D' band.

At low temperature a wide modulated bump can be detected in the high wavenumber region where the second-order Raman bands are to be expected. At higher temperatures weak G' and D+G bands are visible. Unfortunately, the other second-order bands which could be found in the MWCNT samples are not strong enough to be clearly observed in the CNF samples. The bands in the low wavenumber region around 520 and 1000 cm^{-1} are caused by the Si substrate, and are only visible for samples with low CNF density.



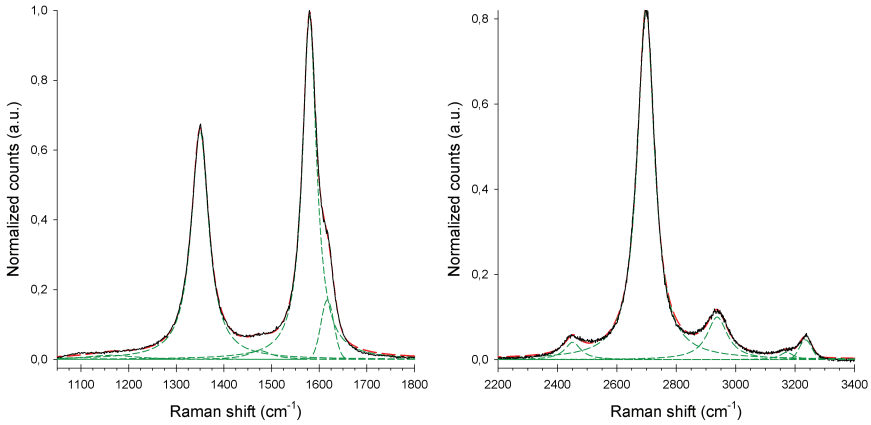
(a) 633 nm laser **(b)** 514 nm laser

Figure 3.5: Raman spectra of CNF grown with 6 nm Ni, normalized to the G band intensity

3.4 Curve fitting

In order to determine the location, magnitude and width of the different Raman bands in fig. 3.4 and 3.5 the spectra are fitted using the non-linear least squares curve fitting routines of Matlab. Eight Lorentzian curves and two Gaussians are used for fitting to obtain the Raman band information of the MWCNT sample. Beside the bands mentioned in the previous section two more around 1100 and 1500 cm^{-1} are added , which gave a more accurate fit as suggested by Ferrari and Robertson [116]. The band around 1100

cm^{-1} has also been observed by several other groups [132, 133]. The bands around 1100 and 1500 cm^{-1} will be referred to as T_1 and T_2, respectively, for simplicity. It was found that a Lorentzian overestimates the higher wavenumber side of the combined G and D' band. A Gaussian proved to give superior fitting for the D' band, and for its overtone, and is also used by others to fit the D' peak [119]. Thus, a total of 4 Lorentzians and a single Gaussian are used to fit the curve around the D and G bands, and the same number is used to fit the observed second-order bands. A small linear baseline is present in the MWCNT spectra, which is removed prior to the fitting using an appropriate fit to the flat areas of the spectrum.



(a) First-order bands **(b)** Second-order bands

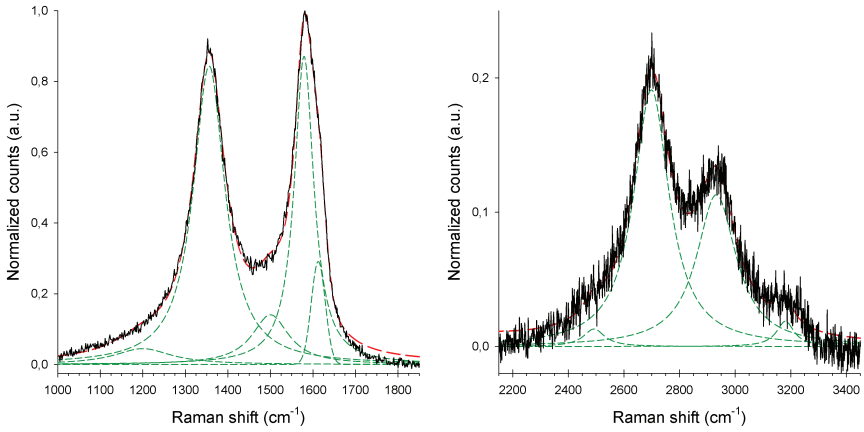
Figure 3.6: Fitted Raman spectra of CNT grown on 3 nm Fe at 650 °C. Original spectrum: solid line; fitting peaks: short dashed line (green); total fitting curve: long dashed line (red)

Fig. 3.6 displays the original Raman spectrum of MWCNT grown with 3 nm of Fe at 650 °C (with the linear baseline removed), together with the curves used to fit the bands (green short dashed lines) and the total fitting curve (red long dashed line). Fig. 3.6a shows that the combined four Lorentzians and single Gaussian fit this part of the spectrum very well. From fig. 3.6b it can be observed the curves fit the second-order bands almost perfectly.

While fitting the Raman spectra of the MWCNT gave accurate results, fitting the CNF data proved to be more cumbersome. From fig. 3.5 it becomes clear that several potential problems arise. First of all there is a strong non-linear baseline present for the low temperature samples, which

becomes linear when temperature is increased. To remove this baseline a high-order polynomial fit was used instead of a linear. Second, at low temperature the second-order bands are hardly visible and appear as a modulated bump. Therefore, only the strong second-order G' and D+G bands will be discussed in case the fitting was reliable, for all other second order bands no reliable fit could be made.

In fig. 3.7a the same approach for fitting the first-order region as with the MWCNT samples is used. Although this gives a good fit, T_1 and T_2 now become more significant. The problem is that these bands are poorly defined, thus the exact wavenumber at which they appear is unknown (this is especially true for the modulation around 1500 cm^{-1}) [116]. Some freedom is given to these bands to allow accurate fitting. For the MWCNT samples setting the boundary conditions did not influence the resulting fit, however, in case of the CNF samples T_1 and T_2 tend to stick to one of the boundary conditions. Giving the bands more freedom to move around has a large impact on the stronger D and G band, making the outcome of the fit inaccurate. A more accurate range of wavenumbers in which T_1 and T_2 should be found would thus allow for more accurate fitting.



(a) First-order bands of CNF fit **(b)** Second-order bands of CNF fit

Figure 3.7: Fitted Raman spectra of CNF grown on 6 nm Ni at 650 °C. Original spectrum: solid line; fitting peaks: short dashed line (green); total fitting curve: long dashed line (red)

Fig. 3.7b displays the fit of the second-order region using 4 Lorentzians. The band around 2450 cm^{-1} and the 2D' band are very weak, they hardly influence the fitting of the two more intense G' and D+G bands. A reason-

able fit of these two larger bands is still possible with samples created at 600 °C and higher. The 2G band is not included during fitting as it is too weak, even for the highest quality CNF samples.

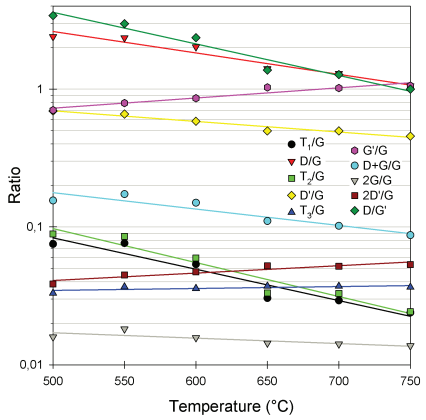
3.5 Fitting results for multi-walled nanotubes

It is commonly assumed in literature (e.g. [93]) that when growth temperature is increased the crystallinity of the samples increases as defects are annealed out. The TEM images (fig. 3.2) confirm this behaviour. Although bamboo defects remain present at higher temperature, the bending of the MWCNT walls decreases suggesting a higher degree of ordering. It can thus be expected that the Raman bands related to defects decrease in magnitude, as the number of defects is decreasing. Something which can already be seen without fitting from the obtained spectra in fig. 3.4.

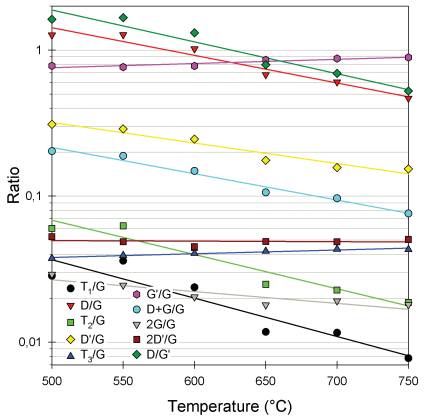
However, beside a change in quality the diameter distribution of these tubes changes slightly, from 20-30 nm to 30-50 nm with always a few 10 nm tubes present. From the TEM images obtained no change in diameter is observed between 650 and 750 °C. It is known from literature that CNT catalyst nanoparticle size [109] and MWCNT diameter [126] can influence the Raman bands. Both papers demonstrate a decrease in defect related bands for increasing diameter. The decrease in tube curvature is likely the cause of this.

Unfortunately, the work of Antunes et al. [109] only relates the band changes to the catalyst nanoparticle diameter distribution used to grow the CNT. It is know that there is a correlation between particle size and CNT diameter (e.g. [91]), but it depends on the process used how big the actual CNT will become. The work of Bokova et al. [126] directly relates the Raman spectra to the MWCNT tube diameter, but their diameter range is only from 5.5-20 nm. It is thus unclear if the decrease in defect related features continues for large diameter tubes, or perhaps flattens out as tube curvature effects become less for large tube diameters. For the low temperature samples (till 650 °C) an additional decrease of the defect related Raman features when temperature increases could be expected, if the diameter related changes are in the same order as the changes caused by an improvement in crystallinity.

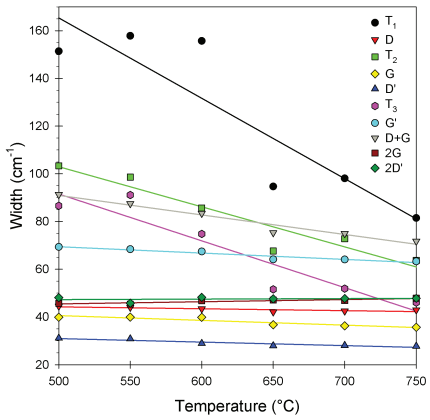
Fig. 3.8 displays the band intensity ratios and FWHM obtained from the MWCNT samples. First the band ratios versus temperature are discussed, followed by the FWHM.



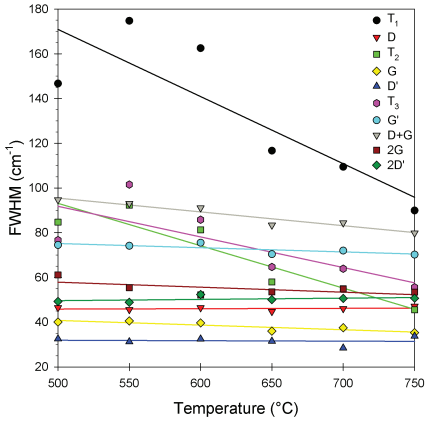
(a) Raman band intensity ratios, 633 nm laser



(b) Raman band intensity ratios, 514 nm laser



(c) FWHM of Raman bands, 633 nm laser



(d) FWHM of Raman bands, 514 nm laser

Figure 3.8: Results obtained from fitting the Raman spectra of MWCNT grown with 3 nm Fe at different temperatures

3.5.1 Band intensity ratios

The band intensity ratios from the first-order region can be found in fig. 3.8a-b. It is known that D and D' are sensitive to disorder [109, 121, 125]. The effects of quality on the first-order spectra of graphite based materials has been extensively researched, and these results confirm the general

finding that the I_D/I_G and $I_{D'}/I_G$ intensities decrease for increasing crystallinity. As the samples can be fitted with a linear line versus temperature over the whole range, there is no indication that the increase in tube diameter for the low temperature samples has a measurable impact on the Raman bands. It can thus be concluded that the changes observed in the MWCNT Raman spectra are dominated by an improvement in crystallinity of the samples.

To my knowledge no publications mention the impact of crystallinity on T_1 and T_2. As mentioned before Tan et al. observed a clear band in the vicinity of T_1 [131, 132]. However, the frequency they observe the band is 1084 cm^{-1} and 1130 cm^{-1} for a laser with a wavelength of 514 nm and 633 nm, respectively. The model fits the band around 1160 cm^{-1}, independent of laser wavelength. Forcing the band towards the frequencies reported by Tan et al. deteriorates the accuracy of the fit. Saito et al. [129] tentatively assigned the bands between 1000-1200 cm^{-1} to the LA and and iTA phonon branches around 3K/4 and K, respectively, caused by a double resonance Raman process. As this process needs elastic scattering with a defect, this matches with the observation of a decreasing intensity for samples with increased crystallinity. They also assigned the band at 1480 cm^{-1} to a double resonance process with the iTO phonon branch. The model fits this band between 1470-1480 cm^{-1} (T_2), which again decreases with increasing crystallinity. Kawashima and Katagiri also observed a band in this region, with similar frequency for the green laser [133]. However, they observed a large dispersion for this band, which is not visible in these results. The double resonance process discussed by Saito et al. doesn't predict a large dispersion for this band either.

Next the second-order band region is discussed, which is less often investigated compared to the first-order region. The $I_{G'}/I_G$ ratio increases for increasing crystallinity, as was observed by others [109, 120]. This band is found to be highly sensitive to the crystalline structure, and also appears in Highly-Oriented Pyrolytic Graphite (HOPG), approaching the intensity of the G-band [113].

The other bands in the second-order spectrum of MWCNT are hardly investigated with respect to sample crystallinity. In these results the D+G overtone shows a decrease with crystallinity, which was also found by Chieu et al. [121] and Hishiyama et al. [127]. Interesting enough Lee [120] found an increase in I_{D+G}/I_G for increasing crystallinity. On the other hand Antunes et al. [119] found that the D+G intensity followed a trend similar to the D band, which is also the case for these results. It could be that the differences in literature are caused by the type of material investigated. Antunes, Chieu and Hishiyama et al. all investigated materials of relative high quality, just

like the MWCNT grown in this study. The material investigated by Lee was made from low quality cellulose which undergone a thermal treatment but are not graphitizable. The absence of the D+G band in HOPG (e.g. [127]) supports the theory that the D+G band is disorder induced and reduces for increasing crystallinity.

For the three weakest second-order features no big changes can be observed. The T_3 band displays a slight intensity increase. As the changes are minimal, it can be concluded that this band is more or less insensitive to disorder. This was also observed by Antunes et al. [119], who found no significant change of this band intensity for different kind of samples with different crystallinity. Again this band is also found in HOPG [127]. A small dispersion of this band was observed: going from ~ 2452 cm^{-1} at 514 nm to ~ 2469 cm^{-1} at 633 nm, equivalent to a dispersion of -37 dω/dE_L. This is close to the value found by Tan et al. [132].

No data is available in literature on the impact of crystallinity on the 2G band. This band showed a slight decline in intensity. However, as the band is weak it is believed that this change is more likely caused by fitting inaccuracy, and the intensity is thus insensitive to the change in crystallinity in these samples.

For the last second-order band, 2D', a small increase in intensity can be observed for increasing growth temperature. This is consistent with results from Chieu et al. [121] and Hishiyama et al. [127]. This band is also observed in HOPG as a strong and sharp band [133]. Interestingly, the rate of change against temperature of $I_{2D'}/I_G$ for the red laser is equal to that of $I_{G'}/I_G$. This effect was also seen for samples grown recently at different catalyst thickness's (not shown here). I suggest that this band is caused by a two phonon intra-valley double resonance process, just like G', but around the Γ point of the BZ as it is a D' overtone. This would explain the presence of this band in HOPG, and the similar increase in intensity as $I_{G'}/I_G$.

$I_D/I_{G'}$ is added, as suggested by Musso et al. [134], where they found that this ratio shows a decline while I_D/I_G remained constant. This ratio shows the strongest sensitivity to the crystallinity of the material in these results when the red laser was used, which is to be expected as it combines the increase in G' band intensity with the decrease in D band intensity. For the spectra obtained using the green laser the observed change in G' is smaller, and hence the sensitivity of $I_D/I_{G'}$.

When the ratios obtained for the different laser wavelengths are compared no large differences in trends can be observed. The only big difference is the magnitude of the ratios, which is considerably larger when a longer wavelength laser is used. It has been shown before that the D band intensity is sensitive to the laser wavelength [119, 122, 125]. Sato et al. [125]

investigated the dependency of the D band versus the laser wavelength and found that their theoretical model for the double resonance Raman scattering could confirm this dependency. It thus seems to be a inherent property of the double resonance process, as also T_1, T_2 and D' displays this behaviour, which all can be linked to single phonon double resonance defect scattering processes [129]. Interestingly, the magnitudes of the second-order bands compared to the G-band are all much less sensitive to the laser wavelength, compared to the large increase in intensity ratios for the single phonon double resonance processes. This suggests that the two phonon double resonance intensity is less sensitive to laser wavelength.

3.5.2 Band widths

Next the FWHM of the different Raman bands will be investigated, as displayed in fig. 3.8c-d. First of all, it should be noted that no large changes are observed between the FWHM magnitude for different laser wavelengths, in contrast to the ratios. For the bands in the first-order region T_1, T_2 and G show a clear decline, while the D and D' band are almost constant. Although decreasing D and D' band widths are commonly reported for increasing crystallinity [109,117,120,121,135] the fact that only the G band showed a decline is uncommon. Antunes et al. [109] attributed an increase in the width of the D peak to spreading in the defect domain size and discussed that the width of the G band could be related to the graphite domain size. Chieu et al. [121] discussed that samples with long range order can show small changes in the D and G band widths, but still a large change in intensity ratios for increasing crystallinity. This suggests the samples have long range order and at higher temperature less defects are present in the MWCNT, but with similar domain size.

For the second-order region T_3 displays the largest decline with temperature. Unfortunately, no data on the FWHM of this band is available in literature. If this band is indeed caused by the overtone of T_1 and D, the observed decline in width found here matches the behaviour of FWHM(T_1). For the other bands G' and D+G show a decline, while 2G and 2D' are more or less stable. The latter two are also rather weak, thus the inaccuracy in fitting is expected to be larger. Very few publications discuss the relation between second-order band width and crystallinity. Lee noted that the FWHM of the G'and D+G band show a steep decline for increasing crystallinity [120].

Although the G' band has been associated with the dimensionality in structural ordering of the material and can have multiple peaks, only a single G' band was observed. This is similar to results from Antunes et

al. which they related to 2D graphite dimensionality [109]. Similar to their results FWHM(G') is about twice FWHM(G), and displays the same trend. Other publications confirmed a decline in the band width for increasing graphite crystallinity [120, 121]. T_3, G' and 2D' all appear as sharp bands in HOPG [127, 133].

3.6 Fitting results for carbon nanofibres

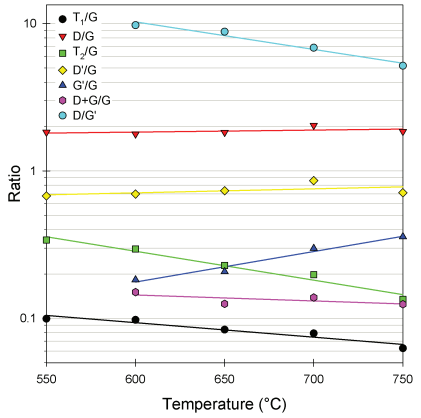
For the CNF the fitting results obtained from the Raman spectra measured from samples grown at different temperatures are displayed in fig. 3.9. As mentioned before the T_3, 2G and 2D' bands are ignored as they cannot be fitted with sufficient accuracy. For $I_{G'}/I_G$ and I_{D+G}/I_G only the data points from the spectra of which the bands are clearly visible are displayed (i.e. the second-order bands when only a modulation is visible are ignored). Again $I_D/I_{G'}$ was added.

It is expected that at higher fabrication temperatures the crystallinity of the samples improves. Compared to the MWCNT the quality will be much less, as CNF normally have a herringbone structure with no long graphite sheets along the fibre axis. The diameter of the, already large, CNF increases considerable with increases growth temperature. As far as I am aware no Raman data has been published relating the CNF diameter to a change in Raman bands. As diameter is already large and CNF have no long graphite planes along their axis it is not expected that the diameter increase has a large influence.

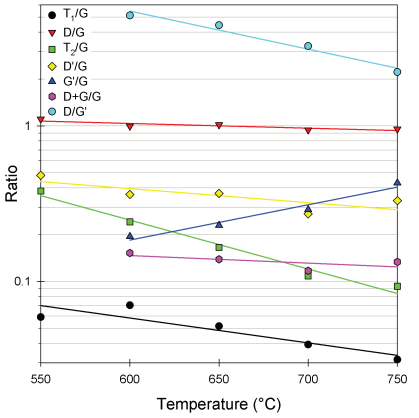
An interesting effect can be observed for $I_D/I_G$and $I_{D'}/I_G$. While for the red laser both lines show a slight increase versus temperature the spectra obtained with the green laser display a decline. Again $I_{D'}/I_G$ follows the same trend as I_D/I_G for both laser wavelengths, just as with the MWCNT samples. The second order band intensity ratios display a unambiguous behaviour, on the other hand. The $I_{G'}/I_G$ ratio increases, while I_{D+G}/I_G decreases.

As can be seen from both the ratio as FWHM of T_2 this band is much stronger compared to the MWCNT samples, especially for the low temperature samples. It is worth nothing that T_1, while decreasing in intensity, actually increases in width. It is assumed that the inaccuracy in fitting the, especially low temperature (550-650 °C), samples makes the model fitting of the G band unreliable.

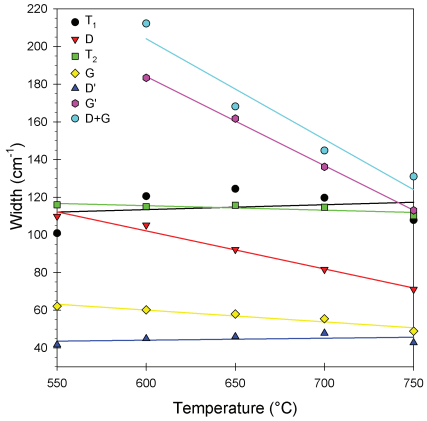
From these results can be concluded that the CNF samples have very short ordering lengths (L_a) and are likely close to the optimum of the I_D/I_G ratio versus L_a as observed by others [116–118]. Just like the results of Zickler et al. [117] using pyrolized wood and Cançado et al. using ion



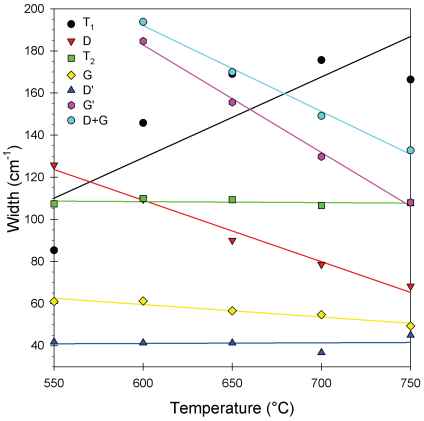
(a) Raman band intensity ratios, 633 nm laser



(b) Raman band intensity ratios, 514 nm laser



(c) FWHM of Raman bands, 633 nm laser



(d) FWHM of Raman bands, 514 nm laser

Figure 3.9: Results obtained from fitting the Raman spectra of CNF grown with 6 nm Ni at different temperatures

bombarded graphene [118] I_D/I_G remains constant, while the FWHM of both D and G decreases. Their results suggest the L_a of these CNF samples is 2-3 nm and only increases a few nm with increasing growth temperature. The large amount of damage in the samples, even at higher temperature, is likely caused by ion bombardment of the sample, which is known to cause damage [103].

3.7 Determining the nanotube quality using Raman spectroscopy

The goal of this research was to investigate which Raman bands can be used to assess the quality of fabricated MWCNT and CNF. This can be useful for determining the impact of different process steps on CNT quality or for growth recipe optimization. As was already shown in section 3.5 for MWCNT the approach used in literature (i.e. using the I_D/I_G ratio) can be sufficient, and for smaller changes the D', G' and D+G band ratios (compared to G) can be added as they display a clear relation to changes in crystallinity. Another possibility is to use the $I_D/I_{G'}$ ratio as suggested by Musso et al. [134]. Although the weakest second-order bands in some cases display a clear growth temperature dependency it is not recommended to use them as they're more prone to fitting inaccuracy. Finally, the same laser wavelength should be used for all samples, as the intensity ratios of the defect related bands (especially the first order bands) depend heavily on laser wavelength. Larger changes can be expected when a longer wavelength laser is used.

Now the question arises: how can what is happening to the crystallinity of the low quality CNF samples be predicted, as the I_D/I_G ratio can show both an increase as decrease for increasing quality? One solution could be to use the second-order bands, if they are clear enough to be observed. For all samples and wavelengths $I_{G'}/I_G$ showed an increase, while I_{D+G}/I_G showed a decline for increasing temperature. As discussed before an increasing $I_{G'}/I_G$ is associated with an increase in crystal ordering [109,120]. A decreasing I_{D+G}/I_G is also observed for increasing crystallinity [121,127], although the inverse has also been observed [120]. In case of a large uncertainty in fitting, the G band the $I_D/I_{G'}$ ratio can be an alternative. Unfortunately, it is difficult to fit the second-order bands for the samples with very low crystallinity as they appear as a modulation only.

The second option is to look at the FWHM of the D and G band. Zickler et al. found that both the D and G band show a decline when the crystallinity increases for samples with short L_a, while I_D/I_G showed a maximum over the same crystallinity range [117]. Just like Ferrari and Robertson [116], they conclude that the relation between the in-plane graphite crystalline size L_a and I_D/I_G found by Tuinstra and Koenig [115] should be taken with caution for samples with low crystallinity. Unfortunately, no empirical relation between the FWHM of the D and/or G band and the crystallinity is known, but it is clear that a decline demonstrates an improve in crystallinity for samples with short L_a.

In case the D and G band can be fitted with sufficient accuracy, and

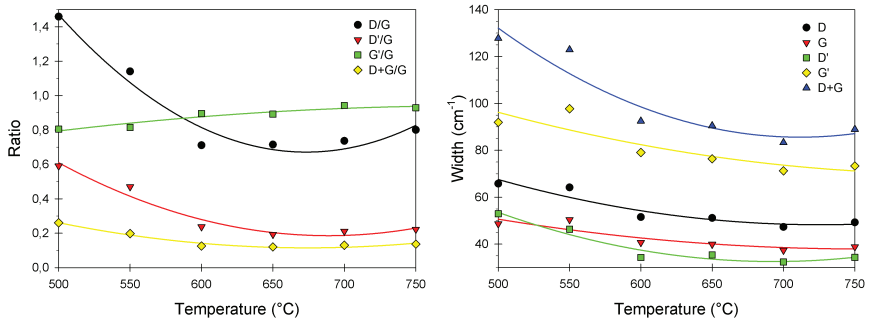
the sample are of high enough quality (I_D/I_G decreases for increasing quality) the in-plane ordering length L_a can be determined using an empirical equation [115, 116, 136]:

$$L_a(\text{nm}) = C(\lambda)\frac{I(G)}{I(D)} \tag{3.1}$$

where $C(\lambda)$ is approximately 4.4 nm for a laser wavelength of 515.5 nm. A more general equation which can be used for different wavelengths has been developed by Cançado et al. [137], however this equation uses the integrated intensity area ratio instead of the peak intensity ratio.

3.8 Detecting the CNT growth method using Raman spectroscopy

In these samples the MWCNT created with Fe grow using the root growth mechanism, while the CNF grown with Ni display a tip growth mechanism. It was found that it is possible to use Raman spectroscopy to distinguish between these two growth modes, if the MWCNT show vertical alignment. Raman spectroscopy only probes the structure within the optical skin depth of the laser wavelength [121]. For aligned MWCNT and CNF samples only the tips are probed.



(a) Raman band intensity ratios **(b)** Raman band FWHM

Figure 3.10: Results obtained from fitting the Raman spectra of MWCNT grown with 10 nm Fe at different temperatures using alternative growth recipe. Laser wavelength 514 nm.

MWCNT could also be grown using a slightly different recipe, in this case the acetylene was added when the system began to ramp up from 500 °C

to the growth temperature. It was observed that the samples grown with this recipe show vertical self-alignment at temperatures of 600 °C and above for CNT grown with 10 nm of Fe, below this temperature the samples are randomly aligned. In fig. 3.10 the fitting results from the Raman spectra obtained using a green laser on these samples are displayed. Only the 5 strongest bands are taken into account. Around 600 °C the trend in the results changes (here fitted with a second-order parabola). From a strong (linear) decline it switches to more or less constant value. This happens to both the ratios and FWHM of the different peaks.

This behaviour can be easily explained taking into account the growth mode. As these samples have root growth the tips of the tubes are created at a lower temperature than the later sections of the tube. However, as Raman spectroscopy only probes the surface area of aligned CNT, these higher quality portions are invisible and only the tips created at the temperature the alignment process started are visible. This is 600 °C, as confirmed by SEM analysis (not shown here). Thus in this case Raman spectroscopy can be used to determine the growth mode. The effects on the tip grown CNF are also investigated, but no such effect could be observed. In those samples the tips are always created at the highest growth temperature and show the largest degree of crystallinity.

3.9 Conclusion

MWCNT and CNF samples were created using CVD at different temperatures and Raman spectra were obtained from these samples. From this the trend of the Raman intensity ratios and FWHM versus temperature were investigated for both first and second order regions. The MWCNT samples show a clear trend for all bands ratios and FWHM, which are attributed to a change in crystallinity. For high quality MWCNT samples the I_D/I_G ratio can be sufficient to estimate change in crystallinity. For small changes adding other ratios, like $I_{D'}/I_G$, $I_{G'}/I_G$ and $I_D/I_{G'}$ and the FWHM of the D, G, D' and G' band can aid in drawing a conclusion. Good match in trend was found between the defect induced bands and several second order bands, which might aid in determining the physical mechanisms behind these bands. For instance, an interesting link between the G' and 2D' band versus crystallinity was found, suggesting they might be caused by a similar mechanism. For samples of sufficient quality it is possible to determine the in-plane ordering length using an empirical formula.

It is more difficult to investigate the crystallinity of CNF using Raman spectroscopy as the I_D/I_G ratio can show conflicting behaviour. It is recommended to use the second-order bands when possible, and look at the

FWHM of the D and G bands to estimate how the crystallinity is changing. If fitting of the G-band is problematic due to the presence of a strong D' peak, $I_D/I_{G'}$ can be used. When assessing crystal quality care should be taken to use the same laser wavelength for both MWCNT as CNF, as the I_D/I_G and $I_D/I_{G'}$ ratios strongly depend on the used laser wavelength. This dependency is not visible for the FWHM of the bands. The same is true when using the I_D/I_G ratio to determine the crystalline length L_a.

4

Growth and integration of vertical carbon nanotubes

During this work several combinations of support layers and catalyst where investigated, this chapter discusses the results of the different experiments. First an overview of the different layers are given, and the low surface energy of the used layers is given as reason the for excellent growth results obtained. Next, the results of growing CNT using Fe and Co as catalyst on TiN are given in terms of electron microscope images and Raman spectra. Using Co it was possible to grow CNT at record low temperatures of 350 °C, which is attributed to the low activation energy of this catalyst. This is followed by growth results using Fe on ZrN, which resulted in the growth of hundreds of μm long CNT on top of an electrically conductive layer. The chapter concludes with an presentation of the required measurement structures and fabrication techniques, like lift-off and sacrificial layers to protect the support layer, to integrate the required materials for CNT growth into semiconductor technology.

4.1 Introduction

As mentioned in chapter 2, CNT require a catalyst and support layer for growth. This chapter discusses two conductive support layers which were found to allow either low temperature growth attractive for monolithic integration (TiN), or the fabrication of long CNT useful for TSV (ZrN). Before the growth results on both layers are shown, a short discussion on the importance of the support layer will be given. Raman spectroscopy as discussed in the previous chapter is one of the techniques used for analysis throughout this chapter.

Growing the CNT is the first step in the fabrication of CNT vias. Another important aspect is the integration of the CNT growth process in semiconductor fabrication for the actual fabrication of CNT tests structures which will be electrically and thermally characterized in, respectively, chapter 5 and 6. The second part of this chapter discusses the used measurements structures. Techniques to pattern the CNT bundles will be given, followed by two schemes for integrating CNT into semiconductor technology called top-down and bottom-up integration. After this the importance of protecting the support layers from damage is discussed. Finally, SEM images of the fabricated CNT test vias are shown.

4.2 Support layers

As discussed in chapter 2, CNT are grown using transitions metals like Fe and Co. If these materials are directly deposited on Si, they will diffuse into the substrate which prevents growth. The metals can also diffuse into the active area of the transistors, reducing the lifetime of the charge carriers and thus transistor performance. In order to prevent the catalyst from diffusing into the substrate a diffusion barrier is required. In current semiconductor technology diffusion barriers like TiN and Ta(N) are used to prevent Cu from diffusing into the active area.

Another important aspect for the catalyst in CNT growth is that it should take the form of nanoparticles. The support layer should allow the transition metal catalyst film to break up into particles when heated, but also prevent the particles from agglomerating together. Al_2O_3 has been shown to be an efficient layer for this purpose, and is often employed to grow dense forests of CNT [30].

The application of the CNT bundles in this thesis is interconnects, and thus an electrically conductive support layer would be favoured. It is possible to make the Al_2O_3 thin enough to allow tunnelling [33]. However, this will result in a relative high contact resistance to the CNT bundle. As

mentioned before, TiN is a diffusion barrier often used in semiconductor technology, which has the advantage of being electrically conductive (104 $\mu\Omega$-cm). It has also been demonstrated that it is possible to grow CNT on this layer and form a good electrical contact [27]. As will be discussed in section 4.3, it was found that reactively sputtered TiN allowed the growth of dense forests of vertically aligned CNT at temperatures as low as 350 °C, which is attractive for vias for monolithic integration. These results will be presented in section 4.3. However, the maximum length which could be achieved with growth on TiN was 70 μm, after which the growth stopped. This is most likely caused by catalyst poisoning. Due to the relative short maximum height the higher temperature growth on TiN is not attractive for long CNT TSV.

However, there are many more potential electrically conductive layers. To limit the number of potential candidates the requirement that the layer doesn't oxidise easily in air will be added, because transfer of the substrates through ambient is required. Three candidates were available in the cleanroom which met these requirements: MoN (300 $\mu\Omega$-cm), MoO_3 (36 $\mu\Omega$-cm), and ZrN (5500 $\mu\Omega$-cm), all of which are reactively sputtered.

Each of these layers was tested as support layer by depositing 1.5 nm of Fe directly on the 50 nm thick sputtered layers and attempting growth using the standard LPCVD recipe at 650 °C. No growth was observed on the MoN and MoO_3 layers. However, the ZrN layer proved to be capable of growing CNT of several hundreds of μm length. This makes ZrN in combination with Fe an attractive candidate for fabricating CNT TSV. The growth results on ZrN will be discussed in more detail in section 4.4.

For the deposited catalyst film to break up into nanoparticles efficiently the catalyst layer should dewet on the support layer, which can be achieved by having a lower surface energy for the support material than the catalyst material [32]. In order to investigate the surface energy of the materials the interaction between the support layer and several different liquids (water, diiodomethane, ethylene glycol, and a mix of 50% water and 50% ethylene glycol) were dropped with the same volume on top of the support layer and their contact angles were analysed using an OCA-20 goniometer. From the contact angles of the different liquids the surface energy can be approximated using one of the many models available for approximating the interaction between the liquid and the surface. This approach is know as the static sessile drop technique.

Three different models were used to determine the surface energy, which were available in the SCA-21 software: the Owens, Wendt, Rabel and Kaelble method (OWRK), Wu method, and Equation of State (EOS), of which the details can be found elsewhere [141]. The results calculated using the

Table 4.1: Surface energies (in mN/m or mJ/m^2) determined using sessile drop technique for the different models mentioned in the text compared with literature.

Material	OWRK	Wu	EOS	Literature
TiN	53.9	61.0	49.3	41-63 [138], 47 [139]
SiO_2	62.3	68.5	54.7	43-106 [32]
Al_2O_3	38.9	44.1	38.5	62-100 [32]
ZrN	55.3	61.3	50.2	36-43 [138], 47.7 [140]

software are shown in table 4.1. The surface energies are close to each other for the different materials. Compared to the surface energy of Fe (2.22 N/m = J/m^2), the measured surface energy of all these materials are substantial lower, which can explain why these layers function well as support layer. The surface energies of MoN and MoO_3 could not be determined, as all test liquids completely wetted on these surfaces. This can indicate a high surface energy for these surfaces, which in turn explains the inability of these materials to sustain CNT growth.

4.3 Growth on TiN

TiN proved to be an effective support layer, allowing dense vertically aligned growth using both Fe and Co as catalyst. With the Fe catalyst CNT could be grown at temperatures ranging from 450-750 °C, while Co and Co-Al allowed growth at record-low temperatures of 350 °C. In the next sections first images obtained using electron microscopy will be shown, followed by Raman data of the different samples. Finally, the growth rates of the different catalysts used in combination with TiN will be compared.

4.3.1 Electron microscope images

The first catalyst investigated, and used for the fabrication of most test vias throughout this work, was 5 nm of e-beam evaporated Fe. In fig. 4.1 SEM images of Fe grown CNT at different temperatures can be found. The minimum temperature at which growth could be achieved was 450 °C, but 500 °C was used as minimum as the growth rate at 450 °C was quite low. The CNT grow vertically aligned, and length increases with temperature. The density of the CNT is estimated to be in the order of 10^{11} tubes/cm^2 by counting.

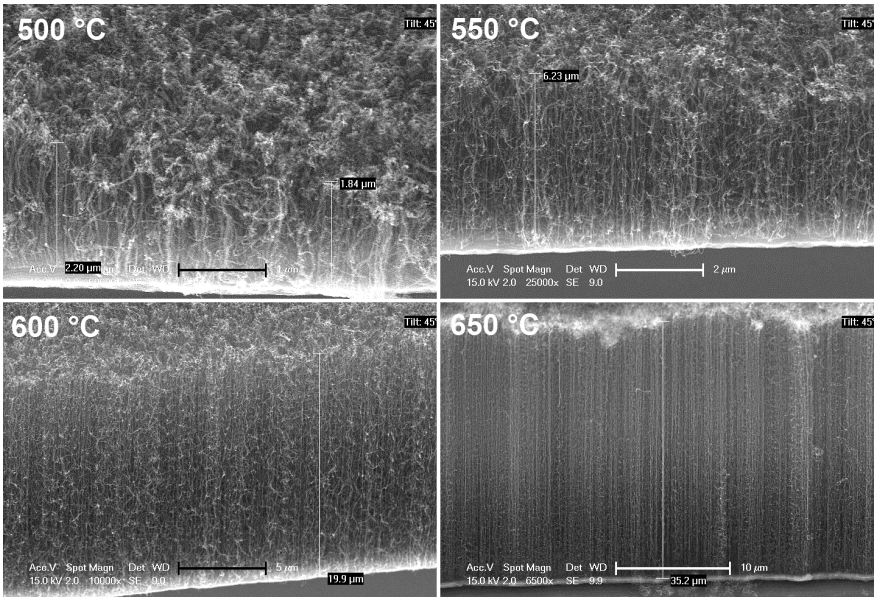


Figure 4.1: CNT grown using 5 nm Fe at different temperatures: 500 °C, 550 °C, 600 °C, and 650 °C. Growth time is 5 min for each sample. Scale bars are 1, 2, 5, and 10 μm, respectively.

It was found that using sputtered 3 nm Co-Al(28%), or 5 nm e-beam evaporated Co, CNT could be grown at temperatures as low as 350 °C. Another advantage of Co as catalyst is that it is considered semiconductor manufacturing compatible, while Fe is not. Fig. 4.2 displays SEM images taken from the growth results obtained using the Co-Al catalyst. The results from Co-grown samples are not shown here as the visual differences are small. Again vertically aligned CNT are obtained, with increasing length with temperature. The growth rate of the Co-Al catalyst is higher than that of Fe, which will be discussed in more detail in section 4.3.3. The density of these bundles is estimated to be slightly lower than that of the Fe-grown bundles, approximately $5 \cdot 10^{10}$ tubes/cm^2.

In order to investigate the diameter distribution of the CNT, TEM is required. Typical TEM images of Fe and Co grown samples at, respectively, 500 °C and 350 °C, can be found in fig. 4.3. The Fe-grown CNT have a clear hollow core, with a diameter distribution of 10-20 nm with an average of 14 nm. This indicates these CNT are MWCNT. Interestingly, the Fe catalyst was found at the tip of these CNT, which indicates a tip-growth

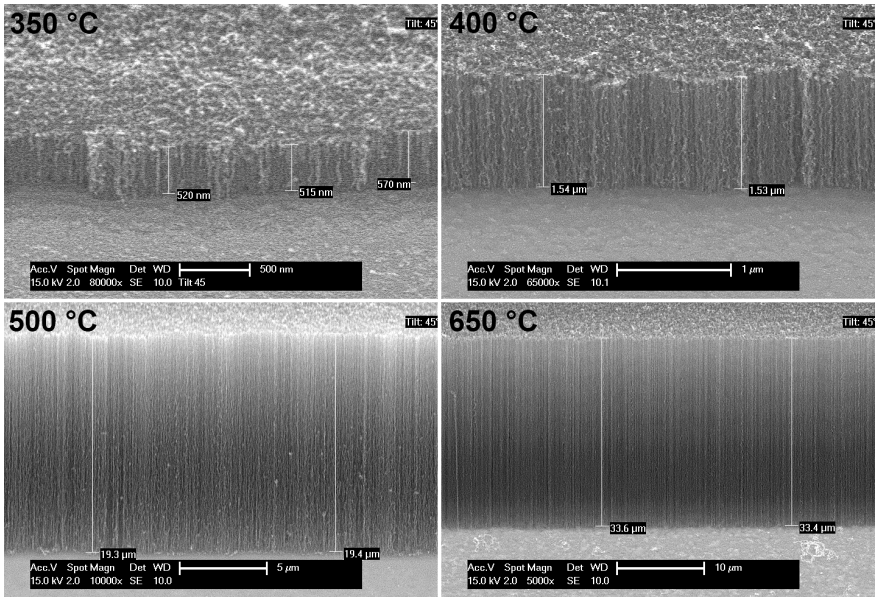


Figure 4.2: CNT grown using 3 nm Co-Al at different temperatures and growth times: 350 °C 30 min, 400 °C 10 min, 500 °C 5 min, and 650 °C 2 min. Scale bars are 0.5, 1, 5, and 10 μm, respectively.

mechanism.

For the Co-grown samples the diameter distribution was found to be 5-15 nm, with an average of 8 nm (for both the Co as Co-Al catalyst, at temperatures of 350 °C and 400 °C). Although this would indicate MWCNT, not always an hollow core was observed as can be seen in fig. 4.3. This indicates some of the tubes are more fibre-like. Finally, no catalyst particles were observed for Co-grown tubes, indicating a base growth mechanism.

As both catalysts give MWCNT and the densities are much lower than those required according to the calculations performed in chapter 2 it can be expected that these CNT will not electrically outperform the current interconnect materials. From the published work on low temperature growth in literature it can be concluded that at lower growth temperatures growth of SWCNT is problematic. Attempts of increasing the density by changing the thickness of the catalyst layer did not result in a noticeable difference or the growth of SWCNT. A cyclic deposition as suggested by Esconjauregui et al. [30] only resulted in lower density growth in case of Fe on TiN.

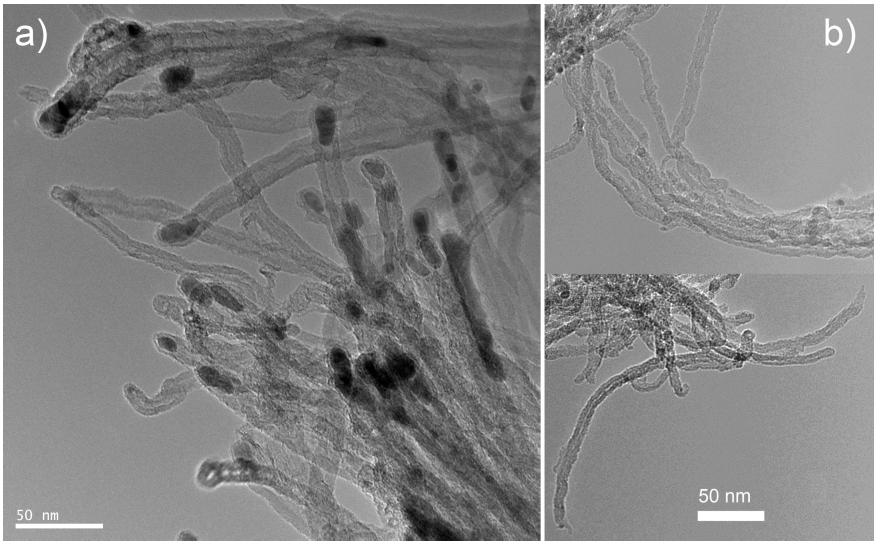


Figure 4.3: Typical TEM images taken from: a) 500 °C Fe grown samples, b) 350 °C Co grown samples.

4.3.2 Raman spectroscopy

Raman data was obtained for Fe, Co, and Co-Al grown samples fabricated at different temperatures and fitted using the procedures described in section 3.4. The fitting results are shown in table 4.2. Only the banfds which were found in chapter 3 to be the best indicators of quality are shown here.

The Fe-grown samples display a clear trend of increasing crystallinity with increasing growth temperature. The quality increase stagnates at the highest temperature, something which has been observed by others and is attributed to the higher rate of catalyst particle agglomeration [104].

Both Co and Co-Al display an increase in quality with temperature, according to the FWHM of the different Raman active bands. The intensity ratios display a more conflicting behaviour. While the $I_{D'}/I_G$ displays a clear decrease the I_D/I_G ratio appears to first decrease followed by an increase. Fitting inaccuracy of the G and D' bands is the most likely cause for this behaviour. The differences between the two Co-based catalysts are too small to distinguish them in terms of crystallinity. When comparing the 500 °C samples of Fe and Co, it appears that the quality of the Fe-grown sample is marginally better.

Table 4.2: Raman data obtained from CNT grown using different catalyst and temperatures

					FWHM [cm^{-1}]			
Catalyst	Temp. (°C)	$I_{D/G}$	$I_{D'/G}$	$I_{G'/G}$	D	G	D'	G'
Fe	500	1.70	0.68	0.43	74	57	44	139
	550	1.64	0.60	0.57	66	54	47	115
	600	1.35	0.37	0.72	56	48	41	96
	650	1.07	0.27	0.84	50	43	36	85
	700	0.78	0.22	0.93	47	39	37	77
	750	0.79	0.27	0.93	54	40	38	78
Co-Al	350	1.22	0.83	0.22	140	63	45	223
	400	1.13	0.59	0.19	134	60	43	217
	500	1.49	0.63	0.25	96	58	43	186
Co	350	1.09	0.65	0.18	152	63	44	223
	400	1.06	0.49	0.17	147	63	43	219
	500	1.26	0.41	0.22	99	59	43	184

4.3.3 Growth rate

As was observed in section 4.3.1 the CNT grow faster for higher temperatures, and display different growth rates for different catalysts. From the SEM images the growth rate can be determined for each sample. If these growth rates are plotted against the inverse temperature an Arrhenius plot of the catalytic reaction is obtained [142]. For the Fe and Co catalyst this plot is shown in fig. 4.4.

According to Ducati et al. [142], the growth rate (R) is proportional to:

$$R \propto \frac{D_0 S_0 \exp\left(-\frac{Q+q}{kT}\right)}{x} \tag{4.1}$$

where D_0 and S_0 are the diffusivity and solubility prefactors, x the diffusion distance, Q and q are the activation energies for diffusivity and solubility, respectively. From the slope of the fitted lines in fig. 4.4 the total activation energies of the different catalyst can be determined. The activation energy of Fe (0.56 eV) is higher than that of the Co-based catalyst (0.40-0.43 eV). This can account for low temperature growth being possible with the Co and Co-Al catalyst by allowing a sufficient growth rate even at low temperatures.

Interestingly, these activation energy are lower than the values of 0.9-1.6 eV reported before for LPCVD growth using C_2H_2 as feedstock and Fe

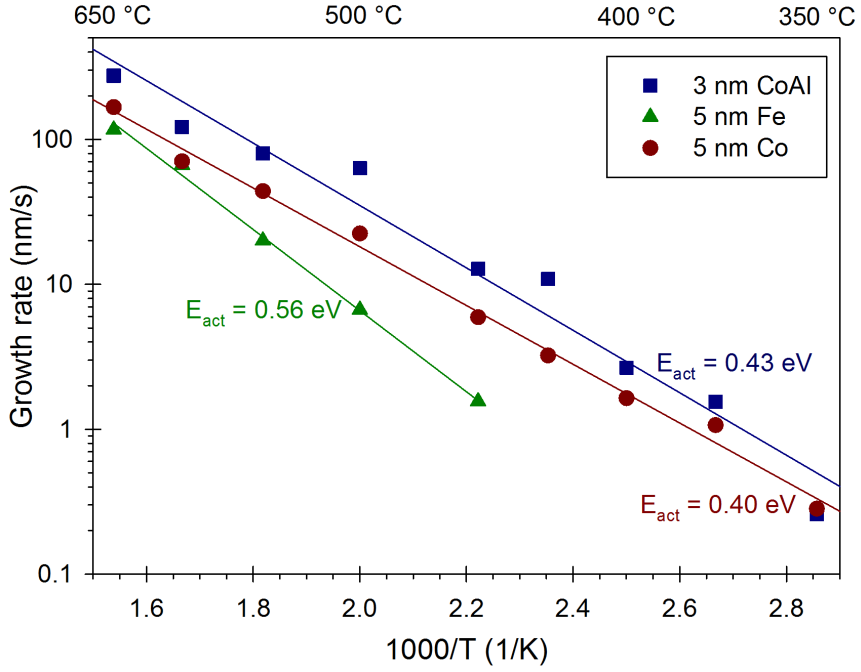


Figure 4.4: Arrhenius plot of the growth rate (in nm/s) against the inverse temperature for the different catalyst used in this work.

as catalyst [143, 144]. On the other hand, the activation energies are just 0.1-0.2 eV higher than values obtained before using C_2H_2 and PECVD [79]. The activation energies of Co are close to calculations of the barrier height of C surface diffusion on Co(111) surface (0.5 eV). This suggest that the catalytic reaction might be surface diffusion limited, just as was found for PECVD based CNT growth. In that case the question remains what causes the lowering of the dissociation energy of the C_2H_2, which is ~ 0.9 eV and normally limits thermal CVD [79]. A possibility could be the support layer, which is TiN here, and Al_2O_3 or SiO_2 in literature. It has been shown that TiN is able to catalyse the reduction of alkynes to alkenes with complex hydrides in solution [145], but to my knowledge no literature exists on gas phase catalyses of C_2H_2 dissociation using TiN.

The samples fabricated with Co-Al have a higher growth rate than those using Co as catalyst, except for the 350 °C grown samples which have roughly the same height. The activation energies (slope) between the Co and Co-Al catalyst are very close to each other. It is assumed that a different

pre-factor is the largest cause of the difference in growth rate between the two Co-based catalysts. As the diameter of the CNT is similar for both catalysts, it is unlikely that the diffusion distance x in eq. 4.1 will be different between Co and Co-Al, as the catalyst particle diameter is linked to the CNT diameter [91]. It is possible that the Al in the Co-Al catalyst enhances the catalytic activity of the nano-particle as has been shown before for Mo and Ti [146,147], thus altering D_0 or S_0.

4.4 Growth on ZrN

As was mentioned in section 4.2 it was discovered that on the electrically conductive ZrN layer long CNT could be grown using Fe as catalyst. In contrast to the TiN growth, which worked for Fe catalyst layers ranging from 2 to over 5 nm, the ZrN growth was found to depend heavily on the catalyst thickness. With the optimum thickness somewhere between 0.5-1.0 nm Fe growth rates close to 100 μm/min were observed for non-patterned samples, while for layers around 1.5 nm this decreased to just 10-20 μm/min. Moreover, it was found that growth in patterns gave geometric loading effects with the standard recipe, resulting in no growth for low fill-factor samples (e.g. samples with very few catalyst area). Both issues are demonstrated in fig. 4.5.

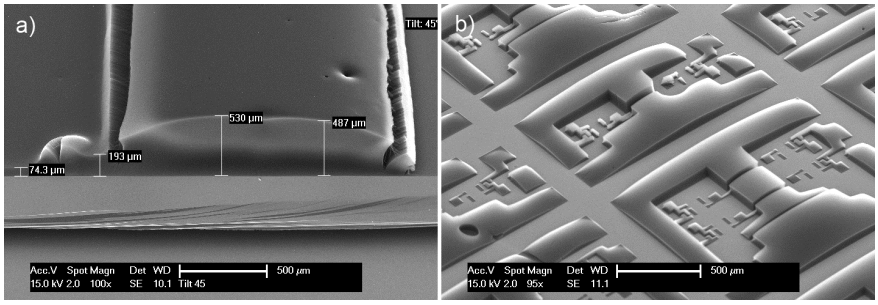


Figure 4.5: Growth issues with Zrn when the standard LPCVD recipe is used: a) edge of the wafer, where the Fe catalyst thickness gradually decreases due to local shielding displaying the sensitivity to catalyst thickness; b) loading effects occurring in patterned samples. Scale bars are 500 μm.

In order to find the optimum catalyst thickness and deposition conditions for the CNT growth on ZrN, a design of experiment using the Taguchi method was performed as part of a masters thesis. Interested readers are strongly encouraged to read the details of this experiment in the thesis, here

only some of the main results will be discussed [148]. Fig. 4.6 displays the outcome of the Taguchi design of experiment for the different parameters varied throughout a set of experiments and their influence on the growth rate. For instance, an optimum catalyst thickness of 0.8 nm Fe and growth pressure of 20 mbar were found. Other parameters, like the ZrN thickness were found to have hardly any influence on the growth rate.

Using the optimum settings (indicated in red in fig. 4.6) the, according to the design of experiment, optimum growth conditions for maximum length were verified. Fig. 4.7a displays SEM image of 30 min growth achieving a height of roughly 900 μm. Using other recipe conditions it was possible to grow vertically aligned CNT on patterns, for instance on a randomly generated pattern with different fill factors as shown in fig. 4.7b. Beside length also optimum conditions for the highest forest density was determined and verified, which resulted in a density of $1.2 \cdot 10^{11}$ tubes/cm^2, which is twice of that of the non-optimized recipe. Still, the density is roughly two orders of magnitude lower than what would be required according to the calculations in chapter 2 in order to outperform current interconnect materials.

Using the right conditions it was found that it is possible to grow SWCNT and DWCNT on ZrN with 0.8 nm of Fe as catalyst at a temperature of 650 °C. The Raman spectrum in fig. 4.8 shows that the CNT are of high quality, with a I_D/I_G ratio of only 0.2. Clear Radial Breathing Modes (RBM) can be observed at wavenumbers of 191 and 282 cm^{-1}, which according to the equation $\omega_{RBM} = 234/d$ translate to diameters of, respectively, 1.23 and 0.83 nm [113]. As only one laser wavelength was used it is unclear which other diameters are present, and what the ratio of semiconducting versus metal tubes is.

Fig. 4.9 displays TEM images taken from samples grown at different conditions and with different catalyst thicknesses. For the thicker catalyst layers MWCNT could be observed, while the 0.8 nm of Fe resulted in DWCNT. The TEM images confirm the high quality of the grown CNT. The 650 °C growth temperature of the samples is too high for direct integration as CNT vias with already fabricated devices. While it was found the CNT could be grown at 550 °C, the growth rate of those samples was significant lower. Still, for silicon interposers which contain no devices but only wiring the currently available growth recipes can already be used as the thermal budget for these interposers is much higher.

4.5 Integration aspects

In order to successfully fabricate test structures using CNT as vertical interconnects the materials and techniques used to grow these CNT, as discussed

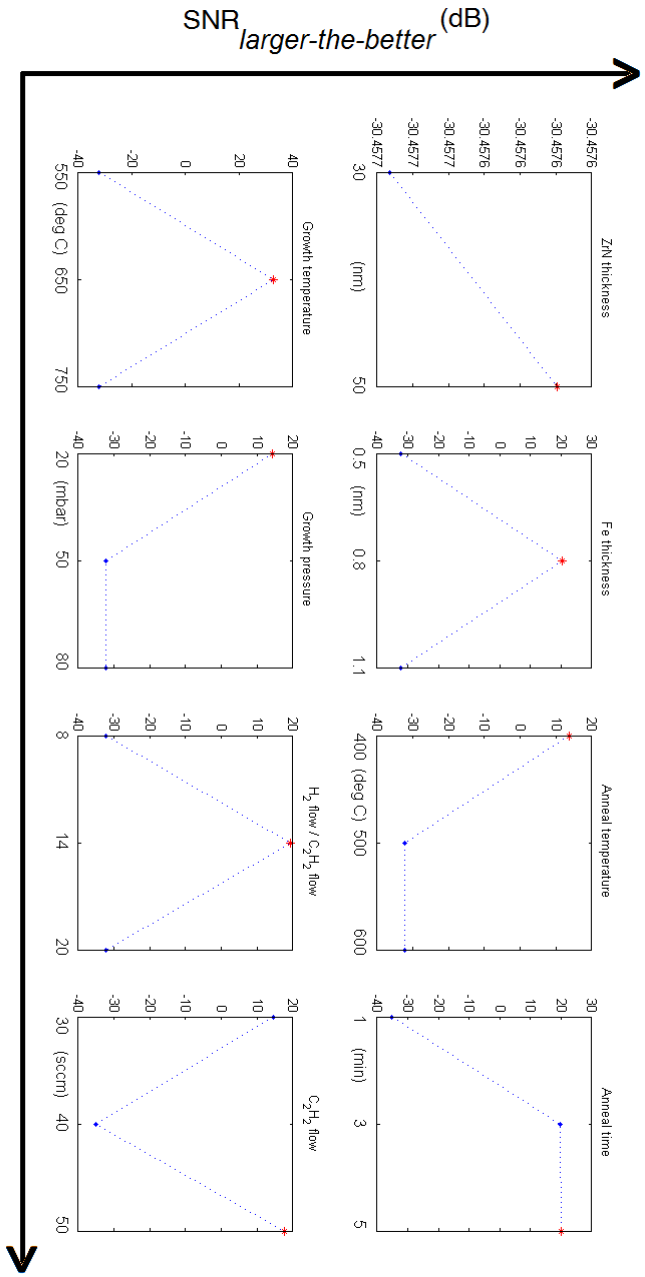


Figure 4.6: Example of the outcome of a Taguchi design of experiment to find the influence of different parameters on the growth rate.

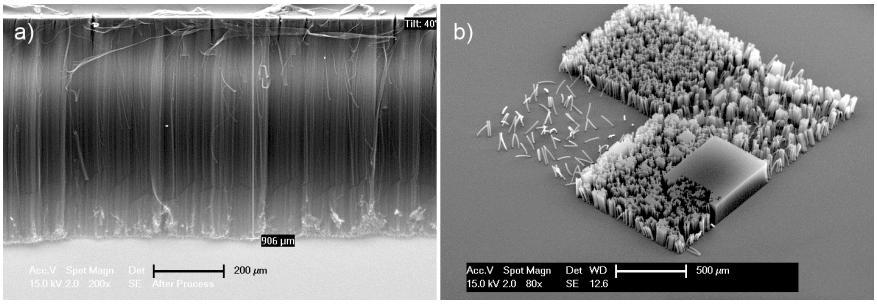


Figure 4.7: SEM images of optimized CNT growth on ZrN: a) optimum growth recipe with parameters as indicated in fig. 4.6, b) growth on area with random patters with different fill factors. Scale bars are 200 and 500 μm, respectively.

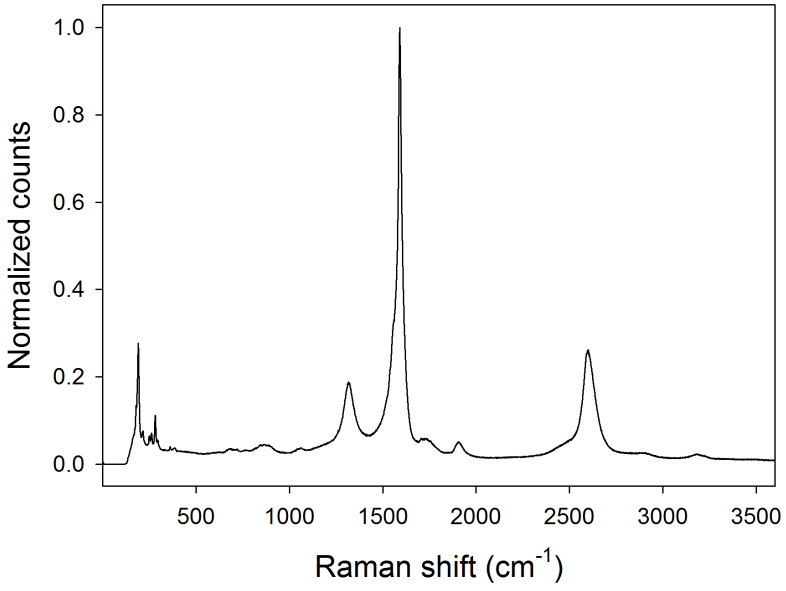


Figure 4.8: Raman spectrum of high quality CNT grown on ZrN with Fe as catalyst. The peaks around the low wavenumbers are the RBM of the CNT, of which the position depends on the diameter of the tube.

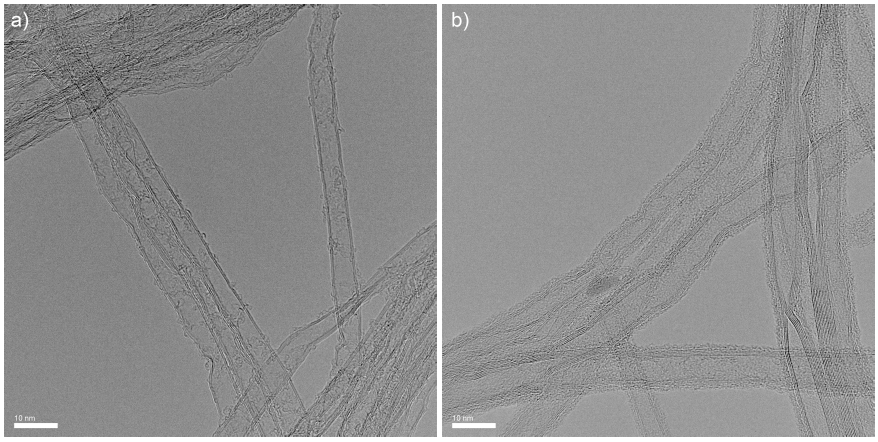


Figure 4.9: TEM images taken from samples grown at different conditions: a) 0.8 nm Fe, 50 mbar with 1000/50 sccm H_2/C_2H_2 showing DWCNT with a diameter of 5 nm; b) 1.1 nm Fe, 80 mbar with 320/40 sccm H_2/C_2H_2 showing MWCNT with a diameter of 8 nm. Scale bars are 10 nm.

in the previous section, have to be made compatible with the IC processing steps required to fabricate vias. First the desired measurement structures will be discussed, followed by a method to pattern the catalyst. After this different approaches to fabricate vias will be discussed. Next, the importance of protecting the support layer is shown. Finally, SEM images of the fabricated vias are given. Integrating the CNT technology into 3D SG-TFT technology will be discussed in chapter 7.

4.5.1 Design of measurement structures

To measure the resistance of a CNT bundle, an electrical contact to both sides of the bundle is required. One of these contacts can be through the support layer on which the catalyst is deposited, while the contact to the tips of the bundle can be formed by another metal layer. In order to electrically separate the metal layers a dielectric will be required.

As accurate measurements of the CNT bundle resistance are necessary a so-called four-point probe technique has to be used. In such a configuration electrical contact are made to the bundle with two sets of probes: one set drives a known current through the bundle (I_{in} and I_{out}), while the other set measures the potential drop over the CNT bundle ($V_{bundle} = V_h - V_l$. As the input impedance of a potential meter is high (ideally infinite), no current is flowing though this second pair and the potential drop is measured accurately regardless of wire and probe resistance. Fig. 4.10 shows a sketch of a four-point probe structure as used in this work, with probe connections denoted.

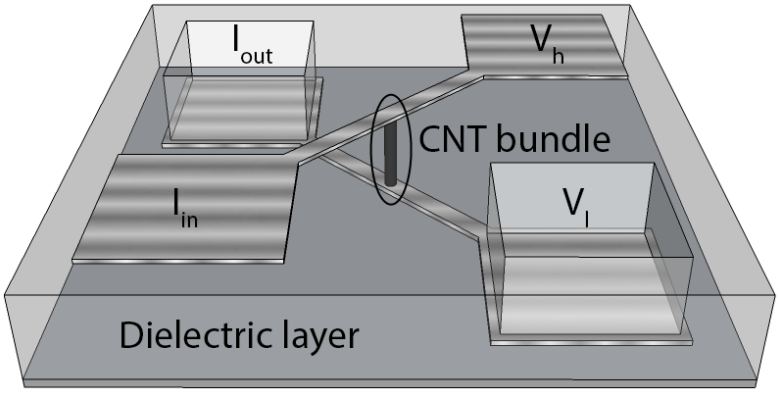


Figure 4.10: Sketch of a four-point probe measurements structure used to electrically characterize a CNT bundle.

4.5.2 Lift-off for catalyst patterning

For the measurement structures in fig. 4.10 the catalyst needs to be grown selectively in the openings. This is achieved by patterning the catalyst layer. Several methods can be used to pattern metal layers: lithography followed by etching, lift-off, and shadow masking. The last method is not flexible as no lithography is used, and will thus be discarded. Lithography combined with (wet) etching is the most straightforward approach, but can not always be used as it might attack the support layer. As alternative for this lift-off is investigated. In contrast to methods based on etching with lift-off the photoresist is deposited and patterned before metal deposition. After metal deposition the photoresist is dissolved using an organic solvent (e.g. N-Methyl-2-Pyrrolidone (NMP)) which will lift-off the metal film on top of the resist from the substrate. The metal layer thus only remains at the sites where the photoresist was removed beforehand. An advantage of this method is that no layers are deposited on top of the catalyst, another is that no etching is required, and layers which are hard to (selectively) etch can still be patterned (e.g. Pd).

The lift-off method was tested with a large variation of catalyst (Fe, Co and Ni) and support layers (TiN and Al_2O_3) during the course of this research, and proved to be effective. Raman spectroscopy has been used to verify that the use of lift-off has no impact on the CNT quality. In fig. 4.11 the quality indicators of the Raman spectra obtained from Fe grown on TiN for different temperatures are shown. The differences between the patterned and non-patterned samples are within the statistical error of the measurements.

For patterning Fe NMP, heated to 70 °C proved to be a powerful solvent, generally requiring no ultrasonic treatment (persistent residues could be removed using a special q-tip for lift-off purposes). Unfortunately, NMP was found to affect Co and Co-Al, resulting in poor growth once the Co had been exposed to the NMP. The low temperature growth processes are especially sensitive to contamination. Lift-off using acetone proved to be insufficient for this purpose, giving bad reproducibility. Several other organic solvents were tested as replacement for NMP, including dimethylformamide, dimethylacetamide, dimethyl sulfoxide and Tetrahydrofuran (THF). From investigation using SEM after treating samples with the different solvents and growth with the same parameters, THF at 35 °C proved to be the most effective solvent in terms of residue removal and not affecting the growth. Best results were obtained by using 15 min of ultrasonic treatment.

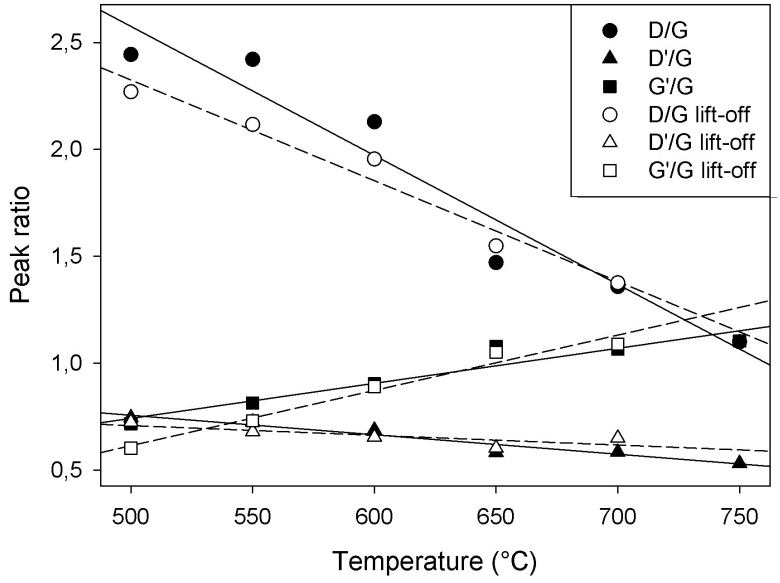


Figure 4.11: Raman band ratios comparison for CNT grown at different temperatures using Fe on TiN, patterned by lift-off, compared to non-patterned samples

4.5.3 Top-down and bottom-up integration

Traditionally vias are fabricated using a top-down approach. After a horizontal metal layer is finished a dielectric layer is deposited, and contact openings to the metal layer are etched. Finally, the openings are filled with metal. While this process is straightforward, it potentially requires the etching and filling of HAR structures with metal. This process can be sensitive to step coverage and void formation, creating reliability issues.

The advantage of CNT is that the growth of them on a patterned catalyst area results in a bottom-up deposition of a CNT bundle with dimensions that can be set by the catalyst area and growth time. This property of CNT allows the fabrication of bottom-up vias, which start with the growth of a free standing CNT bundle, followed by dielectric deposition over and around the bundle, CMP to uncover the CNT bundle and finally horizontal metallisation. Fig. 4.12 displays a schematic overview of both processes.

While bottom-up vias were fabricated before using CNF by Li et al. [149], no attempts were made to fabricate such structures consisting of dense bundles of MWCNT. Also, in order to allow low-temperature bottom-up in-

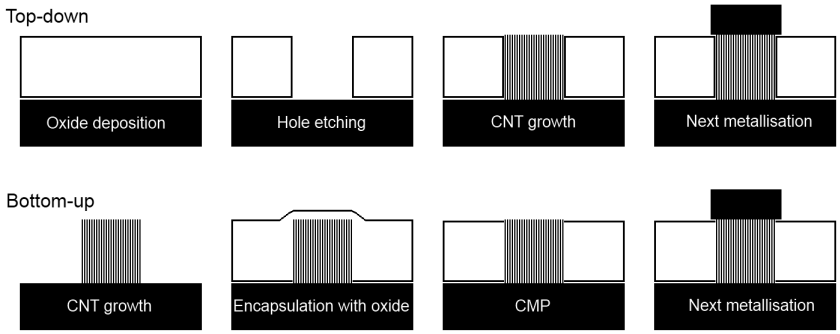


Figure 4.12: Schematic overview of top-down and bottom-up integration process

tegration, CNT have to be covered by a low-temperature dielectric. This in contrast to the high temperature LPCVD Tetraethyl Orthosilicate (TEOS) used by Li et al. [149]. For low-temperature dielectric deposition PECVD is the preferred method in the semiconductor industry. However, it is possible that the plasma might damage the grown CNT by ion bombardment or oxidation. To investigate this, free-standing bundles of CNT with a height of approximately 5 μm were grown on TiN substrates using Fe patterned by lift-off (fig. 4.13a) and covered with PECVD TEOS, silicon oxide and nitride at temperatures of 350 °C for the TEOS deposition, and 400 °C for the other two.

Fig. 4.13b displays a SEM image taken of an array of 5x5 2 μm wide CNT bundles covered by 1 μm TEOS. Good step coverage is achieved, although deposition on the side-walls ($\sim$ 600 nm on each side) of the CNT is lower compared to the total thickness of the TEOS layer. In fig. 4.13c the same array is completely covered by 5 μm of PECVD oxide (deposited from SiH_4 and N_2O). Planarization will be necessary to remove the excess oxide. Finally, fig. 4.13d shows the array covered by 200 nm silicon nitride (from SiH_4 and NH_3). The deposition is significantly less smooth compared to the oxide depositions.

Using Raman spectroscopy, the CNT crystallinity was investigated before and after PECVD dielectric deposition of 1 μm of TEOS or oxide and 200 nm nitride. Fig. 4.14 shows that only minor changes to the crystallinity can be observed. The TEOS deposition appears to induce the least amount of damage, with only the width of the D band increasing slightly. Oxide deposition from silane, on the other hand, displays an increase of the D band,

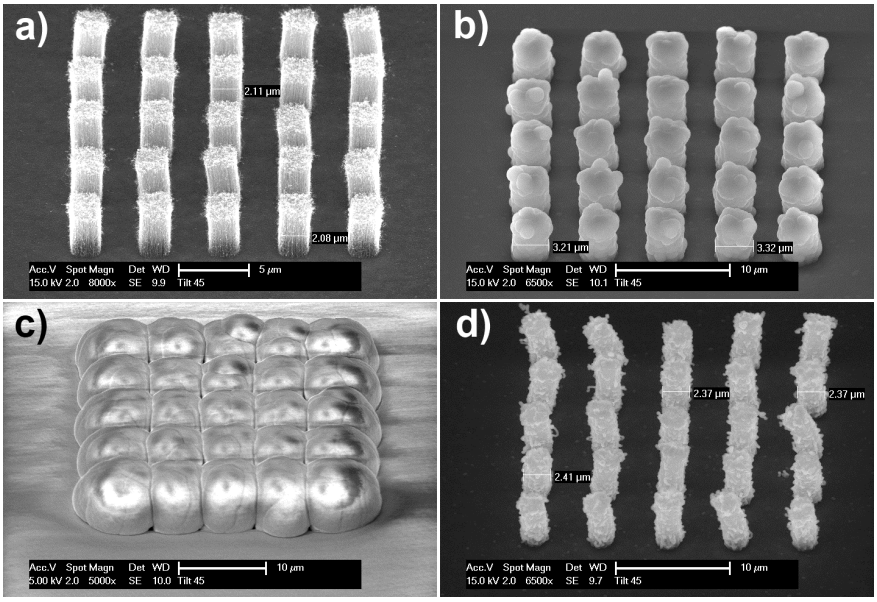


Figure 4.13: SEM images of: a) free-standing bundles grown on TiN (scale: 5 μm), b) bundles covered by 1 μm TEOS (scale: 10 μm), c) bundles covered by 5 μm SiO_2 (scale: 10 μm), d) bundles covered by 200 nm Si_3N_4 (scale: 10 μm).

indicating a reduction in crystallinity. The width of the D band is similar to that of the D band after TEOS deposition. Finally, nitride deposition has a D band intensity between that of CNT covered by TEOS and oxide. Again the width of the D band is similar to that of TEOS covered CNT. It can thus be concluded that PECVD deposition does not induce a significant amount of defects in the CNT bundles, opening up the possibility to use this method for low-temperature bottom-up integration.

Another advantage of the bottom-up process is that bundle densification techniques can be used. The simplest method is exposing the CNT bundle to an alcohol (e.g. isopropanol), which makes the bundle collapse by a combination of surface tension of the liquid and strong van der Waals interaction [150]. In fig. 4.15a an example is shown for a 5 μm wide bundle which has an almost 50 % reduction in top area.

Fig. 4.15b-d display SEM images of CNT after approximately 1 μm of bulk oxide was removed using CMP at Philips MiPlaza. The CNT are cut-off at the same height as the oxide. Gaps can exist between CNT

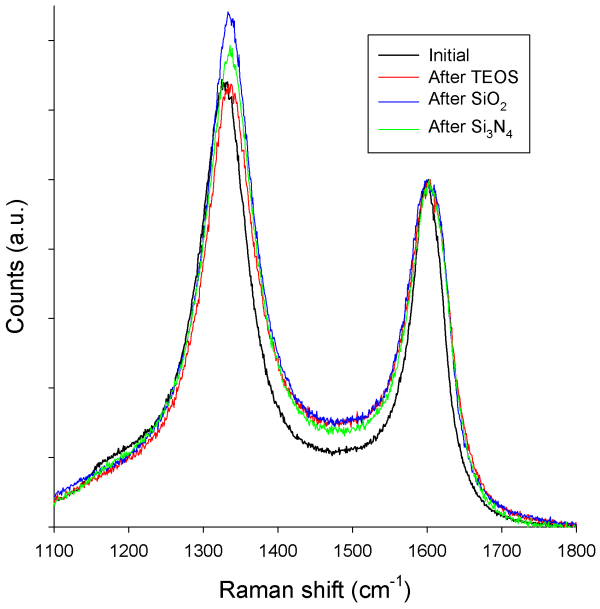


Figure 4.14: Raman spectra of CNT before and after covering with PECVD dielectrics. The intensity is normalized to the G-band.

bundles spaced closed to each other, due to a non-optimized PECVD oxide deposition process (fig. 4.15c). Decreasing deposition rate likely solves this issue. As shown in fig. 4.15b, in some larger CNT bundles cracks appear with a width of several hundred nm, which are caused by the non-optimized CMP process.

It must also be noted that difficulties were encountered in polishing large bundles with widths of $\geq 6\mu$m as shown in fig. 4.15d. Most of these bundles are removed during CMP, which is attributed to mechanical removal as the substrate adhesion of CNT is generally low [151]. The bundles are only covered on the outside by the PECVD oxide. Embedding the CNT in a layer of atomic layer deposited dielectric, as demonstrated by Chiodarelli et al. [38], to increase mechanical stability could circumvent this problem and the formation of cracks in medium sized bundles. The CMP process requires additional improvement, a recent publication by Van der Veen et al. [40] may give insight into which parameters could be optimized.

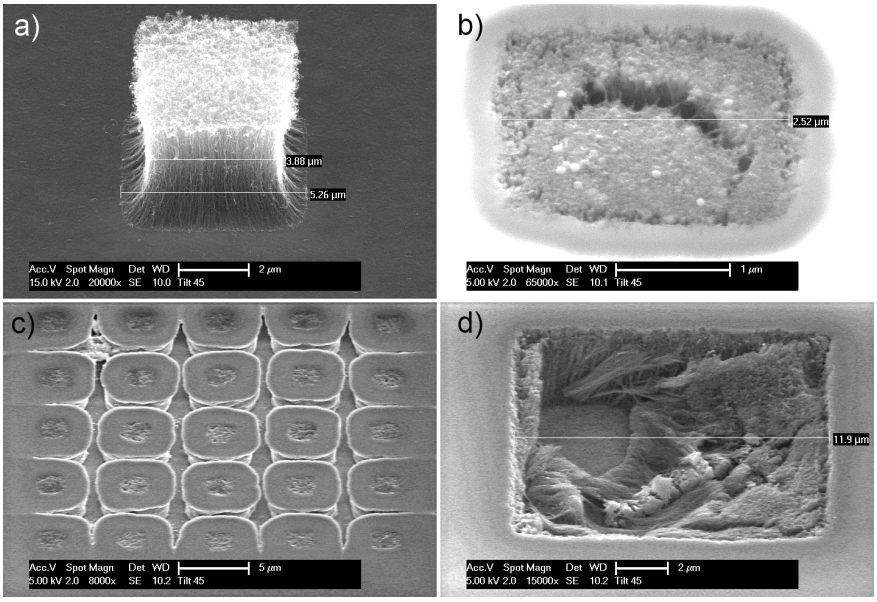


Figure 4.15: SEM images of: a) liquid densified bundle, b) densified bundle after CMP, c) array of bundles after CMP, d) large bundle after CMP displaying tube removal. Scale bars are: 2, 1, 5, and 2 μm, respectively.

4.5.4 Protecting the TiN

As mentioned in section 4.3 TiN was used as support layer for CNT growth. It was found that certain common process steps in semiconductor technology can induce microscopic changes in the TiN layer, preventing low temperature self-aligned CNT growth. This section discusses the impact of chemical solutions and plasma treatment on the TiN layer, and the subsequent low and high temperature CNT growth. For this the TiN layer was exposed to the conditions specified in table 4.3. After this treatment Fe was evaporated and CNT were grown at 500 °C (low temperature) and 650 °C (high temperature).

In fig. 4.16 the SEM images taken from the resulting CNT growth on the five different samples at low and high temperature can be found. Both plasma treated samples display no self-aligned vertical growth on low temperature. The other three samples grow self-aligned CNT with a height of several microns. Interestingly, sample B displays the highest CNT (3.7 μm), followed by sample A (3.3 μm) and E (2.5 μm). It is unsure if this is caused by slight differences in the treated surface (HF might passivate

the TiN surface), or due to small temperature differences as growth rate is highly temperature dependent.

The high temperature samples again display a difference between samples A, B, E and C, D. Although self-aligned growth is now possible on all samples, the CNT height of sample C and D is approximately half of the other samples. Also density and alignment suffers from the plasma treatment. At high temperature the length of samples A and B is found to be the same (31 μm), while E is slightly longer (35 μm), which is in contrast to the situation at low temperature.

Table 4.3: Overview of surface treatments used on different samples.

Sample	Treatment
A	10 min. HNO_3 (99.9 %)
B	1 min. HF (0.55 %))
C	5 min. 1 kW oxygen plasma
D	1 min. 100 W fluorine plasma
E	No treatment

Table 4.4: Raman data obtained from CNT grown on different samples.

				FWHM [cm^{-1}]			
Sample	$I_{D/G}$	$I_{D'/G}$	$I_{G'/G}$	D	G	D'	G'
A: 500 °C	2.84	1.24	0.30	81	63	44	148
650 °C	2.22	0.81	0.88	54	47	39	92
B: 500 °C	2.80	1.18	0.27	81	62	43	151
650 °C	2.28	0.75	0.63	52	47	37	90
C: 500 °C	3.13	1.30	0.44	69	59	44	116
650 °C	1.56	0.57	0.78	50	42	33	75
D: 500 °C	2.66	1.29	0.37	85	63	45	136
650 °C	1.63	0.73	0.79	57	45	38	81
E: 500 °C	2.74	1.14	0.30	80	62	43	148
650 °C	2.13	0.68	0.60	53	46	36	93

Using Raman spectroscopy it was investigated if the treatment of the support layer influenced the crystal quality of the CNT growth. In table 4.4 the intensity ratios and FWHM of the different Raman bands are displayed. Table 4.4 clearly shows that CNT grown at higher temperature have higher

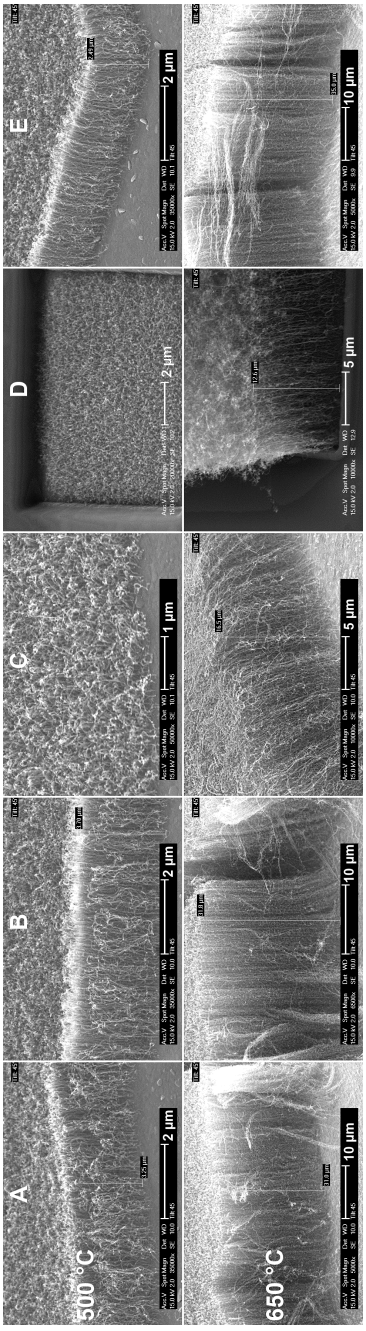


Figure 4.16: SEM images of CNT grown on differently treated TiN substrates at 500 °C and 650 °C.

crystallinity. The band ratios and widths of samples A, B and E are close to each other, indicating that chemical treatment of the TiN surface with either HNO_3 or HF has no profound impact on CNT crystallinity. On the other hand, sample C and D display a different behaviour. The I_D/I_G ratio is significantly higher for the low temperature C sample, and lower for the high temperature C and D sample. This could indicate lower and higher crystallinity, for respectively low and high temperature samples. On the other hand, the FWHM of the low temperature growth on sample C suggest a higher crystallinity compared to A, B, D and E.

In order to investigate potential causes for the change in low and high temperature CNT growth on plasma treated surfaces the samples were measured after their treatment with Atomic Force Microscopy (AFM), see fig. 4.17. No significant difference exist between samples A and E (and B, which is not displayed here). Sample C, on the other hand, appears to have a more smoothed surface (i.e. less sharp edges between the different TiN grains). The change in surface roughness is only minor, and unlikely to be the cause for the change in growth. Sample D displays the largest change. It appears as if the TiN layer was partly sputtered forming clusters of small particles. The surface morphology of sample D is changed extensively, which could account for the observed change in CNT growth on these samples.

To further examine the influence of the TiN layer treatment on the CNT growth AFM was also performed on samples on which Fe was deposited and pre-annealed for catalyst growth, see fig. 4.18. Both sample A and E display small nanoparticles of similar size (the bigger bright spots on sample A are most likely particles deposited on the wafer during HNO_3 treatment). The same holds for sample B (not shown here). On sample C and D, however, beside the small nanoparticles a significant amount of larger nanoparticles can be found. This will result in CNT growth with large diameter distribution and, most likely, lower density. This can explain the absence for self-alignment at low growth temperature for samples C and D. It can also explain the higher crystal quality observed by Raman spectroscopy on those samples. As found by Antunes et al. [109] CNT grown from larger nanoparticles at the same temperature show a lower I_D/I_G, $I_D/I_{G'}$ and FWHM, and a higher $I_{G'}/I_G$. This does, however, not account for the large I_D/I_G ratio observed for the low temperature C sample. Sample D has low temperature Raman data which matches closer with that obtained from sample E. Indeed the nanoparticle distribution of sample D is, compared to sample C, more similar to that of sample E. Increased surface roughness of sample D is most likely the cause of the observed broader particle deposition. For sample C it is believed that the oxidation of the TiN surface due to the oxygen plasma alters the surface properties in such a way that activation of

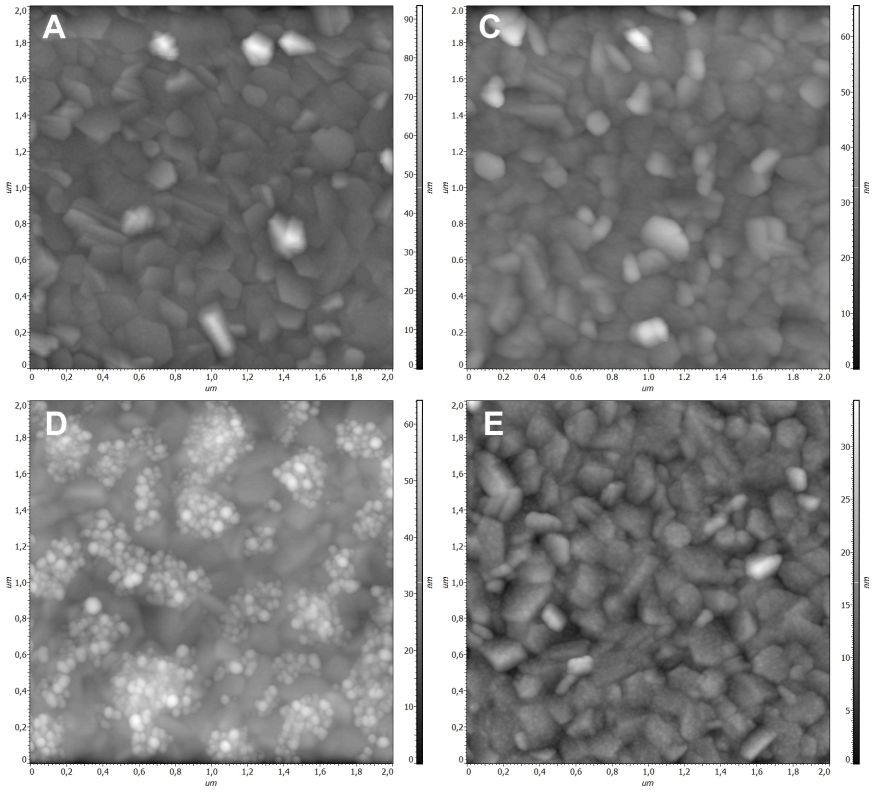


Figure 4.17: AFM images taken from samples A, C, D and E displaying the effect of the surface treatments on the TiN surface. Area 2 by 2 μm, height map in nm.

the catalyst layer becomes more difficult.

In order to protect the TiN, a sacrificial layer was deposited on top of the TiN. It is important that this layer can be removed without damaging the TiN. Several layers were tested for this, of which 100 nm Ti or AlN proved to give the best performance and simplest integration. Both layers can be selectively removed by wet etching, using 0.55 % HF or MF322 developer, respectively. Ti has been used throughout most of the experiments, due to it simplicity to deposit and fast and clean removal. However, in some cases Ti was an insufficient barrier layer for fluorine plasma etching, especially when a long overetch is required when creating deep oxide openings. For these processes the AlN layer proved to be useful, which is very resilient against

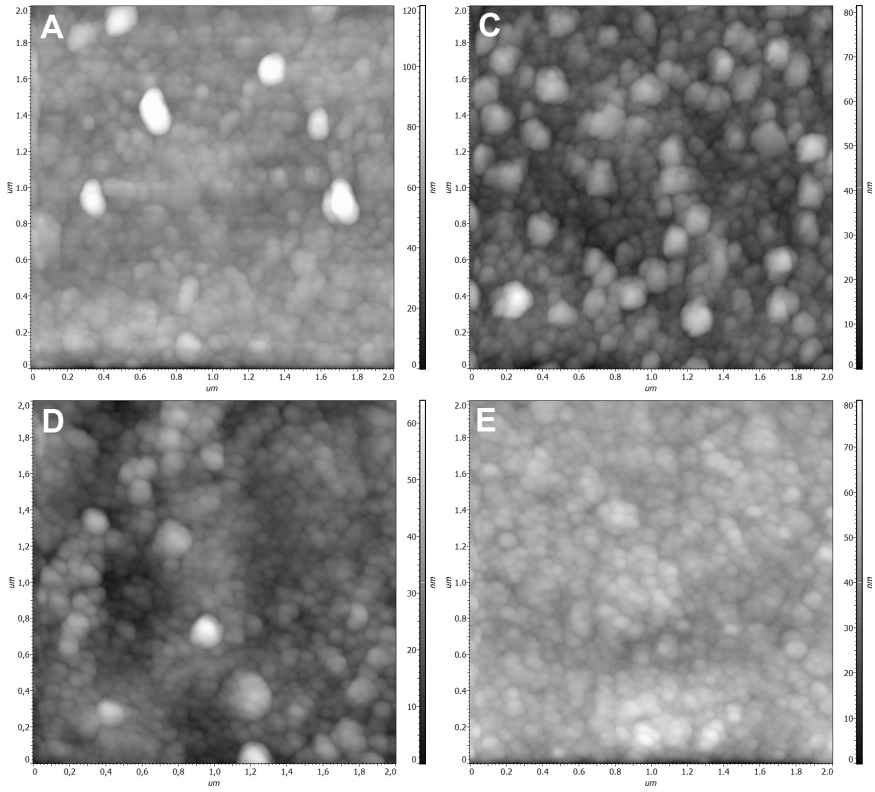


Figure 4.18: AFM images taken from samples A, C, D and E displaying the catalyst nanoparticles after activation. Area 2 by 2 μm, height map in nm.

fluorine plasma etching, although wet removal takes longer and appeared more prone to leaving residues.

4.5.5 Images of fabricated vias

Using the methods described in the previous sections, CNT test vias were fabricated using both the top-down and bottom-up approach. In case of the top-down approach vias were fabricated at 350 °C and 400 °C using Co as catalyst, and at 500 °C and 550 °C with Fe as catalyst, an example flowchart is given in appendix A.1. Co-Al, being a sputtered layer, proved to be more problematic for integration. Lift-off cannot be used due to the

sputtering temperature of 350 °C, and direct sputtering after contact opening formation gave growth on the SiO_2 layer and side-walls. Sputtering the catalyst before dielectric deposition and protecting it with an AlN barrier is possible (HF etches Co-Al, so Ti cannot be used). However, even the developer for AlN removal was found to affect the catalyst layer.

In fig. 4.19 two cross-sections can be found: one prepared using Focused Ion Beam (FIB) milling of a Fe-grown via, and another prepared using mechanical cleaving of a Co-grown via. As can be seen the CNT grow well-aligned. At the top of the bundle a small 100-200 nm gap exist, which is caused by hole tapering. The tips of the CNT are embedded into the top metal layer, which consists of 100 nm of Ti and 3 μm of Al(1% Si). Finally, a gap between the TiN and SiO_2 can be observed which is due to over-etching of the Ti layer. Bottom-up vias were fabricated using Fe at 500 °C. No cross-section of these vias could be made due to the low yield of the process. Some top-view images of these vias can be found in section 4.5.3.

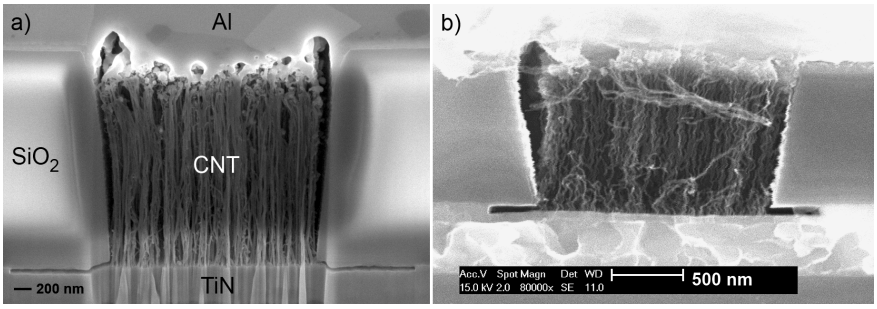


Figure 4.19: SEM cross-sections of CNT test vias: a) FIB prepared sample of 2.6 μm long via grown at 500 °C using Fe (54° tilt); b) mechanically cleaved sample of 1 μm long via grown at 350 °C using Co.

4.6 Conclusion

In this chapter CNT growth using different support layers and catalysts was investigated. Two support layers were found to provide excellent growth, which is attributed to their low surface energy. It was found that on TiN layers CNT could be grown for monolithic integration purposes, at temperatures as low as 500 °C using Fe, and record-low temperatures of 350 °C using Co and Co-Al. Another advantage of Co is that it is considered semiconductor manufacturing compatible. SEM images and Raman data of Fe and Co-grown CNT were shown, typically Fe gave the highest density of

tubes. The growth rate of both catalysts was investigated, and it was found the the Co-based catalyst have a lower activation energy, allowing the lower temperature growth.

Growth using Fe on ZrN resulted in long and high quality tubes with diameters as small as 0.83 nm. Loading effects were observed which could be prevented by tuning the growth conditions using a Taguchi design of experiment. This resulted in the fabrication of CNT bundles with lengths up to 900 μm. To the best of my knowledge these are the first CNT bundles with length over several hundreds of μm fabricated directly on electrically conductive layers. This makes the ZrN support layer with Fe catalyst attractive for the fabrication of CNT TSV, especially for silicon interposers which have a relative high thermal budget due to the absence of active devices.

In the second half of this chapter the desired 4-point probe measurement structures were discussed. This was followed by several integration aspects. First, lift-off was presented to pattern the catalyst which allows the catalyst to be patterned without etching the support layer. After this top-down and bottom-up integration were presented, and it was demonstrated that it is possible to use low temperature deposition techniques for bottom-up integration without damaging the CNT. This was followed by a discussion on the importance of protecting the support layer, as it was found that plasma damage to the TiN layer prevent vertically aligned growth. Finally, SEM cross-sections of the resulting test vias were shown.

5

Electrical characterisation of carbon nanotube vias

Electrical measurements performed on test vias using 4-point probe structures on vias with different widths, lengths, and fabricated at different temperatures using different catalysts are described in this chapter. The chapter starts with the I-V characteristics, followed by the uniformity and yield. It was found that heater non-uniformity causes spread in the resistance. Using vias with different lengths the contact resistance was determined, which was found to be low compared to the CNT bundle resistance. Comparing the electrical measurements with Raman data it was determined that the MWCNT exhibit conduction among multiple walls. Compared to literature the lowest resistivities obtained here (20 mΩ-cm) are among the average values reported, which is caused by the low quality and density of the CNT bundles. The thermal coefficient of resistance of the CNT vias was found to be negative (-400 ppm/K for Fe and -830 ppm/K for Co-grown tubes). A bundle-size dependent effect was observed, which can partly be explained by taking into account a temperature dependent contact resistance. The chapter concludes with electrical reliability measurements. The highest allowed current density was found to be 9 MA/cm^2, and failure appears to be either at the contacts or due to Joule heating in the centre.

5.1 Introduction

In this chapter the electrical measurements of the CNT test vias fabricated using the growth processes and fabrication techniques described in chapter 4 are discussed. The measurements are performed on short and low temperature grown CNT bundles, which are meant for integration into monolithic 3D ICs. For this several sets of wafers with test devices were fabricated: two sets with Fe as catalyst on TiN with different bundle lengths grown at 500 °C (one patterned by the waferstepper, one by the contact aligner), one at 550 °C, and one set with Co on TiN grown at 350 °C and 400 °C with a fixed length. For these sets vias with different widths were fabricated using a top-down approach. Two wafers were fabricated using a bottom-up approach and CNT growth at 500 °C, of which one of the wafers was densified using isopropanol. Although these two wafers had a low yield, still some electrical measurements could be performed.

First the IV-characteristics will be discussed for the different sets of devices in section 5.2.1. This will be followed by an investigation of the wafer uniformity of the electrical resistance in section 5.2.2. One of the Fe-grown sets was fabricated using the contact aligner instead of waferstepper, and has thus a higher inaccuracy in via diameter. The CNT length of this set was, however, investigated in more detail using FIB cross-sections prepared by the National Institute of Standards and Technology (NIST). The contact resistance between the metal-CNT will be determined using this set of devices in section 5.2.3. After this the number of parallel conducting MWCNT walls is estimated from the measurement data. Finally, the resistivity of the test vias fabricated using different catalysts, temperatures and integration approaches will be compared to values from literature in section 5.2.5. All measurements were performed on the four-point probe structures using a semi-automatic probe station with Agilent 4156 series high accuracy semiconductor parameter analyser.

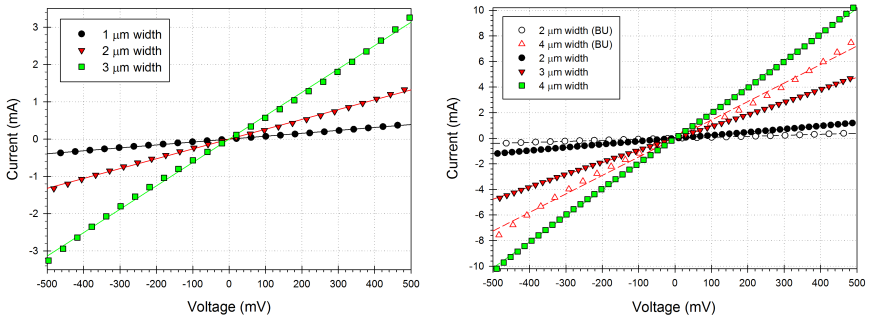
Besides the electrical resistance measurements performed at room temperature, measurements at elevated temperatures were performed in order to determine the TCR of the vias. The results of these measurements on samples fabricated at 350, 400 and 500 °C will be discussed in section 5.3. This is followed by a discussion on the electrical reliability of the fabricated CNT vias using ramp to failure and voltage hold test in section 5.4.

5.2 Resistance measurements

5.2.1 IV-characteristics

In fig. 5.1 typical I-V characteristics obtained from test vias fabricated at 350 °C (fig. 5.1a), and 500 °C using both a top-down as bottom-up (BU) approach are shown. All top-down fabricated vias display an almost completely linear response, indicating ohmic contact between the metal and CNT interfaces.

For the bottom-up fabricated vias a small non-linear behaviour can be observed. As the contact at the TiN-CNT interface should not be affected by the different integration approaches, as CNT are directly grown on TiN in both cases, the difference in top metal contact is likely the cause of this non-linear behaviour. The contact area is much smaller for the bottom-up fabricated vias, while the top-down vias are embedded in the top metal as will be shown in section 5.2.3.



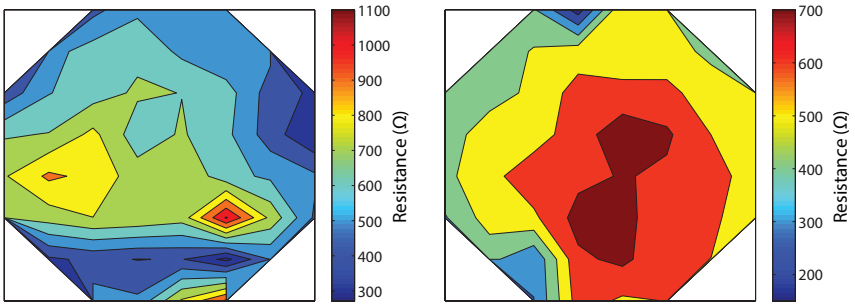
(a) (b)

Figure 5.1: I-V characteristics obtained from: a) CNT grown at 350 °C, b) CNT grown at 500 °C using top-down and bottom-up (BU) approach.

5.2.2 Uniformity and yield

In manufacturing uniformity and yield are important aspects. As in this work growth was performed on wafer-scale, it allows these aspect of the CNT growth to be investigated. As the electrical resistance is the key parameter of a via, the uniformity of this parameter will be studied. As benchmark, vias with a width of 1.5 μm, which is one step bigger than the critically sized 1 μm wide via, were used. It is expected that any potential lithography and dry etching non-uniformities resulting from working on the

non-critical dimension should have only a small impact on vias of this size and larger.



(a) (b)

Figure 5.2: Resistance contour plot obtained from 1.5 μm wide CNT vias fabricated at: a) 350 °C, and b) 400 °C.

Fig. 5.2 displays contour plots of the resistance of vias fabricated at 350 °C and 400 °C with Co as catalyst. The vias fabricated at 400 °C display a higher resistance in the centre, something which was also often observed for CNT vias fabricated using Fe at 500 °C. This pattern is caused by the non-uniformity of the heater in the CVD chamber used for CNT growth, of which the temperature is slightly higher in the centre than at the edge. As was mentioned in chapter 4 the growth is highly dependent on temperature. This non-uniformity in heater temperature during growth results in shorter CNT at the edge, compared to the centre, which in turn results in a lower resistance. Improving the heater design from a single-zone to a multi-zone heater can easily remove this observed non-uniformity. In fig. 5.2a, besides the non-uniformity caused by the heater, some isolated high-resistance point can be observed. It is assumed that these are caused by photoresist residues remaining after the lift-off process (for these wafers aceton was used). The improved lift-off process using THF as described in section 4.5.2 will likely results in improved uniformity, but has not yet been tested for a test via process.

In order to investigate the spread of the resistance for CNT test vias fabricated at different temperatures, the cumulative frequency plots of the full-wafer (52 dies) resistance values are plotted in fig. 5.3a. The distribution around the median of the resistances appears to be similar for the wafers fabricated at the lowest three temperatures, but deviates for the wafer fabricated at 550 °C. It is assumed that this deviation is caused by

the rougher surface of the bundle grown at 550 °C, which has a larger variation in individual CNT lengths. If yield is defined as all vias which fall within ±0.5 of the mean value the yields are, 87 %, 89 %, 88 %, and 84 %, for temperatures of 350 °C, 400 °C, 500 °C, and 550 °C, respectively.

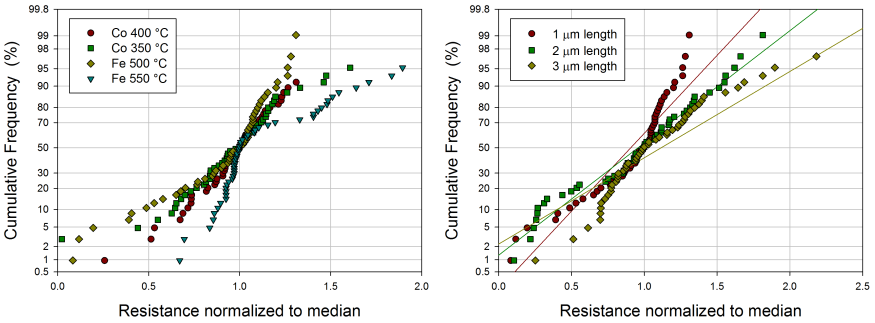


Figure 5.3: Cumulative frequency plots of: a) CNT vias grown at different temperatures, b) CNT via resistances of different length grown using Fe at 500 °C. Obtained from vias of 1.5 μm width, all values are normalized to the median.

Beside temperature the length of the CNT vias is of interest, as the aim is to achieve vias of high aspect ratio. Fig. 5.3b displays the cumulative frequency plot of CNT vias fabricated using Fe at 500 °C, but with different growth times and in deeper oxide openings. The spread in values increases for longer CNT vias (indicated by the decreasing slope of the linear fit). This can be caused by larger variations in CNT height for increased growth times. The yield are now 88 %, 71 %, and 84 % for, respectively, 1, 2, and 3 μm long CNT vias.

5.2.3 Contact resistance

In fig. 5.4, the measured average resistance determined from the 10 centre dies for different bundle lengths and widths can be found, fabricated at 500 °C using Fe as catalyst and patterned using the contact aligner. Each length of the via was determined from several cross-sections investigated in the SEM. Extrapolating the resistances to zero length results in a negative contact resistance, which is physically impossible. It was found that the width of the vias changes neglectable with increasing length, ruling out an area effect caused by hole tampering as the cause for the negative contact resistance.

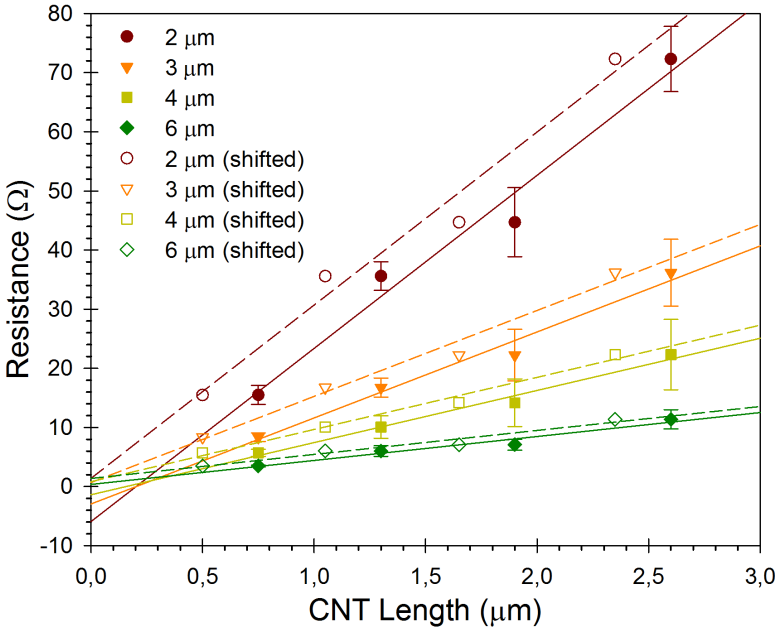


Figure 5.4: CNT bundle resistance vs. length for different bundle widths (2-6 μm). Closed symbols and solid line: measurement data corrected for approximate measured CNT length. Open symbols and dashed line: data shifted to take into account contact area.

As could be observed in the SEM cross-section of the fabricated structures presented in chapter 4, the tips of the CNT are embedded in the top metal contact. This embedding of the CNT tips could account for the negative contact resistance observed in fig. 5.4. Since the contacts are fabricated similar for the four different samples, the embedding of the CNT tips results in an approximately equal reduction of CNT electrical length. In fig. 5.5, a close-up of a 1 μm long CNT bundle is shown, as captured by an back-scatter electron detector. A clear contrast difference is observed between the CNT tips and Ti contact layer. As can be observed there is a contact area around the CNT tips, which has a length ranging from 200-300 nm. The difference in contact length is likely caused by the not well-aligned CNT tips which tend to partly buckle and differ from length locally.

If now a length reduction of 250 nm is assumed the data points shift to the left, as shown in fig. 5.4 (open symbols and dashed lines). Upon extrapolation a positive contact resistance is obtained. It must be noted that

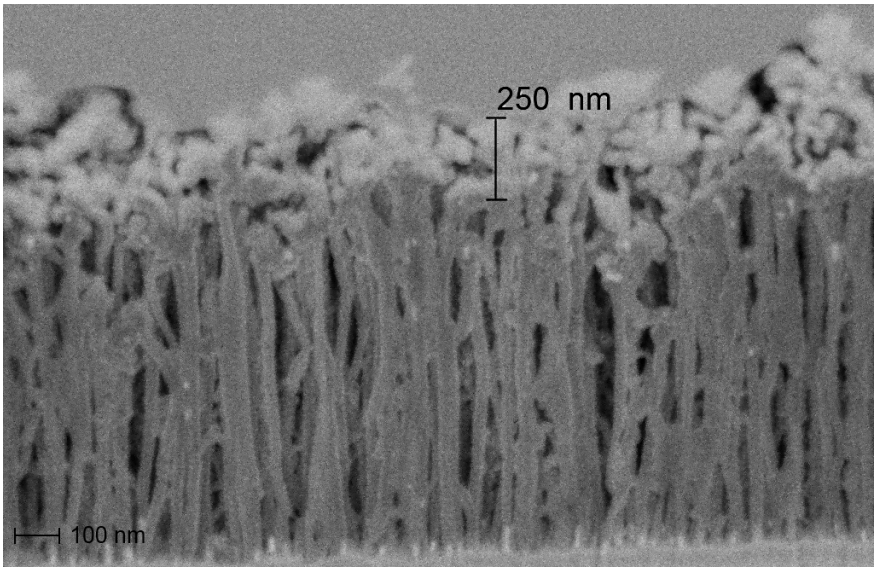


Figure 5.5: Close up of the CNT tips as imaged by the back-scatter electron detector in the dual-beam FIB/SEM, displaying a clear contrast between Ti and CNT.

this data can only be used to get an impression of the order of magnitude of the calculated values. For a more accurate determination it is required to know the length, area and tube density of the CNT bundles with higher accuracy, of which the length is the largest uncertainty in this work.

Table 5.1: Linear fitting parameters of fig. 5.4 and calculated per tube properties.

Bundle width (μm)	$R_{C,bundle}$ (Ω)	$r_{L,bundle}$ (Ω/μm)	$R_{C,CNT}$ (kΩ)	$r_{L,CNT}$ (kΩ/μm)
2	1.4	29	5.6	117
3	0.7	14	6.3	131
4	0.8	8.8	13	141
6	1.4	4.1	49	146
Average			18	133

Table 5.1 displays the parameters used for the linear fitting of the measured resistances. Using the area and the density (10^{11} cm^{-2}) the number

of parallel MWCNT per bundle can be estimated. Assuming all tubes are contributing to the conduction, the per-tube contact resistance and length dependent resistance can be determined using eq. 2.9, as shown in table 5.1. The average per tube contact resistance of 18kΩ is almost one order of magnitude smaller than that of the length dependent resistance (133 kΩ/μm). Due to this, a reduction in length of a few hundred nm can result in a negative contact resistance being observed.

5.2.4 Multi-wall conduction

In the previous section the CNT via resistance against length was used to determine the contact resistance by extrapolation. Another parameter which could be obtained was the length dependent resistance. As the length dependent part depends on the MFP of the CNT vias, it can be used to estimate the quality of the CNT vias.

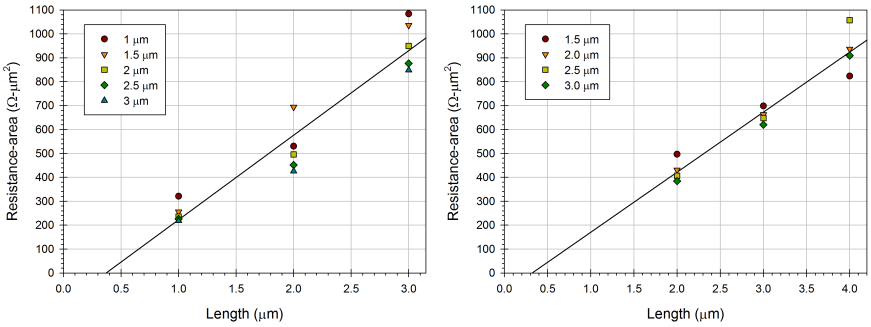


Figure 5.6: Resistance-area of smallest size CNT vias versus length, fabricated at 500 and 550 °C using Fe as catalyst

In fig. 5.6 the resistance multiplied by the unit area (in μm^2) of the smallest sized CNT vias are plotted against length, for vias fabricated at 500 °C and 550 °C (both patterned using the waferstepper). The solid lines represent a fit to the ensemble of data points per length, in order to get the average for differently sized vias. The vias fabricated at both temperatures display a negative resistance, which is again due to tip embedding. Interestingly, the point where both lines cross $R = 0$ is almost the same, indicating the length reduction is similar for bundles grown at different temperatures.

As the vias are fabricated using the exact same process for each length, and with a linear increasing growth time which was verified by SEM in-

spection, it can be assumed that the length reduction by embedding is independent of length. Although the exact electrical length of the CNT vias is not known, the slope of the line is thus not affected. This slope (r_L) is 354 Ω/μm and 251 Ω/μm for, respectively, vias fabricated at 500 °C and 550 °C.

The MFP of the CNT can be determined using the length dependent part of eq. 2.9, which can be rewritten as:

$$\lambda_{CNT} = \frac{12.9\text{k}\Omega}{DAN_{channels}r_L} \tag{5.1}$$

in which D is the density and A the area. The value of $N_{channels}$ can be determined from the diameter of the tube and eq. 2.4. For the tubes here, which have an average diameter of 14 nm, this would result in a maximum of 18.4 channels available (case 1). This is, however, only the case if all the channels are contacted. As the resistance between shells is high, it is possible that only the outer wall contributes to conduction if the inner walls are not directly contacted, as was shown by Frank et al. [152]. In this case only 2.2 channels would be available (case 2).

As was shown in section 3.7 the in-plane ordering length L_a can be determined from the I_D/I_G ratio of the Raman spectrum. As L_a is the average distance between defects, it should be equivalent to the MFP of the sample. From the I_D/I_G ratios found in table 4.2 the MFP are approximately 2.6 and 2.7 nm for samples fabricated at 500 °C and 550 °C, respectively.

Using eq. 5.1, a density of 10^{11} tubes/cm^2, and the values of r_L determined previously, the λ_{CNT} for case 1 is: 2.0 nm and 2.8 nm for the 500 °C and 550 °C samples, respectively. For case 2 this is: 16.6 nm and 23.4 nm. If one now compares the electrically approximated MFP with L_a it suggests that almost all walls are contributing to the conduction.

In the previous section it was already found that the contact resistance is small compared to r_L. Here it was found that there appears to be an excellent contact to the individual MWCNT walls. As the metals used to contact the CNT are similar to those used by other researchers (e.g. Chiodarelli et al. [153]) the selection of materials is not the primary cause of the low contact resistance.

Inspecting the contact area might give an explanation of the multi-wall contacting. The bottom contact is formed between the TiN and the CNT, which grow on top of this substrate and are mechanically attached. This specific contact resistance is expected to be small due to TiC formation [25, 27]. However, the same layer was used by Chiodarelli et al., which observed a high contact resistance.

The top contact, on the other hand, could account for the difference in contact resistance with the work of others. Many researchers use dielectric

filling followed by CMP to expose the tips of the CNT [21, 26, 29, 35, 153]. Yokoyama et al. [26, 29] found that CMP reduces contact resistance. They state that it aids in contacting multiple walls in each CNT by removing the tip. Beside CMP there exist other methods to form a good electrical contact. It was found that a good wettability is important in forming a low resistance contact by enhancing the contact area [53], and simulations have shown that embedding the contacts reduces the Schottky barrier [154]. As was shown in fig. 5.5 the top-contact is well embedded, and Ti is a material known to have good wettability to CNT.

Still, embedding the top contact does not necessarily mean that a good contact is formed to all MWCNT walls, as resistance between individual walls is high [26]. As the CNT grow by a tip growth mechanism, as was found in section 4.3.1, the Fe catalyst particle is positioned at the tip. This likely enables contact to multiple walls of the CNT. In case of Yokoyama et al. the tubes displayed a base growth mechanism, and no catalyst particles were visible at the tip. It is believed that the combination of enlarged contact area in combination with a tip growth mechanism can account for the observed low contact resistance and conduction along multiple MWCNT walls.

5.2.5 Resistivity

In chapter 1 an overview of electrical resistivities calculated from results published by other researchers was given. In fig. 5.7 the average resistivities obtained in this work for different catalysts and growth temperatures are shown. The resistivities of the 500 °C and 550 °C vias are averaged over all test vias with different lengths. All structures, except for the bottom-up vias, are fabricated using the waferstepper. To calculate the resistivity the via length was assumed to be equal to the bundle length as observed in SEM images. The electrical length reduction as discussed in section 5.2.3 is not taken into account, and R_c is part of the resistivity for equal comparison with values from literature.

The resistivity increases for decreasing CNT growth temperature, which confirms a reduction of CNT crystallinity (quality) for decreasing growth temperature. A large gap in resistivities exist between the Fe (500 °C and 550 °C) and Co-grown (350 °C and 400 °C) samples. Part of this can be explained by a reduction in density (roughly 2 times lower for the Co samples), and diameter, resulting in less conduction bands being available for the 8 nm Co-grown tubes.

The bottom-up fabricated vias display a large variation of resistivity with diameter. This is likely caused by the high contact resistance to the

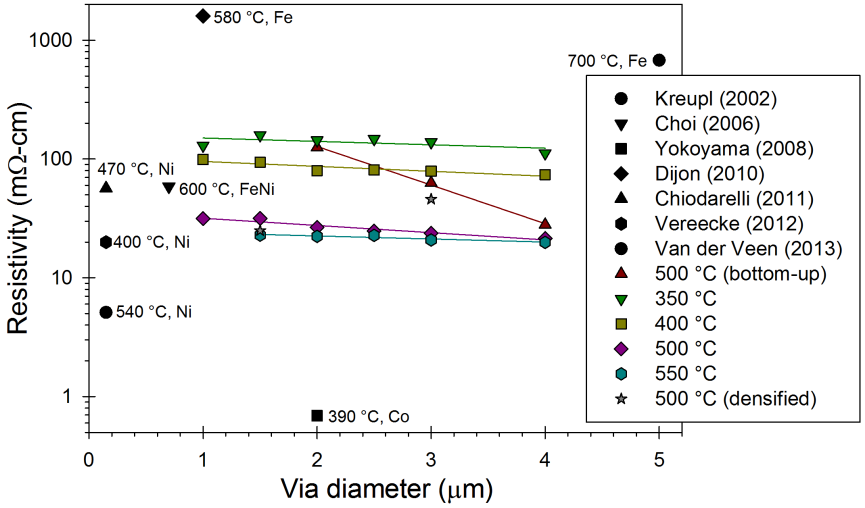


Figure 5.7: Resistivity from samples fabricated at different temperatures, compared with values obtained from literature.

top of the CNT bundles, which increases for small diameter bundles. For the densified bundles the width after densification has been used. The 3 μm bundle resistivities are close to each other. However, the 1.5 μm wide bundle performs much better, which is likely due to process variations.

Compared to values from literature these CNT bundles outperform samples fabricated at higher temperatures, which is likely due to the lower contact resistance of these samples. Further improvements can be made, as suggested by the lower resistivity values form literature, by further optimizing the integration process and improving the quality by recipe tuning. Moreover, the maximum density of 10^{11} tubes/cm^2, is two orders of magnitude lower than that required according to calculations performed in section 2.2. There is quite some improvement required in order to outperform current materials like Al and Cu, which have a 3-4 orders of magnitude lower resistivity.

5.3 Thermal coefficient of resistance

An advantage of CNT over metals which was not mentioned in chapter 1 is their potential negative TCR [155, 156], which aids in the reliable operation of the interconnects. As VLSI circuits are usually operated well above

room temperature, a positive TCR results in an increase in RC-delay and losses, which in turn increases the temperature even further. A negative TCR, on the other hand, will reduce delay and losses with increasing temperature. Metals have a positive TCR, with that of bulk Cu and W being 3900 and 4500 ppm/K, respectively. While electrical measurements of CNT vias have been performed by various researches [17, 21, 29, 35, 37]; hardly any measurement data is available for the TCR of CNT vias. The only publication appears to be a paper by Yokoyama et al. [29] which actually showed a positive TCR.

The resistances at different temperatures were measured using a temperature controlled chuck, which was first ramped up to the maximum temperature of 190 °C, and subsequently cooled down in several steps towards 25 °C. This way any potential annealing effect at elevated temperature influencing the CNT bundles resistance is circumvented. Fig. 5.8 displays an example of the relation between the resistance and the temperature for 1 μm long vias with different widths. The response appears to be linear with temperature for the measured temperature range, with the resistance of the vias decreasing with temperature.

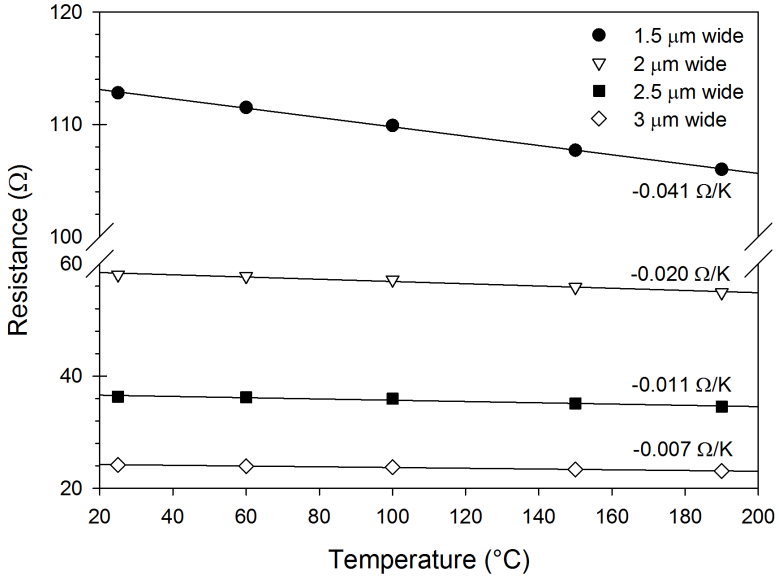


Figure 5.8: Resistance plotted against temperature for 1 μm long CNT bundles of various widths. The solid line indicates a linear least squares fit.

The temperature coefficient of resistance of each wafer with different

bundle lengths, and different via widths (ranging from 1 to 10 μm) were obtained using linear fitting of resistances measured at 5 different temperatures using the automatic probe-station. In fig. 5.9 this data is plotted for each length against via width. As can be clearly seen all small vias show a negative TCR, which is caused by additional conduction bands becoming available in the multi-walled CNT with increasing temperature [155]. However, after a certain width, which appears to depend on the total via length the characteristics change, and the vias display a positive TCR.

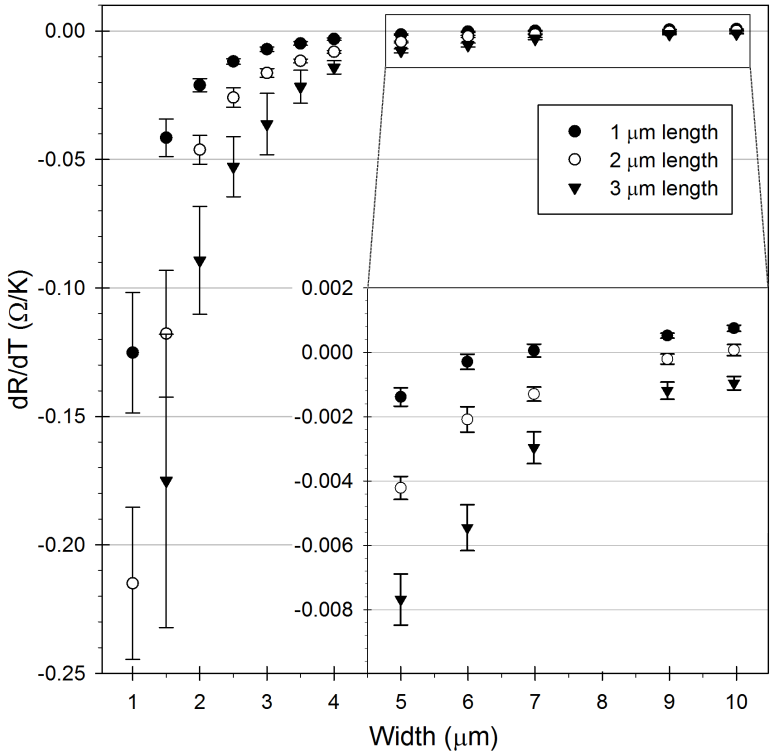


Figure 5.9: Thermal coefficient of resistance values for the measured temperature range, plotted for all via widths and lengths. The inset show a close-up of the vias ranging from 5-10 μm.

This trend is better observable when the TCR data in Ohm per Kelvin is converted into ppm/K by dividing by R_0, the resistance at room temperature (25 °C), as shown in fig. 5.10. All small vias appear to have a TCR between -300 ppm/K and -400 ppm/K, which displays no clear dependency

to the via length. After a via width of 3 μm this changes and a clear dependency with via length and width can be observed. For relatively shorter and wider vias a clear change to a positive TCR is seen, while the longest vias don't show this behaviour for the fabricated range of via widths.

Fig. 5.10 also includes the TCR data obtained from vias fabricated using Co at 350 °C and 400 °C. The TCR has a substantial larger value of about -830 ppm/K, with no apparent difference between the two low growth temperatures. The increase in the TCR for the low temperature samples is surprising, as models in literature predict a decreasing TCR for decreasing MWCNT diameter [155]. As these tubes are more defective, additional defect scattering can be expected. It could be that due to the higher defect density the electron scattering hardly increases with temperature in the measured range. If this is the case the opening up of additional conduction bands can have a larger impact on the resistance, thus resulting in a more negative TCR.

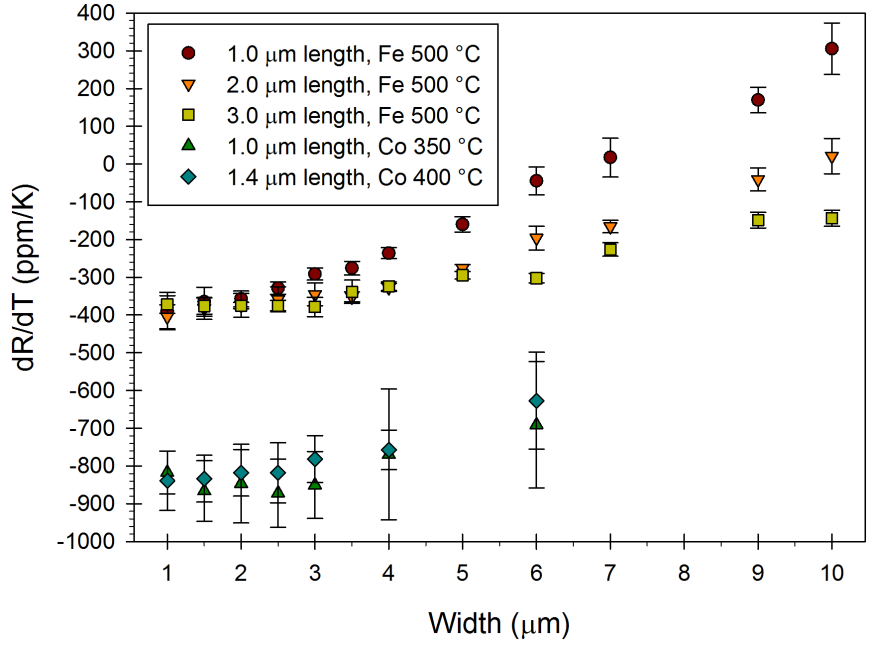


Figure 5.10: Thermal coefficient of resistance values for the measured temperature range in ppm/K, plotted for all via widths and lengths.

As discussed in chapter 2 the resistance of a CNT bundle can be split

into two parts as shown in eq. 2.9. One part is the contact resistance caused by the quantum resistance and the non-ideal contact between the CNT and the metal, both of which are independent of the bundle length. The other part is a length dependent part, which appears if the CNT bundle is longer than its ballistic length. As these CNT are fabricated at a low temperature they contain many defects. In the previous section it was determined that the MFP of these CNT is in the order of 2 nm. The CNT bundle length is thus much longer than its MFP.

It is known that both R_Q and λ_{CNT} depend on the temperature of the bundle, with R_Q decreasing as a result of the increase in the available conduction bands, and λ_{CNT} decreasing due to the increase in phonon scattering [155]. No predictions are presented in the literature for the temperature dependency of the metal-CNT contacts, however it can safely be assumed that this resistance is also influenced by the temperature. If a linear temperature dependency as observed in fig. 5.8, and the dependency on area (A) are added to the equation for the resistance of a bundle, the following equation can be obtained:

$$R_{bundle}(T) = \frac{1}{A}(r_C(1 + \alpha_C(\delta T)) + \rho_{CNT} l(1 + \alpha_{CNT}(\delta T))) \tag{5.2}$$

Here r_C is the sum of the contact and quantum resistance times unit area, and ρ_{CNT} is the equivalent resistivity of the CNT bundle (excluding the contact and the quantum contact resistances), both at room temperature (T_0). $\delta T = T - T_0$, while α_C and α_{CNT} are the TCR of, respectively, the contact resistance and the CNT bundle resistance. The derivative to temperature of equation 5.2 is as follows:

$$\frac{dR_{bundle}}{dT} = \frac{1}{A}(r_C \alpha_C + \rho_{CNT} l \alpha_{CNT}) \tag{5.3}$$

If the obtained TCR data is now multiplied by the area, then only the length dependency remains in the right side of the equation. In fig. 5.11 the measured data has been multiplied by the via area in μm^2 and fitted by a linear fit. Two trends in the slope are visible. For bundles between 1 and 3 μm the slope is roughly the same, while for the larger bundle widths the slope deviates from the smaller bundles, but again have similar slopes. It is very likely that a second order effect that is not incorporated in the model causes this shift in the slope.

If a fit is performed on the ensemble of data points of the vias with widths between 1 and 3 μm the following expression for the TCR per unit area can be obtained:

$$A\frac{dR_{bundle}}{dT} \sim 0.059 - 0.137l \tag{5.4}$$

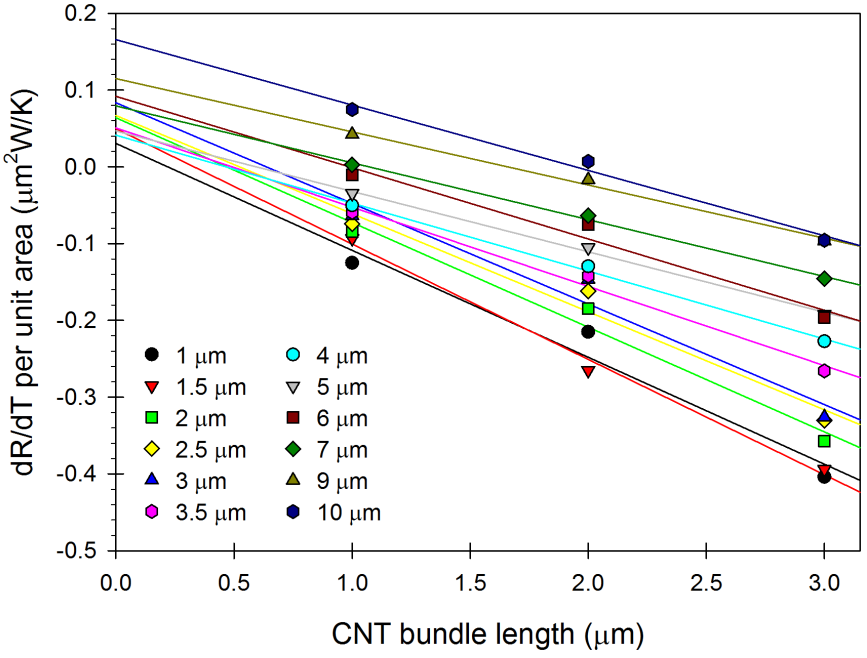


Figure 5.11: TCR normalized per unit area plotted against length. Each solid line represent a linear least squares fit.

this fit suggests that the length dependent part of the CNT bundle (and thus R_Q) gives a negative contribution to the TCR, while the contact resistance gives a net positive contribution (remember the contact resistance consists of both the length independent part of R_Q, and R_C). The resistance versus length obtained in section 5.2.4 equals ρ in eq. 5.2, and thus $\rho \approx 35.4$ mΩ-cm. Using this value in eqs. 5.3 and 5.4, an α_{CNT} can be obtained of -387 ppm/K, which corresponds closely to the values found in fig. 5.10 for the small width vias.

As can be seen from fig. 5.10 and fig. 5.11 the simple linear model does not hold for the large diameter vias. It is possible that a length dependency of the CNT contribution to the TCR exist, as was shown in simulations found in literature [155, 156]. This data set for the different lengths is too small to perform any sensible modelling on this respect. Beside the length effect there appears to be an area dependency, as can clearly be observed in fig 5.10. It is possible that interactions between CNT within a bundle influence the TCR, or perhaps more likely that the contact resistance starts

dominating the behaviour of the bundle TCR.

Unfortunately, the effect of the bundle diameter on the CNT resistance has been hardly investigated in literature. A publication by Mahanandia an Nanda [157] demonstrates a decrease in sensitivity to temperature for larger bundles, without explanation. However, their bundles widths were 10 times larger than the ones used in this study. Being the first systematic study on the TCR of manufactured CNT vias makes it difficult to compare these results to the few single values found in literature on either isolated tubes [64, 158] or large bundles [157, 159]. Additional research will be required in order to fully understand the TCR behaviour of CNT vias.

5.4 Electrical reliability

As mentioned in chapter 1, one of the arguments for the use of CNT for vias is the high current density they can withstand due to the strong sp^2 bonds. In the previous discussions on the growth and electrical resistance it already became clear that the low-temperature grown CNT used in this work contain many defects. As these defects not only increase electrical resistance, but also can decrease electrical reliability, it is important to investigate the electrical reliability of the created samples.

Reliability testing was performed in collaboration with NIST, which performed the measurements and provided FIB SEM images of the tested CNT vias. All tests were performed on the set of wafers fabricated using Fe at 500 °C, of which the patterns were defined using the contact aligner. Two kinds of test were performed: ramp to failure, and voltage hold. Both failure tests were performed using a sourcemeter on 2 μm, 3 μm, and 4 μm wide vias, fabricated in 3 μm deep holes etched in SiO_2.

5.4.1 Ramp to failure tests

Fig. 5.12 displays a plot of the ramp to failure test performed on 2 μm vias. Most vias fail between 1.1-1.2 V, with a current around 15 mA. Two exceptions were observed, which both failed around 1.8 V, of which the best performing via could handle a maximum current of 55 mA. For the best performing via this translates into a current density of $1.4 \cdot 10^6$ A/cm^2. However, as the CNT do not completely fill the via, the usual approach in literature is to divide the current by the actual area of the CNT, which for a 2 μm via equals $6.16 \cdot 10^{-9}$ cm^2 (4000 tubes with a diameter of 14 nm). This results in a current density of 8.9 MA/cm^2 for the best performing via, and 2.4 MA/cm^2 for the early failure vias. The best via thus outperforms Cu in terms of current carrying capability.

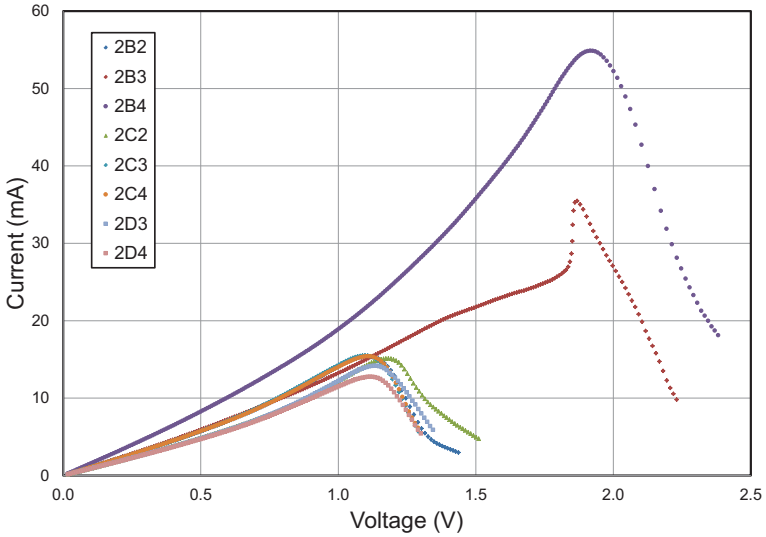


Figure 5.12: Ramp to failure tests on vias with a width of 2 μm.

The same test was performed on 4 μm vias present on the same wafer. The results are shown in fig. 5.13. Again a bimodal distribution can be observed, of which the failure potentials are similar to that of the 2 μm vias. The best via can now handle a current of 230 mA, which translates into a current density of 9.3 MA/cm^2.

In order to investigate the failure mechanism, cross-sections were made from the 2 μm vias using FIB and imaged in a SEM. Fig. 5.14 displays the SEM images of the best performing via, and a typical early failure via after ramp to failure test. The best performing via has a clear cut in the centre of the CNT bundle, which suggests Joule heating in the centre as the main failure mechanism [160].

In contrast, for the early failure vias not always a clear cut was observed, as can be seen in fig. 5.14b, suggesting failure at the contacts. All early failures were found to be of shorter length than the two best performing 2 μm vias, which was due to their location at the edge of the wafer. Most early failure vias also displayed a densification, likely due to aceton penetrating the sample after etching the top metal through small voids. This zipping could introduce additional heating due to a high local tube density, and thus introduce early failure. However, the second best performing 2 μm via also displayed local densification.

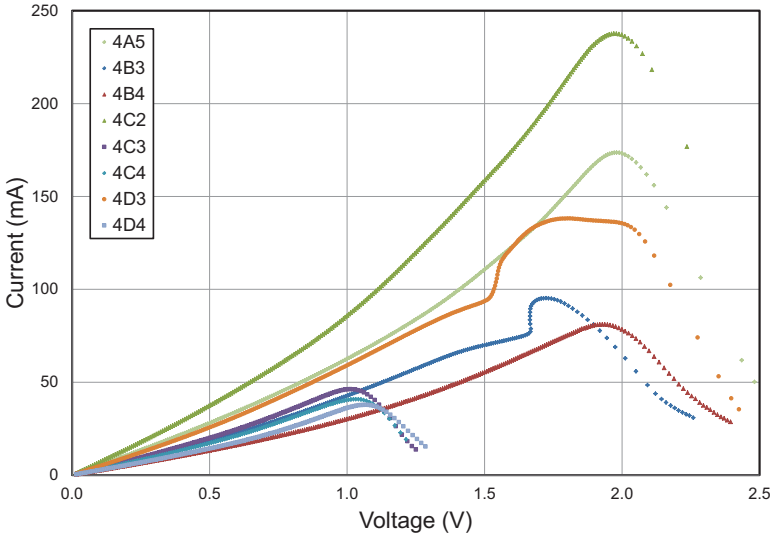


Figure 5.13: Ramp to failure tests on vias with a width of 4 μm.

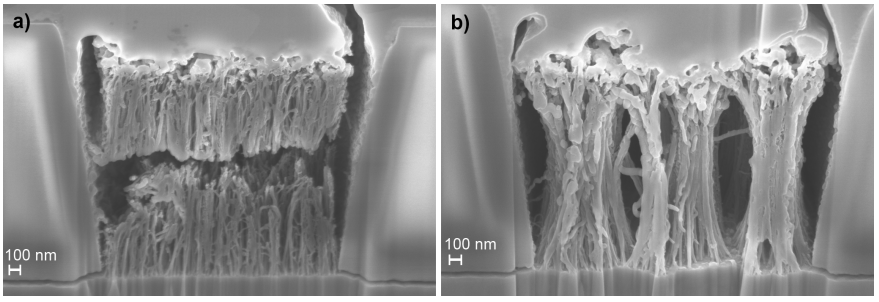


Figure 5.14: Post-mortem FIB cross-sections of 2 μm vias: a) best performing via, b) typical early failure via.

Another possibility is that the failure is electric field dependent, which can explain the length dependence. However, the best performing 4 μm via was cross-sectioned and was found to be short (again due to its location at the edge of the wafer). With the available data it appears that the best performing CNT bundles always fail in the centre of the bundle, while the early failing tubes do not necessarily display this behaviour. This indicates that there exist two failure mechanism, one of which is Joule heating, and the other likely failure at the contacts. The early failure mechanism would

thus be attributed to a bad metal-CNT interface, potentially resulting in electromigration of the metal at the contact [161].

5.4.2 Voltage hold test

To investigate the long-term stability of the CNT vias a voltage hold test was performed on a 3 μm wide via. During this test the voltage was first ramped to a value at which the via resistance started increasing (thus failure was being induced), after which the voltage was reduced to 90% of that value and kept that way for an extended period, during which the resistance was measured (both at the high voltage hold current, and periodically at a lower current).

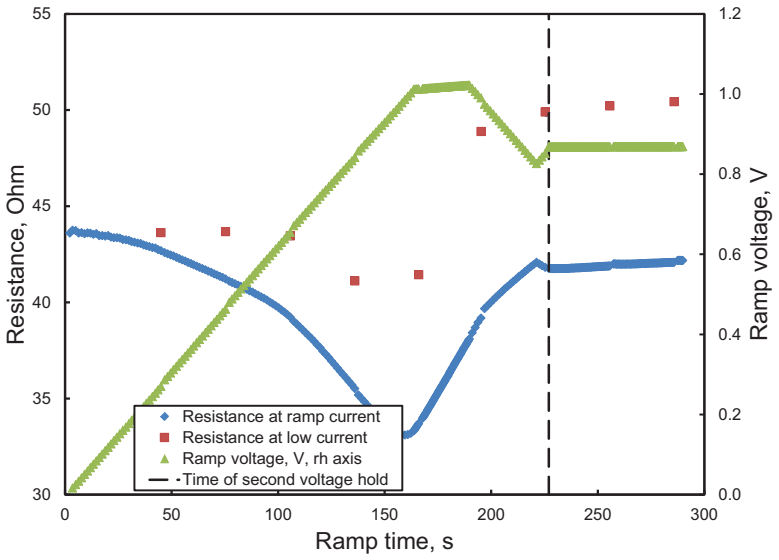


Figure 5.15: Start of volatge hold test performed on 3 μm wide via.

Fig. 5.15 displays the initial part of the test. First a decrease of CNT resistance is observed, which can be attributed to self-heating reducing the resistance due to the negative TCR of the sample (see section 5.3), this is confirmed by the large difference between the resistance for low and high current in fig. 5.15. The decrease in the low current resistance observed around 150 s can be the result of annealing improving the metal-CNT contact. After the maximum ramp current has been achieved at 160 s, a clear increase in both low and high current resistance can be observed due to the

onset of failure.

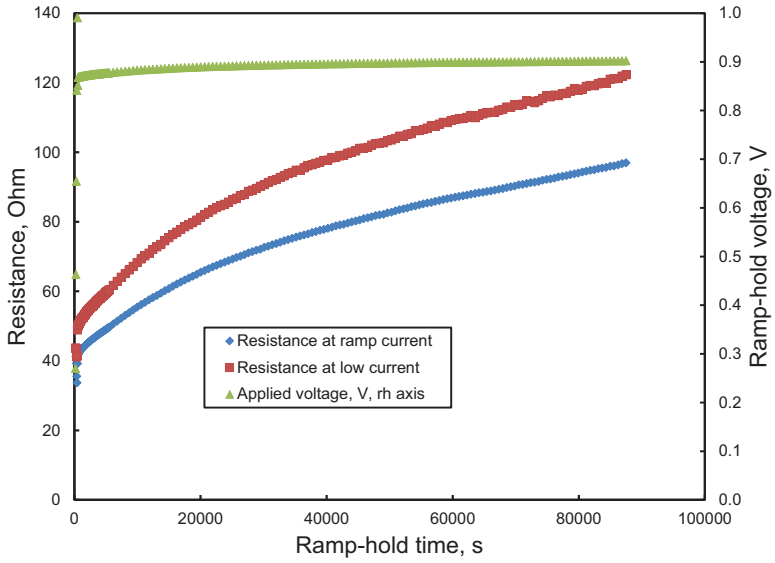


Figure 5.16: Complete 24 hours voltage hold test performed on 3 μm wide via.

In fig. 5.16 the full 24 hour long voltage hold test can be found. The CNT via resistance increases steadily over time, more than doubling from the initial failure. The increase appears to go faster in the initial part of the experiment, but increased linearly after roughly 10 hours. The clear difference between low and high current resistance can again be explained by self-heating in combination with the negative TCR. Interestingly, this difference increases with time. This can either be caused by an increase in self-heating due to the higher resistance, or by the increase in defect density making the negative TCR more profound, as was also observed in fig. 5.10 for samples fabricated at different growth temperatures.

5.5 Conclusion

In this chapter the results of electrical measurements performed on four-point probe structures were presented. From the I-V characteristics it was shown that top-down integrated vias display an Ohmic contact, while bottom-up integrated vias show a slightly non-linear resistance. The full-

wafer resistance for top-down wafers fabricated at different temperatures and lengths were investigated. Most uniformity appears to be caused by heater non-uniformity. Decreasing the growth temperature has no major effect on the uniformity of the resistance, while increasing the via length has.

Using samples fabricated with different via length the contact resistance could be approximated. It was found that the average contact resistance was one order of magnitude lower than the average length dependent resistance. This low contact resistance is attributed to a good top contact by tip embedding. From the slope of the resistance versus length the electrical mean free path could be calculated, which was compared to the L_a determined by Raman spectroscopy. The results suggest that most walls of the multi-walled CNT are contributing to conduction.

The electrical resistivity of the different samples was determined. A clear increase of resistivity with decreasing growth temperature was observed. Compared to values from literature the resistivities obtained outperform vias fabricated at significant higher temperatures, but do not outperform the lowest published values. In any case the resistance of CNT vias is 3-4 orders of magnitude higher than that of Al or Cu.

It was found that the fabricated vias have a negative TCR, which is attributed to the increase in conductions bands with temperature. This property is advantageous for the reliable operation of interconnect. Size and length dependent effects were observed in the TCR, which can partly be explained by assuming a positive temperature dependent contact resistance.

Using ramp to failure measurements the electrical reliability of the CNT vias was investigated. The best performing vias clearly outperformed Cu in terms of maximum current density, with the highest current density measured being 9 MA/cm^2. Two failure mechanisms appear to exist: one by Joule heating, and an early failure mechanism at the contacts. Stress testing was performed using voltage hold measurements at 90% of the maximum current. Although resistance increased more than twice the initial value, no breakdown occurred after 24 hours of testing.

6

Thermal characterisation of carbon nanotube vias

Using a novel vertical 3ω-method the thermal conductivity of CNT vias was measured. The chapter starts with an explanation of the method, and validation of the correctness by simulations and measurements. This is followed by thermal resistance measurements performed on vias with different lengths, from which the thermal boundary resistance could be determined. It was found that the thermal boundary resistance dominates the thermal properties. Finally, the thermal conductivity was determined to be 1.4 W/mK, which is attributed to the low quality of the CNT.

6.1 Introduction

As mentioned in chapter 1 one of the advantages of CNT is that they can potentially transport an almost ten times larger amount of heat than Cu. This is advantageous for interconnect in 3D IC, as the increase in the number of transistors per unit area increases the demands on thermal management. In chapter 2 it was discussed that the thermal conductivity of CNT depends on the number of defects. As became clear in chapter 4 and 5 the CNT used in this thesis contain numerous defects due to the low fabrication temperature.

As mentioned in chapter 2 much data is published on the thermal conductivity of individual CNT and bundles. However, none of the published results represent CNT directly grown at low temperatures, and at the desired location. Most results are obtained from tubes fabricated using arc-discharge, laser ablation, or high temperature (> 700 °C) CVD. None of these production methods are suitable for the actual fabrication of CNT vias due to the need of full wafer fabrication and low growth temperatures as mentioned before. It is thus of interest to investigate the thermal properties of the CNT used to fabricate the vias, as it cannot be assumed that the thermal conductivity of these low temperature grown CNT is the same as that of values published in literature.

In this chapter the measurements on the thermal conductivity of vertical CNT vias manufactured using the process described in chapter 4 are discussed. In order to determine the thermal conductivity, a novel vertical 3ω-method was developed which enables the measurement of thermal conductivity using pure electrical measurements. The details of this technique will be discussed in section 6.2. This is followed by simulations to demonstrate the validity of this method in section 6.3. The thermal boundary resistance will be determined in section 6.4, followed by the thermal conductivity in section 6.5.

6.2 Vertical 3ω-method

The technique used here to measure the thermal conductivity of CNT bundles was based on the 3ω-method. Traditionally, this method has been used to characterize the thermal performance of thin films. For this a metal line with known resistance and thermal coefficient of resistance was deposited on top of an electrically insulating substrate. Upon applying a known sinusoid current through the line with radial frequency of ω, the line heats up with the double of this frequency. Due to the change in resistance by temperature a third harmonic $V_{3\omega}$ is induced which can be measured using

a lock-in amplifier. The magnitude of this potential can be related to the heat sinking capability of the thin film underneath the metal line.

Recently, this method was adjusted by Lu et al. [162] in order to measure the thermal conductivity of the line itself, when it was suspended over a gap to thermally isolate it from its surroundings. The validity was demonstrated by measuring a Pt nanowire, and the technique was employed by the group of Lu and others to measure the thermal conductivity of individual [61, 64, 65], and bundles [70, 159], of horizontally suspended CNT.

The thermal properties of the CNT (bundle) can be related to the $V_{3\omega}$ by eq. 6.1, in which I_0 is the root mean square current, R the sample resistance, $R^{'}$ the sample TCR, L the length of the sample, κ the thermal conductivity, and A the cross-sectional area of the sample. This equation is valid when the measurements are performed in the low frequency limit: $\sqrt{\alpha/2\omega} \gg L$, where α is the thermal diffusivity [162], and when both ends of the CNT (bundle) are at T_0 (room temperature).

$$V_{3\omega} = \frac{4I_0^3 R R^{'} L}{\pi^4 \kappa A} \tag{6.1}$$

For performing the thermal measurements a SR830 lock-in amplifier at high dynamic reserve, with 1 second time constant and 24 dB/oct filter was used. To generate the known current a custom improved Howland current pump was used, which changed the reference 1 kHz sinusoide voltage output of the lock-in amplifier into a known current with an accurate resistor with low TCR. The structure was probed using the semi-automatic probe station, a schematic overview of the setup is shown in fig. 6.1. Data collection was performed using a National Instruments LabView VI which communicated directly with the SR830 and controlled the reference voltage. The sensitivity was set automatically by the instrument.

6.3 Experimental validity

Whereas in regular 3ω measurements the CNT (bundle) is orientated horizontally over a gap in vacuum [61, 64, 65, 70] these bundles are vertically oriented between two metal heat sinks and isolated from thermal conduction by a (vacuum) gap. Although the exact orientation of the bundle, of course, does not influence the measurements, the heat sinking properties of the contacts may be different. Equation 6.1 only holds in case the contacts are thermal sinks at temperatures T_0. While it can be assumed that this is true for the bottom contact, as it is in direct contact with the Si bulk, this is not necessarily the case for the top contact, which is formed by a 3 μm Al(1% Si) line.

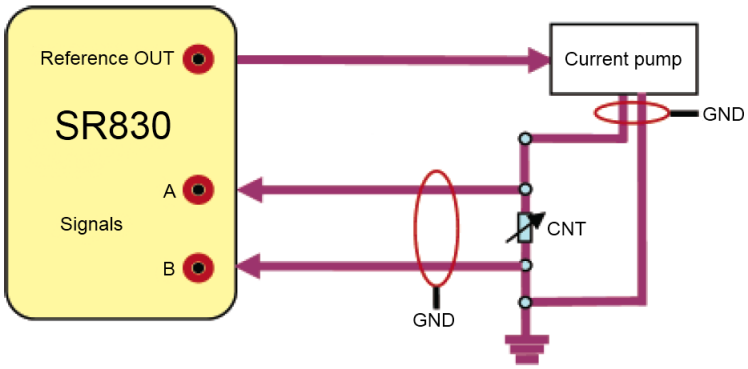


Figure 6.1: Schematic overview of the measurement setup.

Finite element simulations were performed by COMSOL Multiphysics 4.3 as part of a summer internship by Sourish Banerjee to verify the potential increase of temperature of the top contact. A cross-section model was constructed for this, and the thermal conductivity of the CNT bundle was modelled as a solid, with a thermal conductivity of 0.5 W/mK. For all other materials the bulk conductivities were assumed.

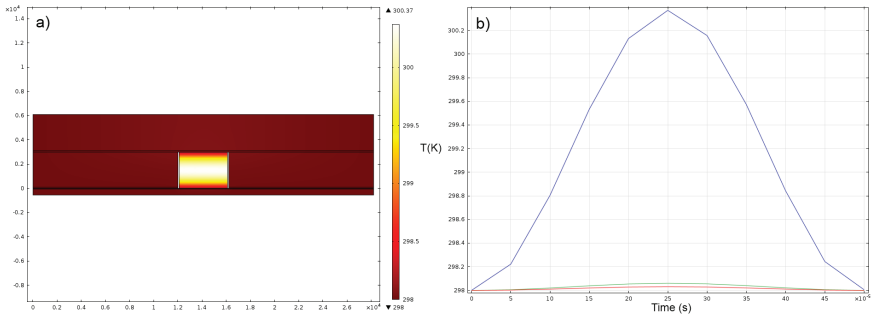


Figure 6.2: (Color online) Finite element simulation of via cross-section: a) temperature distribution at peak of sinusoide current, b) temperature at different locations in cross-section: centre of bundle (blue line), bottom electrode (green line), and top electrode (red line).

Figure 6.2 displays the simulation results for a 4 μm wide via, with a maximum current density equal to an I_0 of 1 mA. As can be seen from fig. 6.2a the heat is localized inside the bundle. In fig. 6.2b the temperature against time at three different locations (centre of the bundle, top

contact 100 nm from bundle, and bottom contact 100 nm from bundle) are displayed. The two contacts only display a minor increase in temperature (< 0.1 K), which are moreover close to each other. Finally, the self-heating of the CNT bundle is small. If the current is increased to 2 mA instead, the maximum temperature in the centre increases to 307.5 K and goes up rapidly for even higher currents.

For accurate measurements it is necessary to select an excitation frequency and current range for the applied sinusoid current. The frequency has to be selected in a way that the CNT are not excited at a resonant frequency of the circuit, and where the reactance is zero. As is shown in fig. 6.3 the samples show no resonant peaks, due to the excellent shielding of the probe station. The resistance is the most stable in the range of 100 Hz to 10 kHz. The current should be low enough so it doesn't induce an excessive amount of self-heating in the bundle, which will result in an error due to radiative losses [162], while still inducing a measurable third harmonic.

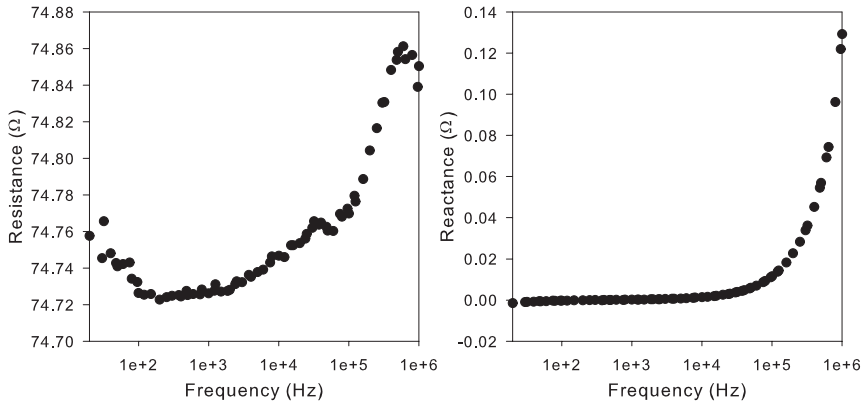


Figure 6.3: Impedance spectra of a typical 2 μm wide via obtained using a LCR-meter.

In order for equation 6.1 to be valid the frequency has also to be selected in such a way that the measurement is performed in the low frequency limit: $\lambda \gg L$. The mass density of the CNT is estimated to be 261 kg/m^3 by calculating the mass of a single CNT and the bundle density [163]. The specific heat of MWCNT bundles has been shown to be close to that of graphite (0.7 J/gK) [164]. If κ is assumed to be in the range of 1-100 W/mK, then α ranges from 5.5×10^{-6}m^2/s to 5.5×10^{-4}m^2/s. For the length of these CNT bundles (a few μm) this would put the measurement in the low frequency limit for frequencies of 1 kHz or lower. No phase change

in $V_{3\omega}$ was measured by the lock-in amplifier at this frequency, confirming the measurement is in the low frequency limit [162].

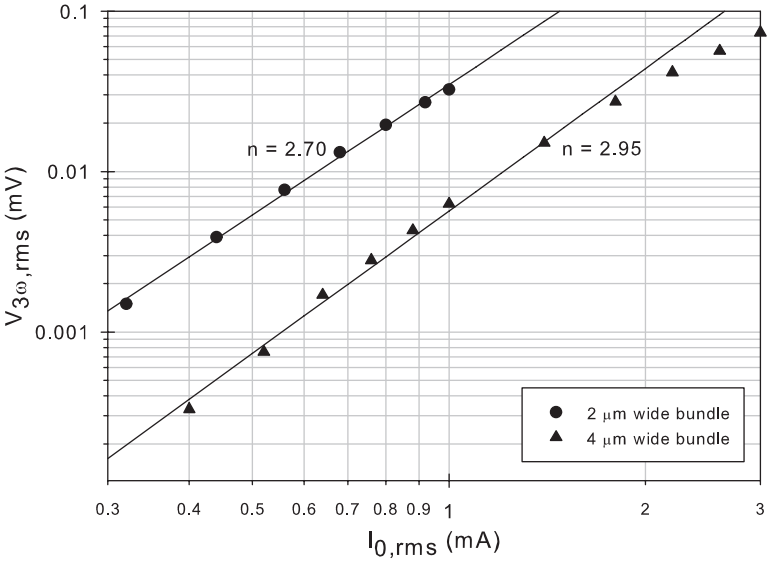


Figure 6.4: Measured third harmonic as function of the applied current.

Figure 6.4 displays the measured third harmonic voltage from CNT vias with a width of either 2 μm or 4 μm grown inside a 3 μm thick oxide. The data was fitted to a power-law using least-squares fitting, as indicated by the solid lines. The fitted power-law indices are close to the theoretical value of $n = 3$. For the 4 μm wide sample a clear deviation from the predicted behaviour can be observed for higher currents, which is likely caused by self-heating of the sample and agrees with the simulations performed. For each sample the measurements range was chosen in such a way that self-heating was kept to a minimum, while still being able to measure the $V_{3\omega}$ accurately. This can be verified by checking the slope of the line, as was done in fig. 6.4.

6.4 Thermal resistance

Thermal measurements were performed on the same samples used to determine the electrical contact resistance in section 5.2.3. Of these samples also TCR measurements were performed, which showed the same behaviour as

the waferstepper fabricated samples discussed in section 5.3. Using the vertical 3ω-method with the electrical resistance and TCR of each individual CNT bundle (i.e. not the average data) the thermal performance of each measured bundle with different length and width could be obtained. By removing the length and area from eq. 6.1 the thermal resistance of each sample can be obtained. Here $\Re$ is used to denote thermal resistance to avoid confusion with the electrical resistance R:

$$\Re_{bundle} = \frac{4I^3RR'}{\pi^4 V_{3\omega}} \tag{6.2}$$

For each CNT bundle length and width $\Re_{bundle}$ was measured of five different samples. The consistency with the predicted behaviour, that is $V_{3\omega} \propto I^3$, was checked for each measurement [162]. Fig. 6.5 displays the average measured thermal resistance for each different bundle width, against the bundle length.

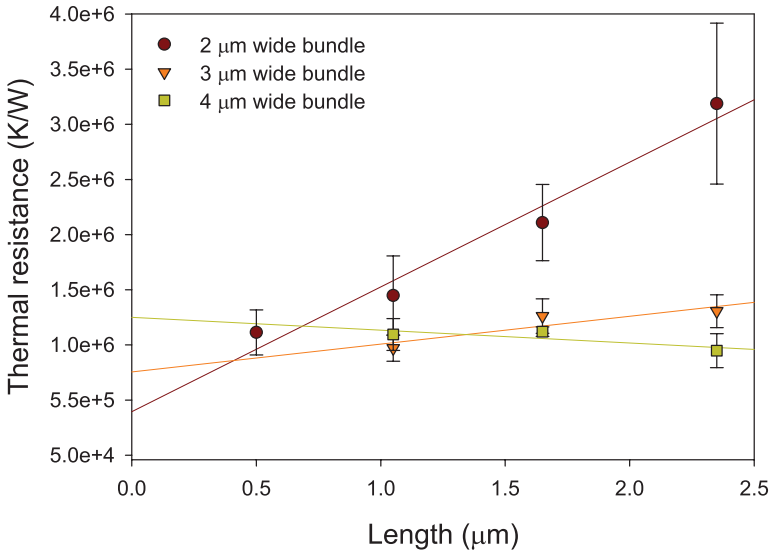


Figure 6.5: Average thermal resistance for each bundle length and width, plotted against the length of the bundle.

Similar to the electrical resistance, the thermal resistance of a CNT bundle ($\Re_{bundle}$) can be defined by a TBR ($\Re_C$) and a length-dependent part:

$$\Re_{bundle} = \Re_C + \frac{1}{\kappa_{CNT} A} l \tag{6.3}$$

From the measurement results displayed in fig. 6.5 it appears that the thermal boundary resistance dominates the thermal behaviour of the 3 μm and 4 μm via, as the thermal resistance does not change measurably with length. This is in strong contrast to the electrical resistance and thermal gradient of the electrical resistance, which both show a significant change with length as shown in chapter 5. The 2 μm wide bundle, on the other hand, displays a clear length dependency. The $\Re_C$ of the measured CNT bundles appears to be in the order of 10^6 K/W, which translates into a per-tube TBR of $10^9 - 10^{10}$ K/W, which is considerable higher than the TBR values found in literature for individual tubes and fibres of $10^6 - 10^7$ K/W [63, 72, 73].

The high TBR thus appears to dominate the thermal resistance of the measured CNT vias. It has been shown that a metal-CNT contact can have a large TBR due to the difference in heat carriers, which are phonons in CNT and electrons in metals, resulting in a weak coupling [71]. Another explanation for the high TBR is the low contact area, especially at the bottom contact. It has been shown that coating the ends of a CNT with metal can improve the heat transfer between the CNT and the metal [63].

6.5 Thermal conductivity

Using the TCR and $V_{3\omega}$ measurement data, together with equation 6.1, the thermal conductivities of the CNT inside the bundle can be obtained. The bundle length L was assumed to be equal to the electrical length used to determine the electrical contact resistance. As the CNT bundle is sparse, the actual cross-sectional area is not equal to that of the opening etched in the oxide. The following equation was used to approximate the cross-sectional diameter of the bundle ($A_{CNT,bundle}$):

$$A_{CNT,bundle} = \frac{\pi d^2}{4} D w^2 \tag{6.4}$$

in which d is the average CNT diameter (14 nm), D the density (10^{11} tubes/cm^2), and w is the width of the opening.

Fig. 6.6 displays the average calculated thermal conductivities based on the assumptions mentioned in the previous paragraph. The values range roughly from 0.5 W/mK to 1.5 W/mK. For the 2 μm bundles the value is constant, except for the shortest via, while the thermal conductivity increases for the 3 μm and 4 μm wide vias. This increase is caused by the more or less constant thermal resistance for these vias. The contribution of the CNT is thus shadowed by the large TBR. An estimation of the contribution of the CNT can be made from the slope of $\Re_{bundle}$ for the 2 μm

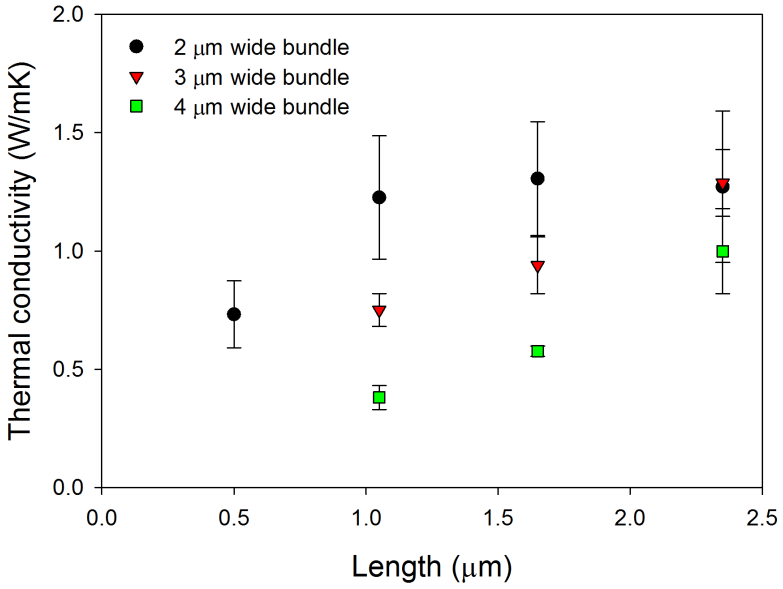


Figure 6.6: Average calculated thermal conductivity for each bundle length and width, plotted against the length of the bundle.

via in Fig. 6.5, which is $1.13 \cdot 10^6$ K/μmW. Using the area from eq. 6.4 in combination with eq. 6.3, this results in a thermal conductivity for the CNT bundle of 1.4 W/mK.

The values for the thermal conductivity are lower than values previously reported, obtained from CNT fabricated at higher temperatures, which are typically between 30 W/mK and 600 W/mK [66–70]. The growth temperature used to fabricate the CNT in this study is much lower than growth temperatures previously reported. From Raman spectroscopy and electrical measurements, the electron mean free path was estimated to be on the order of 2 nm, much lower than previously reported values which can be as high as 25 μm [165]. The reported thermal conductivities here are close to that reported before for CNF, which indeed were found to have a short phonon mean free path of just a few nm [63], even though these samples consist of MWCNT.

6.6 Conclusion

A novel vertical approach of the 3ω-method was proposed, and verified using simulations and measurements. This method was used to analyse the thermal properties of CNT vias fabricated with different lengths and widths. It was found that the thermal boundary resistance dominates the thermal performance of the CNT vias, being as high as 10^6 W/K per via, and $10^9 - 10^{10}$ W/K per CNT. This can be attributed to the mismatch in heat carriers in the CNT and metal, which are respectively phonons and electrons. Another cause can be the low contact area between the TiN and the bottom of the CNT bundle.

Using the approximate CNT area the thermal conductivity of the CNT bundles could be calculated. It was found that the thermal conductivity ranges from 0.5-1.5 W/mK for the entire via, with a calculated CNT contribution of 1.4 W/mK. These values are considerable lower than the values mentioned before in chapter 2. This can be explained by the low quality of the CNT.

7

CNT as vias in monolithic 3D IC

The integration results of low-temperature CNT vias into monolithic 3D single-grain thin-film transistor technology is discussed in this chapter. Integration was found to be challenging, due to the SG-TFT process affecting the TiN layer and thus the growth. Electrical measurements were performed on test vias integrated alongside the active devices, demonstrating that via resistivity does not increase significantly compared to the measured test vias of chapter 5. This is followed by the measurement results on individual transistors, fabricated in both a single-layer as double-layer process. It was found that the via resistance influences the SG-TFT performance. Finally, more complex structures like CMOS inverters and 6T-SRAM cells are measured.

7.1 Introduction

As mentioned in chapter 1 one of the goals of this thesis is to integrate CNT as vias into monolithic 3D integrated circuits and check the subsequent performance. For the fabrication of the active devices for these SG-TFT are used, which offer Silicon-on-Insulator-like performance and have previously been used to fabricate double-layer 3D circuits [8, 9]. For these devices the vias consisted of Al (1% Si), which can only be fabricated in a limited aspect ratio as the metal is sputtered into the contact openings.

In this chapter the low-temperature (≤ 500 °C) CNT growth techniques described in chapter 4 are integrated into the 3D IC SG-TFT technology. This proved to be a difficult task, as the steps of the SG-TFT process were found to interfere with the growth of CNT. Therefore, a section is dedicated to the fabrication details of the 3D process with the different iterations and the process which in the end resulted in working devices.

This is followed by the electrical characterisation of the fabricated devices. First the performance of test vias fabricated alongside the SG-TFT are measured. Second, individual transistor measurements will be shown, both of a single layer of SG-TFT with CNT vias, as double-layer SG-TFT. This is followed by the measurements on 3D Complementary Metal Oxide Semiconductor (CMOS) inverters, with the active areas being positioned directly on top of each other and connected with CNT vias with different diameters. After this, more complex 6T-Static Random Access Memory (SRAM) cells are demonstrated.

7.2 Fabrication details

The SG-TFT 3D process consists of the fabrication of two layers of transistors by using the μ-Czochralski process, as shown in fig. 7.1. In this process ≈ 100 nm wide holes, dubbed grain filters, were fabricated by etching 1 μm wide holes in an oxide layer, followed by 830 nm PECVD oxide filling. Over this, a layer of a-Si is deposited using LPCVD at 545 °C. Upon excimer laser exposure the a-Si melts, and recrystallizes into a grain of single crystal orientation from this grain filter (fig. 7.1c-d). Due to this the crystallinity of the Si inside a single grain is high, allowing electron mobilities as high as 400 cm^2/Vs. In the 3D SG-TFT process two of these layers are fabricated on top of each other, separated by 1.2 micrometer of oxide. As the second layer deposition temperature is too high to use Al in the first layer, the gate and interconnects in this layer are fabricated from poly-Si, while for the top layer Al can be used.

As mentioned before in chapter 4 CNT can be grown directly on a TiN

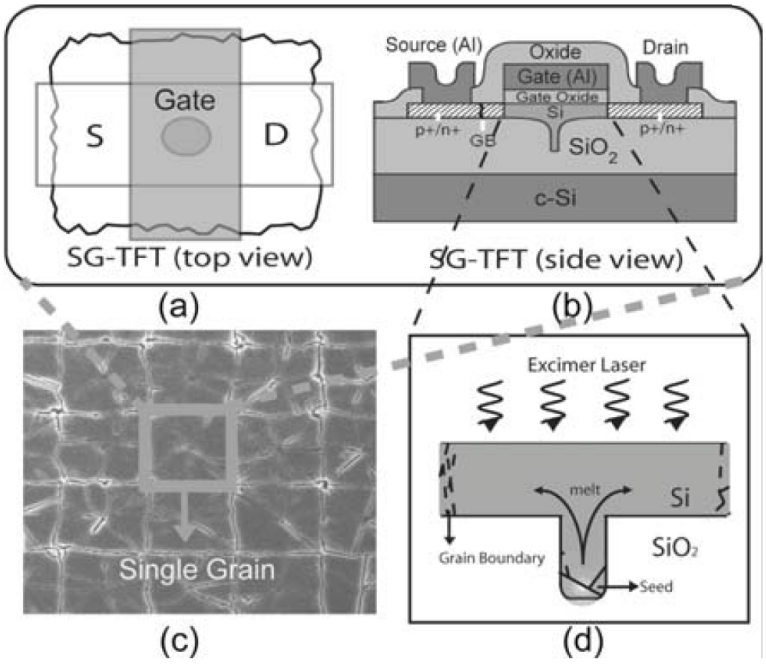
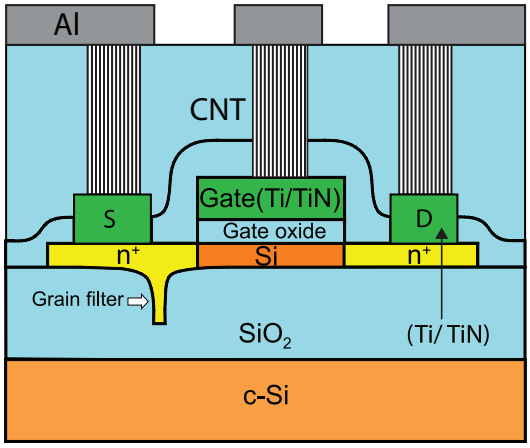


Figure 7.1: Overview of μ-Czochralski SG-TFT process: a) SG-TFT top view, b) cross-section, c) SEM image of single-grains formed after laser crystallization, d) schematic of laser crystallization.

layer. The first approach to integrating CNT into the SG-TFT technology was simply by replacing all traditional poly-Si metallisations by a stack of Ti/TiN/Ti (250/50/100 nm). As Ti has a much higher melting point, the metal lines should survive the relative high temperature LPCVD Si deposition.

It was possible to fabricate a single layer of SG-TFT with CNT vias using this approach, as depicted in fig. 7.2. However, several problems were encountered. First of all, the yield of working transistors and circuits of the single-layer process was low. It appears that the Ti layer was very prone to residue formation around steps (e.g. hillocks around the grains, or the etched gate and Si islands), which proved to be hard to remove by additional dry or wet etching, resulting in shorts. Secondly, the growth rate (200 nm/min instead of 400 nm/min) and alignment of the CNT vias deteriorated as shown in fig. 7.2c. The most serious problem was that

after depositing the second a-Si layer the stress in the Ti film was increased to such an extent that the TiN cracked. During the wet etching of the sacrificial Ti layer on top of the TiN this resulted in complete removal of the Ti layer underneath the TiN.



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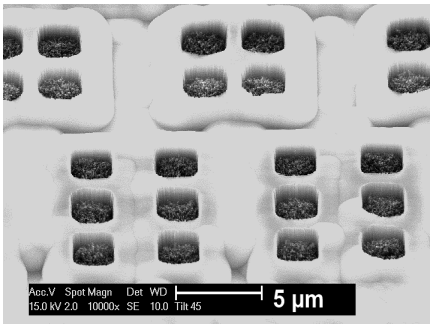

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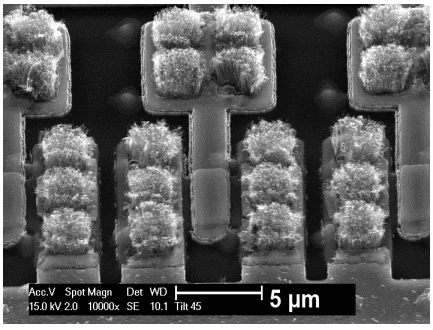


(c)

Figure 7.2: Single-layer SG-TFT with Ti/TiN metallisation and CNT vias: a) design; b) SG-TFT with top-down CNT vias; c) SG-TFT with bottom-up CNT vias.

A pure Ti/TiN/Ti metallisation was thus abandoned, and replaced by 250 nm thick poly-Si interconnect, covered by Ti/TiN/Ti (10/50/100 nm) where the 10 nm of Ti is an adhesion layer. Still, electrical short were found to be a problem with this approach. This resulted into a redesign of the

process where Ti/TiN was being kept away from the active regions. This was achieved by first fabricating the bottom layer Si island and poly-Si gate, followed by 600 nm of TEOS oxide in which contact openings were etched. Into these openings a Ti/TiN/Ti layer (10/50/100 nm) was deposited, as shown in fig. 7.3a.

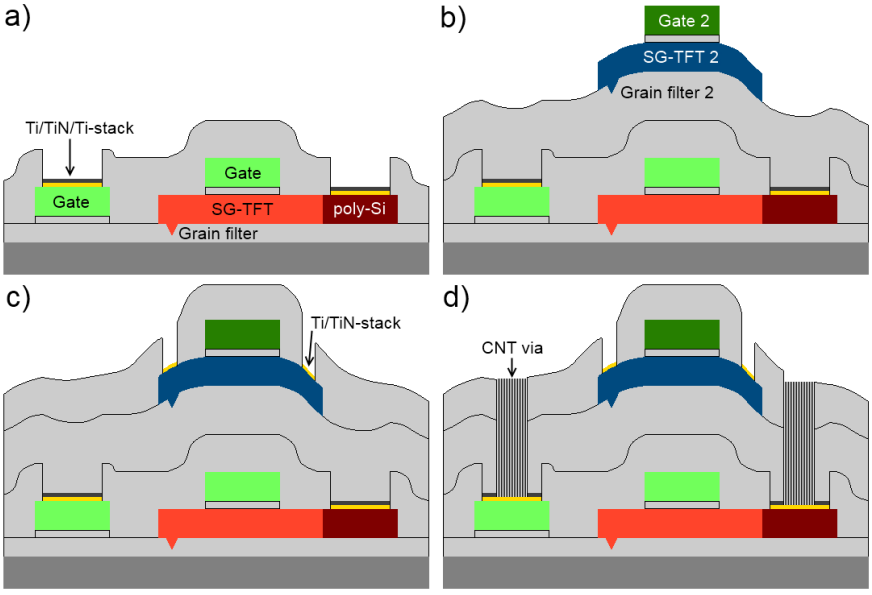


Figure 7.3: Cross-sectional view of final 3D SG-TFT process: a) after SG-TFT formation and deposition of Ti/TiN/Ti-stack; b) after fabrication of second-layer SG-TFT; c) after deposition of Ti/TiN oxidation barriers; d) after growth of CNT vias, before metallization. Layer thicknesses are not to scale.

After this the interlayer isolation and second layer grain filters were fabricated, followed by a second layer of SG-TFT with poly-Si gate, fig. 7.3b. Again a 600 nm oxide layer was deposited over these top-layer transistors, contact openings were defined and Ti/TiN was deposited, see also fig. 7.3c. The purpose of these Ti/TiN pads is to prevent oxidation of the contacts to the top layer SG-TFT, as after CNT growth no HF dip-etch or RF plasma native oxide removal can be used. Next, the openings to the first layer are etched, followed by wet Ti removal and catalyst deposition. After this catalyst deposition and lift-off are performed, followed by CNT growth (fig. 7.3d). Finally, the CNT vias and top SG-TFT are connected with each

other by a layer of 2 μm of Al (1% Si). Fig. 7.4a shows the design of an inverter using this process.

The above described process resulted in the successful removal of the Ti layer on top of the TiN, and prevented the formation of shorts by Ti residues. However, a new problem was found as only random growth was observed on top of the TiN pads with Fe as catalyst. This is attributed to a change in properties of the TiN layer during the SG-TFT process, influencing the growth as was also seen before after plasma treatment of the TiN in section 4.5.

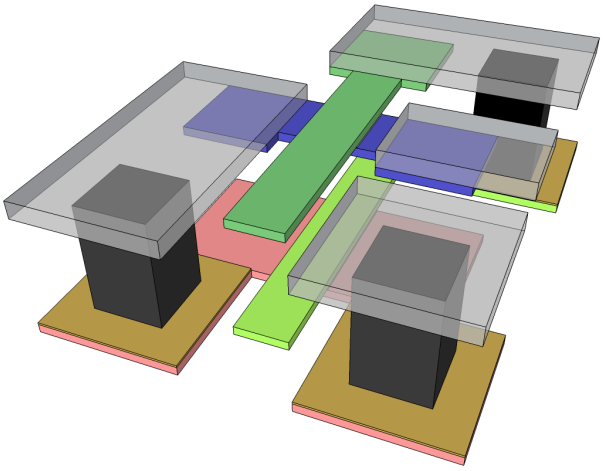
The second layer a-Si LPCVD deposition was found to alter the TiN, but still vertically aligned CNT could be obtained, albeit with decreased growth rate. It was thus assumed that the combination of LPCVD a-Si deposition, and second layer crystallization and/or dopant activation by excimer laser, damaged the TiN in such a way that CNT growth was prevented. Several other protective layers were tested, including AlN, but it was found that no aligned CNT growth could be obtained after these layers were exposed to only an LPCVD a-Si deposition. Using no protection layer at all gave growth which appeared to be unaffected by the LPCVD process. Unfortunately, the TiN layer proved to be a good absorber for the wavelength of the excimer laser, resulting in destruction of the TiN layer (and the oxide covering it).

Switching to 5 nm thick Co as catalyst was found to be the solution. While Fe as catalyst only resulted in random CNT, the Co catalyst appears to be less sensitive to changes in the TiN layer and gave vertically aligned growth. Fig. 7.4b-c display images of 3D SG-TFT with CNT vias. All process iterations are summarized in table 7.1, and the flowchart of the final process can be found in appendix A.2.

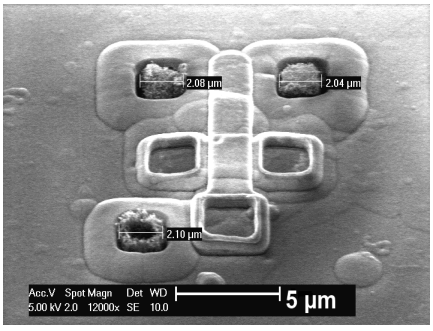
A cross-section prepared using wafer cleaving is shown in fig. 7.5. The square boxes indicate the SG-TFT areas. While the bottom-layer transistor and gate are relative easy to observe, the top transistor is less clear due to the bending of the Si island. This is due to the lack of planarization in this process, which was found before not to hamper SG-TFT performance. The bright area around the bottom of the CNT via is the Ti/TiN-stack. The via itself is likely damaged due to the mechanical cleaving.

Table 7.1: The four iterations of the 3D SG-TFT process as discussed in the text, with differences and issues.

Nr.	Bottom metal	Location of metal	Catalyst	Issues
1	Ti/TiN/Ti	full	Fe	Shorts, TiN cracking
2	poly-Si/Ti/TiN/Ti	full	Fe	Shorts
3	poly-Si/Ti/TiN/Ti	only at contacts	Fe	Random growth
4	poly-Si/Ti/TiN/Ti	only at contacts	Co	None



(a) Red: p-type Si, blue: n-type Si, green: gates, brown: Ti/TiN stack, black: CNT vias, grey: Al (1% Si). All layers thickness's and dimensions are to scale.



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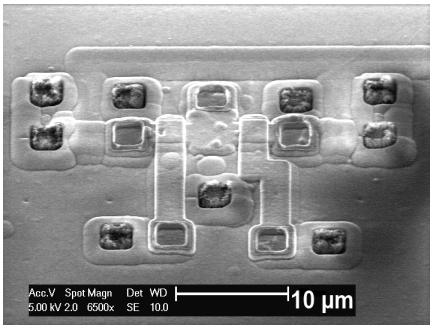

(c)

Figure 7.4: Double-layer SG-TFT with poly-Si/Ti/TiN metallisation and CNT vias: a) design of 3D inverter; b) SEM top view of 3D inverter with top n-Type Metal Oxide Semiconductor Field-Effect Transistor (NMOS); c) SEM top view of 3D 6T-SRAM cell with top p-Type Metal Oxide Semiconductor Field-Effect Transistor (PMOS).

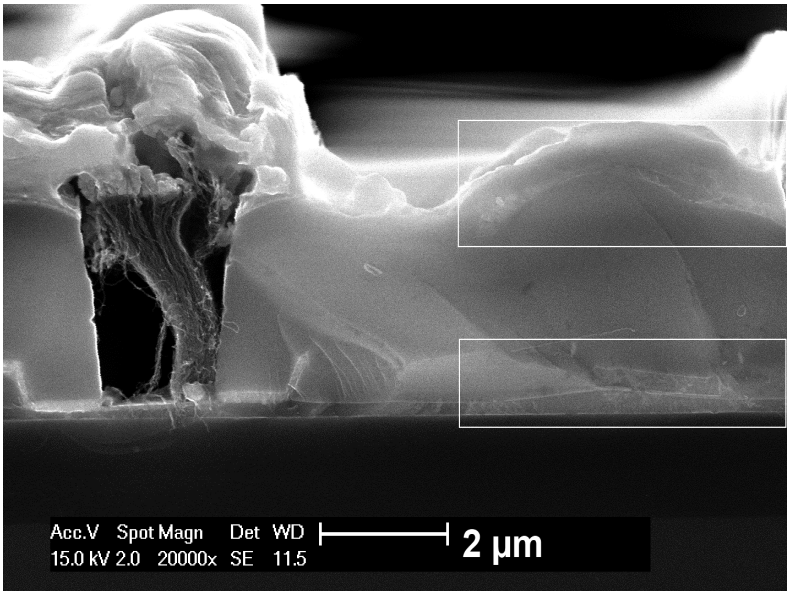

Figure 7.5: SEM image of a cross-section prepared using wafer cleaving. The square boxes indicate the position of the two SG-TFT.

7.3 Electrical characterisation

Electrical measurements were performed on the wafer fabricated with an all-Ti metallization with single-layer SG-TFT and CNT vias grown with Fe as catalyst, and a wafer with 3D SG-TFT with CNT vias grown with Co as catalyst. First the electrical measurement of CNT via test structures available on the wafer alongside the devices will be discussed, followed by the electrical characterisation of the individual SG-TFT transistors for both a single-layer and double-layer process, CMOS inverters and 6T-SRAM cells.

7.3.1 CNT test vias

On the wafers for 3D SG-TFT fabrication, four-point measurement structures were available with CNT vias to both the gate and metal layer of the bottom layer of transistors. As both layers are approximately on the same level as shown in figs. 7.2 and 7.3, a CNT via can be fabricated to both layers with a single growth process. Resistance measurements were performed

on the via test structures in order to investigate if the additional processing influenced the CNT via resistance.

Fig. 7.6 displays the calculated resistivities obtained from the resistance measurements, assuming a via height of 1 μm and 2.5 μm for the single-layer and double-layer process, respectively. As can be observed from the figure, in all cases the resistivity is higher than that of the test vias measured in chapter 5 at 500 °C.

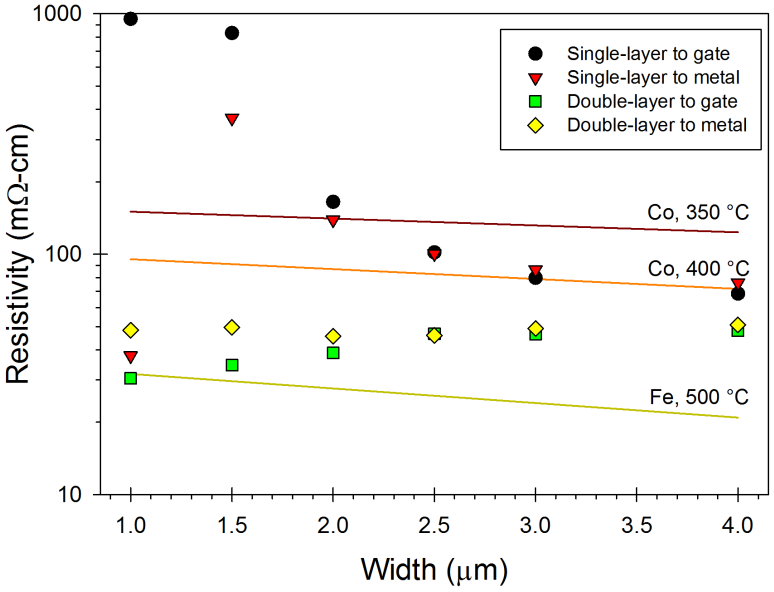

Figure 7.6: Calculated resistivities obtained from CNT vias to the bottom gate and metal levels from single and double layer processes, compared to result obtained in chapter 5.

For the single-layer process a steep increase in via resistivity can be observed with decreasing diameter for vias to both layers. The exact cause of this increase is unknown, but is likely caused by problematic CNT growth in small openings. The increase in resistivity for the vias to the metal layer is the smallest, and actually displays an anomalous point for the 1 μm wide vias. The differences in the resistivities for both layers is likely caused by the different point in the process where these layers were deposited. The gate layer is deposited before implantation, and is thus also exposed to excimer laser annealing which can heat up the Ti/TiN/Ti stack. The steep drop in resistivity for the 1 μm wide via could be caused by problematic filling of the

openings by CNT, allowing the metal deposited over the CNT to provide an additional conduction path. Indeed, measurement on parallel vias with the same surface area as single vias display a smaller resistance, while for all test vias in chap. 5 the opposite was observed. This can indicate a circumference dependent conduction, which can be caused by metal deposition at the sides of the CNT bundle.

The double-layer process displays a significant lower resistivity, which is moreover more stable over the range of via widths measured. It is difficult to compare the resistivity to measurements from chapter 5, as no test vias grown at 500 °C with Co were fabricated before, and could not be fabricated anymore within the scope of this thesis. The differences between the vias to the two different layers are smaller, which can be attributed to the fact that the Ti/TiN/Ti stack to both Si island and gate are deposited at the same time.

Interestingly, a bimodal distribution was observed for the resistances of the double-layer CNT vias centred around a low and high resistance value, which are separated by at least one order of magnitude. For the single-layer vias discussed previously a distribution around one centre value was found. The low resistance I-V curves normally displayed a linear response, while the high resistance curves often had slight non-linearities. This indicates that for the high resistance vias the contacts between the metal-CNT interfaces are not perfect.

Table 7.2 summarizes the resistance data for the double-layer vias to the metal and gate levels. The number of low-resistance vias, expressed by the yield percentage, appears to decrease for larger vias. This could be caused by larger vias having a less uniform CNT bundle, as could already be observed in fig. 7.4b for the 2 μm wide vias, resulting in a poor electrical contact between the tip of the bundle and Ti/Al metallization. The vias to the Si island show the highest average resistances and lowest yield. This is likely caused by the Si island being more rough due to the laser crystallization, which locally melts the Si. As no grain filters were present underneath the via test structures, the Si surface roughness increases as no grains are formed. This additional roughness will also be present in the relative thin Ti/TiN metallization, and could hamper the growth of CNT.

7.3.2 Single-layer transistors

The mask design for the 3D SG-TFT process included single transistors with the same design as the 3D inverter in fig. 7.4a in which one of the two active layers was omitted. For each layer both PMOS and NMOS were available, and for the bottom transistor layer the transistor gate and source/drain

Table 7.2: Via low and high average resistances with their subsequent standard deviations (SD) and yield percentage indicating amount of low resistance vias. For each type 52 vias were measured.

	Width (μm)	Low avg. (Ω)	Low SD (Ω)	High avg. (kΩ)	High SD (kΩ)	Yield (%)
Gate	1	761	176	49.5	-	98
	1.5	384	53.4	52.4	24.6	90
	2	243	35.3	10.5	6.62	69
	2.5	187	48.1	6.95	5.04	48
	3	129	12.4	3.64	2.09	46
	4	75.1	9.81	1.99	0.70	44
Island	1	1207	404	108	120	48
	1.5	551	108	82.6	83.5	83
	2	285	39.7	9.54	3.03	87
	2.5	184	17.0	8.28	5.92	71
	3	136	15.5	4.24	2.34	35
	4	79.4	6.35	3.67	2.74	37

were contacted by CNT vias with widths of 1, 2 or 3 μm. This section discusses the measurements obtained on these transistors using a single layer of SG-TFT with Fe grown CNT vias, and the double layer SG-TFT with Co grown CNT vias. As reference measurements on the top SG-TFT of the double-layer process, which have no CNT vias, are included.

7.3.2.1 Single-layer TFT with CNT vias

Using a top-down approach SG-TFT test structures with 1 μm, 2 μm, and 3 μm wide CNT vias were fabricated and characterized. The I_D-V_G characteristics of an NMOS and PMOS can be found in fig. 7.7 and 7.8, respectively. The channel length is 1.5 μm, while the channel widths are 2 and 4 μm for NMOS and PMOS. When performance indicators like mobility, threshold voltage (V_{th}), Subtreshold Slope (SS) and on/off ratio ($I_{on/off}$) are compared to results published before for SG-TFT with normal Al metallization [9], it can be found that the transistor performance is very similar. This indicates that the CNT growth process has no destructive influence on the SG-TFT performance.

As the CNT bundle resistivity and thus resistance is higher than regular metals it might limit the maximum current of the SG-TFT. Fig. 7.9 displays the I_D-V_D for two NMOS SG-TFT with 1 μm and 2 μm wide vias and similar

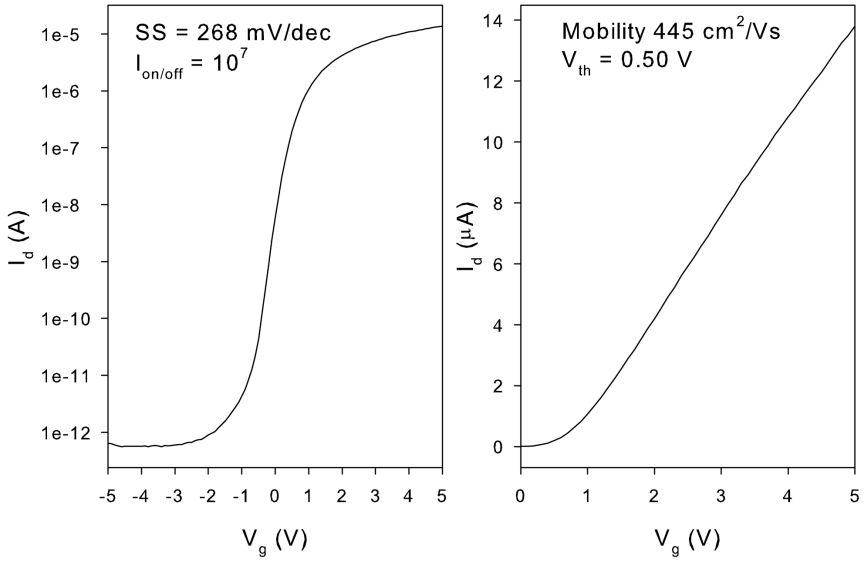

Figure 7.7: I_D-V_G of a NMOSFET SG-TFT transistor with 1 μm^2 CNT vias. V_D = 0.1 V.

mobilities (445 cm^2/Vs and 479 cm^2/Vs, respectively) and V_{th} (0.50 V and 0.84 V, respectively). The maximum current is substantially higher for the SG-TFT with wider vias. The same was found for PMOS SG-TFT (not shown here). The only difference between SG-TFT with different via size is the width of the CNT bundle, the Ti/TiN contact pad on the SG-TFT source and drain is held constant. Thus, via resistance should be reduced in order not to limit the performance of the SG-TFT with minimal size vias.

As mentioned before the yield of the Ti metallization process was problematic, for the NMOS approximately 16 % of the transistors worked, while this was $<$ 10 % for the PMOS. The most prominent failure mechanism was a short between gate and source/drain, which is attributed to problems with the Ti metallization.

7.3.2.2 Double-layer TFT with CNT vias

For the double-layer process the CNT vias with different widths were again fabricated using a top-down approach but now with Co as catalyst, as described in section 7.2. The I_D-V_G characteristics were similar as those of the single-layer transistors and are thus not shown here. Instead the extracted

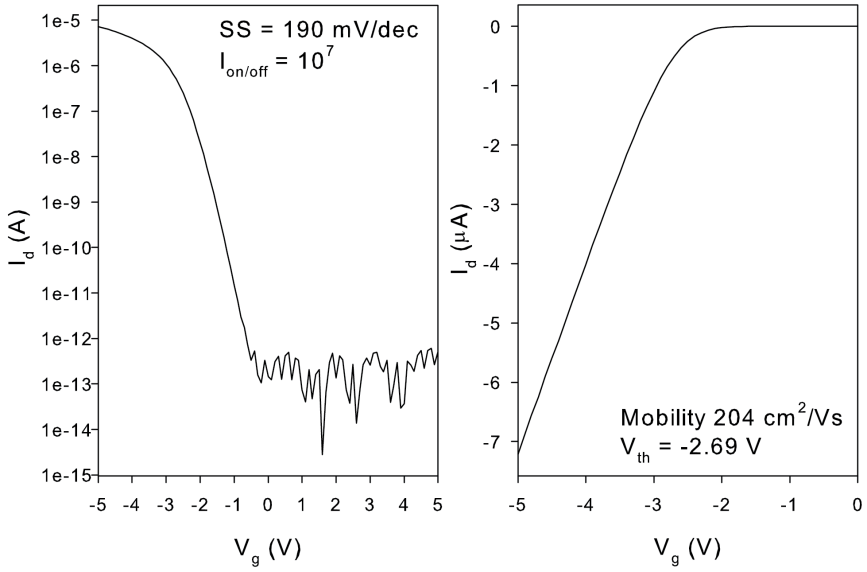

Figure 7.8: I_D-V_G of a PMOSFET SG-TFT transistor with 1 μm^2 CNT vias. V_D = -0.1 V.

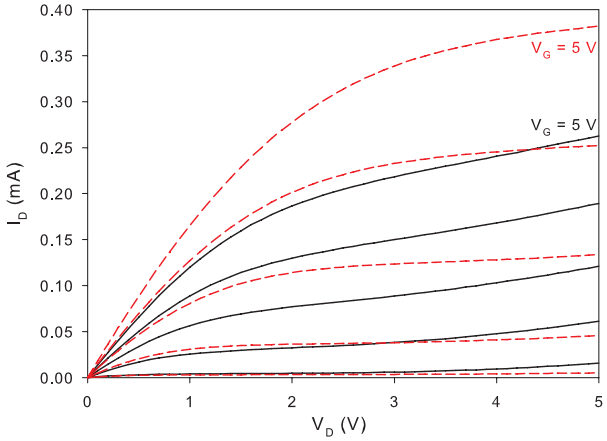

Figure 7.9: I_D-V_D of a NMOS SG-TFT transistor with 1 μm (solid line) and 2 μm (dashed line) wide CNT vias. V_G ranges from 1 V to 5 V, in steps of 1 V.

transistor parameters are given in table 7.3. A total of 156 individual transistors were measured for each CNT via width.

Table 7.3: Transistor parameters for bottom-layer SG-TFT with different CNT via widths. The top-layer SG-TFT are added as reference (width N/A). Note: for the 3 μm PMOS yield reduced due to laser ablation, see also the discussion at the end of section 7.3.3.

	Via width (μm)	V_{th} (V)	On/Off ratio	Mobility (cm^2/Vs)	Yield (%)
PMOS	1	-2.02 $\pm$ 0.60	$2.6 \pm 2.7 \cdot 10^5$	20 $\pm$ 17	15
	2	-2.21 $\pm$ 0.50	$1.7 \pm 1.5 \cdot 10^6$	63 $\pm$ 32	81
	3	-2.01 $\pm$ 0.40	$1.2 \pm 1.3 \cdot 10^6$	75 $\pm$ 25	65
NMOS	1	0.42 $\pm$ 0.32	$1.1 \pm 1.5 \cdot 10^5$	59 $\pm$ 51	10
	2	0.66 $\pm$ 0.36	$4.6 \pm 4.6 \cdot 10^6$	148 $\pm$ 82	83
	3	0.71 $\pm$ 0.19	$3.9 \pm 3.0 \cdot 10^6$	149 $\pm$ 50	81
PMOS	N/A	-3.15 $\pm$ 0.59	$1.4 \pm 1.3 \cdot 10^6$	69 $\pm$ 29	92
NMOS	N/A	0.98 $\pm$ 0.45	$2.0 \pm 1.9 \cdot 10^6$	185 $\pm$ 67	84

While working transistors were obtained for each via width, the yield decreased considerably for the smallest size vias. This in contrast to the test via structures, indicating that growth on the small SG-TFT contacts is difficult for small openings. This could be caused by the location of the opening, which is right on top of the grain filter and is thus locally less flat. For the transistors with larger vias the yield is close to that off the transistors without CNT vias, except for the 3μm PMOSFET. Besides that, a steep decrease in mobility and on/off ratio can be observed for the smallest size vias. This is not caused by the transistor itself, but by the high resistance CNT vias limiting the amount of current which can be driven in the on-state. Transistors with 2 or 3 μm wide vias have almost the same mobilities, indicating that the intrinsic SG-TFT mobility of this process is reached. Again, via resistance should be reduced in order not to limit the performance of the SG-TFT with minimal size vias.

The mobility of the transistors is lower than that of 3D SG-TFT structures fabricated before [9]. This can be caused by a number of reasons. First of all, the way of contacting the transistors, with a Ti/TiN pad, is completely different. Ti and TiN have both a higher resistivity than Al, and potentially the contact resistance between the Si and Ti/TiN is higher in case of a C49-phase silicidation resulting in a higher resistivity $TiSi_2$ due to a too low temperature silicidation process. Beside that, process variability with the excimer laser has been known to cause low mobility. Both the top and bottom layer transistors demonstrate a low mobility, while they

were crystallized at different settings, but share Ti/TiN as contact material. The most likely cause is thus a high resistivity silicide or bad contact being formed between the Si and Ti/TiN pads. While Ti/TiN was also used in the single-layer process, the Ti layer was much thicker (5000 nm) compared to the 10 nm Ti used in the double-layer process. It could be that this layer is too thin to allow the formation of a good silicide.

7.3.3 3D Inverters

Using the design shown in fig. 7.4a inverters in which both active areas are directly on top of each other were fabricated, with the PMOS being twice the width of a NMOS, respectively 4 and 2 μm. Both PMOS up and down configurations were present on the wafer, each with vias widths of 1, 2 and 3 μm. Using a V_{dd} of 5 V the V_{in}-V_{out} characteristics were measured, and mid-point voltage (V_M), the voltage swing, and Voltage Noise Margin (VNM) were extracted. Here the VNM are defined as:

$$VNM_H = V_{dd} - V_{IH} \tag{7.1}$$

$$VNM_L = V_{IL} \tag{7.2}$$

where V_{IL} and V_{IH} are defined as the input voltages for the points where the slope of the V_{in}-V_{out} characteristics equals -1 for an input equal to a logic '0' and '1', respectively (see fig. 7.10). For good stability large VNM are desired. Fig. 7.10 displays the input-output characteristics of a PMOS bottom 3D inverter with minimal size CNT vias and full voltage swing.

The extracted inverter parameters can be found in table 7.4 for both the PMOS and NMOS-bottom inverters. Just as was the case for individual transistors, the smallest size vias have a large impact on the performance and yield of the inverters. From the perspective of V_M being close to half of V_{DD} and large VNM, a PMOS as bottom transistor offers the best performance. This can be explained by looking at the threshold voltages of the transistors in table 7.3, which are much larger for the PMOS than the NMOS. This is especially the case for the bottom NMOS, which makes the transistor switch faster, subsequently lowering V_M and VNM_L.

The differences in yield are most likely caused by the location of the structures in the excimer laser spot. The large via NMOS were located close to the centre of the spot, while the large via PMOS were closer to the edge. In the centre of the spot more ablation of the Si was observed, resulting in more defective transistors, especially when crystallizing the second layer of transistors. This can also be the cause of the large yield drop between the 2 and 3 μm PMOS observed in table 7.3.

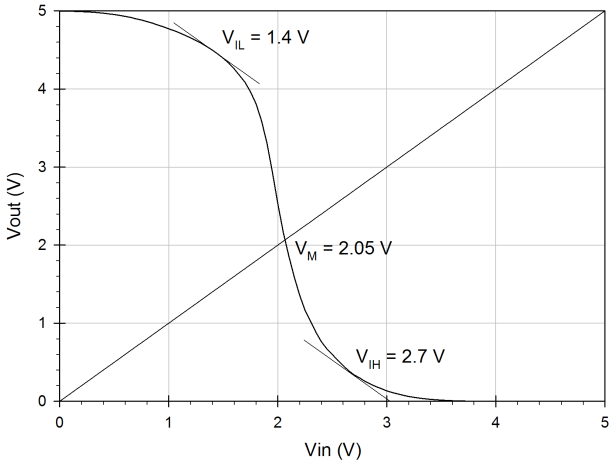

Figure 7.10: V_{in}-V_{out} characteristics of a PMOSFET bottom 3D inverter with 1 μm wide vias.

Table 7.4: Extracted average parameters for inverters with different bottom SG-TFT and different CNT via widths. For each size and type 156 inverters were measured.

Bottom TFT	Via width (μm)	V_M (V)	Swing (V)	VNM_L (V)	VNM_H (V)	Yield (%)
PMOS	1	1.41 ± 0.46	4.58 ± 0.61	0.56 ± 0.46	3.30 ± 0.56	20
	2	1.91 ± 0.33	4.95 ± 0.20	1.18 ± 0.45	2.71 ± 0.40	92
	3	1.98 ± 0.28	4.91 ± 0.32	1.29 ± 0.42	2.61 ± 0.35	86
NMOS	1	2.07 ± 0.88	4.58 ± 0.67	1.63 ± 0.98	2.25 ± 1.10	23
	2	1.44 ± 0.50	4.88 ± 0.33	0.89 ± 0.48	3.19 ± 0.63	77
	3	1.23 ± 0.45	4.89 ± 0.30	0.66 ± 0.40	3.47 ± 0.55	62

7.3.4 6T-SRAM cells

In the mask design 6-transistor SRAM cells which were previously fabricated in SG-TFT 3D technology have been included [9]. For more information regarding the simulations and design of these SRAM cells the reader is kindly referred to the MSc thesis of Negin Golshani [166]. The design was adapted to the combined CNT and SG-TFT process by including a Ti/TiN metallization. Fig. 7.11 shows the mask design of a 6T SRAM cell with 2.6 μm access transistors, 24 μm wide NMOS and 16 μm wide PMOS for both a single-layer and double-layer process. A distinct area advantage can be observed for the 3D design, which has all the PMOS in the top layer.

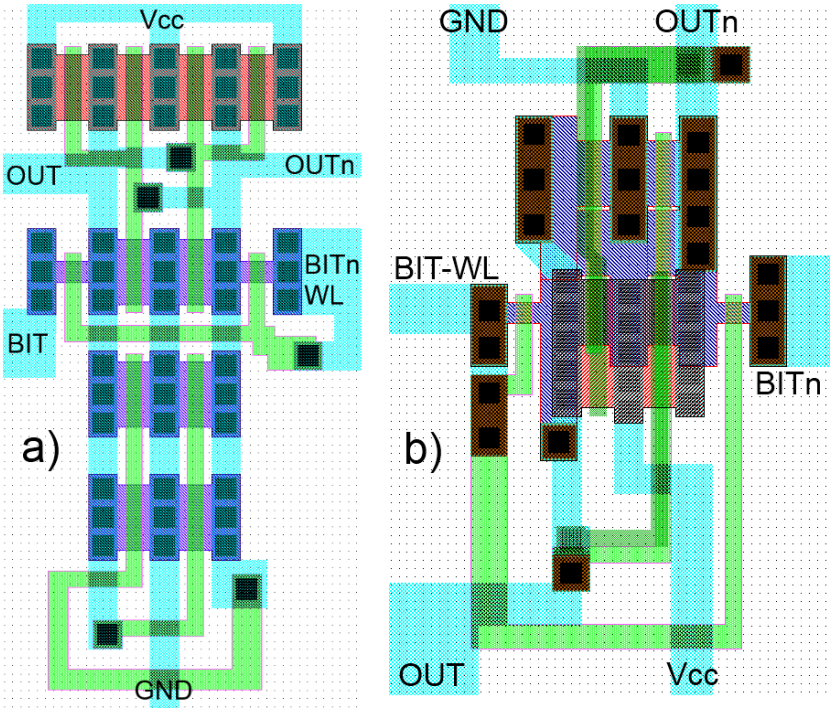

Figure 7.11: Mask lay-out of SRAM cells: a) single-layer; b) double-layer. Red: p-type Si, blue: n-type Si, green: gates, brown: Ti/TiN stack, black: CNT vias, grey: other contact openings, light blue: Al (1% Si), the grid spacing is 1 μm.

At a high V_{dd} of 10 V a few large-sized SRAM cells were found working. The working devices have 24 μm wide NMOS pull-down transistors in the bottom layer, 16 μm wide PMOS pull-up transistors and either 2.6 or 4 μm wide NMOS access transistors. Fig. 7.12 displays the butterfly diagram of the best working 3D SG-TFT SRAM. The device has only low read-noise margins, judging from the small openings in the butterfly read curves. This can be attributed to the design which were tailored for a traditional SG-TFT process, which have much lower resistivity vias than the CNT vias used here. Moreover, the mobility of the SG-TFT measured here is lower than that assumed in the design (300 and 100 cm^2/Vs for NMOS and PMOS, respectively). Due to this, the pull-up, pull-down and access transistors are brought out of their designed balance, resulting in non-working SRAM cells.

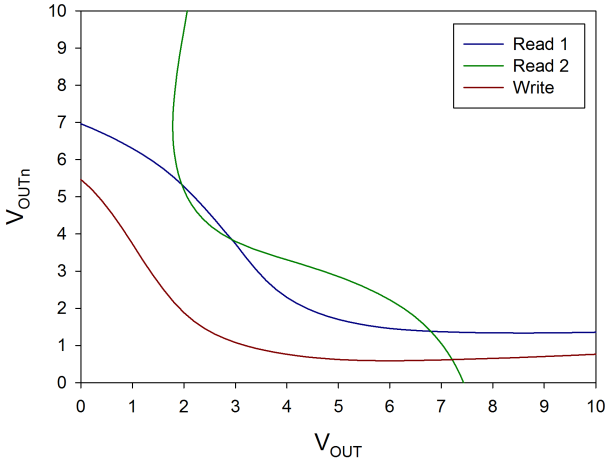

Figure 7.12: V_{OUT}-V_{OUTn} characteristics of a 3D SG-TFT 6T-SRAM cell during read and write operations.

7.4 Conclusion

Integrating CNT vias into the 3D SG-TFT process proved to be non-trivial, due to the SG-TFT process LPCVD a-Si deposition and excimer laser steps influencing the CNT growth. In the end a combination of Co as catalyst, and Ti/TiN/Ti pads on poly-Si gate and islands resulted in working transistors. Measurements on the test vias fabricated alongside the active devices demonstrated that the resistivity of the CNT vias is higher than that of the test vias measured in chap. 5 for the single-layer process. For the double-layer process the resistivity was comparable, as Co is less affected by the change in TiN properties.

The higher resistance vias influence the performance of the circuits made. Measurements on individual transistors demonstrated that for 1 μm wide vias the resistance limits the performance, while this is not the case any more when the via width is increased to 2 μm. It was found that for the double-layer process the mobility was lower than expected, which is attributed to a bad silicidation of the Ti/TiN contacts, Working 3D CMOS inverters were demonstrated, with a reasonable yield of 80 % for the non-minimal sized vias. It was also shown that is possible to fabricate more complex 6T-SRAM cells, although the high CNT via resistance and lower transistor mobilities had a large impact on their stability.

8

Conclusions and recommendations

8.1 Conclusions

In this thesis carbon nanotubes have been investigated for the application as vertical interconnects in 3D integrated circuits. CNT can potentially offer high current carrying capability, good electrical conduction, high thermal conductivity and high aspect ratios. All of these are of interest for 3D IC based on both through silicon vias as well monolithic 3D IC. For TSV it is especially important that long bundles can be fabricated. For monolithic 3D IC the direct integration with transistors puts more strict demands on the maximum growth temperature and the materials used. The main conclusions of this thesis are as follows:

- Using electrical models it became clear that a high packing density in the order of 10^{13} tubes and high crystallinity would be required to obtain electrical resistivities comparable to that of Al and Cu. Also, for the thermal performance CNT of high quality will be required. The only method fit for depositing CNT directly at the desired location, and at sufficiently low temperatures is chemical vapour deposition.
- Raman spectroscopy is a powerful technique for investigating CNT crystallinity (quality). Several Raman active bands were found to be sensitive to the number of defects, namely the D, D' and G' bands. Their ratios and full-widths at half maximum can be used to both qualitatively as quantitatively investigate the quality of the samples when process conditions like temperature are changed. For high quality tubes the I_D/I_G ratio can be sufficient to accurately inspect qual-

ity, for lower quality samples also the other bands and their widths can be taken into account to prevent ambiguities. When assessing the quality using Raman spectroscopy care should be taken to use the same laser wavelength, as the magnitude of the defect related peaks changes with laser wavelength. Finally, the I_D/I_G ratio can be translated into the in-plane crystallite size using an empirical formula from literature.

- It was found that both TiN as ZrN are attractive electrical conductive support layers, allowing respectively low temperature growth fit for monolithic integration, and high growth rates for TSV. It was concluded that these layers work well due to their low surface energy. Both Fe, Co and Co-Al were used as catalyst on TiN, of which Co and Co-Al allowed growth at record-low temperatures of 350 °C, while Fe had a minimum growth temperature of 450 °C. This difference in minimum growth temperatures was caused by a difference in activation energy of the catalytic process. Quality of the CNT for both catalyst decreases with temperature. The Fe catalyst was found to give the highest tube density and quality of the three catalysts.

  Growth on ZrN was found to highly depend on catalyst thickness and the geometric pattern of the catalyst (loading effects). Using a Taguchi design of experiments the different parameters for the CNT growth were optimized for maximum length and density. Using the maximum length conditions it was verified that a height of 900 μm could be obtained, while the maximum density recipe led to a doubling of the density ($1.2 \cdot 10^{11}$ tubes/cm^2). From TEM and Raman it became clear that the sample consists of SWCNT and DWCNT of high quality. The growth of ZrN is especially of interest of TSV in Si interposer technology.

  Lift-off was found to be an attractive method for pattering the catalyst without damaging it its support layer. Still, the support layer can be damaged by plasmas, and should thus be protected by a sacrificial layer. CNT allow for both top-down and bottom-up integration, the latter not requiring any etching of holes. It was found that PECVD plasma deposition does not damage the CNT and can thus be used for bottom-up integration.

- Electrical measurements were performed on four-point probe via structures manufactured for monolithic integration using both top-down and bottom-up integration. While the top-down structures display linear I-V characteristics for all growth temperatures (350-550 °C), this was not the case for the bottom-up structures due to a non-ohmic

top contact. The uniformity of the electrical resistance does not depend on catalyst and growth temperature between 350-500 °C. However, a decrease in uniformity with increasing length was observed. This is caused by non-uniformity caused by the substrate heater. It was found that the electrical contact resistance of the CNT vias was low, which is attributed to top contact embedding. By fitting the data using the models given in chapter 2 it was found that most shells of the multi-walled tubes are contributing to conduction. The resistivity of the fabricated tubes increases with decreasing growth temperature from 20 to 160 mΩ-cm. Although comparable to values found in literature, this is much higher than that of Cu (1.69 $\mu\Omega$-cm). This is due to the low density and quality of the CNT bundles.

The thermal coefficient of resistance of the CNT vias was found to be negative, which is attractive for interconnect applications. Size dependent effects were observed, which can partly be explained by including a positive TCR for the contact resistance. The electrical reliability of the CNT vias was investigated, the best performing vias could withstand a current density up to 9 MA/cm^2, which is higher than that of Cu. Two failure mechanisms appear to exist: Joule heating and contact failure.

- Using a novel vertical 3ω-method, which was verified using simulations and from the measurement data, it was determined that the thermal boundary resistance dominates the thermal performance of the CNT vias. This is likely caused by bad transmission at the metal-CNT interface and small bottom contact area. The thermal conductivity of the CNT was determined to be 1.4 W/mK, much lower than other values in literature as high as 3500 W/mK. This can be attributed to the low quality of the CNT material.

- Integration of low-temperature CNT as vias into a monolithic 3D SG-TFT process was achieved. The LPCVD Si deposition and excimer laser process steps of the SG-TFT process were found to affect the TiN layer, resulting in random growth with Fe. By changing to a Co catalyst vertically aligned vias could be fabricated at 500 °C. The resistivity of the CNT test vias fabricated alongside the active devices was found to be higher than that of the test vias measured in chapter 5. While working individual transistors, CMOS inverters and 6T-SRAM cells could be fabricated it was found that the high CNT vias resistance affected the transistor performance, and in case of minimum sized 1 μm^2 vias also the yield.

8.2 Recommendations for future work

The results in this thesis provided insight in the electrical and thermal properties of CNT vias, and demonstrated the possibility to use CNT as vias in actual monolithic 3D integrated circuits. While several breakthroughs have been achieved, more research will be required in order to allow CNT to be used as future materials for vias:

- As became clear from the conclusion the CNT grown at low temperatures have an electrical and thermal performance which are generally three orders of magnitude less than the maximum values published in literature. This can be mainly attributed to the low quality and density of the CNT bundles. Using recipe and process optimization it is to be expected that both the density and quality can be increased. Such an increase will be necessary for CNT to be able to compete with current via materials.
- Within the scope of this thesis no actual electrical measurements on CNT TSV could be performed. However, the growth on ZrN shows huge potential for the fabrication of CNT TSV, especially for Si interposer technology. It is strongly recommended to continue the work on this support layer.
- Although many new electrical measurements were presented, still several things could not be measured within the scope of this thesis due to time constraints. A more detailed electrical characterization on the low temperature growth using Co is recommended, especially on the length dependent resistance and electrical reliability. For the TCR data more measurements would be useful in order to investigate the observed area dependency of the TCR.
- While low temperature CNT currently not have the high electrical conductivity, this does not mean they cannot be used for other electrical applications. An area of interest for CNT is the use as supercapacitors, on which I collaborated with G. Fiorentino [167]. For this application the surface area of the CNT can be advantageous, and the electrical performance of the CNT is of less concern.
- The higher temperature growth process on TiN, ZrN and Al_2O_3 can be very interesting in the field of microelectromechanical systems, which often have a higher thermal budget. Collaborations already resulted in the use of the CNT as light absorbing layer [168], and for thermal management [169]. Another interesting topic can be the use of CNT for HAR surface micro-machining.

A

Flowcharts

A.1 CNT test via process

Main steps for top-down fabrication of low-temperature CNT test vias using Fe or Co on TiN.

- Si substrate with alignment markers
- (reactive) Sputtering: Ti/TiN/Ti stack (500/50/100 nm)
- (reactive) Sputtering: Ti/TiN (10/50 nm) backside deposition (against catalyst diffusion into backside)
- PECVD: TEOS deposition of various thickness
- Lithography: Via mask
- Dry etching: oxide to Ti layer
- Wet etching: sacrificial Ti in 0.55 % HF
- Evaporation: 5 nm Fe or Co catalyst
- Lift-off: NMP for Fe, THF for Co
- CNT growth: LPCVD recipe with growth time for height equal to oxide thickness
- Sputtering: 100 nm Ti, 3 μm Al(1% Si)
- Lithography: full-wafer mask

- Wet etching: backside Fe or Co clean in, respectively, 10 % HNO_3 or 0.55 % HF
- Lithography: Metal mask
- Dry etching: 3 μm Al(1% Si), 100 nm Ti

A.2 Monolithic 3D SG-TFT process with CNT vias

Main steps for fabrication of double-layer 3D SG-TFT with low-temperature CNT vias.

- Si substrate
- Oxidation: 520 nm
- Lithography: zero layer
- Wet etching: 520 nm SiO_2 in BHF (1:7)
- Oxidation: cumulative thickness of 750 nm on non-etched areas
- Lithography: grain filter 1 mask
- Dry etching: 750 nm of SiO_2
- PECVD: 830 nm of TEOS SiO_2
- LPCVD: 250 nm a-Si at 545 °C
- Implantation: B^+ channel implantation $2.5 \cdot 10^{11}$ cm^{-2}
- Excimer laser: crystallization at 450 °C
- Lithography: island 1 mask
- Dry etching: 250 nm of a-Si (front and backside)
- Wet etching: native oxide dip etch in 0.55% HF
- PECVD: 50 nm TEOS gate oxide
- LPCVD: 250 nm a-Si at 545 °C
- Lithography: gate 1 mask
- Dry etching: 250 nm of a-Si
- Dry etching: 50 nm gate oxide
- Lithography: NMOS 1 mask

- Implantation: P^+ implantation $5 \cdot 10^{15}$ cm^{-2}
- Lithography: PMOS 1 mask
- Implantation: B^+ implantation $5 \cdot 10^{15}$ cm^{-2}
- Excimer laser: dopant activation at room temperature
- PECVD: 600 nm of TEOS SiO_2
- Lithography: contact openings 1 mask
- Dry ethcing: 600 nm of SiO_2
- Wet etching: native oxide dip etch in 0.55% HF
- Sputtering: 10 nm Ti, 50 nm TiN, 100 nm Ti
- Lithography: metal 1 mask
- Dry etching: Ti/TiN/Ti stack
- PECVD: 1.2 μm interlayer TEOS SiO_2
- Lithography: grain filter 2 mask
- Dry etching: 750 nm of SiO_2
- PECVD: 830 nm of TEOS SiO_2
- LPCVD: 250 nm a-Si at 545 °C
- Implantation: B^+ channel implantation $2.5 \cdot 10^{11}$ cm^{-2}
- Excimer laser: crystallization at 450 °C
- Lithography: island 2 mask
- Dry etching: 250 nm of a-Si (front and backside)
- Wet etching: native oxide dip etch in 0.55% HF
- PECVD: 50 nm TEOS gate oxide
- LPCVD: 250 nm a-Si at 545 °C
- Lithography: gate 2 mask
- Dry etching: 250 nm of a-Si
- Dry etching: 50 nm gate oxide
- Lithography: NMOS 2 mask
- Implantation: P^+ implantation $5 \cdot 10^{15}$ cm^{-2}

- Lithography: PMOS 2 mask
- Implantation: B^+ implantation $5 \cdot 10^{15}$ cm^{-2}
- Sputtering: 100 nm of pure Al (for laser annealing protection)
- Lithography: metal 3 (for laser annealing protection)
- Excimer laser: dopant activation at room temperature
- Wet etching: 100 nm Al in PES 77-19-04
- PECVD: 600 nm of TEOS SiO_2
- Lithography: contact openings 2 and 3 masks
- Dry ethcing: 600 nm of SiO_2
- Wet etching: native oxide dip etch in 0.55% HF
- Sputtering: 10 nm Ti, 50 nm TiN
- Lithography: source/drain barrier 2 mask
- Dry etching: Ti/TiN stack
- Lithography: Via mask
- Dry etching: 2.5 μm of SiO_2 back to first transistor layer
- Evaporation: 5 nm Co catalyst
- Lift-off: THF
- CNT growth: LPCVD recipe with growth time for height equal to oxide thickness
- Sputtering: 100 nm Ti, 2 μm Al(1% Si)
- Lithography: full-wafer mask
- Wet etching: backside Co clean in 0.55 % HF
- Lithography: metal 2 mask
- Dry etching: 2 μm Al(1% Si), 100 nm Ti

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Summary

Carbon nanotubes as vertical interconnects in 3D integrated circuits

While downscaling generally improves transistor performance, downscaling the interconnects result in an increase of delay times, power dissipation and pushes the current interconnect materials like Cu to their physical limits in terms of current density and aspect ratio. Three dimensional (3D) integration has been proposed as a solution for interconnect delays and power dissipation, by providing an additional routing dimension and thus decreasing the interconnect length. Die stacking using through silicon vias (TSV) just became commercially available, and in the future monolithic integration can improve the performance of 3D integrated circuits (IC) by further reducing interconnect lengths. To create the multiple layers of transistors in monolithic 3D IC single-grain thin-film transistor (SG-TFT) technology can be used, which offers high mobility and a low fabrication temperature. For both die stacking with TSV and monolithic integration high aspect ratio reliable vertical interconnects (vias) have to be fabricated, and thermal management can be an issue. In this thesis it is proposed that carbon nanotubes (CNT) can be an attractive material for fabrication of these vias, due to their excellent thermal and electrical conductivity, electrical reliability, and high aspect ratios.

With an equivalent circuit it is shown that the most important components that will influence the electrical performance of a CNT bundle are its quantum resistance, contact resistance, and for the delay the electrostatic capacitance (chapter 2). The electrical resistance of a bundle decreases with increasing bundle density, quality and decreasing CNT diameter due to an

increase in conductive channels. It is concluded that a density close to the theoretical close packing limit of circles and ballistic conduction over the entire via length will be required in order to outperform Cu in terms of electrical resistivity. In the same chapter the thermal performance is discussed and it is concluded that a low thermal boundary resistance (TBR) and high CNT quality are required. Finally, chemical vapour deposition is identified as the preferred growth method for the fabrication of CNT vias.

In order to investigate the crystallinity (or quality) of the CNT Raman spectroscopy can be employed, which has the advantages to be relative fast (compared to electron microscopy), non-destructive and quantitative. From CNT and carbon nanofibres (CNF) fabricated at different temperatures the impact of growth temperature on the Raman spectra was investigated in chapter 3. Using only the commonly used I_D/I_G ratio of the Raman spectra without any additional knowledge of the sample or the Raman spectra can result in the wrong conclusion, as the I_D/I_G ratio peaks when plotted versus sample quality. For high quality samples using the I_D/I_G ratio, with additional information of the $I_{D'}/I_G$ and $I_{G'}/I_G$ and the widths of the D, G, D' and G' bands can be sufficient. For CNF or CNT samples with low quality using second-order bands is difficult to their weak amplitudes, while the use of the I_D/I_G ratio can show conflicting behaviour. For this kind of samples taking into account the widths of the D and G band is recommended. Care should be taken to employ the same laser wavelength when comparing samples. Finally, it is possible to translate the Raman data into the in-plane crystalline length with an empirical formula from literature.

For CNT growth a catalyst and a support layer which acts as diffusion barrier and should aid in the formation of catalyst nanoparticles are required. For electrical applications this layer should be electrically conductive. In chapter 4 the results of growth on conductive TiN and ZrN layers are discussed. These layer appear to work well due to their low surface energy aiding in the de-wetting of the Fe or Co catalyst. Using Fe as catalyst, it is possible to grow at temperatures as low as 450 °C on TiN, while Co and Co-Al could provide growth at a record low temperature of 350 °C. This is attributed to the lower activation energy of the Co-based catalysts. In all cases the quality of the CNT increases with growth temperature. Due to the low growth temperature the combination of Fe or Co on TiN is interesting for monolithic integration. It was found that ZrN with Fe as catalyst has the potential to grow hundreds of micrometer long single-walled CNT. In contrast to the often used Al_2O_3 for the growth of long CNT, this material is electrically conductive which makes it an excellent material for TSV. To integrate CNT as vias for monolithic 3D IC both top-down and bottom-up integration can be utilized, the latter having the advantage that no holes

in the dielectric have to be etched. It was also found that the TiN layer is sensitive to plasma damage, which can be prevented with a protective sacrificial layer.

Electrical measurements performed on CNT test vias with different widths, lengths, and fabricated at different temperatures using different catalyst are described in chapter 5. The I-V characteristics are linear, indicating ohmic contact, except for bottom-up fabricated vias. It was found that heater non-uniformity causes spread in the resistance over the wafer. The yield for low temperature vias was around 90%, while longer vias showed a decrease in yield. By measuring vias with different lengths the contact resistance was determined. This was found to be low compared to the CNT bundle resistance, which is attributed to contact embedding. Comparing the electrical measurements with Raman data it was determined that the multi-walled CNT exhibit conduction along multiple walls. Compared to literature the lowest resistivities obtained here (20 mΩ-cm) are among the average values reported, which is caused by the low quality and density of the CNT bundles. The thermal coefficient of resistance of the CNT vias was found to be negative (-400 ppm/K for Fe and -830 ppm/K for Co-grown tubes). A bundle-size dependent effect was observed, which can partly be explained by taking into account a temperature dependent contact resistance. The chapter concludes with electrical reliability measurements. The highest allowed current density was found to be 9 MA/cm^2, and failure appears to be either at the contacts or due to Joule heating in the centre.

Using a novel vertical 3ω-method the thermal conductivity of CNT vias was measured in chapter 6. With measurements and Comsol simulations the validity of the method was demonstrated. From vias with different bundle lengths and widths the thermal resistance was determined. When plotting this resistance versus length it became clear that the TBR dominates the thermal resistance, except for the smallest measured via width (2 μm). It is estimated that the TBR is $10^9 - 10^{10}$ K/W per tube. This is likely caused by the difference between the heat carriers in CNT (phonons) and the metals contacts (electrons) and the small contact area. The thermal conductivity of the CNT bundle was determined to be 1.4 W/mK, which is 3 orders of magnitude lower than the highest values reported. This is caused by the low quality of the CNT due to their low growth temperature.

In chapter 7 the integration of CNT vias in 3D SG-TFT technology is demonstrated. It was found that the SG-TFT fabrication process affects the TiN layer, requiring a switch from Fe to Co as catalyst in order to allow the growth of CNT for vias with an aspect ratio as high as 2.5. Test vias fabricated alongside the 3D SG-TFT demonstrate that the via resistivity does not increase noticeably when these technologies are combined. The

resistance of the CNT vias and TiN contact pads was found to limit the performance in terms of mobility of SG-TFT in both a single- and double-layer process, especially for minimum sized vias (1 μm^2). It was demonstrated that it is possible to fabricate 3D inverters and even more complex 6T static random access memory cells with this technology.

Finally, chapter 8 provides the conclusions. The main conclusion is that CNT are in theory an excellent via material, but both the electrical as thermal performance are limited by the low quality and density of the CNT bundles. While it was shown, for the first time, that CNT can be directly integrated with active devices, the transistor performance will be severely limited if the resistivity of the CNT bundles cannot be decreased.

Samenvatting

Koolstof nanobuisjes als verticale interconnecties in 3D geïntegreerde schakelingen

Terwijl het verkleinen van de dimensies van transistoren over het algemeen de prestaties verbetert, resulteert het verkleinen vn de dimensies van de interconnecties in een toename van vertraging, vermogensdissipatie en duwt het de huidige verbindingsmaterialen zoals Cu naar hun fysieke grenzen in termen van de stroomdichtheid en aspect ratio. Drie dimensionale (3D) integratie is voorgesteld als een oplossing voor de interconnectie vertraging en vermogensdissipatie, door het toevoegen van een extra dimensie voor routering waardoor de totale interconnectie lengte afneemt. Chips gestapeld door middel van *through silicon vias* (TSV) zijn onlangs commercieel verkrijgbaar geworden en in de toekomst kan monolithische integratie de prestaties van de 3D geïntegreerde schakelingen (IC) verder verbeteren door het verder reduceren van de interconnectie lengtes. Voor het creëren van meerdere lagen van transistoren in monolithische 3D IC kan enkele-korrel dunne-laag transistor (SG-TFT) technologie worden gebruikt, welk een hoge mobiliteit en lage fabricage temperatuur biedt. Zowel voor chip stapelen met TSV als monolithische integratie moeten hoge aspect ratio betrouwbare verticale interconnecties (vias) worden gefabriceerd en is thermische management een probleem. In dit proefschrift wordt voorgesteld dat koolstof nanobuisjes (CNT) een aantrekkelijk materiaal zijn voor de fabricage van deze vias, dankzij hun uitstekende thermische en elektrische geleiding, elektrische betrouwbaarheid en hoge aspect ratio's.

Door middel van een equivalent circuit is aangetoond dat de meest belangrijke componenten die de elektrische prestaties van een CNT bundel be-

ïnvloeden de kwantum weerstand, contact weerstand, en voor de vertraging de elektrostatische capaciteit zijn (hoofdstuk 2). De elektrische weerstand van een bundel vermindert met een toenemende bundel dichtheid, kwaliteit en afnemende CNT diameter door een toename van het aantal geleidende kanalen. Geconcludeerd wordt dat een dichtheid nabij de theoretische dichte stapel limiet van cirkels en ballistische geleiding over de gehele via lengte nodig zijn om Cu in termen van elektrische resistiviteit te overtreffen. In hetzelfde hoofdstuk worden de thermische prestaties behandeld en wordt er geconcludeerd dat een lage thermische grensweerstand (TBR) en hoge CNT kwaliteit nodig zijn. Chemische damp depositie wordt tenslotte geïdentificeerd als voorkeursmethode voor de fabricage van CNT vias.

Om de kristalliniteit (kwaliteit) van CNT te onderzoeken kan gebruik worden gemaakt van Raman spectroscopie, dat als voordeel heeft dat het relatief snel is (ten opzichte van elektronen microscopie), niet-destructief en kwantitatief. Van CNT en koolstof nanovezels (CNF) gefabriceerd bij verschillende temperaturen is de invloed van de groei temperatuur op het Raman spectrum onderzocht in hoofdstuk 3. Het gebruik van alleen de I_D/I_G ratio van het Raman spectrum zonder enige extra informatie van het monster of het Raman spectra kan resulteren in verkeerde conclusies, aangezien de I_D/I_G ratio piekt wanneer uitgezet tegen de kwaliteit van het monster. Voor hoge kwaliteit monsters is het gebruik van de I_D/I_G ratio met extra informatie van de I_{D+G}/I_G en $I_{G'}/I_G$ ratio's en de breedte van de D, G, D' en G' banden voldoende. Voor CNF, of CNT monsters van lage kwaliteit, is het gebruik van tweede-orde banden moeilijk door hun zwakke amplitude, terwijl het gebruik van de I_D/I_G ratio tegenstrijdig gedrag kan tonen. Voor dit soort monsters wordt aangeraden om rekening te houden met de breedte van de D en G banden. Bij het vergelijken van monsters moet er voor worden gezorgd dat dezelfde laser golflengte gebruikt wordt. Het is tenslotte mogelijk om de Raman data te vertalen in de in-plane kristalliniteitslengte door middel van een empirische formule uit de literatuur.

Voor het groeien van CNT zijn een katalysator en een ondersteuningslaag, welk fungeert als een diffusie barrière en helpt in de formatie van nanodeeltjes, nodig. Voor elektrische toepassingen moet deze laag elektrisch geleidend zijn. In hoofdstuk 4 worden de resultaten van groei op geleidende TiN en ZrN lagen behandeld. Deze lagen lijken goed te werken door hun lage oppervlakte energie welke helpt in het opbreken van de Fe of Co katalysator. Gebruik makend van Fe als katalysator is het mogelijk om te groeien op temperaturen zo laag als 450 °C op TiN, terwijl Co en Co-Al groei bieden bij een record-lage temperatuur van 350 °C. Dit wordt toegeschreven aan de lagere activatie energie van de op Co gebaseerde katalysatoren. In alle gevallen neemt de kwaliteit toe met groei temperatuur.

Dankzij de lage groei temperatuur is de combinatie van Fe of Co op TiN interessant voor monolithische integratie. Het blijkt dat ZrN met Fe as katalysator de potentie heeft om honderden micrometers lange enkelwandige CNT te groeien. In tegenstelling tot het vaak voor de groei van lange CNT gebruikte Al_2O_3 is dit materiaal elektrisch geleidend, wat het een uitstekende kandidaat maakt voor TSV. Voor het integreren van CNT als vias voor monolithische 3D IC kunnen zowel *top-down* als *bottom-up* integratie gebruikt worden, waarvan de laatste het voordeel heeft dat er geen gaatjes in het diëlektricum hoeven te worden geëtst. Het blijkt ook dat TiN gevoelig is voor plasma schade, welke kan worden voorkomen door het gebruik van een beschermende opofferingslaag.

Elektrische metingen uitgevoerd op CNT test vias met verschillende breedtes, lengtes, en gefabriceerd op verschillende temperaturen door middel van verschillende katalysatoren, worden beschreven in hoofdstuk 5. De I-V karakteristieken zijn lineair, wat duidt op een ohms contact, met uitzondering van die van *bottom-up* gefabriceerde vias. Het bleek dat verwarmer non-uniformiteit zorgt voor een variatie in weerstand over de plak. De opbrengst voor lage-temperatuur vias was rond de 90 %, terwijl langere vias een afname in opbrengst toonden. Door het meten van vias met verschillende lengtes kon de contactweerstand worden bepaald. Deze bleek laag te zijn ten opzichte van de CNT bundel weerstand, wat wordt toegeschreven aan contact inbedding. Door middel van het vergelijken van de elektrische metingen met Raman data werd bepaald dat de meerdere-wandige CNT geleiding over meerdere wanden tonen. Vergeleken met literatuur behoren de laagst behaalde resistiviteiten (20 mΩ-cm) tot de gemiddelde gerapporteerde waardes, wat wordt veroorzaakt door de lage kwaliteit en dichtheid van de CNT bundels. De temperatuurcoëfficiÃńnt van de weerstand van de CNT vias bleek negatief te zijn (-400 ppm/K voor Fe, en -830 ppm/K voor met Co gegroeide buisjes). Een bundel-grootte afhankelijk effect werd waargenomen, wat deels kan worden verklaard door het in acht nemen van een temperatuur afhankelijke contact weerstand. Het hoofdstuk sluit af met elektrische betrouwbaarheid metingen. De maximale stroomdichtheid bleek 9 MA/cm^2 te zijn, en falen lijkt op te treden bij de contacten, of in het midden door Joule verwarming.

Door middel van een nieuwe verticale 3ω-methode is de thermische geleiding van de CNT vias gemeten in hoofdstuk 6. Door middel van metingen en Comsol simulaties is de deugdelijkheid van de methode gedemonstreerd. Van vias met verschillende bundel lengtes en breedtes is de thermische weerstand bepaald. Wanneer deze weerstand wordt uitgezet tegen de lengte werd het duidelijk dat de TBR de thermische weerstand domineert, behalve bij de kleinste via breedte (2 μm). De TBR wordt geschat op $10^9 - 10^{10}$ K/W

per buisje. Dit wordt waarschijnlijk veroorzaakt door het verschil tussen de warmtedragers in CNT (phononen) en de metaalcontacten (elektronen), en het kleine contact oppervlak. De thermische geleiding van de CNT bundel werd vastgesteld op 1.4 W/mK, wat 3 ordes in grootte lager is dan de hoogste gerapporteerde waardes. Dit wordt veroorzaakt door de lage kwaliteit van de CNT door de lage groei temperatuur.

In hoofdstuk 7 wordt de integratie van CNT vias in 3D SG-TFT technologie gedemonstreerd. Het bleek dat het SG-TFT fabricage proces de kwaliteit van de TiN laag beïnvloedde, waardoor een wisseling van katalysator van Fe naar Co nodig was voor de groei van CNT vias met een aspect ratio zo hoog als 2.5. Test vias gefabriceerd naast de 3D SG-TFT demonstreren dat de via weerstand niet opmerkelijk toeneemt als de twee technieken worden gecombineerd. De weerstand van de CNT vias en TiN contact gebieden blijken de prestaties in termen van de mobiliteit van de SG-TFT in zowel een enkel-laags als dubbel-laags proces te beïnvloeden, vooral voor minimum formaat vias (1 μm^2). Het is aangetoond dat het mogelijk is om 3D *inverter* en zelfs meer complexe *6T static access memory* cellen te fabriceren met deze techniek.

Tenslotte geeft hoofdstuk 8 de conclusies. De hoofdconclusie is dat CNT in theorie een uitstekend via materiaal zijn, maar dat zowel de elektrische als thermische prestaties worden gelimiteerd door de lage kwaliteit en dichtheid van de CNT bundels. Terwijl voor de eerste keer werd gedemonstreerd dat CNT direct geïntegreerd kunnen worden met actieve apparaten, zullen de transistor prestaties ernstig worden beperkt als de resistiviteit van de CNT bundels niet kan worden verlaagd.

Acronyms

AFM	Atomic Force Microscopy.
BZ	Brillouin zone.
CMOS	Complementary Metal Oxide Semiconductor.
CMP	Chemical Mechanical Polishing.
CNF	Carbon Nanofibres.
CNT	Carbon Nanotubes.
CVD	Chemical Vapour Deposition.
DWCNT	Double-Walled Carbon Nanotubes.
FIB	Focused Ion Beam.
FWHM	Full Width at Half Maximum.
HAR	High Aspect Ratio.
HOPG	Highly-Oriented Pyrolytic Graphite.
IC	Integrated Circuit.
ITRS	International Technology Roadmap for Semiconductors.

LPCVD	Low-Pressure Chemical Vapour Deposition.
MFP	Mean Free Path.
MWCNT	Multi-Walled Carbon Nanotubes.
NMOS	n-Type Metal Oxide Semiconductor Field-Effect Transistor.
NMP	N-Methyl-2-Pyrrolidone.
PECVD	Plasma-Enhanced Chemical Vapour Deposition.
PMOS	p-Type Metal Oxide Semiconductor Field-Effect Transistor.
RBM	Radial Breathing Modes.
SEM	Scanning Electron Microscope.
SG-TFT	Single-Grain Thin-Film Transistors.
SRAM	Static Random Access Memory.
SS	Subtreshold Slope.
SWCNT	Single-Walled Carbon Nanotubes.
TBR	Thermal Boundary Resistance.
TCR	Temperature Coefficient of Resistance.
TEM	Transmission Electron Microscope.
TEOS	Tetraethyl Orthosilicate.
THF	Tetrahydrofuran.
TSV	Through Silicon Vias.
VLSI	Very-Large-Scale Integration.
VNM	Voltage Noise Margin.

List of publications

Journal papers

1. **S. Vollebregt**, S. Banerjee, A.N. Chiaramonti, C.I.M. Beenakker, and R. Ishihara "Dominant thermal boundary resistance in multi-walled carbon nanotube bundles fabricated at low temperature", *Applied Physics Letters*, submitted
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About the author

Sten Vollebregt was born in Delft, The Netherlands, in 1984. He received his bachelor degree, cum laude, in electrical engineering from the Delft University of Technology in 2006. After this he spend one year as full-time daily board member of the Delftsche Studenten Bond student society (300 members), responsible for the mensa and the exploitation of the rooms in the weekend for internal and external events.

In September 2008 he joined the Laboratory of Electronic Components, Technology and Materials (ECTM) and the Delft Institute of Microsystems and Nanoelectronics (DIMES), both part of the Delft University of Technology, Faculty of Electrical Engineering, Mathemathics, and Computer Science (EEMCS) for his M.Sc. thesis on carbon nanotubes. During his M.Sc. thesis he visited AIXTRON, Cambridge, UK and NanoLab, Newton, MA, USA to perform depositions. He graduated, cum laude, in September 2009 and started pursuing his Ph.D. on the application of carbon nanotubes as vertical interconnects in 3D integrated circuits in the same group. During his Ph.D. he was treasurer of the Micro-Electronic Systems & Technology Association, for M.Sc. and Ph.D. students in Microelectronics and Computer Engineering, for several years. He created and assisted a new lab course for M.Sc. students on the application of carbon nanotubes for vias for two years, as part of a course by Dr. R. Ishihara and Dr. J.F. Creemer. His work has been published in several journals (e.g. Carbon, Applied Physics Letters, IEEE Transaction on Electron Devices), two book chapters, and presented at numerous conferences. In 2014 he won the best oral presentation award of the Tenth International Thin-film Transistor conference.

He currently holds a 3 year Post-Doc position for an STW HTSM project on the wafer scale fabrication of graphene for sensor applications under Prof. P.M. Sarro in ECTM and DIMES. His interest include the integration of carbon based materials in semiconductor processing, carbon nanotubes and graphene, process development, and Raman spectroscopy. His personal interests include reading, photography, and playing electric guitar.