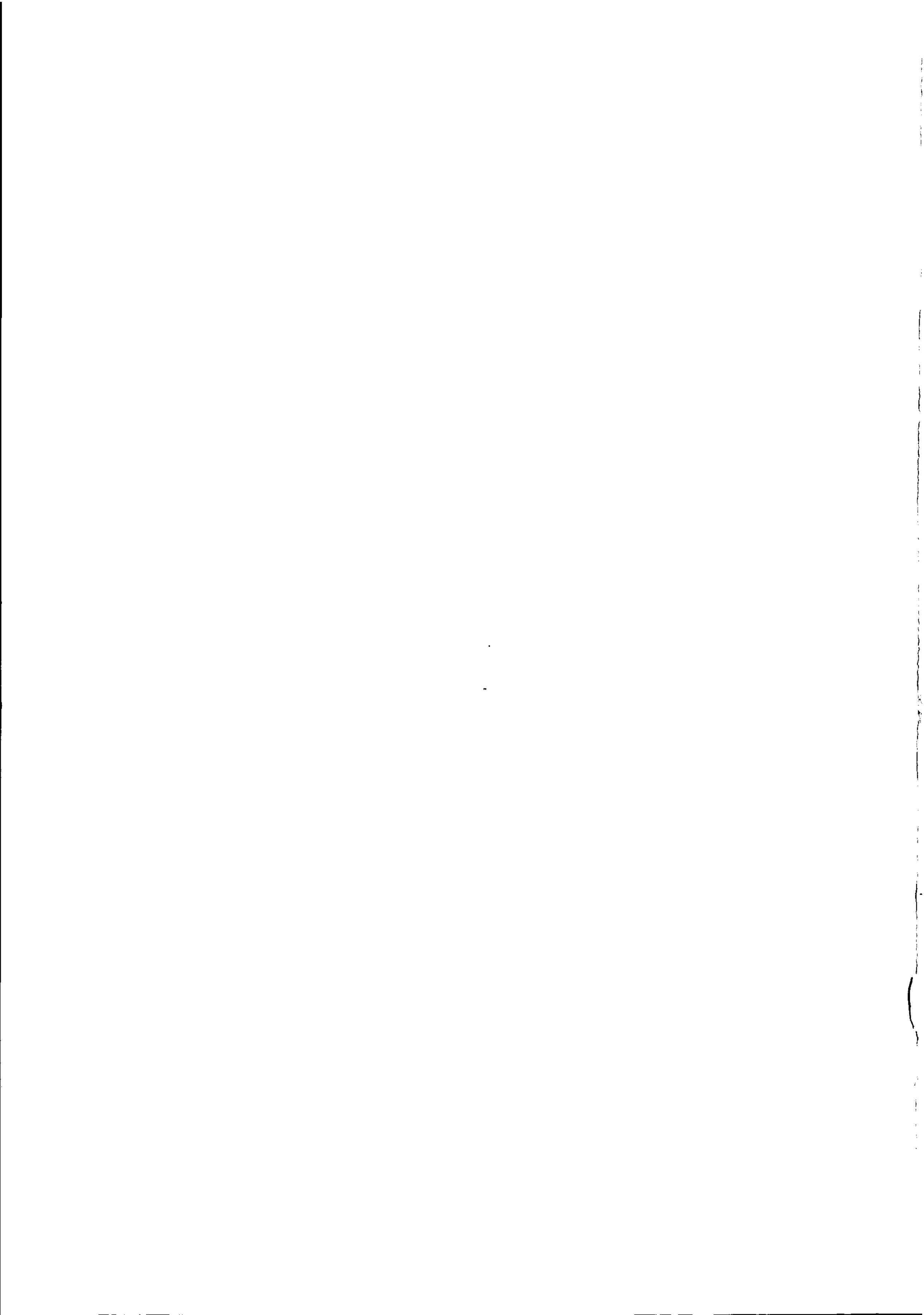
Formation of crystalline-silicon islands for thin-film transistors by excimer-laser-induced lateral growth

Paul van der Wilt



TR 3983 S

Stellingen

behorende bij het proefschrift

Formation of Crystalline-Silicon Islands for Thin-Film Transistors by Excimer-Laser-Induced Lateral Growth

door

Paul van der Wilt

Delft, 6 januari 2003

1. De 'grain filter' methode is een concurrerende methode voor het vervaardigen van dunne-film transistoren met eigenschappen, welke die vervaardigd met perfect kristallijn silicium benaderen.
2. De bovengrens voor de belichtingsenergie in een enkel-puls excimeer-laser kristallisatie proces wordt gevormd door het ontstaan van rimpelingen in de film. Deze worden veroorzaakt onder invloed van door temperatuursgradienten opgewekte verschillen in de oppervlaktespanning.
3. Het beheersen van de kristal orientatie is de ultieme resterende wetenschappelijke uitdaging in de excimeer-laser-kristallisatie van dunne silicium films.
4. Hoewel er in een enkel-puls excimeer-laser kristallisatie proces doorgaans geen patronen geprojecteerd worden, is er toch een projectie systeem gewenst voor het verkrijgen van een scherp afgebakende puls.
5. Bij het gebruik van de atomic force microscope in de contact mode dient men alert te zijn dat de naald daadwerkelijk het oppervlak in kaart brengt in plaats van dat het oppervlak de naald in kaart brengt.
6. Een proefschrift dient geschreven te worden vanuit de optiek dat anderen minder weten van het onderwerp in plaats van dat de kandidaat er meer van weet.
7. Het verschil in arbeidsethos tussen Nederlanders en Amerikanen kan getypeerd worden als respectievelijk het streven naar een levensstijl die past bij het inkomen en het streven naar een inkomen dat past bij de levensstijl.
8. Het gemak van het schrijven van brieven in Microsoft Word veroorzaakt voor een belangrijk deel het slechte imago van dit product aangezien men ten onrechte concludeert direct ook grote documenten te kunnen schrijven.
9. In plaats van veelvuldig de zegen van God over hun land te commanderen, zouden Amerikanen beter de grootsheid van God kunnen scanderen.
10. Voor mensen die alleen onder druk goed presteren is het raadzaam de promotie en de bruiloft op de zelfde dag te plannen.

1. The grain filter method is a competitive method to obtain thin-film transistors with performance approaching those made with perfect crystalline silicon.
2. The upper limit of the radiation energy density for a single-pulse excimer-laser crystallization process is the creation of surface ripples. These are created as a result of differences in the surface tension caused by temperature gradients.
3. The control of the crystallographic orientation is the ultimate remaining scientific challenge in the field of excimer-laser crystallization of thin silicon films.
4. Although commonly no patterns are projected in a single-pulse excimer-laser crystallization process, it is still desirable to have a projection system to obtain a sharply defined spatial profile.
5. When using the atomic-force microscope in the contact mode, one must ensure that the surface is being probed by the tip, rather than that the tip is being probed by the surface.
6. A thesis should be written from the point of view that others know less about the subject rather than that the candidate knows more about it.
7. The difference in work ethics between Dutch and Americans can be characterized by striving for a lifestyle that fits the income and striving for an income that fits the lifestyle, respectively.
8. The ease of writing letters with Microsoft Word is an important cause for the negative image this product has as people wrongly conclude that they are also able to write large documents.
9. Rather than frequently commanding God's blessing over their country, Americans should rather proclaim God's greatness.
10. For those people that only perform well under pressure it is advisable to plan the thesis defence and the wedding on the same day.

Deze stellingen worden verdedigbaar geacht en zijn als zodanig goedgekeurd door de promotor prof. dr. C.I.M. Beenakker.

39919
786390
TR 3983

Formation of Crystalline-Silicon Islands for Thin-Film Transistors by Excimer-Laser-Induced Lateral Growth

Paul van der Wilt

Beghinnen can ick, Volherden will ick, Volbringhen sal ick.

(Geveltekst Kruisstraat 26, Haarlem)

Formation of Crystalline-Silicon Islands for Thin-Film Transistors by Excimer-Laser-Induced Lateral Growth

Proefschrift

BIBLIOTHEEK TECHNISCHE UNIVERSITEIT
Prometheusplein 1
2628 ZC
DELFT

ter verkrijging van de graad van doctor
aan de Technische Universiteit Delft,
op gezag van de Rector Magnificus prof. dr. ir. J.T. Fokkema,
voorzitter van het College voor Promoties,
in het openbaar te verdedigen op maandag 6 januari 2003 om 13.30 uur
door Paul Christiaan VAN DER WILT
elektrotechnisch ingenieur
geboren te Boskoop.

Dit Proefschrift is goedgekeurd door de promotor:

Prof. dr. C.I.M. Beenakker

Samenstelling promotiecommissie:

Rector Magnificus, voorzitter	Technische Universiteit Delft
Prof. dr. C.I.M. Beenakker	Technische Universiteit Delft
Prof. dr. J.N. Burghartz	Technische Universiteit Delft
Prof. dr. R.E.I. Schropp	Universiteit Utrecht
Prof. dr. H. Wallinga	Universiteit Twente
Prof. dr. J.S. Im	Columbia University (USA)
Dr. T. Shimoda	Seiko Epson Corporation (Japan)
Dr. R. Ishihara	Technische Universiteit Delft

Dit werk is mede tot stand gekomen door financiële ondersteuning door de Stichting Fundamenteel Onderzoek der Materie (FOM) te Utrecht.

Van der Wilt, P.C.

Formation of Crystalline-Silicon Islands for Thin-Film Transistors by Excimer-Laser-Induced Lateral Growth, Ph.D. Thesis, Delft University of Technology, 2003.

ISBN 90-6464-066-1

Copyright © by P.C. van der Wilt

All rights reserved.

No part of this publication may be reproduced, stored in a retrieval system, or transmitted in any form or by any means without the prior written permission of the copyright owner

Printed in the Netherlands

Summary

Formation of Crystalline-Silicon Islands for Thin-Film Transistors by Excimer-Laser-Induced Lateral Growth

This thesis presents a new method to form crystalline-silicon islands on a predetermined position in a thin silicon film. Devices were made within these islands and the performance approached that of devices made in crystalline silicon films obtained by the separation by implantation of oxygen (SIMOX) method.

Chapter 1 gives a general introduction. The main application of thin-film transistors (TFTs) is active-matrix LCDs. Depending on device performance, a number of system components can be integrated on the panel, which is believed to lead to better, smaller, and cheaper displays. Although large-grain poly-Si could potentially lead to sufficient performance, it was recognized that device uniformity is degraded by the random location of the grain boundaries. The goal of this research was the development of a method of grain-location control: when the location of the grain is controlled with respect to the subsequent device fabrication, TFTs free of planar defects can be made.

Chapter 2 discusses the excimer-laser crystallization (ELC) of thin silicon films. This method could potentially yield the desired material properties through the concept of controlled super-lateral growth (C-SLG). Furthermore, grain-location control could be obtained when the C-SLG can be manipulated in such a way that it starts on only a single seed. Two concepts of C-SLG in a single-pulse ELC process were selected for further investigation: based on the dependence of the complete-melt energy density on insulator thickness and on film thickness, respectively. We found that the upper limit of a single-pulse ELC process is due to the creation of surface ripples as a result of local differences in surface tension imposed by temperature gradients.

Chapter 3 presents the experimental work. The fabrication of structures that were used to obtain grain-location control and the various laser-crystallization conditions are presented. The device fabrication process used was based on a low-temperature

process in which source and drain implantations are activated through excimer-laser annealing. However, the gate oxide was thermally grown rather than deposited. Finally, the heat-flow simulation model is described.

Chapter 4 presents the results obtained with the heat-sink grain-location control method. It was found that the energy-density window for C-SLG was very limited and that the control of the grain location was low. This was attributed to the insufficient control of both the size of the incompletely molten region and its number of seeds.

Chapter 5 presents two variations of the embedded-seed structure: a cavity in the insulator layer that is filled with silicon. With bottle-shaped cavities, the diameter of the unmolten portion was minimized and the yield of grain-location control was increased. With grain filters, in addition to this, a single seed for lateral growth was successfully selected. This selection was obtained during the vertical growth stage through the cavity that precedes the lateral growth of an island and it is based on the occlusion of grains that is normally observed during re-growth from the liquid phase. Islands with a diameter up to ~7 μm in 250 nm Si films were grown, though often containing planar defects. As was revealed with electron backscatter diffraction measurements, however, the majority were twin boundaries, which are expected to have little influence on device performance. Through a combination of cross-sectional transmission electron microscopy and heat-flow simulations this was attributed to the creation of defects on the rim of the cavity as a result of the growth velocities experienced at this stage. It was found experimentally that defect creation could be largely suppressed by sharpening the rim of the grain filters.

Chapter 6 presents the results from devices that were made in the islands obtained with the grain-filter method as well as in thin c-Si films and in directional poly-Si films. The latter were made by the so-called sequential lateral solidification (SLS) method, which is considered to be a very competitive crystallization method. From the comparison it was found that the performance of the grain-filter TFTs approaches that of the c-Si devices. It was found that they have better sub-threshold behavior but worse above-threshold behavior than the devices made in directional poly-Si TFTs. This was related to the planar defects being less defective but less ideally placed with respect to the current flow. As expected from the microstructure, the diameter of the grain filter was found to have a significant influence on device performance, whereas influence of energy density was less significant. An important aspect that needs to be addressed is that of the poor uniformity of the devices that is likely to be related to the randomness of crystallographic orientation.

Chapter 7 gives a comparison with published device results obtained with alternative crystallization methods and it was found that the grain-filter process is a competitive method to obtain high-performance TFTs.

Paul van der Wilt

Samenvatting

Vorming van Kristallijn-Silicium Eilanden voor Dunne Film Transistoren middels door Excimeer-Laser Teweeggebrachte Laterale Groei

Dit proefschrift bespreekt een nieuwe methode voor de vorming van kristallijn-silicium eilanden op een van te voren aangewezen positie in een dunne silicium laag. Transistoren gemaakt in deze eilanden bleken eigenschappen te bezitten naderend aan die gemaakt in kristallijn silicium (c-Si) lagen verkregen middels de separatie door implantatie van zuurstof (SIMOX) methode.

Hoofdstuk 1 geeft een algemene introductie. De voornaamste toepassing van dunne film transistoren (TFT's) is de actieve matrix LCD. Afhankelijk van de transistor eigenschappen kunnen een aantal systeem componenten op het beeldscherm geïntegreerd worden, hetgeen kan leiden tot betere, kleinere en goedkopere schermen. Hoewel poly-Si tot toereikende transistoren kan leiden, blijkt dat de uniformiteit slecht is door de willekeurig geplaatste kristalgrenzen. Het doel van dit onderzoek was het ontwikkelen van een methode ter vastlegging van de kristallokatie: als de deze vastligt ten opzichte van de daaropvolgende transistor fabricage, kan een TFT zonder planaire defecten gemaakt worden.

Hoofdstuk 2 bespreekt de excimeer-laser kristallisatie (ELC) van dunne silicium lagen. Deze methode kan leiden tot de gewenste materiaal eigenschappen middels het concept van gecontroleerde superlaterale groei (C-SLG). Bovendien kan het vastleggen van de kristallokatie bereikt worden door te verzekeren dat de C-SLG op slechts een enkel entkristal begint. Twee concepten voor C-SLG in een enkel-puls ELC proces zijn geselecteerd: respectievelijk de isolatie- en de laagdikte afhankelijkheid van de energiedichtheid voor volledig smelten. We tonen aan dat de bovengrens in een enkel-puls ELC proces is bepaald door het ontstaan van oppervlakte-rimpelingen door de door temperatuursgradiënten veroorzaakte verschillen in oppervlaktespanning.

Hoofdstuk 3 beschouwt het experimentele werk. De fabricage van structuren voor vastlegging van de kristallokatie en de verschillende omstandigheden voor laser-

kristallisatie worden besproken. De transistor fabricage is gebaseerd op een laag-temperatuurs proces waarin de source- en drain implantaties zijn geacitiveerd met de excimeer laser. Het gate oxide is echter gegroeid middels oxidatie in plaats van gedeponeerd. Als laatste wordt het warmtestroom simulatie model beschreven.

Hoofdstuk 4 beschouwt de resultaten verkregen met de heat sink kristallokatie vastleggingsmethode. Het energiedichtheidsregime voor C-SLG was beperkt en de controle over het aantal entkristallen was beperkt. Dit werd toegeschreven aan de ontoereikende beheersing van zowel de afmeting van het ongesmolten deel alsmede het aantal kiemen.

Hoofdstuk 5 beschouwt twee variaties van de ingebedde kiem structuur: een met silicium gevulde holte in de isolatie. Met flesvormige holtes wordt de afmeting van het ongesmolten deel geminimalizeerd en de opbrengst van kristallokatie vastlegging verhoogd. Met de grain filter wordt bovendien een entkristal voor de laterale groei geselecteerd. Dit gebeurde tijdens de aan de laterale groei voorafgaande vertikale groeifase en wordt toegeschreven aan de uitsluiting van kristallen welke normaal is tijdens planaire kristalgroei vanuit de vloeibare fase. 7 µm grote eilanden zijn verkregen in een 250 nm dikke laag, hoewel doorgaans niet vrij van planaire defecten. Uit metingen aan diffractie patronen gevormd door teruggekaatste electronen bleek echter dat het merendeel grenzen tussen tweelingkristallen waren van welke verwacht wordt dat ze een beperkte invloed op de transistor eigenschappen hebben. Door een combinatie van doorsnede transmissie electronen- microscopie en warmte-stroom simulaties werd geconcludeerd dat deze defecten ontstonden door de hoge groeisnelheden op de rand van de holtes. Het scherper maken van deze randen bleek een effectieve methode om de defect creatie grotendeels tegen te gaan.

Hoofdstuk 6 beschouwt de metingen naar transistoren gemaakt in eilanden verkregen met grain filters alsmede in c-Si lagen en gericht poly-Si lagen. Laatstgenoemde zijn verkregen middels de herhaalde laterale stollings (SLS) methode die beschouwd wordt als een zeer concurrerende methode. Uit de vergelijking bleek dat de eigenschappen naderde aan die van de c-Si transistoren. Het schakelgedrag bleek beter, maar de geleiding bleek minder dan die van gericht poly-Si TFT's. Dit werd toegeschreven aan enerzijds de lagere defectdichtheid en anderzijds de slechtere plaatsing van de planaire defecten. Zoals verwacht had de diameter van de holtes een significante invloed op de transistor eigenschappen terwijl de invloed van de energiedichtheid minder significant was. Een belangrijk onderwerp voor onderzoek is dat van de beperkte uniformiteit van de transistoren, die waarschijnlijk gerelateerd is aan de willekeurige kristalorientatie van de eilanden.

Hoodstuk 7 vergelijkt de resultaten met die van gepubliceerde resultaten verkregen met andere methoden. Het kan geconcludeerd worden dat de grain filter methode een concurrerende methode is voor verkrijging van hoogkwaliteits TFT's.

Paul van der Wilt

Contents

1. Introduction 1

1.1. Background 1
1.1.1 Applications of Thin-Film Transistors 1
1.1.2 Polycrystalline Silicon Thin Films 2
1.1.3 Metal-Oxide Semiconductor Field-Effect Transistors 5
1.1.4 Polycrystalline-Silicon Thin-Film Transistors 6
1.2. Goal of this Research 9
1.3. Outline 10

2. Excimer-Laser Crystallization of Thin Silicon Films 11

2.1. Systems and Samples for ELC 11
2.2. Crystallization Mechanisms 14
2.2.1 Explosive Crystallization 14
2.2.2 Melting and Regrowth 17
2.2.3 Planar Defects in ELC poly-Si 22
2.2.4 Film Damage 23
2.2.5 Grain-Size Enlargement 30
2.3. Controlled Super-Lateral Growth 33

3. Experimental, Analysis, and Heat-Flow Simulations 37

3.1. Experimental 37
3.1.1 Laser Setups 37
3.1.2 Layers and Patterning 39
3.1.3 Manufacturing of Heat Sinks 42
3.1.4 Manufacturing of Embedded-Seed Structures 44
3.1.5 Manufacturing of Thin-Film Transistors 51
3.2. Sample Analysis 55

3.2.1 Material Characterization 55
3.2.2 Device Characterization 57
3.3. Heat-flow Simulations 57

4. Heat-Sink Grain-Location Control 59
4.1. Introduction 59
4.2. Experimental Results 61
4.3. Simulation Results 63
4.4. Discussion and Conclusions 64

5. Embedded-Seed Grain-Location Control 67
5.1. Introduction 67
5.2. Bottle-Shaped Cavities 70
5.3. U-Shaped Cavities 73
5.3.1 Island Properties 73
5.3.2 Defect Analysis 82
5.3.3 Melt Depth and Interface velocity 88
5.4. Discussion and Conclusions 93

6. Properties of Thin-Film Transistors 97
6.1. Introduction 97
6.2. Irregularities in TFT Characteristics 98
6.3. TFT Characteristics 103
6.3.1 Grain-Location Controlled TFTs 103
6.3.2 Grain-Boundary-Location Controlled TFTs 107
6.4. Discussion and Conclusions 110

7. Conclusions 115
7.1. Alternative Crystallization Methods 115
7.1.1 Description of Crystallization Methods 115
7.1.2 Device Comparison 118
7.2. Conclusions and Recommendations 120
7.2.1 Conclusions 121
7.2.2 Recommendations 124

Bibliography 127

Publication List 135

Nawoord 137

About the Author 139

CHAPTER 1

Introduction

1.1. Background

The research presented in this thesis focuses on improving polycrystalline-silicon thin-film transistors (poly-Si TFTs), in particular by improving the semiconductor quality. TFTs can be found in many applications where bulk silicon cannot be used to make transistors. Such applications are for instance those that require very large, transparent or flexible substrates. Often, these substrates are made of nonrefractory materials, such as glass or plastic, which puts a limit to the maximum allowed processing temperature. In general in these applications, a thin layer of semiconducting material to be used in the device fabrication is applied to the substrate.

Another situation in which TFTs are used is when transistors are being stacked, e.g. in order to increase device density and/or to reduce transmission times between devices. Only the first layer of transistors can be made of bulk silicon. For the following layers, a new layer of semiconducting material must be applied.

1.1.1 Applications of Thin-Film Transistors

An important group of applications in which TFTs are used because of the transparency of the substrate is that of displays with active-matrix pixel addressing, e.g. active-matrix liquid-crystal displays (AMLCDs) [1]. In this class of displays, each pixel is equipped with a switch that controls the flow of data to the pixel, as is drawn schematically in Figure 1.1. The switch can be made with a single TFT. Both the gate and the source of the TFT are connected to long interconnect lines, combining an entire row of pixels or an entire column of pixels, respectively. These data and scan lines are connected to drivers placed at the periphery of the display. The scan lines are used to open the gates of one row of TFTs. Simultaneously, the

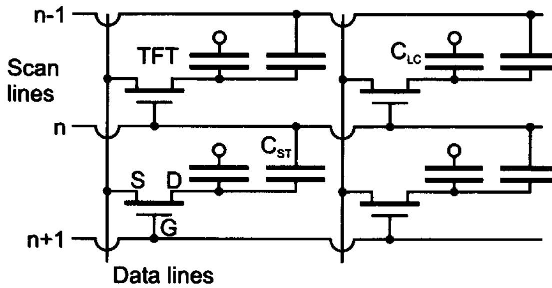


Figure 1.1. Network equivalent of four pixels in an AMLCD. The counter electrode of the pixel capacitor C_{LC} is located on the other substrate. C_{ST} is the storage capacitor.

data lines offer a certain voltage to the source of each of these TFTs. Meanwhile, the other rows pixels are not addressed and it is therefore crucial that the TFTs have a very low off-current in order to maintain the data on these pixels.

Conventionally, the driver circuits are made in bulk silicon, which are subsequently mounted to the periphery of the display, e.g., by flip-chip bonding. Alternatively, the drivers can also be integrated on the display using TFTs. In this case, the TFTs are required to have a high carrier mobility (~50 cm^2/Vs) to allow for sufficiently high-frequency operation [2]. When even higher carrier mobilities (~500 cm^2/Vs) can be realized, it makes sense to also integrate components such as memory and controllers [3]. Additionally, this would require the channel length to go to submicron dimensions. Such a highly integrated system on a single panel could potentially lead to more compact and less expensive displays.

Important components in which stacked transistors are used are static random-access memories (SRAMs) [2]. TFTs are used as load transistors and were introduced to achieve a higher packing density and thus a lower cost. Eventually this development could lead to that of three-dimensionally integrated circuits (3D-ICs): various layers of devices stacked upon each other to reduce area and interconnections.

1.1.2 Polycrystalline Silicon Thin Films

AMORPHOUS-SILICON VERSUS POLYCRYSTALLINE-SILICON

For many applications, sufficiently good TFTs can be made with hydrogenated amorphous silicon (a-Si:H). Such a process is cheap because of the low number of mask steps required. The a-Si:H TFTs have carrier mobilities of ~1 cm^2/Vs, have very low off-currents and are very uniform. An example where a-Si:H TFTs suffice is the pixel switches on larger LCDs. Disadvantages of a-Si:H TFTs are the large dimensions required to achieve sufficient on-current and the fact that they need to be

shielded from incoming light to avoid degradation. The aperture ratio of the display (i.e., the transparency) could be less than 50%, the rest being shielded by the pixel switch [4].

For smaller (i.e., higher resolution) displays this will lead to unacceptably low brightness of the display. For these displays, the TFTs should have higher carrier mobility so that they can be smaller. Poly-Si films fulfill this requirement, also because they do not need to be shielded from the light. Likewise, when driver integration is required, a-Si:H does not offer sufficient carrier mobility and poly-Si TFTs must be used. In this case, the same TFTs should also be used for the pixel switches, as a-Si:H TFTs and poly-Si TFTs cannot easily be made in the same process [5]. Disadvantages of poly-Si TFTs are the higher cost of fabrication and the higher off-currents.

Polycrystalline silicon films can be obtained by direct deposition or by (re-) crystallization of an amorphous or polycrystalline precursor. In addition to this, for large-area electronic applications, such a method should be compatible with low-temperature substrates such as glass. At these conditions, crystallization gives the possibility to grow grains with a diameter far exceeding the film thickness, whereas directly deposited poly-Si films have much smaller grains.

Two common ways to crystallize thin silicon films compatible with these substrates are solid-phase crystallization (SPC) and excimer-laser crystallization (ELC). Both methods have shown considerable improvements in the recent years, albeit sometimes at the cost of increased process complexity. ELC is the method used in this research and will be discussed in detail in Chapter 2. Two alternative methods that will be discussed briefly in Chapter 7 are continuous-wave laser crystallization and metal-induced crystallization. The former resembles zone-melting recrystallization (ZMR), whereas the latter is a solid-phase crystallization process.

GRAIN BOUNDARIES: ELECTRICAL BEHAVIOR

Polycrystalline silicon is characterized by the presence of grain boundaries (GBs) separating small crystals (i.e., grains). This means that unlike a-Si or c-Si films, poly-Si films are not homogeneous, which could heavily impact device uniformity. The grain boundaries constitute a discontinuity of the otherwise periodic lattice and can be seen as planar defects as opposed to point defects (e.g., interstitials and vacancies) or line defects (i.e., dislocations). The boundary planes are filled with dangling bonds and strained bonds, which will lead to the introduction of electronic states in the forbidden gap. Dangling bonds typically lead to deep states (i.e., states around midgap), whereas strained bonds lead to tail states (i.e., states closer to either the conduction or the valence band). The electronic states in the forbidden gap will act as trapping centers for the carriers, which leads to an increase in the

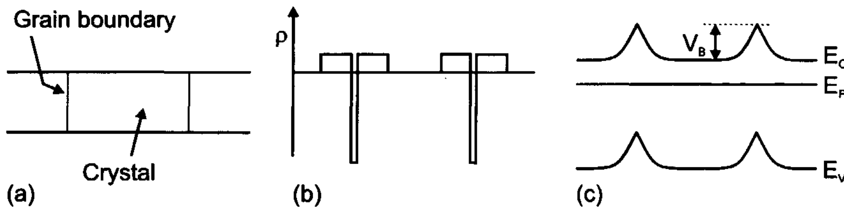


Figure 1.2. (a) Two grain boundaries in n-type poly-Si lead to a charge distribution shown in (b). The resultant energy band diagram is shown in (c).

recombination or generation rates of carriers. This will lead to a modified electrical behavior of poly-Si.

The electrical conduction in poly-Si films is described by the grain-boundary-trapping model [6, 7]. This model assumes that all traps in the poly-Si are located at the grain boundaries and furthermore that they have a monoenergetic distribution around midgap (i.e., only one level of deep states). Carriers are trapped at the grain boundaries and as a result of this charge build-up they are surrounded by depletion regions (Figure 1.2 (b)). The effect of this trapping is thus twofold: (1) the carrier concentration is lowered and (2) potential barriers are formed at the grain boundaries that impede the flow of carriers (Figure 1.2 (c)). Both these effects will lead to a decrease of electrical conductivity with respect to bulk silicon the extent of which scales with the number of grain boundaries, that is, with the grain size.

According to the GB-trapping model, carriers can cross the potential barriers by thermionic emission over the boundaries. The current depends exponentially on $-qV_B/kT$, in which q is the electronic charge (1.6021×10^{-19} C), V_B is the height of the potential barrier, T is the temperature, and k is Boltzmann's constant (1.381×10^{-23} J/K). V_B reaches a maximum when the carrier concentration equals the charge trapped at the grain boundaries. Above this carrier concentration, the potential barrier goes down, and electrical conduction increases. In addition to increasing the grain size, this leads to two concepts of increasing the electrical conduction of a given poly-Si film: (1) increasing the carrier concentration and (2) decreasing the trap state density Q_t of the grain boundaries. The former can be achieved for instance by (heavy) doping of the poly-Si and the latter can be achieved for instance by passivation of the defects by hydrogenation, that is, by lowering Q_t.

GRAIN BOUNDARIES: TRAP STATE DENSITY

The trap state density Q_t of a grain boundary is essentially the number of dangling and strained bonds and depends on the mismatch between the two adjacent grains. When the orientation of the one grain is only slightly rotated with respect to the other grain, Q_t roughly scales with the angle of rotation [8]. As the grains are almost similarly oriented, these low-angle grain boundaries are found to be networks of

discrete dislocations. The spacing of the dislocations decreases for increasing misorientation and it can thus be understood that Q_t increases with the relative rotation angle. These grain boundaries are also referred to as sub-grain boundaries

Above a certain angle of misorientation (~15°), however, this model no longer holds. For these high-angle grain boundaries the mismatch between the two grains can be described by looking at the number atoms that lie on positions common to both grains: so-called coincident sites. The idea in this coincident-site lattice (CSL) model is to discern two sets of positions that the atoms can occupy, which together are called the superlattice. On one side of the boundary the atoms occupy the first set of positions and on the other side of the boundary the atoms occupy the second. If at the boundary itself some of these positions coincide, these positions will then of course be occupied by atoms and the lattice is not disrupted at this point. As a result, there is no dangling bond associated with this position and Q_t is decreased.

The superlattice can be described by the relative number of positions in these two sets that coincide and it is classified by the reciprocal value of this number: the Σ-value. This value describes the periodicity in the superlattice and in general it is true that the mismatch between two grains decreases with increasing periodicity of their superlattice, that is, for low Σ-value. Especially the twin boundaries ($\Sigma3$, $\Sigma9$, $\Sigma27$, etc, or, first order, second order, third order, etc. twin boundaries) are found to have low defect densities. Opposite of these special high-angle grain boundaries are the random high-angle grain boundaries, that have no coincident sites and have a defect density in the order of the surface-state density.

1.1.3 Metal-Oxide Semiconductor Field-Effect Transistors

The electrical behavior of a poly-Si TFT is similar to that of a metal-oxide semiconductor field-effect transistor (MOSFET).

In the linear regime, the drain current in an n-channel MOSFET can be expressed as (assuming that the source voltage $V_S = 0$):

$$I_D = \frac{WC_{ox}\mu_n}{L}\left[(V_G - V_T)V_D - \tfrac{1}{2}V_D^2\right], \tag{1.1}$$

where W and L are the width and the length of the channel region, respectively; V_G, V_D, and V_T are the gate voltage, the drain voltage, and the threshold voltage, respectively; μ_n is the electron mobility; and C_{ox} is the gate-oxide capacitance. For low V_D this equation can be simplified to:

$$I_D \approx \frac{WC_{ox}\mu_n}{L}(V_G - V_T)V_D. \tag{1.2}$$

Due to scattering by the $Si–SiO_2$ interface and the fixed oxide charge, carrier mobility in the inversion layer of a MOSFET is in general much lower than that in bulk silicon [9]. For thermally oxidized silicon, the interface properties are strongly influenced by the crystallographic orientation of the silicon and the carrier mobility varies accordingly [10]. When the interface is rough, the mobility is degraded even more.

In the subthreshold regime (i.e., for weak inversion of the channel surface), the drain current depends exponentially on the gate voltage. The inverse of the slope of $\ln(I_D)$ vs. V_G is known as the subthreshold swing, S. The swing is a measure of the $Si–SiO_2$ interface trap density in MOSFETs. It is found that S is given by:

$$S = \frac{kT}{q}\ln 10\left(1+\frac{C_d + C_{it}}{C_{ox}}\right), \tag{1.3}$$

where C_d is the capacitance of the depletion layer and C_{it} is the capacitance of the interface states.

1.1.4 Polycrystalline-Silicon Thin-Film Transistors

The poly-Si TFT differs from the MOSFET in several respects. The most important one from the point of view of this research is the presence of defects in the channel region. This is shown schematically in Figure 1.3 (a) and (a'). Typically, the grain size in the poly-Si film is much smaller than the active channel dimensions, so that the carriers have to pass many grain boundaries.

ON-CURRENT

Because the channel region is intrinsic or only moderately doped, the potential barriers are high and conductivity is low. By applying a vertical electric field, however, the potential barriers can be lowered in a way similar to that achieved with doping of the film [11]. Based on the GB-trapping model of the poly-Si as a periodic structure of defect-free grains separated by grain boundaries, the current can be written as:

$$I_D \approx \frac{WC_{ox}\mu_n}{L}(V_G - V_T)V_D \times \exp\left(\frac{-qV_B}{kT}\right). \tag{1.4}$$

When it is assumed that the thickness of the conduction layer is proportional to $1/(V_G–V_T)$ and all traps are filled, the grain boundary potential barrier shows the following proportionality [12]:

$$V_B \sim \frac{Q_t^2}{(V_G - V_T)^2}. \tag{1.5}$$

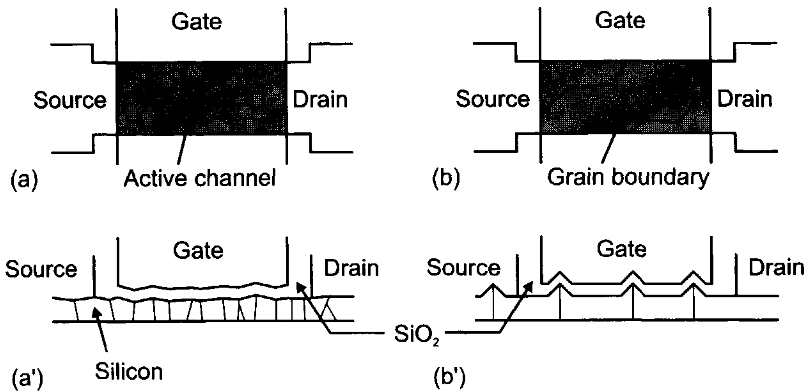


Figure 1.3. Schematic top-view drawings of a TFT with (a) small-grain poly-Si and (b) large-grain poly-Si. (a') and (b') show cross sections of these TFTs.

From this it can be concluded that at high V_G the traps at the grain boundary no longer hamper the flow of carriers [13]. This implies that, given that only few grain boundaries are present, the carrier mobility should approach that of a MOSFET. The presented results, however, showed mobilities much less than this. This could partially be attributed to the fact that tail states have been neglected in the GB-trapping model, as it was assumed that only deep states were present at the grain boundaries. From hydrogenation experiments, however, it is known that the tail states also have a strong influence on carrier mobility [14]. Many of the tail states are intragrain defects rather than that they are located at the grain boundaries and as a result the passivation rate is much lower.

In a different approach to model the conduction in poly-Si TFTs, a continuous density of states (DOS) through the bandgap was employed, that is, including tail states [15]. The defect distribution, however, is spatially uniform, which is in contrast with the GB-trapping model, where traps are concentrated at the grain boundaries. For small-grain non-hydrogenated poly-Si devices, it was found that this model was indeed in better agreement with the experiment than the GB-trapping model [16]. For relatively large grains (i.e., when the grain diameter closes the channel dimensions), however, this model also fails, as the individual contributions of each grain boundary must be taken in account. To this end a model was developed that combines both an intragrain and an intergrain DOS function and indeed more accurate results were obtained with this model [17].

SWING, THRESHOLD VOLTAGE, AND OFF-CURRENT

From hydrogenation experiments [14] it was found that both the subthreshold swing and the threshold voltage are more sensitive to the passivation of deep states than to that of tail states. The swing can then be written as:

$$S = \frac{kT}{q}\ln 10\left(1+\frac{C_d + C_{it} + C_t}{C_{ox}}\right), \tag{1.6}$$

where the term C_t, the capacitance due to the density of (mainly deep) trap states in the film, has been added in comparison to Equation 1.3.

For non-hydrogenated small-grain poly-Si TFTs it was found that the off-current (I_{off}) scales linearly with $-V_D$ [18]. It was assumed that not the generation of the carriers, but the lifetime of the carriers limited the current, and that this caused the Ohmic behavior. This agrees well with the observation that I_{off} scaled with channel length. After hydrogenation, however, carrier lifetime increased considerably and I_{off} became independent of the channel-length. It was assumed that in this case the current became generation rate limited and, furthermore, that generation occurred close to the drain, as the electric field is highest in this region [19]. Although the exact nature of this 'anomalous' leakage current is not agreed upon, it seems plausible that the presence of defects near the drain region plays an important role [20].

LARGE-GRAIN POLY-SI THIN-FILM TRANSISTORS

To obtain poly-Si TFTs with high channel mobility, it is essential to reduce the number of grain boundaries in the active channel region. Since the thin films are typically in the order of 100 nm thick, this requires a process to grow grains with a diameter several times the film thickness. Furthermore, the grains should have a low intragrain density as well. As will be shown in Chapter 2, poly-Si films obtained by excimer-laser crystallization (ELC) satisfy these conditions. However, two problems remain; one is specific to large-grain poly-Si TFTs and the other for ELC poly-Si TFTs:

1. When grain size becomes comparable to the channel dimensions, TFTs can become highly non-uniform [21, 22, 23]. The random location of the grain boundaries leads to large transistor-to-transistor variations in channel properties and subsequently in variations in device characteristics. This situation is schematically drawn in Figure 1.3 (b).

2. As will be explained in Section 2.2.2, large protrusions in the order of the film thickness are commonly associated with the grain boundaries in ELC large-grain poly-Si films. These protrusions can lead to decreased reliability of the device as electric fields over the gate dielectric are locally increased, as can be seen from Figure 1.3 (b') [24]. Also, as is generally the case with increased surface roughness, the carrier mobility, and to a lesser extent V_T and S, will be degraded. Even for SPC poly-Si films, which typically have much smoother surfaces, it was shown that chemical-mechanical polished (CMP) films had better device characteristics [25].

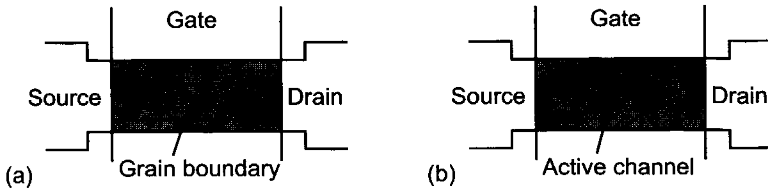


Figure 1.4. Schematic drawings of TFTs in (a) a grain-boundary location-controlled film and (b) a grain location-controlled film.

1.2. Goal of this Research

In order to develop a reliable and uniform high-performance TFT process with ELC poly-Si films, the problems described in the previous section must be solved. In general, these problems can be solved by controlling the melting and solidification behavior of the film. In this thesis, this is achieved by creating structures in or below the film with standard lithography. Alternatively, this can be achieved by manipulating the incoming laser light. Either way, these methods aim at one of the following goals [26]:

1. *Uniform poly-Si film:* Reduce the randomness of the poly-Si film so as to make a more periodical microstructure, for example like the one in Figure 1.4 (a). This way, the device characteristics of the poly-Si TFTs will potentially be more uniform.

2. *Grain-location control:* Make large grains on a predetermined position in the silicon film. If these grains are large enough, a TFT with a single-crystalline channel can be made (Figure 1.4 (b)).

Considering the fact that often the grains in ELC poly-Si films contain planar defects, the second goal could be rephrased as:

2'. Make location-controlled large grains in the film that are free of high-defect density planar defects or, in other words, that are free of planar defects with a high electrical activity.

An important issue is that of the crystallographic orientation of the grains. Especially in the case of grain location-control, it is important that orientation is also controlled. When multiple grains are present in the channel region, as in the case of a periodical microstructure, this issue is less important. To this end, a grain-location control method could of course also be used to create perfectly uniform poly-Si films, in other words, to include a number of location-controlled grains in the active channel region of a TFT. This can then be referred to as grain-boundary-location control.

1.3. Outline

Chapter 2 gives an overview of excimer-laser crystallization of thin silicon films. In the last section, two lithography-based methods to manipulate the growth of large grains are discussed. Based on these two methods, different structures were developed to control the location of a single grain in ELC poly-Si films: heat sinks and embedded seeds. The manufacturing of these structures will be discussed in Chapter 3. Also, the manufacturing of thin-film transistors, the analysis tools, and the heat-flow simulations that were used are described. Results obtained with the heat-sink grain-location control and the embedded-seed grain-location control methods will be described in Chapters 4 and 5, respectively. The most promising of these methods, the grain-filter method, was used to make devices. Results of the DC-characterization is presented in Chapter 6 and a comparison is made with devices made in c-Si, poly-Si and directional poly-Si films. Finally, Chapter 7 compares the work presented in this thesis with that of others as reported in literature. Some recommendations for further research will be given as well.

CHAPTER 2

Excimer-Laser Crystallization of Thin Silicon Films

An early application of pulsed-laser annealing in microelectronics was the annealing of implanted silicon layers and dopant activation [27]. Later it was found that large-grain poly-Si films with a low defect density could be obtained [28]. This could potentially be of great interest to large-area electronics.

The excimer laser is very suitable for pulsed-laser crystallization since it emits high-power and short-wavelength (UV) pulses. An advantage is that at these short wavelengths, the absorption depth in c-Si is less than 7 nm [29] and for a-Si even less. Another advantage is the low spatial coherence of the light and the consequent ease of manipulating it. ELC was first used for TFTs in 1986 [30] as an alternative for SPC. Unlike SPC this is a liquid phase crystallization process and as such, the intragrain defect density is low. The process is also fast and compatible with low-temperature budget materials.

In this chapter an overview of excimer-laser crystallization (ELC) is given. In addition, the results from some supplementary experiments with non-patterned samples are discussed. These experiments were performed to investigate the upper limit of a one-pulse grain-location-control method and to investigate how such a method can be obtained. Based on these findings, two concepts of grain-location control were developed, which will be discussed in Chapters 4 and 5, respectively.

2.1. Systems and Samples for ELC

SYSTEMS

In excimer lasers, a rare gas, such as Kr or Xe, is excited or even positively ionized after collision with an electron. The excited atoms or ions are highly reactive and will form molecules with halogen atoms, such as F or Cl. The thus obtained rare-gas

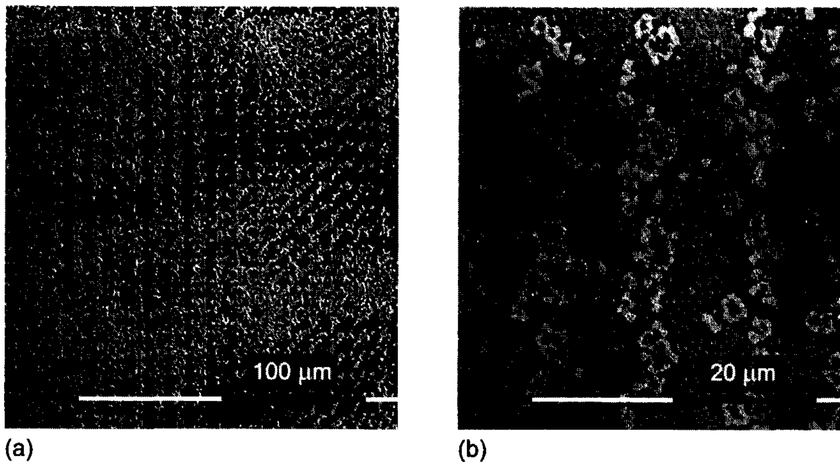


Figure 2.1. Optical microscopy images from a ~215 nm thick silicon film irradiated at the complete melt threshold (0.69 J/cm^2). Due to the interference in the laser light a ~15 μm periodic pattern of molten and incompletely molten regions is created. (a) and (b) show the same region with a different magnification. Images were made using a confocal scan module (CSM) to visualize topography.

halide molecule, or dimer, is in an excited state and after 5-15 ns [31] it will fall back to its ground state under emission of an ultraviolet photon. The term 'excimer' is hence an abbreviation of the words excited dimer. After emission, the molecule will rapidly dissociate, as the rare-gas atom will regain its inert properties. As a result the lifetime of this molecule is extremely short (<10^{-12} s [31]), which ensures population inversion.

Commonly used gas mixtures are Kr with F_2, and Xe with either Cl_2 or HCl. For the KrF laser, the light has a wavelength of 248 nm, whereas for XeCl, it has a wavelength of 308 nm. The latter gas mixture is most popular for laser crystallization and this work was exclusively done with XeCl lasers. Pulse durations are typically in the order of tens of ns. The spatial profile (that is, the intensity profile perpendicular on the direction of propagation) of the pulse is nearly Gaussian in one direction and nearly constant in the other [32]. Most applications, however, need homogeneous irradiation and thus the intensity profile needs to be modified. In general, the beam can be homogenized by splitting it into different beamlets that are subsequently fully overlapped again. The more beamlets the beam is split into, the better the homogeneity. Commonly, this is accomplished by two sets of cylindrical lens arrays [33]. Like the other lenses in the system, these arrays are made of UV-transparent optics, mostly fused silica, and have an anti-reflection coating. The mirrors are coated with a high-reflection coating.

For many lasers other than excimer lasers the spatial coherence of the light is too large and interference patterns will result from the homogenization. Even though the coherence and hence the interference effects with excimer lasers are limited, for some applications, such as laser ablation, it can still lead to an unacceptable intensity fluctuation in the final pulse [34]. The sample in Figure 2.1 was irradiated close to the threshold energy for complete melting and hence the interference effects can clearly be seen.

The ambient under which the samples are irradiated can influence the TFT performance by the absorption of impurities. It was found that an inert ambient with low thermal conductivity such as argon gave the best device performance, although irradiation under vacuum still proved to be much better [35]. The worst devices properties were obtained when the samples were irradiated in air. This was attributed to the incorporation of oxygen atoms and the resultant increased trap state density. The samples in these experiments were irradiated with 96% overlap between consecutive pulses so that each unit of area is irradiated 25 times. It can be assumed that the degradation by oxygen incorporation can effectively be reduced by using a single-pulse process. A further degrading factor could be the increased surface roughness observed for samples irradiated in air [36] leading to enhanced carrier scattering in TFTs.

SAMPLES

For the manufacturing of TFTs, the typical sample configuration is an active layer, in our case silicon, on top of a passive layer, in our case SiO_2. As described in Chapter 1, ELC is particularly interesting for applications on transparent substrates. Although quartz is used, more commonly glass is used as it is cheaper and has a thermal expansion coefficient that better matches that of the silicon active layer [37].

The precursor of the active layer is commonly an amorphous silicon film. Often, this film is deposited by LPCVD at temperatures around 550°C when the precursor is silane (SiH_4) or around 470°C when the precursor is disilane (Si_2H_6). These temperatures are below the softening point of most glasses [37]. When even lower temperatures are required, plasma-enhanced CVD (PECVD) a-Si, typically deposited at 250°C, is used. These films have a hydrogen content of ~10 atom % or even more. When irradiated at energy densities high enough to completely melt the film, it will ablate by the explosive release of hydrogen. Therefore, the films have to be dehydrogenated either thermally at temperatures of ~500°C or by laser irradiation at low energy densities [38] prior to the actual crystallization.

The silicon film is normally separated from the substrate by an SiO_2 layer. This layer is needed both as a thermal insulator to protect the glass and as a diffusion barrier against impurities from the glass [39]. In one report it was calculated that for irradiation of a 100 nm a-Si film preheated at 400°C, a 1.5 μm thick SiO_2 layer was

needed to keep the substrate below 600°C [40], although in practice thinner layers are found to suffice. When working with c-Si substrates, an insulating film may be utilized to reduce the cooling rate of the film, which will lead to better material characteristics (Section 2.2.5) [41].

2.2. Crystallization Mechanisms

During pulsed-laser crystallization of LPCVD a-Si, the material proceeds through various phases. A number of transformations are thus observed depending on the incident laser energy density. Also, the morphology of the film changes through the process. The initially smooth film gets roughened and for high energy density it could even become discontinuous.

2.2.1 Explosive Crystallization

The melting point of amorphous silicon lies below that of crystalline silicon (=1685 K) by 200-300 K [42]. Because of this, the rapid melting of a-Si results in a deeply supercooled liquid. Without the presence or nucleation of crystalline fractions (i.e., seeds for crystal growth) the liquid silicon will not crystallize when cooling down and it will again solidify as a-Si. This amorphization can only occur at very high cooling rates and a critical velocity of the interface of 15 m/s was reported for the growth of a-Si [43].

At lower cooling rates the supercooled liquid will crystallize, either on available seeds or on nucleated seeds. The heat of fusion that is released during this crystallization will further melt the remaining a-Si, which is again followed by immediate crystallization. This rapid and self-sustaining transformation of an amorphous precursor into fine-grain polycrystalline material is called explosive crystallization (XC) and it was shown that this transformation is indeed intermediated by melting [44]. Also, it was shown by transient conductance measurements that this transformation is common in pulsed-laser crystallization of a-Si [45]. Combined with surface-reflectance measurements, these measurements showed that a molten layer propagates through the amorphous film leaving fine-grain poly-Si behind. This transformation will continue until it is quenched by the loss of heat required to raise the temperature of the a-Si to the melting point.

For growth-front velocities less than the critical velocity for amorphization, two scenarios can be distinguished (both shown in Figure 2.2):

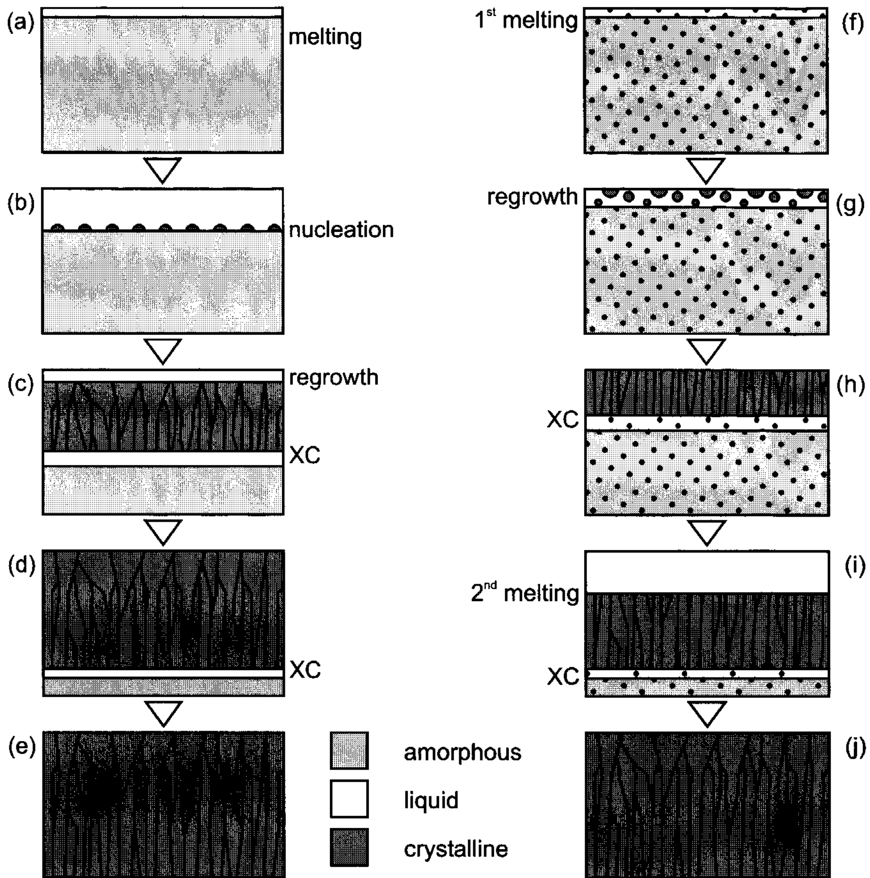


Figure 2.2. Schematic drawings of the explosive crystallization in a fully a-Si film (a)-(e) and an a-Si film containing small crystalline clusters (f)-(j). In latter series, for simplicity it is assumed that seeds are distributed uniformly over the film.

1. The film is fully amorphous, that is, no crystalline fractions are present in the film. When the film is completely molten (i.e., when irradiated at high energy density), all a-Si melts and no XC occurs. When the silicon is only partially molten, however, seeds for crystal growth will be heterogeneously nucleated at the solid–liquid interface. The molten silicon will subsequently solidify as poly-Si. At the same time, the heat of fusion that is released in the process will trigger the XC of the underlying previously unmolten a-Si.
2. The film contains small crystalline fractions. Initially, the film will not melt completely as the crystalline fractions have a higher melting temperature than the amorphous matrix in which they are embedded. As the melt is deeply supercooled, it will immediately start to solidify on these crystalline fractions. Again, the heat of fusion that is released will trigger the XC of the underlying

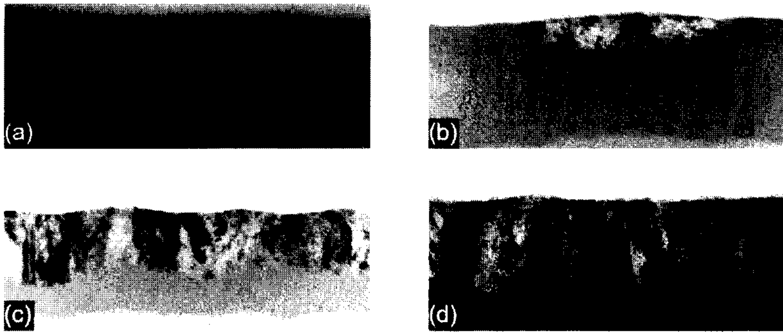


Figure 2.3. Cross-sectional TEM images of a 200 nm thick silicon film taken from reference [48]: Films were irradiated at (a) 156 mJ/cm^2, (b) 166 mJ/cm^2, (c) 185 mJ/cm^2, and (d) 210 mJ/cm^2.

a-Si. Note that compared to the case of a fully amorphous films, the XC takes place in a much earlier stage and is followed by a secondary melt. This implies that this transformation will occur regardless of whether the film is partially or completely molten.

It was suggested that LPCVD a-Si contains small crystalline fractions as it was observed from transient reflectance measurements that XC always occurs regardless of the energy density [28, 46]. Implanted a-Si films, on the other hand, are fully amorphous and will behave according to the first scenario. Hence, when the implanted film is an LPCVD a-Si film, there is a threshold implantation dose above which all crystalline fractions are removed by the implantation. This coincides with a change in the solid-phase crystallization (SPC) behavior [47]: below the threshold, some crystalline fractions remain after implantation and the sample will automatically start to crystallize when heated. Above the threshold, however, no crystal fractions remain and crystals have to nucleate. As a result, there is an incubation time before the onset of crystallization.

Figure 2.3 shows a TEM analysis of the various stages of explosive crystallization for a 200 nm thick LPCVD a-Si film: at the melt-threshold the film will melt locally (due to the energy fluctuations) and the XC is triggered at those isolated melts. The transformation is quenched rapidly and small XC poly-Si islands remain. As this transformation takes place with high interface velocity (velocities exceeding 10 m/s are reported [45]), the grains have a very high defect density. For increasing energy density, more of the surface is melted and accordingly, more of the film is transformed into small-grain poly-Si. From the TEM analysis it was found that the grains are columnar and typically have a diameter of 20-50 nm [49].

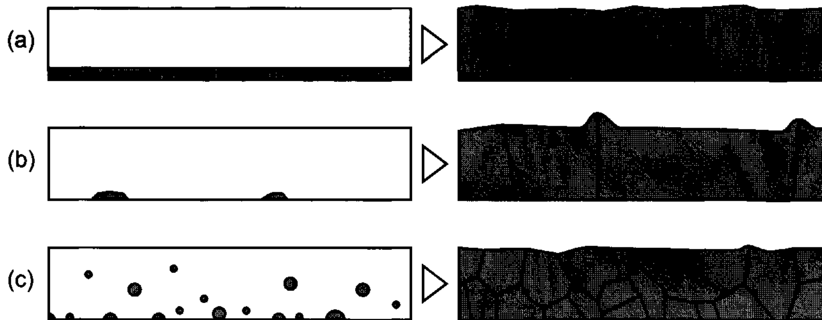


Figure 2.4. Schematic drawings of three different regrowth scenarios: (a) incomplete melt, (b) near-complete melt, and (c) complete melt, followed by nucleation of solids.

2.2.2 Melting and Regrowth

INCOMPLETE MELT

Above a certain threshold energy density, the explosively crystallized silicon will remelt at the surface (Figure 2.4 (a)). Unlike the previous, primary melt, this secondary melt is not severely supercooled and as a result the solidification rate is much lower (heat-flow simulations showed typical regrowth velocities of 2 m/s [50]). Therefore, even though the solidification is seeded by the highly defective XC poly-Si, the defect density of the grains is much lower, as can be seen in Figure 2.5 (a). Also, as many grains are occluded during the epitaxial regrowth, the average grain size is much larger. When the secondary melt is sufficiently deep, this occlusion mechanism can lead to grains with a diameter comparable to the film thickness. The reduced number of planar defects in the film will lead to improved TFT characteristics [51].

COMPLETE MELT

At a certain energy density, the film will melt completely (Figure 2.4 (c)). Above this complete-melt energy density (E_{CM}), there are no solid seeds for growth left. Therefore, as the liquid film cools down and reaches the solidification temperature, it will not immediately solidify, as solids first have to be nucleated. This allows the film to become severely supercooled as much as ~500 K below steady-state solidification temperature [52].

According to the classical nucleation theory, solid atom clusters are always present in the melt by random fluctuations [53]. Above the equilibrium melting temperature T_m, these clusters are small and unstable but below it, they could become stable, given that they overcome a certain critical dimension. This process is

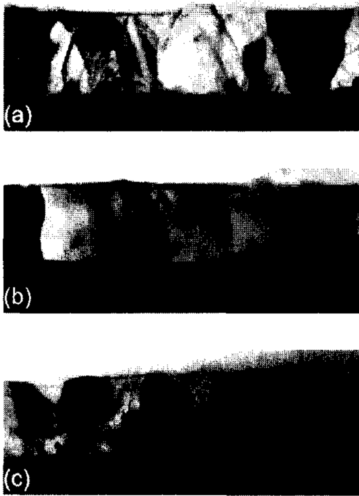


Figure 2.5. Cross-sectional TEM pictures of a 200 nm silicon film taken from reference [48]: Films were irradiated at (a) 590 mJ/cm^2, (b) 665 mJ/cm^2, and (c) 740 mJ/cm^2.

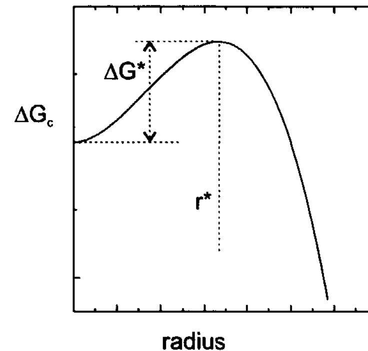


Figure 2.6. The free energy of a solid cluster in a supercooled liquid (Equation 2.1), with r* the critical nucleus radius and ΔG* the accompanying change in the free energy.

called nucleation and after nucleï are formed, the film will rapidly solidify. Assuming the clusters are spherical, the critical radius r* can be derived from the change in total free energy associated with the formation of a solid atom cluster. There are two contributing factors: the first is the change in volumetric free energy in going from the liquid phase to the solid phase ($\Delta G_{V,ls}$). Below T_m, this change in free energy becomes negative, as the solid phase is more favorable. The second factor is the change in free energy associated with the formation of a discontinuity: the surface free energy of the cluster (σ_{ls}). Unlike $\Delta G_{V,ls}$, this energy is always positive. The total free energy associated with the cluster formation (ΔG_c) can then be expressed as follows:

$$\Delta G_c = \frac{4}{3}\pi r^3 \Delta G_{V,ls} + 4\pi r^2 \sigma_{ls} . \tag{2.1}$$

This relationship is plotted in Figure 2.6 and it can be seen that for small radius, the addition of atoms to the cluster will increase the total free energy of the system and as a result, these clusters are unstable. Above the critical radius r*, however, the addition of atoms leads to a decrease of the free energy of the system and the cluster becomes a stable nucleus for crystal growth.

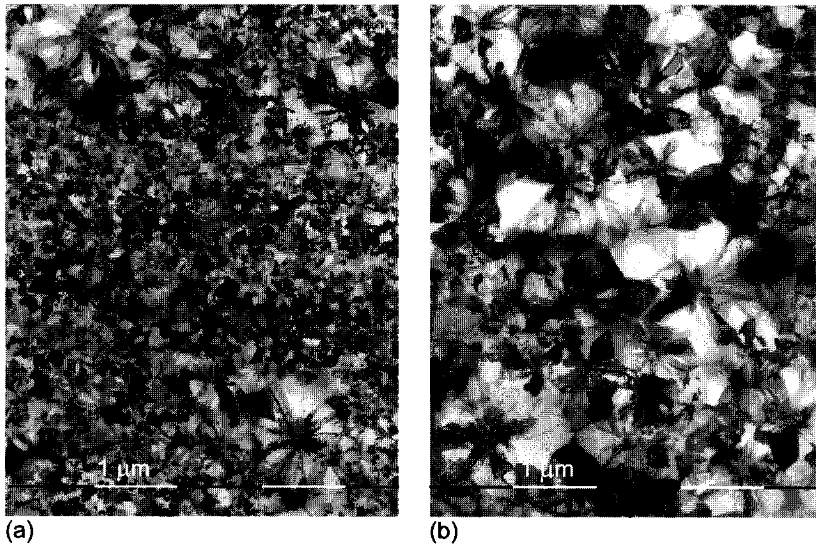


Figure 2.7. Top view bright field TEM images of (a) a 150 nm silicon film irradiated at ~1.58 × E_{CM} and (b) a 250 nm silicon film irradiated at 1.27 × E_{CM}. The pulse duration was ~190 ns.

It is found that the rate of nucleation is a strong exponential function of temperature [53]. At moderate supercooling, $\Delta G_{V,ls}$ is relatively small and as a result r* is very large. At the same time, however, the solid clusters are very small and as a result, the nucleation rate is negligible. As temperature decreases, however, r* will decrease whereas the clusters will grow larger. At sufficient supercooling, stable nucleï will be formed and the material will start to solidify. The temperature at which this occurs depends strongly on the cooling rate: at higher cooling rates, the temperature at which nucleation starts will be lower. This is caused by the finite time required to create super-critical clusters. The temperature at which nucleation starts, is further affected by the exact nucleation mechanism. When for example, impurities or interfaces are present, these could trigger heterogeneous nucleation well before the onset of nucleation in the bulk or homogeneous nucleation.

Initially, both the nucleation rate and the solidification rate are very high. Very soon, however, the film will start to heat up again (a phenomenon called recalescence) by the release of latent heat. As a result, the nucleation of solids comes to an end. Eventually, the film will reach a steady-state solidification temperature and the solidification rate will drop accordingly. In the case of thin silicon films, the steady-state solidification temperature was believed to be only a few tens of degrees below T_m, leading to growth-front velocities of ~1 – 2.5 m/s [54].

The top-view image of a nucleated film in Figure 2.7 (a) shows that the nucleated-grain diameter exhibits a bimodal distribution: a few large grains coexist among

many small grains. As film thickness increases, a shift of the distribution to the larger grains is observed, as can be seen in Figure 2.7 (b). Also, by cross-sectional TEM investigation it was found that the small grains exist throughout the film, whereas the large grains always seem to originate at (or close to) the Si – SiO_2 interface. It could be that the larger grains originate on the earliest nucleation events, which would explain their location near the (cool) interface and their larger diameter. Alternatively, it could be that the former is the result of homogeneous nucleation and that the latter is due to heterogeneous nucleation at the interface [55]. The simultaneous occurrence of both types then suggests a competitive behavior: although the heterogeneous nucleation takes place at lower degree of supercooling than the homogeneous nucleation, its rate is very low, so that copious homogeneous nucleation can also occur.

The large grains in Figure 2.7 are seen to contain a highly defective core surrounded by a ring of low-defect grains. Although these grains originate from the same nucleus, often they no longer show any relationship in terms of crystallographic orientation. This could be due to the growth initially taking place at deep supercooling and therefore being highly defective. Alternatively, it has been suggested that this is related to the nucleation of a-Si seeds rather than c-Si seeds [54]. According to this paper, the initially amorphous core of the grain will later on transform to c-Si by explosive crystallization right after crystals are nucleated at the solid – liquid interface. The nucleation events will lead to the growth of multiple unrelated grains. This then leads to the typical flower-like microstructure observed in nucleated films.

NEAR-COMPLETE MELT

In the incomplete melt regime, the grain size only marginally increases with the energy density. Close to E_{CM}, however, the grain size increases rapidly and will start to exceed the film thickness. This super-lateral growth (SLG) phenomenon has been related to the near-complete melting of the silicon film: parts of the film are completely melted, whereas at other positions, solid remains (Figure 2.4 (b)) [28]. Very close to E_{CM}, the unmolten part of the film reduces to a collection of isolated solid seeds at the interface. During the subsequent solidification, these seeds will grow laterally until they collide with other growing grains. Initially, these opposing growth fronts will originate from other solid seeds, like in Figure 2.5 (b). When the solid seeds are spaced farther apart, however, the opposing growth fronts could also originate from nucleated solids. In this case, one can discern a lateral-growth time interval (Δt_{LG}) between the onset of solidification and the onset of nucleation. During this interval, only grains from unmolten seeds will grow and the lateral growth distance will thus roughly scale with Δt_{LG}. Figure 2.8 shows laterally grown grains that are surrounded by nucleated matter (as the samples were treated with a defect-delineating etchant (Section 3.2.1), most of the nucleated film was etched away). It

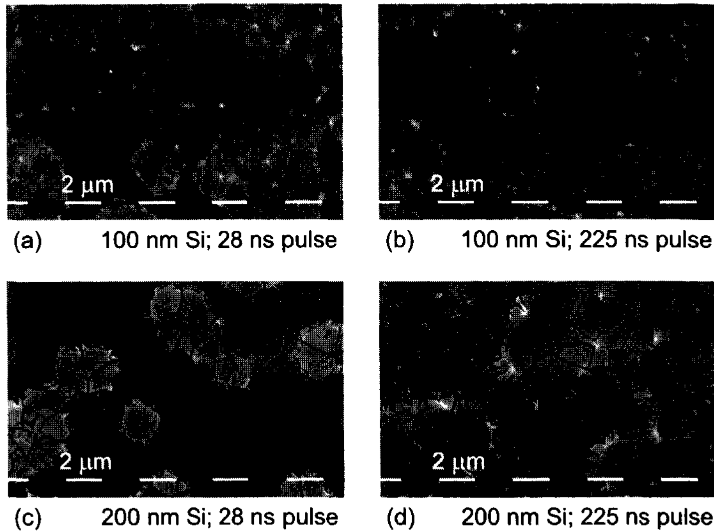


Figure 2.8. Top view SEM images of samples irradiated at E_{CM} with different film thickness and pulse duration. Note the differences in lateral growth distance: an increase is observed for increased film thickness and pulse duration.

can be seen that the lateral growth distance scales with both film thickness and pulse duration. This is related to a reduction of the cooling rate, which leads to an increase in Δt_{LG} (Section 2.2.5).

SLG is observed at the transition between two regimes and it is not a regime in itself. Still, it is tempting to talk about a regime, as the transition from the one to the other regime is far from abrupt. In this view, one can talk about an energy-density process window in which very large grains are obtained, and a value of +/– 2.5% of the energy density was mentioned [56]. Pulse uniformity and pulse-to-pulse stability of many state-of-the-art lasers, however, is in the same order. Therefore, this 'regime' is not really applicable to an industrial process, although promising results were obtained by scanning a ramped line beam over the film [51]. In this method, the film is irradiated multiple times. Each part of the film is subjected to a number of pulses in which it is completely molten. The energy density, however, is slowly decreasing, so that there is at least one pulse in which the film is nearly completely molten. The rest of the pulses will be in the incomplete melt regime so that the SLG microstructure is not significantly changed.

The large spread in the local melt-through conditions could speculatively be related to the non-uniform melting behavior of the many grains in the XC poly-Si. The various grains will differ in crystallographic orientation and in defect density. These differences are very likely to cause a heterogeneous melting behavior. It was suggested that the more defective grains melt before the less defective grains and that

this explains the low defect density of the solidified large-grain poly-Si film [48]. This is more so because the solidification takes place at only moderate supercooling and only few additional defects are created during the crystal growth.

During solidification the silicon expands as the density of solid silicon lies below that of liquid silicon [57]. For vertical regrowth (the incomplete melt regime) this has only few consequences for the surface roughness. In the case of lateral growth, however, this results in the lateral transport of liquid silicon pushed forward by the growth front [58]. When two growth fronts collide, this accumulated liquid protrudes and solidifies as a ridge. When three or more growth fronts collide, a hillock is formed at that point. The height of the hillock could be in the order of the film thickness.

2.2.3 Planar Defects in ELC poly-Si

The performance of poly-Si TFTs is governed in part by the presence of planar defects, as was discussed in Section 1.1. Three categories of defects that are commonly observed in ELC poly-Si films are:

1. Random grain boundaries between grains that were grown from different seeds. These are typically high-angle grain boundaries with high defect density. As was mentioned in previous section, in the SLG regime, these typically come together with ridges and hillocks.
2. Defects created due to breakdown of the growth front. During re-growth of incompletely molten silicon films, growth can become defective if interface velocity is too high for the atoms to be placed correctly [59]. Obviously, this effect is highly dependent on the crystallographic orientation as some orientations have a more densely packed surface than others and consequently a higher energy barrier for the creation of a new crystal plane. Initially, this will result in the formation of stacking faults and twins. For even higher velocities, the growth front will completely break down and a-Si will be formed. This has also been observed in lateral growth in ultra-thin silicon films [60]. The critical velocities above which defects are created were reported to range from 5-6 m/s for {111} oriented grains to 14 m/s for {001} oriented grains.
3. Planar defects that are formed during the lateral growth of silicon. This defect formation was related to the thermal stresses associated with the rapid cooling [61]. In this plastic deformation model, it was proposed that the tensile elastic strain in the silicon slowly builds up until, as lateral growth proceeds, yielding of the material occurs. The defect formation was dependent on crystallographic orientation: for some orientations, defect-free growth proceeded much longer than for other orientations. Also, depending on crystallographic orientation,

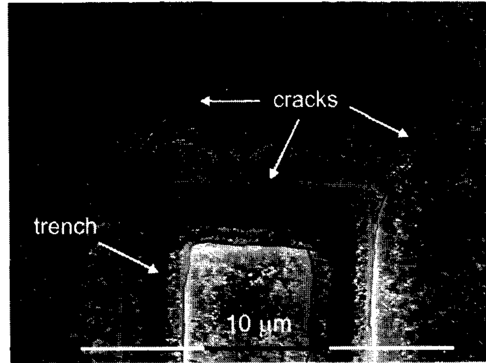


Figure 2.9. Top-view SEM image of a 'cracked' film. Before silicon deposition, a trench was etched in the SiO_2. After defect delineation, cracks are observed that run parallel to the edge of the trench and from the corners of the trench into the planar region.

different types of planar defects were seen to dominate [62]. Mostly, sub-grain boundaries were observed, but for certain crystallographic orientations also microtwins (i.e., closely stacked twin boundaries) and stacking faults were found to be common. If after the formation of a sub-grain boundary the lateral growth proceeded even further, it was found that it gradually transformed in a random grain boundary. At this point, the relation between the sub-grains was completely lost and the boundaries between them are typically random and high-angle grain boundaries. The spacing between these boundaries was shown to scale predominantly with the film thickness.

2.2.4 Film Damage

As this thesis deals with a single-pulse ELC process, any source of damage that is created in one pulse can put a limit on the application of such a process. Two sources of film damage were observed: agglomeration and cracking. The latter was, however, only observed after defect delineating with a wet etchant of $\geq$ 200 nm thick films (Section 3.2.1). The example in Figure 2.9 shows that typically cracks originate from steps in the film that were created during lithography. This indicates that cracks are formed by a release of thermal stress that was build up during solidification due to the difference in thermal expansion rates of silicon and SiO_2.

SINGLE-PULSE AGGLOMERATION

The wetting properties of a liquid film on a solid substrate are determined by the film-vapor interfacial free energy of the liquid (γ_{fv}), the film-substrate interfacial free

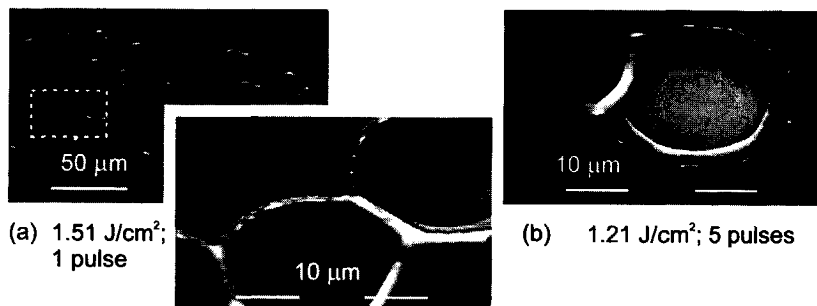


Figure 2.10. SEM images of agglomerated films taken at an angle of 45°. (a) and (b) show the agglomeration due to one pulse, but at different magnifications. (c) shows the agglomeration after 5 pulses. Note that the dimension of the holes after the previous pulses is still visible in the SiO_2.

energy (γ_{fs}), and the substrate-vapor interfacial free energy (γ_{sv}) [63]. The thin film is in a metastable equilibrium when:

$$\gamma_{fv} + \gamma_{fs} > \gamma_{sv}, \tag{2.2}$$

or, in other words, when the total free energy of the system can be lowered by (partial) removal of the film. Partial de-wetting is accomplished by decomposition of the film into a collection of beads, that is, by agglomeration. It is known from zone-melting recrystallization (ZMR) experiments that a silicon film on SiO_2 indeed tends to agglomerate when sufficiently heated [64]. In pulsed-laser irradiation of silicon films, this phenomenon was used to create periodic patterns in the film [65].

The condition for agglomeration to happen, however, is the formation of holes in the film. As soon as such holes are formed, they will grow in diameter until they collide and the film is decomposed into beads. However, when the duration of the melt is very short, as in the case of ELC, the holes may not collide but solidify instead, as can be seen in Figure 2.10 (a) and (b). The diameter of the hole is typically in the range from 5 to 35 μm as a function of film thickness and energy density. When the film is molten again by a subsequent laser pulse, the hole will grow further (Figure 2.10 (c)).

We observed that in a single-pulse ELC process with a-Si as a precursor, agglomeration holes appear in the film at an energy density well beyond E_{CM}. This critical energy density for agglomeration (E_{AGG}) is not well defined as the density of holes is very low (typically less than ten holes in a ~0.5 cm^2 spot were observed). For increasing energy density, however, the density of holes increased until at a certain point the entire film decomposed into beads. Beyond this point, ablation of the film was observed. As this coincided with energy density at which the holes cover the

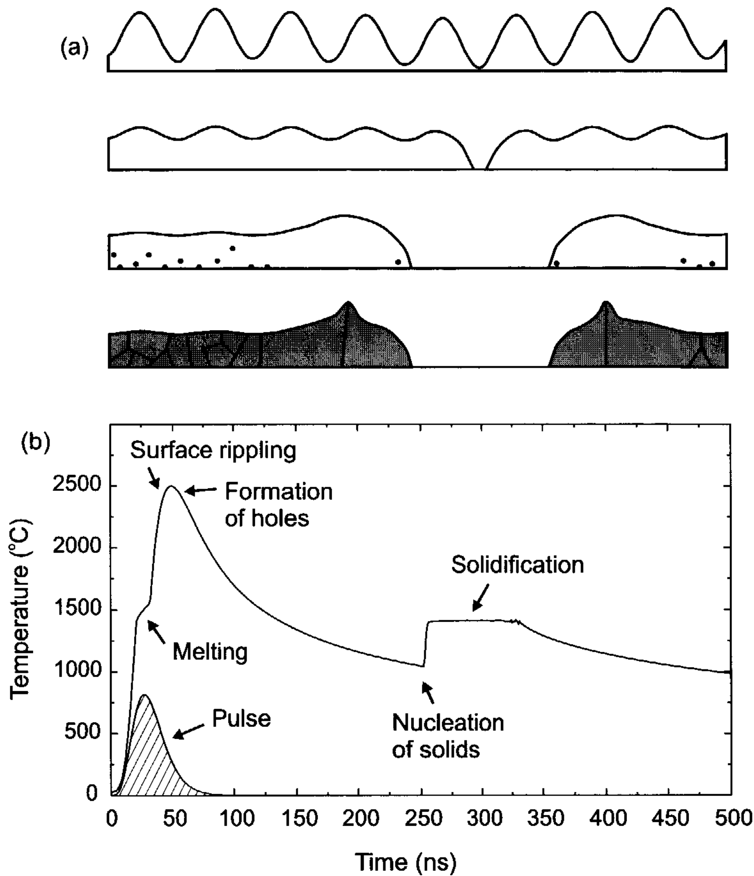


Figure 2.11. (a): Schematic drawings of the agglomeration of a completely molten film. Note that the frequency of the film thickness fluctuations is highly exaggerated. (b): A typical temperature trace of (the surface of) a completely molten film (28 ns pulse, 100 nnm Si) generated by the simulation package used in this work (Section 3.3).

entire surface, it could be concluded that ablation was not related to evaporation of the film, but to excessive agglomeration.

The formation of a hole requires the occurrence of thickness fluctuations of the liquid silicon film. This is clarified by the schematic drawing in Figure 2.11 (a). The amplitude of the fluctuations has to be such that the film surface reaches the SiO_2 interface. From the observation that agglomeration does indeed take place, it can be deduced that these fluctuations must have been present at some stage during the laser-crystallization process. After solidification, however, we did not observe such large-amplitude fluctuations. The film, however, did show small-amplitude fluctuations with a wavelength in the order of several μm. The amplitude of the

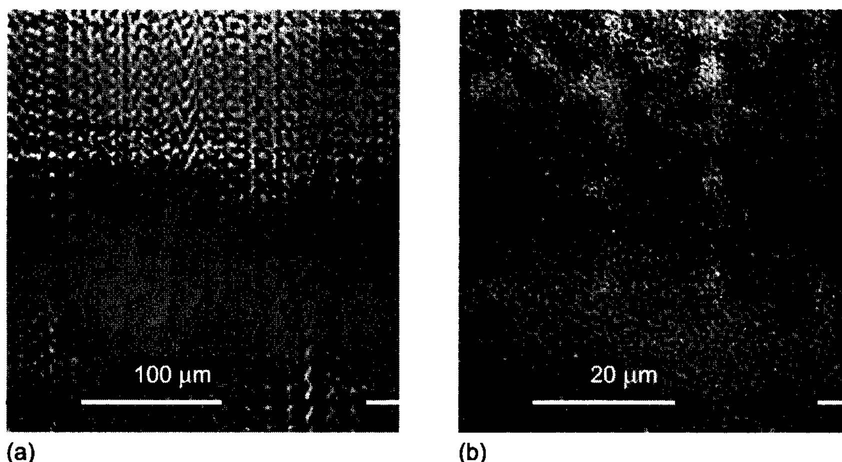


Figure 2.12. Optical microscopy images of a 215 nm silicon film irradiated at the threshold for surface ripples at different magnification (0.95 J/cm^2 = 1.37 x E_{CM}). Note the abruptness of the process visible due to non-uniformity of the laser light. Images were made using a confocal scan module (CSM) to visualize topography.

ripples was in the order of tens of nm and they were best observed with optical microscopy as can be seen in Figure 2.12. These ripples were only observed in films irradiated at or above a well-defined energy density beyond E_{CM}. From Figure 2.12, it can be seen that this energy density threshold for surface ripples (E_{SR}) was very abrupt.

The onset of agglomeration was seen to always occur at energy densities somewhat above E_{SR} as can be seen from the optical microscopy images in Figure 2.13. From this, it seems plausible to assume that the two effects are related. Apparently, the fluctuations must have been created at an early stage of the process at which time they must have been much larger. During the remainder of the melt, however, they were damped, presumably by the surface tension of the liquid. At the time of solidification through nucleation, only small-amplitude ripples remained.

The maximum amplitude of the thickness fluctuations can be deduced from the agglomeration characteristics. At energy densities slightly above E_{SR}, no agglomeration holes were observed and apparently, the fluctuations were still smaller than the film thickness. At E_{AGG}, however, the first agglomeration holes appeared, which indicates that the thickness fluctuations were now in the order of the film thickness. From Figure 2.13 it can be seen that the holes that were created all had the same diameter of a few μm, indicates they were all formed at the same time and that growth could proceed for at least some time before solidification. This supports the earlier conclusion that film thickness fluctuations reach their maximum at an early stage in the process. From Figure 2.13 it can also be seen that the diameter of the

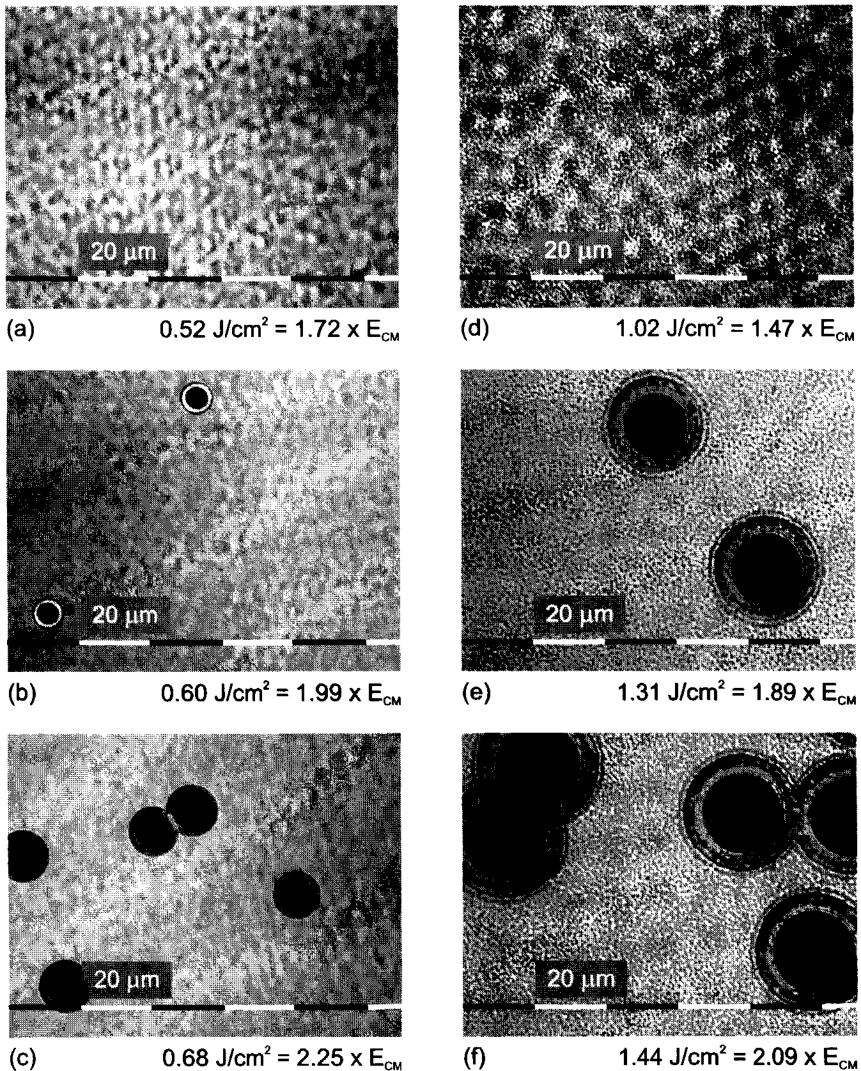


Figure 2.13. Optical microscopy images (CSM) showing surface ripples and agglomeration for different energy densities and film thickness (a-c: 60 nm, d-f: 215 nm)

agglomeration holes scaled with both the film thickness and the energy density, which could be related to the increase of melt duration.

Surface rippling is very common with pulsed-laser annealing of surfaces or thin films [66]. Often, the source of rippling is related to non-uniformities in the spatial profile of the laser pulse. In addition to the intensity fluctuations that originate from the homogenizing (Section 2.1), such non-uniformity can also be created by

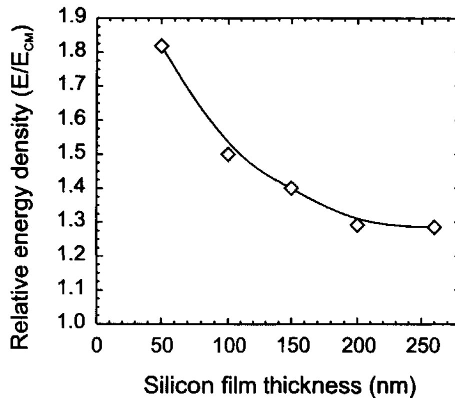
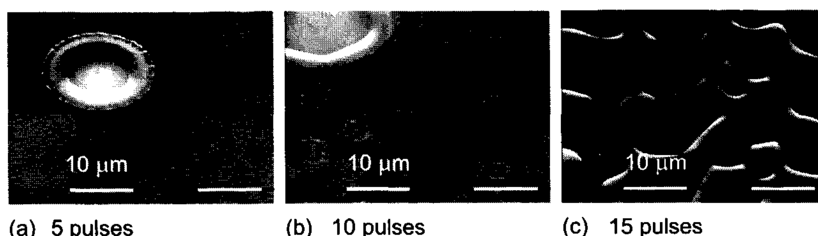


Figure 2.14. The relative threshold for surface rippling (E_{SR}/E_{CM}) as a function of film thickness.

interference between the incident beam and the laterally scattered beams [67]. Lateral scattering can for instance take place on particles that lie on the sample surface, which will lead to a set of concentric circular waves around the scattering source [68]. In a multiple-pulse ELC process, lateral scattering can also result from hillocks produced during the preceding pulses [36]. Eventually, this could lead to a highly periodic surface ripples with a periodicity dictated by the wavelength of the incoming light. As this work deals solely with single-pulse processes and with smooth samples processed in a clean environment, neither of these scattering mechanisms were expected to contribute to the creation of surface ripples.

Comparison of Figure 2.1 to Figure 2.12 shows similar periodicities in the surface ripples. From this it can be concluded that the onset of surface rippling was related to the beam non-uniformity originating from the homogenizer. One way that this non-uniformity could lead to surface ripples is through acoustic surface waves. Such waves can for example be created by the recoil after the laser pulse [69], by an explosive phase change [70] or by the volume change upon melting [71]. When acoustic waves are created in a thin film, the wavelength is expected to scale with the film thickness. Although it can be seen from Figure 2.13 that this was indeed the case, the fact that E_{SR} is well above E_{CM} indicates that there is no relation to the above-mentioned sources of acoustic surface waves and thus the surface ripples are not created by acoustic surface waves. Also, the possible melting of the underlying SiO_2 layer cannot be related to the surface rippling, as it was found that E_{SR} occurred at identical relative energy density (E/E_{CM}) when the silicon was deposited on Si_3N_4 instead of SiO_2.

Another way in which non-uniform heating can lead to surface rippling is through surface-tension gradients [72]. In general, the surface tension of a liquid decreases with temperature. When one part of the film is hotter than another, there will thus be



(a) 5 pulses (b) 10 pulses (c) 15 pulses

Figure 2.15. Various stages in the complete agglomeration of a 250 nm silicon film irradiated at 1.04 J/cm^2 = 1.22 × E_{CM}.

a surface-tension gradient. The result of this difference in surface-tension is a shear stress exerted on the surface of the film. This effect is the so-called Marangoni effect: silicon will start to flow from hot regions towards cold regions in the film. As surface tension decreases drastically with increasing temperature, it is expected that this effect becomes significant only for a certain temperature >> T_m. This correlates well with the fact that E_{SR} is at much higher energy than E_{CM}. In addition to this, temperature gradients and duration of the high temperature interval must also be sufficient for silicon flow to become significant.

Figure 2.11 (b) shows a typical temperature trace of the film during the laser crystallization. Also, the order of events in the theory we propose for agglomeration in a single-pulse ELC process is shown. During the temperature peak, lateral temperature gradients resulting from the beam non-uniformity have not yet disappeared due to heat flow. As the film is very hot, surface tension is low and silicon could start to flow as a result of the temperature gradients. For thinner films, the duration of the temperature peak is shorter and a higher threshold temperature for surface rippling is expected. Assuming the temperature of the film is proportional to the normalized energy density E/E_{CM}, this is indeed confirmed by the experimental data shown in Figure 2.14. The difference in wavelength observed as a function of film thickness can also be related to the film thickness: for thinner films, the lateral heat flow is less and as a result the shorter wavelength fluctuations in the lateral temperature profile will remain longer and will also induce mass flow.

In conclusion it can be said that the surface rippling is caused by the beam non-uniformity due to the homogenizer. Most likely it is the gradients in surface tension that causes the silicon to flow. The time scale at which the process takes place depends on the film thickness. As a result, the wavelength increases with film thickness and the threshold energy decreases with film thickness.

MULTIPLE-PULSE AGGLOMERATION

We observed that agglomeration also occurs in a multiple-pulse ELC process, even for energy densities below E_{SR} as is shown in Figure 2.15. Figure 2.16 shows the

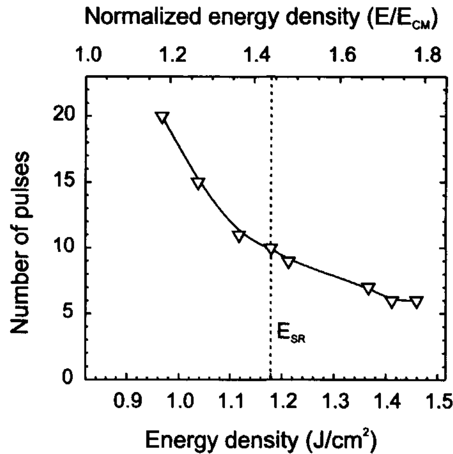


Figure 2.16. The threshold number of pulses for complete decomposition into beads as a function of energy density and relative energy density (E/E_{CM}) on the top x-axis.

number of pulses required for complete decomposition into beads versus the energy density. As can be seen, the number of pulses decreases for increasing energy density, and no influence of E_{SR} is observed. This indicates that the cause of surface rippling is not necessarily related to that in a single-pulse ELC process. From Figure 2.15 it can be seen that after a certain number of pulses the fluctuations become so severe, that the film melts only partially at positions where the film is thick as indicated by the SLG regions. This leads to the conclusion that agglomeration in a multiple-pulse process is mostly related to film thickness fluctuations that are created during lateral growth. The periodicity of ~15 μm observed in Figure 2.15 (b) shows that this process is also triggered by the non-uniformity of the laser beam.

2.2.5 Grain-Size Enlargement

In order to make single-crystalline TFTs, it is required that sufficient lateral growth takes place to create islands larger than the active-channel region. The research in this thesis is based on a single-pulse ELC process. As other important grain-location control methods are based on multiple-pulse ELC processes, grain-size enlargement with multiple pulses is also discussed.

SINGLE-PULSE GRAIN-SIZE ENLARGEMENT

In a single-pulse ELC process, the grain size can potentially be increased by postponing the onset of nucleation, that is, by increasing the lateral-growth interval Δt_{LG}. As the onset of nucleation is strongly temperature dependent, such a delay can be realized by reducing the cooling rate of the molten silicon. For a given configuration, this can for instance be achieved by substrate heating or by extension

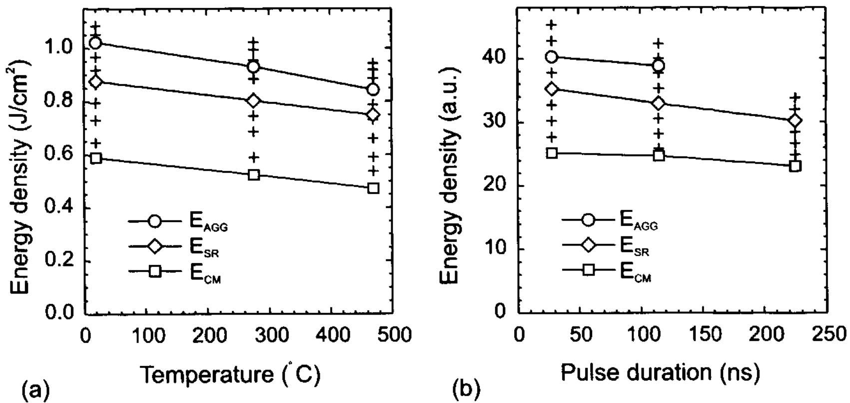


Figure 2.17. The various thresholds, E_{CM}, E_{SR}, and E_{AGG}, vs. substrate temperature (a) and pulse duration (b) for a 150 nm silicon film. The crosses show the energy densities at which the samples were irradiated. For most situations, the energy density is limited by the critical energy density for ablation. For a 225 ns pulse duration, however, the energy density was limited by the maximum output energy of the laser as total transmittance of the system was very low due to the pulse duration extender.

of the pulse duration [40]. Similarly, this can be achieved by simultaneously irradiating the sample from the front side and the back side [73]. In each of these cases, the vertical temperature gradient in the oxide at the time of solidification, and hence the cooling rate, is reduced.

Both substrate heating and pulse-duration extension will have an influence on the threshold energy densities encountered in a single-pulse ELC process. Figure 2.17 (a) shows the various threshold energy densities plotted versus the substrate temperature. Obviously, less energy is needed to reach any of these transitions when the substrate is preheated. Figure 2.17 (b) shows the various threshold energy densities as a function of the pulse duration. Based on intuition, the threshold energy densities are expected to increase with increasing pulse duration, as more heat is "lost" to the substrate at the onset of solidification. The results, however, seem to indicate that this was not the case and that E_{CM} even decreased for increasing pulse duration. It was found, however, that this is at least partially an artifact of the system set-up [74]: when the optical device to obtain pulse-duration extension was inserted in the system, part of the light was "clipped off" by the small mirrors and by improper alignment of the mirrors. Consequently, less light is clipped off in the remainder of the system and the transmittance of this part appears to be higher. The energy density at sample level, however, was assumed to be a set fraction of the energy density measured right before this part (Figure 3.3). As a result, the calculated energy density, and thus the experimentally obtained critical energy densities, are an underestimation of the real value.

MULTIPLE-PULSE GRAIN-SIZE ENLARGEMENT

A multiple-pulse ELC process allows for additional ways to increase the grain size. One way to increase grain size is to simply irradiate multiple pulses at an energy density close to E_{CM}. After the first pulse, a collection of grains is obtained with approximately random crystallographic distribution. During the consecutive pulses, however, grains with a certain preferential surface orientation grow at the expense of the other grains [75, 76]. At some point, only these grains remain, and further grain-size enlargement is stopped. A side effect of this grain-enlargement method is thus that the film also becomes textured, according to the reports with a {111} surface orientation.

The mechanism behind this process was suggested to be similar to that of secondary, or abnormal, grain growth observed in thermally annealed thin films [77]. In normal grain growth, the driving force is the reduction of the total energy of the system through minimization of the grain boundary area. The growth rate, however, drops significantly when grain sizes become equal to the film thickness. Secondary grain growth, on the other hand, is driven by a reduction in surface free energy and is mainly observed in very thin films. The surface free energy reaches a minimum for {111} oriented grains and therefore the films become {111} textured. Depending on the original distribution of the preferred grains, grain sizes far exceeding the film thickness can be obtained.

The grain enlargement in such a solid-state grain growth process is a very slow process. In multiple-pulse ELC processes, however, the growth rates of the preferential grains are much higher. This was thought to be related to the preferential melting of the grain boundaries during ELC at an energy density close to E_{CM} [78]. The grains become separated by a molten region and during regrowth they grow laterally into this region. During regrowth, the grain boundaries are reconstructed on a position that depends on the melting and growing behavior of the grains on either side. This behavior is in part determined by the surface and the interface free energy, both of which will of course depend on crystallographic orientation. This way, grains with a certain surface orientation will start to grow at the expense of other grains until they are all consumed.

An entirely different way of grain-size enlargement can be achieved when the beam can be patterned and when this patterned beam can be translated with respect to the sample. This concept is clarified with the example in Figure 2.18 and has been termed sequential lateral solidification (SLS) [79]. In the first pulse, a small strip of silicon is completely molten and as a result, lateral growth will start from the edges of the molten region. Given that the width of the molten region is not too large, the two growth fronts will collide in the center and the microstructure shown in Figure 2.18 (b) is obtained. Subsequently, the sample is translated with respect to the patterned beam over a distance less than the lateral growth distance. At this point, a

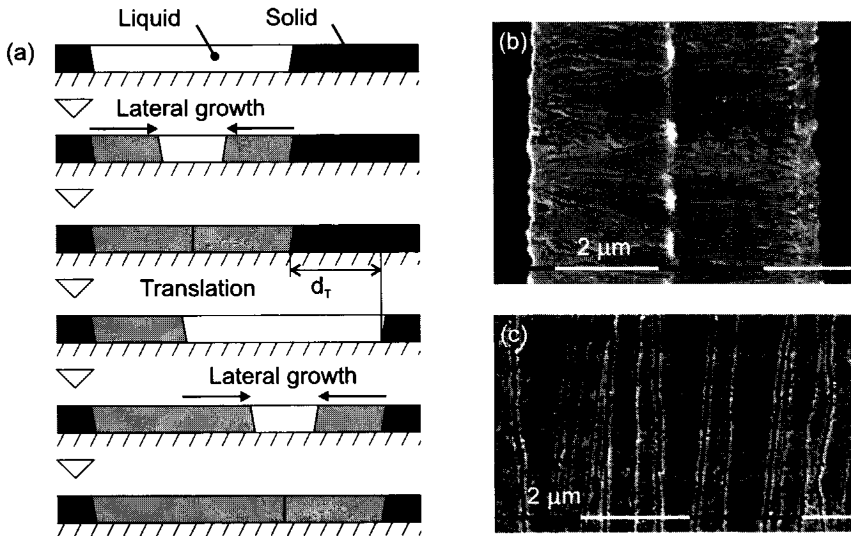


Figure 2.18. (a): Schematic drawing of the sequential lateral solidification process, (b) a typical microstructure after one pulse, and (c) the microstructure after n overlapping pulses (100 nm Si).

second laser pulse is irradiated and again lateral growth will start from the edges. As on one side the edge consists of laterally grown grains from the previous pulse, these will get extended. When this process is repeated several times, very long grains can be grown. An example of such "directional" poly-Si is shown in Figure 2.18 (c). The SLS process will be further discussed in Section 7.1.1.

2.3. Controlled Super-Lateral Growth

Because pulsed-laser-induced SLG shows a low intragrain defect density and is compatible with low-temperature substrates, it is an attractive method for creating large-grain poly-Si films for TFTs. As was mentioned before, however, device uniformity is at stake with these films as only few randomly positioned grain boundaries are present in the active channel region (Section 1.1.4). Another problem that was mentioned is the energy-density process window, which for SLG is very small as it occurs only on the transition from the incomplete to the near-complete melting regime (Section 2.2.2).

Many researchers, however, have shown tremendous creativity in developing methods to obtain SLG for a large range of energy densities. These methods have collectively been termed controlled SLG (C-SLG) [80] and are aimed at controlling the seeds for lateral growth over a long range of energy densities. When in addition to this, single-crystalline TFTs are required; the lateral growth should exceed a

certain value. Depending on channel dimensions this might imply that the lateral growth should be extended beyond that obtained in the SLG regime. An overview of the various C-SLG methods can be found for instance in [81]. From the equipment point of view, these can roughly be divided into two groups: optics-based and lithography-based C-SLG.

In the first group, C-SLG is obtained by modulation of the incident laser light. No lithographic steps are added to the process; however, more complex laser irradiation systems are required (e.g. capable of projection and focusing). The alignment is another issue in these methods: when attempting to make c-Si TFTs, the modulated light pattern should be aligned to the subsequent lithographic steps. The SLS process described in 2.2.5 is an example of an optics-base C-SLG method. In the second group, lithographically-made structures ensure the presence of a seed for a large range of energy densities. Lithography is both the advantage and the disadvantage of this category of methods: the location of the seeds is controlled as accurately as any feature in lithography, but the addition of lithographic steps will add to the cost of the process. Also, a combination of lithography and optical modulation can be used to obtain C-SLG [e.g.: 82].

Lithography-based methods generally rely on locally changing the conditions at which complete melt occurs, in other words by locally varying E_{CM}. This can for instance be accomplished by varying the amount of incident light coupled into the film by applying reflective or anti-reflective coatings [83]. In addition to changing reflectivity, these capping layers will also act as a heat sink for the heat absorbed in the film. In this work, however, we are concerned with the two remaining options to locally vary E_{CM}: variation of the insulator thickness, or variation of the silicon film thickness.

The effect of the insulator film thickness on the various threshold energy densities is shown in Figure 2.19 (a). When the SiO_2 thickness is in the order of or less than the diffusion length of the heat, the heat extraction rate is increased. As a result, more energy is needed to reach complete melt of the film. This concept was utilized in making heat sinks underlying the silicon film. When the film is irradiated, the conditions will locally be modified by the heat sink and through this, C-SLG can be obtained. When conditions are optimal, grain-location control can be obtained. Results of this method are presented in Chapter 4.

The effect of the silicon film thickness on the various threshold energy densities is shown in Figure 2.19 (b). All energy densities scale almost linearly with the film thickness. This concept was utilized in making embedded seeds for C-SKG. The results of this method are described in Chapter 5. It was found that through the additional effect of grain filtering, this method was successful in obtaining grain-location control for a large range of energy densities.

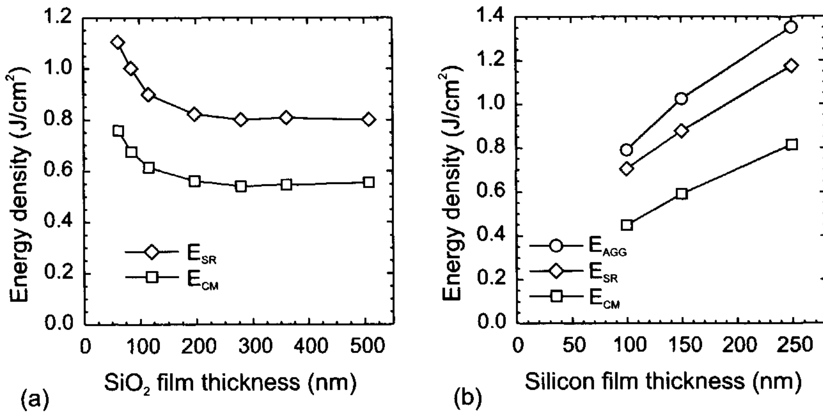


Figure 2.19. The various threshold energy densities, E_{CM}, E_{SR}, and E_{AGG}, as a function (a) of SiO_2 thickness and (b) silicon film thickness.

CHAPTER 3

Experimental, Analysis, and Heat-Flow Simulations

Based on the lithography-based methods of controlled super-lateral growth (C-SLG) described in Section 0, two different concepts for grain-location control were developed. In this chapter, the manufacturing of these structures is discussed, as well as the manufacturing of thin-film transistors. Subsequently, a description of the analysis tools and the heat-flow simulations is given.

3.1. Experimental

Laser crystallization was performed both at Delft University of Technology and at Columbia University. All other experimental procedures were performed at the cleanroom facilities of the Delft Institute of Microelectronics and Submicrontechnology (DIMES).

3.1.1 Laser Setups

Two excimer-laser setups have been used, the "XMR system" at Delft University of Technology and the "Microlas system" at Columbia University in New York City.

XMR SYSTEM

A schematic drawing of the XMR 7100 system is shown in Figure 3.1. The XMR 5100 laser is filled with a mixture of Xe and Cl_2 as active gases, and Ne as a buffer gas. 308 nm light is emitted from the transition into the ground state of the 'excited dimer' (abbreviated to excimer) XeCl and emits a 56 ns full width at half maximum (FWHM) pulse with a wavelength of 308 nm. The temporal profile of the pulse is shown in Figure 3.2 (a). The laser output energy can be measured by a removable energy meter (Gentec ED-500) placed immediately at the output of the laser. A wide

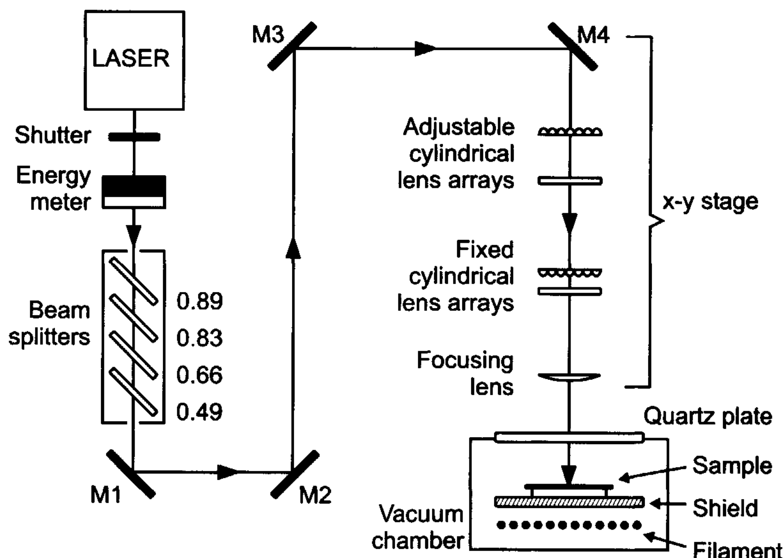


Figure 3.1. Schematic drawing of the XMR system in Delft.

range of energy densities can be achieved by inserting one or more out of four beam splitters with a set transmittance value. To obtain a uniform spatial profile, the pulse is directed through two sets of cylindrical lens arrays: the homogenizer. By changing the position of the two upper lenses, the spot size (maximum) can be varied to accurately control the energy density at sample level. Typical spot size values that were used in this work range from ~0.3x0.5 cm^2 to 1x1 cm^2. Finally the pulse is projected on the sample with a focusing lens.

The sample is held under high vacuum (~10^{-7} Torr) and can be preheated up to 470°C by a tungsten filament separated from the sample by a radiation shield. The wafers are placed inside the process chamber by a robot arm. In a typical cycle, the wafer is taken from the load lock and placed inside an alignment chamber, where the wafer is aligned to the flat before it is placed in the process chamber. After processing, the wafer is allowed to cool down in a chilling chamber before it is returned to the load lock.

In the experiments the approximate pulse energy at sample level was determined by multiplying the measured laser output energy with the transmittance value of the system (~0.78 × the total transmittance of the beam splitters). The actual energy density was determined by dividing this value by the spot size.

MICROLAS SYSTEM

A schematic representation of this system is shown in Figure 3.3. The Lambda LPX 300 laser emits a 28 ns FWHM pulse, of which the temporal profile is shown in

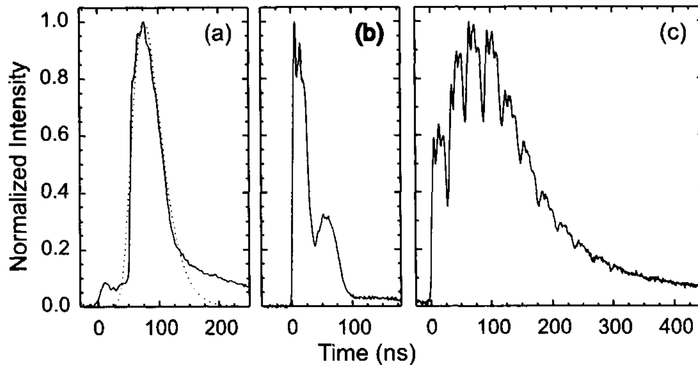


Figure 3.2. Temporal profiles of (a) the XMR laser and (b) the LPX laser. (c) shows the pulse after the pulse duration extender with 6 stages. The dotted line in (a) is the lognormal fit to the XMR pulse used in simulations.

Figure 3.2 (b). As an option, the pulse is directed through a pulse duration extender (PDE) from Exitec. This device consists of up to eight stages, each consisting of two opposing mirrors. Halfway each stage, a semi-transparent mirror reflects part of the pulse back into the system. A train of slightly overlapping pulses results, where the composite pulse duration depends on the number of stages installed in the PDE. As an example the pulse from four stages is shown in Figure 3.2 (c).

Pulse energy can be varied continuously from ~5 to ~95 % of the input value by an attenuator, which consists of a coated quartz plate of which the transmission is a strong function of the angle of incidence of the pulse. The pulse energy can thus be modified by rotating the coated quartz plate. A second non-coated quartz plate is rotated as well to compensate for the beam shift caused by the first plate. The pulse energy is measured from the reflected light of a high transmittance beam splitter. After the homogenizer, the beam is directed through a mask mounted on an x-y stage. The thus obtained pattern is demagnified by 5 and projected on the sample that lies on an x-y-z precision stage.

This system is designed for sequential lateral solidification (SLS; Section 2.2.5), which is an important optics-based C-SLG method. Due to the large amount of optical components in this system, the exact laser energy density on sample level was not determined, as the total transmittance of the system was seen to be unstable over time. Therefore, energy densities were expressed relative to E_{CM}, which was determined separately for each experiment.

3.1.2 Layers and Patterning

For manufacturing the lithography-based C-SLG structures and the TFTs, various deposition processes were used. A short description is given of the processes and of

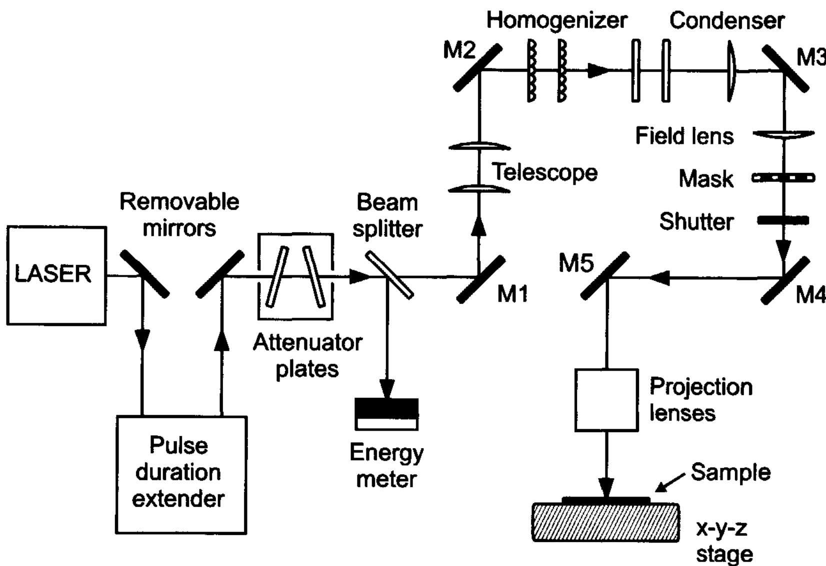


Figure 3.3. Schematic drawing of the Microlas system at Columbia University.

the lithography and etch processes to pattern these layers. All structures were made on oxidized c-Si wafers for easier processing, although the process is developed to be fully compatible with glass substrates. The main reason for this is the better compatibility with the equipment used to make the various structures. For instance, the detection sensors of many machines require opaque substrates so that transparent substrates are not recognized.

LAYERS

The SiO_2 layers used to make the C-SLG structures were either deposited or grown. Deposition was performed by plasma-enhanced chemical-vapor deposition (PECVD) in a Novellus Concept One using either silane (SiH_4) and O_2 mixture or tetraethylorthosilicate ($Si\{OCH_2CH_3\}_4$ also abbreviated as TEOS) at 400°C or 350°C, respectively. Thermal oxidation was performed in an H_2–O_2 ambient at 1100°C. Obviously, this process is not compatible with glass substrates, however, it was used for ease of processing and ease of analysis of the C-SLG structures. Thickness of the various SiO_2 layers was determined by reflectometry. Amorphous silicon (a-Si) films were deposited by LPCVD at 545°C with SiH_4 as a source of silicon [84]. Thickness of these layers was measured with ellipsometry.

For manufacturing the TFTs, various layers were used. Low-temperature gate oxide was deposited by LPCVD at 425°C with SiH_4 and O_2 gases. For most TFTs, however, gate oxide was thermally grown in an O_2 ambient at 950°C for better

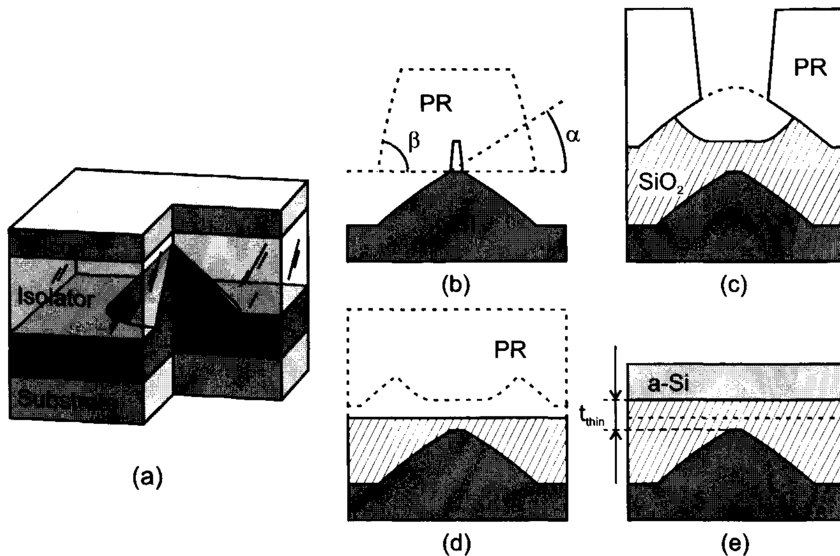


Figure 3.4. Schematic drawings of the heat-sink structure: (a), a 3D cross section of this structure implemented on an arbitrary substrate. (b)-(e), The process flow of heat-sink fabrication in silicon using the 2-step planarization method (dotted lines show the structure prior to each particular step): (b), cone etching with; (c), crude planarization; (d), fine planarization; (e), SiO_2 and Si deposition.

performance and better uniformity. Also, TEOS PECVD SiO_2 layers were deposited for insulation and Al layers were sputtered at room temperature for contacting.

PATTERNING

Lithography was performed with an I-line ASML PAS 5000/50 wafer stepper. The spun-on Shipley SPR 3012 photoresist layers were exposed and developed to define the area to be etched away. In addition to occasional wet etching, three different plasma etchers were used:

- A Drytek 384T triode etcher with, among others, CF_4, CHF_3, C_2F_6, O_2 gases for etching SiO_2, Si, and PR layers.
- A low-power Alcatel GIR300 parallel-plate etcher with, among others, CF_4, CHF_3, and He gases for etching SiO_2.
- A Trikon Omega 201 electron cyclotron resonance (ECR) etcher with, among others, HBr and Cl_2 gases for etching Al.

3.1.3 Manufacturing of Heat Sinks

The heat-sink structure is aimed to achieve grain-location control by modifying the local E_{CM} by means of a variation in the insulator thickness (Figure 2.19 (a)). The structure is shown in Figure 3.4 (a); it consists of a cone formed in a heat-conducting layer covered with an insulating material (see Section 4.1 for a discussion about the mechanism). The surface of the insulator is planar and, as a result, the central area has an insulator thickness less than that of the surroundings. The thickness of the thinnest part of the insulator (t_{thin}) and the angle α of the cone are important parameters as they determine the heat extraction rate. Rather than depositing and patterning a heat-conductive layer, the cones were made directly in the silicon substrate, which is a good heat conductor itself.

CONE ETCHING

Cones were made with a technique previously proposed to make field emitters [85], which are for example used in a certain type of flat-panel display: field-emission displays (FED). In this process, schematically depicted in Figure 3.4 (b)-(e), cones are etched in silicon with a mask-erosion technique: both the silicon and the masking layer are etched in the plasma. As masking layer a layer of photoresist (PR) was spun on. Because the PR pattern has (slightly) tapered edges, it will also be etched horizontally and as a result its footprint will shrink. The thus exposed area of the silicon will be etched shorter and tapered edges are created. When the PR pattern consists of a dot that is completely etched away during the process, a silicon cone remains. Overetching is to be avoided, as this reduces the sharpness and height of the cone. Therefore, etching is stopped before the entire masking layer is removed, so that the cone has a slightly flattened top (Figure 3.4 (b)) with a very small remnant of PR that is reduced with an O_2 plasma.

The angle of the silicon cone (α in Figure 3.4 (b)) is determined by the ratio of the horizontal etch rate of the PR and the vertical etch rate of the silicon. This ratio can be influenced both by adjusting the angle of the tapered edges (β in Figure 3.4 (b)) of the PR dot as well as by tuning the etch rates during plasma etching. β can be decreased by off-focus exposure during lithographic patterning of the PR. The angle as a function of the degree of off-focus exposure is shown in Figure 3.5. If the deviation of ideal focus becomes too large, β also becomes dependent on the dot size and this can introduce non-uniformity. Therefore, an underfocus of "just" 1 μm was chosen for further processing.

The etch rates of silicon and PR were tuned in such a way that a certain angle α was achieved. Samples were etched in a $CF_4 - O_2$ mixture in the Drytek etcher and the (horizontal) etch rate of the PR was modified by varying the O_2 content of the mixture. Figure 3.6 (a) shows a cone immediately after etching; the remnant of the PR can still be seen on the top of the cone.

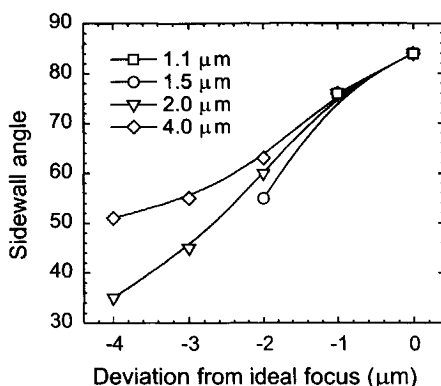


Figure 3.5. The side-wall angle of a PR dot as a function of the deviation from ideal focus and of dot diameter.

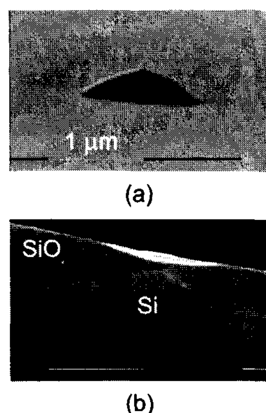


Figure 3.6. SEM images of (a) a silicon cone, and (b), an oxide-covered cone with planarized surface.

ONE-STEP SURFACE PLANARIZATION

A PECVD SiO_2 layer was deposited on top of the cones to act as an insulation layer between the cone and the silicon film. The protruding SiO_2 needs to be removed. To this end, a layer of PR was spun on. As any kind of surface topography was drastically smoothed during the spinning, its surface would be planar [86]. To further enhance planarity, the PR layer was flood irradiated with UV light and given a thermal reflow. Subsequently, this planar surface was transferred to that of the SiO_2 by simultaneously etching, provided that the etch rates of the PR and the oxide were equal. Etching was performed in a C_2F_6 – CHF_3 – O_2 mixture in the Drytek etcher and equal etch rates could be achieved by adjusting the CHF_3/O_2 ratio [87]. For increasing ratio, the SiO_2 etch rate increases slightly whereas the PR etch rate decreases rapidly. It was found that a flow of 18 sccm, 130 sccm, and 32 sccm, for C_2F_6, CHF_3, and O_2, respectively, gave the desired results: etch rates of a PR-covered wafer and an oxide-covered wafer were equal.

TWO-STEP SURFACE PLANARIZATION

It was found, however, that locally etch rates differed markedly at those positions where PR and the SiO_2 were etched simultaneously. This micro-loading effect is presumably caused by a local increase of the oxygen content in the plasma due to the release of oxygen from the SiO_2 as it gets etched. The effect is that small-scale non-planarities are introduced to the surface exactly at those positions where the protrusions were.

To reduce the effects of the micro-loading, the final planarization was preceded by a crude planarization step during which most of the protruding oxide was removed.

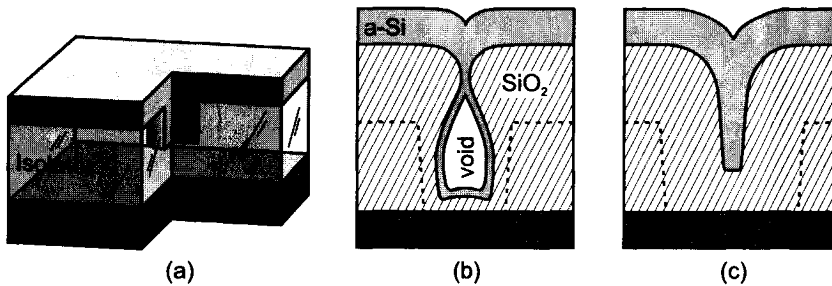


Figure 3.7. Schematic drawings of (a), the concept of the embedded seed structure, (b) and (c), the cavities as they were obtained after SiH_4-based PECVD and TEOS-based PECVD of SiO_2, respectively.

The crude planarization is shown in Figure 3.4 (c): a PR layer was spun on and patterned with the negative image of the one used to define the cones. A relatively short exposure time was used during the lithographic patterning so that only the top of the oxide protrusions was uncovered during the development of the PR layer. During the subsequent wet etching in HF, the protrusions were isotropically etched away and small ridges remained where the base of the protrusions used to be. Then, shown in Figure 3.4 (d), the previously described planarization procedure was performed and a reasonably planar surface was obtained. Figure 3.6 (b) shows a SEM cross-section: the surface is still not completely planarized, however, it is smooth. A thin SiO_2 layer was deposited to get a certain designed value for t_{thin} and subsequently a ~150 nm thick a-Si film was deposited (Figure 3.4 (e)). Samples were irradiated with the XMR laser at room temperature and with energies around and above E_{CM} ($\approx$0.62 J/cm^2).

3.1.4 Manufacturing of Embedded-Seed Structures

These structures are aimed at achieving grain-location control by variation of film thickness (Figure 2.19 (b)). One such structure is shown in Figure 3.7 (a): when the thin part is completely molten, seeds for lateral growth may still be present in the thick part of the film (see Section 5.1 for a discussion about the mechanism). This structure can be made by filling and covering a small indentation (or a cavity) in the insulating layer with a-Si. As the diameter of the column has to be in the order of 100 nm, the cavity could not be made in a single lithographic step. Therefore, a two-step procedure was developed in which large-diameter holes (~1.0 μm) etched in an inslulating layer were made narrower by depositing a second insulating layer. A side effect of this method is that the rim of the cavity is no longer sharp, but rounded. Depending on the deposition method, two shapes of cavities were obtained: (1) bottle-shaped cavities (Figure 3.7 (b)): a cavity with inward sloped walls of which only the diameter of the opening is very small and (2) U-shaped cavities (Figure 3.7

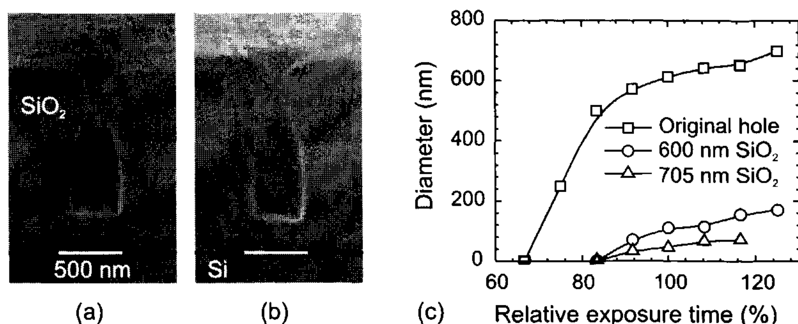


Figure 3.8. (a) and (b): SEM images of two cavities with relative exposure time of ~108% and with 600 nm and 705 nm thick second SiO_2 deposition, respectively. (c): the diameter of the original holes and the neck of the cavity as measured from the SEM images.

(c)): a cavity with almost straight walls that has a somewhat larger diameter that is close to constant over the depth of the cavity. These cavities are then covered and filled with a-Si. Obviously, if the walls of the cavity are inward sloped, a void remained in the cavity (Figure 3.7 (b)). For reasons explained in Chapter 5, the second structure will be referred to as a 'grain filter'.

The diameters of these cavities were varied in large steps by varying the size of the openings in the mask used during the lithographic patterning of the first SiO_2 layer from 0.6 to 1.4 μm in steps of 0.2 μm. Additionally, a small variation around the designed value was obtained by varying the exposure time of the PR during the lithographic patterning of the first SiO_2 layer. Time was varied from 79% to 121% of the optimized value. By this method, the diameter could be changed in steps of ~20 nm.

BOTTLE-SHAPED CAVITIES

For the bottle-shaped cavities a ~800 nm thick SiH_4-based PECVD SiO_2 layer was patterned into a grids of ~0.6 μm holes by etching in a CHF_3 – C_2F_4 plasma. The second SiO_2 layer was deposited by SiH_4-based PECVD. The step coverage of this deposition was very poor and as a result 'shouldering' occurs, meaning that the edges of the hole grew faster horizontally than the walls. Apparently, the mobility of radicals from the plasma over the surface is very low and local deposition rate is determined by the arrival rate of radicals [88]. The SEM images in Figure 3.8 (a) and (b) show examples of bottle-shaped cavities. The minimal diameter (i.e., at the neck of the bottle), was measured from these images. The neck diameter, d_{neck}, is shown as a function of total exposure energy during lithographic patterning of the first SiO_2 layer in Figure 3.8 (c).

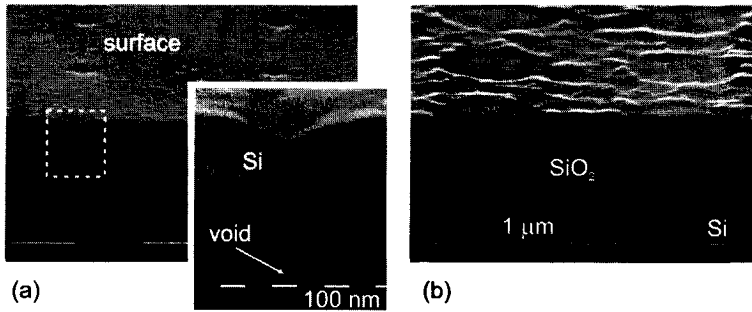


Figure 3.9. Cross-sectional SEM images taken in bird's-eye view to also show the surface of embedded seed structures (a) before and (b) after ELC.

The second oxide deposition is followed by a-Si deposition and ELC. Figure 3.9 shows cross sectional SEM images taken in bird's-eye view, both before and after irradiation. Two things can be observed: (1), the cavities are not filled completely as the neck is closed before the entire cavity can be filled and (2), the indentation at the surface of the silicon disappears during ELC, presumably by surface-tension-driven reflow. As a result of the incomplete filling, a void remained inside the cavity. The top of the void was seen to lie deeper for increasing neck diameter or, in other words, the height of the silicon column increased for increasing neck diameter. This seemingly negligible effect does have important implications, as during the subsequent laser annealing the silicon could agglomerate when the melt reaches the void. As will be discussed in Section 5.2 it was indeed found that beyond a certain energy density, no lateral growth was observed. This seems to indicate that the molten film was no longer in contact with the solid due to agglomeration.

U-SHAPED CAVITIES; TWO-STEP PROCESS

These structures were developed partially in order to avoid the problems related to the presence of the void. As will be become clear from the discussion in Section 5.1, the ideal cavity is deep, narrow, and has straight walls. In order to obtain such cavities, three parameters were adjusted: (1), the thickness of the first SiO_2 layer (i.e., the depth of the original hole), (2), the diameter of the original hole, and (3), the thickness of the second SiO_2 layer.

A 515 nm or a 755 nm thick thermally grown SiO_2 layer was patterned into grids of ~0.8, ~1.0, ~1.2, and ~1.4 μm holes. In addition to that, a smaller variation of diameter was sometimes obtained by the variation of the exposure time during lithographic patterning. The second SiO_2 deposition was performed with TEOS-based PECVD with variable thickness. This deposition had a rather conformal step coverage due to high surface mobility of the radicals from the plasma and as a result no shouldering occurred. The ratio between the horizontal and vertical deposition

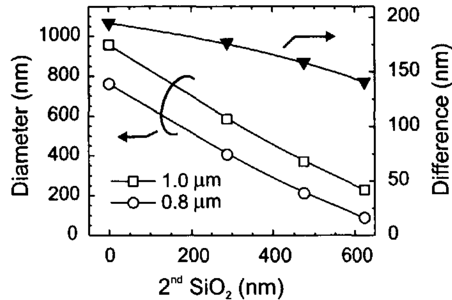


Figure 3.10. Cavity diameter as a function of second oxide thickness and the difference between diameter of an originally 0.8 μm hole and a 1.0 μm hole.

rates decreased from an initial value of ~0.7 to less than 0.4 at the end of the deposition. Because of this, any absolute non-uniformity in the diameter of the original holes became less during the deposition, which enhances the reproducibility of the cavities. An example of this effect is found in Figure 3.10: both the diameter of an originally 0.8 μm and of an originally 1.0 μm wide hole are shown as a function of thickness of the deposited SiO_2. The difference in diameter is plotted on the secondary y-axis and it can be seen that the difference decreases with more than 25%.

The SEM images in Figures 3.11 and 3.12 show cross sections of cavities obtained for a 515 nm and a 755 nm thick first SiO_2 layer, respectively. For the former it was found that the best combination was a 0.8 μm wide hole with a 705 nm thick second SiO_2 deposition. The 1.0 μm wide holes still had outwardly sloped walls after deposition so that cavities were essentially V-shaped. For the latter thickness it was found that the best combination was a 1.0 μm wide hole with a 925 nm thick second SiO_2 deposition. The walls of the cavities made with 0.8 μm wide holes become inwardly sloped and for a 925 nm second SiO_2 deposition, this results in closure of the cavity. From these results, it can be concluded that, in order to get deep, narrow and straight cavities for a given hole depth, there is only one combination of hole diameter and second SiO_2 thickness that results in the ideally shaped cavity.

Nevertheless, the hole diameter was varied without changing the other two parameters in order to investigate the effect of cavity diameter on the crystal growth. Figure 3.13 shows cross-sections of cavities after a-Si deposition resulting from four different original hole diameters after a 100 nm a-Si deposition. As expected, the walls were only straight for a small range of diameters (overexposed 1.0 μm holes and underexposed 1.2 μm holes) around the optimized diameter. As a result, the smaller cavities had voids inside and the larger cavities were V-shaped and had a deeper indentation at the surface. For thicker a-Si films, the indentation is of course

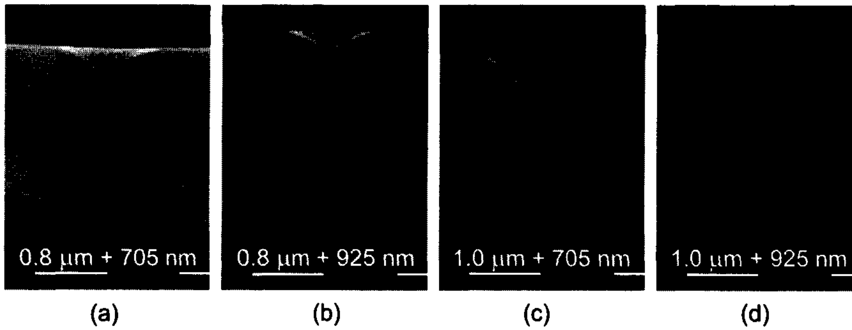


Figure 3.11. SEM images showing cross sections of some cavities made with various combinations of hole diameter and second SiO_2 thickness in a 515 nm thick first SiO_2 layer.

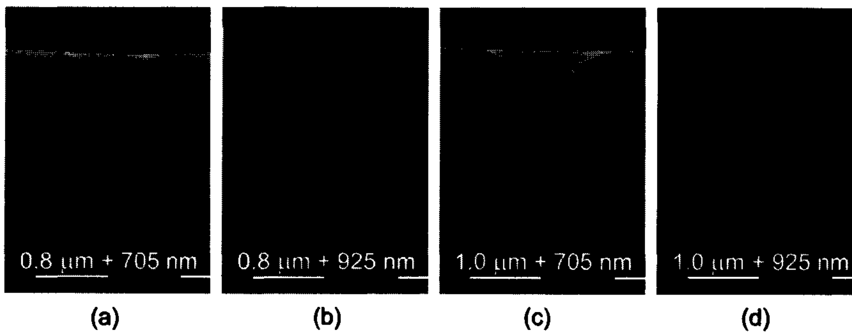


Figure 3.12. SEM images showing cross sections of some cavities made with various combinations of hole diameter and second SiO_2 thickness in a 755 nm thick first SiO_2 layer.

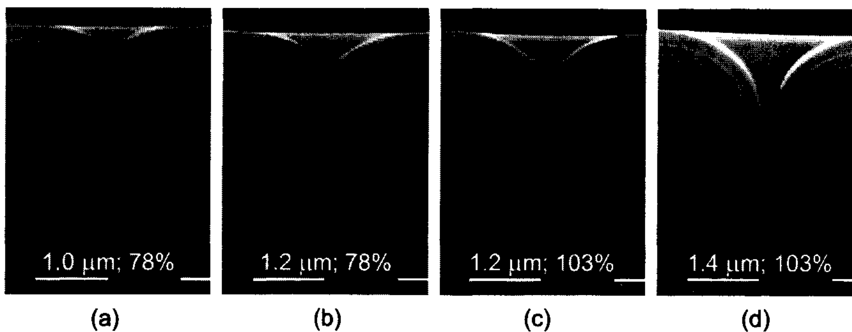


Figure 3.13. Four SEM images showing cross sections of cavities with increasing diameter after 100 nm a-Si deposition. The original hole diameter and the relative exposure time during lithography are given separately in each image. Note that (b)-(d) have had a HF-dip to enhance the contrast between Si, PECVD SiO_2, and thermal SiO_2.

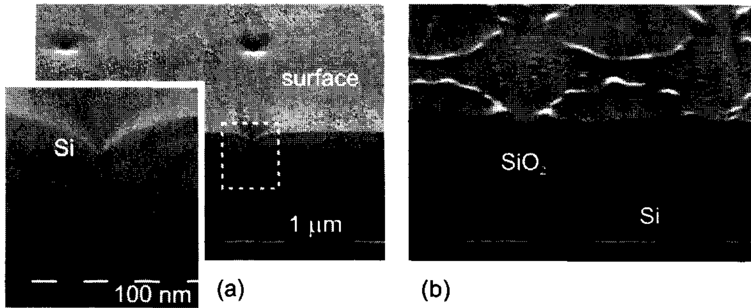


Figure 3.14. Cross-sectional SEM images taken in bird's-eye view to also show the surface of the grain-filter structures (a) before and (b) after ELC.

expected to be shallower. A further observation that can be made from these images is that the depth of the cavity decreases with increasing original hole diameter.

Figure 3.14 shows a bird's-eye view of a grain filter before and after irradiation. As can be seen the indentation disappeared by the surface-tension-driven reflow of the molten silicon. The lateral growth is marked by the formation of a ridge and the interior of the island has a smooth surface. When the active region of the TFT is made within the island, the surface interface of the device is planar.

U-SHAPED CAVITIES; THREE-STEP PROCESS

It is inherent to the two-step process that the rims of the cavities are rounded. For some samples, a third step was added to the process (shown schematically in Figure 3.15) in which these rounded edges were sharpened by either one of two different planarization procedures. In the first method the sharpening was performed by chemical-mechanical polishing (CMP) equipment using Cabot Semi-Sperce slurry and a Suba IV polishing cloth. Prior to this planarization procedure, a sacrificial a-Si layer was deposited to already fill the cavities and to avoid abrasive particles from clogging up the cavities. Following an ultrasonic cleaning procedure to remove abrasive particles from the surface, the wafers were again covered with a-Si. To ensure good contact between the a-Si film and the a-Si filling of the cavity, the samples were given a short dip etch in 0.55% HF prior to deposition to remove any SiO_2 formed on the silicon by exposure to air (native SiO_2). Figure 3.16 shows a cross section of one of the resultant structures. In the IC fabrication, CMP has become a rather standard procedure when multiple layers of interconnect are applied to an IC. Therefore, in a 3D-electronics application, CMP can be used to sharpen the rim of the cavities.

CMP is, however, not compatible with large-area electronics. Therefore an alternative planarization procedure based on plasma etching was developed. The method employs the surface-tension-driven planarizing during a laser pulse to create

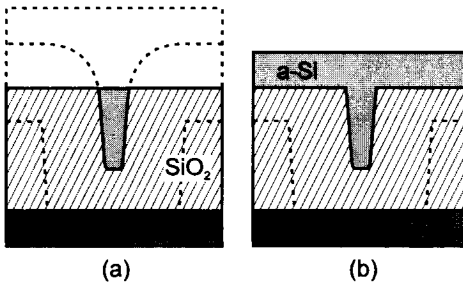


Figure 3.15. Schematic drawings of the planarization process: (a) removal of the sacrificial a-Si layer and the rim (shown with dotted lines), followed by (b) a-Si deposition.

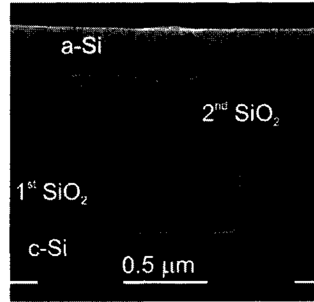


Figure 3.16. SEM cross section of CMP planarized grain filter

a planar surface, as was shown in 3.14. During a plasma etch with equal etch rates for Si and SiO_2, this surface is transferred down and sharp corners are created. The laser and plasma planarization (LPP) sequence is followed by deposition of a second a-Si layer. To ensure good contact between film and the silicon in the cavity, the native oxide was removed prior to deposition.

The laser planarization was done by irradiating the samples with an energy density >> E_{CM}. Subsequently, one or more low-energy pulses were used to planarize the ridges and hillocks resulting from the lateral growth caused by the first pulse. During these, the film is only partially melted and as a result reflow is vertical and roughness decreases. Figure 3.17 show AFM scans and traces for different energy densities of the first pulse followed by a single low energy density pulse at ~88% of E_{CM}. As can be seen, the indentation does not completely disappear at low energy density, whereas at high energy density the ridges and hillocks between the islands are not sufficiently planarized by the second pulse. The ridges and hillocks are especially large at positions where four islands collide and even with multiple pulses, it was found that these did not disappear.

The plasma planarization was performed with a CF_4-based plasma in the Drytek etcher. The etch rates of the silicon and the SiO_2 were tuned by addition of either CHF_3 or O_2 [89]. The F-content of the plasma is either increased or decreased by addition of oxygen or hydrogen, respectively. The silicon etch rate increases with the F-content, whereas the SiO_2 etch rate remains almost the same. It was found that for a mixture of 70 sccm CF_4 and 5 sccm O_2, the global etch rates of silicon and SiO_2 were the same. At those positions where both Si and SiO_2 were etched simultaneously, however, the etch rate of silicon was increased, presumably by the local increase of the oxygen content of the plasma. It was found that local etch rates *were* similar when etched in a mixture of 70 sccm CF_4 and 10 sccm CHF_3. Figure 3.18 shows cross sections of the resultant structure after Si deposition for both

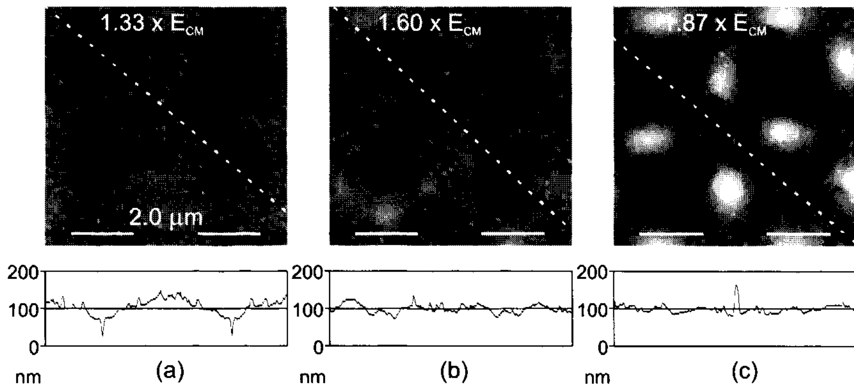


Figure 3.17. AFM scans and traces of a matrix of four grain-filters (original hole diameter = 1.2 μm) irradiated with varying energy densities followed with a pulse at ~0.88 × E_{CM}. The trace is taken diagonally over two of the grain filters.

etching conditions. Even though overall planarity is not as good as with CMP, sharp corners were indeed obtained with the CF_4 – CHF_3 plasma, and this mixture was chosen for further LPP steps.

3.1.5 Manufacturing of Thin-Film Transistors

Of the various structures for grain-location control that were made: heat sinks, bottle-shaped cavities and grain filters (GFs), only the last were used in a TFT process. Top-gate n-channel TFTs were made in GF poly-Si films with a process described in detail elsewhere [90]. Parallel to this, TFTs were made in small-grain ELC poly-Si films and in directionally solidified poly-Si films. The latter films were obtained by a simplified version of the sequential lateral solidification (SLS) process: line-scan SLS (LS-SLS), also referred to as 1D-SLS [91]. As was shown in Figure 2.18 (b), this optics-based C-SLG method leads to long and parallel grains or, in other words, to directional poly-Si. A further discussion of SLS can be found in Section 7.1.1. Poly-Si films were obtained either by partial melt crystallization (PMC), that is, irradiated below E_{CM}, or by complete melt crystallization (CMC). This led to large-grain and small-grain poly-Si, respectively.

As was mentioned before (Section 1.1.2) the heterogeneity of poly-Si is expected to contribute to the non-uniformity of the devices. In order to be able to distinguish between non-uniformity caused by the channel microstructure and that caused by any other source, TFTs were also made in 'ideal' silicon-on-insulator (SOI) films obtained by the 'separation by implantation of oxygen' (SIMOX) method. The conditions for each wafer are summarized in Table 3.1. The main characteristics of the process were:

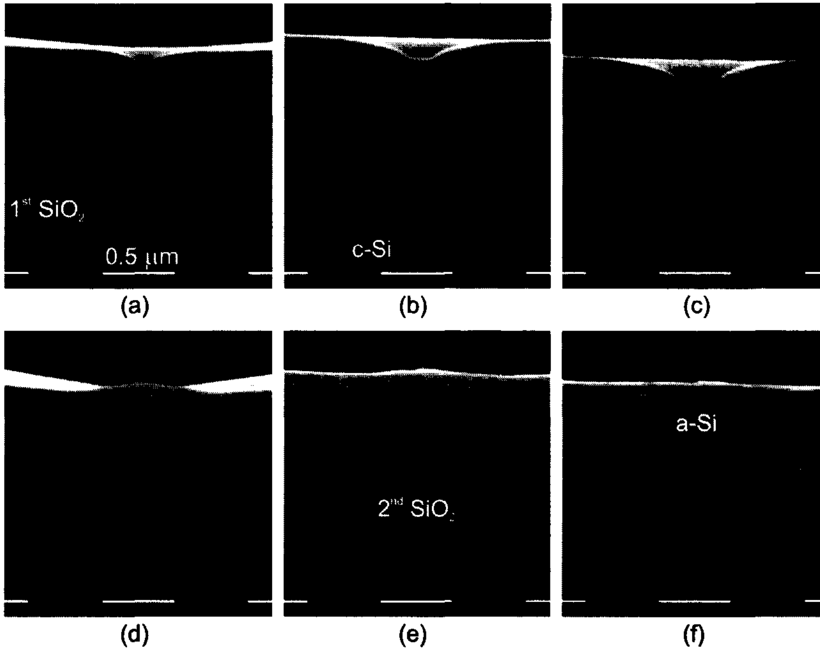


Figure 3.18. SEM cross sections showing grain-filters planarized (a-c) with a 70/5 sccm CF_4/O_2 mixture and (d-f) with a 70/10 sccm CF_4/CHF_3 mixture, respectively. Original hole diameters were 1.0, 1.2, and 1.4 μm from left to right.

- The silicon films were lightly doped with boron to a concentration of 10^{16} ions/cm^3 prior to ELC. The dopants were activated during the solidification after the laser melting.
- The silicon layer of the SIMOX wafers was thinned by thermal oxidation and subsequent wet etching in HF solution. The same implantation was given as for the laser-crystallized wafers, but activation was performed thermally at 1000°C for 30 minutes.
- In the low-temperature process described in [90], a ~155 nm thick gate oxide was deposited by LPCVD of SiO_2 at 350°C with SiH_4 and O_2 as source gases. The quality and uniformity of this oxide are very poor, however, and this will have repercussions on the TFT performance and uniformity. Since in this research the main interest is in film properties rather than device properties, a thermally grown gate dielectric was used. Samples were oxidized for 65 minutes in an O_2 ambient at 950°C and resultant SiO_2 thickness was 34 nm. It is known that at this temperature the crystal quality is improved, whereas the grain boundaries remain on the same location [92]. To compare the results with those of a low-temperature process, two wafers, of which one was annealed at 950°C, were given the low temperature oxide.

Table 3.1. Overview of the various process conditions in the TFT manufacturing. Sets 2 and 3 were manufactured on the same wafer, only different dies.

#	Process	Film thickness	Crystallization conditions (E/E_{CM}, T, pulse duration)	Gate dielectric	S/D activation energy
1	2 step GF-TFTs	100 nm	1.64, RT, ~190 ns	34 nm th. SiO_2	0.30 J/cm^2
2a		150 nm	1.38, RT, ~155 ns	34 nm th. SiO_2	0.38 J/cm^2
2b			1.58, RT, ~155 ns		
3		150 nm	1.89, 470°C, 56 ns	34 nm th. SiO_2	0.38 J/cm^2
4a		250 nm	1.42, 470°C, 56 ns	34 nm th. SiO_2	0.30 J/cm^2
4b			1.72, 470°C, 56 ns		
5a		150 nm	1.75, 470°C, 56 ns	155 nm LPCVD SiO_2	0.43 J/cm^2
5b			1.90, 470°C, 56 ns		
6a	2 step GF-TFTs (high T)	150 nm	1.75, 470°C, 56 ns	155 nm LPCVD SiO_2	0.43 J/cm^2
6b			1.90, 470°C, 56 ns		
7a	3 step (LPP) GF-TFTs	250 nm	1.43, 470°C, 56 ns	34 nm th. SiO_2	0.56 J/cm^2
7b			1.75, 470°C, 56 ns		
8a	PMC-TFTs	150 nm	0.93, 470°C, 56 ns	34 nm th. SiO_2	0.38 J/cm^2
8b	CMC-TFTs		1.82, 470°C, 56 ns		
9	LS-SLS TFTs	100 nm	$>E_{CM}$, RT, ~155 ns	34 nm th. SiO_2	0.30 J/cm^2
10	SIMOX-TFTs	100 nm	N/A	34 nm th. SiO_2	0.41 J/cm^2
11		150 nm	N/A	34 nm th. SiO_2	0.50 J/cm^2
12		250 nm	N/A	34 nm th. SiO_2	0.61 J/cm^2

- To form the gate, an aluminum layer was sputtered on and patterned in an $HBr–Cl_2$ plasma. Subsequently, the gate oxide was patterned in a low-power fluor-based plasma with the Al gate as a mask.
- The source and drain implantations were performed in a self-aligned manner with the aluminum–gate-oxide stack as a mask. The phosphorus dose was chosen independent of film thickness: 10^{16} ions/cm^2 at 35 keV. Implantations were performed directly into the silicon to avoid excessive lateral implantation and the damage associated with it [93].
- The source and drain implantations were activated by excimer-laser annealing pulses with 95% overlapping [94]. The energy density was chosen to be slightly below E_{CM} to achieve maximum activation while at the same time preserving the microstructure [95]. Again, the $Al–SiO_2$ stack of the gate was used as a mask to avoid lateral dopant diffusion from source and drain into the channel region.

Table 3.2. The spacing between the grain filters as a function of the various TFT dimensions.

W or L, whichever is larger (μm)	2	3	4	5	6	20
grain filter grid spacing (μm)	4	4	5	6	8	3

- For the isolation of the device, a thick TEOS-based PECVD SiO_2 layer was deposited. In order to get better step coverage, the deposition was performed in two steps. Prior to the second deposition, part of the first layer was etched away in a plasma.
- Finally, contact openings were etched and a second Al layer was sputtered and patterned to form contacts and large bonding pads placed around the device. The contacts were alloyed for 50 minutes in a N_2–H_2 ambient at 400°C.
- After electrical measurements, some wafers were given a 60 minute hydrogen plasma anneal at 350°C using the Novellus with N_2 and NH_3 gases at a ratio of 1:1. The pressure and power were 2 Torr and 75 W, respectively.

A schematic drawing of the thus obtained GF-TFT is shown in Figure 3.19. As can be seen in this figure, the TFT is placed on the central grain filter of a grid. Depending on the spacing between the grain filters, this could lead to the presence of a grain boundary between the contacts of either source or drain and the active channel region (these are shown in Figure 3.19 (b)). However, as doping concentration in this region is very high, this grain boundary does not impose a barrier for the carrier flow.

Large sets of TFTs were designed with varying dimensions and configurations (a full description of the layout is given in [90]). The various channel dimensions of TFTs manufactured and the corresponding spacing between the grain filters are listed in Table 3.2 The actual width and length of the channel were measured with SEM and it was found that length was 0.2 to 0.7 μm less than the designed value, depending on the actual processing conditions.

By shifting the TFT over a distance half the grid spacing, a TFT with a grain boundary either perpendicular or parallel to the current flow can be made, depending on the direction of the shift. Such TFTs were made to investigate the influence of a random grain boundary on the electrical properties. Also, very wide and long TFTs were made with several of these location-controlled grain boundaries either parallel or perpendicular to the current direction.

For the GF-TFTs, the sets of TFTs were made on grain filter grids with an original hole diameter of ~1.0, ~1.2, and ~1.4 μm. In addition to this variation in cavity diameter, a smaller variation was introduced by varying the exposure time during lithographic definition of these grids from 79% to 121% of the optimized value. This variation was done from left to right on the wafer in steps of ~6%. These values are

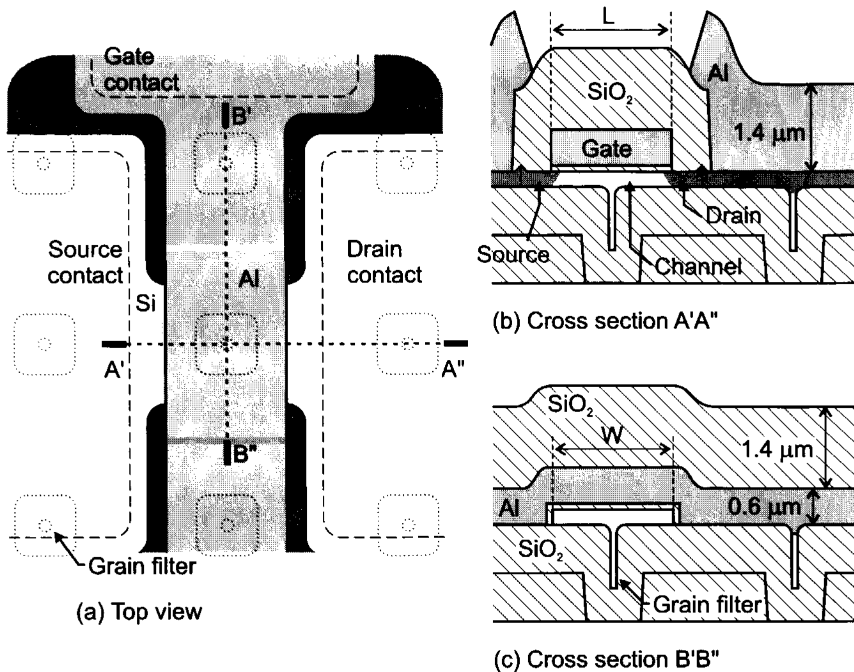


Figure 3.19. Schematic drawings of a grain filter TFT. (a) Top view with the passivation SiO_2 and the second aluminum layer removed showing the location of the grain filters and the planes of cross sections A'A" and B'B". (b) A cross section parallel to the carrier flow. (c) A cross section perpendicular to the carrier flow.

such that a 1.0 μm hole exposed with 121% of the optimized energy results in a similar grain filter as a 1.2 μm hole exposed with 79% of the optimized energy, and likewise for the other diameters. This allowed for an accurate investigation of the influence of the grain filter diameter on poly-Si microstructure and thus on transistor properties.

3.2. Sample Analysis

The various C-SLG methods were characterized both by studying the microstructure and by studying the electrical characteristics of TFTs.

3.2.1 Material Characterization

Most commonly, samples were analyzed after treatment with some defect-delineating wet etchant followed by analysis with scanning electron microscope (SEM). As a defect etchant, diluted Schimmel etch was preferred over the more

commonly used Secco etch because of its lower etch rates and higher etch rate ratio [96, 97]. Diluted Schimmel etch was made by solving 12.9 g CrO_3 in a mixture of 478 ml de-ionized water and 272 ml 49% HF. The CrO_3 acts as an oxidizing agent and the thus created SiO_2 is removed by the HF. The etch rate of LPCVD a-Si was ~11.5 nm/s, which equals that of PECVD TEOS, whereas {100} c-Si had an etch rate of ~4.3 nm/s. The etch rate of a grain boundary is anywhere between these two extremes, depending on the actual defect density.

The surface orientation of the grains in the poly-Si films and the nature of the boundaries between them were investigated with electron backscatter diffraction (EBSD) [98]. With this method, three-dimensional information of the crystallographic orientation of the grains is obtained by analyzing the backscattered electrons. The electron backscatter pattern (EBSP) was captured with a phosphor screen placed inside the SEM. The pattern consists of so-called Kikuchi bands that result from the backscattering on the various crystal planes. The patterns were automatically indexed by software from HKL Technology, Inc. by comparing to theoretically obtained patterns. Also, the grain boundaries were classified according to the CSL model (Section 1.1.2).

For EBSD, the samples were analyzed with a JEOL JSM-5600 microscope at Columbia University. In order to get a signal that is strong enough for detection, the SEM had to be operated at high voltage (20-25 kV) and the sample must be tilted to an angle of ~70° or more. The resolution is much less than common in SEM and in this research a lowest resolution of 200 nm was achieved. As a result, small grains and closely spaced planar defects could not be resolved. Still, this method gives a good idea of the grain boundary population and the crystallographic orientation of grains over a large area.

A more detailed view of the samples was obtained by transmission electron microscopy (TEM). Both top-view and cross-sectional images were made. Samples for top view TEM images were made with a lift-off method: the film is scratched around the area of interest and immersed in a 49% HF solution. During this, the SiO_2 layer is removed and parts of the film come floating to the surface. After dilution with de-ionized H_2O, these were caught with copper TEM grids and inspected with a JEOL JEM-100C microscope operated at 100 kV.

Cross sections for TEM observation were prepared and analyzed at the National Center for HREM at Delft University. Samples were made by cutting off a slice of the specimen, which was grinded and polished down to a thickness of ~15 μm. Subsequently, the sample was placed on a copper TEM grid and further thinned to electron transparency by argon ion milling. Samples were observed with a Philips CM30T operated at 300 kV.

To determine surface morphology, samples were analyzed with a DI Multimode Atomic Force Microscope (AFM) at Columbia University operated in contact mode with standard silicon nitride tips.

3.2.2 Device Characterization

TFT characteristics were measured with a HP 4156A/B Semiconductor Parameter Analyzer. Both output characteristics (i.e., I_D versus V_D) and transfer characteristics, (i.e., I_D versus V_G) were measured. From these measurements, the parameters described in Section 1.1.2 were determined.

From Equation 1.2 it can be seen that the carrier mobility in the linear regime can be calculated by determining the first derivative of I_D to V_G or, in other words, by determining the transconductance $g_m = \partial I_D/\partial V_G$ at a fixed value of V_D. This is called the field-effect mobility, μ_{FE}, which in this work was determined at $V_D = 0.2$ V [9]:

$$\mu_{FE} \approx \frac{Lg_m}{WC_{ox}V_D}. \tag{3.1}$$

Alternatively, the effective mobility in the linear regime can be obtained from the output characteristics by determining the conductance $g_D = \partial I_D/\partial V_D$. This is called the effective mobility μ_{eff}:

$$\mu_{eff} \approx \frac{Lg_D}{WC_{ox}(V_G - V_T)}. \tag{3.2}$$

Effective mobility was determined at $V_G - V_T = 1$ V or $V_G - V_T = 3$ V. Both definitions of mobility can be used to determine carrier mobility from TFT measurements. Care must been taken, however, to ensure that the device works in the linear regime (i.e., that V_D is small and $V_G - V_T > V_D$).

To determine μ_{eff}, the threshold voltage V_T must be known. V_T is obtained from linear extrapolation of the tangent to the I_D versus V_G curve ($V_D = 0.2$ V) at the inflection point, that is, at maximum slope. The intercept of the tangent with the V_G axis gives the threshold voltage.

The subthreshold swing S can be determined by taking the inverse of the maximum slope of the log (I_D) versus V_G curve.

3.3. Heat-flow Simulations

Heat-flow simulations were performed with a model recently developed at Columbia University [99, 100]. The model is capable of separately simulating the heat flow, the interface motion, and the nucleation of solids in a three-dimensional domain. The

domain is divided into an array of orthorhombic nodes and the maximum node number is 255 in either direction, allowing for accurate modeling, especially of nucleation events. The model has successfully been used in the simulation of C-SLG in the sequential lateral solidification of thin silicon films [101].

Through a non-equilibrium interface-tracking algorithm, the solid–liquid interfaces are allowed to depart from the equilibrium melting temperature. The rate of this kinetically limited interface motion is linked to its temperature through a user-defined interface-response function: an analytical expression of velocity versus temperature. While the interface moves, latent heat release or consumption is modeled as a local heat source or heat sink term within the nodes that contain the interface.

The stochastic nature of nucleation is modeled by calculating the nucleation probability at each liquid node and by comparing this to a random number assigned to each node at each time step. To describe this probability, the model uses Poisson statistics, as nucleation events are independent. If the random number is less than the calculated probability, this will result in nucleation occurring within this node. Only one nucleation event can occur in each node, so nodes should be sufficiently small in those areas of the domain where nucleation is expected.

All simulations that were performed within the scope of this research were done with a variable time step. Within this mode of operation, the model decreases the time step whenever either the temperature change or interface motion exceeds a certain user-defined maximum. This is done to ensure accurate simulation of the process without unnecessarily increasing calculation time.

The laser pulse was assumed to have a lognormal temporal profile, which is shown in Figure 3.2 (a) to give a good fit to the temporal profile of the XMR laser. However, the pulse from the LPX laser showed a secondary peak, which is not incorporated in the lognormal fit. This should then lead to an underestimation of the lateral growth distance due to a pulse by the LPX laser.

CHAPTER 4

Heat-Sink Grain-Location Control

This chapter discusses the results obtained with the first of two controlled super-lateral growth (C-SLG) structures of which the manufacturing was discussed in Section 3.1.3: the heat-sink structure. It was found that this structure indeed leads to C-SLG, although only for a small range of energy densities. Grain-location control, however, was achieved only to a limited extent, as the number of seeds for SLG was not sufficiently controlled. The majority of the laterally grown islands contained random high-angle grain boundaries.

4.1. Introduction

When the silicon is irradiated in vacuum, the heat absorbed in the film either diffuses out through the oxide–silicon interface or is lost by radiation at the surface. When the SiO_2 film is relatively thick compared to the thermal diffusion length (~0.5 μm), the rate of heat extraction to the substrate is solely determined by the thermal properties of the SiO_2. On the other hand, for a relatively thin SiO_2, it is also determined by the underlying layer. When this layer has a high thermal conductivity, heat-extraction rate will be increased. As was shown before in the case of crystalline silicon (Figure 2.19 (a)), this leads to an increase in the complete-melt energy density (E_{CM}), that is, more energy is needed to completely melt the film. Obviously, when glass substrates are used, a separate heat-conducting layer must be deposited to establish this effect. This will inevitably add to the complexity of the process.

By locally decreasing oxide thickness below the thermal diffusion length in oxide, a heat sink can be made. At this location, the rate of heat loss to the substrate is higher and the film will therefore remain at a lower temperature throughout the process. The subsequent increase in E_{CM} is partially compensated for by lateral diffusion of heat from the surrounding film towards the silicon on top of the heat

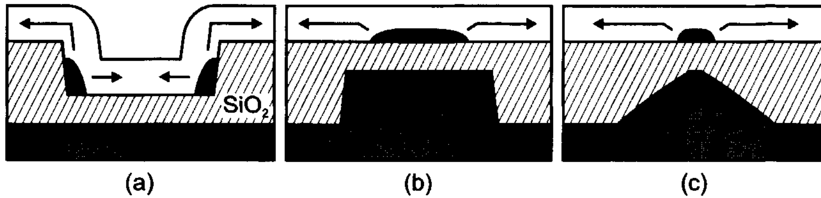


Figure 4.1. Three alternative implementations of a heat sink. The arrows give the direction of the lateral growth starting from the unmolten portions.

sink. Still, when the irradiation energy density is only slightly above E_{CM} for the surrounding film, a small unmolten portion can remain at the heat sink. During solidification, grains will laterally grow from this portion until stopped by nucleation of the surrounding film. The lateral growth distance, and thus the grain size, will be comparable to that obtained in 'standard' SLG, as the energy density is similar.

Although the SiO_2 could be locally thinned simply by etching a hole in a planar SiO_2 film like in Figure 4.1 (a), this would lead to unacceptable non-planarities in the subsequently deposited silicon film. Non-planarities can lead to incomplete melting due to effective film-thickness variations on these positions, as is schematically shown in Figure 4.1 (a). To enable the planarity of the silicon film, a mesa has to be made in the conductive layer. Then after SiO_2 deposition, the surface is planarized and the structure of Figure 4.1 (b) is obtained. When a seed starts growing in the center of this structure, it can freely grow beyond the edges of the structure and successful C-SLG is achieved.

To achieve grain-location control, the unmolten portion that remains should seed the growth of a single grain only, that is, it should contain only a single seed. Then, when no further defects are created during lateral growth, a true single-crystalline island is grown. If, on the other hand, multiple seeds are present in the unmolten portion, a polycrystalline island is formed with the grain boundaries lying parallel to the growth direction. The position of these grain boundaries is random and as a result, none of the goals stated in Section 1.2 can be achieved.

The seeds that are present in the unmolten portion are the remnant of the poly-Si that was created during the explosive crystallization phase. Therefore, to get a high yield of single-crystal islands, the unmolten portion should be smaller than the average grain size in the explosively poly-Si: 20-50 nm [49]. The thin oxide area, that is, the top of the heat sink, should therefore be as small as possible. To ensure sufficient heat conductance of the entire heat sink, however, the base should be sufficiently wide. The resultant structure is the cone-shaped heat sink, the manufacturing of which was discussed in Section 3.1.3.

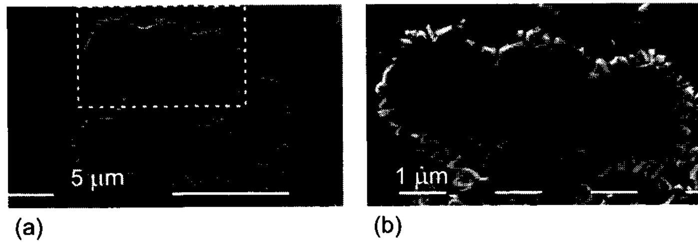


Figure 4.2. Two top-view SEM images taken of the same 4 × 4 grid of heat sinks treated with Schimmel etch, but with a different magnification. The heat sinks had a slope of ~20° and were irradiated at ~0.64 J/cm^2 at room temperature.

4.2. Experimental Results

An example of islands grown on a 4 × 4 grid of heat sinks with a pitch of 2.2 μm is shown in Figure 4.2. The cones had an angle α of ~22°C with the surface. If equal etch rates during the planarization etch are assumed, the thickness of the SiO_2 on top of the cone, t_{thin}, should be ~0.21 μm. From Figure 3.6, however, it can be seen that this was not the case and that t_{thin} was less than intended. As a ~0.1 μm thick SiO_2 film was deposited after the planarization (Figure 3.4 (e)), t_{thin} is at least ~0.1 μm. About four of the islands seem to be free of random grain boundaries, although some less defective planar defects can still be distinguished. The other islands clearly contain random grain boundaries. At some heat sinks, on the other hand, no large grains are observed. Apparently no unmolten portion remained at these positions during excimer-laser crystallization.

The SEM images in Figure 4.3 show the crystal growth on the same 4 × 4 grids for various energy densities. Below E_{CM} (Figure 4.3 (a)) the entire film was partially molten and only small grains can be observed. Around E_{CM} (Figure 4.3 (b)), lateral growth occurred around the heat sinks, but at the center of the heat sinks, the grain size is still very small. Slightly above E_{CM} (Figure 4.3 (c)), lateral growth was only observed around the heat sinks and no small grains were left in the center. Although it can be concluded that at this energy density full control of the SLG was obtained, the islands all consisted of multiple grains. Only when the energy density was further increased, single-grain islands were obtained. At these energy densities, however, SLG was no longer fully controlled, as at many heat sinks all silicon was molten. At energy densities only ~6% above E_{CM}, all silicon at the heat sinks was melted (Figure 4.3 (f)).

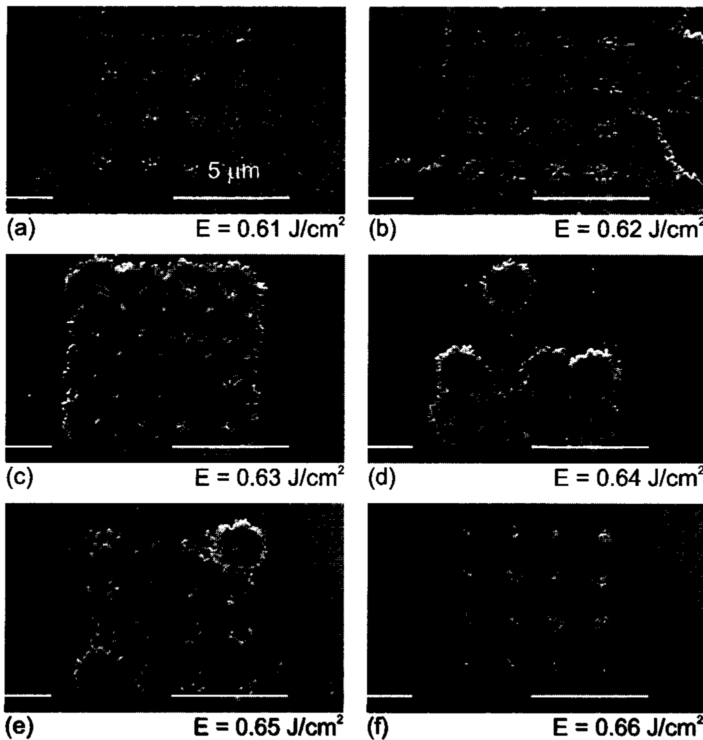


Figure 4.3. Top view SEM images of similar heat sink grids as in Figure 4.2 irradiated at various energy densities.

Figure 4.4 shows the distribution of the number of grains in one island as a function of energy density counted over 256 heat sinks. The heat sinks were distributed over a large area (several 100 μms wide) and thus the results were somewhat blurred as the laser energy density could not be considered constant over this area. Still, assuming that the number of grains was indicative of the number of seeds, the histograms give a good indication of the spread in the number of seeds remaining at each of the heat sinks. The average number of grains in one island drops from 6 to 3.5 to 2.5 for 0.63, 0.64, and 0.65 J/cm^2, respectively. The deviation around these values, however, is of a similar order so that at 0.64 and 0.65 J/cm^2 respectively ~52% and ~73% of the 256 analyzed heat sinks did not show lateral growth. At these positions, the film was completely melted and the film solidified after nucleation of solids.

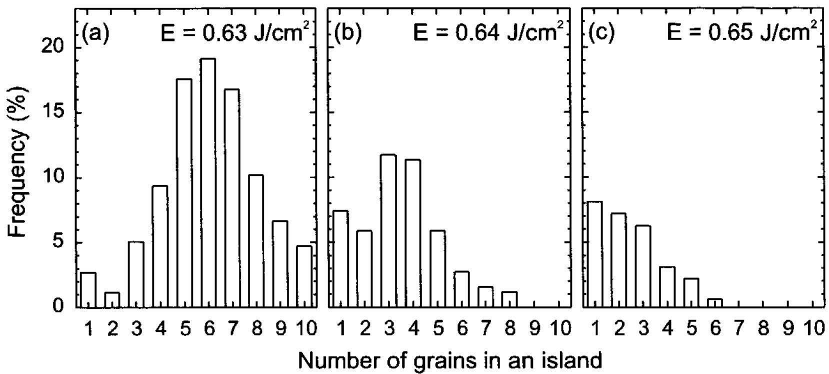


Figure 4.4. Number of grains originated at the center of the heat sinks shown in Figures 4.3 and 4.4. The number of locations analyzed was 256 for each energy density.

4.3. Simulation Results

The melt and growth fronts were monitored in three-dimensional grids with the model described in Section 3.3. The monitoring interval was 5 ns, although the time-step was of course much shorter. We found that for a 56 ns pulse (Figure 3.2 (a)), maximum melt depth for energy densities around E_{CM} was reached at t = 110 ns (i.e., ~35 ns after the peak power of the pulse). Figure 4.5 shows the size of the unmolten portion at that point of time for various energy densities. Only one quarter of the actual domain was simulated due to the four-fold symmetry of the pyramid structure. A cross section of the solid–liquid interface was taken along one of the edges of the simulation domain starting from the center of the heat sink. As expected, both the height and the diameter of the unmolten portion decrease with energy density. The portions have "tails" at their edges, but these are most likely due to instabilities in the calculations when the thickness or the unmolten portion becomes less than one node. At higher energy densities, the unmolten portion size becomes comparable to the node size and the simulations are less reliable. Still, a continuously decreasing portion size with energy density was monitored.

From these calculations, the E_{CM} at the center of the heat sink was calculated for various values of α and t_{thin} (Figure 4.6). Furthermore, with one-dimensional simulations, the E_{CM} of planar films was calculated as a function of SiO_2 thickness. This corresponds to the extreme situation $\alpha = 0°$. For comparison, the measured values from Figure 2.19 (a) are also plotted. It can be seen that the model agrees well with reality for these calculations. Also, it can be seen that the E_{CM} at the center of the heat sink is much lower than what is expected on the basis of the value of t_{thin}. This is indicative of the lateral heat flow from the surrounding silicon towards the

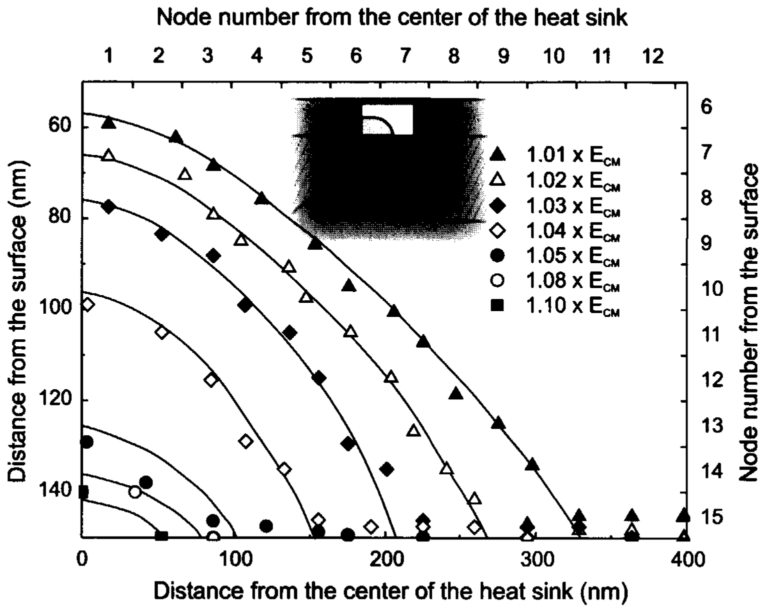


Figure 4.5. Simulated cross sections of the unmolten portion at various energy densities for a heat sink with $\alpha = 30°$, and t_{thin} is 40 nm (the part of the simulation domain that is shown is highlighted in the inset). The energy density needed to completely melt the silicon was ~1.15 × E_{CM} of the surrounding film.

heat sink. The result of this is that the energy density processing window is very small.

4.4. Discussion and Conclusions

With the use of heat sinks, C-SLG was obtained. The energy density window, however, was much smaller than expected based on Figure 2.19 (a). This is due to the lateral flow of heat through the highly conductive molten silicon towards the heat sink. Within the window of 100% yield of C-SLG, no single-grain islands were obtained or, in other words, the unmolten portion was significantly larger than the average grain size in the explosively-crystallized silicon. Only at higher energy densities, some islands free of random grain boundaries were observed. However, these coexisted with islands containing multiple grains and locations where no large grains were grown. The maximum yield observed was ~8%, although in that case, the area over which heat sinks were analyzed was very large, and consequently, the laser energy density could not be considered constant. Still, even on a small scale of only 4×4 heat sinks (i.e., less than 10×10 μm^2), no high yield of single-grain islands was obtained. Partially, this can be contributed to the energy-density fluctuations by

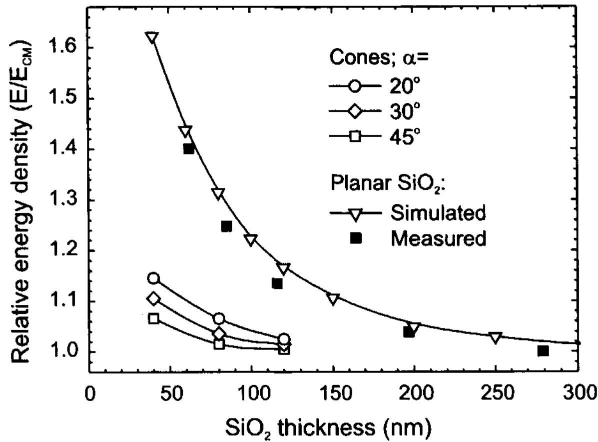


Figure 4.6. Local values of E_{CM} as a function of t_{thin} for various values of the angle of the cone α. The calculated and measured E_{CM} of a non-structured planar film stack is also given.

interference effects caused by the cylindrical lens arrays as discussed in Section 3.1.1. Also, it is conceivable that during lithography and planarization non-uniformities were introduced in the shape of the cone and t_{thin}, respectively.

Apart from these technological sources of non-uniformities, there is also a more fundamental limit to the yield of single-grain islands. The seeds for the lateral growth were created during the explosive crystallization. The grain size is small and the location of the grains is random. As a consequence, even if the unmolten portion has a diameter less than the average grain size, there still is the possibility that it contains multiple seeds.

The single-grain islands that were obtained had a diameter similar to that of grains grown in the incomplete melt regime. The quality of the grains, however, seems to be slightly less as only few of the observed islands were free of low defect-density planar defects. This can most likely be related to the selection mechanism. In SLG, the least defective grains are "selected", whereas with heat sinks a "lucky" grain is selected for its location, even when it is highly defective.

In conclusion, it can be said that the heat sink structure is not applicable for a high performance TFT process. The size of the unmolten portions could not be sufficiently controlled and as a result they often contained multiple seeds.

CHAPTER 5

Embedded-Seed Grain-Location Control

In this chapter, the second concept of grain-location control is discussed in which embedded portions of unmolten silicon seed the lateral growth. Two different variations of this concept were investigated: bottle-shaped and U-shaped cavities (the manufacturing of these structures was discussed in Section 0). Compared to the heat sinks (Chapter 4), the former structure led to a much higher yield of grain-location control. This was attributed to a much better control of the diameter of the unmolten portion. The latter structure was found to lead to almost complete grain-location control: the majority of the islands were free of random grain boundaries. This was attributed to the concept of grain filtering in which a single seed is selected for lateral growth.

5.1. Introduction

From Chapter 4 it was concluded that the heat sink structure could not lead to a high yield of grain-location control. The two problems that can be discerned are: (1) the insufficient control of the size of the unmolten portion and (2) the lack of control on the number of seeds in the unmolten portion. These two problems have to be solved in order to get a ~100% yield of grain-location control over a large range of energy densities. In the embedded-seed grain-location-control (ES-GLC) methods that are discussed in this chapter, the first problem is solved by putting a geometrical constraint on the diameter of the unmolten portion. The second problem is solved by adding a selection stage prior to the lateral growth in which a single grain is selected to act as seed.

EMBEDDED SEEDS

Controlled super-lateral growth (C-SLG) is obtained through the film-thickness dependence of the complete-melt energy density (E_{CM}) shown in Figure 2.19 (b). Locally, the film thickness is increased so that more energy is needed to completely melt the film. Through the fabrication of a cavity prior to a-Si deposition (Section 0), this thicker part lies embedded in the underlying SiO_2 layer, as is shown in Figure 5.1. When the film is completely melted, a small unmolten portion remains embedded in this cavity. This portion will act as a seed for lateral growth and its diameter is now more accurately controlled than was the case with the heat sinks. When the diameter is in the order of the average grain size of the explosively crystallized poly-Si film, there is a good chance that the portion contains only one seed. As a result, the yield of grain-location control is higher than was the case with heat sinks. Again, like with the heat sinks, the difference in E_{CM} (i.e., the energy density process window) is partially compensated for by lateral diffusion of heat from the surrounding film towards this structure. Unlike for the heat sinks, however, this can be dealt with by simply increasing the depth of the cavity.

As was discussed in Section 0, sufficiently small cavities could not be made in one step because the resolution of lithography (~1 μm) was more than one order of magnitude larger than the diameter of the explosively crystallized (XC) poly-Si grains (20-50 nm). The two-step process that was employed yielded two significantly different embedded-seed structures: the bottle-shaped and the U-shaped cavities (Figure 5.1 (a) and (b), respectively). In the former method, accurate control of the diameter of the cavity immediately below the surface is achieved. When this structure is irradiated at an energy density slightly above E_{CM} of the surrounding film, the melt reaches into the neck of the bottle. The unmolten portion seeding the lateral growth now has a minimal diameter and a high yield of grain-location control is expected. Results obtained with this method are discussed in Section 5.2.

GRAIN FILTERING

The unmolten portion in the bottle-shaped cavities is, however, still expected to contain a random number of seeds, although the average number is now much smaller. With the U-shaped cavities, on the other hand, a single seed could be obtained prior to the lateral growth of an island by a selection mechanism. When most of the silicon column in the cavity is melted during excimer-laser crystallization, the lateral growth will be preceded by a vertical-growth stage. This growth will start on a small unmolten portion that lies embedded at the bottom of the cavity, as shown in Figure 5.1 (b). This portion is a remnant of the explosively-crystallized poly-Si and hence will contain one or more crystalline seeds. During the vertical growth stage, however, some of the grains that grow from these seeds will be occluded from further growth. Such occlusion of grains is commonly observed

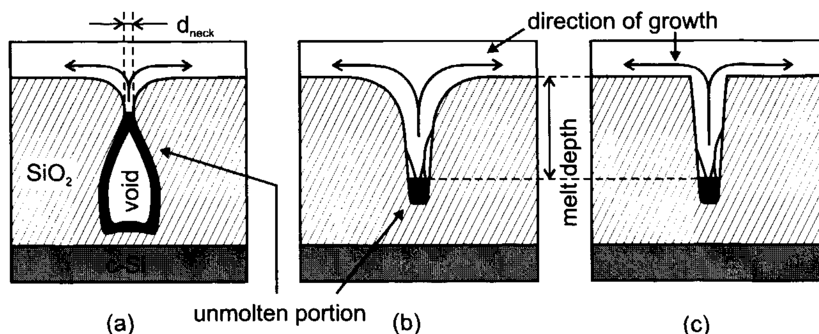


Figure 5.1. Schematic drawings of the three ES-GLC structures and the associated principle of C-SLG: (a), the bottle-shaped cavity, (b), the U-shaped cavity, or grain filter, made with the two-step process, and (c), the grain filter made with the three-step process.

during planar regrowth from the liquid phase [102], for example in the incomplete melt regime (Section 2.2.2). When this stage lasts long enough (i.e., when the melt is sufficiently deep), only a single grain will remain. This grain will then seed the lateral growth of an island that is thus potentially single crystalline. Because of the ability of this structure to 'filter' out a single grain from a set of initial grains, we call this structure 'grain filter'. Furthermore, as this occlusion is often driven by the crystallographic orientation of the grain (i.e., certain orientations are preferred over others), this could potentially lead to a textured film, that is, having a preferred surface orientation. Results obtained with the U-shaped cavities will be discussed in Section 5.3.

An important assumption in the occlusion hypothesis is that the growth front during the vertical growth stage is planar. If it were concave, growth would always be directed towards the center of the cavity. Based on differences in thermal conductivity between Si and SiO_2, however, it is expected that the growth front is at least slightly concave. This is due to heat flowing from the surface through the thermally conductive silicon column into the surrounding SiO_2. This lateral temperature gradient at the walls of the cavity will lead to a concave growth front. To minimize this effect, one should make the grain filter diameter sufficiently small.

ENERGY DENSITY WINDOW

The lower limit for C-SLG is formed by the complete-melt threshold, E_{CM}, of the surrounding film and the upper limit is formed by the energy density at which no unmolten portion is left. The energy density window is thus expected to be proportional to the depth of the cavity. When the cavity is sufficiently deep, however, the upper limit of C-SLG is no longer determined by the local E_{CM}, but by the global critical energy density for agglomeration: E_{AGG}. From Figure 2.19 (b) it

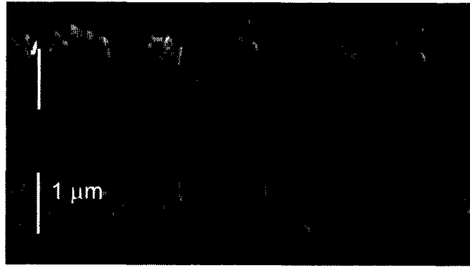


Figure 5.2. Top-view SEM image of a defect-etched row of islands grown from bottle-shaped cavities. Film thickness was ~150 nm, $d_{neck} \approx 35$ nm, and energy density was 0.74 J/cm^2 (E_{CM} = 0.71 J/cm^2) irradiated with the XMR system at room temperature.

can be seen that E_{AGG} lies well above E_{CM} and as a result the energy density window for C-SLG is very large.

In the case of the grain filters, it also makes sense to talk about the energy density window for grain-location control. The upper limit is expected to be equal to the upper limit for C-SLG. The lower limit for grain-location control, however, should be somewhat higher as successful filtering is required to take place. This limit is expected to be related both to the melt depth and the cavity diameter. To a first approximation the lower limit can then be defined as a certain depth-to-diameter ratio of the melt: the larger the diameter of the cavity, the longer it takes for successful filtering to take place and the larger the required melt depth.

As the grain filters fabricated with the two-step process described in Section 0 have a rounded rim (Figure 5.1 (b)), the diameter of the cavity rapidly increases above a certain level. As filtering is no longer expected to occur in this larger-diameter region, a larger depth-to-diameter ratio of the melt is thus required to get grain-location control. This then will increase the lower limit for grain-location control. To this end, the three-step process for grain filters was developed: when the rim is sharp, successful filtering is expected to take place at lower energy densities than for a rounded rim (Figure 5.1 (c)).

5.2. Bottle-Shaped Cavities

Figure 5.2 shows a top-view SEM image after Schimmel etching of a row of islands grown from bottle-shaped cavities. Of the six islands, the last two contain defects that are clearly more defective than the defects found in the other four islands. It is thus considered that these planar defects are random high-angle grain boundaries, whereas the others are special high-angle grain boundaries or sub-grain boundaries. Due to the absence of random high-angle grain boundaries, the first four islands are

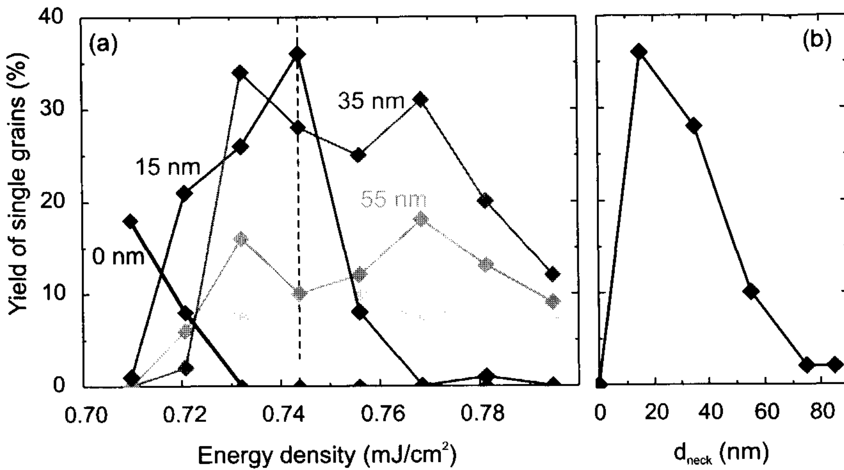


Figure 5.3. Yield of single grains in a 150 nm film as a function of (a) both energy density and neck diameter and (b) of neck diameter alone at E = 0.74 J/cm^2.

considered to have originated on a single seed. In other words, at these positions, successful grain-location control was achieved.

Out of grids of 100 embedded-seed structures, the yield of grain-location control was counted as a function of energy density and neck diameter d_{neck}. The yield as a function of the energy density is plotted in Figure 5.3 (a). In Figure 5.3 (b), the yield is plotted as function of d_{neck} at 0.74 J/cm^2 (this energy density is indicated in Figure 5.3 (a) by a dotted line). A maximum yield of 36% was recorded at this energy density, which, in comparison to what was obtained with heat sinks (~8%), proves the viability of the embedded seed concept. Such high yield is only reached for very small d_{neck} and decreases rapidly for diameters of ~55 nm and larger. This result agrees very well with what was obtained from cross-sectional TEM analysis, which showed that the explosively-crystallized grains have a diameter of 20–50 nm. When the neck diameter is smaller than this, there is a considerable chance of grain-location control.

As was expected, the lower limit for C-SLG is the E_{CM} of the surrounding film, regardless of the neck diameter. The upper limit was found to depend on d_{neck}. When the cavity was completely closed during second SiO_2 deposition (Figure 5.4 (a): d_{neck} = 0), the upper limit of C-SLG is defined by the complete melt of the silicon. Since the indentation is very shallow, this energy density is only marginally higher than E_{CM} of the surrounding film. Within this energy density window for C-SLG, an 18% yield of grain-location control was found (Figure 5.3 (a)).

For non-zero values of d_{neck}, it was expected that the upper limit for C-SLG was determined by the complete-melt threshold of the silicon in the cavity. It was found, however, that the upper limit was at much lower energy density. This was related to

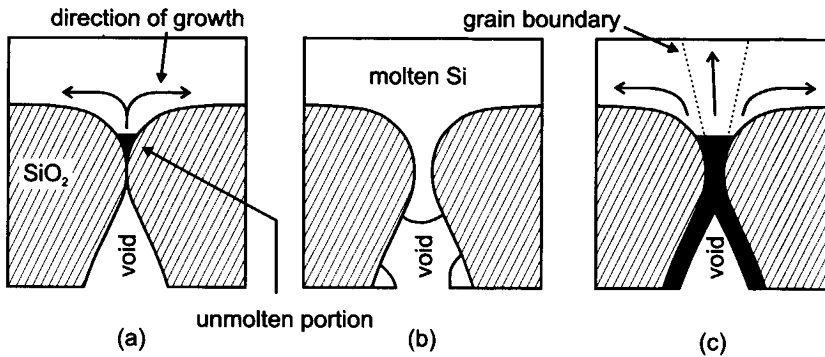


Figure 5.4. Schematic drawings of (a) C-SLG from a closed cavity (i.e., $d_{neck} = 0$). (b) Complete melt and agglomeration of the upper part of the silicon deposited in the cavity. (c) The growth of multiple large grains when energy density is too low for a high yield of single grains, although C-SLG is indeed obtained.

the presence of a void: when the melt reaches the void, the silicon in the cavity could start to agglomerate. When this happens, the silicon could become discontinuous: the liquid silicon of the film is no longer in contact with the silicon in the cavity: Figure 5.4 (b). As a result, there is no longer a solid portion left to seed the lateral growth; the film will become supercooled and will solidify after nucleation into small-grain poly-Si. It was found that this upper limit of C-SLG scaled with the neck diameter. This could be related to the thickness of the a-Si inside the cavity, which increases with increasing d_{neck} as deposition in the cavity stops when the neck is filled with a-Si. For thin silicon the agglomeration led to the film becoming discontinuous at lower energy density than for thicker silicon.

This upper limit of C-SLG is also reflected in Figure 5.3: above this energy density, the yield of grain-location control drops as a result of the agglomeration. At energy densities slightly above E_{CM} of the surrounding film, on the other hand, the yield is seen to increase with energy density. This can be related to an initial decrease in diameter of the unmolten island as is illustrated in Figure 5.4 (c): only when the melt reaches beyond the neck of the cavity, a maximum yield of grain-location control is obtained.

From the results it can then be concluded that C-SLG with a significant yield of grain-location control can indeed be obtained with the bottle-shaped cavities. The energy density window, however, is constrained by the presence of the void: when the melt reaches the void, the film could become discontinuous due to agglomeration and no large grains will grow. Although the average number of seeds in the unmolten portion is reduced by controlling the diameter, real control of the number of seeds is not obtained. Even when grain-location control was obtained, the size of the grains was only marginally larger than those obtained in the SLG "regime".

5.3. U-Shaped Cavities

As was discussed in Section 5.1, the U-shaped cavities are expected to lead to a higher yield of grain-location control through the concept of grain filtering. This section discusses the results obtained with this method and the influence of various parameters on the quality and the diameter of the islands. Next, the filtering and the creation of defects are discussed in more detail. Finally, heat-flow simulation results are discussed. These simulations were used to better understand the experimental results.

5.3.1 Island Properties

The properties of the islands grown with grain filters were investigated with SEM on Schimmel etched samples. Grain filters with varying diameter were investigated, as well as grain filters made with the two-step and the three-step process, that is, non-planarized and planarized grain filters. A strong dependence of island quality and diameter on energy density and on film thickness was observed. Pulse duration and substrate heating were found to have a strong influence on the diameter of the islands, but no significant influence on island quality was observed.

ENERGY DENSITY EFFECTS

Figure 5.5 shows an overview of experimental results obtained as a function of energy density and grain filter diameter, for non-planarized and planarized grain filters. Planarization was performed by the laser and plasma planarization (LPP) process described in Section 0. The film thickness was 250 nm and 235 nm, respectively and samples were irradiated at a temperature of 470°C with the XMR system. Although similar results were obtained with samples irradiated at room temperature, these are not discussed, as analysis was complicated by cracking of the film during defect etching (Section 2.2.4).

The grain-filter grid spacing was 3 μm so that islands could not grow larger than $3 \times 3\ \mu m^2$. Each image in Figure 5.5 shows 2×4 islands out of a much larger grid. The bright spots on the corners of these islands are hillocks created by the collision of four growth fronts at that position (Section 2.2.2). From these images, a number of qualitative observations about the microstructure of the islands can be made:

- Square $3 \times 3\ \mu m^2$ islands are obtained for the complete range of energy densities from E_{CM} to E_{AGG} and even beyond (as long as the film does not ablate). Compared to the bottle-shaped cavities, this is a remarkably large window in which C-SLG is obtained. Only for the planarized grain filters irradiated at $1.20 \times E_{CM}$ some nucleation could occur in the film before lateral growth started from the grain filter. This was attributed to the thin layer of

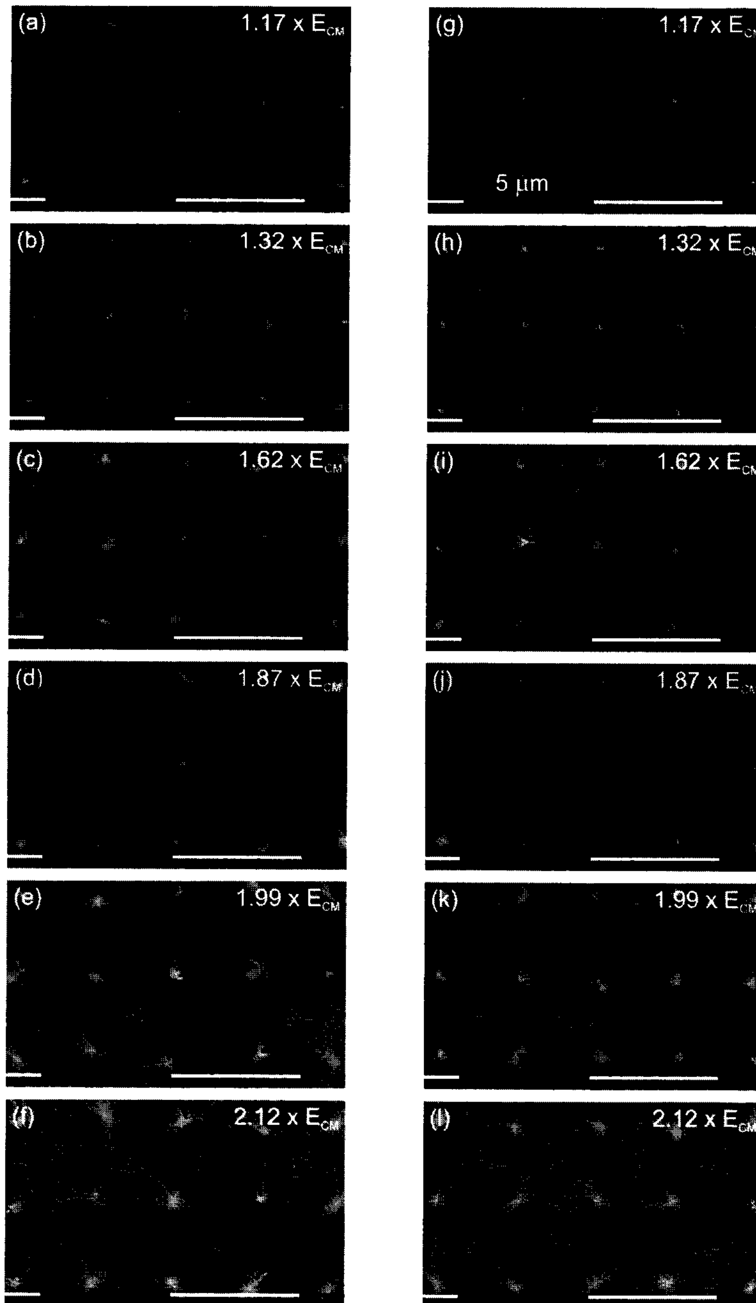


Figure 5.5. SEM images of a Schimmel etched ~250 nm silicon film on a 3 μm grid of grain filters irradiated at different energy densities. (a)-(f): 1.4 μm grain filters. (g)-(l): 1.2 μm grain filters

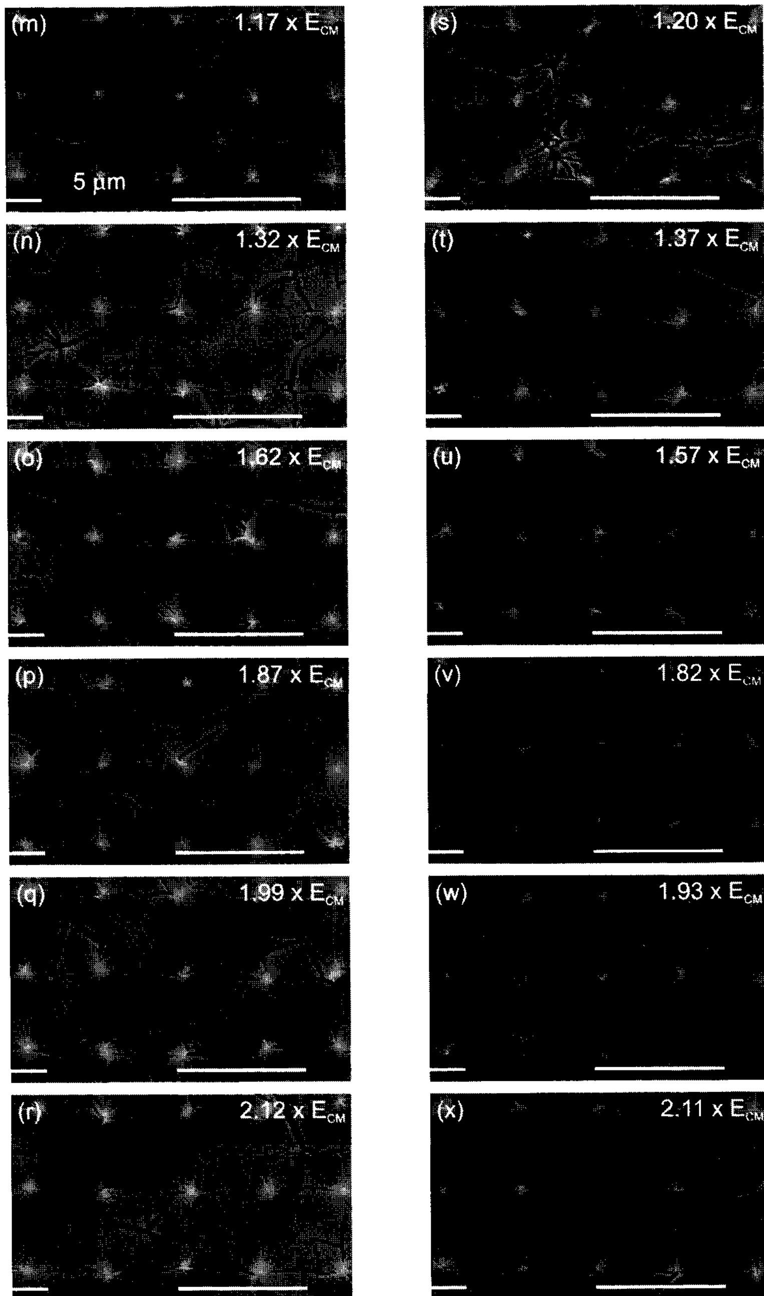


Figure 5.5 (continued) (m)-(r): 1.0 μm grain filters, and (s)-(x): 1.0 μm planarized grain filters.

native SiO_2 that, in spite of a short dip etch, may have been present between the silicon of the first deposition and that of the second deposition [103]. Apparently, this layer remained intact during the process, and as a result, no seeds for lateral growth were present. With higher energy densities, this layer will be broken and it will dissolve in the silicon.

- With the non-planarized grain filters, the quality of the islands improves both with decreasing cavity diameter and with increasing energy density. For large diameters and for low energy densities, the majority of the planar defects seem to originate at the center of the grain filter. Also, from their course, they appear to be random high-angle grain boundaries. This suggests that during the vertical growth stage, more than one grain survived or, in other words, that filtering was not successful. At somewhat higher energy density and for the 1.0 μm cavities, on the other hand, the planar defects often originate in the approximate surroundings (within a few 100 nm) of the grain filter rather than at the exact center. Also, since they are often straight and less severely etched during Schimmel etching, they appear to be mostly special grain boundaries (i.e., low-Σ-value CSL boundaries or sub-grain boundaries). This suggests that the islands originate on one seed (i.e., filtering was successful), but that planar defects are created during growth. For the 1.0 μm cavities, this seems to be the case for all energy densities from $1.32 \times E_{CM}$ to $2.12 \times E_{CM}$ as no significant changes in microstructure are observed.
- Up to a relative energy density of $1.82 \times E_{CM}$, the islands obtained with the planarized grain filters contain less planar defects than those with the non-planarized grain filters. This lower number of planar defects seems to be caused by the absence of those defects that originate in the approximate surrounding of the grain filter. This suggests an influence of the rim of the grain filter on the creation of planar defects. Apparently, when the rim has a large radius of curvature, many defects are created in this region. When the rim is sharp, on the other hand, this defect creation mechanism is largely suppressed. Above a normalized energy density of $1.93 \times E_{CM}$, however, the number of planar defects in the islands obtained with the planarized grain filters increases abruptly.

The sudden increase in planar defect density observed for the planarized grain filters coincides with a decrease in the lateral-growth distance as measured from isolated grain filters (i.e., a grid spacing that was much larger than the lateral-growth distance). A similar effect was observed for the grain filters with a large cavity diameter. Results of these measurements are shown in Figure 5.6; the average diameter of four islands is shown and the lateral-growth distance is of course half this value. It is found that for all structures apart from the non-planarized 1.0 μm structures, there is an energy density above which the island diameter drops. Not

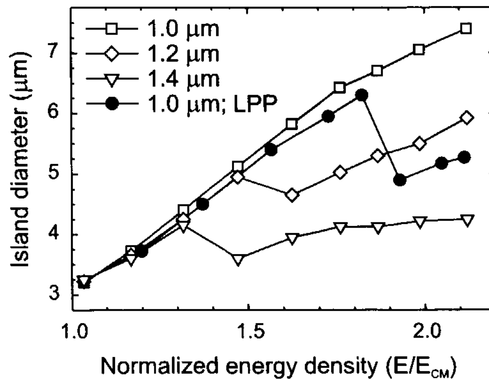


Figure 5.6. The average lateral dimension of the islands grown in a ~250 nm film from both types of grain filters as a function of normalized energy density at 470°C.

shown in this graph are the results from 1.2 and 1.4 μm planarized grain filters. The drop in island diameter was at very low energy density and above this energy density island diameter became comparable to that of nucleated grains.

The abrupt reduction in island diameter and quality seem to suggest that growth started on nucleated solids rather than on an unmolten solid. As temperature near the bottom of the cavity is coolest, this is where nucleation is most likely to occur. Initial growth rate is very high and this explains the high defect density of the islands. Also, as growth started past the lateral-growth interval Δt_{LG}, the size of the islands is much smaller. The energy density at which complete melt of the silicon in the cavity (i.e., the local E_{CM}) is obtained, apparently depends on both depth, diameter, and rim curvature of the grain filter. More evidence for this complete melt hypothesis is obtained from heat-flow simulations presented in Section 5.3.3.

In conclusion, it can be said that from these qualitative observations we found that grain filtering seems to be obtained over a large range of energy densities when the diameter of the cavity is very small. Still, the islands contain many planar defects. Since they seem to be less defective and since they often seem to originate at the rim of the grain filter, it was concluded that they were created during the growth. From the comparison of results with those obtained with planarized grain filters, it was concluded that defect creation is related to the rim. A more detailed analysis of defect creation is presented in Section 5.3.2.

FILM-THICKNESS EFFECTS

Figure 5.7 shows a comparison of islands grown on samples with variable film thickness. All samples were irradiated with the Microlas system, that is, at room temperature and in air. The pulse duration was not found to have a significant influence on the microstructure. The lateral growth distance of course increases with

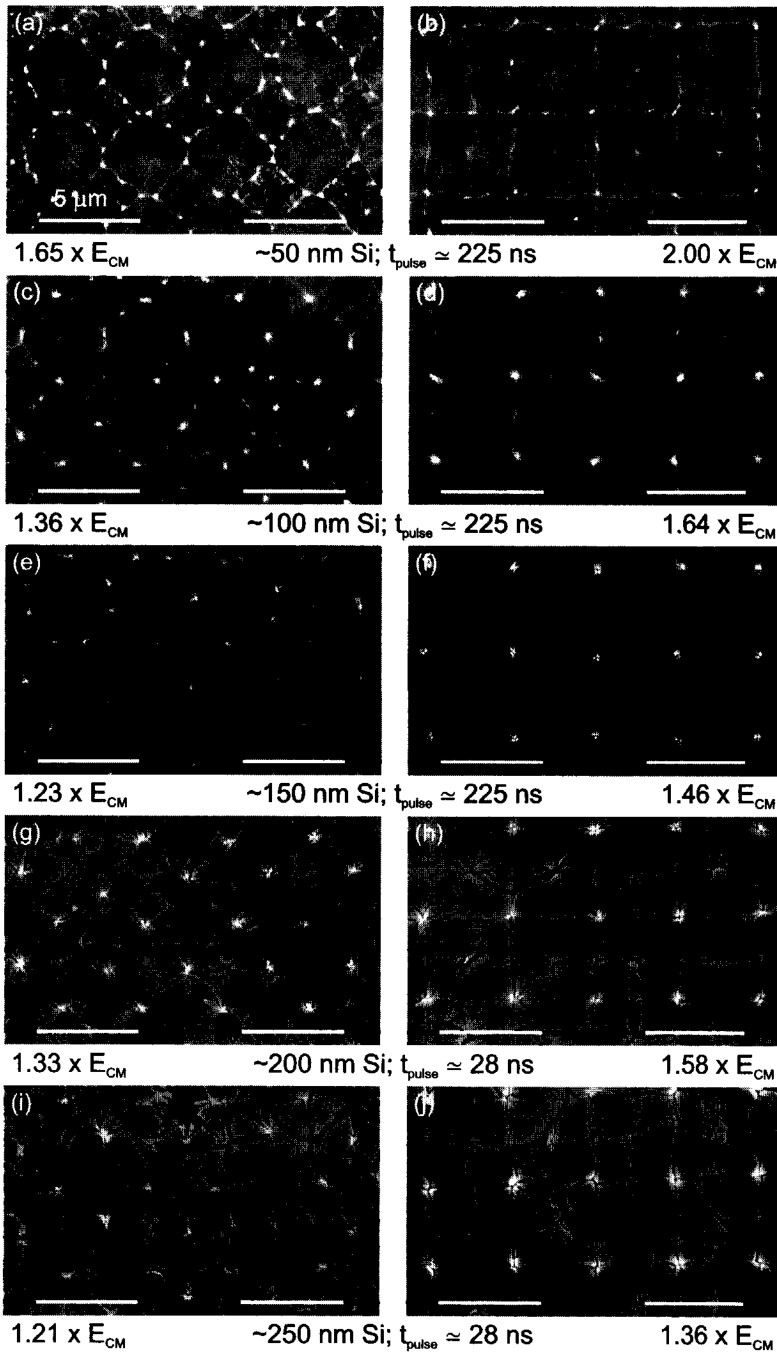


Figure 5.7. Top-view SEM images of islands grown from a 4 µm grid of non-planarized grain filters with an original diameter of 1.0 µm. Five different film thicknesses are shown irradiated at a low and the highest energy density.

the pulse duration, and therefore we preferred using the longest possible pulse. For the 200 and 250 nm films, however, it was found that E_{CM} at this pulse duration was close to the maximum energy density of the system. This is due to losses in the many optical components of the pulse-duration extender. Therefore, for these films, the results from samples irradiated with the 28 ns beam of the laser are shown.

The grid spacing was 4 μm and again 2 × 4 islands are shown. The 250 nm films and to a lesser extent the 200 nm films show severe cracking, especially at high energy densities. In Section 2.2.4, this was related to the release of thermal stress during Schimmel etching. Some qualitative observations that were made from the images in Figure 5.7 are:

- The number of planar defects increases with decreasing film thickness. Whereas for the thicker films the defects seem to originate mostly at or close to the grain filter, for the thinner films, defects are also created further away from the grain filter, that is, during the lateral growth stage. These observations are similar to what was observed in sequential lateral solidification (SLS) experiments of thin silicon film, as was discussed in Section 2.2.3 [61]. Planar defects are common in lateral growth and the spacing between them increases with film thickness. From SLS experiments on c-Si thin films, however, it was found that defects form only after a few pulses. When the film is very thin and when the growth is radial (from one point outwards), on the other hand, it seems plausible that even within one pulse defects can be created due to the thermal stresses.
- The indentation that is present at the surface of the silicon film after deposition does not fully disappear for the 50 nm thin films. The same was observed for larger-diameter grain filters, even for thicker films. Apparently, in these cases the melt duration was not sufficient for complete reflow.

Figure 5.8 shows the island diameter as a function of normalized energy density for a 150 nm film irradiated with a ~225 ns pulse at room temperature. Like in a ~250 nm film (Figure 5.6), the island diameter depended on the cavity diameter. There was, however, no clear drop in island diameter as a function of energy density that could be related to the complete melt of the silicon column. Instead, the island diameter seemed to decrease gradually with cavity diameter. This could be due to the reflow of liquid silicon, which for thinner films is likely to have more impact than for thick films. The inward transport of liquid silicon leads to an increase of volume at the center of the grain filter and, apparently, the lateral growth is slowed down by this process. The sudden rise in island diameter for the narrowest cavity is an artifact from the spacing of the grain filters, which was 8 μm. At this energy density, islands started to close in on each other as a result of which the film between the opposing growth fronts was heated, and nucleation was avoided.

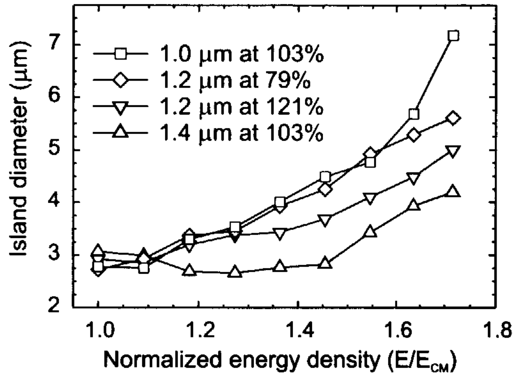


Figure 5.8. The average lateral dimension of the islands grown from non-planarized grain filters as a function of normalized energy density. Film thickness was ~150 nm and pulse duration was ~225 ns.

SUBSTRATE TEMPERATURE AND PULSE DURATION EFFECTS

As was already observed, the substrate temperature and the pulse duration do not seem to have a significant influence on island quality. The maximum lateral growth distance, however, is seen to increase with both these parameters. Figure 5.9 shows this effect for three different values of the film thickness. The minimal energy density required to obtain a certain square grain size is plotted together with the threshold energy densities for surface rippling and agglomeration. The crosses show the energy densities that were used in this experiment and as can be seen, energy densities above E_{AGG} were also used. The number of holes that appear in the film, however, was still very low. At these high energy densities, square islands with a diameter of 7 μm were obtained in a 250 nm thick film irradiated at 470°C.

With the ranges of temperatures and pulse durations used in this work, similar effects on lateral growth distance were obtained. Still, some relevant differences can be discerned:

- With substrate heating, external energy is used to heat the substrate and also the film, so that less laser energy is needed to completely melt the film. With pulse-duration extension (PDE), on the other hand, heat from the pulse itself is used to heat the substrate, and as a result, more laser energy is needed to completely melt the film. In addition to this, a lot of laser energy is wasted due to the many optical elements required for PDE (typically more than 50%).
- With substrate heating, the threshold energy densities for surface rippling (E_{SR}) and agglomeration (E_{AGG}) are increased relative to the complete-melt threshold (E_{CM}) and as a result the upper limit of the process window is increased. With PDE, however, E_{SR} and E_{AGG} are decreased relative to E_{CM}.

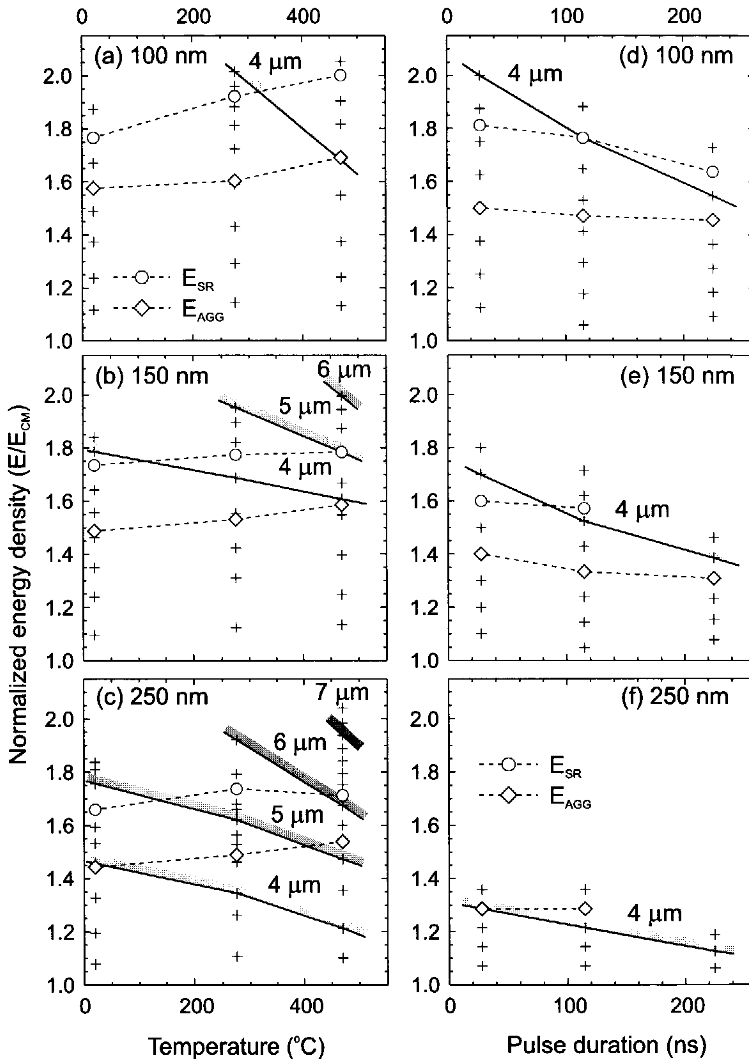


Figure 5.9. The minimal normalized energy densities at which square islands are obtained from a grid of 1.0 μm grain filters as a function of both temperature (a-c) and pulse duration (d-e) for 100 nm, 150 nm, and 250 nm films, respectively. Also shown are the critical energy densities for surface rippling and agglomeration as these determine the upper limit for the process.

- Substrate heating proved to be successful in reducing the thermal stress in the film that was visible through cracking of the film during the Schimmel etch. With PDE, on the other hand, cracks were still present.

From an experimental point of view it can thus be concluded that, at least in the case of grain filters, substrate heating is the preferred method to enhance lateral growth.

Apart from a reduction in the cooling rate, another method to enlarge grain size that was mentioned in Section 2.2.5 is multiple-pulse irradiation at an energy density close to E_{CM}. Although this was indeed seen to lead to larger islands in some cases, in many cases the islands even shrank to a diameter less than 1 μm. As grain-size enlargement is only expected for grains with surface crystallographic orientation close to {111}, this was an indication that the islands have random crystallographic orientation. Normally, without embedded seeds, the grains that do not have the preferential orientation will be completely consumed by those that have. With grain filters, however, this will not happen as the seeds lie embedded in the SiO_2 and cannot fully melt at the energy densities at which the grain size enlargement can be achieved. As a result, small grains with a non-preferential orientation will remain at many of the grain filters.

5.3.2 Defect Analysis

A better understanding of the filtering and defect creation mechanisms can be obtained from analyzing the nature and the origin of the planar defects. This was done by electron backscatter diffraction (EBSD) and transmission electron microscopy (TEM), as described in Section 3.2.1.

NATURE OF THE PLANAR DEFECTS

EBSD was performed to analyze the planar defects and to investigate possible texture obtained with the grain filters. Not all positions on the sample gave patterns that could be indexed: when the electron beam is pointed exactly on the grain boundary between two grains, the pattern will be a mixture of that of both these grains. Obviously, indexing in this situation is prone to error, but as long as enough data is gathered from the immediate surroundings, this missing spot can be filled in by post-measurement extrapolation. With small grain size, however, some grains may be missed altogether and extrapolation may lead to erroneous results. Such is the case when the average grain size, that is, the average planar defect spacing, is less than the EBSD step size, which was at least 0.2 μm. As a result, the indexing efficiency was very low for the 50 and the 100 nm samples, as the grain boundary spacing was small (Figure 5.7). For the same reason, large-diameter grain filters and samples irradiated at low energy density had low indexing efficiency making the measurements less meaningful.

Figure 5.10 shows a representative example of an EBSD scan performed on a sample with 1.0 μm grain filters with a spacing of 4 μm and a film thickness of 150 nm. The measurement is split into four different maps to highlight different types of defects. Figure 5.10 (a), (b), and (c) show the $\Sigma3$, the $\Sigma9$, and the $\Sigma27$ grain boundaries, respectively. Figure 5.10 (d) shows the remaining grain boundaries and the zero solutions or, in other words, the positions where no indexing was possible.

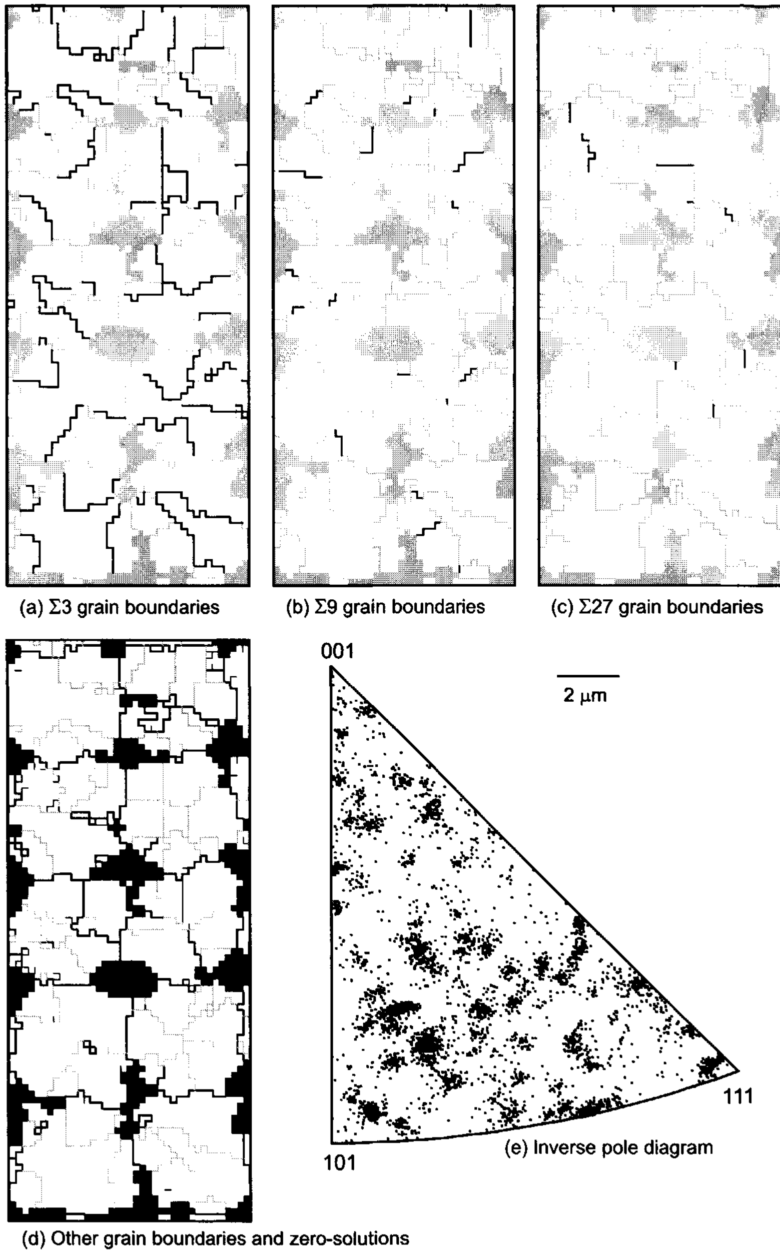


Figure 5.10. Results of a single EBSD scan of islands in a 150 nm silicon film grown from a grid of 4 μm 2x5 1.0 μm grain filters irradiated at 1.46 × E_{CM}. The results are split into four maps showing Σ3, Σ9, Σ27, and other grain boundaries. The black areas are locations where the pattern could not be fitted to the model. These correspond to the hillocks found at the corners of the islands.

These are mostly located at the corners of the islands as a result of the hillocks at these positions. It can be seen that all islands contain planar defects, but that the majority are Σ3, Σ9, or Σ27 grain boundaries and few other, more random, grain boundaries are present. For increasing cavity diameter, we found that the number of random grain boundaries increased, which was already suggested by the SEM images in Figure 5.5. Interestingly, the ratio between Σ3, Σ9, and Σ27 grain boundaries was found to be independent of both energy density and cavity diameter and was approximately 35:5:2, respectively.

From the inverse pole figure shown in Figure 5.10 (e) it can be seen that no texture is obtained. This either suggests that the occlusion of grains is not related to the crystallographic orientation or that the vertical growth stage did not start on a sufficiently large set of grains, so that the preferred orientation was often not present. The former could be the case when the filtered grain is just a "lucky" grain that happens to survive the vertical growth through the cavity, for example because it is located exactly at the center. The latter could be the case when the size of the seeds is in the order of the cavity diameter. From both the cross-sectional TEM measurements in [49] and the results obtained with the bottle-shaped cavities, we know that the seeds are 20-50 nm in diameter as they were created during the explosive crystallization (XC) phase. Thus, since the grain filter diameter is in the order of 100 nm, in principle multiple seeds should be present in the unmolten portion. However, it could be that during XC through the cavity, some of the grains are occluded while at the same time no new grains start growing. If this 'downward occlusion' is not orientation driven, which is likely at the high growth rates during XC, this might lead to a very low number of randomly orientated grains present at the bottom of the cavity.

An additional factor in the absence of texture is of course the defect creation: grains with an orientation different from the original seed will start to grow. However, even when only very few planar defects were present, for instance with planarized grain filters and thick films, no texture was observed. Figure 5.11 shows an EBSD scan of a grid of planarized 1.0 μm grain filters with a ~250 nm Si film. Zero solutions and grain boundaries other than Σ3, Σ9, or Σ27 are highlighted. Very few islands were found to be completely free of planar defects although the majority was found to be free of random grain boundaries. Thus, the absence of etched defects in the SEM images is misleading, as defects are often present. The fact that they were not, or hardly, etched, however, confirms their low defect-density. The ratio between Σ3, Σ9, and Σ27 grain boundaries was found to be similar to that found with non-planarized grain filters with a 150 nm silicon film.

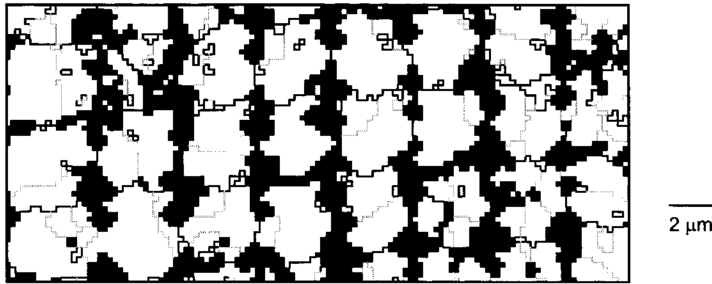


Figure 5.11. Results of an EBSD scan of a 3 μm grid of planarized 1.0 μm grain filters with ~250 nm silicon irradiated at 470°C and 1.65 × E_{CM}. This map shows the Σ3, Σ9, and Σ27 boundaries in gray and the other grain boundaries and zero solutions in black (same settings as Figure 5.10 (d)).

ORIGIN OF THE PLANAR DEFECTS

As was already suggested by the SEM images in Figure 5.5, the majority of defects seem to be created during growth rather than that they originate from the seeds. The top-view TEM image shown in Figure 5.12 shows four islands grown in a 150 nm thick film from a 3 μm grid of non-planarized grain filters. The grain filters can be seen as dark spots in the center of each island. This image confirms that many of the defects are created in the close proximity of the grain filter and that they are often special grain boundaries.

Cross-sectional TEM analysis was performed to investigate the vertical growth stage and the origin of the planar defects. 150 nm Si non-planarized grain filters were irradiated with the Microlas system with a ~155 ns pulse at 0.83 × E_{CM}, 1.17 × E_{CM}, and 1.5 × E_{CM}, respectively. From these three samples, cross sections were obtained from 1.4 μm, 1.0 μm, and 1.4 μm grain filters, respectively. Also, 0.8 μm planarized grain filters were investigated.

Figure 5.13 shows the cross section of a 1.4 μm grain filter irradiated at 0.83 × E_{CM}. As this sample was irradiated below the complete melt threshold, the film has a stratified microstructure: the bottom layer is the remainder of the explosive crystallization (XC) and the top layer is the small-grain poly-Si layer that grew epitaxially on the XC layer. The thickness of the small-grain poly-Si layer is thinner at the grain filter. This is most likely due to the surface being sloped at this position, as a result of which less energy is absorbed per unit area. Also, as the melt duration was very short, no reflow is observed.

From the cross sectional TEM research on non-patterned a-Si films in [49], it was found that a 200 nm silicon film could completely be crystallized during XC at an energy density below the surface melt threshold. In other words, the quench rate of the explosive crystallization was very low. In the grain filter, however, it is seen that

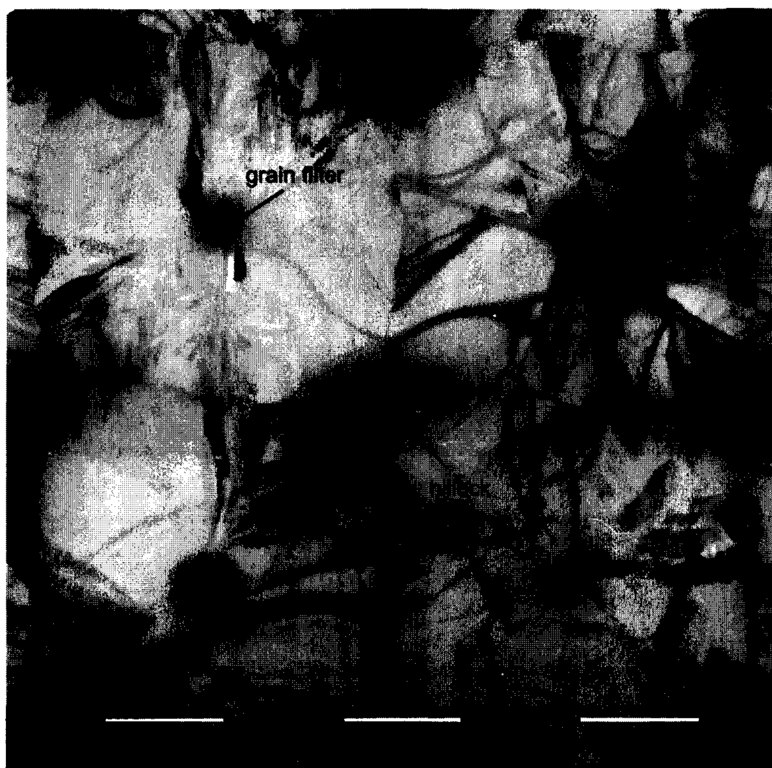


Figure 5.12. Top-view TEM image of four islands grown in a ~150 nm Si film from a grid of 3 μm spaced non-planarized grain filters. The sample was irradiated at room temperature and with a ~155 ns pulse.

the XC is quenched very rapidly: even though the film is irradiated above the surface melt threshold, the XC layer hardly extents into the cavity. Apparently, the cooling rate is increased due to lateral heat flow to the colder SiO_2.

Figure 5.14 shows a cross section of a 1.0 μm grain filter irradiated at 1.17 × E_{CM}. Again, only a small part of the silicon column is explosively crystallized, most of which was melted during the remainder of the pulse. As a result of this, the seeds (i.e., the unmolten portion) could hardly be distinguished from the epitaxially grown silicon. Still, it can be seen that even at this low energy density, a single grain grew from the top of the grain filter and seeded the lateral growth. During the growth around the corners of the cavity, however, defects were created. These are the defects that were also observed in the top-view SEM images.

Below the explosively crystallized silicon, a large amorphous part of the column remains. It can be seen that even though the walls of the cavity were very steep, the filling of the cavity was almost complete and only a very small void remained. This image also shows that the surface indentation was almost completely reflown at this

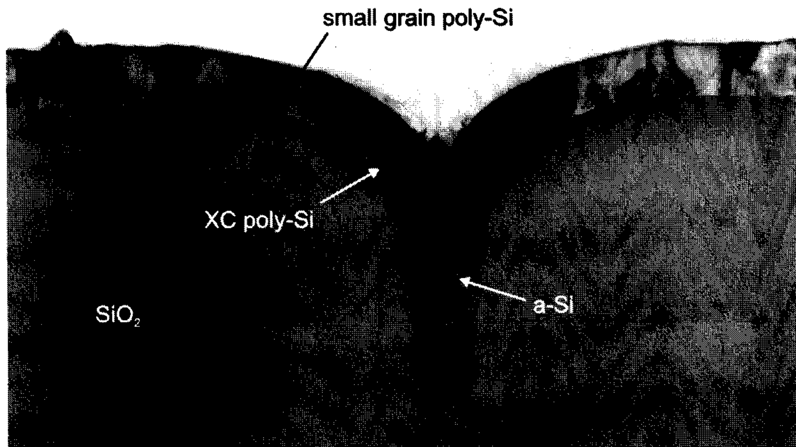


Figure 5.13. Cross sectional TEM image of a 1.4 μm grain filter with a 150 nm silicon film irradiated at 0.83 × E_{CM}.

relatively low energy density. The ridge that was created by collision with the island grown from the next grain filter is relatively low. It should be said, however, that the height of this protrusion increased closer to the corner of the island and that the hillocks at the corners of the islands could have a height exceeding the film thickness.

The images in Figure 5.15 show bright field and dark field pictures of a 1.4 μm grain filter irradiated at 1.50 × E_{CM}. The silicon column is completely crystallized and no a-Si remained. From the heat-flow simulation results presented in Section 5.3.3, it can even be concluded that no explosively crystallized silicon remained either or, in other words, that the silicon column was completely molten. Due to the large diameter of the cavity, a lot of heat is transported downwards and melt is very deep compared to narrower grain filters. As the column still remains somewhat cooler than the film, nucleation is most likely to start near the bottom of the cavity. As such, the small-grain material seen close to the bottom in this TEM image is thought to be from nucleated solid. The dark-field image shows clearly that during vertical regrowth, one of two vertically growing grains was occluded. At the same time, however, many defects were created. Again, most defects originate on the walls and the corners of the cavity.

The TEM image shown in Figure 5.16 shows a cross section of a planarized grain filter with a 250 nm film irradiated at 1.79 × E_{CM}. The original hole diameter before second SiO_2 deposition was 0.8 μm and the surface was planarized by CMP. As can be seen, close to the top the walls were inwardly sloped and filling was not complete. As a result, the liquid Si in the cavity agglomerated during the process. From the image, it looks as if the silicon became discontinuous (i.e., no longer in contact with

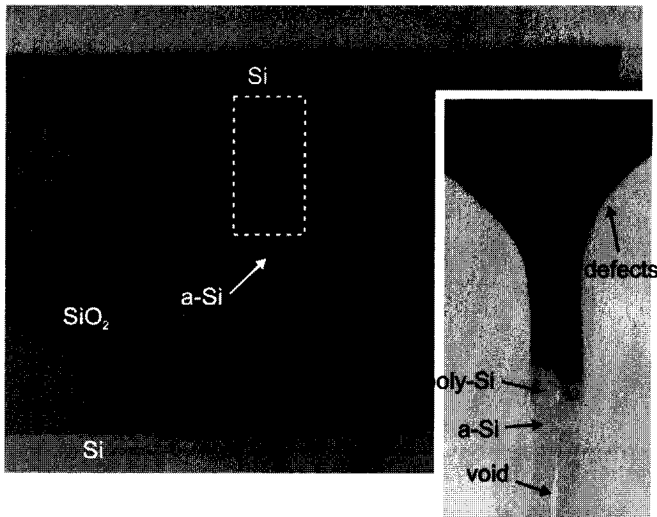


Figure 5.14. Cross sectional TEM image of a 1.0 μm grain filter with a 150 nm silicon film irradiated at 1.17 × E_{CM}.

the solid part of the column). The orientation of the grain below and above the upper void, however, was found to be equal and apparently, the connection between these two was removed during sample preparation. Analysis revealed that the orientation of the seed was very similar to that of the island. The defects that were created during the early stage of lateral growth were shown to be sub-grain boundaries.

From the cross-sectional TEM images, it can be concluded that grain filtering was indeed successful, even at low energy densities. It seems, however, inevitable that defects are created, mostly at the rim of the grain filter. When the diameter of the grain filter is large, the silicon in the cavity may melt completely and consequently growth starts on nucleated solids. Despite this, grain filtering could still be successful, although the seed remained highly defective, so that the island still contains more defects than if the growth started on an unmolten portion.

5.3.3 Melt Depth and Interface velocity

Three-dimensional heat-flow simulations were used to investigate the melt and regrowth processes in and around the grain filter. The model was briefly discussed in Section 3.3. Due to the fourfold symmetry of the domain, we simulated only one quarter of the grain filter. Melting and regrowth were investigated as a function of various parameters and in addition to this, the diameter of the island (twice the lateral growth distance) was recorded. Island diameter, however, is determined by the location of nucleation events as well and therefore cannot be simulated reproducibly. To get an impression of the island diameter, we looked at the diameter during the

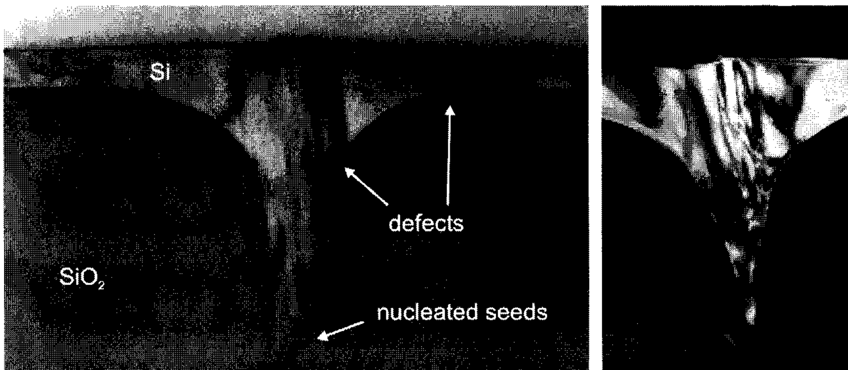


Figure 5.15. Cross sectional TEM images of a 1.4 μm grain filter with a 150 nm silicon film irradiated at 1.50 × E_{CM}. Left, a bright field image and right a dark field image.

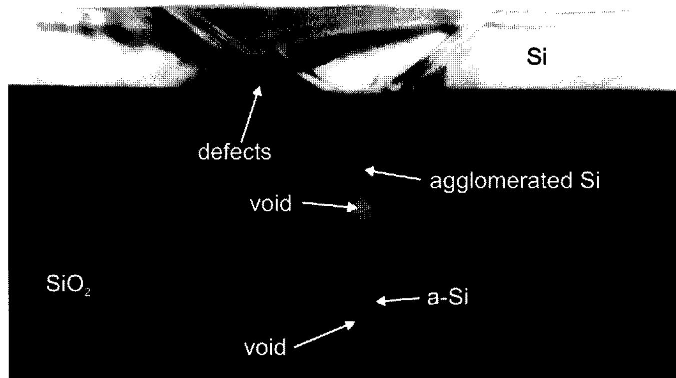


Figure 5.16. Cross-sectional TEM image of a CMP planarized grain filter with an original diameter of 0.8 μm. Si film thickness is 250 nm and the sample was irradiated at 1.79 × E_{CM} at 470°C.

(approximate) onset of nucleation of the surrounding film (i.e., at the end of the lateral-growth time interval Δt_{LG}). This nucleation time, t_{nucl}, was determined from 3-dimensional simulations with a very small node size. Both from experiment and simulation, it is known that lateral growth after t_{nucl} can be as much as 1 μm, depending on film thickness and irradiation conditions. Thus, in that case, approximately 2 × 1 μm must be added to the diameter at t_{nucl} to obtain the final island diameter.

Figure 5.17 shows an example of top-view snap shots of the status of the nodes closest to the Si–SiO_2 interface at different instants. Nodes can be either liquid or

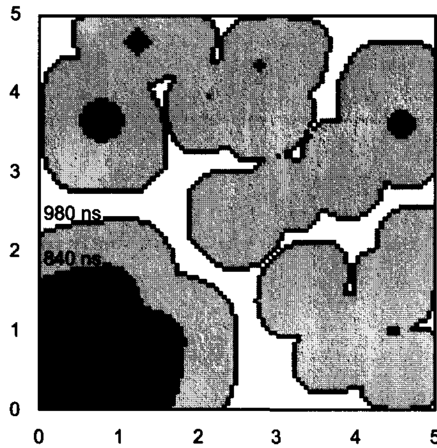


Figure 5.17. Various stages in the lateral growth from a grain filter in the lower left corner as seen from the top of the 3D grid. The instants at which the growth front is shown are 560 ns, 700ns, 840 ns, and 980 ns, respectively. Nucleation started around 820 ns.

solid or a combination of liquid and solid. The latter are called slush nodes and are the nodes that contain the solid–liquid interface. It can be seen that after ~1 μm of lateral growth the growth front become instable: the island becomes clover-shaped. In the model, all material properties are considered to be isotropic and therefore the growth front should be circular.

VERTICAL GROWTH STAGE

The vertical growth stage was investigated with a grid that had $10 \times 10 \times 15$ nm^3 nodes in the cavity and larger nodes in the surroundings. Figure 5.18 shows examples of growth fronts during regrowth for different grain filters and different conditions with 20 ns intervals. From these simulations, it appears that at least for diameters up to 200 nm the growth front is basically planar, thus, the requirement for occlusion to occur seems to be satisfied.

Figure 5.18 (a) and (b) show the growth front in a planarized and a non-planarized grain filter, respectively. Film thickness is 150 nm and the cavities were 750 nm deep, so that the bottom lies 750 + 150 = 900 nm below the surface of the film. The non-planarized grain filter had a rim curvature of ~490 nm and a planar silicon surface (i.e., no indentation at the surface). It was found that the melt depth increases with increasing rim curvature, whereas maximum interface velocity remains virtually constant. As was reasoned in Section 5.1, however, the increased melt depth does not lead to improved filtering, as filtering is only expected to occur below the curved rim. Figure 5.19 (a) shows both melt depth in the center of the cavity and the island diameter at t_{nucl} as a function of rim curvature. The rim curvature has only a marginal

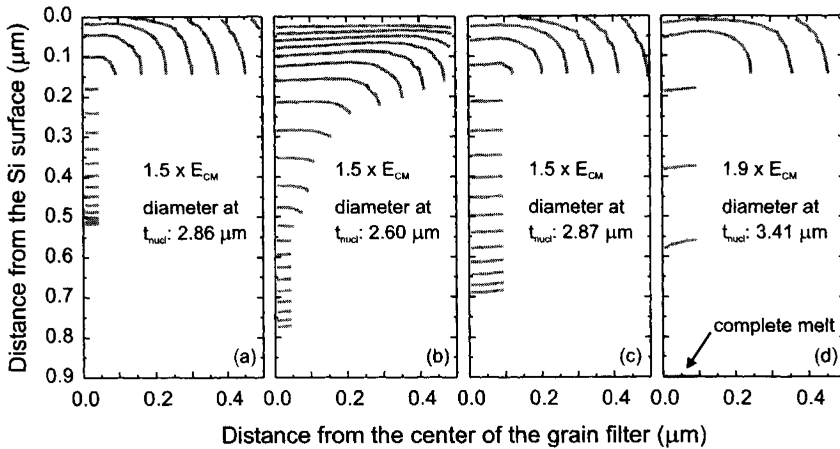


Figure 5.18. Growth fronts during the vertical regrowth and the onset of the lateral growth with 20 ns intervals. All examples have a 150 nm silicon film and were irradiated with a ~115 ns lognormal pulse. (a), a planarized 100 nm grain filter, (b), a non-planarized 100 nm grain filter with a ~490 nm rim curvature, (c), a planarized 200 nm grain filter, and (d) the same structure irradiated with higher energy density.

effect on island diameter. In practice, however, the reflow of silicon may cause the effect to be stronger as there is an inward transport of silicon as was already discussed in Section 5.3.1.

Figure 5.18 (c) and (d) show the growth fronts in a 200 nm wide planarized grain filter irradiated at 1.5 × E_{CM} and 1.9 × E_{CM}, respectively. A comparison of Figure 5.18 (c) with Figure 5.18 (a) shows that the melt depth increases with the diameter of the cavity. In general, heat flows laterally from the surrounding liquid silicon towards the grain filter and subsequently flows downwards through the grain filter where it is lost laterally to the surrounding SiO_2. For increasing cavity diameter, both the downward heat flow and the lateral heat loss are expected to increase. Apparently, however, the downward heat flow increases more than the lateral heat loss. The melt depth is shown as a function of normalized energy density, that is E/E_{CM}, in Figure 5.19 (b). It can be seen that the melt depth in the 200 nm cavity increases more rapidly with energy density than that in a 100 nm cavity. At 1.9 × E_{CM}, the silicon in the 200 nm cavity is completely melted, as can also be seen in Figure 5.18 (d). Growth started on a nucleated grain somewhere close to the bottom of the cavity and vertical interface velocity was ~10 m/s. Figure 5.19 (b) shows that at this energy density, the island diameter suddenly drops compared to that obtained with a 100 nm grain filter. This agrees well with what was found experimentally (Figure 5.6).

Figure 5.19 (c) and (d) show the melt depth and the island diameter at t_{nucl} as a function of substrate temperature and pulse duration, respectively. These graphs

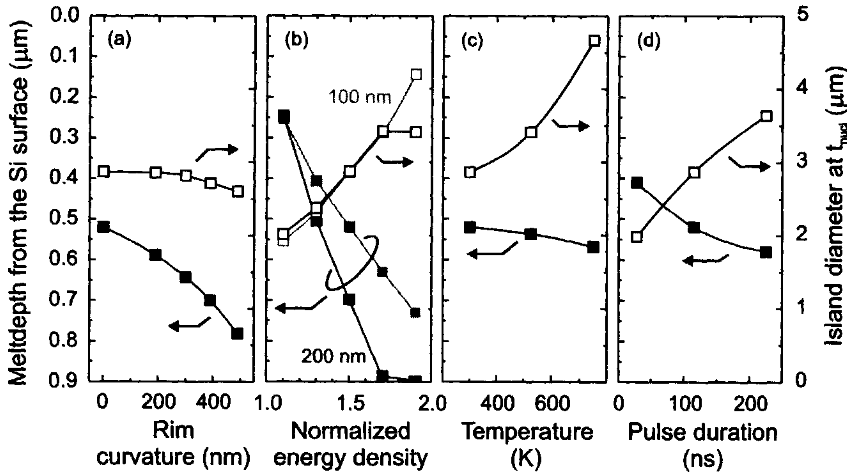


Figure 5.19. Black dots show the meltdepth in grain filters of which the bottom lies 900 nm under the silicon surface so that cavities were 900 – 150 = 750 nm deep. White dots show the diameter of the island grown from these grain filters.

show the melt depth and island diameter at 1.5 x E_{CM}. It should be noted that E_{CM} of course decreases with substrate temperature and increases with pulse duration. For both substrate heating and pulse duration extension, melt depth is seen to increase only marginally, whereas the island diameter increases significantly.

LATERAL GROWTH STAGE

Growth rate has an important influence on defect creation, as was discussed in Section 2.2.2. The interface velocity along the Si–SiO_2 interface both in and around the grain filter as a function of the lateral distance from the grain filter is shown in Figure 5.20 for various parameters. In each graph, results are compared with one single simulation of a 100 nm planarized grain filter irradiated at room temperature with a 115 ns pulse and a 150 nm thick film. Figure 5.20 (a)–(d) show the interface velocity in planarized grain filters for various conditions. As long as pulse duration, energy density, and film thickness are not too small, peak velocity is always experienced on the corner of the cavity. The influence of the various parameters, substrate heating, pulse duration, energy density, and film thickness, is as expected: interface velocity goes down as cooling rate goes down.

Figure 5.20 (e) shows the interface velocity from a non-planarized grain filter with a rim curvature of ~490 nm. Compared to the planarized grain filter, the peak velocity is experienced further away from the center of the grain filter. Due to the rotational symmetry of the design, this implies that peak velocity is experienced over a larger area. If defect creation is indeed related to interface velocity, this would indicate why planar defect density is higher for non-planarized grain filters.

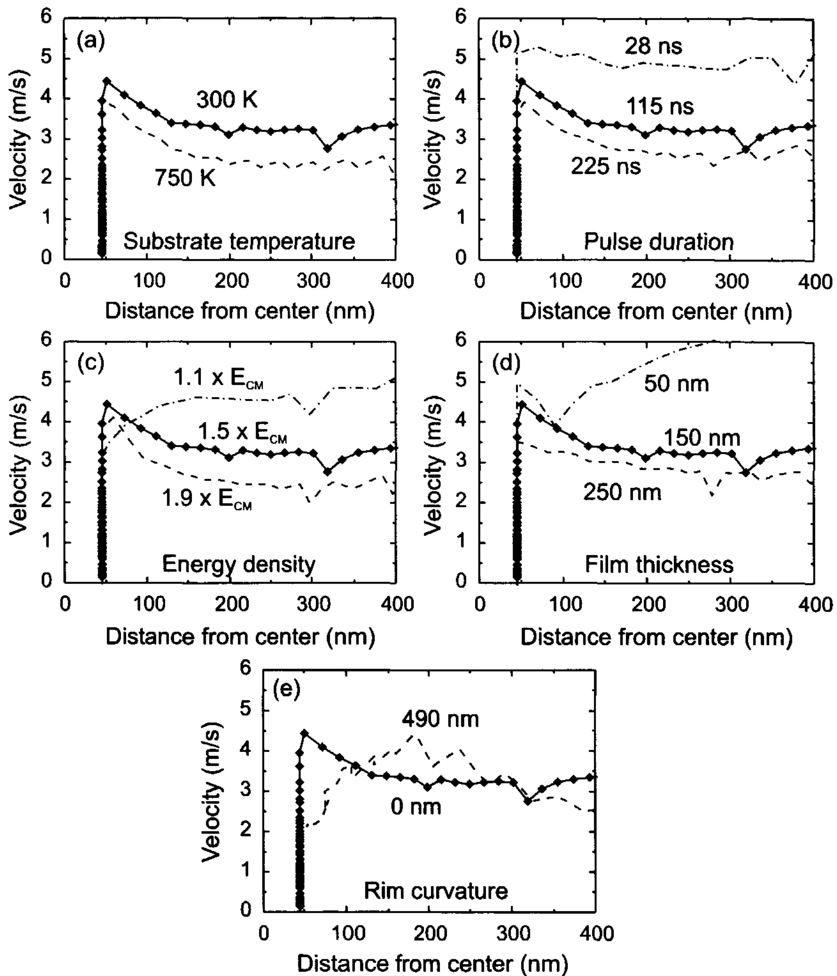


Figure 5.20. Growth-front velocities along the Si–SiO_2 interface as a function of the distance from the center of the grain filter. Each graph shows the effects of one of the parameters on velocity compared to a sample with 150 nm silicon irradiated at 1.5 × E_{CM} with a 115 ns pulse at room temperature.

5.4. Discussion and Conclusions

From the experimental results presented in this chapter it is clear that the embedded-seed structure lead to C-SLG. For bottle-shaped cavities, however, the energy density window is still very small due to the presence of a large void. The U-shaped cavities, on the other hand, were shown to have an energy density window that could extend

up to the critical energy density for agglomeration of the surrounding film. Also, through the concept of grain filtering, grain-location control could also be obtained.

Despite the successful filtering of a single seed for lateral growth, the islands almost always contained planar defects. Although electron backscatter diffraction (EBSD) measurements were limited in resolution, it could still be concluded that the majority of high-angle grain boundaries within the islands were $\Sigma3$, $\Sigma9$, and $\Sigma27$ grain boundaries and that very few sub-grain boundaries were observed. Also, even though the total number of planar defects decreases with film thickness, cavity diameter, and rim curvature, the relative distribution stays the same. Compared to other crystallization methods, this distribution is preferred as fewer defects are present. For example, samples irradiated with multiple pulses in the SLG regime also contained many $\Sigma5$, $\Sigma7$, and $\Sigma11$ boundaries besides the predominant $\Sigma3$ and $\Sigma9$ boundaries [98]. In directionally solidified films with the sequential lateral solidification (SLS) method, on the other hand, many sub-grain boundaries were found and $\Sigma3$ boundaries were less dominant [62]. It should of course be noted that the grain boundaries between the islands grown from grain filters were not included in this analysis. These are likely to be random high-angle grain boundaries having high defect density. In contrast to SLG and SLS processed films, however, the grain-filter process allows TFTs to be positioned within one island, so that these random grain-boundaries are not present within the active channel. It is therefore justified to conclude that grain-filter processed films have a preferential grain boundary distribution in terms of defect density.

The TEM analysis revealed that the majority of these planar defects were created at the rim of the cavity and that only few originated from the seeds at the bottom of the cavity. When all the silicon in the cavity was melted, however, many defects also originated from the vertical growth stage, which occurred at velocities exceeding 10 m/s. In Section 2.2.3 it was already mentioned that at these velocities, growth could be defective depending on crystallographic orientation [59]. Also, when the film is very thin, additional defects were created during the lateral growth. These were related to the thermal stresses in the film during solidification [61].

The exact nature of the defect creation at the rim of the cavity is not understood. Similar defects were observed in bridging epitaxy: poly-Si was deposited on an SiO_2 layer that contained openings to the silicon substrate and subsequently, the poly-Si layer was molten so that grains grew epitaxially from the c-Si [104]. At the corners of the openings, however, defects were created. The defect creation at the rim of the grain filters could be partially suppressed by sharpening the corners of the cavities by a planarization process. From the heat-flow simulations it was found that peak interface velocity occurred at the rim of the cavity. This could indicate that the defect creation mechanism is similar to that observed at high-velocity regrowth of a partially molten silicon layer [59]. The heat-flow simulations, however, showed that

interface velocity at the rim was around 4 m/s, which is still less than the reported critical velocities for defect creation in partially melted silicon films. Possibly, the critical velocities for defect creation are lowered when growth is along an SiO_2 interface. When the rim is curved, peak velocity is experienced over a larger area, which could increase the number of defects formed. Also, as critical velocity is dependent on crystallographic orientation and as the crystal orientation changes gradually with respect to the interface, there is a good chance that somewhere during growth the velocity exceeds the critical velocity for defect formation. This could explain why fewer defects were created when the rim was sharp.

The EBSD analysis also showed that, even when few planar defects were created, no texture was obtained with the grain filter method. Whether this is due to the absence of multiple seeds or the lack of influence of crystallographic orientation on the occlusion mechanism could not be concluded.

The heat-flow simulations revealed that the abrupt decrease in island quality observed above a certain energy density, could be related to the complete melt of the silicon column. The melt depth was found to be a strong function of cavity diameter and rim curvature. Substrate heating and pulse duration extension, on the other hand, only had a marginal effect on melt depth. The island diameter, however, was seen to increase drastically for these parameters, whereas no significant improvement in island quality was observed. From these two ways to enhance the island diameter, substrate heating was the preferred method, because less laser energy is needed to completely melt the film and no laser energy is wasted with optical components. In addition, the thermal stress in the film that was created due to the difference in thermal expansion coefficient between Si and SiO_2 was less with substrate heating.

CHAPTER 6

Properties of Thin-Film Transistors

From the results presented in Chapters 4 and 5 it was found that only the grain filter method led to a high yield of grain-location control. In this chapter the results are presented of devices made within the islands grown with the grain filter method. Also, a comparison is made with devices made in small-grain poly-Si, in directional poly-Si, and in c-Si films. It is found that device properties of the grain filter TFTs (GF-TFTs) can be close to the best-case scenario, that of c-Si TFTs. It is also found, however, that device uniformity is poor.

6.1. Introduction

From the different sets of transistors that were shown in Table 3.1, we found that only few showed regular transistor behavior. For the others, two irregularities could be discerned, one in the off-state and the other in the on-state of the device:

1. High off-current regardless of V_G. This effect was observed with almost all samples crystallized with the XMR system at 470°C (sets 3–8 in Table 3.1). The complete-melt crystallization TFTs (CMC-TFTs) were the exception. For the samples crystallized with the Microlas system, it was found that leakage current scaled drastically with increased film thickness and with increased channel width.
2. Low on-current for small V_D. This effect was observed mainly for 100 nm thick films and much less for 150 nm thick films. For 250 nm thick films, this anomaly was absent.

These irregularities will further be discussed in Section 6.2. The consequence was that a full set of data could only be obtained for those devices made in 100 nm or 150 nm thick films crystallized with the Microlas system (sets 1, 2, and 9 in Table 3.1)

and for the SIMOX-TFTs. Especially for the 100 nm films, however, many transistors had a low on-current and therefore statistical significance of the data was affected. Due to the failure of so many devices, the following could not be investigated:

1. The influence of the rim curvature on the device properties. Both the planarized and the non-planarized grain filters with ~250 nm thick films (sets 4 and 7) had high off-current.
2. The influence of the thermal oxidation on the material properties. The three sets of transistors that were made to investigate this (sets 3, 5, and 6) were all crystallized with the XMR system and had high off-current.
3. The influence of grain-location control on the device uniformity. The partial-melt crystallization TFTs (PMC-TFTs; set 8a) that were expected to show non-uniformity due to the random location of the large grains also had a high off-current.
4. The influence of crystallographic orientation on device uniformity. The ~20 μm wide TFTs with 7 islands grown from grain filters had a high off-current. A comparison of the device uniformity of one-island GF-TFTs and that of seven-islands GF-TFTs could have indicated what the nature of possible non-uniformities was.

Also, a proper comparison with earlier work could not be made as those GF-TFTs were all made in ~250 nm thick films [105, 90]. Nevertheless, from the data obtained, a comparison could be made with other crystallization methods and with the perfect crystalline TFTs (the SIMOX-TFTs). For the 150 nm thick GF-TFTs, the influence of grain filter diameter and energy density could be investigated. Also, the influence of a single location-controlled grain-boundary could be investigated. These results are presented in Section 6.3.

6.2. Irregularities in TFT Characteristics

As was mentioned in the introduction to this chapter, two different irregularities were observed in behavior of the crystallized transistors. These are both visible in the transfer characteristics of a matrix of SLS-TFTs shown in Figure 6.1. As width and length of the channel region varied over the matrix, the dependence of the irregularities on these parameters can also been seen. In this section we investigate the nature of the anomalous behavior and discuss whether it is related to material properties (i.e., the crystallization) or to transistor fabrication.

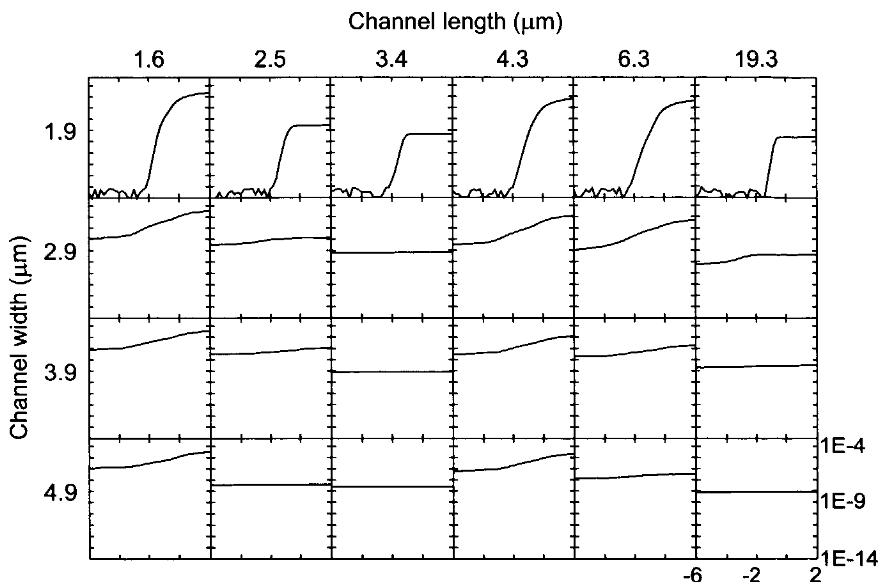


Figure 6.1. Transfer characteristics at $V_D = 0.2$ V of a 6×4 matrix of 100 nm thick SLS-TFTs with a spacing of 360 μm.

OFF-STATE ANOMALY

For the samples crystallized with the Microlas system, the off-current scaled drastically with increased width and with increased thickness of the channel. The leakage did not depend on the crystallization method: off-currents were similar for both GF-TFTs and SLS-TFTs. For a ~1.6 μm long GF-TFT in 100 nm thick Si, it was found that although the off-current was still below the detection limit (~10^{-14} A) for a channel width W of ~1.9 μm, it increased to ~10^{-11} A for $W \approx 2.9$ μm. For a 150 nm thick silicon film, the off-current even increased to ~10^{-9} A. To a certain extent, the leakage could be suppressed by applying a negative bias to the substrate; an example is shown in Figure 6.2. This indicates that the anomalous off-current is due to the presence of a back channel that can be turned off by applying a negative substrate bias.

A similar effect was observed elsewhere where it was concluded that the back channel was induced by positive charges in the underlying oxide [106]. The leakage current could be suppressed by passivating defects with hydrogen. In the research presented in this thesis, however, the TFTs showed very high gate leakage as a result of hydrogenation. Since thermal SiO_2 is not prone to deterioration during hydrogenation, the leakage cannot be created by the gate dielectric. Most likely the passivation SiO_2 that lies between the gate and the channel both at the source and the drain is the cause of the leakage (see the cross section parallel to the current flow in

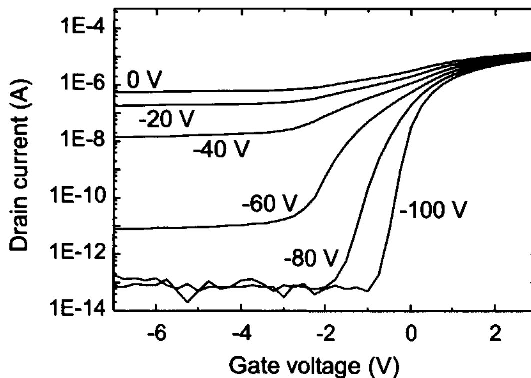


Figure 6.2. Transfer characteristics of a W/L = 3.9/3.25 μm, ~150 nm GF-TFT at various values of the substrate voltage as indicated at the lines.

Figure 3.19). In any case, because of the gate leakage, a possible reduction in the back channel could not be observed.

With the samples crystallized with the XMR system, the effect was even stronger than with the Microlas system and the ~1.9 μm TFTs also had high off-current. Again, the effect occurred regardless of the crystallization method, although much less so for the CMC-TFTs. This may be due to the small grain size of this material and hence the low conductivity. One of the wafers with grain filters contained both TFTs that were crystallized with the Microlas system and that were crystallized with the XMR system. For these devices, the only differences were the substrate temperature, the pulse duration, and the ambient during crystallization. Still, the leakage current for $W \approx 1.9$ μm devices was higher than for those crystallized with the XMR system. It is not understood what exactly the influence of these parameters on the back channel is. In any case, applying a maximum substrate bias of −100 V was not sufficient to suppress the back channel for the samples irradiated with the XMR system.

The back-channel leakage current was absent in earlier experiments [105]. In those experiments, the source and drain activation was performed at energy densities well below the energy density for complete melt E_{CM} (0.3 mJ/cm^2 for ~250 nm thick films), whereas in this research energy densities close to E_{CM} were used. At this condition, only a small top part of the film is actually melted and therefore high activation efficiency is only achieved close to the surface. Below the surface layer, activation efficiency will be much less, and in addition to that, the film may be very small-grain explosively crystallized poly-Si or even amorphous. Then, if a back channel is present, it may be that there is a high series resistance between the back channel and the source/drain contacts, so that current is negligible.

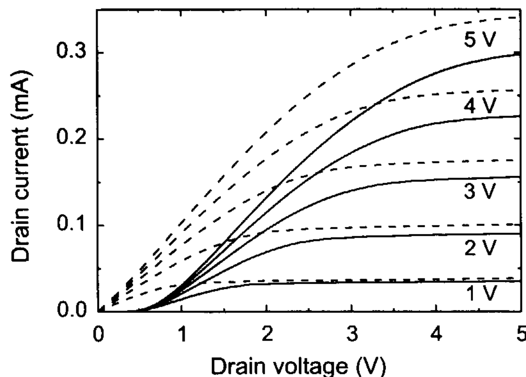


Figure 6.3. Output characteristics of two W/L = 1.9/2.6 μm, ~100 nm SIMOX-TFT at various gate voltages indicated in the graph.

ON-STATE ANOMALY

In Figure 6.3 the output characteristics of a device with low on-current at low V_D are shown in comparison with those of a regular device. Apparently, for the devices with low on-current, there is a barrier for the current flow. This so-called current crowding is related to the presence of a series resistance between channel and source/drain contacts, for example a contact resistance [107]. In the research presented in this thesis, however, contact resistance was less than 10 Ω for 4 × 4 μm^2 contacts, so we exclude this possibility.

From the matrix of output characteristics in Figure 6.1 it can be seen that the devices with low on-current were not randomly distributed. Instead, they seem to be periodically arranged in columns. The periodicity was found to be similar to the translation distance of the laser pulse during S/D laser activation. Such a dependence on activation energy was observed before in excimer-laser crystallization of thin a-Si films for making low-ohmic poly-Si resistors [108]. In this work, it was found that the sheet resistance could be substantially higher when the first pulse came from the ramped edge of the laser pulse. The first pulse is important, as, because of the amorphous nature of the silicon, more heat will be absorbed. Also, more latent heat is associated with the amorphous film and as a result, the melt will be deeper than during the subsequent pulses. When the first pulse is at a lower energy density (e.g., when it is from the ramped edge of the pulse), however, this may not be the case. As a result, those areas that were first irradiated with the edge of the laser pulse might experience less efficient dopant activation than other areas. Also, the final grain size may be smaller when the first pulse was at lower energy density.

Still, this lower activation efficiency and the smaller grain size are not expected to cause a significant increase in sheet resistance, as the doping concentration of the S/D regions is very high [95]. This is confirmed by the absence of current crowding

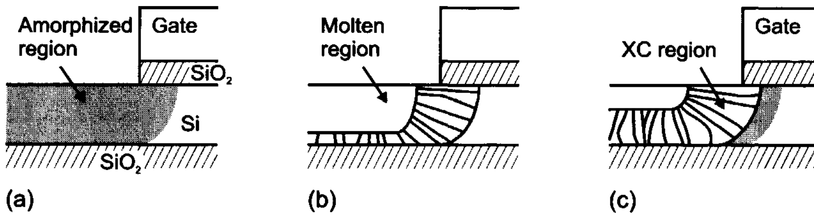


Figure 6.4. Schematic drawings of the channel region around the gate (a) after implantation, (b) during laser activation with a high energy density, and (c) during laser activation with a low energy density.

in earlier work in which lower activation energy was used [105]. Closer to the gate, however, the situation might be different. During implantation, the silicon was most likely partially or completely amorphized, depending on the film thickness. Due to lateral implantation, this amorphous region extended partially under the gate, as is shown schematically in Figure 6.4 (a) [93]. As implantation conditions were the same regardless of the film thickness, the extent of this region is basically the same for all TFTs. During laser activation this region is not irradiated as it is protected by the aluminum gate. The extent to which it is recrystallized thus depends on the amount of lateral heat flow during activation or, in other words, on the laser energy density. The aluminum gate, however, will act as a heat sink during this process, as it is separated from the silicon by just a 34 nm layer of SiO_2 (i.e., the gate dielectric).

The activation energy density was chosen to be close to E_{CM} and thus depended on film thickness. As a result, the lateral heat flow and consequently the lateral recrystallization distance varied with film thickness. It could therefore be that when the film is thin, the lateral damage under the gate will not fully anneal. However, since many of the 100 nm TFTs did not show current crowding, it can be concluded that the recrystallization distance was large enough to complete anneal all amorphized material. This situation is shown schematically in Figure 6.4 (b).

When the first pulse is at a lower energy density, however, the recrystallization distance will be less and some a-Si remains. During the subsequent pulses, the amorphous region may not be completely recrystallized as less heat is absorbed and less latent heat is released. When, in addition to this, the film was amorphized throughout during implantation, this amorphous region will extend throughout the thickness of the film. This situation is shown in Figure 6.4 (c). Unlike highly doped small grain poly-Si, the sheet resistance of highly doped a-Si is several orders of magnitude higher than that of c-Si [93]. This amorphous layer will therefore have a high resistance and form a barrier for the current. This situation is similar to that observed in inverted-staggered a-Si:H TFTs where the current has to cross the intrinsic film to get from the source/drain contacts to the channel [109]. It was found that the current through this region was space-charge limited and this current

mechanism scales with ~V^2 [110]. Thus, at higher V_D, the barrier for the current will be less. We conclude that the non-linear resistance that results from this amorphous region is the cause of the current crowding observed in the

In the case of current crowding, the field-effect mobility does not give a good impression of the actual carrier mobility, as it is determined at $V_D = 0.2$ V. For example, the SIMOX-TFT with and without series resistance had a $\mu_{FE,pk}$ of 24 and 670 cm^2/Vs, respectively. Effective mobility, on the other hand, was determined at a set value of $V_G - V_T$ and for a variable value of V_D between 0 and 1 V. The values of the effective mobility at $V_G - V_T \approx 1$ V are 303 and 527 cm^2/Vs, respectively. Apparently, even for high V_D, the current barrier does not become negligible.

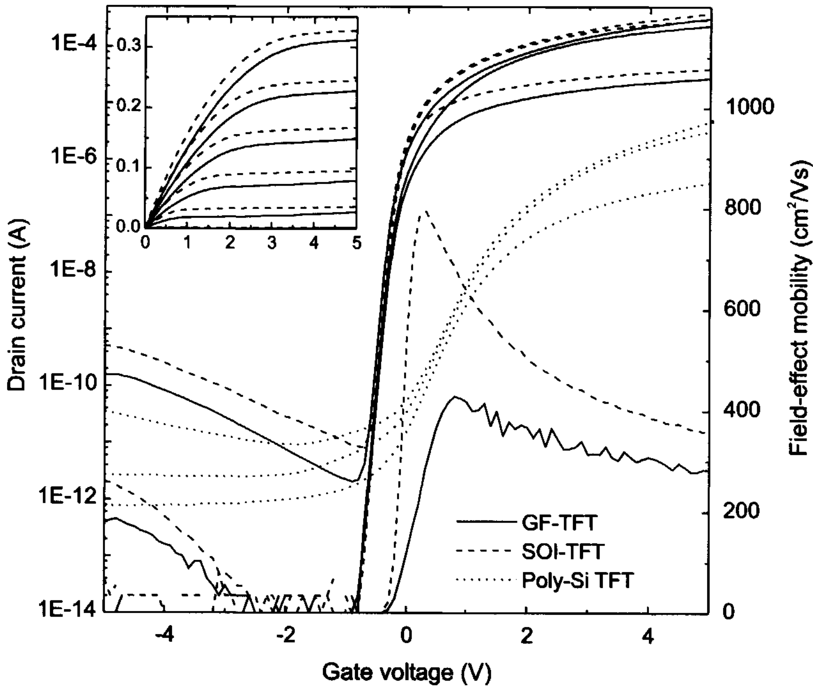
6.3. TFT Characteristics

In this section, the properties of the regular TFTs are discussed. The sets of TFTs that showed regular behavior, however, also contained many devices that displayed current crowding. To distinguish between regular and irregular devices, a selection was made based on the on-current at low V_D. Only those devices of which $I_D > 10^{-6}$ A at $V_G >> V_T$ and $V_D = 0.2$ V were considered. Some devices that showed only little current crowding were thus still included and consequently, statistical data may be affected.

6.3.1 Grain-Location Controlled TFTs

Figure 6.5 shows both transfer and output characteristics of a typical GF-TFT, a typical SIMOX-TFT, and a typical CMC-TFT. In addition to that, the field-effect mobility is shown for the GF-TFT and the SIMOX-TFT. The μ_{FE} of the CMC-TFT is not shown, as it was found to be only ~12 cm^2/Vs at its peak. Application of a substrate bias (like in Figure 6.2) showed that a limited back channel was present in the CMC-TFTs that could be suppressed with a –20 V bias. The results shown in Figure 6.5, however, are without substrate bias and hence the off-current was one order of magnitude higher due to the back channel. All transistors had similar channel dimensions and a film thickness of ~150 nm. It can be seen that the characteristics of the GF-TFT approaches those of the SIMOX-TFT.

An overview of the various parameters is shown in the appended table. The field-effect mobility was calculated using values for W and L obtained from SEM analysis after channel patterning and gate patterning, respectively. It can be seen that the calculated $\mu_{FE,pk}$ of the SIMOX-TFT is somewhat high compared to commonly found values for MOSFET. This is most likely due an overestimation of L by the lateral implantation under the gate. The source and drain regions will extend over a value ΔL under the gate and the real channel length should then be $L - 2 \times \Delta L$.



	W/L (μm)	$\mu_{FE,pk}$ (cm²/Vs)	S (mV/dec)	V_T (V)
GF-TFT	1.9/2.35	429	82	0.14
SIMOX-TFT	1.9/2.5	797	67	-0.09
CMC-TFT	1.9/2.55	12	409	2.97

Figure 6.5. Transfer characteristics of a ~150 nm GF-TFT, of a ~150 nm SOI-TFT, and of a ~150 nm, >E_{CM}-ELC poly-Si TFT. I_D–V_G curves are shown for V_D = 0.2, 2.0, and 5.0 V, respectively. Also, the field-effect mobility of the GF-TFT and the SOI-TFT is shown as a function of V_G. The inset shows the output characteristics (I_D (mA) vs. V_D (V)) at V_G = 0, 1, 2, 3, 4, and 5 V, respectively, of the GF-TFT and the SOI-TFT.

The mobility of the GF-TFT is significantly less than that of the SIMOX-TFT. This may in part be due to the difference in crystallographic orientation. Below the mobility peak, mobility will also be degraded by the presence of deep states at the planar defects in the film [111]. As discussed in Section 1.1.4, according to the grain-boundary trapping model, this will lead to potential barriers that impede the flow of carriers. The presence of deep states is also reflected in the increased value of the subthreshold swing S. The influence of the grain-boundary potential barriers will decrease with increasing V_G.

Beyond the mobility peak, mobility may also be degraded by surface roughness or the presence of tail states [112]. The surface of the islands grown with the grain filter method, however, are very smooth, so that it can be concluded that the presence of tail states is the main cause of mobility degradation. The influence of tail states on the mobility was shown by hydrogenation experiments of SPC poly-Si TFTs where mobility was seen to increase substantially only when strained bonds were passivated, that is, for long hydrogenation time [14].

INFLUENCE OF GRAIN FILTER PROCESS

In those TFTs manufactured with the two-step grain filter process (i.e., non-planarized grain filters), influence of grain filter diameter and ELC energy density was investigated. The influence of grain filter diameter on μ_{eff}, S, and V_T of 150nm GF-TFTs is shown in Figure 6.6. Results are shown for three different values of the channel length. The decrease in mobility observed for shorter channel lengths was also observed for the 150 nm SIMOX-TFTs, albeit at much smaller scale. This decrease may be attributed to the series resistance between the TFT and the environment [90]. Although series resistance is expected to be low, it may have a significant influence at small channel length as it becomes comparable to the channel resistance. The calculation of mobility does not take in account the effect of series resistance and as a result it may appear lower. The difference between SIMOX-TFTs and GF-TFTs can then be attributed to the lower defect density of the SIMOX film and hence its lower series resistance.

The plot in Figure 6.6 shows that mobility decreases for increasing grain filter diameter and that both threshold voltage and subthreshold swing increase. At the same time, the threshold voltage and, to a lesser extent, the subthreshold swing increased. The step-like increase in V_T can be attributed to processing non-uniformities as it is seen to vary from left to right on the wafer; exposure time during patterning of the first SiO_2 layer increased from left to right on the wafer. These trends clearly confirm what was already seen from SEM observations: the number and the randomness of the defects in the islands grown with grain filters increases for increasing grain filter diameter. An abrupt decrease in properties that could be attributed to the complete melt of the silicon column, however, was absent. From the island diameter measurements in Figure 5.8, the complete melt condition could not be discerned either. Apparently, for thin films, the degradation of island properties as a function of cavity diameter is mostly due to the decreased filtering capabilities, rather than the complete melt of the silicon column.

TFTs were also made in 1.0 μm structures that were irradiated at a lower energy density: at $1.38 \times E_{CM}$ rather than $1.58 \times E_{CM}$. The effective mobility at $V_G - V_T \approx 3$ V for a TFT with W/L = 1.9/2.35 μm decreased from 270 ± 67 cm^2/Vs to 232 ± 53 cm^2/Vs. Also, the swing increased slightly from 100 ± 29 mV/dec to 109 ± 23

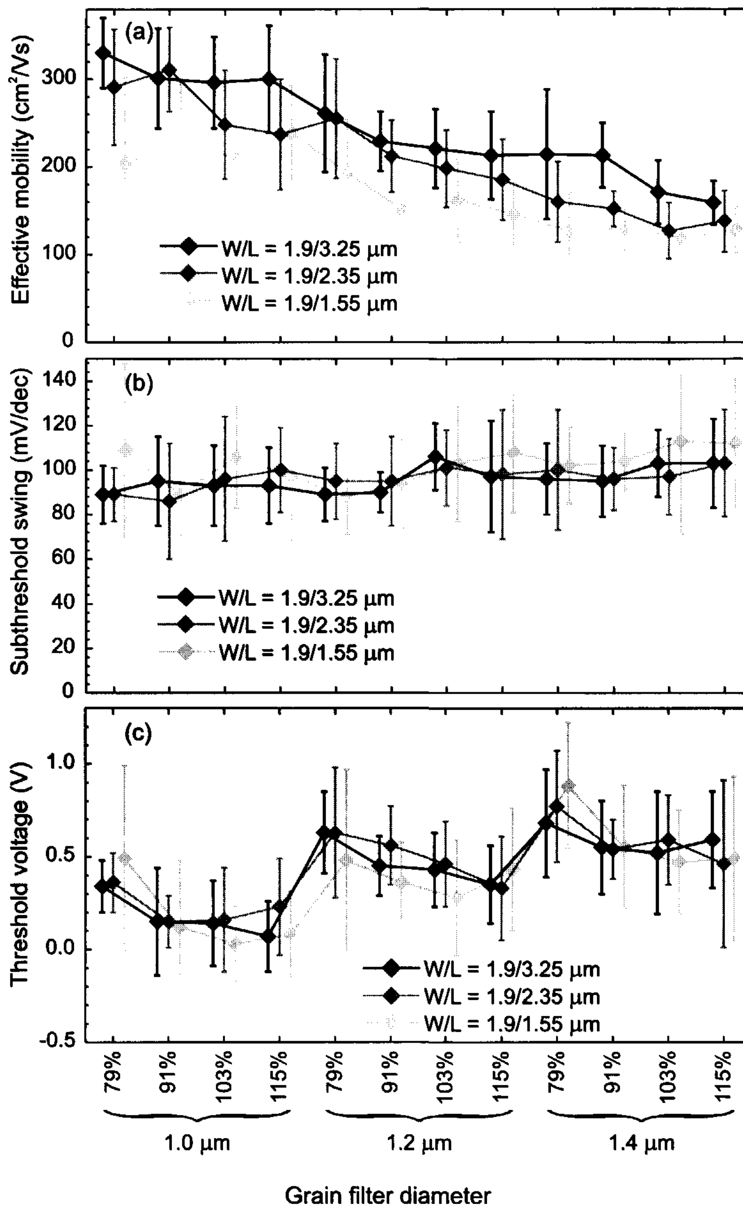


Figure 6.6. (a) The effective mobility at V_G–$V_T \approx 3$ V, (b) the subthreshold swing, and (c) the threshold voltage for a W = 1.9 μm and L = 1.55, 2.35, or 3.25 μm, ~150 nm GF-TFT as a function of grain filter diameter.

mV/dec. It can thus be concluded that a significant change in energy density gives a relatively mild change in transistor parameters.

6.3.2 Grain-Boundary-Location Controlled TFTs

The random crystallographic orientation of the islands grown with the grain filter method is expected to affect the device uniformity. A solution could be to make each channel region in a number of parallel islands from grain filters. This way, there will be random grain boundaries running parallel to the current direction. To judge the influence of the presence of such a grain boundary, TFTs with a single random grain boundary either parallel (//-TFTs) or perpendicular (⊥-TFTs) to the current flow were made. This was done by shifting the channel with respect to the grain filter grid.

GF-TFTS

Figure 6.7 shows the trends observed in μ_{eff}, S, and V_T for grain-boundary-location controlled GF-TFTs as a function of grain filter diameter. It is clear that for small grain filter diameters, a parallel grain boundary is much less detrimental to these parameters than a perpendicular grain boundary. By comparing the figure with Figure 6.5 (note that W/L = 1.9/1.55), it can be seen that the average mobility of the //-TFTs is higher than that of the ordinary GF-TFTs. Apparently, a parallel grain boundary could even be beneficial for the above-threshold behavior of a device. Also from this comparison one can see that V_T is lower for //-TFTs, and higher for ⊥-TFTs. The latter is due to the potential barrier associated with the grain boundary [113]. The former could indicate that a current path can be created along the grain boundary at a slightly lower V_G than through the grain. This could, however, also lead to increased off-current, although at V_D = 0.2 V, off-current was still below the detection limit.

The average effective mobility is shown for two different values of the gate voltage. When V_G is increased, μ_{eff} is expected to decrease due to the increased vertical field and the associated scattering. This was indeed observed for the SIMOX-TFTs. For both the //-TFTs and the ⊥-TFTs, however, such a trend is not observed; the latter even showed an increase for increasing V_G. This behavior indicates the presence of grain-boundary potential barriers in the channel that are suppressed by the gate. Apparently, the potential barrier associated with a perpendicular random grain boundary is higher than that of the sub-grain boundaries present in the island grown from a grain filter. This confirms the observations from Chapter 5 that even though many planar defects are still present in the islands grown from a grain filter, they generally have lower defect density than random grain boundaries.

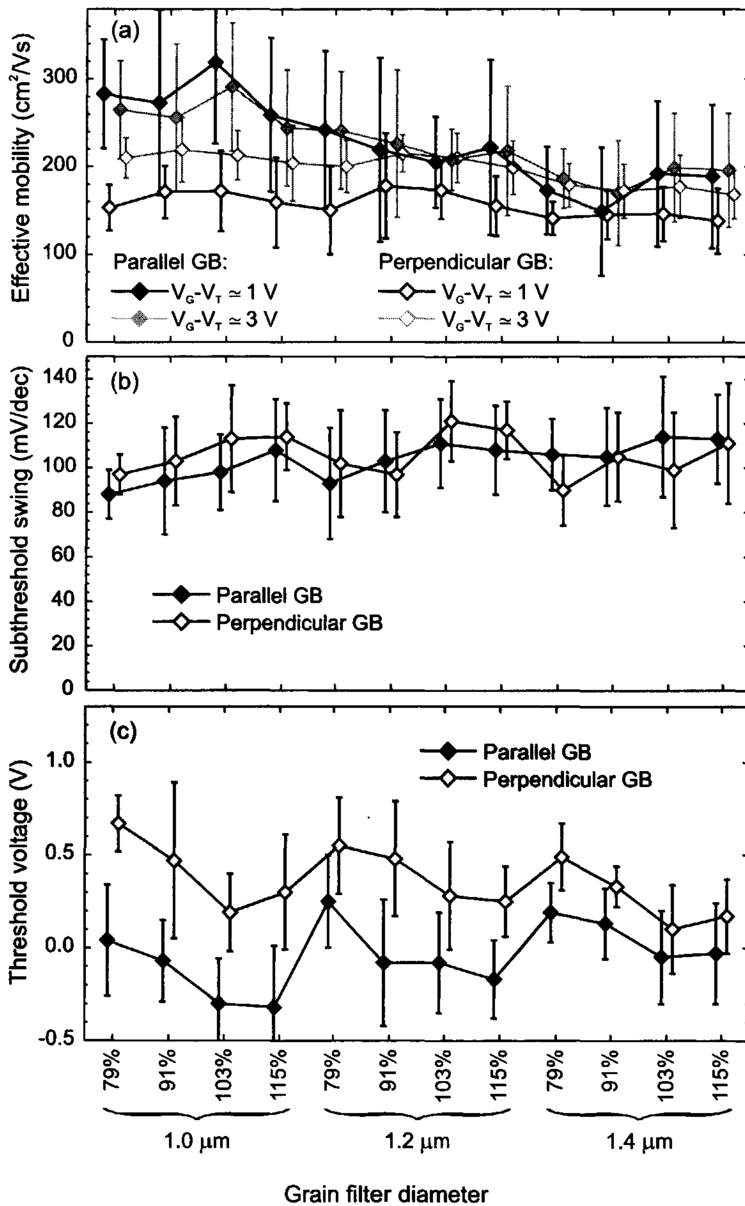


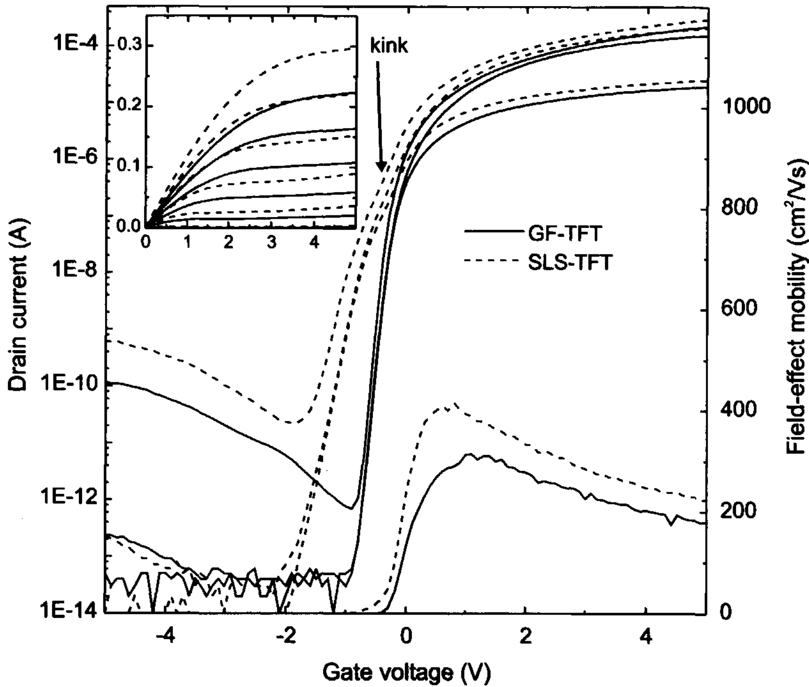
Figure 6.7. (a) The effective mobility at $V_G - V_T \approx 1$ V and ≈ 3 V, (b) the subthreshold swing, and (c) the threshold voltage for a W/L = 1.9/1.55 μm, 150 nm GBLC GF-TFT as a function of grain filter diameter.

A similar conclusion can be drawn if one looks at the dependence of the various parameters on the grain filter diameter of the GB-location-controlled TFTs. With increasing grain-filter diameter, the difference between the //-TFTs and the ⊥-TFTs becomes less. Apparently, the effect of the location-controlled grain boundary becomes less dominant relative to the effect of the planar defects in the islands. This is due to the increase in both the number and the associated defect density of the planar defects.

SLS-TFTS

Another method of GB-location control is the SLS process: long grain boundaries lie parallel to each other and the grains are thus potentially indefinitely long. The spacing between the grain boundaries is determined predominantly by the film thickness [61]. TFTs were made with the current flow parallel to these grain boundaries. Although the SLS process can also be used to obtain large single crystalline islands [114], these processes are much less practical, as the location of the islands is not controlled by lithography. For real grain-location control (i.e., for c-Si TFT fabrication), an alignment method is required that is both accurate enough and that is compatible with the subsequent lithographic alignment. Directional poly-Si made with SLS, on the other hand, can readily be employed to a TFT process as each TFT will contain multiple parallel grain boundaries. It is therefore considered to be justified to compare the results of GF-TFTs with these SLS-TFTs, even though the latter process is not really aimed at creating large grains for c-Si TFTs.

Figure 6.8 shows both transfer and output characteristics of a typical SLS-TFT and a typical GF-TFT. Both transistors had a ~100 nm thick film and comparable channel dimensions. It is immediately clear that the GF-TFT had better subthreshold behavior, whereas the SLS-TFT had better above threshold behavior. This can be attributed to the latter having more random grain boundaries, which results in a higher subthreshold swing. Careful inspection of the subthreshold behavior of the SLS-TFT shows that a little kink can be discerned. The curve appears to be the sum of that of two TFTs with a slightly different V_T and also a different on-current. This again can be attributed to the parallel grain boundaries: conduction along these grain boundaries apparently starts at slightly lower V_G than through the grains. As the grain boundaries are parallel to the current flow, they do not influence the above-threshold behavior, as is confirmed by the higher mobility. The situation is exemplified by the schematic drawings of Figure 6.9: the planar defects in the GF-TFT are less defective but are less ideally placed with respect to the current flow.



	W/L (μm)	$\mu_{FE,pk}$ (cm²/Vs)	S (mV/dec)	V_T (V)
GF-TFT	1.9/2.45	314	90	0.08
SLS-TFT	1.9/2.45	416	154	-0.09

Figure 6.8. Transfer characteristics of a ~100 nm GF-TFT and of a ~100 nm LS-SLS TFT. I_D–V_G curves are shown for V_D = 0.2, 2.0, and 5.0 V, respectively. Also, field-effect mobility (μ_{FE}) of both TFTs is shown as a function of V_G. The inset shows the output characteristics (I_D (mA) vs. V_D (V)) at V_G = 0, 1, 2, 3, 4, and 5 V, respectively, of both TFTs.

6.4. Discussion and Conclusions

Two irregularities in TFT behavior were found: high off-current and low on-current. The nature of the anomalous off-current was not understood. It was found that the crystallization conditions (substrate temperature, pulse duration, and ambient) had some influence on the off-current. The absence of this effect in the earlier work by Van Dijk [90] seems to indicate that it became apparent by the laser activation used in this process. It can therefore be concluded that the anomalous off-current is specific for devices fabricated with the process developed at Delft University of Technology. The back channel that was identified to be the cause of the leakage

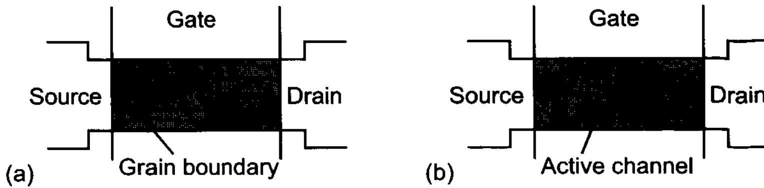


Figure 6.9. Schematic drawings of the location of grain boundaries, or more general planar defects, in the channel region of (a) an SLS-TFT and (b) a GF-TFT.

current could be induced by charges in the underlying SiO_2. Such a channel can be suppressed by increased channel doping or even by a back-channel doping [93].

The current crowding that was observed mainly with the 100 nm silicon films was related to the insufficient annealing of the source/drain implantation damage during laser activation. This effect could therefore be avoided by implanting at lower acceleration voltage possibly combined with an alternative activation procedure such as low-temperature thermal dopant activation [115].

The properties of those TFTs that could be successfully measured are summarized in Table 6.1. In the first column, the number of devices on which the values were based, are shown. Also, the standard deviation of mobility and swing are given to assess the device uniformity. Due to the current crowding effect in some devices, however, the values of the mobility are less reliable. Realizing that the non-uniformity of the SIMOX-TFTs is determined by the processing rather than the channel microstructure, it can then be concluded that process non-uniformity is less than 10%. From the non-uniformity of the laser-crystallized devices it can be seen that the crystallization non-uniformity exceeds the process non-uniformity. This can be attributed to the random crystallographic orientation and to the variable defect density. Significant trends that could be observed from this data were:

- Device performance of GF-TFTs decreases significantly with grain filter diameter.
- The planar defects that are present in the islands grown with grain filters have far less deteriorating influence than a random grain boundary perpendicular to the current flow.
- GF-TFTs had significantly lower subthreshold swing than SLS-TFTs whereas the latter had higher mobility.

In addition to this a somewhat less significant dependence of mobility on film thickness can be found for the GF-TFTs. This could be related to the number of defects in the channel region, which increases with decreasing film thickness, as became clear from Figure 5.7.

Due to the irregularities in TFT behavior, a number of aspects could not be investigated. These were summarized in Section 6.1. Based on what we found, however, we expect the following:

ad 1. From the observations of the microstructure, it is found that the number of planar defects decreased when planarized grain filters were used. Therefore mobility, threshold voltage, and subthreshold swing will improve when the rim is sharp.

ad 2. Although it was reported that grain boundary did not significantly rearrange at the temperature of thermal oxidation used [92], some influence might be expected. The improvement, however, is likely to be similar for the GF-TFTs and the SLS-TFTs as these materials are similar in terms of grain size. Therefore, the relative performance that was found will still hold at a low-temperature process: GF-TFTs have better subthreshold behavior, whereas SLS-TFTs have better above-threshold behavior.

ad 3. The non-uniformity of small TFTs made in large-grain poly-Si TFTs with a {111} texture [23] had a non-uniformity comparable to the GF-TFTs in this thesis. Due to the texture, this non-uniformity could mainly be attributed to the randomness of the grain boundaries. Thus, when in addition to this, crystallographic orientation would be random; non-uniformity is likely to be worse than with the GF-TFTs. We thus anticipate that GF-TFTs have higher uniformity than PMC-TFTs as the non-uniformity induced by randomly placed high-defect density grain boundaries is prevented.

ad 4. In general, it is true that the device uniformity will increase with the number of islands, as they have a completely random orientation. Uniformity as a function of the number of islands is expected to be better than the uniformity as a function of the number of grains in SLS-TFTs. This is due to the fact that the grains in directional SLS are not completely unrelated to each other, as many originate from the same seed and only have a slight relative misorientation.

Table 6.1. Comparison between the various TFTs that could successfully be measured, that is, those devices that were not leaky and that did not clearly suffer from a current crowding. The effective mobility at $V_G - V_T \approx 3$ V is shown except when indicated.

type and number	set	film (nm)	W/L (μm)	$\mu_{eff,pk}$ (cm^2/Vs) & std. dev.	S (mV/dec) & std. dev.	V_T (V) & std. dev.
SIMOX-TFT (115)		100	1.9/ 2.6	568 ± 41 (=7%)	65 ± 4 (=6%)	–0.10 ± 0.03
GF-TFT (17)		100	1.9/ 2.45	214 ± 81 (=38%)	81 ± 17 (=21%)	–0.01 ± 0.19
SLS-TFT (45)		100	1.9/ 2.45	294 ± 91 (=31%)	141 ± 31 (=22%)	–0.36 ± 0.22
SIMOX-TFT (140)		150	1.9/ 3.35	559 ± 43 (=8%)	64 ± 5 (=8%)	–0.04 ± 0.06
GF-TFT (50)	1.0 μm	150	1.9/ 3.25	305 ± 53 (=17%)	93 ± 17 (=18%)	0.16 ± 0.24
GF-TFT (51)	1.2 μm	150	1.9/ 3.25	229 ± 51 (=22%)	96 ± 17 (=18%)	0.46 ± 0.22
GF-TFT (50)	1.4 μm	150	1.9/ 3.25	187 ± 47 (=25%)	100 ± 17 (=17%)	0.58 ± 0.29
GF-TFT (50)	high E	150	1.9/ 2.35	270 ± 67 (=25%)	93 ± 23 (=25%)	0.22 ± 0.23
GF-TFT (52)	low E	150	1.9/ 2.35	232 ± 53 (=23%)	104 ± 25 (=24%)	0.08 ± 0.17
GF-TFT (50)	no GB	150	1.9/ 1.55	232 ± 86 (=37%) at 1V	97 ± 26 (=25%)	0.11 ± 0.28
//-TFT (50)	// GB	150	1.9/ 1.55	294 ± 104 (=35%) at 1V	97 ± 21 (=22%)	–0.18 ±0.30
⊥-TFT (49)	⊥ GB	150	1.9/ 1.55	171 ± 50 (=29%) at 1V	107 ± 19 (=18%)	0.37 ± 0.28

CHAPTER 7

Conclusions

There are a large variety of crystallization methods for thin silicon films under investigation by different groups. The work of three groups, each studying a different concept, is briefly summarized in this chapter. Results of high-performance TFTs were presented and will be compared with the results obtained in this research. Although device characteristics not only depend on microstructure but also, on device architecture, an attempt is made to compare the material properties to the work presented in this thesis. Next, the conclusions from this research are summarized and finally, some recommendations are given for further research.

7.1. Alternative Crystallization Methods

The focus of this research and that of many other groups has been on the fabrication of the ideal c-Si TFT. Due to the nature of the crystallization processes, the material properties will not be as good as for instance SIMOX films. Nevertheless, device performance approaches that of SIMOX-TFTs.

7.1.1 Description of Crystallization Methods

SEQUENTIAL LATERAL SOLIDIFICATION

Of the various pulsed-laser crystallization methods, sequential lateral solidification is a very promising optics-based method to obtain controlled SLG (C-SLG) [79]. The concept was already discussed in Section 2.2.5. Two aspects characterize SLS: the modulation of the incident laser light and the precise between-pulse translation of the sample with respect to this beam pattern. Masks are used to pattern the beam, which is subsequently projected on the sample. As the focus depth is in the order of 10s of μm, the sample is placed on an accurate Z-stage. A schematic drawing of a system for SLS was already shown in Figure 3.3. For the accurate between-pulse translations, an X-Y-stage is also required. When the subsequently molten regions

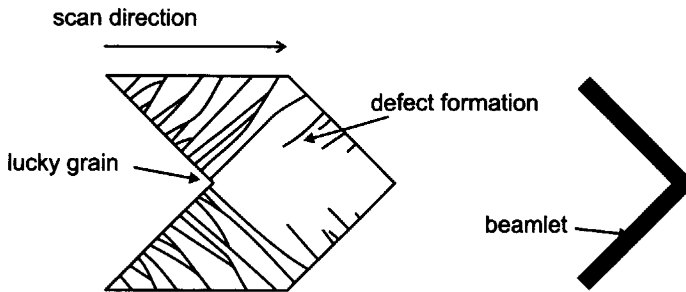


Figure 7.1. The microstructure (left) that can be obtained by scan with a chevron-shaped beamlet (right).

overlap, elongated grains can be obtained that lie parallel to each other (Figure 2.18 (c)). This directionally solidified material also has a very low surface roughness, as all grain boundaries were grown parallel and no protrusions are created. During the first few iterations of this process the number of grains is decreasing rapidly because of the occlusion of others. As a result, the average spacing between the grain boundaries increases. Due to the simultaneous creation of sub-grain boundaries, after several pulses this process saturates and the grain boundary spacing reaches a certain value that predominantly scaled with the film thickness [62].

Location-controlled single-crystal islands can be obtained with this method when a chevron-shaped beamlet is scanned over the surface rather than a straight beamlet [114]. As the grain boundaries line up perpendicular to the growth front, the grain that happens to be positioned at the corner of the chevron could grow into a large single-crystalline island, as is illustrated in Figure 7.1. During the lateral growth away from the central axis of the crystallized region, however, defects will be created due to the thermal stresses associated with the rapid cooling [61].

Results of devices made in directionally solidified poly-Si and in chevron-SLS c-Si islands were published and will be used for comparison [116,117]

CONTINUOUS-WAVE LASER CRYSTALLIZATION

Instead of using a pulsed laser to crystallize the silicon, some researchers use a continuous-wave (CW) solid-state laser [118]. Like the SLS process, the sample is translated with respect to the beam to obtain directionally solidified material. The microstructure that is obtained with CW laser crystallization (CWLC) resembles that obtained with directional SLS, although the direction in which the grain boundaries grow is less well defined. The material was reported to lead to films with a preferential {100} surface orientation [118]. Due to the CW nature of the light source, higher scanning speed can be obtained compared to an excimer-laser-based process. Also, the solid-state laser has higher stability than the excimer laser. At the same time, however, the spot size of such a CW laser is typically very small (e.g. 400

× 20 μm^2) and as a result more scans are needed to completely crystallize a given area. This means that the crystallization rate, that is, the area of film that is crystallized per unit of time, will be lower. Another aspect of the CW laser light is that it cannot easily be homogenized nor patterned because of the high degree of coherence. As patterning is required to obtain single-crystal regions, no true single-crystalline islands can be made with this process.

METAL-INDUCED LATERAL CRYSTALLIZATION

The solid-phase crystallization of a-Si can be accelerated by the presence of metal impurities, most commonly a thin Ni layer deposited on top of the silicon film (an overview of the current status of this process can be found in [119]). When Ni is used, small silicide precipitates are formed that migrate through the material, leaving a trail of crystallized material. Metal-induced lateral crystallization (MILC) can occur when the Ni layer is patterned: around the Ni islands, the silicide precipitates will migrate laterally, leaving a film with large elongated grains. The grains have a predominant {110} surface orientation, and the majority of grain boundaries are of the low-angle type.

In the simplest process to make TFTs with MILC material, the windows that will be used to contact the source and drain regions are also used to bring the film in contact with the Ni layer. The source and drain regions will be crystallized vertically into small-grain poly-Si. The channel region, however, will crystallize laterally from the source/drain towards the center and as a result, a high-angle grain boundary will be formed halfway the channel where the growth fronts met. Apart from the degradation by these perpendicular grain boundaries, the device characteristics are also deteriorated by the presence of Ni impurities in the channel. This is mainly visible by a drastic increase in the off-current. To avoid both the devastating effects of the perpendicular grain boundaries and of the Ni-rich areas, a non-self-aligned process was proposed, where the active channel region is made within a laterally crystallized area [120].

These TFTs still suffer from high off-currents, and some sort of gettering process is required in which Ni impurity atoms are either removed from the channel or deactivated. Impurities can be removed by thermal annealing, during which the Ni atoms diffuse to the P-doped source and drain regions [121]. This, however, renders the process incompatible with glass substrates. Alternatively, gettering can be achieved by laser annealing [119]. It is believed that in this process the Ni atoms either form Ni precipitates or are trapped at the grain boundaries. Either way, the atoms are electrically deactivated and I_{off} is decreased. This effect becomes apparent at energy densities close to E_{CM}, that is, when most of the silicon is melted. When the film is completely molten, however, the grain size drops significantly and the film

Table 7.1. An overview of the fabrication process of the devices made with the crystallization methods discussed in this section.

	Chevron SLS [116]	Directional SLS [117]	CWLC; at 20 cm/s [118]	MILC; 560°C for 20 hr [122]
Si film	220 nm (LPCVD)	100 nm	150 nm (PECVD)	100 nm (LPCVD)
Gate dielectric	24 nm thermal SiO_2	100 nm deposited SiO_2	120 nm SiO_2 (PECVD SiH_4)	11 nm thermal SiO_2
S/D doping & activation	Gas-immersion laser doping	Pre-crystallization ion-doping	Activation by excimer laser annealing	N/A
TFT architecture	Top-gate n-channel	Top-gate n-channel	Top-gate n-channel	Dual-gate n-channel

loses its texture, which was obtained during MILC. This limits the process window of the laser gettering to that of the SLG regime, which is unpractical.

The devices that are included in the comparison in this chapter received a 900°C anneal reduce density of planar defects and presumably to deactivate Ni impurity atoms [122].

7.1.2 Device Comparison

Table 7.1 briefly summarizes the devices fabrication processes used with the crystallization methods discussed in this section. The device results that were obtained with these crystallization methods are summarized in Table 7.2. For comparison, the results of 150 nm GF-TFTs and of 100 nm SLS-TFTs from Table 6.1 are also added. Like with the GF-TFTs for the CWLC-TFTs and the MILC-TFTs, also data from SIMOX-TFTs made in the same process was available. Although a true comparison can only be made when the devices are made in the same process, the data still allows for a comparison of the various crystallization methods.

ABOVE-THRESHOLD BEHAVIOR

When data from SIMOX-TFTs is available, a fair comparison of the carrier mobilities can be made by looking at the relative value of mobility with respect to that obtained with defect-free material. It is found that the mobilities of MILC-TFTs, CWLC-TFTs, and 150 nm GF-TFTs are 81%, 63%, and 55% of those of the SIMOX-TFTs, respectively. This order of relative mobilities correlates with the microstructural observations: (1) very small MILC-TFTs are often free of planar defects. (2) CWLC-TFTs do have planar defects, but they run parallel to the current

Table 7.2. An overview of the values of device parameters made with various crystallization methods. Note that, by lack of actual values, some values in this table were extracted from the graphs presented in the references.

	W/L (μm)	μ_n (cm^2/Vs)	S (V/dec)	V_T (V)	I_{off} (A)
Chevron SLS [116]	10/3	357 [2])	0.1-0.2	0.6	~10^{-12} at V_D = 0.1 V [1])
Directional SLS [117]	10/20	290 [2])	0.41	1.2	~10^{-13} at V_D = 0.1 V [1])
CWLC [118]	3/5	422 [2])	0.14	-0.1	~10^{-13} at V_D = 1 V [1])
62 nm {100} SIMOX [118]	N/A	670 [2])	N/A	N/A	N/A
MILC [122]	1.5/1.5	430 [3])	0.073	0.29	~10^{-13} at V_D = 0.05 V [1])
MILC [122]	4.5/4.5	288 [3])	0.095	0.64	~10^{-12} [1])
SIMOX [122]	N/A	~530 [1,3])	N/A	N/A	N/A
GF-TFTs (150 nm)	1.9/3.25	304 [4])	0.093	0.16	~10^{-13} at V_D = 2 V
SIMOX-TFTs (150 nm)	1.9/3.35	559 [4])	0.064	-0.04	~10^{-13} at V_D = 2 V
SLS-TFTs (100 nm)	1.9/2.45	294 [4])	0.141	-0.36	~10^{-13} at V_D = 2 V

[1]) Extracted from the graphs, rather than copied from the text.
[2]) Peak value of the field-effect mobility.
[3]) Effective mobility at $V_G - V_T \approx 0.5$ V.
[4]) Effective mobility at $V_G - V_T \approx 3$ V.

flow. (3) GF-TFTs have planar defects that are randomly oriented with respect to the current flow and thus can impose barriers for the current flow. In addition to this correlation with microstructure there is also the fact that MILC leads to {100} surface-oriented grains, which in general gives highest mobility.

The relative mobility of a MILC-TFT was seen to decrease drastically with channel width. For W/L = 4.5/4.5 the relative mobility dropped to 54%, which is even less than the value of CWLC-TFTs but comparable to the value of GF-TFTs. Mobility degraded both as a function of the width and as a function of the length of the channel. The degradation of carrier mobility as a function of width was related to the presence of planar defects and to the Ni impurities in the channel. The degradation as a function of length shows that the material is not uniform in that

direction. Indeed, it was found that closer to the Ni seeding window, the Ni content is much higher and as a result, carriers are scattered [123].

The mobility of the directional SLS-TFTs is very close to the values obtained in this thesis. The length of the channel, however, was different by a factor of eight. Apparently, the grain length in directional solidified films is not limited and true directional behavior can still be obtained for very long devices.

SUB-THRESHOLD BEHAVIOR

The subthreshold swing of devices in general depends not only on defect density in the channel, but also on gate-oxide thickness and quality. Although these parameters were different for all the devices that are discussed, some conclusions can be drawn from a comparison of those devices that were made with thermal SiO_2.

The MILC-TFTs have similar subthreshold swings as the GF-TFTs. Again, however, the swing was found to deteriorate with increasing channel dimensions, whereas such behavior was not found for GF-TFTs. Also, the off-current for devices close to the seeding windows was found to be much higher. This is again related to the high Ni content close to the seeding window [123].

The chevron-SLS TFTs have significantly larger subthreshold swing than the GF-TFTs. Interestingly, when the same results were presented in a different context, a much lower value of the subthreshold swing of 0.07 V/dec was reported [124]. This seems to indicate a non-uniformity in the microstructure obtained with the chevron-SLS process. Indeed, it is known that the selection mechanism during chevron SLS does not always work: when one or more grain boundaries are present near to the exact corner of the chevron, they could grow exactly in the center of the island or, in other words, they are not "pushed aside" by the sloped growth fronts on either side of the corner [74]. In any case, if such grain boundaries are present, they will most likely be random high-angle grain boundaries and as such they will deteriorate the subthreshold swing.

BELOW-THRESHOLD BEHAVIOR

Off-currents were not thoroughly investigated in this thesis as the use of thermal oxide decreases the off-current for low values of V_D below the detection limit. Also, detailed off-current data was absent in the references discussed in this section. In addition to this, the device fabrication and architecture differed significantly.

7.2. Conclusions and Recommendations

In general, it can be concluded that the grain-filter method is a promising method of grain-location control. In this section, the conclusions from the research presented in

this thesis are summarized. Also, some recommendations for further research are given.

7.2.1 Conclusions

The conclusions that were obtained in this research are summarized for each part of this thesis:

PROBLEM STATEMENT

1. When making relatively small devices in poly-Si films with relatively large grains, the heterogeneity of the film can lead to highly non-uniform device performance. It was reasoned that to solve such non-uniformity, either the periodicity of the poly-Si must be increased or the location of grains must be fully controlled. The research presented in this thesis led to the development of a grain-location control method in a single-pulse excimer-laser crystallization (ELC) process.

SINGLE-PULSE EXCIMER-LASER CRYSTALLIZATION

2. Excimer-laser crystallization is found to be a very flexible way to obtain various microstructures in poly-Si films. The most important aspect in this flexibility is the possibility to control the super-lateral growth (SLG) of large low-defect-density grains. Although a multiple-pulse ELC process could potentially lead to a larger range of microstructures, a single-pulse ELC process is still of interest as fewer laser pulses are required to crystallize a certain area.
3. Controlled SLG (C-SLG) can be obtained in a single-pulse ELC process by lithographically making patterns that influence the melting and solidification behavior of the film. In this work, the best concept of lithography-based C-SLG was found to be the film thickness dependence of the threshold energy density for complete melt (E_{CM}). At the position of the thickest film, a seed for lateral growth could remain. The energy-density process window is then defined by the E_{CM} of the surrounding film and the E_{CM} of the thickened part of the film.
4. When the E_{CM} of the seed is very high, it could be that the process window is limited by the agglomeration of the surrounding film rather than by the local E_{CM}. Agglomeration was investigated in detail and it was found that it occurs as a result of severe film thickness fluctuations observed at energy densities well beyond E_{CM}. These surface ripples were concluded to be resulting from the reflow of liquid silicon due to surface tension gradients created by energy-

density fluctuations in the laser pulse (the Marangoni effect). Such fluctuations were created by the homogenizer lens arrays.

GRAIN-LOCATION CONTROL

5. It was found that in a single-pulse ELC method, a C-SLG method alone cannot lead to grain-location control, as the number of seeds for lateral growth is not fully controlled. The solution of this problem was found to be the addition of a selection mechanism by which only a single seed for lateral growth is selected from an initial set of seeds. It was argued that this behavior could be observed for U-shaped cavities and therefore this structure was termed grain filter. The method is based on the occlusion of grains that is normally observed during planar regrowth of a liquid.
6. From the top-view SEM analysis, it was found that successful grain filtering could be obtained over a long range of energy densities. Against expectations, however, the occlusion mechanism did not seem to be driven by the crystallographic orientation of the grains as no texture was obtained. It could, however, also be that a large set of seeds was never present to begin with. This could be related to the downward occlusion during the explosive crystallization of the silicon column that lies embedded in the SiO_2.
7. When the spacing between the grain filters was smaller than the lateral-growth distance, a grid of square islands was obtained over a large range of energy densities. Also, within a large window, the quality of these islands did not change significantly with energy density. As it was also found that the cavities were reasonably reproducible despite the two-step procedure, it can be concluded that the grain-filter process has a sufficient reproducibility.
8. When the spacing between the grain filters was larger than the lateral-growth distance, it was found that islands with a diameter > 7 μm could be grown. These large islands were obtained in ~250 nm thick films pre-heated to 470°C. Although grain-size enhancement could also be obtained with pulse-duration extension, this method was considered to be less preferential as more laser energy is required and the films have larger stress.
9. Although successful grain filtering was established, the islands still contained many planar defects. From the TEM investigations it was concluded that the rim and the diameter of the cavity have a decisive influence on the quality of the islands. When planar defects are present in the seed, they can be filtered out when the cavity is narrow enough. During the final stage of the vertical growth and the early stage of the horizontal growth, however, many defects are created. It was found that this could for a large part be suppressed by sharpening the rim of the grain filter.

10. The defects that are created on the rim are mostly Σ3 grain boundaries and therefore this defect creation was linked to the breakdown of the growth front at elevated velocities. The defect creation by thermal stresses during solidification typically leads to sub-grain boundaries. These were, however, hardly found with the electron backscatter diffraction (EBSD) analysis, although it should be mentioned that closely-spaced planar defects could not be resolved with this method. For very thin films, on the other hand, the latter defect-creation mechanism does seem to play a role.

11. From the heat-flow simulations it was found that the sudden deterioration of island quality and diameter that was mainly observed for thick films could be related to the complete-melt condition of the silicon column. Nucleation in the cavity is followed by growth at high velocity and thus with high density of defects.

12. It was also found from heat-flow simulations that growth velocity reaches a peak on the rim of the cavity but that it does not exceed the critical value for breakdown of the growth front observed in partial melting of Si films. Based on the observations, however, it was speculated that the critical velocity for defect creation could be decreased when growth is along an interface. The observation that defect creation can be suppressed by sharpening the rim could be related to the velocity dependence on the crystallographic orientation of the growth front. When the rim is curved, the growth front along the interface gradually changes its orientation and at some point a minimum in the critical velocity is reached and defects could be created.

DEVICE PERFORMANCE

13. The irregular behavior in the off-state was found to be related to the device fabrication rather than the crystallization as high off-current was present regardless of crystallization conditions. Nevertheless, the exact conditions were found to have an influence on the degree of leakage that is observed. The exact mechanism behind this, however, was not understood, although it seems clear that leakage is through the presence of a back channel. In general such a channel can be avoided by increased channel doping or even a back channel doping.

14. The current crowding for low V_D was found to be related to the insufficient annealing of damage resulting from the source/drain implantation. This was due to the self-aligned nature of the activation process with respect to the implantation and to the heat-sink behavior of the aluminum gate that is separated from the film by only a thin oxide layer.

15. In general it was found that devices made in islands grown from grain filters showed behavior close to that of devices made in defect-free material:

SIMOX-TFTs. Compared to the devices made in films crystallized through the sequential lateral solidification (SLS) method, it was found that subthreshold behavior was better and above-threshold behavior was worse for GF-TFTs. This was related to the distribution and the defect density of the planar defects in the channel region.

16. For increasing cavity diameter, the performance of the device was observed to decrease. This was attributed to an increase of the number and of the randomness of the planar defects in the channel. By comparison to devices with a random grain boundary deliberately placed in the channel region, it was confirmed that the planar defects in islands grown with the narrower grain filters indeed have lower defect density.
17. In general the impression is that device uniformity is poor with the GF-TFTs. Intuitively, this is related to the randomness of the crystal orientation rather than the variations in defect distribution. However, evidence for this conclusion was not found, as multiple-island TFTs did not show regular TFT behavior.
18. The excellent subthreshold behavior of the GF-TFTs was confirmed by comparing the data with that presented by other groups working on alternative crystallization methods. On-state behavior typically was found to be poorer. This is expected to be less so for planarized grain filters. These, however, could not be measured due to the off-state anomaly.
19. Of the alternative methods, metal-induced lateral crystallization seems to have a fundamental limitation in performance due to degrading presence of impurities. Sequential lateral solidification and continuous-wave laser crystallization are similar in some ways, although the former is more flexible as the beam can be patterned. Also, crystallized area per time unit is expected to be larger for the former.

7.2.2 Recommendations

Based on the conclusions, some recommendations for further can be given:

1. For a uniform c-Si TFT process, it seems essential that the crystallographic orientation of the grains is controlled. Some preferential orientation could become apparent when the vertical growth stage starts on a larger number of seeds. These seeds are, however, required to be very small because of the limited diameter of the cavity. It may be better to either add a separate process step in which a textured precursor is made or to use multiple islands in device fabrication.
2. Even if a textured precursor is created, the defect creation at the rim of the cavity can still result in a random surface orientation. It is therefore important that defect creation mechanisms are further investigated. One way to do this is

to bring the bottom of the silicon column in contact with the c-Si substrate so that the defect creation as a function of crystallographic orientation can be investigated. To reduce the loss of heat to the c-Si wafer through heat-conduction through the grain filter, this experiment should be carried out with SIMOX wafers rather than c-Si wafers.

3. Although promising results were obtained with the grain-filter method, it must still be shown whether it can be economically implemented in a large-area application. Recognizing that sequential lateral solidification is the most promising of the alternative crystallization methods, this question is related to weighing the cost of an extra lithographic step to that of the more complex crystallization step.

4. In addition, one could focus on other applications for this method. For example in IC-manufacturing, thick layer deposition is a common step for the isolation of devices. Also, as chemical-mechanical polishing is typically used to decrease surface topography in case of multiple layers of interconnect; this step could potentially be utilized for planarizing the cavities. This opens the way for three-dimensional circuit integration.

5. The anomalies in device performance must be addressed, as it seems clear that they are related to the device fabrication. Dopant activation can easily be performed in a better way, so that current crowding can be avoided. The back channel effect, however, might imply the use of a different underlying oxide. An additional requirement to the SiO_2 layer is that it has good step coverage, so that steep cavities can be made.

Bibliography

[1] W.C. O'Mara, *Liquid crystal flat panel displays: manufacturing science and technology* (Van Nostrand Reinhold, New York, 1993).

[2] N. Yamauchi and R. Reif, *Polycrystalline silicon thin films processed with silicon ion implantation and subsequent solid-phase crystallization; theory, experiments, and thin-film transistor applications*, J. Appl. Phys. **75**, 3235 (1993).

[3] Y. Matsueda, S. Inoue, and T. Shimoda, *Concept of system on panel*, Proc. AM-LCD, 77 (2001).

[4] V.G. Chigrinov, *Liquid crystal devices: physics and applications* (Artech House, Boston, 1999), Chapter 3.

[5] P. Mei, J.B. Boyce, M. Hack, R. Lujan, S.E. Ready, D.K. Fork, R.I. Johnson, G.B. Anderson, *Grain growth in laser dehydrogenated and crystallize polycrystalline silicon for thin film transistors*, J. Appl. Phys. **76**, 3194 (1994).

[6] J.Y.W. Seto, *The electrical properties of polycrystalline silicon films*, J. Appl. Phys. **46**, 5247 (1975).

[7] G. Baccarani, B. Ricco, G. Spadini, *Transport properties of polycrystalline silicon films*, J. Appl. Phys. **49**, 5565 (1978).

[8] W. Bollmann, *Crystal defects and interfaces* (Springer, New York, 1970), Chapter 11.

[9] D.K. Schroder, *Semiconductor material and device characterization* (John Wiley, New York, 1990), Chapter 5.

[10] T. Sato, Y. Takeishi, H. Hara, and Y. Okamoto, *Mobility anisotropy of electrons in inversion layers on oxidized silicon surfaces*, Phys. Rev. B **4**, 1950 (1971).

[11] J. Levinson, F.R. Shepherd, P.J. Scanlon, W.D. Westwood, G. Este, and M. Rider, *Conductivity behavior in polycrystalline semiconductor thin film transistors*, J. Appl. Phys. **53**, 1193 (1982).

[12] R.E. Proano and D.G. Ast, *Effects of the presence/absence of HCl during gate oxidation on the electrical and structural properties of polycrystalline silicon thin-film transistors*, J. Appl. Phys. **66**, 2189 (1982).

[13] J.G. Fossum and A. Ortiz-Conde, *Effects of grain boundaries on the channel conductance of SOI MOSFETs*, IEEE Trans. Electron Devices **30**, 933 (1983).

[14] I.W. Wu, T.Y. Huang, W.B. Jackson, A.G. Lewis, and A. Chiang, *Passivation kinetics of two types of defects in polysilicon TFT by plasma hydrogenation*, IEEE Electron Device Lett. **12**, 181 (1991).

[15] G. Fortunato, D.B. Meakin, P. Migliorato, and P.G. Le Comber, *Field-effect analysis for the determination of gap-state density and Fermi-level temperature dependence in polycrystalline silicon*, Phil. Mag. B **57**, 573 (1988).

[16] T.J. King, M. Hack, and I.W. Wu, *Effective density-of-states distributions for accurate modeling of polycrystalline-silicon thin-film transistors*, J. Appl. Phys. **75**, 908 (1994).

[17] G.A. Armstrong, S. Uppal, S.D. Brotherton, and J.R. Ayres, *Differentiation of effects due to grain and grain boundary traps in laser annealed poly-Si thin film transistors*, Jpn. J. Appl. Phys. **37**, 1721 (1998).

[18] S.D. Brotherton, N.D. Young, and A. Gill, *Leakage currents in low temperature processed polycrystalline-Si TFTs*, Proc. ESSDERC **17**, 671 (1987).

[19] J.G. Fossum, A. Ortiz-Conde, H. Shichijo, and S.K. Banerjee, *Anomalous leakage current in LPCVD polysilicon MOSFET's*, IEEE Trans. Electron Devices **32**, 1878 (1985).

[20] A. Rodriguez, E.G. Moreno, H. Pattyn, J.F. Nijs, and R.P. Mertens, *Model for the anomalous off-current of polysilicon thin-film transistors and diodes*, IEEE Trans. Electron Devices **40**, 938 (1993).

[21] N. Yamauchi, J.J.J. Hajjar, and R. Reif, *Polysilicon thin-film transistors with channel length and width comparable to or smaller than the grain size of the thin film*, IEEE Trans. Electron Devices **38**, 55 (1991).

[22] T. Noguchi, *Appearance of single-crystalline properties in fine-patterned Si thin film transistors (TFTs) by solid-phase crystallization (SPC)*, Jpn. J. Appl. Phys. **32**, L1585 (1993).

[23] R. Ishihara, *Effects of grain-boundaries in excimer-laser crystallized poly-Si thin-film transistors*, Proc. ESSDERC **31**, 479 (2001).

[24] M. Kimura and S. Inoue, *Device simulation of interface roughness in laser-crystallized p-Si TFTs*, Proc. AM-LCD, 263 (1999).

[25] A.B.Y. Chan, C.T. Nguyen, P.K. Ko, S.T.H. Chan, and S.S. Wong, *Polished TFT's: surface roughness reduction and its correlation to device performance improvement*, IEEE Trans. Electron Devices **44**, 455 (1997).

[26] J.S. Im and R.S. Sposili, *Crystalline Si films for integrated active-matrix liquid-crystal displays*, Mat. Res. Soc. Bull. **21**, 39 (1996).

[27] *Laser Annealing of Semiconductors*, edited by J.M. Poate and J.W. Mayer (Academic Press, New York, 1982).

[28] J.S. Im, H.J. Kim, and M.O. Thompson, *Phase transformation mechanisms involved in excimer laser crystallization of amorphous silicon films*, Appl. Phys. Lett. **63**, 1969 (1993).

[29] D.E. Aspens, in *Properties of crystalline silicon*, edited by R. Hull (IEE, London, 1999), Chapter 12.

[30] T. Sameshima, S. Usui, and M. Sekiya, *XeCl excimer laser annealing used in the fabrication of poly-Si TFT's*, IEEE Electron Device Lett. **7**, 276 (1986).

[31] M.C. Gower, in *Excimer lasers: principles of operation and equipment*, edited by R.C. Rafer and P.J. Oakley (Chapman&Hall, London, 1993), Chapter 8.

[32] K. Jasper, S. Scheede, B. Burghardt, R. Senczuk, P. Berger, H.J. Kahlert, and H. Huegel, *Excimer laser beam homogenizer with low divergence*, Appl. Phys. A **69**, S315 (1999).

[33] T.S. Fahlen, *Optical beam integration system*, U.S. patent no. 4,733,944 (March 29, 1988).

[34] P. Dainesi, J. Ihlemann, and P. Simon, *Optimization of a beam delivery system for a short-pulse KrF laser used for material ablation*, Appl. Opt. **37**, 7080 (1997).

[35] A.T. Voutsas, A.M.Marmorstein, and R. Solanki, *The impact of annealing ambient on the performance of excimer-laser-annealed polysilicon thin-film transistors*, J. Electrochem. Soc. **146**, 3500 (1999).

[36] D.J. McCulloch and S.D. Brotherton, *Surface roughness effects in laser crystallized polycrystalline silicon*, Appl. Phys. Lett. **66**, 2060 (1995).

[37] R.A. Lemons, M.A. Bosch, and D. Herbst, *Crystallization of silicon films on glass: a comparison of methods*, Mater. Res. Soc. Proc. **13**, 581 (1983).

[38] P. Mei, J.B. Boyce, M. Hack, R. Lujan, R.I. Johnson, G.B. Anderson, D.K. Fork, and S.E. Ready, *Laser dehydrogenation/crystallization of plasma-enhanced chemical vapor deposited amorphous silicon for hybrid thin film transistors*, Appl. Phys. Lett. **64**, 1132 (1994).

[39] A.M. Marmorstein, A.T. Voutsas, and R. Solanki, *A systematic study and optimization of parameters affecting grain size and surface roughness in excimer laser annealed polysilicon thin films*, J. Appl. Phys. **82**, 4303 (1997).

[40] H. Kuriyama, et al., *Enlargement of poly-Si film grain size by excimer laser annealing and its application to high-performance poly-Si thin film transistor*, Jpn. J. Appl. Phys. **30**, 3700 (1991).

[41] K.Shimizu, S. Imai, O. Sugiura, and M. Matsumura, *Transient temperature profiles in silicon films during pulsed laser annealing*, Jpn. J. Appl. Phys. **30**, 2664 (1991).

[42] A.G. Cullis, *Fundamental aspects of high speed crystal growth from the melt*, Mater. Res. Soc. Proc. **35**, 15 (1985).

[43] M.O. Thompson, J.W. Mayer, A.G. Cullis, H.C. Webber, N.G. Chew, J.M. Poate, and D.C. Jacobson, *Silicon melt, regrowth, and amorphization velocities during pulsed laser irradiation*, Phys. Rev. Lett. **50**, 896 (1983).

[44] H.J. Leamy, W.L. Brown, G.K. Celler, G. Foti, G.H. Gilmer, and J.C.C. Fan, *Explosive crystallization of amorphous germanium*, Appl. Phys. Lett. **38**, 137 (1981).

[45] M.O. Thompson, G.J. Galvin, J.W. Mayer, P.S. Peercy, J.M. Poate, D.C. Jacobson, A.G. Cullis, and N.G. Chew, *Melting temperature and explosive crystallization of amorphous silicon during pulsed laser irradiation*, Phys. Rev. Lett. **52**, 2360 (1984).

[46] J.H. Yoon and J.S. Im, *Rapid melting dynamics of amorphous Si films*, Metals and Materials **5**, 525 (1999).

[47] R.B. Iverson and R. Reif, *Dose dependence of crystallization in implanted polycrystalline silicon films on SiO2*, Appl. Phys. Lett. **52**, 645 (1988).

[48] F.C. Voogt and R. Ishihara, *Explosive crystallization during excimer-laser annealing of LPCVD a-Si films*, to be published in J. Appl. Phys.

[49] F.C. Voogt and R. Ishihara, *A combined TEM and time-resolved optical reflectivity investigation into the excimer-laser crystallization of a-Si films*, Thin Solid Films **383**, 45 (2001).

[50] V.V. Gupta, H.J. Song, and J.S. Im, *Numerical analysis of excimer-laser-induced melting and solidification of thin Si films*, Appl. Phys. Lett. **71**, 99 (1997).

[51] S.D. Brotherton, D.J. McCulloch, J.P. Gowers, J.R. Ayres, and M.J. Trainor, *Influence of melt depth in laser crystallized poly-Si thin film transistors*, J. Appl. Phys. **82**, 4086 (1997).

[52] S.R. Stiffler, M.O. Thompson, and P.S. Peercy, *Supercooling and nucleation of silicon after laser melting*, Phys. Rev. Lett. **60**, 2519 (1988).

[53] J.W. Christian, *Theory of Transformations in Metals and Alloys: Part I Equilibrium and General Kinetic Theory*, (Pergamon, New York, 1975), Chapter 10.

[54] S.R. Stiffler, M.O. Thompson, and P.S. Peercy, *Transient nucleation following pulsed-laser melting of thin silicon films*, Phys. Rev. B **12**, 9851 (1991).

[55] R. Ishihara and F.C. Voogt, *Heterogeneous nucleation in excimer-laser melted Si thin-films*, Solid State Phen. **80-81**, 163 (2001).

[56] D. Pribat, P. Legagneux, C. Collet, F. Plais, O. Huet, and C. Reita, *Excimer laser processing for low temperature TFTs and circuits*, Proc. AM-LCD, 9 (1998).

[57] M. Miyasaka and J. Stoemenos, *Excimer laser annealing of amorphous and solid-phase-crystallized silicon films*, J. Appl. Phys. **86**, 5556 (1999).

[58] D.K. Fork, G.B. Anderson, J.B. Boyce, R.I. Johnson, and P. Mei, *Capillary waves in pulsed excimer laser crystallized amorphous silicon*, Appl. Phys. Lett. **68**, 2138 (1996).

[59] A.G. Cullis, N.G. Chew, H.C. Webber, and D.J. Smith, *Orientation dependence of high speed silicon crystal growth from the melt*, J. Cryst. Growth **68**, 624 (1984).

[60] H.S. Cho, D.B. Kim, A.B. Limanov, M.A. Crowder, and J.S. Im, *Sequential lateral solidification of ultra-thin a-Si films*, Mater. Res. Soc. Proc. **621**, Q9.9.1 (2000).

[61] M.A. Crowder, A.B. Limanov, B.A. Turk, and J.S. Im, *Characterization & Analysis of Sub-Grain Boundaries in Sequential Lateral Solidification Processed SOI Films*, Mater. Res. Soc. Proc. **685E**, D11.3.1 (2001).

[62] M.A. Crowder, *Microstructural development in sequential lateral solidification of thin silicon films*, Ph.D. thesis, Columbia University, 2001, Chapter 4 and 5.

[63] D.J. Srolovitz and M.G. Goldiner, *The thermodynamics and kinetics of film agglomeration*, J. Minerals, Metals and Materials **47**, 31 (1995).

[64] H.E. Cline, *Silicon thin films formed on an insulator by recrystallization*, J. Appl. Phys. **55**, 2910 (1984).

[65] G. Groos and M. Stutzmann, *Realization and characterization of Si nanostructures*, Phys. Stat. Sol. A **166**, 687 (1998).

[66] M. von Allmen and A. Blatter, *Laser-beam interactions with materials* (Springer, Berlin, 1995), Section 2.3.1

[67] C. Hill and D.J. Godfrey, *Changes in surface topography after pulsed laser anneal of silicon*, J. de Phys. Coll. **41**, 79 (1980).

[68] A.G. Cullis, in *Laser Annealing of Semiconductors*, edited by J.M. Poate and J.W. Mayer (Academic Press, New York, 1982), Chapter 6.

[69] A.G. Cullis, H.C. Webber and N.G. Chew, *Correlation of the structure and electrical properties of ion-implanted and laser-annealed silicon*, Appl. Phys. Lett. **36**, 547 (1980).

[70] S.I. Valyanskii, *Recoil momentum in lead and zinc irradiated with a Q-switched ruby laser*, Sov. Phys. Tech. Phys. **23**, 1265 (1979).

[71] G. Gorodetsky, J. Kanicki, T. Kazyaka, and R.L. Melcher, *Far UV pulsed laser melting of silicon*, Appl. Phys. Lett. **46**, 547 (1985).

[72] T.R. Anthony and H.E. Cline, *Surface rippling induced by surface-tension gradients during laser surface melting and alloying*, J. Appl. Phys. **48**, 3888 (1977).

[73] K. Shimizu, O. Sugiura, and M. Matsumura, *High-mobility poly-Si thin-film transistors fabricated by a novel excimer laser crystallization method*, IEEE Trans. Electron Devices **40**, 112 (1993).

[74] B.A. Turk and J.S. Im (private communication).

[75] H. Kuriyama, et al., *Lateral grain growth of poly-Si films with a specific orientation by an excimer laser annealing method*, Jpn. J. Appl. Phys. **32**, 6190 (1993).

[76] H. Kuriyama, T. Nohda, Y. Aya, T. Kuwahara, K. Wakisaka, S. Kiyama, and S. Tsuda, *Comprehensive study of lateral grain growth in poly-Si films by excimer laser annealing and its application to thin film transistors*, Jpn. J. Appl. Phys. **33**, 5657 (1994).

[77] C.V. Thompson, *Secondary grain growth in thin films of semiconductors: theoretical aspects*, J. Appl. Phys. **58**, 763 (1985).

[78] H.J. Kim and J.S. Im, *Multiple pulse irradiation effects in excimer laser-induced crystallization of amorphous Si films*, Mater. Res. Soc. Proc. **321**, 665 (1994).

[79] R.S. Sposili and J.S. Im, *Sequential lateral solidification of thin silicon films on SiO2*, Appl. Phys. Lett. **69**, 2864 (1996).

[80] J.S. Im, et al., *Controlled super-lateral growth of Si films for microstructural manipulation and optimization*, Phys. Stat. Sol. A **166**, 603 (1998).

[81] G. Fortunato, L. Mariucci, R. Carluccio, A. Pecora, and V. Foglietti, *Excimer laser crystallization techniques for polysilicon TFTs*, Appl. Surf. Sci. **154-155**, 95 (2000).

[82] C.H. Oh and M. Matsumura, *A proposed single grain-boundary thin-film transistor*, IEEE Electron Device Lett. **22**, 20 (2001).

[83] L. Mariucci, et al., *Lateral growth control in excimer laser crystallized polysilicon*, Thin Solid Films **337**, 137 (1999).

[84] P.J. French, B.P. van Drieënhuizen, D. Poenar, J.F.L. Goossen, R. Mallée, P.M. Sarro, and R.F. Wolffenbuttel, *The development of a low-stress polysilicon process compatible with standard device processing*, IEEE J. Microelectromech. Systems **5**, 187 (1996).

[85] M.R. Rakhshandehroo and S.W. Pang, *Fabrication of Si field emitters by dry etching and mask erosion*, J. Vac. Sci. Technol. B **14**, 612 (1996).

[86] L.K. White, *Planarization Properties of Resist and Polyimide Coatings*, J. Electrochem. Soc. **130**, 1543 (1983).

[87] Y.X. Li, *Plasma etching for integrated silicon sensor applications*, Ph.D. thesis, Delft University of Technology, 1995, Chapter 4.

[88] H.C. Cheng, in *ULSI Technology*, edited by C.Y. Chang and S.M. Sze (McGraw-Hill, New York, 1996), Chapter 5.

[89] A.J. van Roosmalen, J.A.G. Baggerman, and S.J.H. Brader, *Dry etching for VLSI* (Plenum, New York, 1991).

[90] B.D. van Dijk, *Electrical characterization of c-Si TFTs fabricated by location-controlled laser crystallization*, Ph.D. thesis, Delft University of Technology, 2002.

[91] R.S. Sposili and J.S. Im, *Line-scan sequential lateral solidification of Si thin films*, Appl. Phys. A **67**, 273 (1998).

[92] A. Hara, F. Takeuchi, and N. Sasaki, *Mobility enhancement limit of excimer-laser-crystallized polycrystalline silicon thin film transistors*, J. Appl. Phys. **91**, 708 (2002).

[93] S.D. Brotherton, et al., *The technology and application of laser crystallised poly-Si TFTs*, Electrochem. Soc. Proc. **98-22**, 25 (1998).

[94] J.P. Lu, P. Mei, R.T. Fulks, J. Rahn, J. Ho, Y. Wang, J.B. Boyce, and R.A. Street, *Excimer laser processing for a-Si and poly-Si thin film transistors for imager applications*, J. Vac. Sci. Technol. A **18**, 1823 (2000).

[95] C.H. Tseng, C.W. Lin, T.K. Chang, H.C. Cheng, and A. Chin, *Effects of excimer laser dopant activation on low temperature polysilicon thin-film transistors with lightly doped drains*, Electrochem. and Solid-State Lett. **4**, G94 (2001).

[96] D.G. Schimmel, *Defect etch for (100) silicon evaluation*, J. Electrochem. Soc. **126**, 479 (1979).

[97] K.H. Yang, *An etch for delineation of defects in silicon*, J. Electrochem. Soc. **131**, 1140 (1984).

[98] S. Christiansen, P. Lengsfeld, J. Krinke, M. Nerding, N.H. Nickel, and H.P. Strunk, *Nature of grain boundaries in laser crystallized polycrystalline silicon thin films*, J. Appl. Phys. **89**, 5348 (2001).

[99] J.P. Leonard and J.S. Im, *Modelling solid nucleation and growth in supercooled liquid*, Mater. Res. Soc. Proc. **580**, 233 (1999).

[100] J.P. Leonard and J.S. Im, *Stochastic modeling of solid nucleation in supercooled liquids*, Appl. Phys. Lett. **78**, 3454 (2001).

[101] D.B. Kim, *Numerical and experimental analysis of rapid lateral solidification of thin films*, Ph.D. thesis, Columbia University, 2002, Chapters 5 to 8.

[102] B. Chalmers, *Principles of Solidification* (Wiley, New York, 1964).

[103] A. Hara, K. Kitahara, K. Nakajima, and M. Okabe, *A new approach for form polycrystalline silicon by excimer laser irradiation with a wide range of energies*, Jpn. J. Appl. Phys. **38**, 6624 (1999).

[104] M. Tamura, H. Tamura, and T. Tokuyama, *Si bridging epitaxy from Si windows onto SiO2 by Q-switched ruby laser pulse annealing*, Jpn. J. Appl. Phys. **19**, L23 (1980).

[105] B.D. van Dijk, P.C. van der Wilt, G.J. Bertens, L.K. Nanver and R. Ishihara, *Single-crystal thin film transistor by grain-filter location-controlled excimer-laser crystallization*, Mater. Res. Soc. Proc. **685E**, D12.3.1 (2001).

[106] S.D. Brotherton, J.R. Ayres, and M.J. Trainer, *Leakage currents in poly-Si thin film transistors*, Solid State Phen. **51-52**, 621 (1996).

[107] M.J. Thompson, N.M. Johnson, M.D. Moyer, and R. Lujan, *Thin-film transistors on a-Si:H*, IEEE Trans. Electron. Devices **29**, 1643 (1982).

[108] L.K. Nanver, et al., *Applications of excimer laser annealing in IC processing*, to be presented at the 203rd Electrochem. Soc. Meeting, April 27 – May 2, 2003.

[109] M.J. Powell and J.W. Orton, *Characteristics of amorphous silicon staggered-electrode thin-film transistors*, Appl. Phys. Lett. **45**, 171 (1984).

[110] S.M. Sze, *Physics of semiconductor devices*, 2nd ed. (Wiley, New York, 1981), Section 7.3.4.

[111] S. Seki, O. Kogure, and B. Tsujiyama, *A semi-emperical model for the field-effect mobility of hydrogenated polycrystalline-silicon MOSFET's*, IEEE Trans. Electron Devices **35**, 669 (1988).

[112] C.T. Angelis, C.A. Dimitriadis, F.V. Farmakis, J. Brini, G. Kamarinos, M. Miyasaka, and J. Stoemenos, *Transconductance of large grain excimer laser-annealed polycrystalline silicon thin film transistors*, Solid-State Electron. **44**, 1081 (2000).

[113] K. Yamaguchi, *Modeling and characterization of polycrystalline-silicon thin-film transistors with a channel-length comparable to a grain size*, J. Appl. Phys. **89**, 590 (2001).

[114] J.S. Im, R.S. Sposili, and M.A. Crowder, *Single-crystal Si films for thin-film transistor devices*, Appl. Phys. Lett. **70**, 3434 (1997).

[115] M. Matsuo, T. Nakazawa, and H. Ohshima, *Low-temperature activation of impurities implanted by ion doping technique for poly-Si thin-film transistors*, Jpn. J. Appl. Phys. **31**, 4567 (1992).

[116] M.A. Crowder, P.G. Carey, P.M. Smith, R.S. Sposili, H.S. Cho, and J.S. Im, *Low-temperature single-crystal Si TFT's fabricated on Si films processed via sequential lateral solidification*, IEEE Electron Device Lett. **19**, 306 (1998).

[117] Y.H. Jung, J.M. Yoon, M.S. Yang, W.K. Park, H.S. Soh, H.S. Cho, A.B. Limanov, and J.S. Im, *The dependence of poly-Si TFT characteristics on the relative misorientation between grain boundaries and the active channel*, Mater. Res. Soc. Proc. **621**, Q9.14.1 (2000).

[118] A. Hara, F. Takeuchi, M. Takei, K. Suga, K. Yoshino, M. Chida, Y. Sano, and N. Sasaki, *High-performance polycrystalline silicon thin film transistors on non-alkali*

glass produced using continuous wave laser lateral crystallization, Jpn. J. Appl. Phys. **41**, L311 (2002).

[119] D. Murley, N. Young, M. Trainor, and D. McCulloch, *An investigation of laser annealed and metal-induced crystallized polycrystalline silicon thin-film transistors*, IEEE Trans. Electron Devices **48**, 1145 (2001).

[120] Z. Meng, M. Wang, and M. Wong, *High performance low temperature metal- induced unilaterally crystallized polycrystalline silicon thin film transistors for system-on-panel applications*, IEEE Trans. Electron Devices **47**, 404 (2000).

[121] Y. Hirakata, et al., *VGA reflection-type poly-Si TFT LCD with integrated digital driver using seven-mask CG Silicon CMOS process*, Proc. SID **31**, 1014 (2000).

[122] H. Wang, M. Chan, S. Jagar, V.M.C. Poon, M. Qin, Y. Wang, and P.K. Ko, *Super thin-film transistor with SOI CMOS performance formed by a novel grain enhancement method*, IEEE Trans. Electron Devices **47**, 1580 (2000).

[123] V.W.C. Chan, P.C.H. Chan, and C. Yin, *The effects of grain boundaries in the electrical characteristics of large grain polycrystalline thin-film transistors*, IEEE Trans. Electron Devices **49**, 1384 (2002).

[124] M.A. Crowder, *Microstructural development in sequential lateral solidification of thin silicon films*, Ph.D. thesis, Columbia University, 2001, Appendix A.

Publication List

1. P.C. van der Wilt and R. Ishihara, *Grain Location Control in Excimer-Laser Crystallization of Thin Silicon Films*, Phys. Stat. Sol. (a) **166**, 619 (1998).
2. P.C. van der Wilt and R. Ishihara, *Grain Matrix made with Excimer-Laser Crystallization of Thin Silicon Films*, Solid State Phenomena **67-68**, 169 (1999).
3. P.C. van der Wilt, R. Ishihara, and G.J. Bertens, *Location-Controlled Large-Grains in Near-Agglomeration Excimer-Laser Crystallized Silicon Films*, Mater. Res. Soc. Proc. **621**, Q7.4.1 (2000).
4. P.C. van der Wilt, B.D. van Dijk, G.J. Bertens, and R. Ishihara, *Study of Crystal Growth in Grain-Filters for Location-Controlled Excimer-Laser Crystallization*, Mat. Res. Soc. Proc. **695E**, D5.20 (2001).
5. P.C. van der Wilt, B.D. van Dijk, G.J. Bertens, R. Ishihara, and C.I.M. Beenakker, *Formation of location controlled crystalline islands using substrate embedded seeds in excimer-laser crystallization of silicon films*, Appl. Phys. Lett. **79**, 1819 (2001).
6. P.C. van der Wilt, B.D. van Dijk, G.J. Bertens, and R. Ishihara, *Properties of a Poly-Si Film Grown from a Grid of Grain Filters by Excimer-Laser Crystallization*, Proc. SAFE **4**, available for download at http://www.stw.nl/safe/ (2001).

Nawoord

Het werk waarvan dit proefschrift verslag legt is tot stand gekomen over een lange periode waarin ik veel hulp en steun heb mogen ontvangen van diverse mensen. Ik wil allereerst mijn promotor Kees Beenakker bedanken voor zijn vertrouwen in mij en voor zijn leiding aan de vakgroep Elektronische Componenten, Materialen en Technologie (ECTM), Wim Metselaar voor het financieel mogelijk maken van mijn onderzoek en Ryoichi Ishihara voor het opzetten en leiden van de TFT-groep en voor de hulp met schrijven en presenteren tijdens de vroege fase van mijn onderzoek.

Gedurende mijn onderzoek hebben mijn mede-promovendi een belangrijke rol gespeeld, zowel voor inhoudelijke discussies als voor de gezelligheid. Een belangrijk deel van mijn onderzoek is in samenwerking met Barry van Dijk geschied die ik met veel vragen bestookt heb en die mij geholpen heeft mijn eigen gedachten op een rijtje te zetten. Samen met Jurgen Bertens die hielp met de uitvoering vormden wij een hecht team en dat heeft in bijzondere mate bijgedragen aan de kwaliteit van mijn onderzoek en aan het plezier dat ik erin vond. Mijn kamergenoot Ad van Zutphen wil ik bedanken voor de motiverende gesprekken en voor de vele koffie die we gedeeld hebben, Leon van den Oever, Wibo van Noort en Marcel van den Berg wil ik bedanken voor het te uitgebreid ingaan op domme vragen van mijn kant en Martin Kroon wil ik bedanken voor zijn niet-aflatende cynisme en zijn nuchterheid. Verder wil ik Agnes Petit, Jan Heemskerk en Chiel Smit bedanken voor de gezelligheid en de koffie in de latere fase van mijn onderzoek en verder ook Bas Korevaar, Roelof Schuitema en Artyom Burtsev. Buiten mijn eigen groep wil ik ook nog Eelco Rouw en Maarten Ditzel bedanken met wie ik veel lol heb gehad in het opzetten van het dispuut MicroElektronica en Silicium Technologie (MEST).

Het experimentele deel van mijn onderzoek is voor een groot deel uitgevoerd in het fantastische laboratorium van het Delfts Instituut voor MicroElektronica en Submicrontechnologie (DIMES). Hierbij heb ik veel steun ontvangen van een grote groep technici onder leiding van Bert Goudena die ik wil bedanken voor het goed laten verlopen van alle werkzaamheden. Ik ben veel dank verschuldigd aan Jurgen

Bertens, die met bijzonder enthousiasme en met significante eigen inbreng geholpen heeft met het uitvoeren van mijn experimenten. Ik wil ook John Slabbekoorn bedanken voor zijn hulp met de laser en met de lithografie en Mario Laros voor zijn hulp met deposities en met de elekronen microscoop. Verder wil ik de volgende mensen bedanken voor hun hulp in het laboratorium: Alfred Apon, Charles de Boer, Alex van den Bogaard, Jan Groenenweg, Ruud Klerks, Hugo Schellevis, Tom Scholtes, Cassan Visser, Wim van der Vlist, Fabian Wahle en Henk van Zeijl.

Voor hulp bij uitvoeren en interpreteren van metingen ben ik vooral Barry van Dijk dankbaar en daarnaast Lis Nanver voor de interpretatie en Tjander Nathoeni voor de uitvoering. Jan Chris Staalenburg wil ik bedanken voor zijn hulp met mijn workstation, hoewel ik niet genoeg kan benadrukken hoe blij ik was van dat ding af te zijn. Verder wil ik ook Jeanne Sirks, Marian Roozenburg en Marysia Lagendijk bedanken voor gezelligheid en organisatie.

Het onderzoek was deel van een samenwerkingsproject met de IC-Technology, Devices, and Reliability groep van Hans Wallinga van Universiteit Twente. Van deze groep wil ik Viet Nguyen Hoang en André Hof bedanken voor het Chemisch Mechanisch Polijsten. Verder wil ik Frans Tichelaar van het nationaal centrum voor Hoge Resolutie Electronen Microscopie (HREM) bedanken voor het uitvoeren van Transmissie Electronen Microscopie, Mirjam Nieman wil ik bedanken voor het corrigeren van mijn Engels, en Juliet van 't Hul voor de hulp bij het bestrijden van RSI-achtige klachten. De stichting voor Fundamenteel Onderzoek der Materie (FOM) wil ik bedanken voor de financiële steun tijdens mijn detachering en voor het brede aanbod aan trainingen.

Part of my research was performed at the Radical Research Group in the Program of Material Science at Columbia University in New York City. I would like to thank James Im for giving me the opportunity to join his group and for the many instructive and silly discussions we had. Also, I would like to thank Alex Limanov for his experimental support, Bert Crowder for teaching me many small things, Brandon Turk for helping me with experiments, John Leonard and Dong Byum Kim for helping me with heat-flow simulations and Chad Gurley for his support of the group and also Robert Sposili, Sharona Hazair, Hans Cho and Jae Beom Choi. I would like to thank Barbara Algin and Marlene Arbo for arranging my stay at Columbia.

Als laatste wil ik al mijn vrienden, mijn ouders en naaste familie bedanken voor de vriendschap en de liefde die ik van hen heb mogen ontvangen. In het bijzonder wil ik mijn paranymfen bedanken: David Nieuwstad en Bas Mijling die door hun vriendschap een grote bijdrage geleverd hebben aan mijn werk. Bovenal wil ik Shirley van Meerendonk bedanken die mijn lieve vriendin is en die veel begrip heeft getoond voor mijn situatie en mij vooral naar het einde toe heeft omringd met zorg en liefde.

Paul

About the Author

Paul van der Wilt was born in Boskoop, the Netherlands, on July 29, 1973. He obtained his VWO diploma in 1991 from the Christelijk Lyceum in Alphen aan den Rijn. In that year he started his study at the department of Electrical Engineering at Delft University of Technology. In his third year he combined this for one year with Industrial Design Engineering and in August 1997 he graduated in Electrical Engineering. His master thesis work was performed in the Laboratory of Electrical Components, Materials on Technology (ECTM) led by Prof. Kees Beenakker and under supervision of Dr. Ryoichi Ishihara. The research was performed at the Delft Institute of Micro Electronics and Submicrontechnology (DIMES).

In November 1997 he continued his research in the same group towards his Ph.D. degree. During his Ph.D. research he co-founded the student association Micro Electronics and Silicon Technology (MEST) and he was a teaching assistant for the practical training on IC-technology. Although initially planning to work on properties of thin-film transistors, the focus of his research gradually switched to the pulsed-laser crystallization of thin silicon films. For this reason, he temporarily joined the group of Prof. James Im in the Program of Material Science at Columbia University in New York City, USA from January to December 2001. In September 2002 he started his current appointment as a post-doctoral researcher in the same group. As a member of the SLS technology transfer team he is involved in the education of industrial customers about this process. He is also involved in various research projects of the group, which are carried out in cooperation with industrial partners.