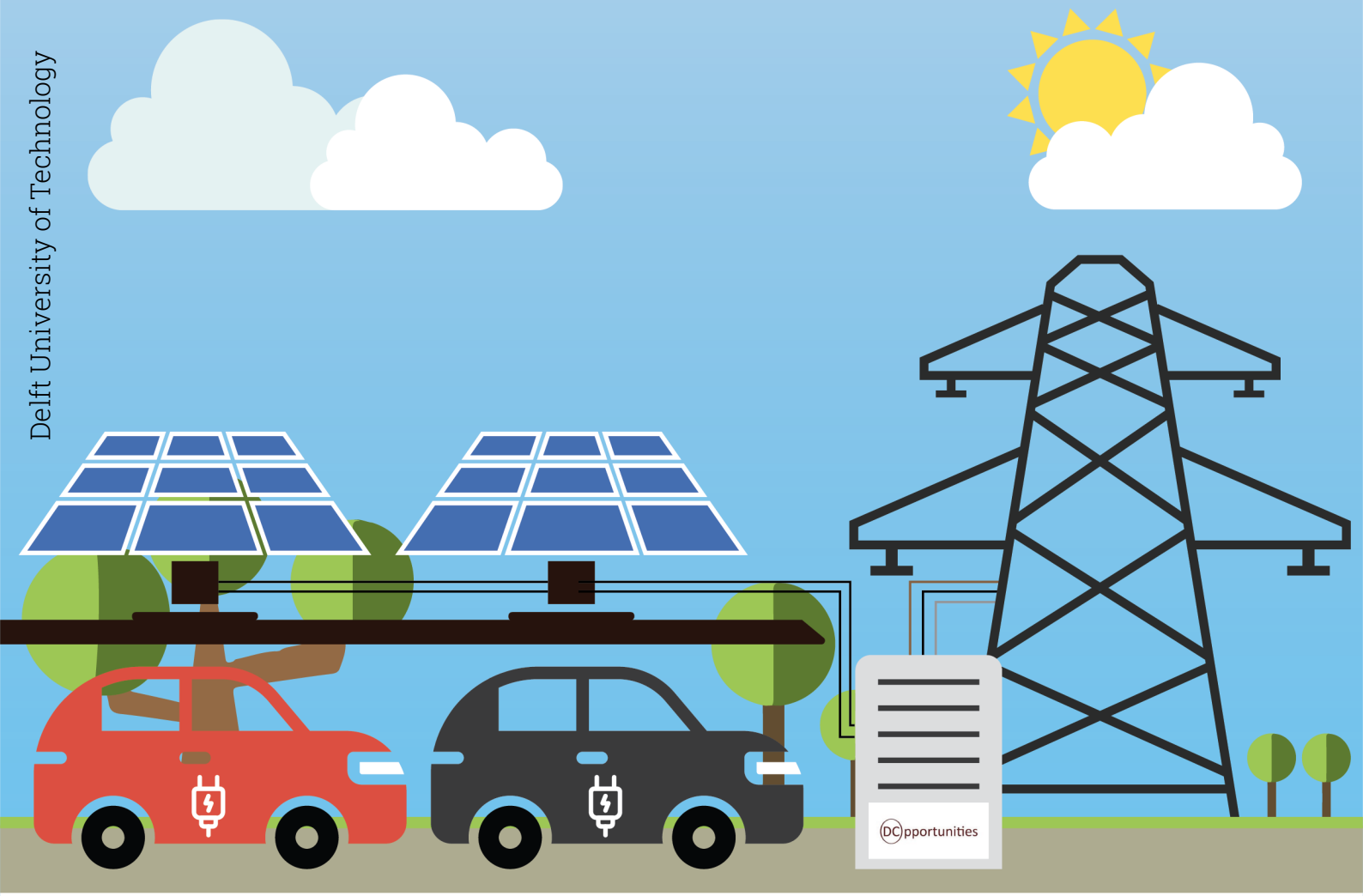
Isolated Bidirectional DC-DC Converter for Modular Medium Voltage (10 kV) Solid-State Transformer Application

A modular approach to connect low voltage DC grid to medium voltage AC grid

Deepak Bikkina

Delft University of Technology



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Isolated Bidirectional DC-DC Converter for Modular Medium Voltage (10 kV) Solid-State Transformer Application

A modular approach to connect low voltage DC grid to medium voltage AC grid

by

Deepak Bikkina

to obtain the degree of Master of Science

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Thesis committee:	Dr. Ir. Zian Qin (TU Delft Supervisor)
	Prof. Dr. Ir. Pavol Bauer (TU Delft)
	Dr. Ir. M. Ghaffarian Niasar (TU Delft)
	Dr. Ir. Laurens Mackay (DC Opportunities)
PhD advisor:	Ir. Adnan Ahmad (TU Delft)
Company supervisor:	Ir. Jesse Echeverry (DC Opportunities)

This thesis is confidential and cannot be made public until August 22, 2025.

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Abstract

Recently, there have been numerous DC microgrids coming up in every sector. Some of these microgrids operate as independent entities with their own renewable energy sources, active loads, distribution networks and energy storage units. However, they are not highly reliable as the renewable energy sources are location and climate dependent. Having a large energy storage unit can be one possible solution, but that involves high expenditure and occupies a large amount of space. Thus, an alternative is to connect the independent DC microgrid to an established AC grid. With the advancements in power electronic technologies, such a connection can be established by a multi-stage converter known as Solid state transformer (SST).

Numerous studies have been conducted on SSTs for low-voltage levels, and there is a wide scope for research in the area of medium and high-voltage converters. Also, the scope of using Planar transformer (PT) as high-frequency transformers in DC-DC converters for medium and high-voltage applications is yet to be extensively explored. Hence, the main focus of this thesis would be to develop an isolated bidirectional DC-DC converter with a planar transformer that can be used in an SST which can potentially connect a low-voltage DC microgrid comprising a solar-based car parking system, to a medium-voltage AC grid.

Firstly, various DC-DC converter topologies have been investigated, and the single phase Dual active full bridge (DAFB) is chosen as the best suitable topology for this application. Secondly, various control strategies have been investigated, and single-phase shift control has been implemented due to its simple control techniques and low data transfer requirement across high isolation. Thereafter, a script is developed to identify the optimal parameters for the Dual active bridge (DAB) and PT design. Further, the planar transformer with high isolation is realized by considering various factors like shielding and termination into account. Finally, a single-cell prototype is developed and tested for DAB operation and isolation requirement of the designed planar transformer.

The result of the presented work is a single-cell isolated bidirectional DC-DC converter rated for 12 kW designed and developed with a PT rated for 16.3 kV isolation.

Acknowledgement

The research work has been carried out at the DC Systems, Energy Conversion and Storage group at TU Delft in collaboration with DC Opportunities. I take this opportunity to express my gratitude to all the people who supported me, motivated me and challenged me to complete this project and my Master's.

Firstly, I would like to thank my parents and my amazing brother who stood beside me and pushed me further in every aspect of life. All of their love and affection have molded me into the person I am today. I would always be grateful to have them as a part of my life.

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I am grateful to Dr. Ir. Laurens Mackay and Ir. Jesse Echeverry for giving me an opportunity to work on this topic at DC Opportunities. I appreciate their constant supervision and help throughout the thesis. The numerous brainstorming discussions, new floating ideas and cross–questioning motivated me constantly. Every person at DC Opportunities has helped me complete this thesis. I extend my gratitude to them as well.

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Finally, there are many others who helped me cross all hurdles and who have put me on the right track in life. Their names might not have been listed here but are strongly imprinted in my heart. Thank you for all the help, support, love, and affection!

Deepak Bikkina
Delft, August 2023

Contents

List of Figures

List of Tables

Nomenclature

List of Acronyms

DC-MGs	DC microgrids
RESs	Renewable energy sources
ESSes	Energy storage systems
EVs	Electric vehicles
MGs	Microgrids
SST	Solid state transformer
LV-DC	Low-voltage bipolar DC
MV-AC	Medium-voltage AC
LFTs	Line-frequency transformers
PT	Planar transformer
PCB	Printed circuit board
MV	Medium voltage
DAB	Dual active bridge
DAHB	Dual active half bridge
DAFB	Dual active full bridge
ZVS	Zero voltage switching
EMI	Electro-magnetic interference
MMF	Magneto-motive force
SPS	Single phase shift
EPS	Extended phase shift
TCM	Triangular current mode
TzCM	Trapezoidal current mode
MMC	Modular multilevel converter
ZCS	Zero current switching
CES	Community energy storage
PI	Planar inductor

Symbols

Symbol	Description	Unit
A_c	Core area	[m^2]
A_g	Air gap	[m]
A_l	Inductance factor	[H/turn^2]
b_w	Width of track of transformer winding	$[m]$
B_{eff}	Effective flux density	[T]
C_d	Differential mode filter Capacitor	[F]
C_{eq_lead}	Leading bridge equivalent output capacitance	[F]
C_{eq_lag}	Lagging bridge equivalent output capacitance	[F]
C_{in}	Input filter capacitance	[F]
C_{OSS}	Output capacitance of the MOSFET	[F]
C_{out}	Output filter capacitance	[F]
C_{pi}	Pi filter Capacitor	[F]
C_{r1}, C_{r2}, C_{ra}, C_{rb}, C_{rc}	Resonant capacitors	[F]
C_y	Y filter Capacitor	[F]
D	Duty cycle	-
D_1 to D_{12}	Diode	-
E	Energy of the inductor	$[J]$
E_{off}	Turn-off energy	$[J]$
E_{oss}	Output capacitance stored energy	$[J]$
f_s	Switching frequency	[Hz]
$f_{s_{max}}$	Maximum switching frequency	[Hz]
H	Magnetic field strength	[Am^{-1}]
H_w	Window height of the core	[m]
i_{cap}	DC link capacitor current	[A]
i_{DAB}	Single cell DAB output current	[A]
i_{inv}	Single cell inverter current	[A]
I_{lk_p}, $I_{p_{rms}}$	Primary side RMS current	[A]
I_{lk_s}, $I_{s_{rms}}$	Secondary side RMS current	[A]
I_m	Magnetizing current	[A]

Symbol	Description	Unit
I_o	Single cell DAB average output current	[A]
I_p	Peak value of inverter current	[A]
$I_{p_{sw_{rms}}}$	Primary switch RMS current	[A]
$I_{s_{sw_{rms}}}$	Secondary switch RMS current	[A]
L_d	Differential mode filter inductor	[H]
L_k	Inductor	[H]
L_{lk}	Leakage inductance of transformer	[H]
L_{lkp}, L_{lks}	Primary and secondary side leakage inductance	[H]
L_m, $L_{m(eff)}$	Effective magnetizing inductance	[H]
L_{r1}, L_{r2}, L_{ra}, L_{rb}, L_{rc}	Resonant inductors	[H]
L_s	Required series inductance of DAB	[H]
m	Modulation index of inverter	-
M	Modulation index	-
MPL	Mean path length of the core	[m]
n	Turns ratio	-
N	Number of turns	-
N_{core}	Number of parallel cores	-
p_1, p_2	Primary and Secondary instantaneous powers	[W]
P	Power rating of the DAB	[W]
P_{max}	Maximum power rating of the DAB	[W]
P_{PI}	Core power loss in planar inductor	$[W]$
P_{psw}	Per switch losses	[W]
P_{PT}	Core power loss in planar transformer	$[W]$
$P_{SST_{max}}$	Maximum power rating of the SST	[W]
Q	Quality factor	-
Q_1 to Q_6	Switch	-
R_{damp}	Damping resistor	[Ω]
$R_{ds(on)}$	On-state resistance of the switch	[Ω]
$R_{th(cs)}/R_{th_{CS}}$	Case to sink thermal resistance	$[^oC/W]$
$R_{th(jc)}/R_{th_{JC}}$	Junction to case thermal resistance	$[^oC/W]$
$R_{th(sa)}/R_{th_{SA}}$	sink to ambient thermal resistance	$[^oC/W]$

Symbol	Description	Unit
S_1 to S_{12}	Switch (MOSFET)	-
t_{db}	Dead band time	[s]
T_a	Ambient temperature	$[^oC]$
T_{HS}	Heatsink temperature	$[^oC]$
T_j	Junction temperature	$[^oC]$
T_{PI}	Core temperature of the planar inductor	$[^oC]$
T_{PT}	Core temperature of the planar transformer	$[^oC]$
T_{sw}	Switching time period	[s]
v_1, v_2	Primary and secondary voltage across the transformer	[V]
V_{core}	Volume of the core	$[m^3]$
$V_{dc(op)}$	Output voltage of the DC-DC converter	[V]
$V_{ll(rms)}$	Line to line RMS voltage	[V]
$V_{ph(p)}$	Phase voltage peak	[V]
V_{pri}	Input voltage of DC-DC converter	[V]
V_{sec}	Output voltage of the DC-DC converter	[V]
Z_{in}	Input impedance of the converter	[Ω]
Z_{out}	Output impedance of the converter	[Ω]
α, β, C_m	Steinmetz coefficients	-
Φ	Phase shift angle	[Radians]
ϕ	Phase shift	-
ρ	Resistivity of copper	$[\Omega m]$

1

Introduction

In this chapter, the motivation for this research thesis is discussed. An overview level of information is given about the project details and two important technical terminologies - SST and planar magnetics. The system-level design strategy is then developed, and the final research questions are stated. The thesis' structure is finally presented, briefly outlining each chapter.

1.1. Motivation - Scale-up of DC-MGs and the Need for Connection to AC Grid

As estimated by the International Energy Agency(IEA), the global energy demand in 2040 will reach up to 25% higher than what it was in 2017. This estimate is based on the assumption that the energy systems are efficient which results from the massive transformation of the power sector, as the modern ways of generating, transporting and storing energy are very different from the traditional ones [1]. In order to facilitate efficient energy systems, Renewable energy sources (RESs), Energy storage systems (ESSes) and new types of loads like Electric vehicles (EVs) and smart street-light systems are merged into a sub-group of flexible entities called Microgrids (MGs) and are operated independently [2]. Over 30% of new electricity connections are estimated to be served by the mini-grids and MGs by 2030 [1]. This number goes up to 70% for rural areas [3].

With a significant increase in these local energy hubs, critical analysis of the control of local power flow and external power flow (to and from the AC grid) becomes necessary. Most of the RESs have fluctuating behaviour, and as a result, the adaption of power flow to loads and ESSes has to be ensured to keep the system operational [4]. This makes the stand-alone DC-MGs less reliable. However, the likelihood of a power shortage in the local network decreases when it is possible to link the isolated DC-MGs to the AC grid. This also can eliminate the use of bulky ESSes that would be needed otherwise.

When the system consists of MGs, ESSes and a connection to the grid, it can perform the role of Community energy storage (CES) and can assist in achieving a better energy market. Recent research justifies that such CES systems also contribute to additional benefits like peak shaving and demand response [5], [6].

1.2. Project Specific Background

A solar-based car charging can be implemented in any commercial/tech-hub sector parking area, which can be powered by a 1-2 MW solar unit to maintain a +700 V/-700 V bipolar DC-MGs. As mentioned previously, solar energy is highly fluctuating in terms of power delivery and hence cannot act as the only source of energy to power the DC-MGs. Hence, in order to improve the reliability, either large ESSes have to be installed or a connection to the AC grid needs to be established. The latter can be done with the help of a SST, explained in the following sub-section. Installation of large ESSes has a few drawbacks, especially with respect to space and cost. Thus, a SST can be designed to establish a connection between the Low-voltage bipolar DC (LV-DC) grid, operating at +700 V/-700 V, to a Medium-voltage AC (MV-AC) grid operating at 10 kV (line-line RMS). A basic schematic of system level overview is given in figure 1.1.

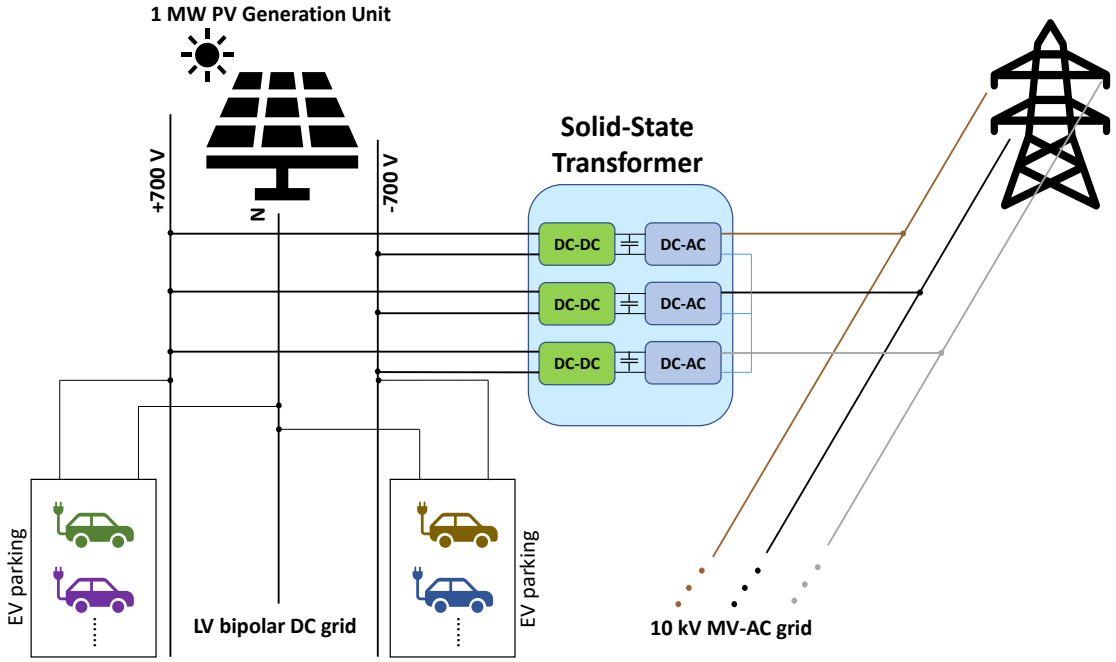


Figure 1.1: Basic system level overview

Powering up a car charging unit like this with renewable energy can aid in moving a step closer to carbon neutrality. The reduction in conversion steps between AC and DC would improve the efficiency of the entire system and would therefore have lesser energy demand.

1.2.1. Solid-State Transformers (SST)

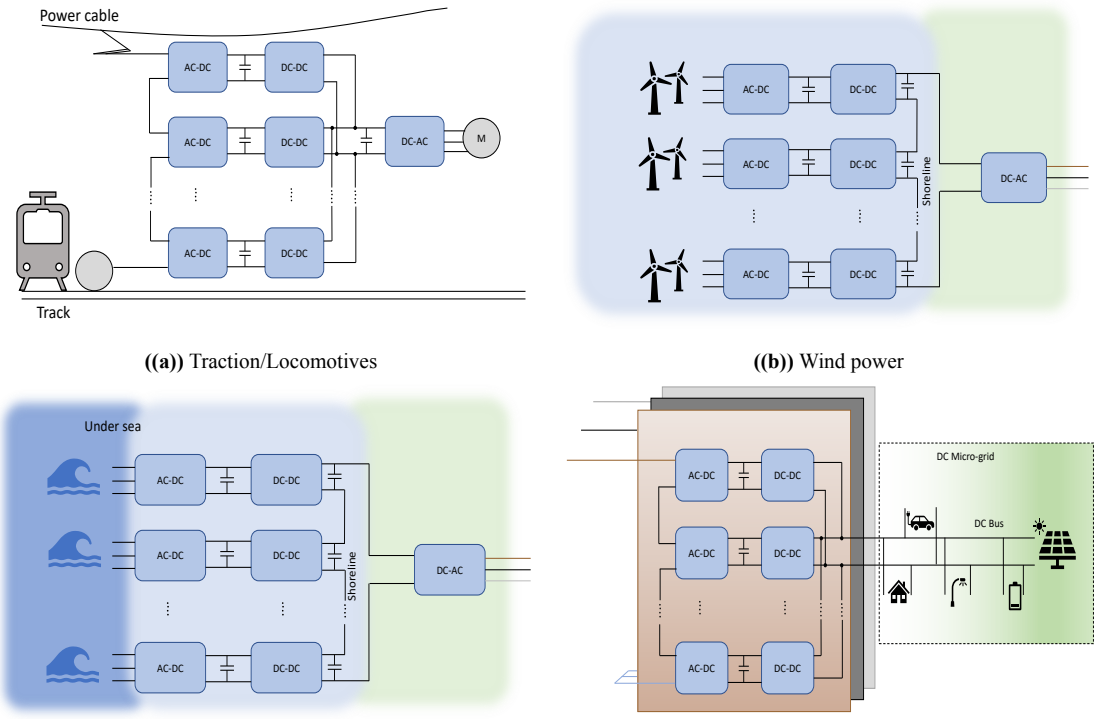
The development of smart DC-MGs has unfolded wide use of power electronic converters for power system applications. One such converter is SST. The concept of SSTs was initially introduced by William McMurray [7]. It is essentially a converter that replaces Line-frequency transformers (LFTs) with high-frequency converters. This enables a reduction in the size of the entire unit.

Due to various advantages and possible applications, the interest in SST has grown multi-fold

in recent times. Some of the advantages of SSTs over LFTs are listed [8], [9]:

- **Smaller volume and weight:** Transformer size is inversely proportional to frequency. Since the SST utilizes a high-frequency transformer, the size is considerably small and thus makes it less bulky.
- **High controllability:** The use of power electronics makes the converter (transformer) more controllable.
- **Can act as isolation unit:** In case of fault, the power through the converter can be stopped by opening the switches, and thus, it can perform the role of circuit breaker (isolation unit) in the system.
- **No effect of voltage swell or sag:** The DC link capacitor maintains the link voltage, and hence the converter does not create any voltage swell or sag.
- **Fast fault detection and protection:** As the voltage and current control loops are used for power transfer, the measured data can be used for immediate fault disconnection.
- **Unity power factor:** If the SST also employs an AC/DC conversion (rectifier) stage, the unity power factor can be maintained in the system.

Many research groups are focusing on various architectures and topologies of SSTs, leading to the replacement of LFTs in various sectors. Some of the fields where SSTs are being implemented are shown in figure 1.2 [10]. In this thesis, the focus is on the smart grid scheme as the goal is to connect the AC grid to the DC grid.



((a)) Traction/Locomotives

((b)) Wind power

((c)) Tidal power

((d)) Smart grid scheme

Figure 1.2: Various applications using SST

1.2.2. Need for Isolation and Planar Magnetics

In any converter, isolation is generally provided for safety requirements. An isolated converter consists of a transformer, which electrically isolates the primary and secondary sides. By using a transformer, the currents from the primary source will not enter the secondary load and vice-versa. In this particular application, isolation serves two main purposes [11]:

- Prohibit fault currents travelling between the AC and DC grids;
- Provide better switching utilization by reducing reactive power circulation.

In order to provide galvanic isolation, the DC-DC converter stage, shown in figure 1.1, has to be an isolated converter that employs a medium/high-frequency transformer. Recent research focuses on the use of PTs in the isolated DC-DC converters application. PTs are the replacement for traditional wire wound transformers where the copper windings are designed as flat wires on the Printed circuit board (PCB). These windings are stacked vertically on top of one another and are placed horizontally along the length of the core. Figure 1.3 shows a simple PT with separate primary and secondary winding. PTs offer various advantages over wire wound transformers [12].

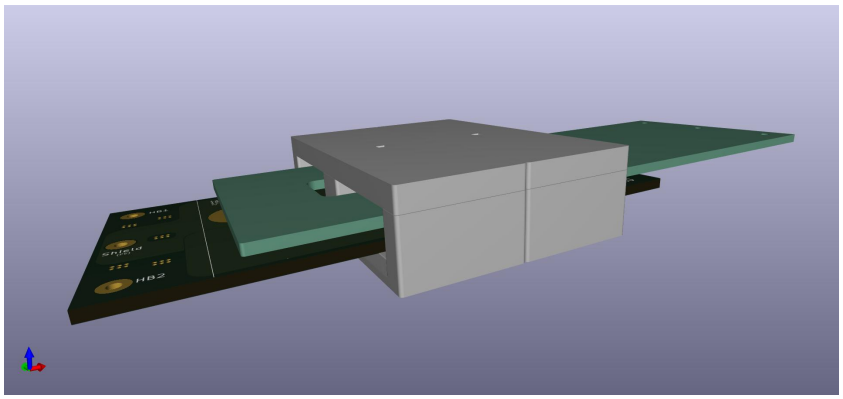


Figure 1.3: Planar transformer model with separate primary and secondary windings

Some of these advantages of PTs are listed below [12]:

- Windings have a very low thickness, which reduces skin effects at high frequencies.
- Wider structure of the core enables better cooling when mounted on the heatsink.
- Since the winding arrangement is structured, parasitic inductance and capacitances can be very well controlled.
- Once the windings are designed, mass production of the PCBs and hence transformers becomes easy and efficient.
- The planar core structure provides a higher magnetic-cross section area, thereby enabling fewer turns.
- It offers a lower profile, lower volume and lower core losses compared to wire wound transformers.

1.2.3. Modular SST realization

It can be seen from figure 1.1 that the SST employed for this application consists of two converter blocks per phase, i.e. DC-DC converter and DC-AC converter. According to the nominal values, the input to the DC-DC converter is 1400 V, and the output of the DC-AC converter is 8.165 kV (peak) according to equation (1.1).

$$Phase\ voltage\ peak,\ V_{ph(p)} = \frac{V_{ll(rms)}}{\sqrt{3}} * \sqrt{2} = \frac{10\ kV}{\sqrt{3}} * \sqrt{2} = 8.165\ kV \tag{1.1}$$

In order to achieve a multi-level modular structure, a cellular-level connection is designed with parallel input and series output as shown in figure 1.4. This approach ensures the modularity of the converter. Depending on the voltage and power levels, multiples of these cells can be connected in various configurations. This is done in order to utilize low-voltage-rated switches.

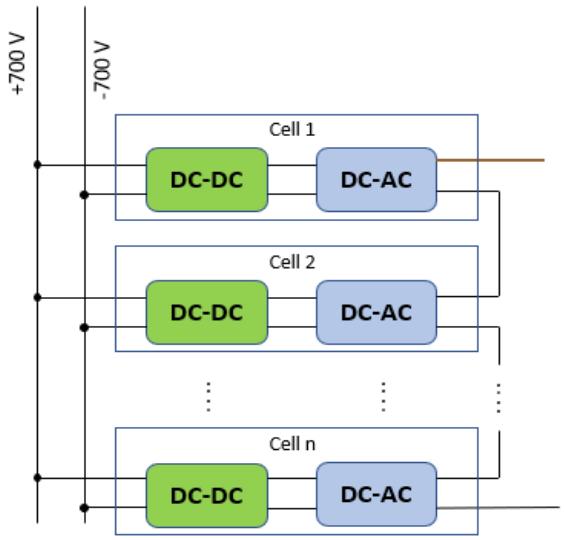


Figure 1.4: Single phase parallel input series output cellular-level connection

For this application, it is intended to use a 1:1 turns ratio DC-DC converter in order to use similar switches on both the primary and secondary sides. Hence, in order to achieve 8.165 kV peak voltage, 6 cells per phase are needed according to equation (1.2).

$$Number\ of\ cells\ per\ phase\ N_{cell/phase} = \frac{V_{ph(p)}}{V_{dc(op)}} * m = \frac{8.165\ kV}{1400} * 1 = 5.832 \approx 6 \tag{1.2}$$

Note that the modulation index is assumed to be 1. However, a higher modulation index can be achieved by space vector modulation or third harmonic injection in sinusoidal pulse width modulation to achieve higher voltages. Considering 6 cells per phase and three phase network, 18 cells in total are needed. Block diagram representation of the complete SST with cellular-level structure is shown in figure 1.5.

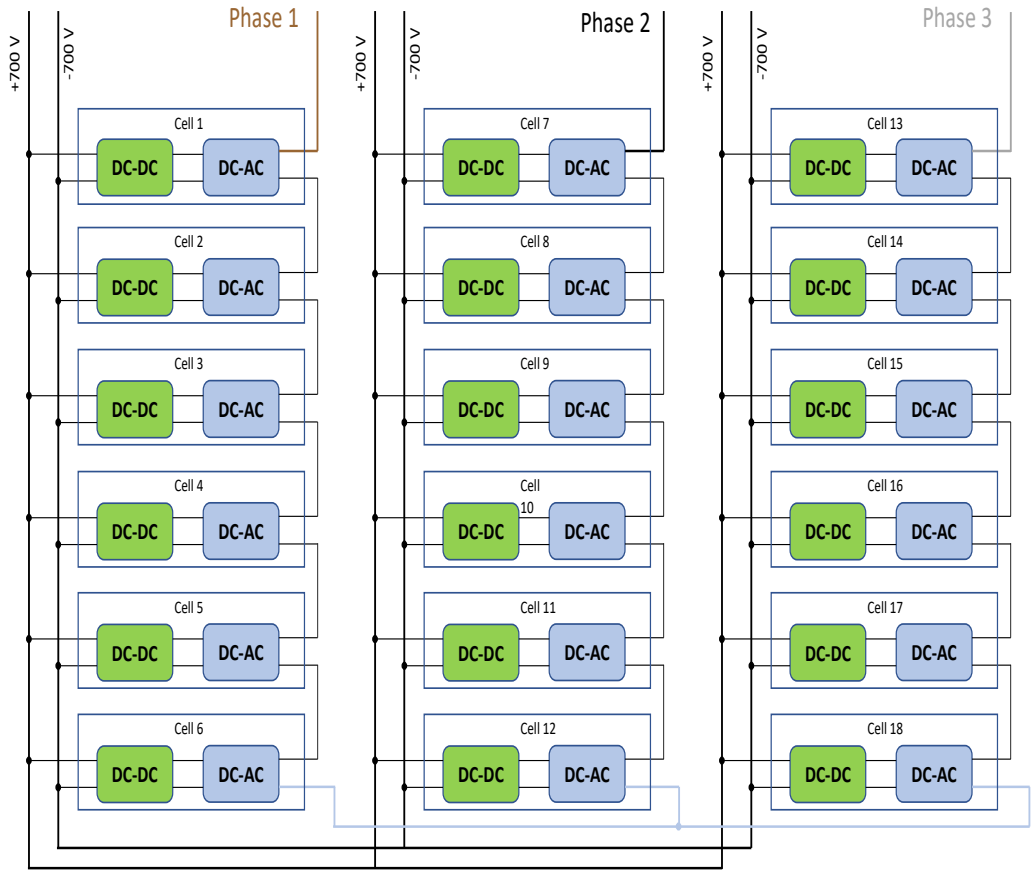


Figure 1.5: Block diagram of cellular-level structure of SST

1.3. Research Questions

The objective of this thesis is to implement a prototype of a DC-DC bidirectional converter with Medium voltage (MV) isolation which can be implemented in a modular SST that connects the LV-DC grid to the MV-AC grid. The research questions addressed in this thesis are stated as follows:

1. *What is the most feasible DC-DC converter topology that can be implemented to develop a modular MV SST?*
2. *What is the most simple yet effective method of controlling this converter on a module and system level and its implementation?*
3. *How to optimally select the parameters of the finalized topology with planar magnetics integration and what are the constraints involved?*
4. *How to design and implement planar magnetics for the selected topology with high isolation and evaluate its effectiveness in comparison to non-planar magnetics?*

1.4. Structure of the Thesis

The above-mentioned research questions are answered in various chapters of the thesis and various design methodologies are discussed in detail. The structure of the thesis consists of seven chapters.

- **Chapter 1:** gives a brief introduction to the project and motivation for the thesis topic. A short introduction about SST and planar magnetics and their advantages are also given in this chapter. The chapter concludes by stating the research questions which are further answered in this thesis.
- **Chapter 2:** gives an introduction to various isolated bidirectional DC-DC converters. Detailed comparison in terms of efficiency, soft-switching range, design and control, power density and economic feasibility is done to select the most feasible DC-DC converter. Finally, the principle and operation of the selected topology are discussed in this chapter.
- **Chapter 3:** focuses mainly on the system-level control approach and various control strategies of the selected topology. The most simple yet effective control strategy is chosen after a careful comparison of all the control strategies. Further, the soft-switching range analysis is done considering the magnetizing inductance of the transformer. Finally, the feed-forward control technique and the droop control limits are discussed in this chapter.
- **Chapter 4:** gives the detailed design approach to build the converter. The chapter mainly focuses on the DAB with planar transformer script where-in the script objectives, constraints, formulas and results are discussed. This chapter also covers the DAB power rating calculation and the required DC-link capacitor rating calculation. Finally, the input EMI filter design is discussed in this chapter.
- **Chapter 5:** discusses the design and implementation of planar magnetics. Final design ideologies for the PT rated for MV insulation. Thereafter, a feasibility comparison of the Planar inductor (PI) and conventional wire-wound inductor is done in order to study the effectiveness of planar magnetics.
- **Chapter 6:** discusses the final hardware implementation and testing results. The procedure for curing epoxy for the secondary winding of the transformer is discussed here. Various tests performed on the PT and the single cell DAB converter are discussed in this chapter.
- **Chapter 7:** provides a conclusion to the thesis, on the selection, design and implementation of the isolated bidirectional DC-DC converter for SST application. The research objectives stated in Chapter 1 are answered here. This chapter then provides a brief description of the future scope of the project.

2

DC-DC Converter Topologies

In this chapter, various isolated bidirectional DC-DC converters will be reviewed. Thereafter, based on the requirements, feasible converters will be chosen and investigated further. Once the choice of the most optimal topology is made, a basic overview of the principle and operation of the finalized converter is explained.

2.1. Various DC-DC Converter Topologies

DC-DC converters can be broadly classified into isolated and non-isolated converters. The isolated converters can be further divided into non-bridge type switch configurations and half/-full bridge switch configurations. The latter can be further divided into converters with and without resonant types. Various topologies in this classification are shown in figure 2.1.

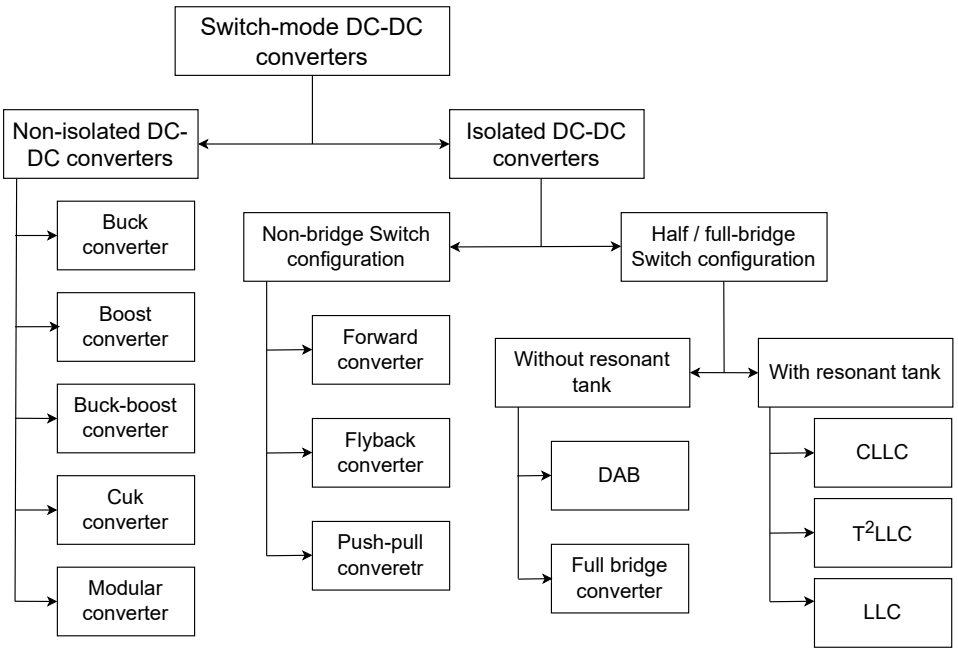


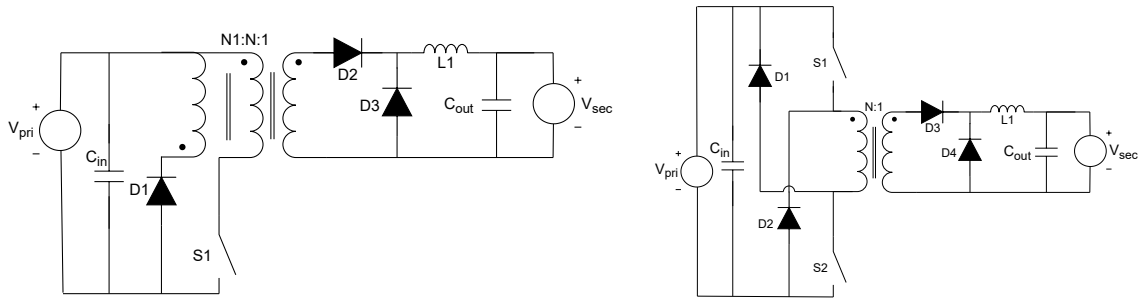
Figure 2.1: Classification of various DC-DC converters

Since one of the requirements for the project is that the converter has to be isolated, as mentioned in section 1.2.2, only the isolated converters are further investigated. It is important to note that one of the requirements is also bi-directional capability, and some of these converters are not inherently bidirectional. However, bi-directionality can be achieved by replacing the diode with switches in some cases or connecting two similar converters in an anti-parallel configuration, thereby activating each of them for operation in the respective direction.

In the following subsections, a brief overview of each converter is given, along with some pros and cons:

2.1.1. Forward Converter

The forward converter is the isolated version of the buck converter and, as such, is unidirectional. Figure 2.2 shows the circuit of the unidirectional forward converter with and without de-magnetizing winding.



((a)) With demagnetizing winding **((b))** Without demagnetizing winding

Figure 2.2: Unidirectional forward converter

The circuit shown in figure 2.2 b, can be modified to make the converter bidirectional. Figure 2.3 shows the circuit of the bidirectional forward converter. Apart from this topology, there are other topologies with resonant tanks mentioned in the literature [13]. In such circuits, the leakage inductance of the transformer is used along with capacitance to create a resonant tank.

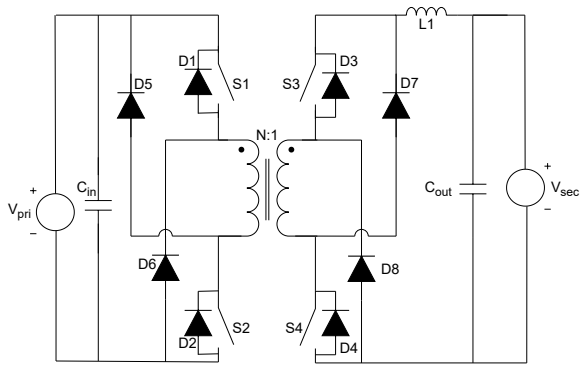


Figure 2.3: Bidirectional forward converter

The main advantage of a forward converter is the possibility to generate a continuous output current due to the presence of an inductor at the output. Some of the disadvantages are its complicated transformer design when an extra de-magnetizing winding has to be incorporated

and low core utilization since the core is excited only in one direction (flux changes from 0 to maximum value), implying that the core only operates in the first quadrant of BH graph. Also, it necessitates the use of a series DC inductor at the output side which is difficult to manufacture. Moreover, this type of converter is generally rated for low and medium-power applications (upto 500 W) [14]. Hence, this topology is not suited for the application.

2.1.2. Flyback Converter

The flyback converter is the isolated version of the buck-boost converter. Figure 2.4 shows the circuit of the unidirectional flyback converter.

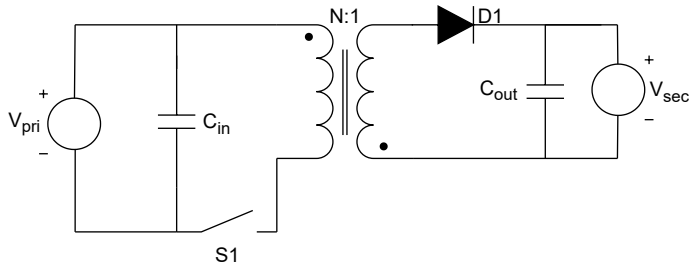


Figure 2.4: Unidirectional flyback converter

This unidirectional converter can be transformed into a bidirectional converter, as shown in figure 2.5. A voltage clamp snubber circuitry is needed to suppress the leakage current of the transformer in this topology [13].

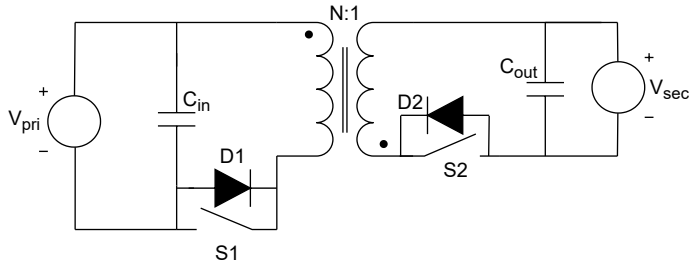


Figure 2.5: Bidirectional flyback converter

The main advantage of a flyback converter is that it is the simplest converter with a minimum number of components. However, this converter has significant drawbacks such as high voltage stress on the switches. However, this can be avoided by using two switches and diodes alongside the transformer. Another disadvantage is that, just like the forward converter, the transformer is excited only in one direction. Hence, this topology has low core utilization and low efficiency as well. This topology is not suited for the SST application as it is generally used for low-power applications

2.1.3. Push-pull Converter

The forward converter shown in figure 2.2 a, can be modified to effectively use the energy stored in the transformer. Thereby obtained converter is the push-pull converter. Hence, the

push-pull converter is also a buck-derived converter. Figure 2.6 shows the unidirectional push-pull transformer. As mentioned earlier, two of these can be connected in an anti-parallel configuration to form a bidirectional converter.

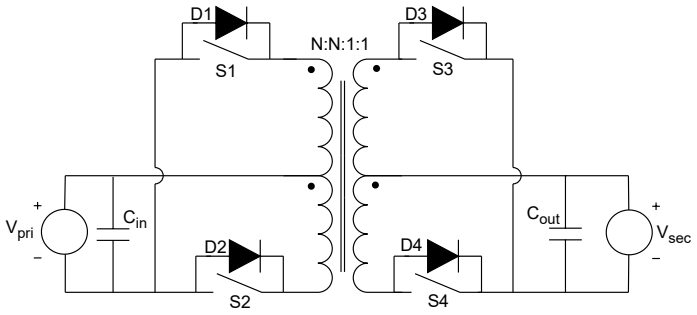


Figure 2.6: Unidirectional push-pull converter

The main advantage of this converter over the previously discussed forward and flyback converter is that the core of the transformer is excited in both directions. This implies that the flux changes from a maximum negative value to a maximum positive value, thereby effectively utilizing the core. However, even this type of converter is limited to power levels of around 1000 W [14]. Also, the efficiency of this converter compared to the bridge-based switch configuration converters like DAB and CLLC converters is low [14]. Hence, this topology is not selected for further investigation.

2.1.4. DAB Converter

A dual active bridge, in short, known as DAB, is made of two bridge networks connected with a medium or high-frequency transformer. It is one of the widely used topologies for isolated bidirectional DC-DC converters for high-power applications. Inherently this is a bidirectional converter and hence does not need two anti-parallel converter arrangements.

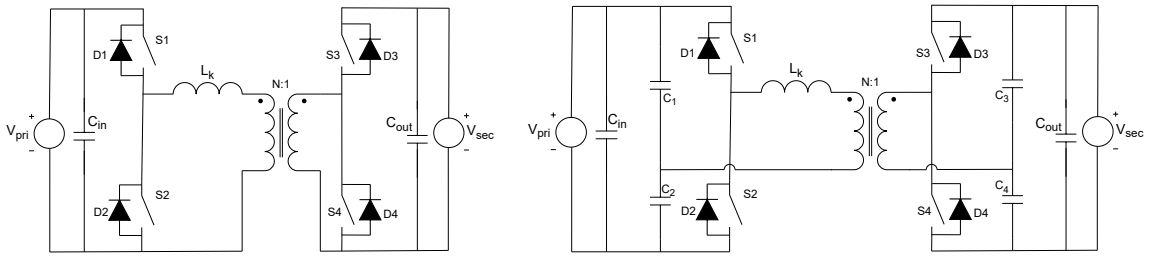
Dual active half bridge (DAHB)

When two switches are used in the bridges, the resulting DAB is referred to as a DAHB. This is shown in figure 2.7 (a). This type of converter has lower power capabilities compared to the full-bridge type (discussed further in this section). It also has unipolar flux swings, which can be avoided by using split capacitors, as shown in figure 2.7 (b). However, using these split capacitors has its own drawbacks. These include complex control to regulate the currents in the transformer and voltage balancing for the capacitors. Moreover, these capacitors should be rated to handle the full load current.

DAFB

A better solution is obtained when 4 switches are used in the bridges. Figure 2.8 shows the circuit of this type of DAB which is called a DAFB converter.

The main advantages of this type of converter are that its symmetrical structure makes the control of the converter simple, ZVS during turn-on is possible, many control techniques can be implemented, which are discussed in section 3.1 and higher power transfer is possible compared to half-bridge topologies due to bipolar flux swing. However, the downside of this type



((a)) Without split capacitors **((b))** With split capacitors

Figure 2.7: Dual active half bridge converter

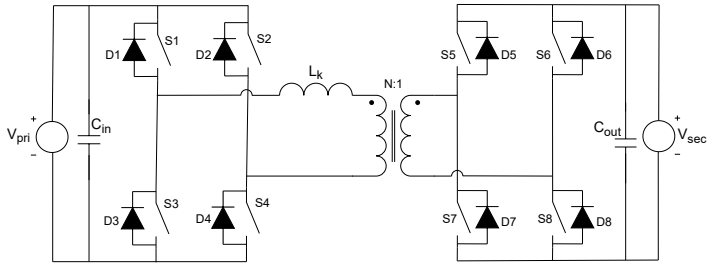


Figure 2.8: Dual active full bridge converter

of converter includes the possibility of losing ZVS at light loads, higher conduction losses due to circulating currents and the requirement of large capacitors at the input and output stage to have low ripple voltages. Various control strategies can be used to extend the ZVS range and reduce the circulating currents. However, they require more complex control algorithms.

Modular multilevel converter (MMC) based DAB

In this topology, the switches of DAB converter are replaced with sub-modules made of low-voltage switches. This topology is shown in figure 2.9. Each sub-module can be composed of a full-bridge or half-bridge topology [11].

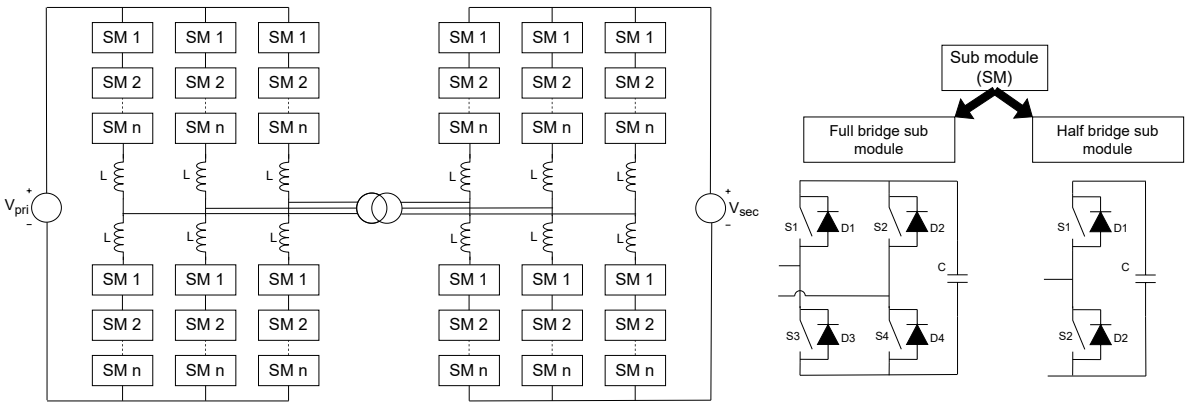


Figure 2.9: MMC based DAB schematic

The main advantage of MMC-based DAB is that it has a modular structure due to which higher voltage levels can be accounted for by just introducing additional sub-modules. Also, it inherently has all the advantages of a DAB converter. However, the main disadvantage is the number of components used, and the requirement of multiple passive components. Due to

the large number of components, the power density of the converter is low. Moreover, for a reliable converter, redundant sub-modules have to be added.

2.1.5. Full-bridge Converter

Similar to DAFB converter, the full bridge converter has two full bridge networks connected by a medium/high-frequency transformer. This configuration has a filter capacitor on the low voltage side and a large DC inductor in series with the output, creating a current-fed source, as shown in figure 2.10.

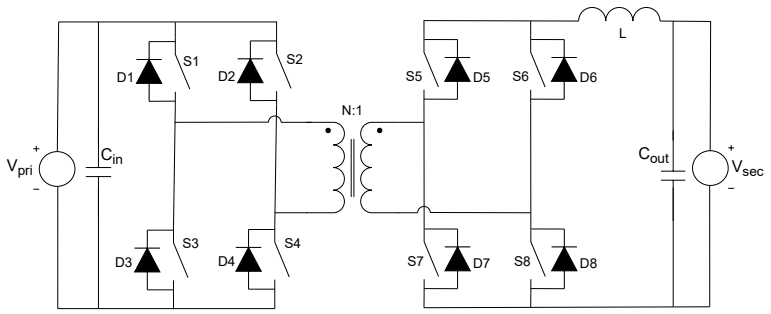


Figure 2.10: Full bridge converter

The main advantage of a full-bridge converter compared to DAFB converter is that the low voltage side capacitor ripple is low when power is transferred from high voltage to low voltage. However, the drawbacks are that the large DC inductor that is needed is difficult to manufacture and the current stresses on the switch are higher [15]. Due to this, the topology is not considered for the application.

2.1.6. LLC Converter

In order to reduce the effect of low ZVS range and low efficiency in DAFB, a resonant tank can be added, which makes the currents sinusoidal. As the name suggests, LLC is made up of two inductors and a capacitor resonant tank, as shown in figure 2.11.

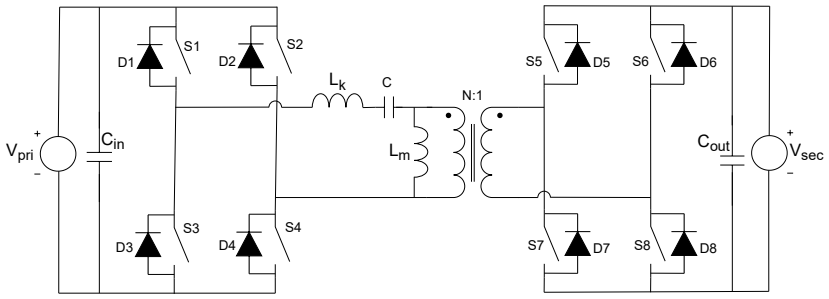


Figure 2.11: Bidirectional LLC converter

The advantage of this type of converter is that the sinusoidal currents make the RMS value of the currents low and hence have lower conduction losses in general. However, this comes at the cost of extra passive components. Also, the frequency has to be maintained at the resonant frequency to obtain the required voltage gain. Thus, the control strategy is more complicated.

Moreover, in the reverse direction, the losses can be significantly higher when the switching frequency deviates from the resonant frequency. As similar operations during power flow in both directions are desired, this topology is considered to be not feasible for the mentioned application.

2.1.7. CLLC Converter

The CLLC converter is the other resonant type of converter. As the name suggests, this converter employs two inductors and two capacitors in its circuit, which is shown in figure 2.12.

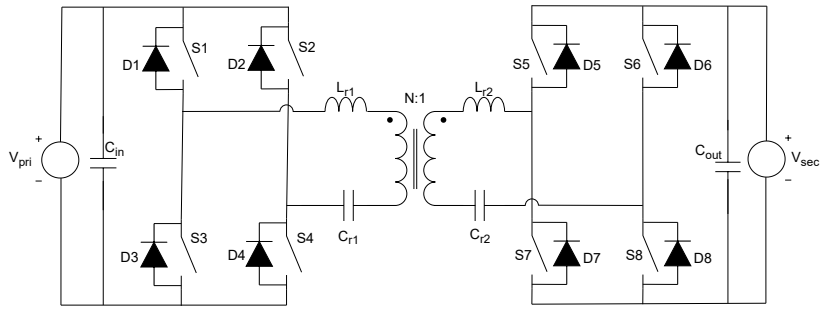


Figure 2.12: Bidirectional CLLC converter

The main advantages of this converter include bidirectional operation due to its symmetrical structure, better efficiency as it uses magnetizing inductance to achieve ZVS at the primary side for the entire load range and synchronize rectifier (SR) control strategy for the secondary side to minimize conduction losses. So, effectively only turn-off losses on the secondary side switches are prominent. This converter can overcome the drawback of high losses in the reverse direction in the case of an LLC converter. However, there are additional passive components involved, which increase the cost and make the analysis and design of the circuit more complex. Due to its critical advantages, this topology is considered for further analysis.

2.1.8. T^2LLC Converter

T^2LLC is an abbreviation for a three-phase triple voltage resonant converter. This topology is recently studied and is mainly employed to reduce the number of sub-modules by increasing the voltage of a single sub-module. It is a series-connected three-phase module used on the medium voltage side. The circuit representation of the topology is given in figure 2.13 [16].

The main disadvantage of this topology is that the voltage conversion ratio and the efficiency of the converter are very sensitive to resonant parameters in the circuit and consistency of three-phase resonant parameters should be ensured to achieve three-phase symmetrical operation. Also, designing a three-phase planar transformer is a challenging task. Furthermore, this topology employs split capacitors which need to be balanced. Hence, this topology is not further considered for this application.

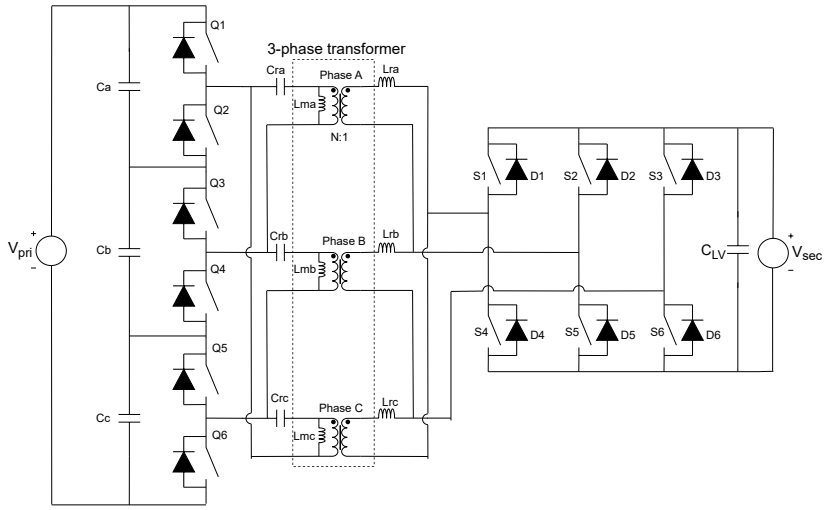


Figure 2.13: Three-phase triple voltage resonant converter

2.1.9. Multi-level Converters

All the converters discussed so far work at the best efficiency when the ratio of the primary and secondary voltages is close to the turns ratio of the transformer. To enable this, a second converter is added either on the primary side or on the secondary side without any galvanic isolation. This converter would act as a buck or a boost converter to maintain the voltages to the required level. However, this configuration of multi-level converters needs higher components making it bulky. Also, to maintain higher efficiency, this non-isolated stage of the converter has to be extremely efficient. Hence, the extra stage of buck or boost converter is not implemented for this project.

2.2. Comparison of feasible converters

In the previous section, a small overview of all the topologies was mentioned and based on the advantages, disadvantages and practical feasibility, DAB and CLLC topologies are chosen for further analysis. In this section, the theoretical comparison based on various literature is done. The analysis focused on 5 main topics - efficiency, soft-switching region, design and control complexity, power density and economic feasibility.

2.2.1. Comparison of DAB and CLLC converters

DAB and CLLC converters have been compared for various applications in the literature. In [17], a comparison of 1 kW DAB and CLLC converters in both half-bridge and full-bridge configurations is done. The results of the comparison have been summarized in the following subsection.

Efficiency

In general, both topologies have exceptional efficiencies. However, both of them operate at their maximum efficiencies under certain system conditions.

The CLLC converter being a resonant converter has its highest efficiency when the switching frequency is at the resonant frequency. When the switching frequency deviates from the resonant frequency, the converter enters either the inductive or capacitive region, as shown in figure 2.14, and thus creates circulating currents. These circulating currents cause circulating power losses and decrease the efficiency of the converter.

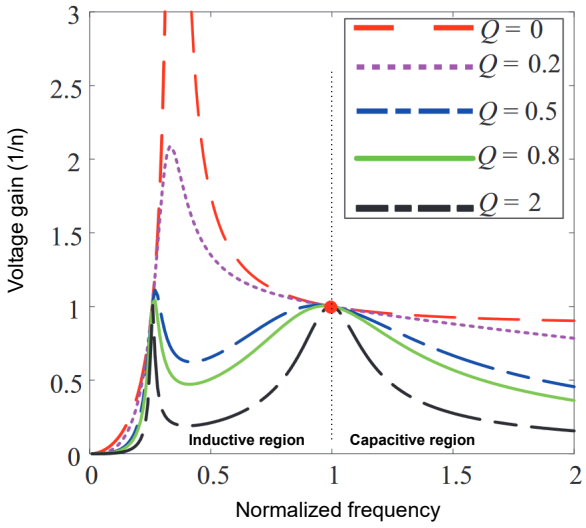


Figure 2.14: Voltage gain vs normalized frequency plot for various Q factors of a CLLC converter [18]

The DAB converter, in comparison to the CLLC converter, has lower efficiencies. This is because DAB loses ZVS at light loads and the SPS control technique causes high reactive powers within the circuit which also decrease the efficiency of the converter.

Soft-switching Region

To enable high efficiencies, operating the converter in the soft-switching region is very important. Hence, having a wider soft-switching region is highly advantageous. In the case of the DAB converter, both primary and secondary side switches can conditionally operate in ZVS mode. On the other hand, in the case of a CLLC converter, the primary side switches can operate with ZVS and the secondary side switches can operate with Zero current switching (ZCS) mode.

In the case of the full bridge CLLC converter, the magnetizing inductance has to be designed in such a way that equation (2.1) is satisfied to achieve ZVS on the primary switches.

$$L_m \leq \frac{t_{db}}{16 C_{OSS} f_{s_{max}}} \tag{2.1}$$

where t_{db} is the dead time between the switch commutation, C_{OSS} is the output capacitance of the MOSFET, and $f_{s_{max}}$ is the maximum switching frequency of the converter.

In the case of DAB, the soft-switching region is governed by the equations (2.2) and (2.3) which are further discussed in detail in section 3.2. DAB loses ZVS operation at light loads when SPS is implemented. Advanced control techniques are introduced in the literature to widen the ZVS range and hence improve efficiency.

$$\Phi > \frac{M - \frac{K_1}{K_2}}{2M}\pi + \frac{4\sqrt{L_s C_{eq\_lead}}}{T_{sw} M K_2}\pi \tag{2.2}$$

$$\Phi > \frac{1 - M\frac{K_1}{K_2}}{2}\pi + \frac{4M\sqrt{L_s C_{eq\_lag}}}{nT_{sw} K_2}\pi \tag{2.3}$$

To summarize, by proper design, soft-switching can be achieved over the entire region in the case of a CLLC converter. Whereas, in the case of DAB converter, the ZVS is lost during light loads.

Design and Control Complexity

As discussed in previous subsections, when CLLC is operated at the resonant frequency, the gain of the converter is 1/n and is independent of the load. Hence, the operating frequency of the CLLC converter has to be chosen in the close range of the resonant frequency. This topology is ideal for constant voltage, and variable load conditions. Moreover, the value of Q has to be chosen with utmost care as it has an influence on the operating frequency range. The lower the Q, the higher the operating frequency range. Hence, Q must be chosen carefully to limit the operating frequency range of wide output voltage converters.

On the other hand, in the case of DAB, the gains are fairly proportional to the phase shift angle. Hence, the design of DAB is fairly simple compared to the CLLC converter's resonant tank design and tuning.

Also, the control of DAB is fairly simple compared to CLLC control techniques. Additional dead time control has to be implemented in the CLLC converter to achieve reliable ZVS conditions.

Power Density

If the assumption is made that the leakage inductance of the transformer accounts for the required series inductances in the case of both converters, the CLLC converter has additional passive components - 2 capacitors. Hence, the power density of the circuit will be lower. This can be argued, as the filters needed to account for harmonics generated by square wave currents in DAB are large compared to the filters needed for the sine wave currents of the CLLC converter.

Economic Feasibility

As the CLLC converter needs a higher number of passive components, it becomes a costlier candidate out of the two. Though it is not a substantially high cost per converter, it becomes significant when the number of converters increases to form one big modular converter, which is the case in this application.

Conclusion

As a whole, the CLLC converter has better performance with respect to efficiency and soft-switching range. However, since the converter is highly sensitive to the parasitic components which affect the resonant tank, every cell in the SST module has to be carefully tuned. Since in this application, the DC-DC converter is connected to the single-phase inverter, the output

voltage is constantly oscillating. Hence the gain of the converter is continuously oscillating. Thus, the control complexity is further increased if the operating frequency is intended to be at the resonant frequency at all times. And finally, the cost of the converter is also higher. Hence, for this application, DAB is chosen as the ideal topology.

2.2.2. Comparison of single phase and three phase DAB converters

Since DAB proves to be a better topology for this application, further investigation is done on single-phase DAB and three-phase DAB converters.

A schematic representation of three-phase DAB is shown in figure 2.15.

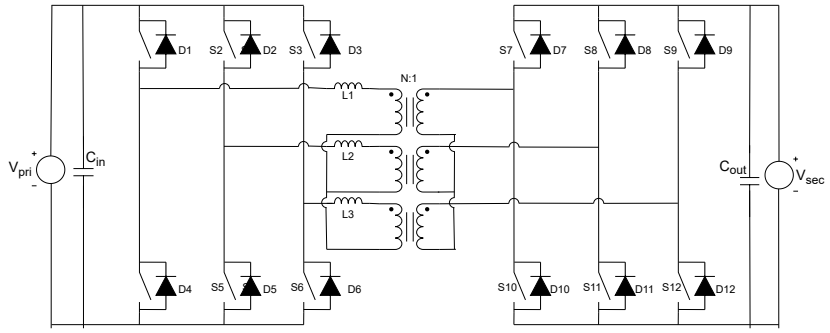


Figure 2.15: Three-phase DAB circuit

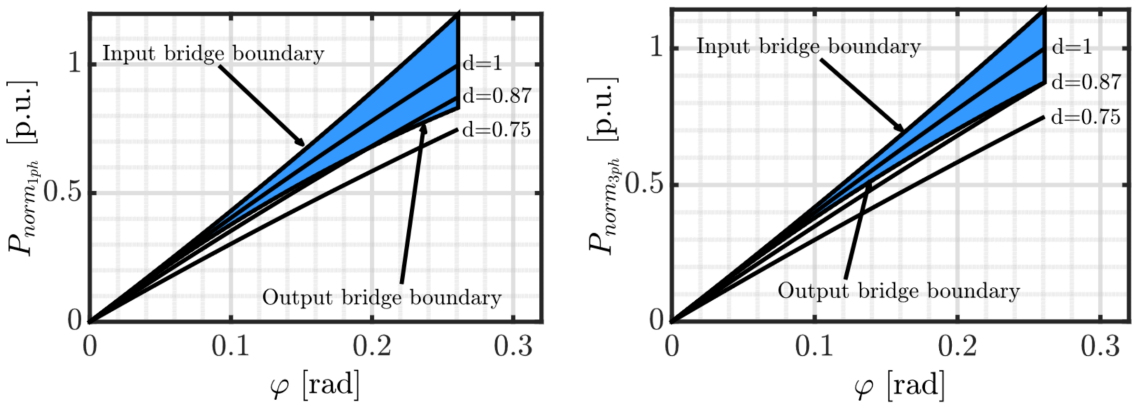
Efficiency

In the literature, 1-phase DAB and 3-phase DAB are frequently compared. In [19] and [20], the comparison of 3-phase DAB and 1-phase DAB was done based on the same amount of power transfer. In [19], it is concluded that the 3-phase DAB has lower back flow power and hence higher efficiency. In [20], similar conclusions are drawn. Segaran D, et al state that the RMS inductor currents in the 3-phase DAB are lower and hence the total conduction losses in all the switches are lower. This in turn states that the 3-phase DAB is more efficient. However, designing both converters for the same power does not draw fair results as the number of components used is different.

In [21], the comparison is done between the converters where the same power per switch is used. Blasuttigh N, et al implemented SPS control algorithm on both the converters for fair comparison and considered gate driver losses. They conclude that the only advantage of using a 3-phase DAB is the reduced size of filter capacitors due to lower ripples. But this comes at a cost of higher total switching losses, conduction losses and RMS currents despite its lower harmonic content.

Soft-switching Region

In [21], Blasuttigh N, et al concluded that the ZVS boundaries for 1-phase DAB are wider when the converters are designed for the same power per switch usage. Figure 2.16 show the comparison of 1-phase DAB and 3-phase DAB ZVS ranges. Also, the converters were tested with SPS control. In 1-phase DAB advanced modulation techniques can be used to widen the ZVS range and improve the performance. This is not possible in 3-phase DAB.



((a)) 1-phase DAB ZVS region **((b))** 3-phase DAB ZVS region

Figure 2.16: Comparison of soft-switching regions [21]

Design and Control Complexity

From a design perspective, planar transformer design for the 3-phase DAB is quite challenging. Also, having the three primary windings and three secondary windings on the same E core will be less effective with respect to window area usage. Also, 3 separate series inductors have to be designed in case of a 3-phase DAB converter as shown in figure 2.15.

Control complexity remains fairly the same. However, the possibility of advanced control techniques implementation in a 3-phase DAB circuit is completely ruled out.

Power Density

When operated with the same power for better efficiency, undoubtedly 1-phase DAB is more power dense due to a fever number of switches, gate drive units, series inductors and in most cases a smaller transformer size due to 1 primary and secondary windings. However, when the switches are used to their complete capacity, ideally, 1.5 times the power can be transferred by the 3-phase DAB. So, depending on the final transformer design and the application, the analysis can be made for the comparison of the power density of the converters.

Economic Feasibility

Again for the same amount of power transfer, in order to achieve higher efficiencies, the required number of components is higher. Hence, 1-phase DAB is a more economical option.

Conclusion

Based on the above findings, it can be summarized that designing the 3-phase DAB for the same power rating and under-utilizing the switch properties is not economical and feasible. And prioritizing maximum switch utilization leaves with better efficiency and ZVS range in case of 1-phase DAB converter. Also, designing the 3-phase planar transformer with given isolation requirements is quite challenging. Hence, the final choice of 1-phase DAB is made for this application. In this thesis, from here on DAB refers to a 1-phase dual active full bridge converter.

2.3. Basic Principle and Operation of DAB Converter

The analysis of the DAB starts with a simple schematic representation of the converter.

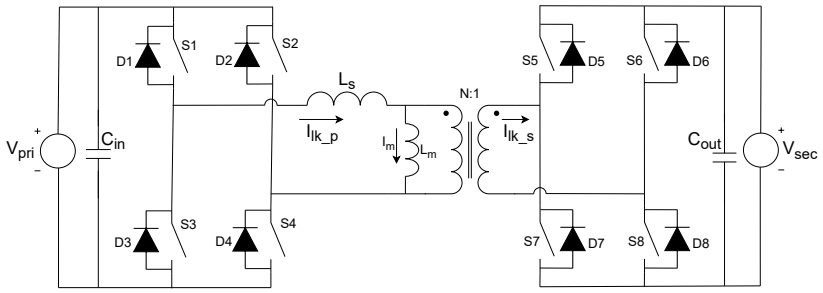


Figure 2.17: Dual active bridge converter with currents

2.3.1. Simplified circuit

In figure 2.17, the transformer magnetizing inductance is shown. However, it can be ignored and the transformer can be assumed to be ideal for the analysis purposes. By controlling the converter using single phase shift control (discussed further in section 3.1.1), a constant duty cycle of 0.5 can be implemented on both full bridges. Thus, the output of the primary side full bridge is a square wave. As the transformer is considered to be ideal and lossless, depending on the turns ratio, a scaled-up or scaled-down version of the same square wave appears on the secondary of the transformer. By referring all the secondary quantities to the primary, a further simplified model can be generated by replacing the full bridges with ideal voltage sources as shown in figure 2.18.

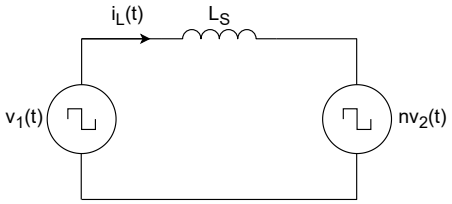


Figure 2.18: Simplified schematic of DAB circuit

2.3.2. Operating Principle

The voltage sources, shown in figure 2.18, receive or generate respective instantaneous powers as given by equation (2.4).

$$p_1(t) = v_1(t)i_L(t) \;\; and \;\; p_2(t) = nv_2(t)i_L(t) \tag{2.4}$$

where,

$$i_L(t) = i_L(t_0) + \frac{1}{L_s}\int_{t_0}^{t}(v_2(t) - nv_2(t))dt \tag{2.5}$$

From equation (2.5), it is clear that the amount of power transfer can be controlled by controlling $v_1(t), v_2(t)$ and/or $i_L(t)$. So indirectly, the control parameters of DAB circuit are:

- The phase shift angle (Φ) between $v_1(t)$ and $v_2(t)$
- The duty cycle, D_1 of $v_1(t)$
- The duty cycle, D_2 of $v_2(t)$
- The switching frequency

The most widely known control - SPS control, operates with constant duty cycles in both the full bridges and at a fixed frequency. So the power flow is controlled by controlling the phase shift between the two full bridges. The waveforms corresponding to SPS control are shown in figure 2.19. Here the power flow is from primary to secondary. Hence the primary voltage is leading the secondary voltage. The inductor current waveform is derived from the equation (2.5).

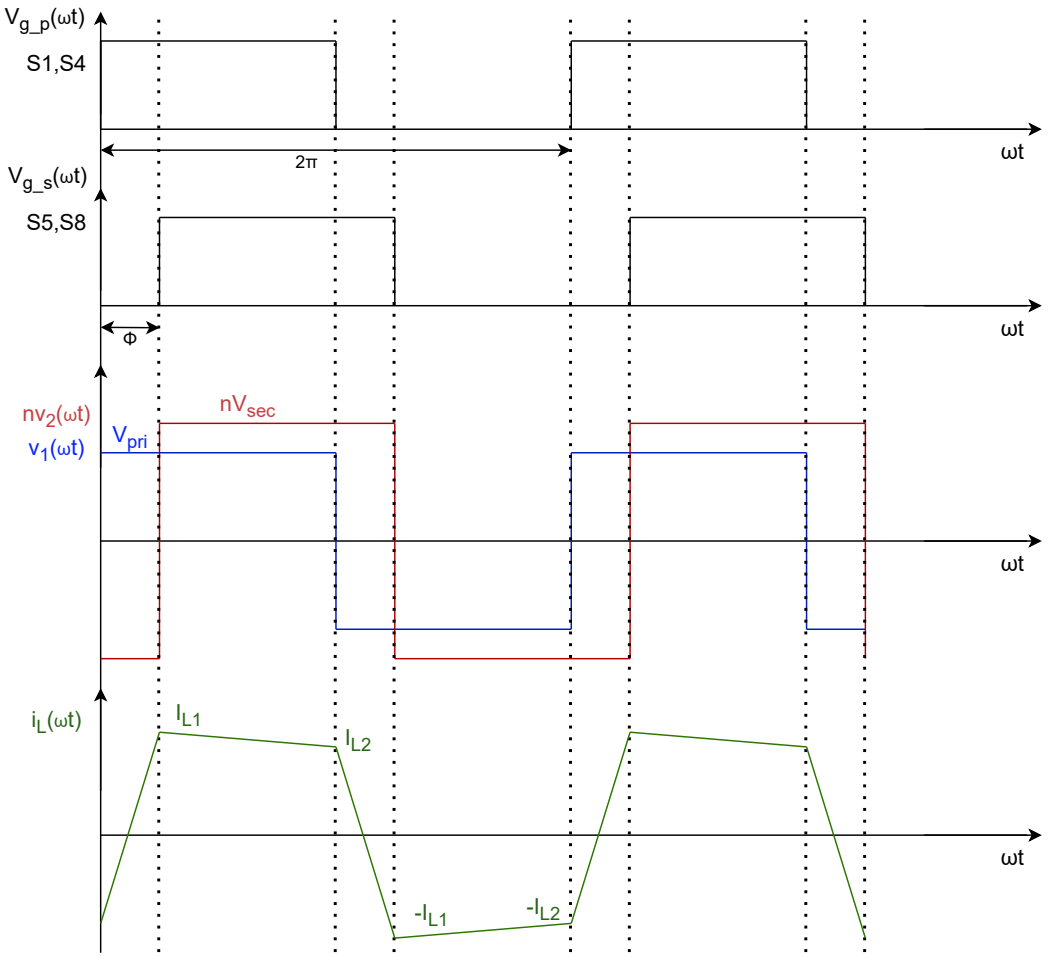


Figure 2.19: Dual active bridge waveforms

2.4. System level representation

Replacing the DC-DC converter with a DAB circuitry and the inverter cell with a full bridge network in figure 1.5 a system-level circuit schematic of the SST can be obtained. This is shown in figure 2.20. It consists of 6 cells per phase and all the inputs are connected to LV-DC in parallel and the outputs are connected in series to form a single phase connection of MV-AC line. So, in total, there are 18 DAB converters and full bridge networks connected in the system. One cascaded inverter network is composed of 6 full bridges and hence the system consists of 3 cascaded inverter networks.

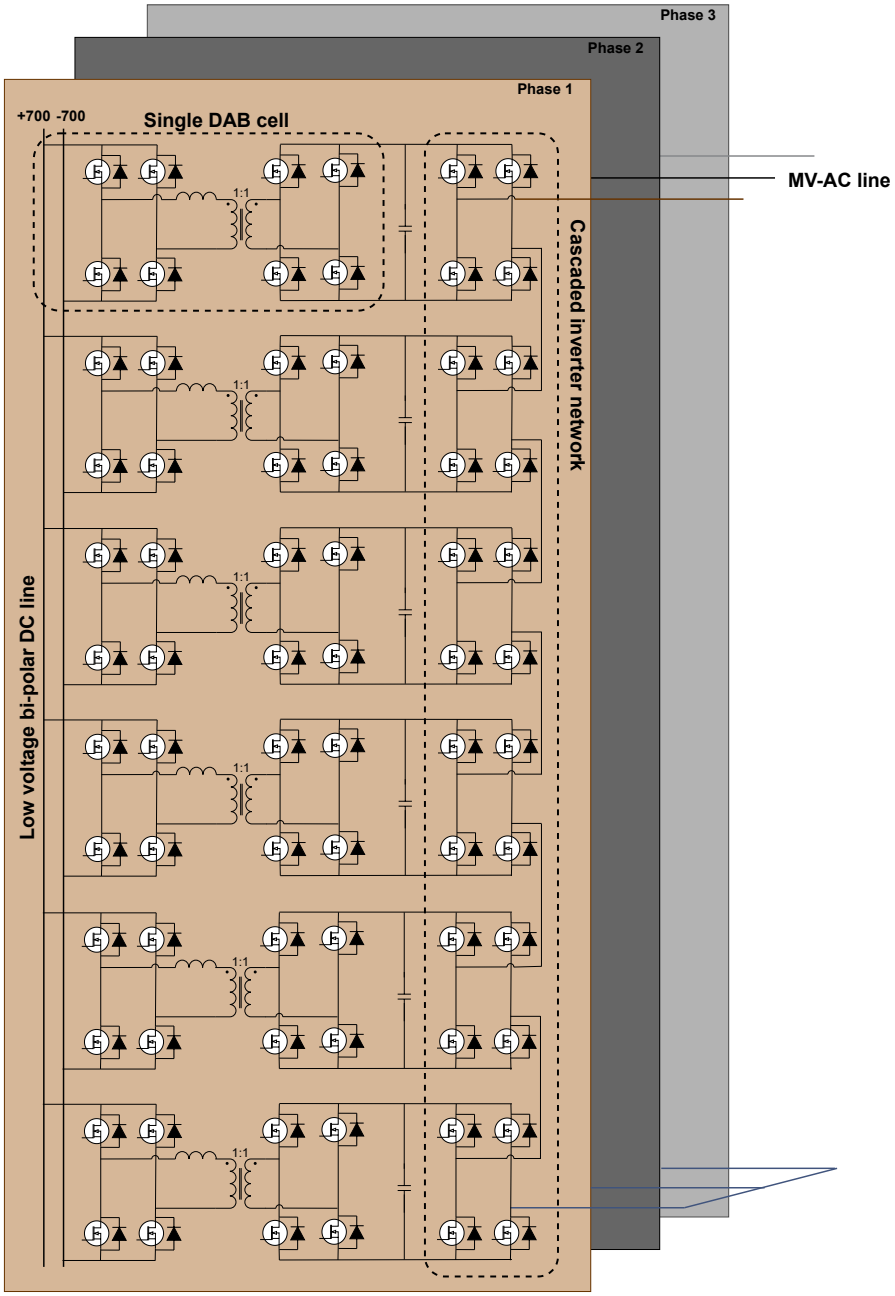


Figure 2.20: Circuit level representation of complete SST

2.5. Summary

In this chapter, various isolated bi-directional DC-DC converters have been discussed. Their advantages and disadvantages are evaluated with respect to the particular application of SST. Most of the converters have been eliminated because of their low-power application properties. Out of all the studied converters, CLLC and DAB are considered the most feasible ones and have been further analyzed and compared in terms of efficiency, soft-switching region, control complexity, power density and economic feasibility. After thorough analysis, though CLLC has better efficiencies and wider soft-switching regions, DAB has been selected to be the best fit for the application because of its simple and robust design and less complex control strategy.

Further studies on single phase DAB and three phase DAB are done based on the same parameters. Finally, single phase DAB proved to be a better fit in terms of economic feasibility and ease of design. The chapter concludes by discussing the basic operation principle of DAB and giving a brief circuit-level overview of the entire SST.

3

Control of DAB

In this chapter, the most popular control techniques of DAB are discussed broadly, and finally, based on the system requirements of the project, one of the control strategies is selected. Further, the selected control strategy is implemented along with feed-forward and droop control. Finally, the system level control of SST is discussed and the relevant PLECS model results are presented.

3.1. Various Control Techniques for DAB

In order to control the power flow in the SST, the DC link voltage is controlled by each DAB cell and the current is controlled by the cascaded inverter cell in both directions of power flow. There are various methods to control the output voltage of the DAB which are proposed in the literature. The following subsections introduce such control strategies:

3.1.1. Single Phase Shift Control (SPS)

SPS is the most common control techniques used for DAB. In this control technique, the control parameter is just the phase shift angle. The duty cycle of the full bridges is maintained constant at 50% and the switching frequency is also a fixed value. The power flow in the circuit is governed by equation (3.1).

$$P = \frac{nV_{pri}V_{sec}\phi(1-\phi)}{2f_sL_s} \tag{3.1}$$

where ϕ is the phase shift and this is related to the phase shift angle as $\phi = \Phi/\pi$

For the convention, assume positive power flow indicates the power flow from primary to secondary and the negative power flow indicates the power from secondary to primary.

To find the phase shift at which maximum power transfer occurs, equation (3.1) has to be differentiated with respect to phase shift and equated to zero.

$$\frac{dP}{d\phi} = \frac{d}{dt}\left(\frac{nV_{pri}V_{sec}\phi(1-\phi)}{2f_sL_s}\right) = 0 \tag{3.2}$$

$$1 - 2\phi = 0 \quad \Rightarrow \quad \phi = 0.5 \tag{3.3}$$

ϕ varies between -0.5 to 0.5, where the negative value of phase shift represents negative power flow and vice versa. Substituting equation (3.3) in equation (3.1), one can arrive at the maximum transferred power equation which is given by equation (3.4).

$$P_{max} = \frac{nV_{pri}V_{sec}}{8f_sL_s} \tag{3.4}$$

The power being transferred is governed by controlling the phase shift angle. This phase shift is given by equation (3.5).

$$\phi = \frac{1}{2}\left(1 - \sqrt{1 - \frac{8f_sL_s|P|}{nV_{pri}V_{sec}}}\right) sgn(P) \tag{3.5}$$

Single phase shift is a simple and least complex control technique. However, compared to other control techniques, the ZVS range is limited and the transformer RMS currents are higher which leads to higher conduction losses and hence lower efficiencies.

3.1.2. Extended Phase Shift Control (EPS)

In EPS control strategy, unlike SPS, the leading full bridge need not operate at a fixed duty cycle of 0.5. Instead, it can operate with a duty cycle of less than 0.5 producing 3 voltage levels (+V, 0, -V).

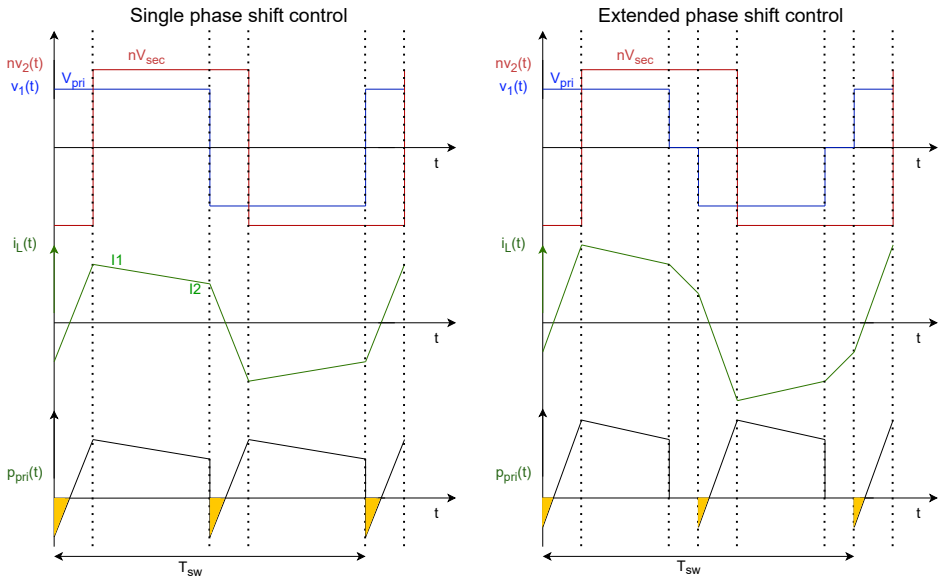


Figure 3.1: Comparison of SPS and EPS backflow power

Assuming primary voltage is a high voltage state, as shown in figure 3.1, compared to SPS, EPS has lower back flow power (shaded region). This is possible due to the introduction of an additional voltage state of the leading full bridge. As it can be observed, though there is an additional voltage state, the switching states per period are the same as the case of SPS, and there is no significant difference in switching losses. However, the conduction losses are lower in EPS due to a reduction in circulating power and hence circulating currents.

3.1.3. Triangular Current Mode Control (TCM)

Unlike the SPS or EPS, in TCM both the full bridges can be operated with a duty cycle of less than 0.5. The main advantages of this control technique are that the low voltage side full bridge can be switched at zero transformer current and the RMS currents of the transformer are reduced compared to SPS and EPS techniques, which improves the efficiency of the converter. Figure 3.2 shows the voltage and current waveforms of TCM control.

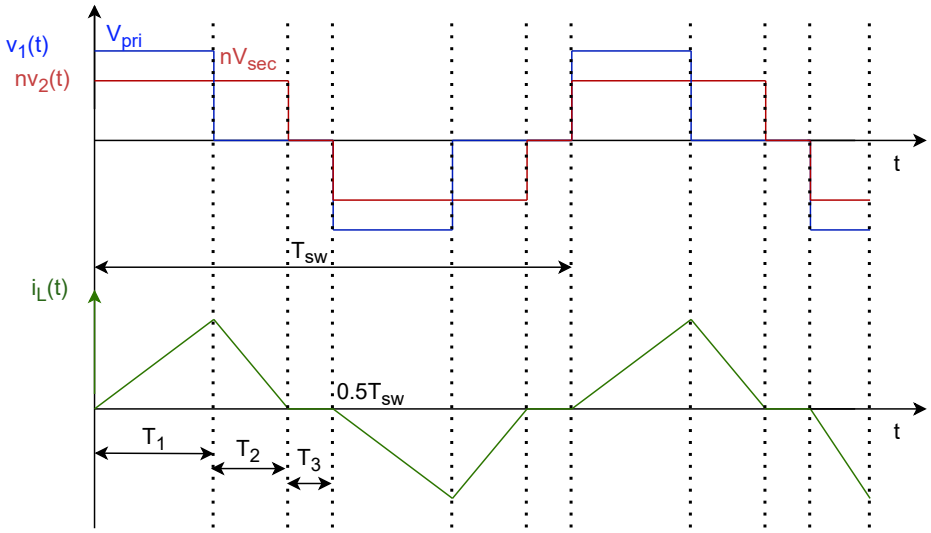


Figure 3.2: TCM waveforms

The time intervals T_1 and T_2 shown in the figure determine the amount of power transfer which is given in equation (3.6).

$$P = \frac{nV_{sec}}{T_{sw}L_s}\left[V_{pri}T_1(2T_2 - T_1) - nV_{sec}T_2^2\right] \tag{3.6}$$

Also, T_2 depends on T_1 so as to achieve $i_L(t_2) = 0$, as given in equation (3.7).

$$P = \frac{nV_{sec}}{T_{sw}L_s}\left[V_{pri}T_1(2T_2 - T_1) - nV_{sec}T_2^2\right] \tag{3.7}$$

$$\phi = T_2/T_{sw} \tag{3.8}$$

So combining equations (3.6), (3.7) and (3.8), one can conclude that the amount of power transfer only depends on the phase shift ϕ.

$$P = \frac{\phi^2 V_{pri}(nV_{sec})^2}{f_s L_s (V_{pri} - nV_{sec})} \quad \forall \quad V_{pri} > nV_{sec} \quad \wedge \quad 0 < \phi < \phi_{\Delta max} \tag{3.9}$$

$$\phi = \sqrt{f_s L_s P \frac{V_{pri} - nV_{sec}}{V_{pri}(nV_{sec})^2}} \quad \forall \quad V_{pri} > nV_{sec} \quad \wedge \quad 0 < \phi < \phi_{\Delta max} \tag{3.10}$$

$$T_1 = \frac{\phi}{f_s} \frac{nV_{sec}}{V_{pri} - nV_{sec}} \tag{3.11}$$

$$T_2 = \frac{\phi}{f_s} \tag{3.12}$$

From figure 3.2, the maximum power transfer in TCM control occurs when $T_3 = 0$. The maximum power transfer is given by equation (3.13).

$$P_{\Delta max} = \frac{n^2 V_{sec}^2 (V_{pri} - nV_{sec}}{4 f_s L_s V_{pri}} \tag{3.13}$$

$$\phi_{\Delta max} = \phi(P_{\Delta max}) = \frac{1}{2}\left(1 - \frac{nV_{sec}}{V_{pri}}\right) \tag{3.14}$$

It can be observed from equation (3.13) that the amount of power transferred when V_{pri} = nV_{sec} is zero. Thus this control strategy cannot be used for all power levels, especially when the voltages V_{pri} and nV_{sec} are close enough. As the turns ratio is limited by the condition of V_{pri} > nV_{sec}, the primary transformer currents (on the high voltage side) are high. Thus the conduction losses on the primary switches are higher.

3.1.4. Trapezoidal Current Mode Control (TzCM)

As seen in TCM, the control strategy becomes effective only for certain ranges of power levels (< $P_{\Delta max}$) and when V_{pri} = nV_{sec}, the power transfer is 0. Thus, in practice, TCM is used along with TzCM when the switching at zero inductor current is not mandatory on the secondary (low voltage) side. By implementing TzCM, power levels greater than $P_{\Delta max}$ can be achieved. Figure 3.3 shows the voltage and current waveforms of TzCM control technique. Since the inductor current goes to 0 after each T_{sw}/2 s, the transition between TCM and TzCM can be done seamlessly.

$$P = sgn(\phi) \frac{nV_{pri}V_{sec}[2nV_{pri}V_{sec}(1 - 2\phi^2) - (V_{pri}^2 + (nV_{sec}^2))(1 - 2|\phi|)^2]}{4 f_s L_s (V_{pri} + nV_{sec})^2} \quad \forall \phi_{\Delta max} < |\phi| < \phi_{\square max} \tag{3.15}$$

where,

$$\phi_{\square max} = \frac{1}{2}\left(1 - \frac{nV_{pri}V_{sec}}{V_{pri}^2 + nV_{pri}V_{sec} + V_{sec}^2}\right) \tag{3.16}$$

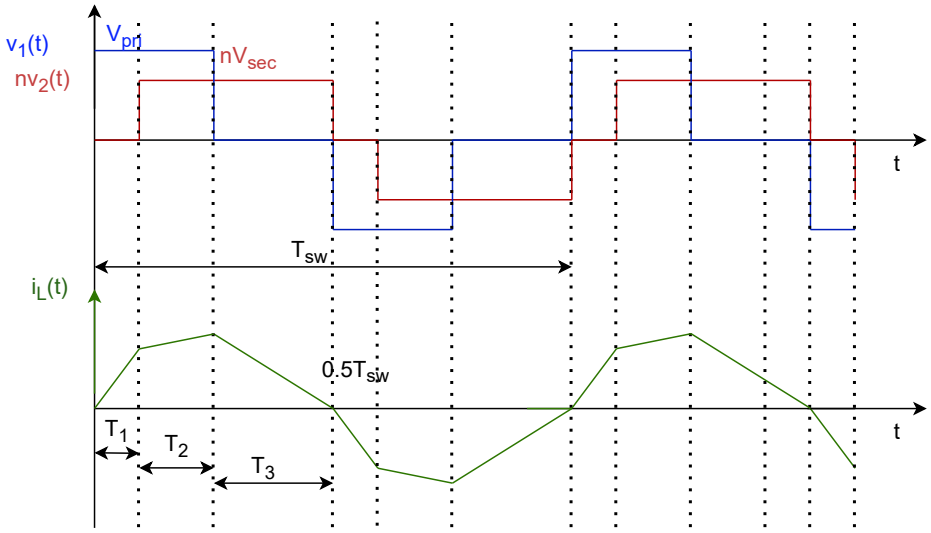


Figure 3.3: TzCM waveforms

The solutions for the required phase shift, T_1, T_2 and T_3 are given by:

$$\phi = \frac{1}{2}\frac{sgn(P)}{V_{pri}^2 + nV_{pri}V_{sec} + V_{sec}^2}\left\{V_{pri}^2 + (nV_{sec})^2 - (V_{pri} + nV_{sec})* \sqrt{nV_{pri}V_{sec}\left(1 - \frac{4f_sL_s|P|(V_{pri}^2 + nV_{pri}V_{sec} + V_{sec}^2)}{(nV_{pri}V_{sec})^2}\right)}\right\} \tag{3.17}$$

$$T_1 = \frac{nV_{sec} - V_{pri} + 2V_{pri}\phi}{2f_s(V_{pri} + nV_{sec})} \tag{3.18}$$

$$T_2 = \frac{1 - 2\phi}{2f_s} \tag{3.19}$$

$$T_3 = \frac{V_{pri} - nV_{sec} + 2nV_{sec}\phi}{2f_s(V_{pri} + nV_{sec})} \tag{3.20}$$

The maximum power that can be transferred is given by equation (3.21).

$$P_{\square max} = \frac{(nV_{pri}V_{sec})^2}{4f_sL_s(V_{pri}^2 + nV_{pri}V_{sec} + V_{sec}^2)} \tag{3.21}$$

Conclusion

Upon considering all 4 control techniques, the ones with higher control variables provide better performance with respect to reduced RMS currents, better efficiencies and/or increased ZVS region. However, this comes with added complexity. For the SST application, SPS seems to be an effective and simpler control strategy. This is because, when SPS is implemented, the primary full bridge can be constantly operated with a fixed duty cycle and all the control

can operate on the secondary side. Thus reducing the need for data transmission from the secondary side to the primary side. Keeping the need for isolation in mind, it is very important to limit the amount of data transfer needed. Hence, for this application, SPS is chosen as the least complex and most effective control technique. The same is implemented as described in section 3.3.

3.2. ZVS Range

Switching losses play a dominant role in high-frequency converters. These losses arise due to the area under the overlap of voltage across the switch (V_{DS}) and the current flowing through the switch (I_D). During turn-on, if V_{DS} falls to zero even before I_D start to rise, then the losses will be zero. This process of eliminating turn-on losses is called ZVS.

One of the key merits of the DAB converter is the high efficiency at nominal ratings due to ZVS operation. However, it is important to note that the ZVS operation is not available over a wide range of loads. When the converter operates in the non-ZVS region, not only the efficiency decreases (due to an increase in switching losses), but also there will be EMI issues in certain conditions. Hence, it is important to identify and try to operate the converter in ZVS region.

For the converter to operate in the ZVS region, a few conditions have to be met. These are discussed in the following sub-sections.

3.2.1. Necessary Conditions for ZVS

To analyze the necessary condition for ZVS, the current through the inductor has to be studied. In the current waveforms of the inductor, two points become very critical. These are the current value flowing through the inductor when the two full bridge networks are switching. Considering a simple model of DAB as shown in figure 3.4, the critical current points are shown as I_1 and I_2 in figure 3.5.

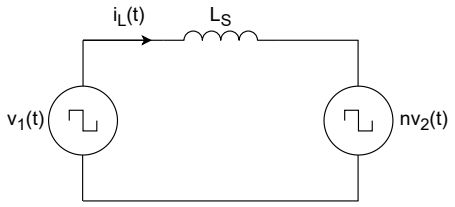


Figure 3.4: Simple representation of DAB circuit

To achieve soft-switching, both I_1 and I_2 have to be positive, respectively. When I_1 and I_2 are positive, the current flows through the body diode of the MOSFET that needs to be turned ON. Thus, when the current flows through the body diode, a zero voltage turn-on will be possible.

From the basic equation of voltage across the inductor,

$$\frac{dI_L(\omega t)}{dt} = \frac{V_{pri} - nV_{sec}}{L_s} \tag{3.22}$$

Considering equation (3.22), and the leakage inductance current in figure 3.4, the following

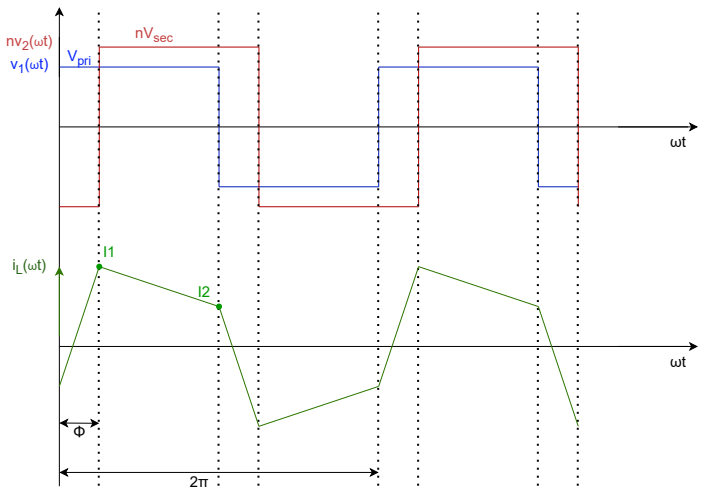


Figure 3.5: Ideal waveform of current flowing through the inductor

equations can be derived considering semi-period operation:

$$V_{pri} + nV_{sec} = L_s \frac{I_1 + I_2}{(\Phi/\pi)T_{sw}/2}, \quad for\ 0 < \omega t < \Phi \tag{3.23}$$

$$V_{pri} - nV_{sec} = L_s \frac{I_1 - I_2}{((1-\Phi)/\pi)T_{sw}/2}, \quad for\ \Phi < \omega t < \pi \tag{3.24}$$

Solving equation (3.23) and equation (3.24),

$$I_1 = \frac{T_{sw}}{4L_s}\left(2\frac{nV_{sec}\Phi}{\pi} + V_{pri} - nV_{sec}\right) \tag{3.25}$$

$$I_2 = \frac{T_{sw}}{4L_s}\left(2\frac{V_{pri}\Phi}{\pi} - V_{pri} + nV_{sec}\right) \tag{3.26}$$

Defining modulation index (M) as,

$$M = \frac{nV_{sec}}{V_{pri}} \tag{3.27}$$

final equations for I_1 and I_2 are given as,

$$I_1 = \frac{T_{sw}V_{pri}}{4L_s}\left(2M\frac{\Phi}{\pi} + 1 - M\right) \tag{3.28}$$

$$I_2 = \frac{T_{sw}V_{pri}}{4L_s}\left(2\frac{\Phi}{\pi} - 1 + M\right) \tag{3.29}$$

From equation (3.28) and equation (3.29), following observations can be made:

- When M = 1, irrespective of the phase shift angle, I_1 and I_2 are equal and positive. Hence the necessary condition for ZVS for all the switches is met.
- When M>1, I_2 is greater than 1 for all the values of Φ. So, the ZVS condition for the lagging full bridge is met for all values of Φ. However, to achieve ZVS in the leading full bridge, the following condition must be met:

$$\Phi > \frac{M-1}{2M}\pi \tag{3.30}$$

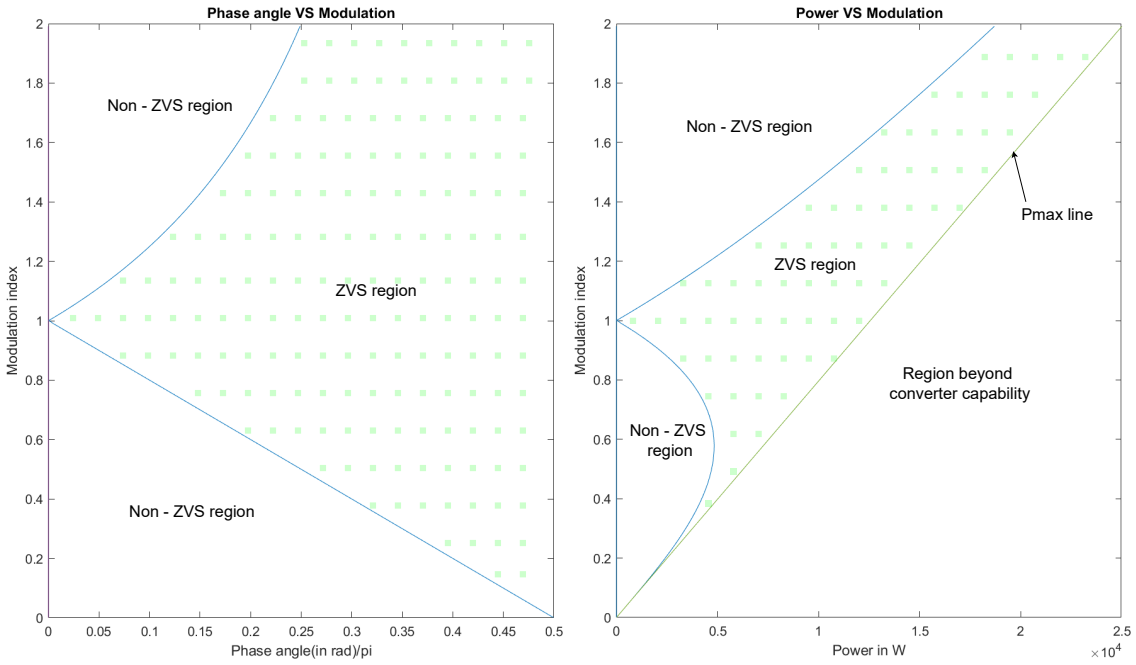
- When M<1, I_1 is greater than 1 for all the values of Φ. So, the ZVS condition for the leading full bridge is met for all values of Φ. However, to achieve ZVS in the lagging full bridge, the following condition must be met:

$$\Phi > \frac{1-M}{2}\pi \tag{3.31}$$

Using the above equations, the graph can be plotted between the phase angle and the modulation index to identify the ZVS and non-ZVS regions. This is shown in figure 3.6 (a).

Also, assuming a constant input voltage (V_{pri}), the power Vs modulation index can be obtained by substituting equation (3.27) in the basic DAB equation to obtain equation (3.32) and using the values of phase shift corresponding to specific modulation index obtained from figure 3.6 (a). This graph is shown in figure 3.6 (b) considering V_{pri} = 1500 V, f_s = 160 kHz and L_k = 140 μ H.

$$P = \frac{MV_{pri}^2\phi(1-\phi)}{2f_sL_s} \tag{3.32}$$



((a)) ZVS region in phase shift vs modulation index

((b)) ZVS region in power vs modulation index

Figure 3.6: Plots that portray ZVS region for DAB operating in SPS

Effect of magnetizing inductance on the ZVS region

From figure 3.4, it can be seen that the magnetizing inductance of the transformer is ignored. However, adding the magnetizing inductance would change the inductor current waveforms, thereby altering the primary and secondary currents and the power transfer capability as shown in figure 3.7. The effect of magnetizing inductance is studied by Shiyuan Yin et al. in [22].

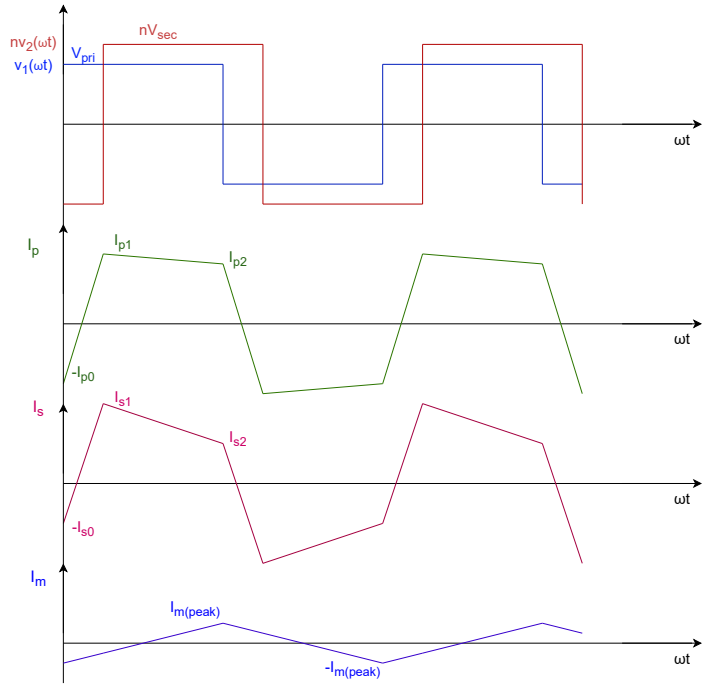


Figure 3.7: Waveforms showing the effect of magnetizing current on primary and secondary currents

Considering magnetizing inductance, equation (3.30), (3.31) and (3.32) can be re-written as equation (3.33), (3.34) and (3.35) respectively.

$$\Phi > \frac{K_2 M - K_1}{2K_2 M}\pi \tag{3.33}$$

$$\Phi > \frac{K_2 - K_1 M}{2K_2}\pi \tag{3.34}$$

$$P = K_2 \frac{M V_{pri}^2 \phi(1-\phi)}{2 f_s L_s} \tag{3.35}$$

where K_1 and K_2 are constants which depend on magnetizing and leakage inductance and are given by equation (3.36) and equation (3.37).

$$K_1 = \frac{4L_m + 2L_{lk}}{4L_m + L_{lk}} \tag{3.36}$$

$$K_2 = \frac{4L_m}{4L_m + L_{lk}} \tag{3.37}$$

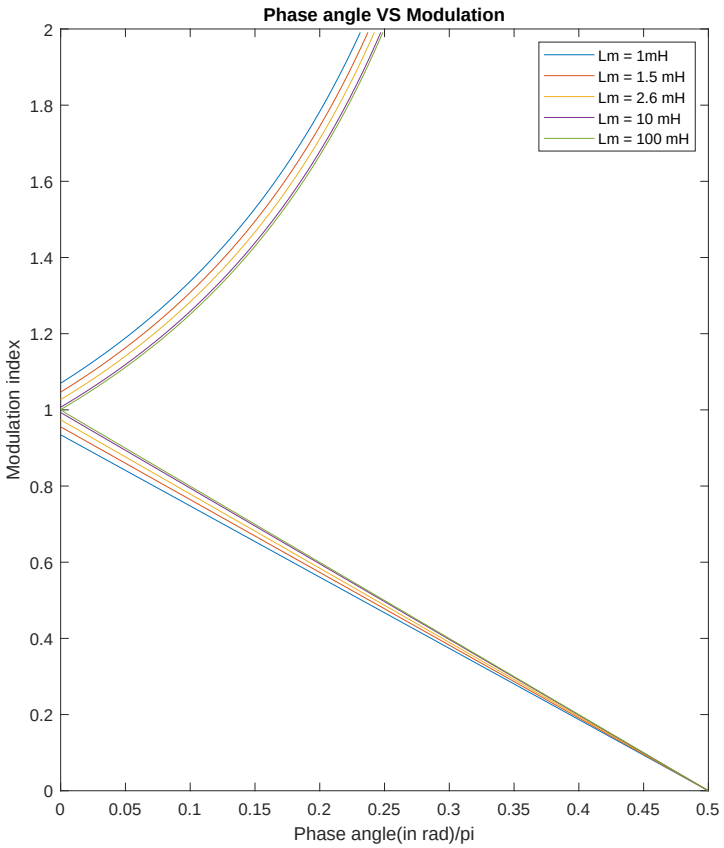


Figure 3.8: Effect of magnetizing inductance

From figure 3.8, it can be seen that upon increasing L_m the ZVS region narrows down. This is because increasing L_m decreases the magnetizing currents and hence there is less current during dead time to discharge C_{OSS}. However, by increasing the L_m, the power transfer capability can be increased and the magnetizing currents can be decreased hence the primary side switches will have lower losses.

3.2.2. Sufficient Condition for ZVS

As discussed, the conditions mentioned in the previous section are necessary for the ZVS operation. However, they are not sufficient conditions. To achieve ZVS, the currents I_1 and I_2 should not only be greater than zero but also should be greater than a certain threshold. The ZVS can be achieved only when the energy stored in the series inductor (E_{L_s}) is higher than the energy stored in the output parasitic capacitor of the switches in the full bridge ($E_{C_{OSS}}$) [23].

$$E_{L_s} > E_{C_{OSS}} \rightarrow \frac{1}{2} L_s i_{L_{s_{FB}}}^2 > 4\frac{1}{2} C_{eq} V_{FB}^2 \rightarrow i_{L_{s_{FB}}} > 2V_{FB}\sqrt{\frac{C_{eq}}{L_s}} \tag{3.38}$$

Considering equations (3.28), (3.29) and (3.38), the sufficient conditions for ZVS can be obtained as follows:

$$I_1 = \frac{T_{sw}V_{pri}}{4L_s}\left(2M\frac{\Phi}{\pi} + 1 - M\right) > 2V_{pri}\sqrt{\frac{C_{eq\_lead}}{L_s}} \tag{3.39}$$

$$I_2 = \frac{T_{sw}V_{pri}}{4L_s}\left(2\frac{\Phi}{\pi} - 1 + M\right) > 2V_{sec}\sqrt{\frac{C_{eq\_lag}}{L_s}} \tag{3.40}$$

Solving equations (3.39) and (3.40), the final conditions are obtained.

$$\Phi > \frac{M-1}{2M}\pi + \frac{4\sqrt{L_sC_{eq\_lead}}}{T_{sw}M}\pi \tag{3.41}$$

$$\Phi > \frac{1-M}{2}\pi + \frac{4M\sqrt{L_sC_{eq\_lag}}}{nT_{sw}}\pi \tag{3.42}$$

Similar to the necessary condition analysis, this does not account for the magnetizing inductance. When the magnetizing inductance is considered, the currents I_1 and I_2 are different on both the full bridges. For the leading full bridge they are given by equations (3.43) and (3.44) and for the lagging full bridge they are given by equations (3.45) and (3.46), respectively.

$$I_{p1} = \frac{T_{sw}V_{pri}K_2}{4L_s}\left(2M\frac{\Phi}{\pi} + \frac{K_1}{K2} - M\right) \tag{3.43}$$

$$I_{p2} = \frac{T_{sw}V_{pri}K_2}{4L_s}\left(2\frac{\Phi}{\pi}\frac{K_1}{K2} - \frac{K_1}{K_2} + M\right) \tag{3.44}$$

$$I_{s1} = \frac{T_{sw}V_{pri}K_1}{4L_s}\left(2M\frac{\Phi}{\pi} + \frac{K_2}{K1} - M\right) \tag{3.45}$$

$$I_{s2} = \frac{T_{sw}V_{pri}K_1}{4L_s}\left(2\frac{\Phi}{\pi}\frac{K_2}{K1} - \frac{K_2}{K_1} + M\right) \tag{3.46}$$

To meet the conditions for leading full bridge, equations (3.43) and (3.38) have to be considered. Whereas, to meet the conditions for a lagging full bridge, equations (3.46) and (3.38) have to be considered.

$$I_{p1} = \frac{T_{sw}V_{pri}K_2}{4L_s}\left(2M\frac{\Phi}{\pi} + \frac{K_1}{K2} - M\right) > 2V_{pri}\sqrt{\frac{C_{eq\_lead}}{L_s}} \tag{3.47}$$

$$I_{s2} = \frac{T_{sw}V_{pri}K_1}{4L_s}\left(2\frac{\Phi}{\pi}\frac{K_2}{K1} - \frac{K_2}{K_1} + M\right) > 2V_{sec}\sqrt{\frac{C_{eq\_lag}}{L_s}} \tag{3.48}$$

Hence, when the magnetizing inductance is considered, the sufficient conditions for ZVS operation are given by equations (3.49) and (3.50).

$$\Phi > \frac{M - \frac{K_1}{K_2}}{2M}\pi + \frac{4\sqrt{L_s C_{eq\_lead}}}{T_{sw} M K_2}\pi \tag{3.49}$$

$$\Phi > \frac{1 - M\frac{K_1}{K_2}}{2}\pi + \frac{4M\sqrt{L_s C_{eq\_lag}}}{nT_{sw} K_2}\pi \tag{3.50}$$

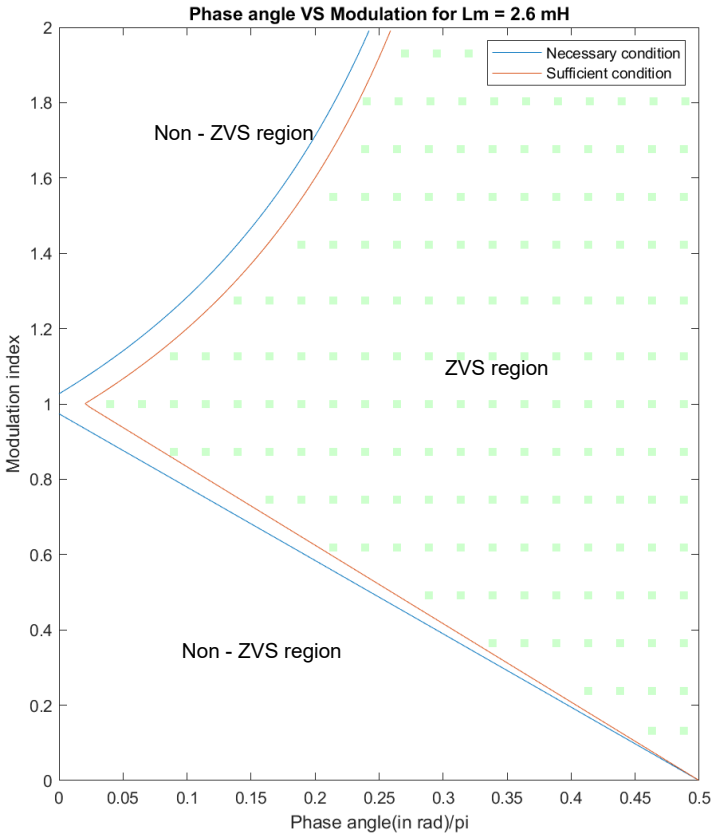


Figure 3.9: Final ZVS region considering magnetizing inductance of 2.6 mH

The ZVS operating region is shown in figure 3.9. The area marked in green represents the ZVS region and the area between the curves represents the region where the necessary condition for ZVS is met but not the sufficient condition. Even at a modulation index of 1, there has to be a certain minimum phase angle difference between the full bridges i.e. there has to be a certain minimum power flow in order to achieve ZVS.

3.3. Implemented Control Strategy

Since the SPS control is chosen as the ideal control strategy for this application, the same is implemented in PLECS. Since the two full bridges have to be isolated with MV isolation, there is no direct communication between the two full bridges. The primary full bridge constantly switches with a 0.5-duty cycle. While the secondary full bridge receives the LV-DC voltage value from the system controller. The system controller communicates with the primary side through a 20 kV optoisolator and it communicates with each level of the secondary side with a 2 kV isolator network. Hence the SPS control is implemented as shown in figure 3.10

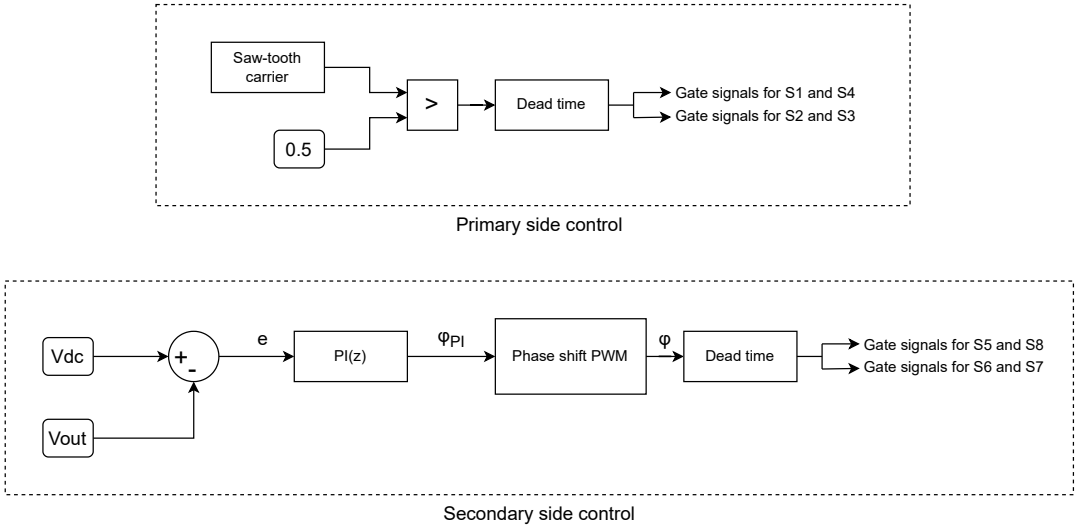


Figure 3.10: Implemented PI control

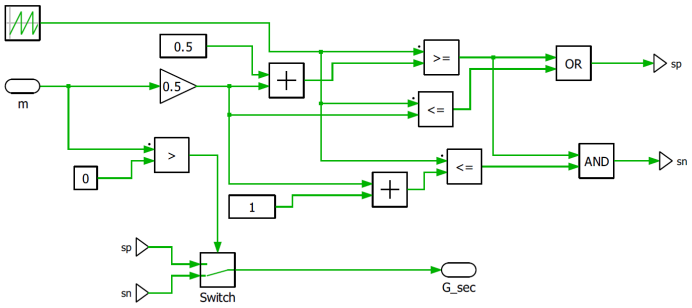


Figure 3.11: Phase shift PWM implementation in PLECS

3.3.1. Feed-forward Control

The PI control implemented is effective for small changes in the voltage. When there is a sudden drop or rise in voltage, to quickly adapt the output voltage to the reference value, a higher/lower phase shift compared to the one generated by the PI controller is needed. In order to achieve this quick response during a sudden drop or rise in grid voltage, feed-forward control is implemented. The feed-forward phase shift is given by the phase shift given in equation (3.5). the modified control is shown in figure 3.12

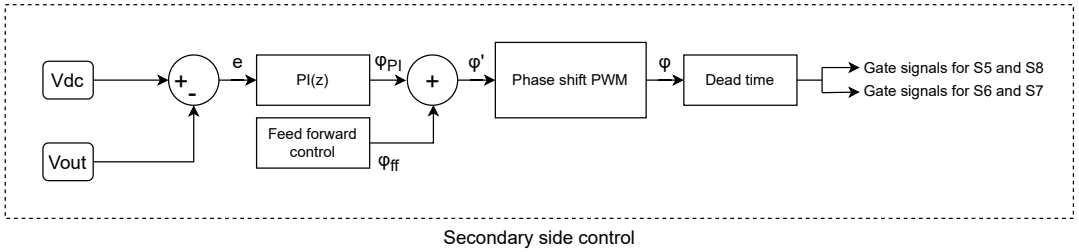
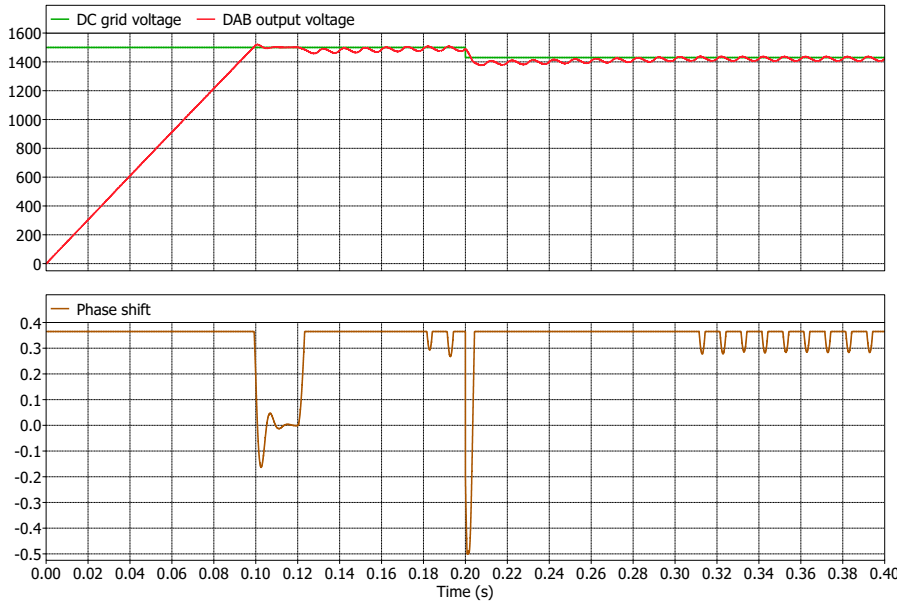
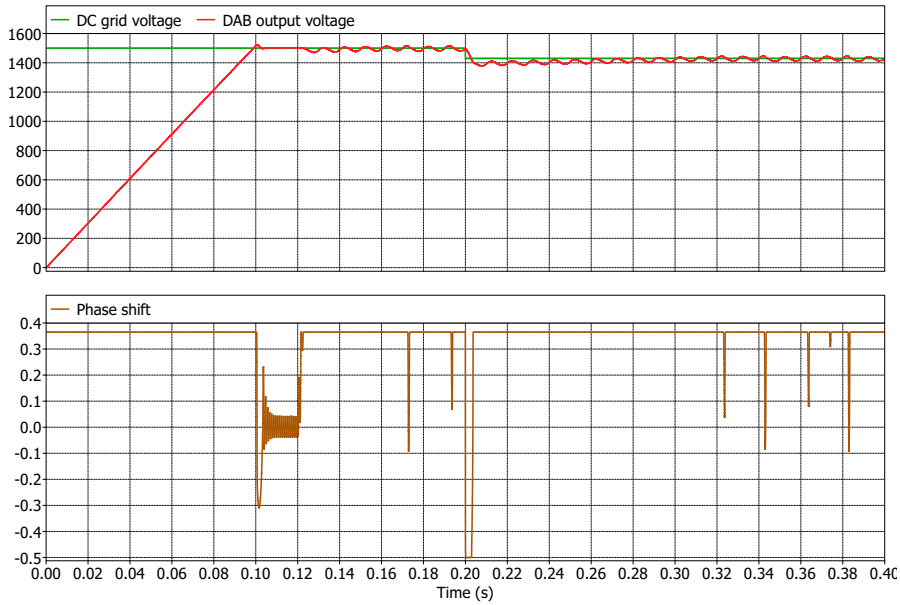


Figure 3.12: Modification of secondary control design to incorporate feed-forward control

The effect of feed-forward control is seen in figure 3.13. Feed-forward control decreases the



((a)) Without feed-forward control



((b)) With feed-forward control

Figure 3.13: PLECS simulation results to show the effect of feed-forward control

time taken for the converter to reach the reference voltage. Thus making the system respond faster. But this happens with the cost of transferring high values of negative power for that instant. Even when there are slight changes in reference voltage, the system responds by setting an extreme value of phase shift. Thus to make a call on the impact of feed-forward control, the system priorities have to be set. In this scenario, being able to maintain desired voltage at the output is important to stay in the ZVS range. Hence, the feed-forward control needs to be

incorporated.

3.3.2. Droop Control Limits

In order to control the direction of the flow of power, whether from the DC grid to the AC grid or from the AC grid to the DC grid is decided based on the AC grid and DC grid voltages. The representation of direction and amount of power flow based on grid voltages is called droop characteristics. The proposed droop characteristic curve is given in figure 3.14.

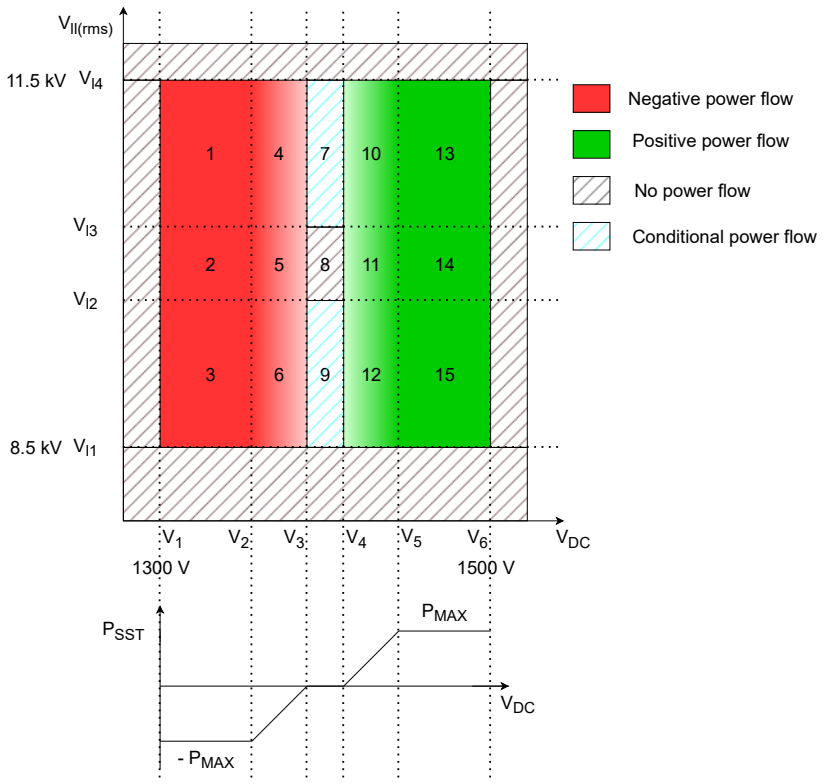


Figure 3.14: Droop characteristics

As seen in figure 3.14, the droop region is split into 15 regions and the outermost shaded region. The outermost shaded region represents the undervoltage and overvoltage regions of the DC and AC grids (assuming +-15% variation on AC grid). In regions 1, 2 and 3, the maximum possible power is transferred from the AC grid to the DC grid (represented as negative power). Though in region 3, the AC grid is at low voltage, it is assumed to be a much stronger grid and hence maximum power can still be transferred. In regions 4, 5 and 6, the power transferred from the AC grid decreases as the DC grid voltage approaches voltage V_3. Similarly, in regions 10, 11 and 12, the DC grid has slightly high voltage indicating excess generation than consumption. Hence the power is transferred to the AC grid and the amount of power transfer increases as the DC grid voltage increases. In regions 13, 14, and 15, the DC grid has high voltage and hence can facilitate the maximum possible power transfer to the AC grid. In regions 7 and 9, a certain minimum amount of power (enough to achieve ZVS) can be provided from the DC grid to the AC grid and from the AC grid to the DC grid periodically untill the voltages fall in other regions.

The maximum power that can be transferred from DC to AC or AC to DC side can be determined based on the voltage levels as given in equation (3.51). The derivation of this equation is given in appendix B.

$$P_{SST} < \frac{\pi\sqrt{3}V_{ll(rms)}nV_{pri}}{16\sqrt{2}f_sL_s} \tag{3.51}$$

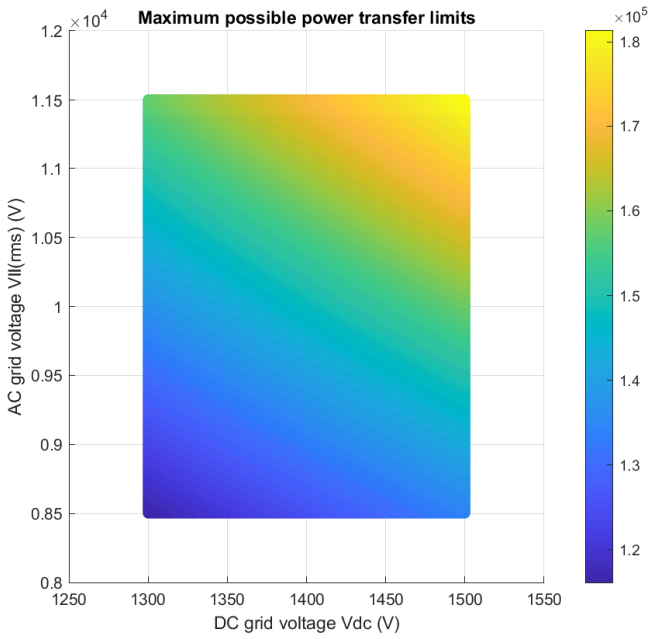


Figure 3.15: Maximum possible power transfer of the SST for various DC and AC grid voltages

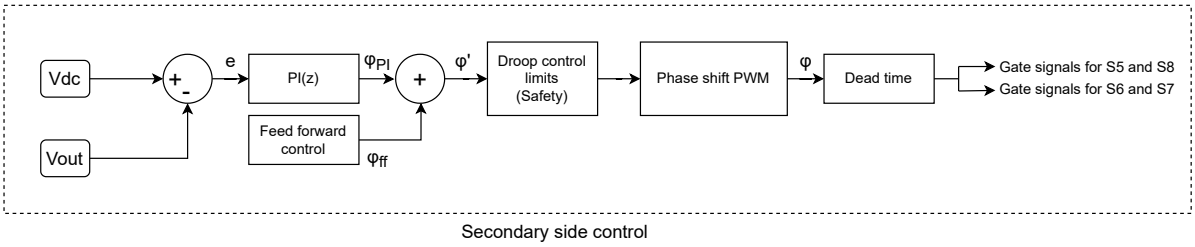


Figure 3.16: Modification of secondary control design to incorporate safety droop limits

3.4. System Level Control of SST

As shown in figure 2.20, every DAB cell is connected to an H-bridge inverter network. In order to facilitate power transfer, voltage and currents have to be controlled. Current control and grid connection is taken care of in the inverter stage. Also, since the inverter is connected in series at the MV side, to facilitate equal power distribution in all cells, a phase-shifted sinusoidal PWM strategy is implemented. The voltage control is implemented in each DAB cell.

During power flow from LV-DC to MV-AC, when the current is drawn from the inverter network, the DC link capacitor discharges and hence the voltage on the secondary terminal of the

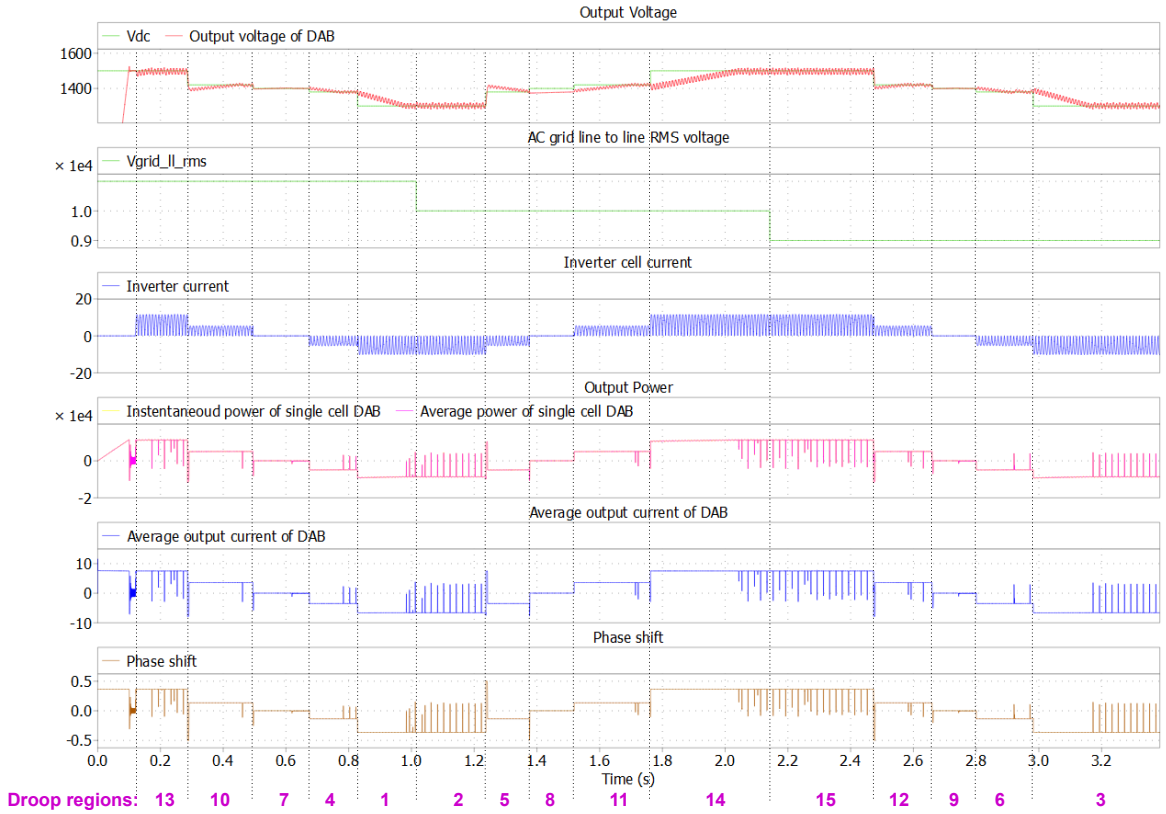


Figure 3.17: PLECS control results of operation of single cell DAB in various droop regions

DAB drops. With the help of PI, control of DAB increases the phase shift and hence increases the voltage on the DC-link capacitors. Thus the DAB maintains the DC link capacitor voltage within a certain threshold. In this project, DAB shall maintain the same voltage at the primary and secondary. Hence, the cascaded inverter stage operates at the desired modulation index to match the grid voltage.

Figure 3.19 shows the PLECS results of the complete SST model in both directions of power flow. Initially, till 0.095 seconds the DC-link capacitors are charged to a voltage equal to the DC grid voltage. From 0.12 seconds, the active power transfer is established by the inverter. Depending on the droop data, the direction and amount of power flow are decided.

3.5. Summary

In this chapter, various control techniques have been discussed and the conclusion has been made to go ahead and implement SPS control due to its simple control approach. The phase shift control is done on the secondary side and the primary switches operate with a fixed duty cycle. Hence the only signal that needs to be transferred from the system controller to the primary side controller in case of SPS is the enable/disable function key (which needs to be synchronized). Further in this chapter, the conditions to achieve ZVS are discussed in which the effect of magnetizing inductance has also been considered.

Next, feedforward control and droop control limits have been discussed. To the main PI con-

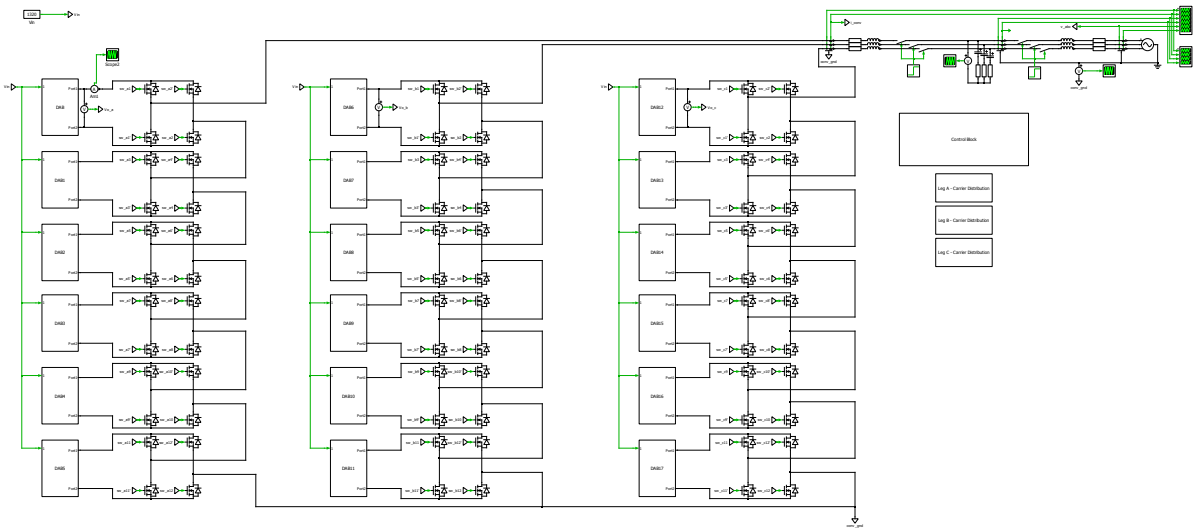


Figure 3.18: PLECS model of complete SST

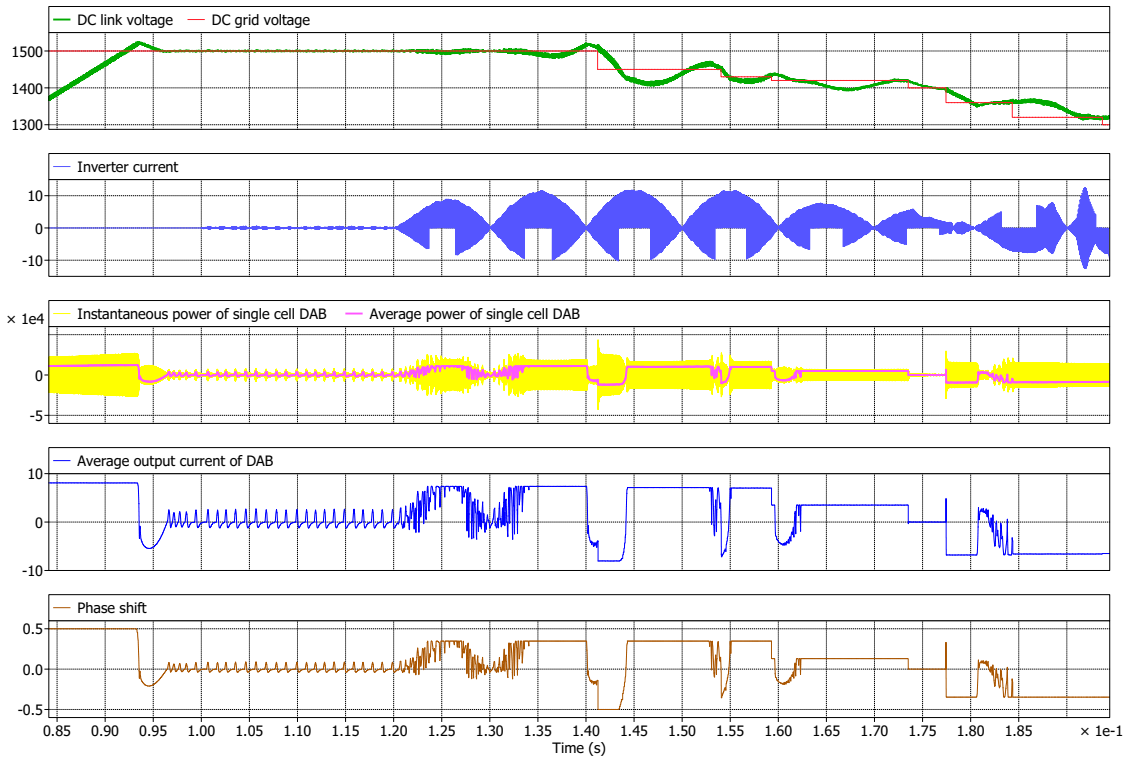


Figure 3.19: PLECS control results of operation of complete system level SST

trol, feedforward and droop control limits have been added to make the system fast and safe, respectively. The SPS control was implemented in PLECS along with feed-forward control and droop limits. The simulation results of the same are also shown in this chapter. Finally, the chapter concludes by briefing the system-level control and its PLECS results.

4

DAB Design and Parameter Selection

4.1. DAB with PT Script

The design of a DAB converter involves the selection of various parameters that are interdependent on each other. Due to this reason, the design procedure is an iterative process. To enable a quick design procedure, a script is implemented in MATLAB to design DAB parameters considering various optimization limits in order to achieve certain objectives. In this section, the script objectives, optimization limits, calculations of DAB parameters and script results are explained.

4.1.1. Script Objectives

To design a DAB, optimal values of various factors need to be selected, and those values depend on several other factors. Hence, a script was developed as a part of the project to identify the following main parameters/components:

- Optimal frequency of operation.
- Optimal number of turns of the transformer.
- Airgap of the transformer.
- Core dimensions and material

Apart from these, other essential parameters are also calculated in the script. Figure 4.1 shows a functional architecture diagram of the script where all the inputs and outputs of the script are mentioned.

The script is run for a sweep of operating frequencies ranging up to 500 kHz and the number of turns of the transformer ranging up to 23 turns. These constraints on the frequency and the number of turns are set based on the limits of SiC MOSFET switching capabilities and manufacturing feasibility of high-layered PCB with buried vias and thick copper layers, respectively. The final choice of parameters is done in order to have low manufacturing costs and high efficiency.

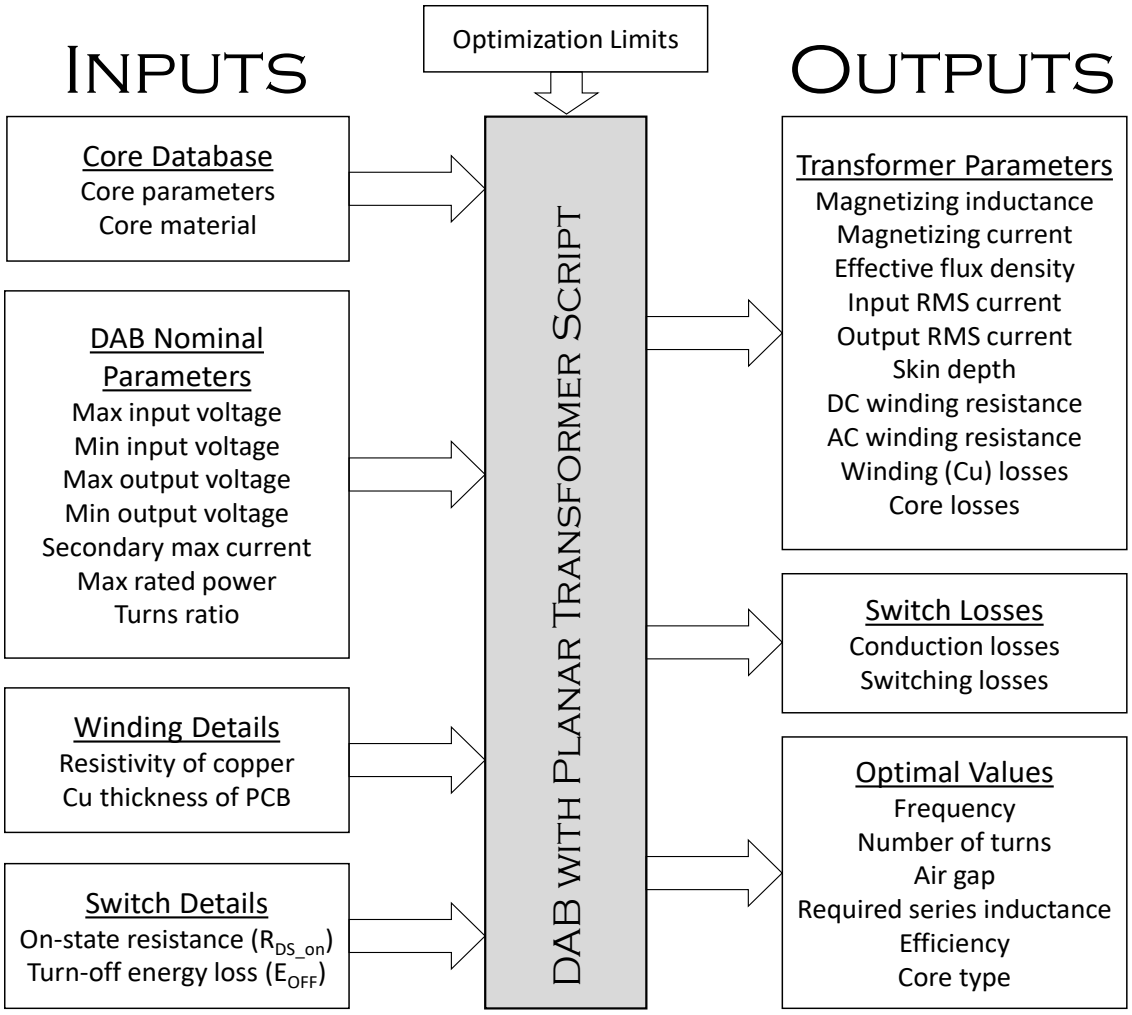


Figure 4.1: DAB with planar transformer I/O diagram

4.1.2. Script Constraints

The following are the constraints that help us narrow down the wide range of possible parameters to optimal values:

- Maximum per switch loss limits
- Core loss limits
- Effective core utilization and core saturation limits
- Switch current limits
- Transformer winding current limits

Once the above limits are implemented, and the range of the number of turns and switching frequencies are narrowed down, the final values of the parameters are chosen to obtain high efficiency with fewer turns as the increase of the number of turns would increase the number of PCB layers thereby increasing the cost and the space needed in the window area of the core.

Estimation of Maximum Permissible Per Switch Losses

Higher power being transferred by DAB would mean higher losses in the switches and hence higher heat generated that needs to be dissipated. There is a limit on the amount of heat that can be dissipated through the PCB and heatsink, thus making it one of the constraints to achieve a higher power rating. Since SMD switches are used, in the case of FR4-based PCB, copper-filled vias are provided on the drain pad area to effectively dissipate the heat through PCB. To achieve this, various via arrangements shown in figure 4.2 are considered. As an alternative, aluminum-based PCBs are usually employed for more effective heat dissipation and, thus, better thermal performance. However, this comes with a downside. Using single-layer aluminium increases the PCB layout complexity and also increases the return path loop that's usually very small when properly routed on the multi-layer PCB. This increases the loop inductance and hence causes EMI issues.

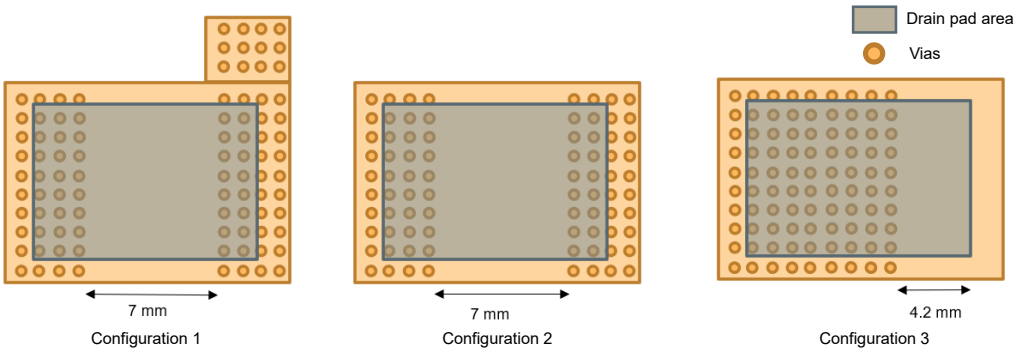


Figure 4.2: Various possible via arrangements for heat dissipation in 4 layers 0.8 mm thick PCB

Various COMSOL simulations are carried out in order to determine the thermal resistance of the case to sink ($R_{th(cs)}$) for both FR4-based PCB and Aluminium substrate PCB cases. The results of these COMSOL simulations are shown in table 4.1:

Table 4.1: $R_{th(cs)}$ values for various PCB configurations

	$R_{th(cs)}$ (K/W)
Configuration 1	2.29
Configuration 2	2.4418
Configuration 3	2.2539
Single layer Al PCB (without vias)	1.22
2 layer Al PCB (without vias)	7.61

Single-layer aluminium-based PCB is selected for this application because there is a significant difference in $R_{th(cs)}$ when FR4 and aluminium-based PCB are compared.

In this project, it is decided to have separate heatsinks for the primary and secondary full bridges. On the primary heatsink, planar transformer and planar inductor are also mounted along with the primary full bridge. On the secondary heatsink, the secondary side full bridge and the inverter cell are mounted. The steady-state model for the thermal behaviour of the primary heatsink, shown in figure 4.3, is built based on the following assumptions:

- Each full bridge of the DAB is on separate heatsinks.

- Inductor and transformer losses are ignored (This assumption holds good as this is the maximum limit. However, in the next section, the core losses of the inductor and transformer are accounted for).
- All the switches in the full bridge have the same amount of losses.
- There is uniform heat spreading over the heatsink due to losses in all switches.
- The ambient temperature is 50 ^{O}C and the maximum junction temperature of switches is 120 ^{O}C.

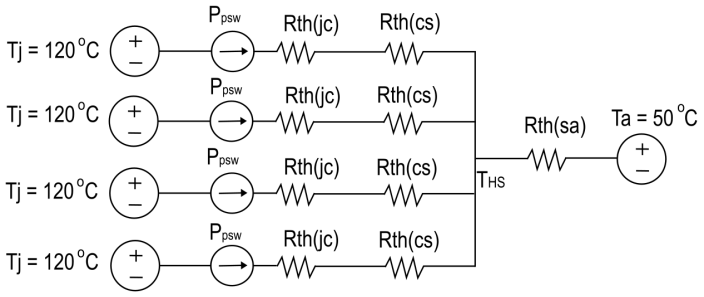


Figure 4.3: Steady-state model for thermal analysis

$$P_{psw} * (R_{th_{JC}} + R_{th_{CS}}) + 4 * P_{psw} * R_{th_{SA}} = T_j - T_a \tag{4.1}$$

where, P_{psw} is the maximum loss in a switch, $R_{th_{JC}}$ is the junction to case thermal resistance which is equal to 1.1 ^{O}C/W [24], $R_{th_{CS}}$ is the case to sink thermal resistance which is equal to 1.22 ^{O}C/W (from table 4.1) and $R_{th_{SA}}$ is the sink to ambient thermal resistance which is equal to 0.08 ^{O}C/W [25].

$$P_{psw} * (1.1 + 1.22) + 4 * P_{psw} * 0.08 = 70 \tag{4.2}$$

Solving equation (4.2) gives P = 26.5 W. Hence, the maximum limit of per switch loss is 26.5 W and hence this becomes the constraint.

Estimation of Maximum Permissible core Losses of PT

During the estimation of the maximum permissible per switch loss, the core loss is ignored. However, since we use a planar transformer and a planar inductor, these losses have to be modelled in the steady state thermal model shown in figure 4.3.

The adapted steady-state thermal model is shown in figure 4.4. This model is made with the following assumptions:

- The convective heat transfer is ignored and all the core losses of the transformer are concentrated and can be dissipated by its bottom surface.
- PI has the same core losses as that of PT. This is a fair assumption because the core losses depend on operating flux density and frequency. The PI would be designed for a similar operating flux density as the core material would be the same.

- Unlike small SMD switches, since there is a large surface area of contact in the case of PT and PI, the heatsink and the core can be assumed to be at the same temperature.
- All the switches in the full bridge have the same amount of losses.
- There is uniform heat spreading over the heatsink due to losses in all switches, PT and PI.
- The ambient temperature is 50 ^{O}C and the maximum temperature of the core is 100^{O}C.

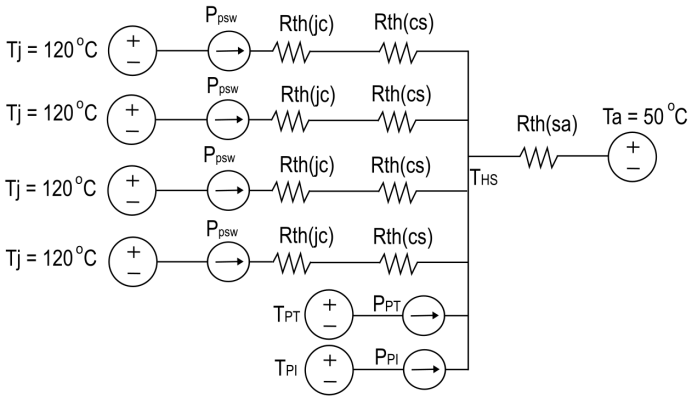


Figure 4.4: Steady-state model for thermal analysis including PT and PI core losses

The maximum limit of the PT core loss for a given heatsink depends on the per switch loss and the PI core loss.

$$P_{psw} * (R_{th_{JC}} + R_{th_{CS}}) + (4P_{psw} + P_{PT} + P_{PI}) * R_{th_{SA}} = T_j - T_a \tag{4.3}$$

Since core losses of PI and PT are assumed to be same,

$$P_{PT} = \frac{70 - 2.32 * P_{psw} - 4P_{psw}R_{th_{SA}}}{2R_{th_{SA}}} \tag{4.4}$$

If the per switch loss is lower than a certain value and the switch is at a junction temperature of 120^{O}C, then the maximum PT core loss is restricted due to maximum core temperature.

$$P_{PT} = \frac{\frac{50}{R_{th_{SA}}} - 4P_{psw}}{2} \tag{4.5}$$

Equations (4.4) and (4.5) represent the maximum limits of core loss. The lower of the two values gives the maximum of the core loss that can be dissipated.

Effective Core Utilization and Core Saturation limits

Since the converter is planned to operate at high frequencies (>100 kHz), ferrite cores are employed as they have low eddy current losses over several frequencies and high relative permeability. Typically these cores have a saturating flux density of 300-350 mT. However, for frequencies over 100 kHz, there would be high core losses when the flux density reaches

over 200 mT as given in the datasheet [26]. Hence, to operate in a safe zone, the maximum limit of saturation flux density is set as 200 mT. Also, the core needs to be effectively utilized. Hence, the minimum value of saturation flux density is another limiting condition that has to be met. For this application, the minimum flux density is chosen as 120 mT. Hence, 120 mT $< B_{eff} <$ 200 mT is considered as the next constraint in the parameter selection.

Switch current limits

As the switches for the converter are fixed, their continuous current carrying limits act as one of the constraints for choosing optimal values of power limits, operating frequency and the number of turns of the transformer. From the switch datasheet [24], assuming the case steady-state temperature of 100^{o}C, the maximum limit of switch current is chosen as 13 A.

Transformer winding currents

The planar cores come in some standard dimensions. There is a possibility to manufacture the cores in any dimension as the manufacturing process of ferrite cores is flexible. However, as this is a prototype, and having a custom core designed is not very economical for fewer quantities, standard cores are taken into account. Standard cores have fixed standard window width, and hence a fixed width of track can be incorporated into the window. Having a fixed copper thickness makes the area of the cross-section of the winding fixed, and hence the current carrying capability is limited. For this project, two turns per layer are considered after careful consideration of possible turns and frequency range. Thus, for each core dimension, the current through the transformer windings is set as a criterion to finalize the power rating, operating frequency and the number of turns of the transformer. For an EILP102 core set, the maximum width of each winding could be 9.5 mm after considering the space for epoxy fill. The thickness of copper is assumed to be 70 μm. Through these windings, 15 A of current can flow, which would raise the PCB temperature to 30 degrees. Hence, 15 A is the maximum limit of current through the windings for an EILP102 core.

4.1.3. Design and calculations of DAB Parameters

As shown in figure 4.1, various parameters like magnetizing inductance, conduction losses, required series inductance, etc., can be calculated based on various input parameters like the power rating of the converter, operating frequency, rated voltages, etc. In this subsection, various important formulas that are used in the script are given:

Series inductance of the DAB

The series inductance in the DAB is the key component which stores energy when there is a phase angle difference between the primary and secondary full bridges. The value of required inductance is given by equation (4.6).

$$L_s = \frac{nV_{pri}V_{sec}\phi(1-\phi)}{2f_sP} \tag{4.6}$$

The maximum power transfer happens at ϕ = 0.5. Hence, the maximum value of series inductance that needs to be present in the DAB to transfer the maximum power of P_{max} is given by

substituting ϕ = 0.5 in equation 4.6.

$$L_{s(max)} = \frac{nV_{pri}V_{sec}}{8f_sP_{max}} \tag{4.7}$$

In an ideal scenario, the series inductor would be designed at a value corresponding to the one calculated from equation (4.7). However, during the design phase, the series inductor is designed for a value lower than the $L_{s(max)}$ because of various reasons, some of which are stated below:

- The DAB can have losses and hence can be rated for higher values of power transfer.
- The converter may need to deliver higher power at times, depending on the application.
- The leakage inductance of the transformer also contributes to the series inductor, and it is difficult to exactly estimate the value.

For the external inductor value, first, the transformer leakage inductance has to be calculated (which is discussed in section 5.1.4). There are various possibilities for avoiding an additional external inductor. There is research going on to design the transformer such that its leakage inductance can be equal to the required series inductance. However, generally, the leakage inductance of the transformer is low and also difficult to estimate. To increase the leakage inductance of the transformer, various techniques, like using a magnetic shunt and different winding configurations, are studied in the literature [27], [28], [29].

Magnetizing inductance

$$L_m = N_{core}A_lN^2 \tag{4.8}$$

By introducing an airgap, there is a fringing factor that is introduced. This is given by equation (4.9) [30].

$$FF = 1 + \frac{A_g}{\sqrt{N_{core}A_c}} * ln\left(\frac{2H_w}{A_g}\right) \tag{4.9}$$

So, the magnetizing inductance when an air gap is introduced in the core is calculated as shown in the equation (4.10) [30].

$$L_{m(gap)} = FF * \frac{\mu_0N^2N_{core}A_c}{A_g + \frac{MPL}{\mu_r}} \tag{4.10}$$

Magnetizing current

Magnetizing current in a DAB depends on several factors. Having a higher magnetizing current helps in having a higher ZVS range. However, since the magnetizing current is also composed of circulating currents, a higher value of magnetizing currents causes higher losses in the circuit. Hence, it becomes necessary to estimate magnetizing currents. The peak magnetizing current in the circuit, at a given phase angle ϕ, is given by equation (4.11) [31].

$$I_{m(peak)} = \frac{\frac{1-\phi}{2f_s} * (V_{pri}L_{lkp} + nV_{sec}n^2L_{lks}) + \frac{\phi}{2f_s} * (V_{pri}n^2L_{lks} + nV_{sec}L_{lkp})}{2L_{m(eff)}\left(L_{lkp}\left(1 + \frac{L_{lks}}{L_{m(eff)}}\right) + n^2L_{lks}\right)} \tag{4.11}$$

The maximum magnetizing current is observed when ϕ is equal to 0. Hence, the maximum magnetizing current is given as shown in equation (4.12)

$$I_{m(max)} = \frac{\frac{1}{2f_s} * (V_{pri}L_{lkp} + nV_{sec}n^2L_{lks})}{2L_{m(eff)}\left(L_{lkp}\left(1 + \frac{L_{lks}}{L_{m(eff)}}\right) + n^2L_{lks}\right)} \tag{4.12}$$

Primary and Secondary RMS Currents

The currents flowing through the transformer windings are shown as primary (I_p) and secondary (I_s) currents in figure 4.5. The analysis carried out in this section is valid for $0 < \phi < 0.5$.

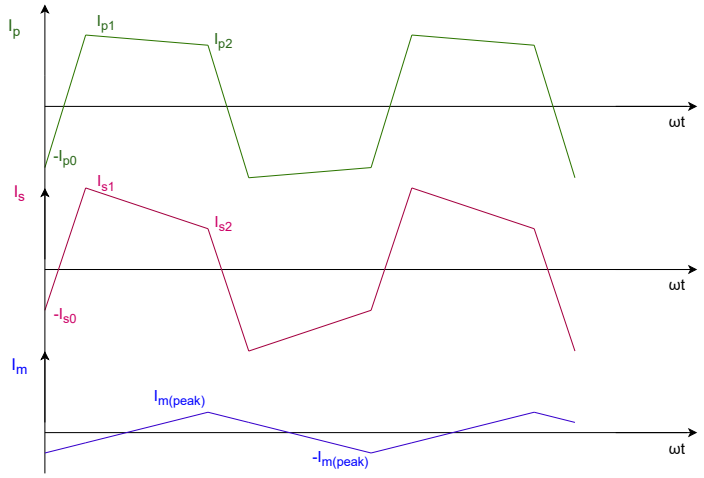


Figure 4.5: Primary, secondary and magnetizing current waveforms

Referring to figure 4.5, the primary and secondary RMS currents are given by equations (4.13) and (4.14) respectively.

$$I_{p_{rms}} = \sqrt{\frac{\phi(I_{p0}^2 + I_{p0}I_{p1} + I_{p1}^2)}{6} + \frac{(2-\phi)(I_{p1}^2 + I_{p1}I_{p2} + I_{p2}^2)}{6}} \tag{4.13}$$

$$I_{s_{rms}} = \sqrt{\frac{\phi(I_{s0}^2 + I_{s0}I_{s1} + I_{s1}^2)}{6} + \frac{(2-\phi)(I_{s1}^2 + I_{s1}I_{p2} + I_{s2}^2)}{6}} \tag{4.14}$$

where, the values of currents I_{p0}, I_{p1}, I_{p2}, I_{s0}, I_{s1} and I_{s2} are given by the equations below [22], [31]:

$$I_{p0} = \frac{V_{pri}K_2\left((M - \frac{K_1}{K_2}) - 2M\phi\right)}{4f_sL_s} \tag{4.15}$$

$$I_{s0} = \frac{V_{pri}K_1\left((M - \frac{K_2}{K_1}) + 2M\phi\right)}{4f_sL_s} \tag{4.16}$$

$$I_{p1} = I_{p0} + \frac{(V_{pri}K_1 + nV_{sec}K_2)\phi}{2f_sL_s} \tag{4.17}$$

$$I_{s1} = I_{s0} + \frac{(V_{pri}K_2 + nV_{sec}K_1)\phi}{2f_sL_s} \tag{4.18}$$

$$I_{p2} = I_{p1} + \frac{(V_{pri}K_1 - nV_{sec}K_2)(1-\phi)}{2f_sL_s} \tag{4.19}$$

$$I_{s2} = I_{s1} + \frac{(V_{pri}K_2 - nV_{sec}K_1)(1-\phi)}{2f_sL_s} \tag{4.20}$$

These primary and secondary RMS currents are used to find the copper losses in the transformer and also the switch currents.

Switch Currents

Since a constant duty cycle of 0.5 is implemented on both the full bridges, the primary and secondary switch currents are given by the equations (4.21) and (4.22).

$$I_{p_{sw_{rms}}} = \frac{I_{p_{rms}}}{\sqrt{2}} \tag{4.21}$$

$$I_{s_{sw_{rms}}} = \frac{I_{s_{rms}}}{\sqrt{2}} \tag{4.22}$$

These currents are used to determine the maximum switch conduction losses.

Effective Flux Density

Since there is an air gap in the core, the effective flux density is as in equation (4.23) [30].

$$B_{eff} = FF\frac{\mu_{r_{gap}}\mu_0 N I_{m(peak)}}{MPL} \tag{4.23}$$

Where, $\mu_{r_{gap}}$ is given by equation (4.24).

$$\mu_{r_{gap}} = \frac{\mu_r}{1 + \frac{\mu_r A_g}{MPL}} \tag{4.24}$$

Winding losses

Since the windings are constructed as copper traces in the PCB, winding loss calculations can be more accurate compared to the calculations done for conventional windings. Firstly, since the currents flowing through the winding have high frequencies, it is important to estimate the AC resistance - considering skin and proximity effect losses. The AC resistance of m^{th} layer

for the design, which considers the given thickness of windings and given turns per layer, is given in equation (4.25) [32].

$$R_{ac} = \frac{R_{dc}\xi}{2}\left(\frac{sinh(\xi)+sin(\xi)}{cosh(\xi)-cos(\xi)} + (2m-1)^2.\frac{sinh(\xi)-sin(\xi)}{cosh(\xi)+cos(\xi)}\right) \tag{4.25}$$

$$\xi = \frac{Trace\ thickness}{skin\ depth}, \qquad skin\ depth = \sqrt{\frac{2\rho}{2\pi f_s \mu_0}} \tag{4.26}$$

$$R_{dc} = L_{coil} N \rho / A_{coil} \tag{4.27}$$

Where L_{coil} is the length of 1 turn of the winding and A_{coil} is the area of the coil and is given as the product of PCB copper thickness and the width of the trace.

$$P_{wind} = I^2_{p_{rms}} R_{p_{ac}} + I^2_{s_{rms}} R_{s_{ac}} \tag{4.28}$$

Core losses

In general, for sinusoidal excitations, the Steinmetz equation (SE) is used to calculate the core losses. There is enough literature to study various methods to estimate the core losses for non-sinusoidal excitations [33], [34]. As proposed by S. Yue et al, out of Modified SE (MSE), Generalised SE (GSE), improved GSE (IGSE) and waveform coefficient SE (WcSE), IGSE has superior precision when the harmonics count (extreme duty cycle area), whereas WcSE is more suitable in the event of relatively low harmonics content of H. In addition, IGSE has better frequency applicability than WcSE and can follow the changing pattern of core loss with the duty cycle better [35]. However, after implementing both IGSE amd MSE, the difference in losses estimated is minute and hence, for ease of calculation, MSE is used for core loss estimation.

$$P_{core} = N_{core} V_{core} \frac{C_m f_s^{\alpha} B_{eff}^{\beta} 2^{\alpha-1} (D^{1-\alpha}(1-D)^{(\alpha-1)}}{\pi^{2(\alpha-1)}} \tag{4.29}$$

where D is the duty cycle, α, β and C_m are the Steinmetz coefficients of the core material, V_{core} is the volume of the core. Note that f_s is in kHz and B_{eff} is in mT.

Maximum Switch Conduction Loss

For the script, the on-state resistance is assumed to be 250 mΩ which corresponds to the value at a junction temperature of 110 ^{O}C. So, the total conduction loss of all the switches is given by equations (4.30).

$$P_{cond} = 2I^2_{p_{sw_{rms}}} R_{ds(on)} + 2I^2_{s_{sw_{rms}}} R_{ds(on)} \tag{4.30}$$

Maximum Switching Loss

To estimate the switching loss, equation (4.31) is used. Since the converter is assumed to operate in ZVS at maximum load point, the turn-on losses are neglected.

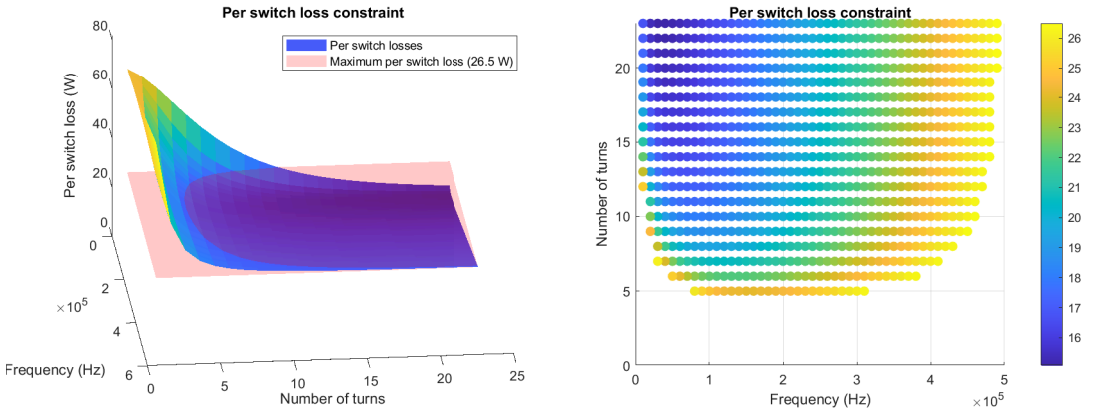
$$P_{sw} = 4\left(\frac{E_{off} f_s (V_{pri(max)} I_{p2} + V_{sec(max)} I_{s1})}{V_{nom} I_{nom}} - \frac{E_{oss} f_s (V_{pri(max)} + V_{sec(max)})}{V_{oss_{nom}}}\right) \quad (4.31)$$

4.1.4. Script Results

The maximum power level of the possible converter is found by running the script for various values of power. It is observed that with given constraints and optimization limits, 12 kW of power transfer can be possible. Hence, the final results are drawn based on the power converter limit of 12 kW.

Per Switch Loss

As discussed earlier, the limit for per switch loss is set to 26.5 W. Figure 4.6 (a) shows the 3D plot of the variation of per switch losses with different number of turns of the transformer and the switching frequencies. Also, it shows the plane which represents the maximum limit that is taken as the constraint for this optimization. It can be observed that the losses in a switch can reach up to almost 65 W for certain frequencies and the number of turns combinations. Figure 4.6 (b) shows the final per-switch losses for various number of turns and switching frequencies after the constraints are implemented.



((a)) 3D plot of per switch loss and the maximum limit

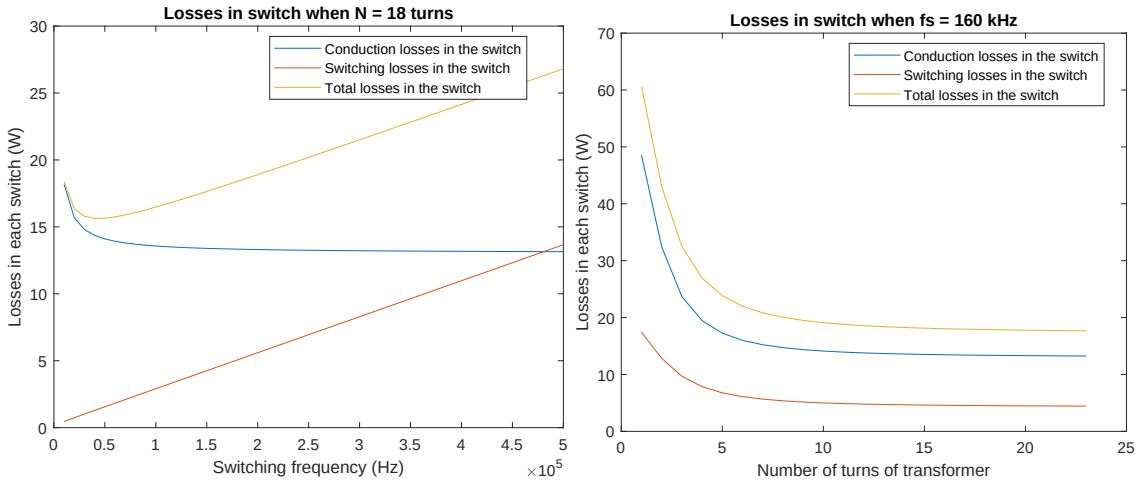
((b)) 2D representation of per switch losses less than 26.5 W

Figure 4.6: Possible solutions for per switch loss optimization limits

In figure 4.6 (b) it can be seen that for the given number of turns, the losses in the switch are high for low frequencies, then decrease for certain frequencies and finally increase for higher frequencies. This is because the conduction losses are dominant at low frequencies and as the frequency increases, the conduction losses sharply decrease due to a decrease in magnetizing currents till a certain frequency level. However, after a certain frequency range, switching losses become dominant and hence increase the overall losses. This can be seen in figure 4.7 (a) where the losses in the switch are plotted for various frequencies keeping the number of turns of the transformer to a fixed value (18 turns).

Similarly, for a given frequency, the losses in the switch decrease as the number of turns of the transformer increase. Increasing the number of turns of the transformer increases the magnetizing inductance of the transformer quadratically, as shown in equation (4.10), which leads to a decrease in magnetizing current and hence decrease in the conduction and switching losses.

However, after a certain number of turns, the magnetizing current becomes significant compared to the switch RMS currents (excluding circulation currents) and hence the loss reduction also becomes insignificant. This can be seen in figure 4.7 (b).



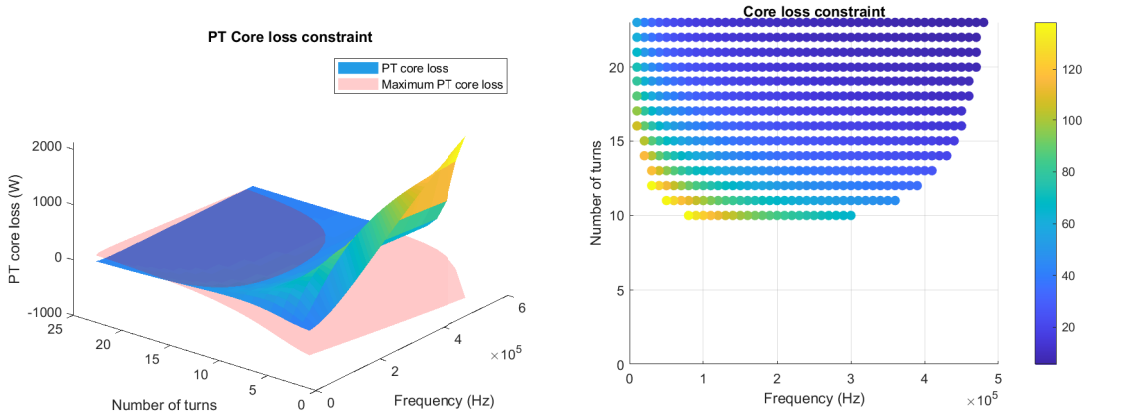
((a)) Variation of losses in a switch with frequency

((b)) Variation of losses in a switch with the number of turns

Figure 4.7: Variation of losses in a switch

PT core Loss

As discussed in the previous subsection, the core loss is calculated using equation (4.29).



((a)) 3D plot of PT core loss and the maximum limit

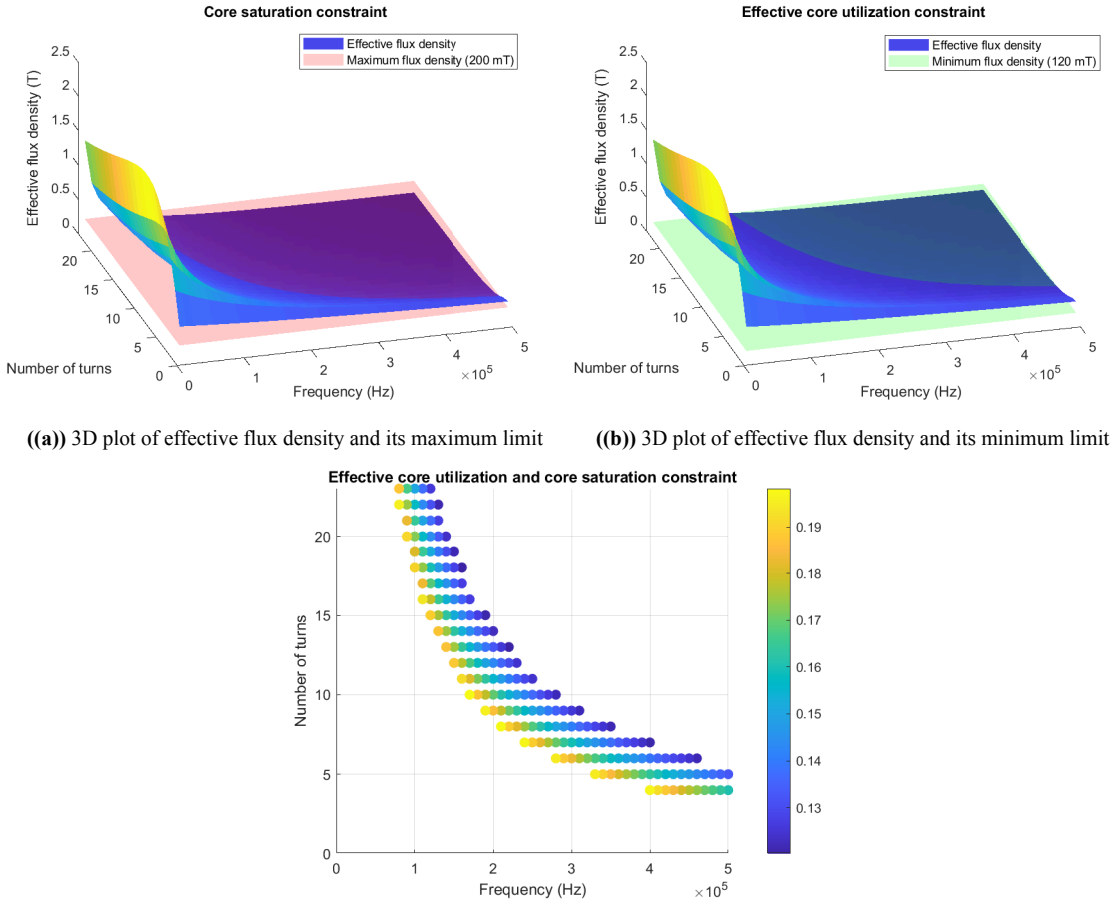
((b)) 2D representation of PT core loss less than the maximum limit

Figure 4.8: Possible solutions for PT core loss optimization limits

It can be seen that the PT core loss increases with a decrease in the number of turns. This is because the effective flux density increases with a decrease in the number of turns. With the increase in frequency, according to equation (4.29), the core losses should ideally increase. However, the effective flux density is dependent on the frequency. With the increase in frequency, the effective flux density decreases. Hence, the overall core loss decreases.

Effective Core Utilization and Core Saturation

Figures 4.9 (a) and (b) show the variation of effective flux density with switching frequency and number of turns of the transformer. They also show the constraint plots. Figure 4.9 (c)



((a)) 3D plot of effective flux density and its maximum limit

((b)) 3D plot of effective flux density and its minimum limit

((c)) 2D representation of effective flux density between 120 mT and 200 mT

Figure 4.9: Possible solutions for effective core utilization optimization limits

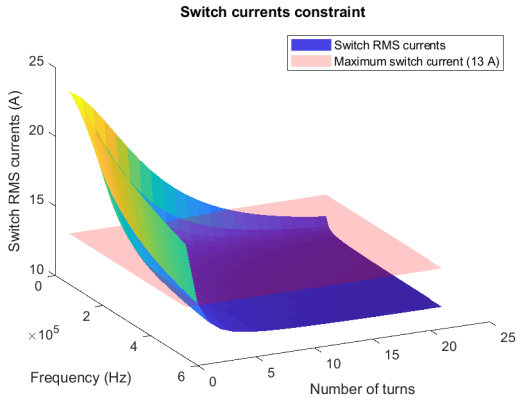
shows the final effective flux densities for the combinations of frequency and number of turns that meet the constraint limits. It also shows that the effective flux density is higher at lower frequencies and it increases with an increase in frequency. Thus, to meet the constraint of 120 mT < B_{eff} < 200 mT, a narrow range of the number of turns and frequencies is finalized.

Switch Currents

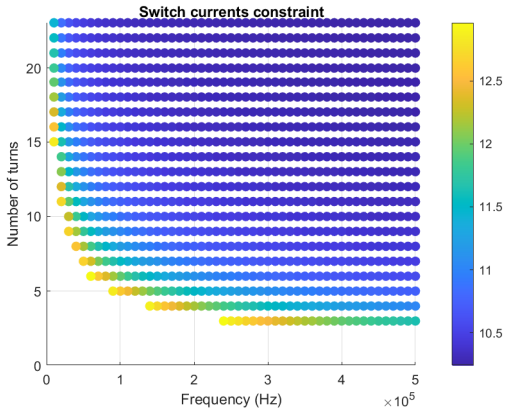
Figure 4.10 (a) shows the variation of switch currents with various switching frequencies and the number of turns of the transformer along with a plot of limits for the same. Figure 4.10 (b) shows the switch currents variation after considering the constraints.

Again, the variation of magnetizing current is the reason for the variation of the switch currents. As frequency increases, initially, the magnetizing current drops drastically. Slowly, the effect of magnetizing current on the current flowing through the switch deteriorates.

Increasing the number of turns increases the magnetizing inductance and hence decreases the magnetizing currents, thereby decreasing the switch RMS currents.



((a)) 3D plot of switch RMS currents and the maximum limit

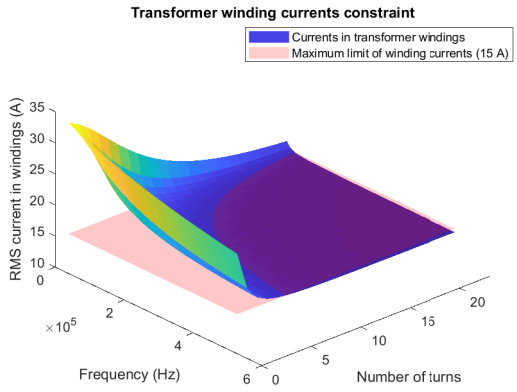


((b)) 2D representation of switch RMS currents less than 13 A

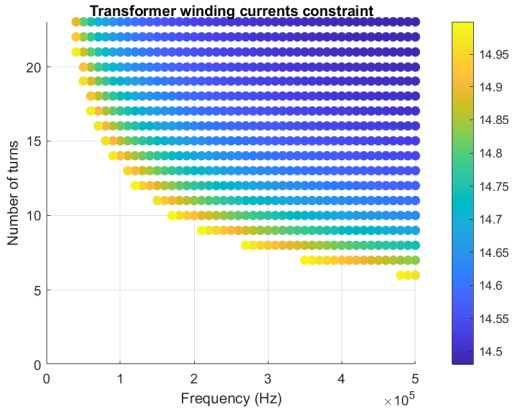
Figure 4.10: Possible solutions for switch RMS currents optimization limits

Transformer Winding RMS Currents

Similar to the above figures, figure 4.11 (a) shows the variation of currents through the windings of the transformer with various switching frequencies and the number of turns of the transformer.



((a)) 3D plot of transformer RMS currents and the maximum limit



((b)) 2D representation of transformer RMS currents less than 15 A

Figure 4.11: Possible solutions for transformer RMS currents optimization limits

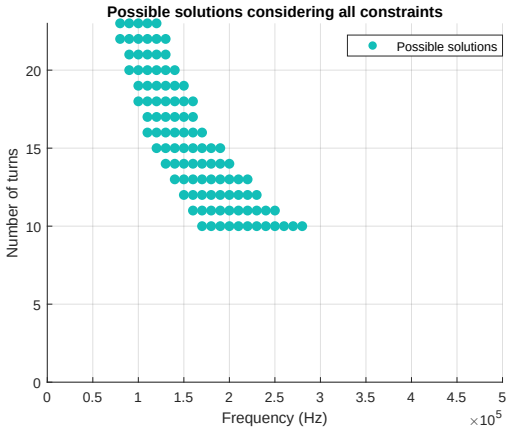
Similar to switch currents, the variation of transformer winding currents can be attributed to the variation in magnetizing currents. The same explanation holds good for this case as well.

Possible solutions and Efficiencies

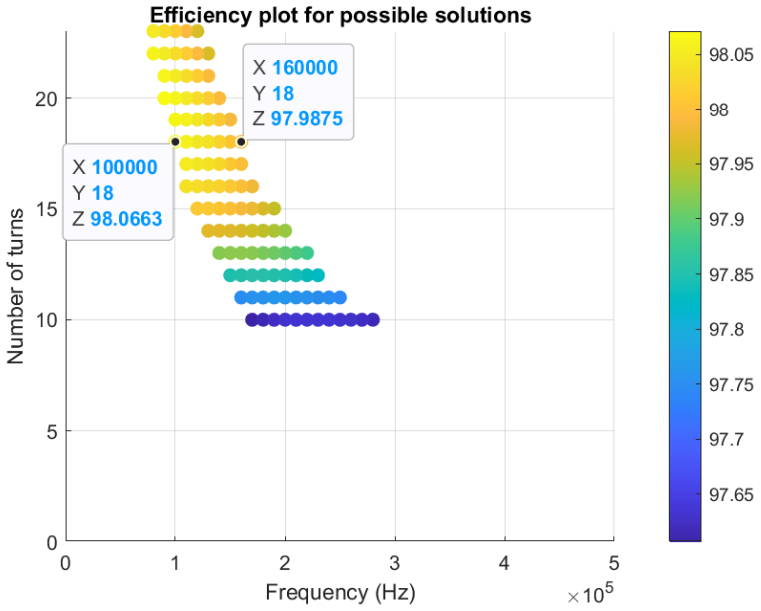
Combining all the possible solutions obtained by all the constraints, the final possible solutions of the number of turns of the transformer and the switching frequencies are given in figure 4.12 (a). The theoretical efficiency plot of the converter (Considering switch losses and transformer losses) is shown in figure 4.12 (b).

From figure 4.12 (b), it can be seen that for a given frequency, the higher the number of turns, the higher the efficiency. However, from the manufacturing capabilities, a 12-layer PCB with 2 Oz copper is the most economically viable option. With the winding arrangement designed

in section 5.1.3, 18 turns is possible and hence that is selected. At N = 18, though at higher frequencies, the efficiency is lower, the external series inductor requirement is lower. Which decreases the losses in the additional inductor. Hence, the switching frequency of 160 kHz is selected.



((a)) Possible solution of the number of turns of transformer and switching frequencies



((b)) Efficiency variation with number of turns and frequencies

Figure 4.12: Final possible solutions and efficiencies for power transfer of 12 kW

Table 4.2: The final parameter list of the DAB with N = 18, f_s = 160 kHz and rated for 12 kW

Effective flux density	120.2 mT	**Per switch loss**	17.9 W
Core type	2x(EILP 102) - N95	**Core loss**	21.5 W
Air gap	0.1 mm	**Copper loss**	117.95 W
Theoretical efficiency	97.9 %	**Effective magnetizing inductance**	2.6 mH
Peak magnetizing current	0.9 A	**Switch RMS current**	10.34 A
Required series inductance	146 μ H	**Transformer RMS current**	14.63 A

4.2. Power Rating of DAB and DC-Link Capacitor Rating

One of the system-level requirements is the power rating of the SST. DC Opportunities aimed to design the SST with at least a 100 kVA power rating. The converter is to be designed using SiC MOSFETs. After a thorough market analysis, the following 1700 V switches were shortlisted:

Table 4.3: Market survey results for switch selection

Mfr. part number	I_D (A)	$R_{DS(on)}$ (mΩ)	Price (€ / piece)
IMBF170R450M1XTMA1	9.8	450	8.58
LSIC1MO170T0750	6.4	750	9.28
IMBF170R650M1XTMA1	7.4	650	6.69
C2M1000170J	5.3	1000	9.36
G2R1000MT17J	5	1000	6.66
G3R450MT17J	7	450	8.32
G3R160MT17J	18	160	13.41

Out of these, considering the current ratings, on-state resistance and the price, G3R160MT17J from GeneSiC was finalized. The maximum switch current was considered one of the constraints for the power rating of the DC-DC converter.

The approach followed in order to determine the power rating of SST is as follows:

1. The maximum single-cell DAB power rating is obtained based on various constraints mentioned in section 4.1.2.
2. Average current of the DAB cell can be obtained for various DC grid voltage levels.
3. The analysis is carried out to determine the maximum current drawn by the inverter stage in each cell. This is shown in section 4.2.1.
4. Determine the DC link capacitor rating as given in section 4.2.2.
5. Determine the power of SST at a given line-line voltage of AC grid using equation (4.32).

In section 4.1.4, it is concluded that a single-cell DAB network is designed for 12 kW after all the constraint considerations. Hence, at 1500 V, the average output current of the DAB = 12000/1500 A = 8 A.

Substituting Io = 8 A in equation (4.34), the peak current of the inverter is calculated to be 12.566 A. The power corresponding to this current, when the grid voltage is 10 kV is obtained from equation (4.32). So, the theoretical power rating of the SST is 153.9 kW. So, hereafter, the power rating considered for the SST design is 150 kW.

4.2.1. Charge Balance of the DC Link Capacitor and DAB Rating

In order to maintain a steady voltage with minimal voltage ripple at the output of the DAB cell and before the input of the inverter cell (referred to as DC link hereafter), a high-value capacitor is added. This is referred to as the DC link capacitor hereafter.

The selection of the DC link capacitor value becomes critical because, with a higher value of

the capacitor, the cost of the converter increase, black-start time increases as the higher value capacitors take higher time to charge, and eventually the system becomes bulkier. On the other hand, if the value is lower, the voltage ripple increases, the phase angle fluctuates often thereby pushing the converter into the non-ZVS region and in this particular application, due to overvoltage, the switches may influence higher stresses with the possibility of failure.

In order to decide on the value of the capacitor, the charge balance principle is followed. The ideal waveform of the current at the input of each inverter cell is shown in figure 4.13 where Ip is the peak current and is obtained by equation (4.32). As shown in the figure, the waveform repeats every 10 ms (100 Hz), assuming the AC grid frequency is at 50 Hz.

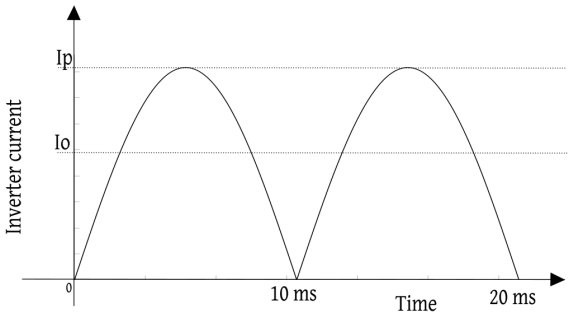


Figure 4.13: Ideal current waveform at the input of each inverter cell

$$Ip = \frac{P_{SST_{max}}}{\sqrt{3} * V_{ll(rms)}} * \sqrt{2} \tag{4.32}$$

here, $P_{SST_{max}}$ is the maximum power rating of the SST and $V_{ll(rms)}$ is the line-to-line rms value of the AC grid voltage.

Power transfer from the DC grid to the AC grid

When the power flows from the DC grid to the AC grid, the current drawn by the inverter is the sum of the current transferred by the DAB and the DC link capacitor. When the current transferred by DAB is higher than the current drawn by the inverter, the DC link capacitor is charged. Similarly, when the current transferred by DAB is smaller than the current drawn by the inverter, the DC link capacitor supplies the difference of current and hence discharges.

$$i_{DAB} + i_{cap} = i_{inv}$$

$$i_{cap} = i_{DAB} - i_{inv}$$

$$if\ i_{inv} < i_{DAB}, i_{cap} > 0\ .....Charging$$

$$if\ i_{inv} > i_{DAB}, i_{cap} < 0\ .....Discharging$$

Power transfer from the AC grid to the DC grid

When the power flows from the AC grid to the DC grid, the power drawn by the DAB cell is the sum of current transferred by the inverter and the DC link capacitor. When the current transferred by DAB is higher than the current drawn by the inverter, the DC link capacitor is

discharged. Similarly, when the current transferred by DAB is smaller than the current drawn by the inverter, the DC link capacitor discharges.

$$i_{DAB} + i_{cap} = i_{inv}$$
$$i_{cap} = i_{inv} - i_{DAB}$$
$$if\ i_{inv} > i_{DAB}, i_{cap} > 0\ .....Charging$$
$$if\ i_{inv} < i_{DAB}, i_{cap} < 0\ .....Discharging$$

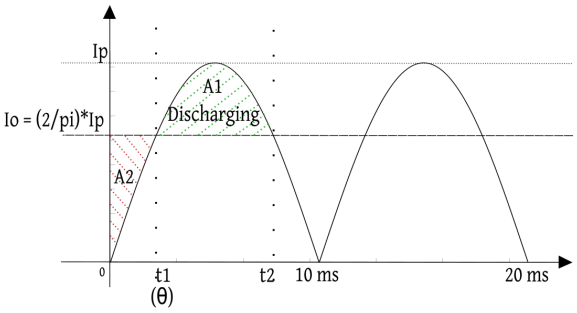


Figure 4.14: Charge balance of DC link capacitor

Referring to figure 4.14, assuming power transfer from DC grid to AC grid, Ip indicates the peak value of current drawn by the inverter, and Io is the average current transferred by DAB. To maintain the charge balance of the DC link capacitor, area A1 should be equal to area 2*A2. In order to find Io, the following integral can be solved, which is obtained by equating the A1 to 2*A2:

$$2\left(\theta sin(\theta) - \int_0^{\theta} sin(x)dx\right) = \int_{\theta}^{\pi-\theta} sin(x)dx - (\pi - 2\theta)sin(\theta) \tag{4.33}$$

Upon solving the above equation,

$$sin(\theta) = \frac{2}{\pi} \Rightarrow Io = \frac{2Ip}{\pi} \tag{4.34}$$

$$\theta = sin^{-1}(2/pi) = 39.54^o \tag{4.35}$$

From the above analysis, it is evident that the average current delivered by the DAB should be equal to 2/pi times the peak current of the current drawn by the inverter.

Since the maximum DAB power limits are obtained based on various limiting factors described in section 4.1.2, the maximum power rating of the entire SST at a given line-line AC voltage can be obtained using the above analysis and equation (4.32).

To achieve 150 kW power transfer, at 10 kV line-line RMS value, the inverter draws current with a peak value of 12.25 A. So, the DAB should be rated to deliver 2*12.25/π = 7.8 A on average. If this current has to be delivered when the DC voltage is 1500 V, the DAB power rating should be at least 11.7 kW ignoring the losses in the converter.

4.2.2. DC-Link Capacitor Rating

In this sub-section, the analytical formula to estimate the required capacitance is derived initially. This is derived based on the basic current through the capacitor formula. Once the final calculation is made, the same is verified using the PLECS simulation.

In figure 4.14, consider the power transfer from the DC grid to the AC grid. Then, area A1 represents the discharging mode of the capacitor. This charging and discharging of the capacitor causes a ripple in the voltage across the capacitor. The value of the capacitor can be calculated in order to maintain this ripple voltage under a certain threshold. The rating of the capacitor is determined as follows:

From the basic capacitor formula,

$$Cdv = \int Idt \tag{4.36}$$

referring to figure 4.14, Cdv should be equal to the area A1 as that is the discharging period of the capacitor.

$$Cdv = \int_{t1}^{t2} Ip * sin(\omega t)dt - Io(t2 - t1) \tag{4.37}$$

$$Cdv = \frac{Ip}{\omega}\left[cos(\omega t1) - cos(\omega t2)\right] - Io(t2 - t1) \tag{4.38}$$

Since sin(ωt) is considered to be repeating after every interval of π, $\omega = \pi$f. Further substituting equation (4.34) in equation (4.38),

$$Cdv = \frac{Ip}{\pi f}\left[cos(\omega t1) - cos(\omega t2)\right] - \frac{2Ip}{\pi}(t2 - t1) \tag{4.39}$$

from figure 4.14, substituting ωt1 = 39.54^o, ωt2 = 140.46^o and t1 = 2.2 ms and t2 = 7.8 ms and f = 100 Hz, one gets,

$$Cdv = \frac{Ip}{\pi 100}\left[cos(39.54^o) - cos(140.46^o)\right] - \frac{2Ip}{\pi}(7.8 - 2.2)10^{-3} \tag{4.40}$$

$$Cdv = 1.344Ip * 10^{-3}\ farad\ volts \tag{4.41}$$

So, when Ip = 12.25 A, and C is 500 μF, dv should be $\frac{1.344*12.25*10^{-3}}{500*10^{-6}}$ = 32.93 V. This is verified using PLECS model whose results are shown in figure 4.2.2. It can be seen that the voltage ripple observed in the PLECS simulation is 36 V, which is slightly higher than the calculated value. This can be because of the non-constant output current of DAB.

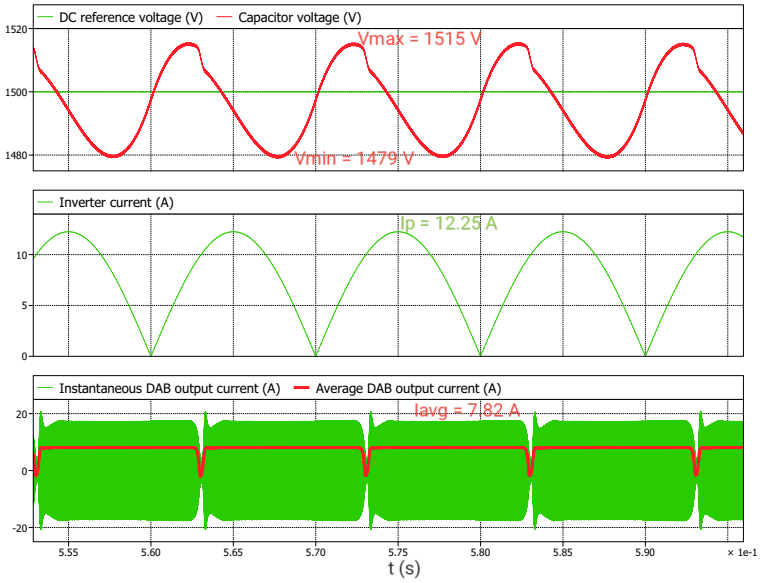


Figure 4.15: PLECS results to verify capacitor rating and voltage ripple

4.3. EMI Filter Design

The currents drawn by the converter from the source are not sinusoidal. Hence, they carry harmonic content which leads to various problems like overheating of the transformer, electrical fires, voltage notching motor vibrations etc. In order to limit the harmonics, various regulations are set. In order to filter out such high harmonics, a differential mode filter is designed and implemented.

In other instances, there could be electromagnetic interference with external devices which could possibly lead to a flow of currents from the terminals of the converter and return through parasitic capacitances to the protective earth (PE). In order to limit these currents, a common mode filter is employed.

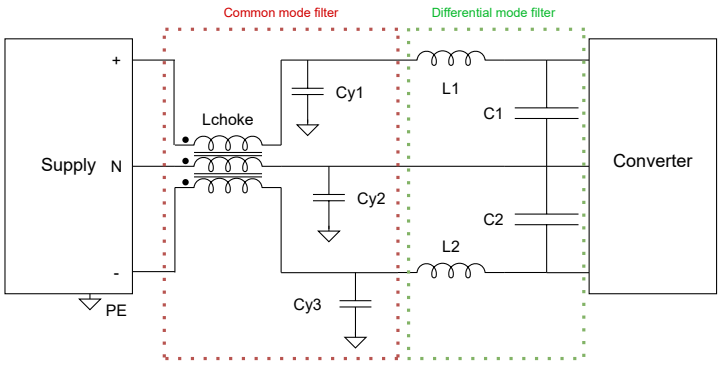


Figure 4.16: Input EMI filter representation for bipolar DC grid

4.3.1. Differential Mode Filter

According to Middle Brook's instability criteria, the input impedance of the converter should be significantly higher than the output impedance of the filter for a stable operation. The input impedance of the converter can be approximated as given in equation (4.42).

$$Z_{in} = \frac{V_{in}^2 \eta}{P_{out}} \tag{4.42}$$

For this application, the minimum input voltage is 1360 V. Assuming 95% converter efficiency and the output power of 12 kW, Z_{in} is calculated to be 146.42 Ω.

The output impedance of the differential mode filter is given in equation (4.43) where L_d is the differential filter inductor (equal to L1 + L2 from figure 4.16) and C_d is the differential filter capacitor (equal to C1*C2/(C1+C2) from figure 4.16).

$$Z_{out} = \sqrt{\frac{L_d}{C_d}} \tag{4.43}$$

To respect Middle Brooks instability criteria, Z_{out} <= Z_{in}/10 and to have a cut-off frequency below 1/10th switching frequency, $1/(2\pi\sqrt{L_d C_d})$ <= f_{sw}/10. Considering f_{sw} = 160 kHz and solving the two inequalities, we find that $C_{d_{min}}$ = 0.71 μF and $L_{d_{max}}$ = 139 μH.

L1 and L2 from figure 4.16 can be assumed as the leakage inductance of the 3-phase choke (Lchoke). Thus L_d can be treated as the leakage inductance of the choke. Assuming the leakage inductance of the choke is 1% of the 3-phase choke inductance value, the 3-phase choke of approximately 10 mH is chosen.

Thus, L_d = 0.1 mH and C_d = 1 μF $\Rightarrow$ C1 = C2 = 2 μF. However, since the current ratings for 2 μF capacitors are low, 2 are added in parallel. This would slightly reduce the cut-off frequency and the filter's output impedance, which is beneficial if space is not a constraint. So, C_d = 2 μF

When the designed differential filter is considered, the gain at the cut-off frequency has a high Q factor and the impedance at the cut-off frequency shoots up violating Middle Brook's instability criteria. This is shown in figure 4.17 where R = 43.2 mΩ represents the ESR of the capacitors.

In order to improve this scenario by making the Q almost equal to 1, a damping resistor can be added in series with the existing capacitors in addition to the ESR. However, that would affect the -40 dB/dec roll-off after the cut-off frequency. Hence a large value of the capacitor (Generally 5*C_d) is used along with an external damping resistor to make the Q factor 1 and the roll-off to be the same. The Bode plot of the filter with and without damping circuit is shown in figure 4.18.

The Q factor is given by equation (4.44). In order to maintain Q = 1, R_{damp} has to be selected such that equation (4.45) is met.

$$Q = \frac{1}{R_{damp}} \sqrt{\frac{L_d}{C_d}} \tag{4.44}$$

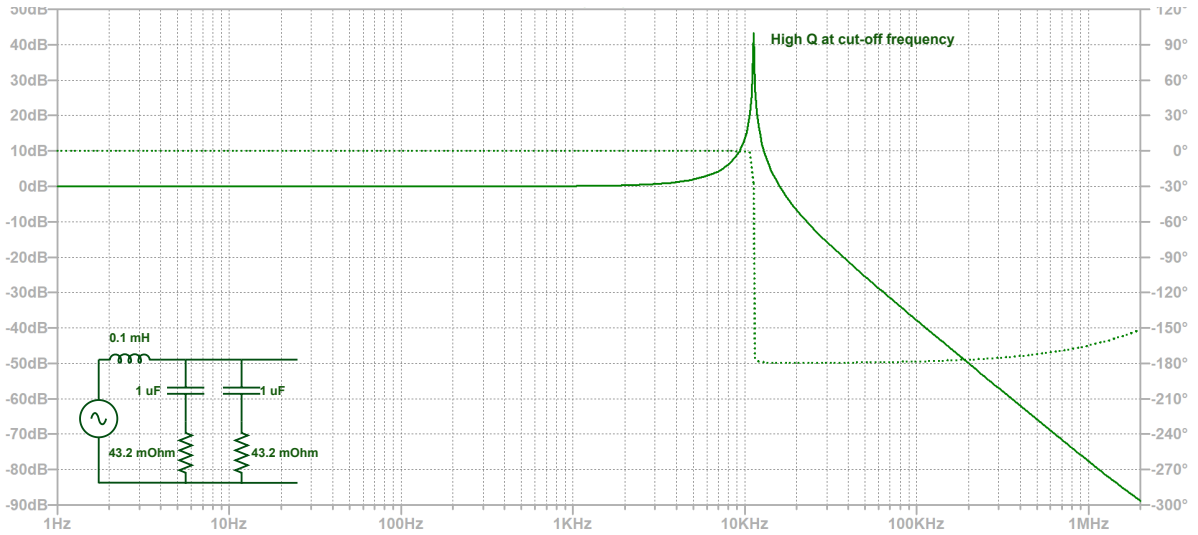


Figure 4.17: Bode plot for the designed differential mode filter to verify high gain at cut-off frequency

$$R_{damp} = \sqrt{\frac{L_d}{C_d}} = \sqrt{\frac{100e-6}{2e-6}} = 7\Omega \tag{4.45}$$

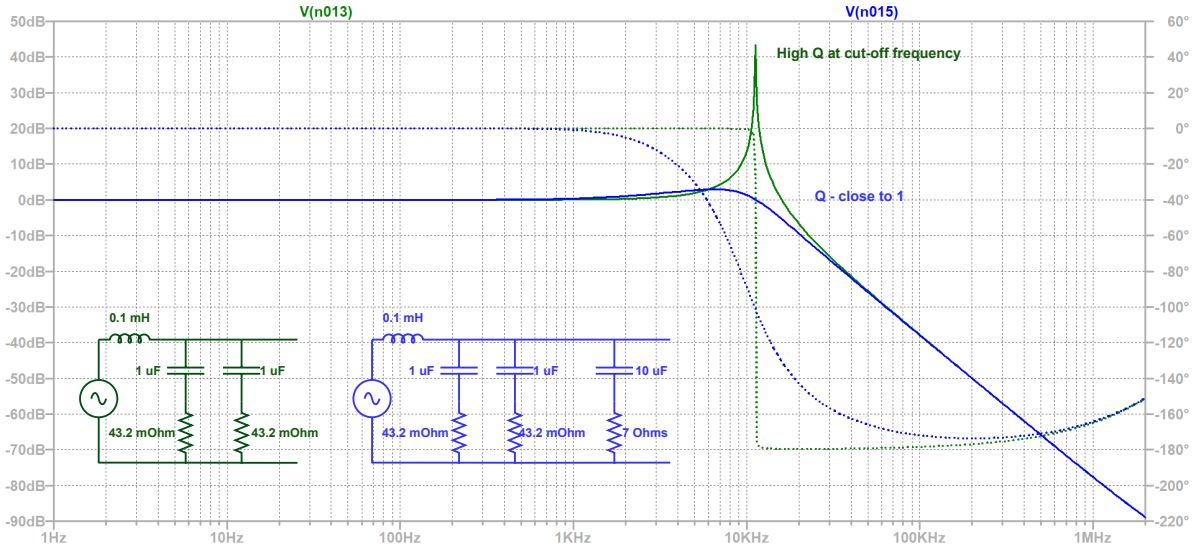


Figure 4.18: Bode plot for the designed differential mode filter with and without damping network

4.3.2. Common Mode Filter

As discussed in the previous section, the common mode choke is selected to provide enough leakage inductance that can directly act as the differential mode leakage. This is economical as there would not be the need for an extra inductor. Another approach is to perform a study on choosing the good size balance of one 3-phase EMI choke and three Y-capacitors. For this project, the first approach is followed. Hence, a 3-phase choke of 10 mH is chosen.

The common mode filter is designed for a cut-off frequency of 75 kHz. Thus the Y-caps are

designed to meet the cut-off frequency requirement of 75 kHz.

$$C_y = \frac{1}{4\pi^2(75 * 10^3)^2 L_{choke}} \tag{4.46}$$

Upon solving equation (4.46), C_y is found to be 4.5 nF.

As a general practice, to get some extra attenuation, pi capacitors (C_{pi}) are added before the common mode choke. These help in differential mode filtering and have no role in common mode filtering. In order to not affect the cut-off frequency, the value of C_{pi} needs to meet the following two conditions:

- $C_{pi} < C_d/5 \Rightarrow C_{pi} < 0.4\ \mu$F
- $C_{pi} > \frac{1}{10\pi f_{sw}} \Rightarrow C_{pi} > 0.2\ \mu$F

Since C_{pi} has to be a combination of two capacitors in series, just like C_d, each capacitor has to be 2*C_{pi}. Hence, the limits are between 0.4 μF and 0.6 μF. As a standard-rated capacitor, 0.47 μF capacitors are chosen. The final input EMI filter with all the parameters is shown in figure 4.19.

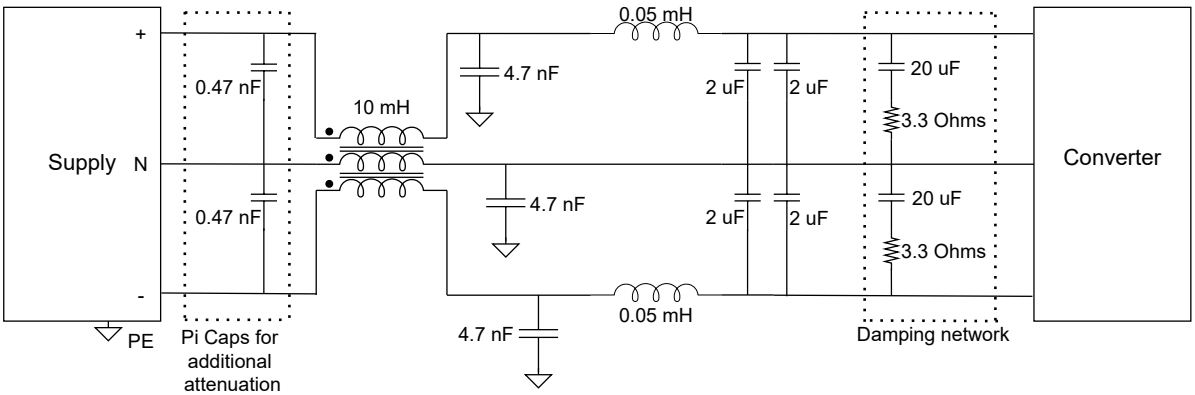


Figure 4.19: Final input EMI filter with designed parameters

4.4. Summary

In this chapter, the first section discusses the design aspects of the DAB converter with PT. It mainly addresses the objectives, constraints and results of the DAB with PT script that is developed as a part of the project. The main objective of the script is to identify the most optimal values of various parameters for having low manufacturing costs and high efficiencies. Various approaches to setting the constraints to the optimization script parameters have been discussed in this chapter. Based on the script results, DAB parameters were selected and finalized. The operating frequency has been chosen as 160 kHz and the number of turns of the transformer has been chosen as 18. The final parameter list is given in table 4.2

In the second section of this chapter, the power rating and DC-link capacitor ratings were evaluated based on basic principles. Each DAB cell is designed for 12 kW power and the DC

link capacitor is designed to be 500 μF to have the voltage ripple of 33 V when AC grid voltage is 10 kV. Finally, in the last section, the input EMI filter design was discussed in the chapter and the final design parameters of both common mode and differential mode filter were shown in figure 4.19.

5

Planar Magnetics

This chapter is broadly classified into two sections - planar transformer and planar inductor. In the PT section, the detailed design of the PT is discussed along with different shielding and termination concepts and the analytical leakage inductance estimation technique. Further, in the planar inductor chapter, the comparison of planar and conventional wire-wound inductors is made based on the analytical calculations. Finally, the PI design is compared to the conventional inductor design to analyze the effectiveness of planar magnetics.

5.1. Planar Transformer

As mentioned in section 1.2.2, there are numerous advantages of using PTs. However, the physical implementation of PTs is a challenging task as there are various interdependencies and constraints to designing and implementing an optimal and efficient PT. Also, the need for medium voltage isolation introduces additional challenges.

5.1.1. Medium-Voltage Isolation

One of the key requirements in this converter is the isolation levels. As mentioned in section 1.2.2, isolation is needed to serve various functions. Since the output of each DAB cell is connected to an inverter which is connected in series at the output, the topmost DAB cell needs to be rated for MV isolation between the primary and secondary coil. In the design of the single-cell network of this project, the primary side converter and the planar transformer are stationed on one heatsink referenced to protective earth, and the secondary converter (consisting of DAB secondary bridge and the inverter cell) is placed on the heatsink referenced to the midpoint of DC link capacitor with the help of split capacitors as shown in 3D figure in appendix A. Thus, isolation is needed even between the secondary coil and the heatsink.

According to ANSI NETA ATS 2017 [36] standard, the isolation requirement for a grid-connected transformer is twice the single-phase peak voltage. Thus the necessary voltage requirement that can be deduced from the given standard is 16.3 kV. Hence, all the COMSOL models presented in this chapter are run for a potential of 16.3 kV.

Since PCB fabrication is a standardized procedure, the most ideal design would be to use the core material of PCB as the dielectric between the high voltage and low voltage windings. However, this poses two concerns. Firstly the di-electric breakdown of FR4 is limited to 12 kV/mm for the continuous field [37]. Hence, the need for a thick core arises thus limiting the voltage isolation to manufacturing capabilities of thick PCBs. Secondly, the clearance from the core also has to be kept in mind. Laterally, due to PCB manufacturing technique, the discharges are more dominant. Hence, an external insulation material becomes a necessity. In literature, PCBs with a core material having high breakdown strength, like polyimide (27 kV/mm) or high voltage polyimide film (110 kV/mm), is used [38]. This would solve the issue of isolation between the primary and secondary windings. But the isolation between the core and the winding is still a concern.

The most optimal design to be implemented for an MV isolation planar transformer with 18 turns in primary and secondary is implemented with separate boards for primary and secondary windings with a layer of epoxy coating of 3.3 mm thickness on the secondary terminal, which would act as the high insulation material because of its high breakdown strength.

However, just using epoxy coating would lead to unwanted partial discharges due to the following two reasons,

1. The commercially available ferrite cores used for PT applications have sharp corners. Thus, when the core is referred to ground potential, corona discharges occur.
2. Since there is a tiny layer of air always present between the epoxy-coated secondary layer and the core or epoxy-coated secondary layer and the primary layer, uneven field distribution occurs. Since the permittivity of air is around $1/4^th$ of that of epoxy, 4 times higher field is concentrated in those air gaps.

The test results of PD measurements in such a setup are shown in section 6.2.2. Partial discharges are observed at around 6-7 kV peak voltage. Thus the need to concentrate all the electric field in the high insulation material arises. This can be done in two ways: Potting of the entire transformer in the epoxy material or using a shielding layer on the epoxy that is referred to ground potential.

However, Potting the entire transformer in epoxy poses the following problems:

1. Heat dissipation: The heat generated due to copper and core losses in the transformer becomes difficult to be dissipated.
2. Possibility and detection of cracks: When the transformer is potted, there is a higher possibility of creating cracks due to the difference in the thermal expansion rate of the core, FR4 and the epoxy. To detect these defects, special equipment like X-ray machines are needed.

Considering the complexity involved in complete potting, the possibility of using a shielding layer (semiconductive shield) is explored further in the thesis.

5.1.2. Electrical Shielding

In the designed PT, two kinds of shields are provided. One is the semi-conductive shield that is a coating of semiconductive paint over the epoxy of the secondary winding and the other is the conductive shield present in both the windings as the outer layer copper and around the edge in each layer. Further details and responsibilities of both shields are discussed below:

Semi-conductive shield to control E-field

To contain the electric fields within the epoxy material, the outside surface of the epoxy coating of the secondary winding has to be connected to the ground potential (PE referred to the LV-DC grid). In order to do this, semiconductive paint is applied on the outer surface of the epoxy layer, as shown in figure 5.1 and is connected to the PE referred to the LV-DC grid. However, this coating cannot be applied till the end connectors as it would violate the clearance and creepage levels. Hence, the semiconductive layer is only applied till a certain area from where the clearance and creepage distance to the terminal connection has to be respected. This is pictorially shown in figure 5.1.

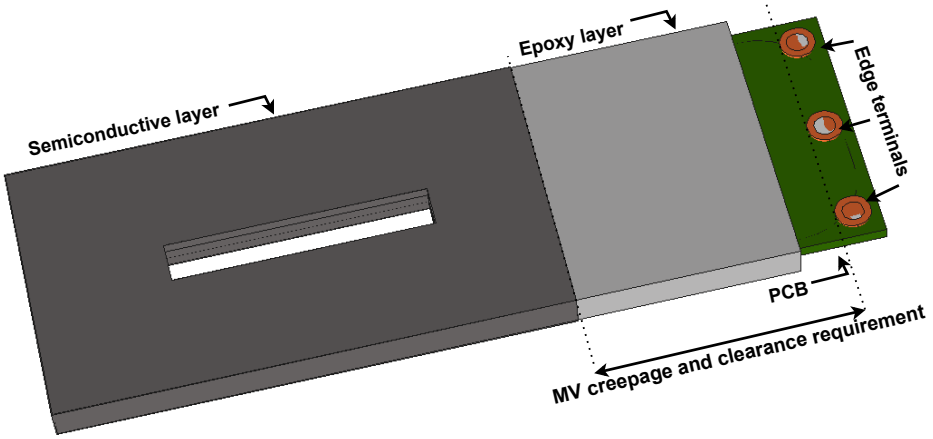


Figure 5.1: Model of the secondary winding (without termination) with semiconductive paint

Figure 5.2 shows the cut view of the secondary winding where all the COMSOL models are zoomed into. It shows the edge of the semiconductive layer where high field concentration takes place without proper terminal treatment.

Since the semiconductive layer is abruptly ended without any grading, just like in the case of HV cables, high fields are concentrated at the edge of the paint. The COMSOL simulations to show the high field concentration at the edge of the semiconductive paint are performed in the 2D domain. The results of the same are shown in figure 5.3. If left alone, these high fields cause a breakdown of air around the edge of the semiconductive layer.

In order to prevent the breakdown of air, terminal treatment is needed. As shown in figure 5.5, an epoxy coating of a certain thickness is given to contain high fields [39]. The thickness of the required amount of epoxy can be decided upon to limit the electric field in the air to a value less than 1.5 kV/mm. From COMSOL simulations, it is verified that epoxy with a thickness of 3.5 mm is needed to restrict the value to less than 1.5 kV/mm.

However, the above-mentioned method of termination leads to higher chances of partial dis-

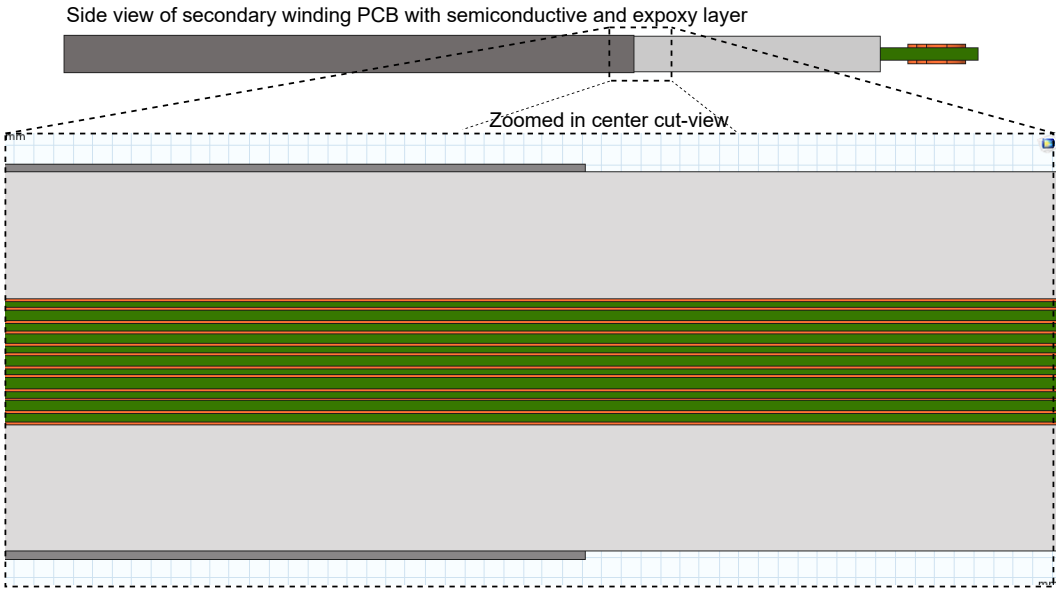


Figure 5.2: Cut view of the secondary winding

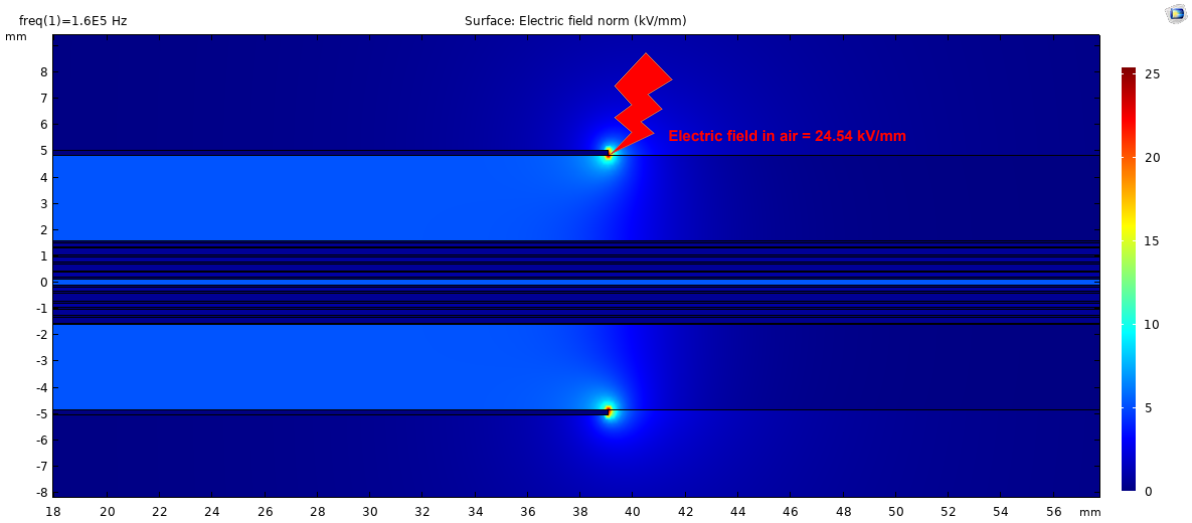


Figure 5.3: High electric field at the edge of semiconductive layer

charges due to high electric fields in the epoxy termination. Hence a new approach for the termination in planar transformer windings is done in this thesis. The technique of field grading is implemented at the edge just like in the case of high voltage cable terminations. The COMSOL results of the same are shown in figure 5.8. It can be observed that the electric field at the edge of the semiconductive shield with field grading is limited to 2 kV/mm.

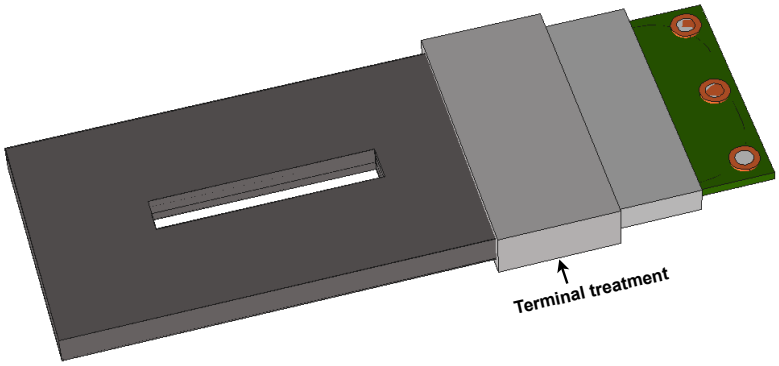


Figure 5.4: Terminal treatment to avoid breakdown of air around the semiconductive edge

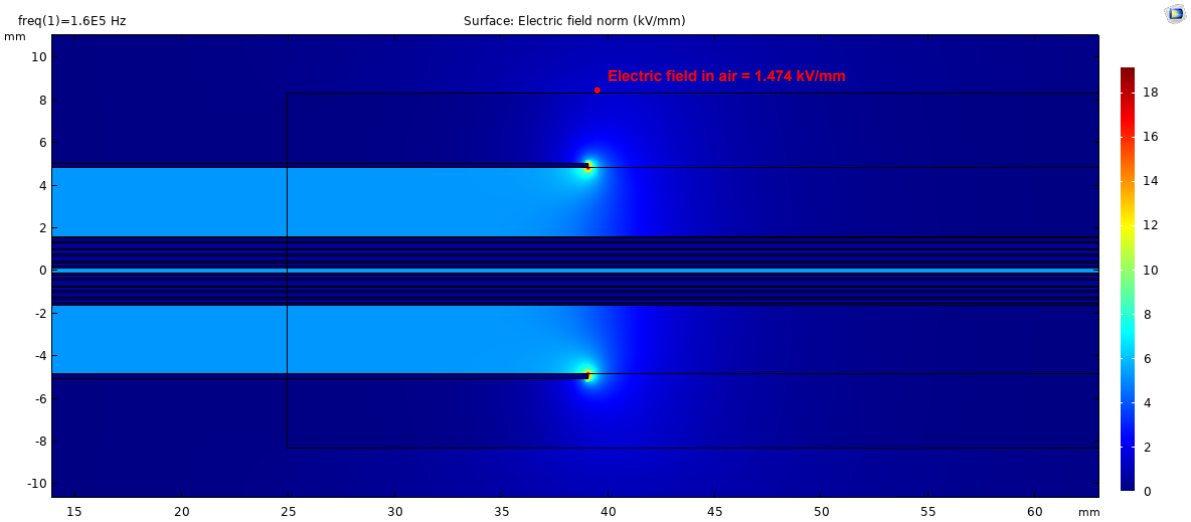


Figure 5.5: COMSOL simulation of secondary winding after terminal treatment

It has to be noted that the shape of the curvature surface is not optimal. The ideal curvature is similar to the stress cone in cable termination as shown in figure 5.6. However, a semi-circular structure is implemented in this thesis for the ease of 3D printing the required structure.

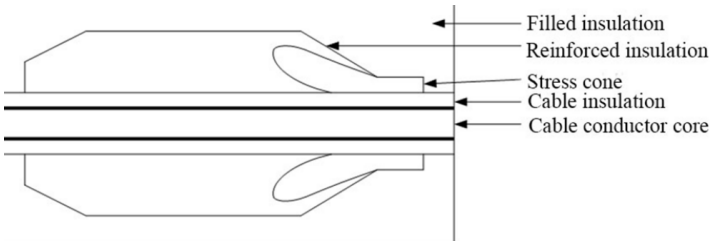


Figure 5.6: Ideal curvature for field grading

Conductive shield

Unlike the semi-conductive shield, the conductive shield is present within the PCB of both primary and secondary windings. This conductive shield is connected to the center point of

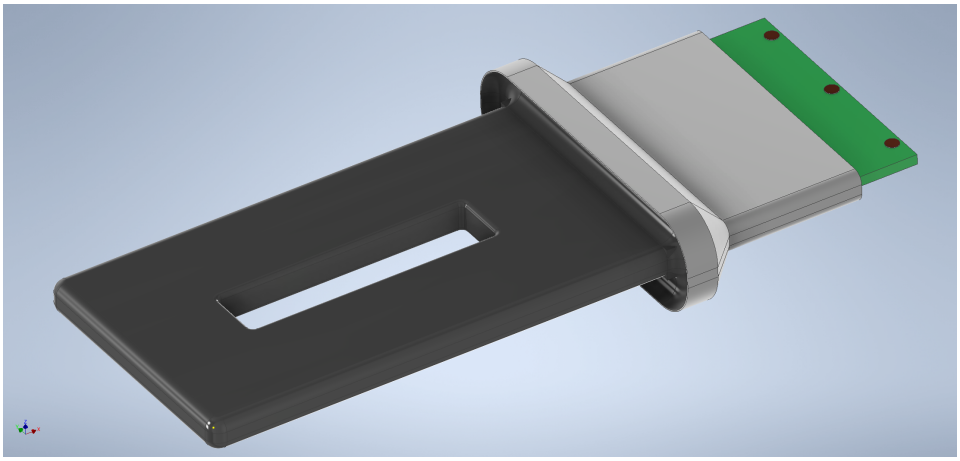


Figure 5.7: Field grading to avoid surface discharges due to breakdown of air around the semiconductive edge

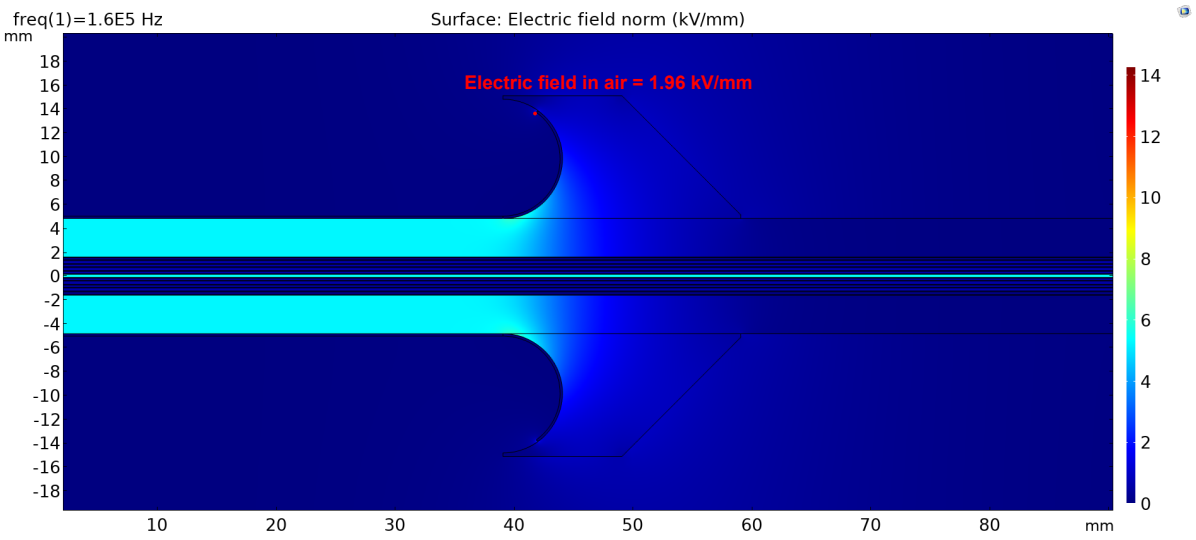


Figure 5.8: COMSOL simulation of secondary winding after field grading

the DC link capacitor voltage on the secondary side, and to the protective earth on the primary side. The copper fill on the outer layers is such that it covers the windings on the internal layer. Also, a slit is designed to avoid a complete turn on the top and bottom layers. This is done so that there are no short circuit currents due to voltage generated by flux linkage from other coils.

This shield is designed for different reasons on the primary and secondary windings. On the secondary windings, it is designed to have a stable extreme potential for the field lines. If the shield was not present, the potential on the outer-most winding of the transformer would fluctuate with the frequency of the DAB. In the case of primary windings, along with providing stable extreme potential surface, it serves another purpose. During a fault on the AC grid, when there is a breakdown of isolation, the fault currents flow from the secondary winding to the primary winding. But this shielding layer on the top layer of primary PCB pushes the currents to protective earth and thus protects the LV-DC grid.

This conductive shield is also provided in each layer to limit the high electric field on the outer-most shield. When the shield is not provided in the inner layers, the electric field distribution

at the inner layers is shown in figure 5.9.

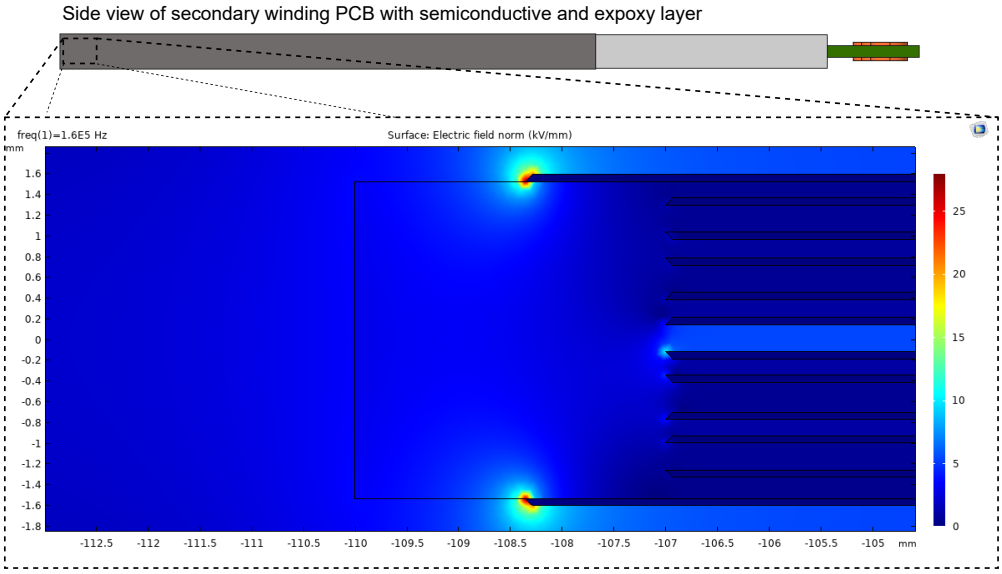


Figure 5.9: COMSOL simulation of electric field on the edge of the conductive shield

Hence, to improve the field distribution, a semi-circular pattern of shield lines is made on each layer. This ensures less stress on the outermost surface. The COMSOL simulation of the semi-circular pattern field lines is shown in figure 5.10.

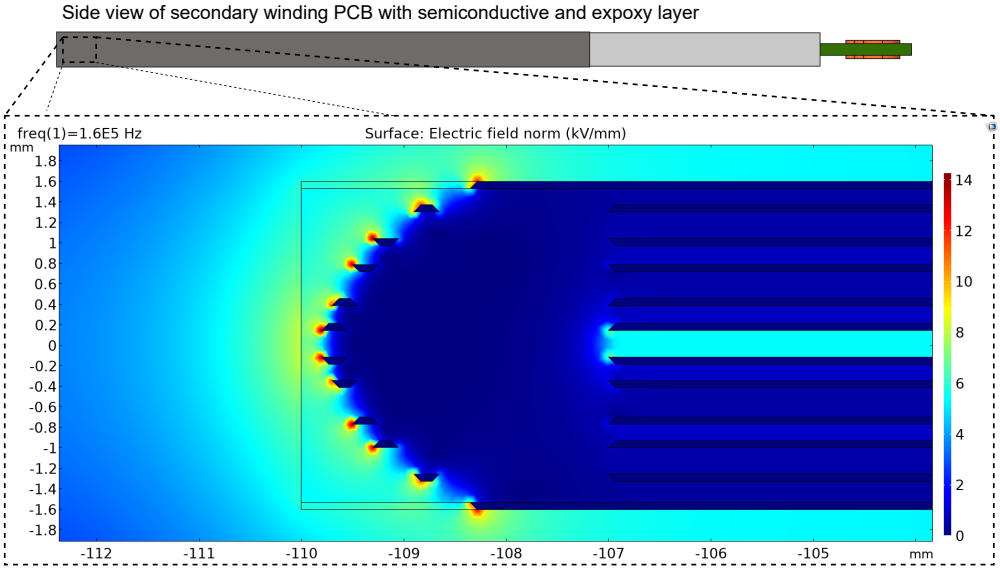


Figure 5.10: COMSOL simulation of the semi-circular pattern of shield lines to reduce the stress on the outermost shielding layer

5.1.3. Winding Format of the Transformer

As discussed in section 4.1.4, the final transformer is designed with 18 turns on primary and secondary. Two parallel EILP 102 cores are used as the core of the transformer. In both the windings, two turns per layer are implemented and buried vias and normal vias are used to

connect the windings of one layer to another layer. So a 12 layer PCB is used per winding. The schematics of each layer are given in appendix A.

There is no interleaving in this project. Having no interleaving in the DAB transformer has the following advantages:

- The insulation needed on the secondary can be easily provided.
- Parasitic capacitance is reduced.
- leakage inductance increases which is beneficial because it decreases the value of external series inductance.

In this thesis, a special type of winding format is implemented to reduce the impact of parasitics. In this new winding technique, the terminals of the transformer are wound as shown in figure 5.11. The windings start in the 5th inner layer go up to the inner layer 1 and then through a via, go down till inner layer 10 and then finally terminate on inner layer 6.

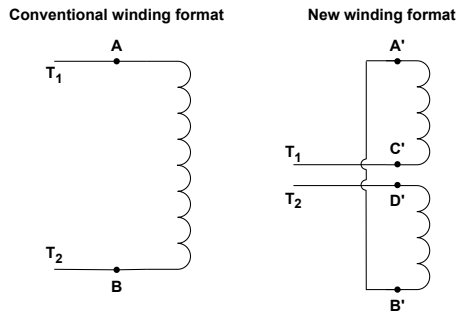


Figure 5.11: Winding format

When the conventional winding arrangement is used, the voltage at points A and B, shown in figure 5.11, are fluctuating between +700 V and -700 V with respect to the neutral connection. This constant change in voltage causes currents in the parasitic capacitances between points A and B and the shield on the outer layers. By designing the windings in the new format, the voltages at A' and B' will be at a potential close to neutral connection and hence the voltage fluctuation will not be high due to which the parasitic losses will be low. However, the effect of parasitics at points C' and D' could be high which is avoided by avoiding the overlapping area of windings in layers 5 and 6. This low overlap is shown in figure 5.12.

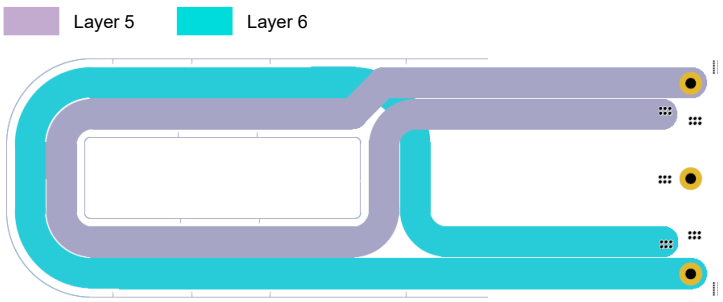


Figure 5.12: Layout of layers 5 and 6 to show the least area of cross-section

5.1.4. Leakage Inductance Estimation of the Planar Transformer

The series inductance in the DAB is the energy-transferring element and thus has a high role in determining the maximum power transfer that is possible. If the actual series inductance in the circuit is less than the calculated and desired value, the maximum power transfer happens at a lower phase shift angle. Which indirectly decreases the ZVS range. And in the other case, when the actual inductance is higher, the power transferred is lower than the desired value. Thus, having a defined series inductance in the circuit is important.

The leakage inductance of the transformer adds to the external series-connected inductor to act as the total series inductor. Hence, evaluating the leakage inductance of the transformer becomes necessary. As mentioned earlier, the theoretical evaluation of leakage inductance of the planar transformer is simple. Furthermore, since there is no interleaving, the estimation is further simplified.

In this section, the leakage inductance of the designed planar transformer is estimated using the evaluation of energy stored in the magnetic field as presented in [40]. This analysis is based on the following assumptions:

- The transformer design is symmetrical
- The Magneto-motive force (MMF) varies linearly in the winding layer. Practically, at higher frequencies, due to skin and proximity effects, the currents and hence MMF is more concentrated at the edge of the conductor. However, this is a valid assumption because the conductor thickness is low compared to the skin depth.
- The reluctance of the path within the magnetic core is ignored (air gap is ignored) compared to the path in the winding.
- The field strength (H) is constant along the plane of the layer.

$$E = \frac{1}{2} \int BH dv = \frac{1}{2} L_{lk} I_p^2 \tag{5.1}$$

The differential volume of each turn = $l_w b_w dx$. Therefore, energy is the sum of energy stored in each elementary area:

$$E = \frac{\mu_o}{2} \sum \int_0^h H^2 l_w b_w dx \tag{5.2}$$

where l_w is the length of each turn and b_w is the total width of turn in one layer.

The MMF distribution is shown in figure 5.13.

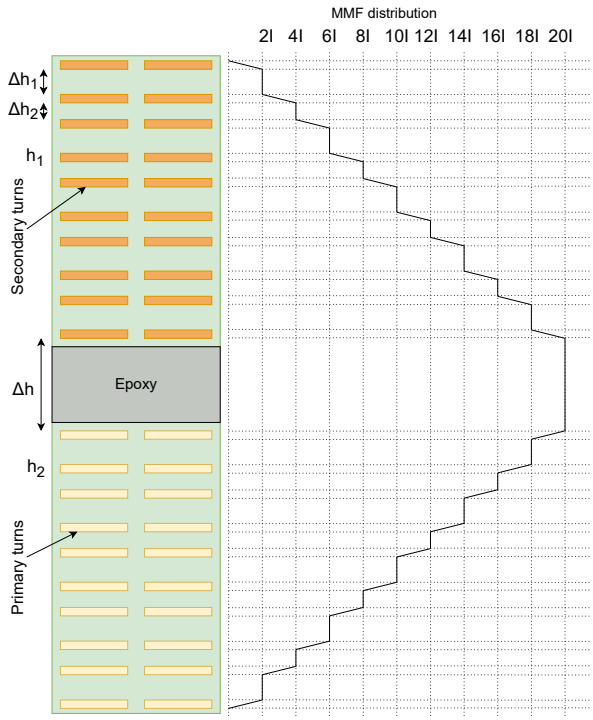


Figure 5.13: Analytical MMF distribution in the transformer windings

$$E = \frac{\mu_o l_w b_w}{2}\left\{10\int_0^{h1}\left(\frac{2I_1 x}{b_w h_1}\right)^2 dx + 10\int_0^{h2}\left(\frac{2I_1 x}{b_w h_2}\right)^2 dx + \left(\frac{2I_1}{b_w}\right)^2(\Delta h_1) + \left(\frac{4I_1}{b_w}\right)^2(\Delta h_2) + \left(\frac{6I_1}{b_w}\right)^2(\Delta h_1) + \left(\frac{8I_1}{b_w}\right)^2(\Delta h_2) + \left(\frac{10I_1}{b_w}\right)^2(\Delta h_1) + \left(\frac{12I_1}{b_w}\right)^2(\Delta h_2) + \left(\frac{14I_1}{b_w}\right)^2(\Delta h_1) + \left(\frac{16I_1}{b_w}\right)^2(\Delta h_2) + \left(\frac{18I_1}{b_w}\right)^2(\Delta h_1) + \left(\frac{20I_1}{b_w}\right)^2(\Delta h)\right\} \tag{5.3}$$

$$E = \frac{I_1^2 \mu_o l_w b_w}{2b_w^2}\left[\frac{40}{3}h_1 + \frac{40}{3}h_2 + \Delta h_1(336) + \Delta h_2(480) + \Delta h(400)\right] \tag{5.4}$$

$$L_{lk} = \frac{\mu_o l_w}{b_w}\left[\frac{40}{3}(h_1 + h_2) + 336\Delta h_1 + 480\Delta h_2 + 400\Delta h\right] \tag{5.5}$$

Considering l_w = 280 mm, b_w = 19 mm, $h_1 = h_2$ = 0.07 mm, Δh_1 = 0.26 mm, Δh_2 = 0.171 mm and Δh = 3.76 mm, L_{lk} is claculated to be 31 μH. This value is further compared to the actual leakage inductance value in section 6.2.1

5.2. Planar Inductor

The energy storing element in DAB converter is the series connected inductor. Since the leakage inductance of the transformer is not enough for the rated power of the DAB, an additional external inductor has to be added. The design of this inductor is fairly complicated due to the voltage and current levels of the converter. Commercially available inductors are available for lower voltage and current ratings. Hence, a wire wound toroidal or planar inductor has to be designed for this application.

The comparison of conventional wire wound inductors and planar inductors are compared for the feasibility study of planar magnetics. The cores chosen for comparison are ferrite toroidal cores and a comparable iron toroidal core for conventional winding and ELP ferrite cores for planar inductors. Based on minimum area product requirement, 3 toroidal ferrite cores are chosen from TDK - R34x20.5x12.5 (Smallest available core), R68x48x13 (best toroidal core with respect to loss/volume ratio) and R140x163x25 (Biggest available core). An iron core of comparable size (compared to the best toroidal core) is chosen - KAM 290 060A. From the planar cores, the ones which have minimum window width to fit atleast one turn of the track (considering 70 μm copper) are chosen from TDK- EILP 43, EILP 58, EILP 64. All the ferrite cores of the same material are chosen (N87 material) as all of them are available in this material type and hence make a fair comparison. The results of the comparison are shown in table 5.1.

Table 5.1: Feasibility study results of planar inductors

	Ferrite toroidal			**Iron toroidal**	**Planar**		
	R34x20.5x12.5	**R68x48x13**	**R140x103x25**	**KAM 290 060A**	**EILP 43**	**EILP 58**	**EILP 64**
Final inductance (μH)	73.21	70.45	73.875	73.5	74.4	71.6	76.23
Number of turns	78	17	12	19	24	18	11
Air gap (mm)	20	2.2	1.4	NA	2.8	2.2	1.2
Volume (mm^3)	5423	46530	172440	92635	11430	21000	36200
Power loss (W)	4.3	36.415	131.34	127.58	9.38	14.16	27.2
Temperature rise (^{o}C)	64.96	117.664	145.69	227.5	80.7	68.22	85.7
B_{eff} (T)	0.2	0.2	0.2	1.174	0.2	0.2	0.2

It can be seen that the temperature rise and the losses in conventional inductors are high. Since the temperatures are higher than 60^{o}C - 70^{o}C, they are not feasible designs. However, in the case of planar inductors, though the temperature rise is higher than 60^{o}C - 70^{o}C, the core of the inductor can be cooled by placing it on the heatsink. Also, using a planar inductor is more efficient as the losses are low.

5.3. Summary

In this chapter, the design of PT with 18 turns which is rated to withstand 16.3 kV isolation is discussed. Also, the concept of shielding in the designed PT is discussed. Further in the chapter, a different winding format is discussed to reduce the EMI between the shield layer and the windings of the secondary coil. Thereafter, the analytical method to estimate leakage inductance of the PT is elaborated with all the assumptions. Finally, in the planar inductor section, the comparison of conventional wire-wound inductors and planar inductors is done to evaluate the effectiveness of the planar magnetics.

6

Hardware implementation and Results

6.1. Secondary Winding Epoxy Casting

The procedure for epoxy casting involves various stages starting from mold making to epoxy curing. Each stage is explained in detail below:

- **3D printing**: The 3D printing of the geometry is done with PLA material plastic. This model will be the mold for the silicon rubber cast. Figure 6.1 represents the 3D models prepared for making silicon rubber mold.

Figure 6.1: 3D model for silicon rubber casting

- **Silicon rubber casting**: The silicon rubber can be cured at room temperature in about 3-4 hours. Figure 6.2 shows the silicon rubber before and after casting respectively. Finally, the mold for epoxy is ready.

((a)) Silicon rubber casting **((b))** Final silicon mold

Figure 6.2: Silicon rubber mold procedure

- **Preheating of epoxy resin and hardner**: Preheating at 60^{o}C of both CY225 (High-temperature epoxy resin) and HY225 (hardner) decreases the viscosity of both liquids to ensure a uniform mixture.
- **Degassing of individual substances**: Both the epoxy resin and harder can be initially degassed at 60^{o}C till there are no bubbles in the mixtures.
- **Degassing of mixed substance**: Both substances can now be mixed constantly for about 30 minutes to ensure uniform consistency and colour. After doing so, the mixture can be degassed in the vacuum chamber again at 60^{o}C for about an hour to ensure no bubbles.
- **Epoxy fill in the mold and degassing**: Now the epoxy mixture can be filled into the silicon mold in which the PCB is placed. Once again, the entire setup can be placed in the vacuum chamber and degassed till there are no air bubbles.
- **Epoxy curing**: The setup can now be transferred into an oven and it can be heated up to 140^{o}C and maintained there for about 8 hours. Thereafter, the temperature can be lowered in the steps of 10^{o}C every 30 minutes to avoid cracks due to unequal thermal expansion coefficients.

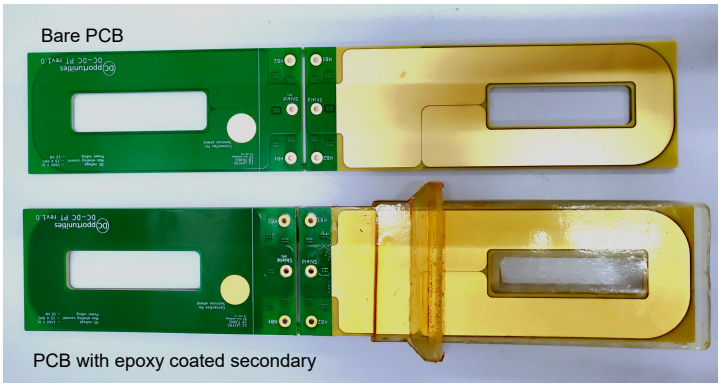


Figure 6.3: Final epoxy cast of secondary winding

6.2. Transformer Tests

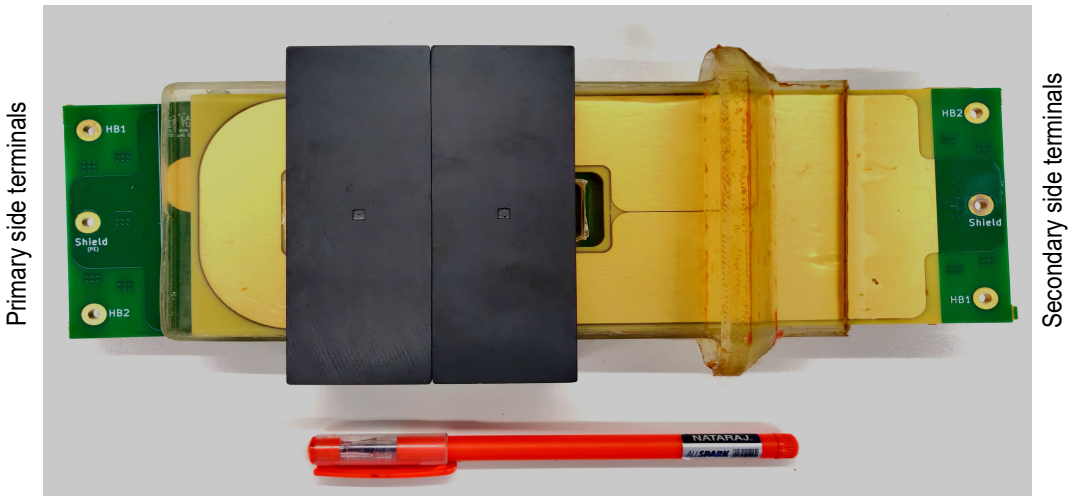


Figure 6.4: Planar transformer hardware model

6.2.1. Leakage Inductance Measurement

In section 5.1.4, the leakage inductance of the transformer was analytically estimated. Once the transformer is built, the leakage inductance measurement is done using Bode 100 to check the accuracy of the analytical calculation. The values of R_{dc}, L_1 and Gain can be measured using bode 100 and the leakage and magnetizing inductance can further be calculated using the equations (6.1) and (6.2). The results of the same are given in table 6.1.

Table 6.1: Results of Bode 100 analyzer

$\mathbf{R}_{dc}$	$\mathbf{L}_1$	**Gain**	$\mathbf{L}_m$	$\mathbf{L}_{lk}$ **(actual)**	$\mathbf{L}_{lk}$ **(analytical)**
0.184 Ω	5.9 mH	0.3735	5.89616 mH	38.4 μH	31 μH

The measured magnetizing inductance is much higher compared to the analytical value due to the lower air gap. In the analysis, an airgap of 0.1 mm was considered and the corresponding magnetizing inductance was obtained to be 2.6 mH.

$$L_m = \frac{Gain * n}{2\pi f}\sqrt{(R_{dc})^2 + (2\pi f L_1)^2} \tag{6.1}$$

$$L_{lk} = L_1 - L_m \tag{6.2}$$

It can be observed that the actual reading is slightly different from that of the analytical value. This is mainly due to close approximations of distances made in section 5.1.4. Also, the measured magnetizing inductance is higher compared to the analytical value due to the lower air gap. In the analysis, an air gap of 0.1 mm was considered and the corresponding magnetizing inductance was obtained to be 2.6 mH.

6.2.2. Straight-Detection Type Partial Discharge Test

In this section, the findings of partial discharge tests are presented which were done to check the feasibility of having bare PCB or only epoxy coating without a semiconductive shield. Table 6.2

Table 6.2: Environmental conditions during PD testing

Lab temperature	Lab pressure
21^{o}C	1022 hPa

The test setup is shown in figure 6.6 which consists of the test sample, high voltage electrode, coupling capacitor, test object, capacitor divider and optical fiber cable to communicate the partial discharge measurements onto the screen.

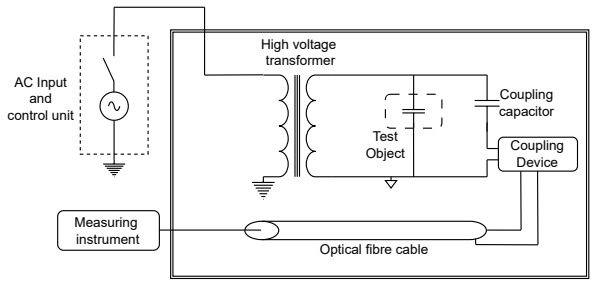


Figure 6.5: Block diagram of straight-detection type partial discharge test setup

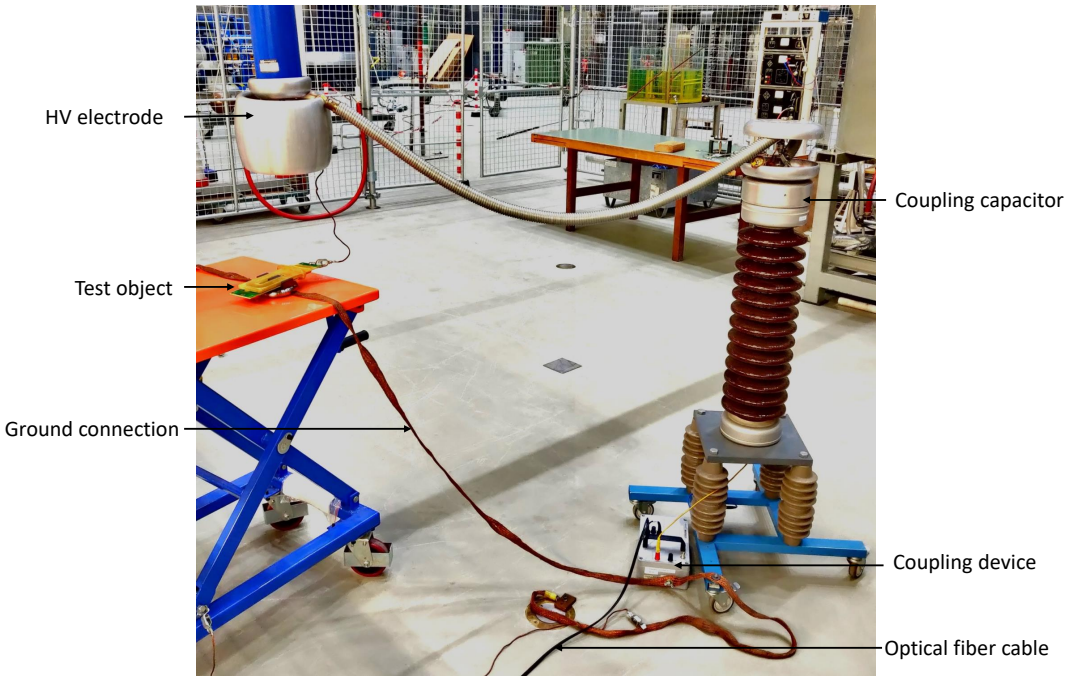
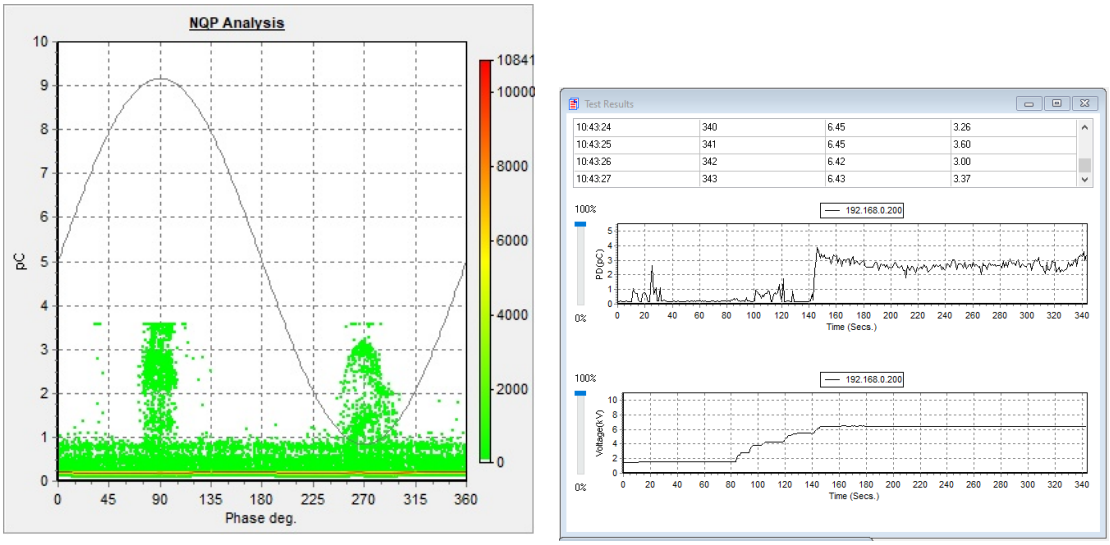


Figure 6.6: Straight-detection type partial discharge test setup

Initial tests were conducted by just placing the secondary PCB in the core by creating a 3.5 mm gap between them by placing a non-conductive material. The results of the tests are shown in figure 6.7.



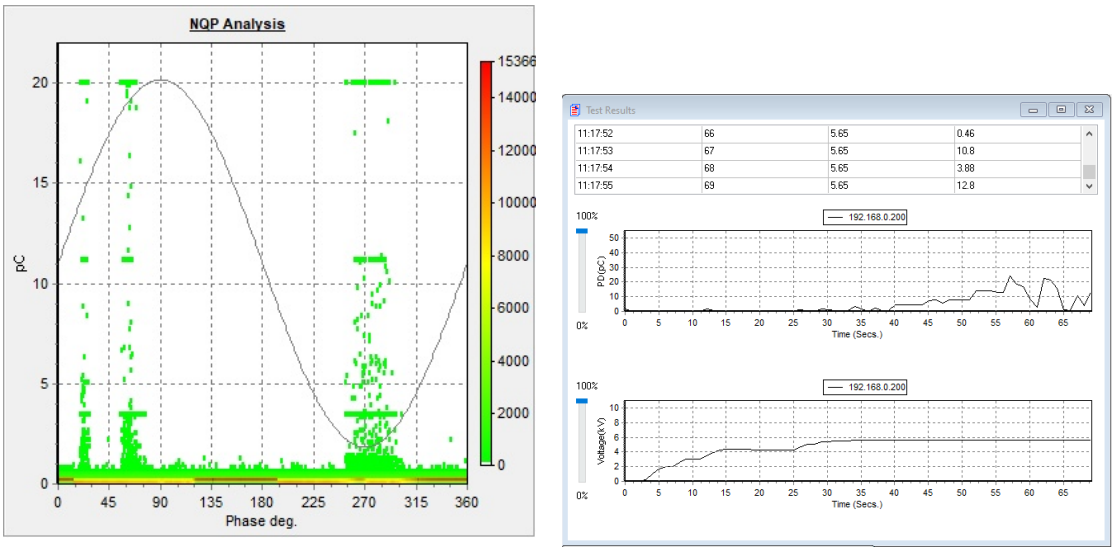
((a)) NQP pattern from DDX9121b software run for 120 sec

((b)) Partial discharge and voltage graphs

Figure 6.7: Bare PCB partial discharge test results

The peak inception voltage of 6.5 kV caused partial discharges over 4 pC.

Next, the PCB with the epoxy coating is placed in the core. The voltage is applied between the winding on the PCB and the core, where the core The results of the same are shown in figure 6.8. The peak inception voltage of 5.5 kV caused partial discharges over 4 pC. Also after a



((a)) NQP pattern from DDX9121b software run for 120 sec

((b)) Partial discharge and voltage graphs

Figure 6.8: Epoxy coated PCB partial discharge test results

prolonged time, the partial discharges increased to higher values.

The cause of partial discharges at lower voltages can be due to corona or high field concentration in air gaps between epoxy and the core. As mentioned in section 5.1.2, the fields need to be concentrated in the epoxy material for which a semiconductive layer coated on the epoxy seems to be a promising solution.

6.3. Hardware Converter Design and Testing

In this section, the hardware design of the DAB converter is discussed in detail. The primary board is designed and developed using KiCAD. It consists of the input terminals which are connected to the LV-DC grid, an input EMI filter consisting of a 3-phase choke, x-caps and y-caps, a power board (consisting of switches and the isolated gate drivers) interface, terminations for inductor and transformer connections, STM32G4 micro-controller to enable high-frequency switching signals to the switches, measuring DC grid voltage, fan control signals for active cooling, and communication of wifi module and master controller and additional auxiliary low voltage circuitry. The physical model of this board is shown in figure 6.9.

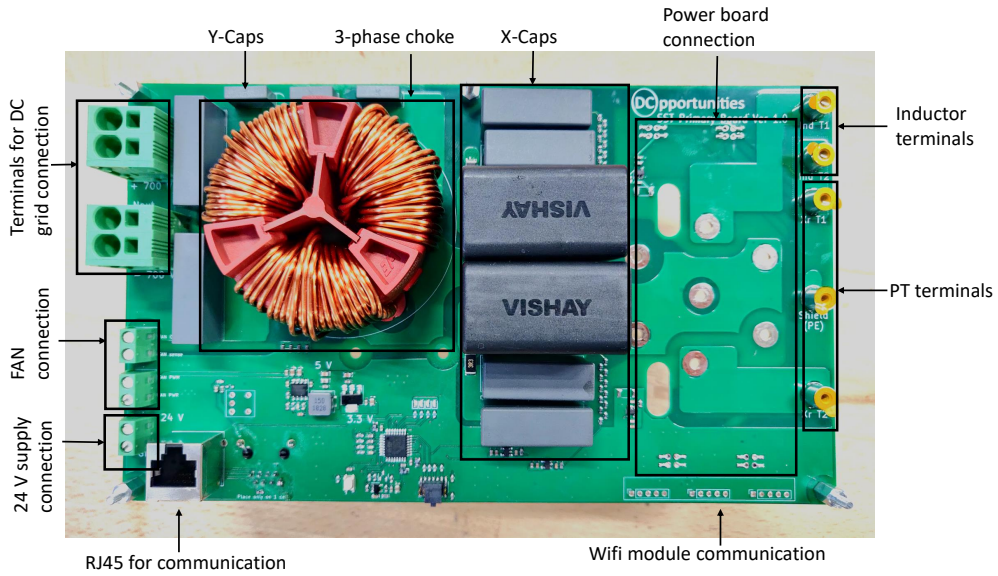


Figure 6.9: Primary board hardware

The planar transformer board is designed with primary and secondary boards split with mouse bites. This is shown in figure 6.10.

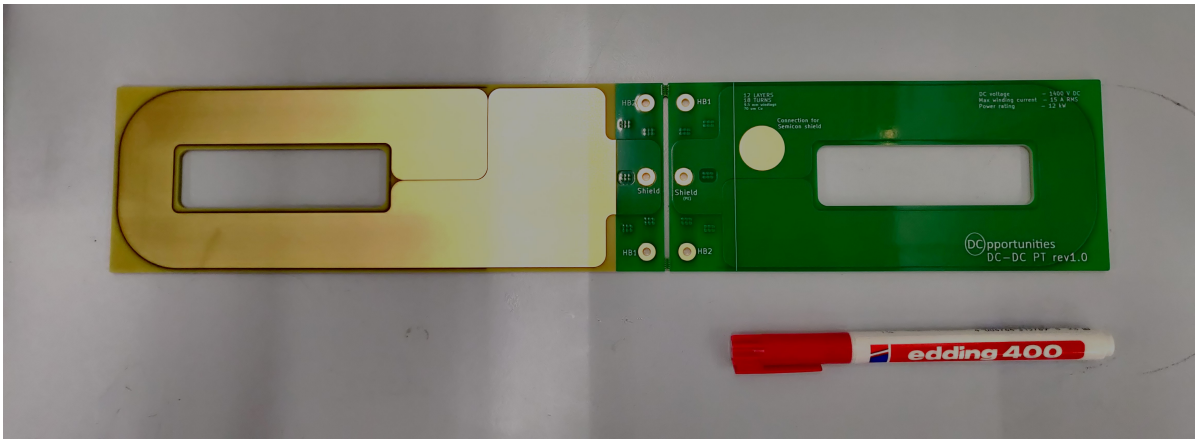


Figure 6.10: Tranformer PCB hardware

6.3.1. Open-loop tests of DAB

The developed hardware is first tested for auxiliary supply and then the working of the controller on both primary and secondary boards. Using SPI communication, synchronization between the controllers on the primary and secondary boards is established where the secondary controller is selected to perform the role of the master controller. Figure 6.11 shows the experimental setup to test the developed hardware of the converter. An external inductor of 10 μH is added on the primary side.

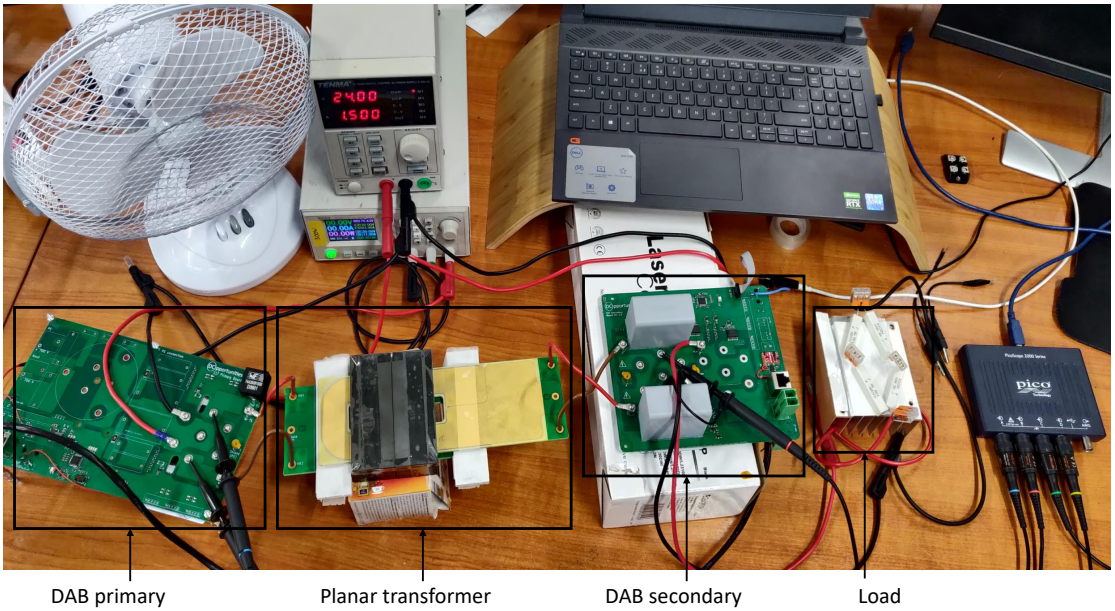


Figure 6.11: Test setup to test the functionality of DAB

Once the synchronization is established, a constant phase shift is given between the gate pulses of the primary and secondary full bridges. First, the test is performed for the low phase shift, and later is carried out for the higher phase shift. The phase shift measurements are shown in figures 6.12 and 6.13 and the corresponding DC output voltages are shown in figures 6.14 and 6.15, respectively.

$$f_s = 160kHz \Rightarrow T_{sw} = 6.25\mu s \tag{6.3}$$

$$\phi = 0.5\frac{\Delta t}{T_{sw}/4} = 0.32 * \Delta t * 10^6 \tag{6.4}$$

where Δt is the time difference of the gate pulses between primary and secondary side full bridges. The same time difference is also seen between the primary and secondary transformer voltages.

Using equation 6.4, the actual phase shift between the full bridges is calculated after measuring the time difference in figures 6.12 and 6.13 and are found to be 0.1238 and 0.33 respectively.

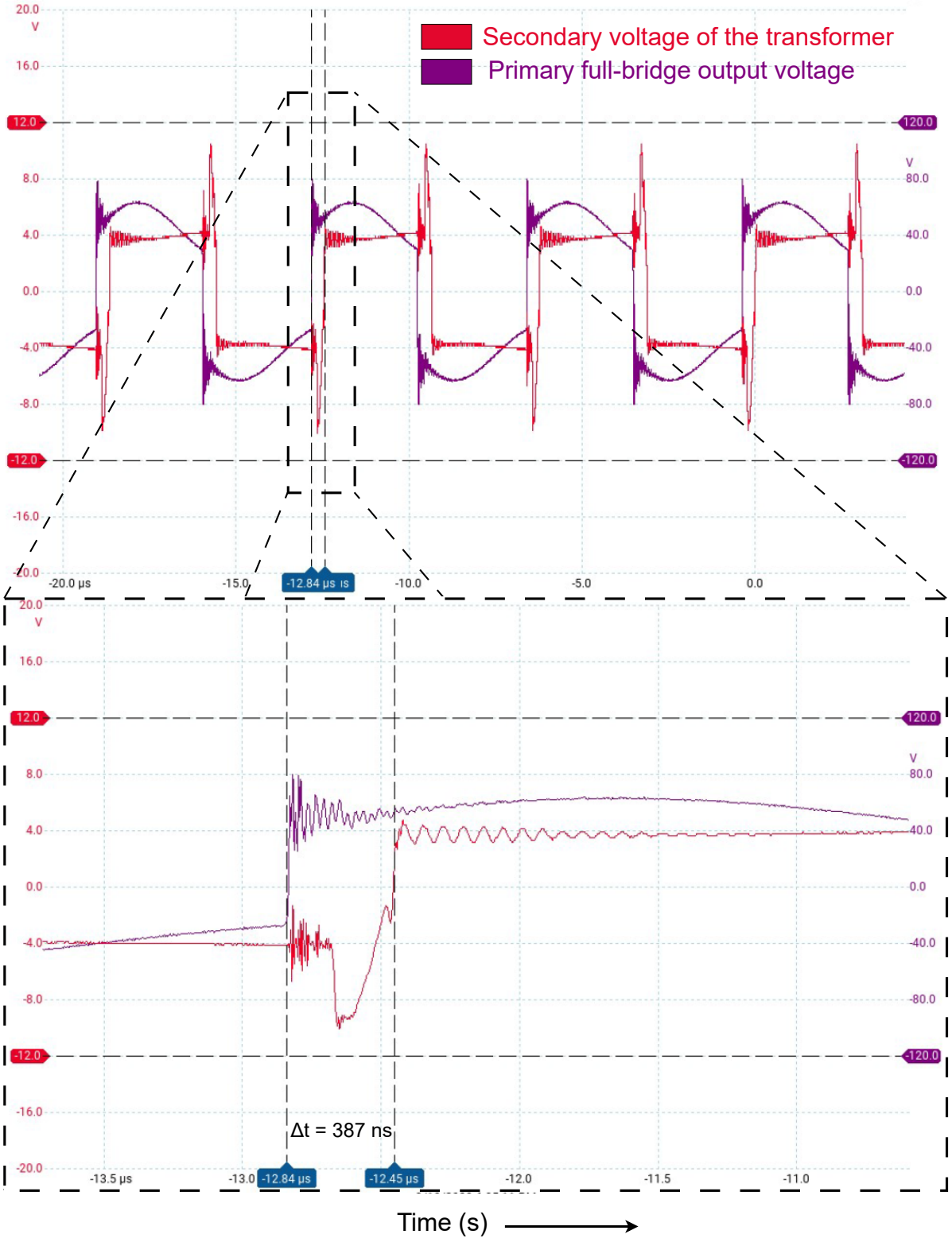


Figure 6.12: Waveforms showing a low phase shift of 1.042 μs ($\phi = 0.1238$)

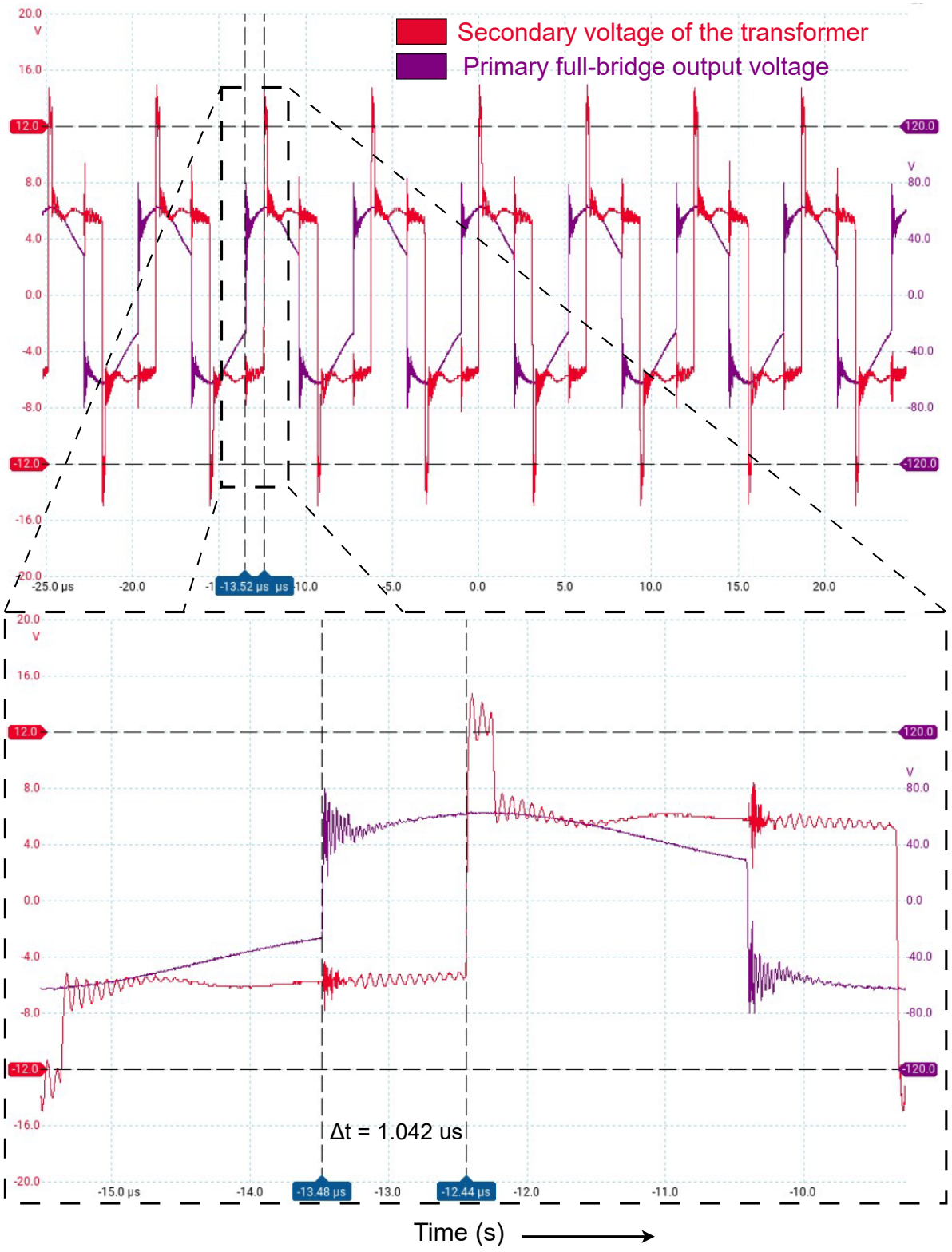


Figure 6.13: Waveforms showing a low phase shift of 387 ns ($\phi = 0.33$)

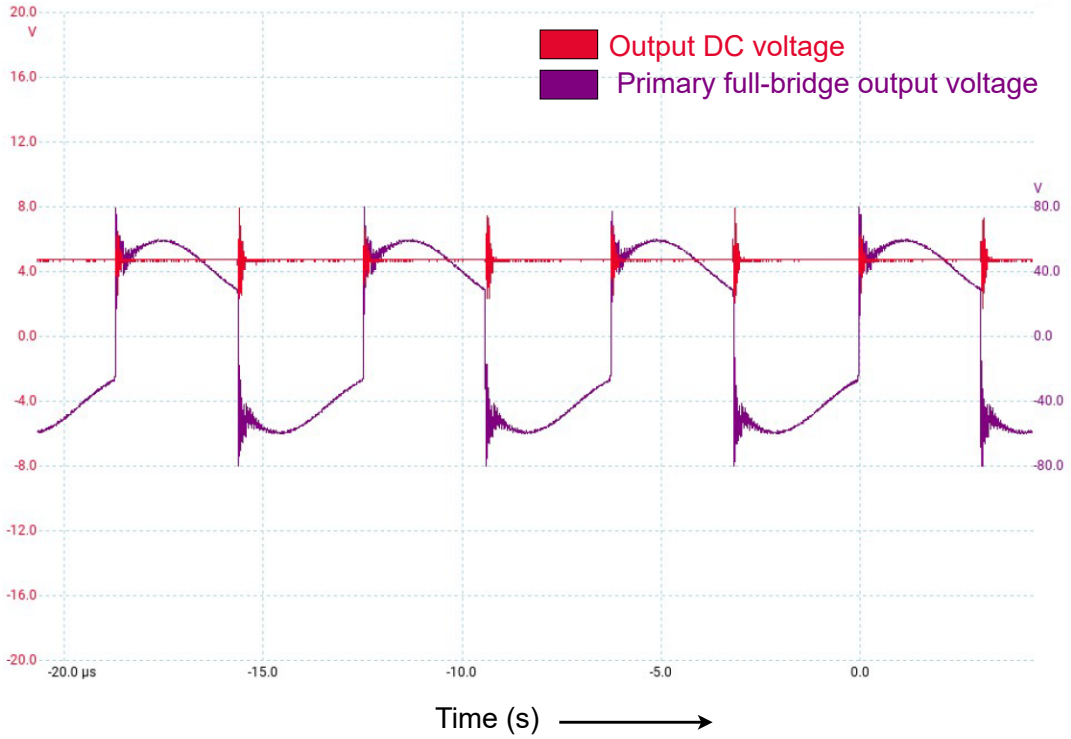


Figure 6.14: DC output voltage waveform of the DAB for low phase shift of 0.1238

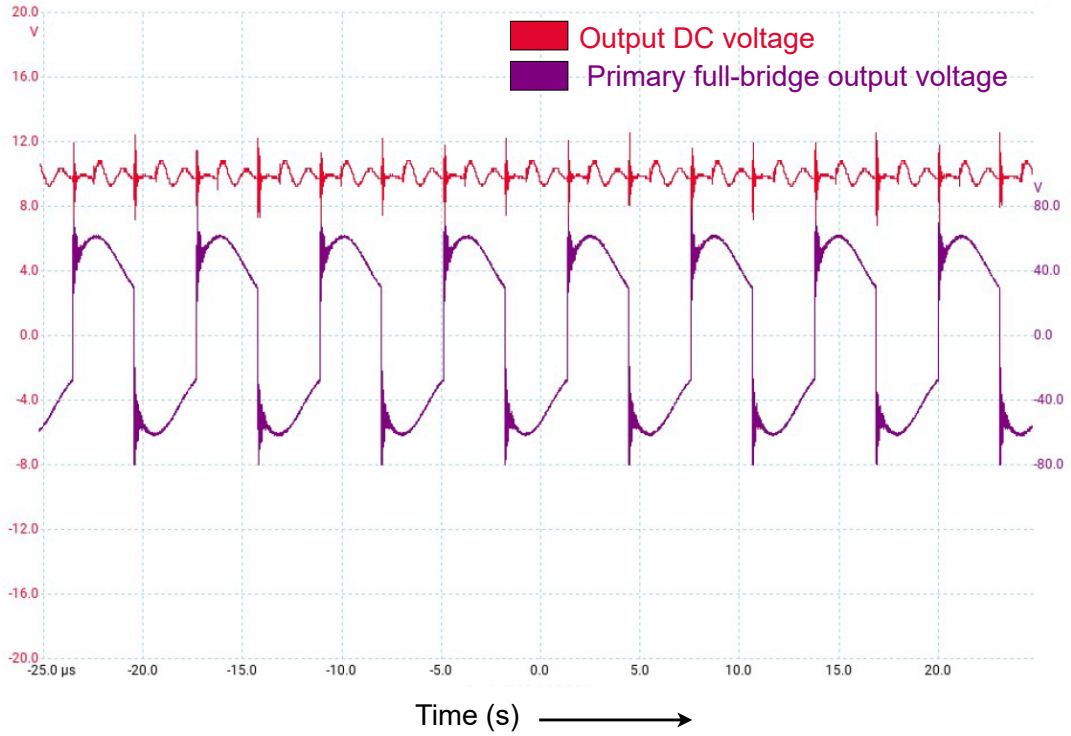


Figure 6.15: DC output voltage waveform of the DAB for high phase shift of 0.33

Considering equation 3.1, and replacing P by V_{sec}^2/R_{load}, the DAB power transfer equation can be rewritten as given in equation 6.5.

$$\frac{V_{sec}^2}{R_{load}} = \frac{nV_{pri}V_{sec}\phi(1-\phi)}{2f_sL_s} \tag{6.5}$$

rearranging the terms,

$$V_{sec} = \frac{nV_{pri}R_{load}\phi(1-\phi)}{2f_sL_s} \tag{6.6}$$

Since all the parameters except V_{sec} and ϕ are constant, equation 6.6 can be re-written as given in equation 6.7

$$V_{sec} = C\phi(1-\phi); \quad C = \frac{nV_{pri}R_{load}}{2f_sL_s} \tag{6.7}$$

Referring to figures 6.12 and 6.14, When ϕ = 0.1238, V_{sec} = 5 V, C from equation 6.7 turns out to be 46.1 V.

Now when the phase shift changes to 0.33 as shown in 6.13, the new secondary DC voltage V_{sec} can be calculated by substituting C = 46.1 V and ϕ = 0.33 in equation 6.7. Upon doing so, V_{sec} = 10.2 V. The same can be verified in figure 6.15.

Thus in general, it can be observed that with the increase in phase shift, the output voltage increases. However, this is till ϕ = 0.5, beyond which the output voltage drops as the phase shift is increased.

6.4. Summary

In this chapter, the procedure for epoxy casting is explained in detail. Further, the transformer leakage inductance has been accurately measured with Bode 100 and partial discharge tests are carried out to find the inception voltage of the designed transformer using straight-detection type partial discharge tests. Thereafter, the hardware developed for the converter is explained. Finally, the tests conducted to verify the working of the converter is explained and the results of the same are discussed.

7

Conclusion and Further Developments

Solid-state transformers can be key contributors to integrating the upcoming and existing DC-MGs to the established AC grids. The connection between the DC-MGs and the AC network improves the reliability and eliminates the need for large ESSes. This thesis focuses on the design and development of an isolated bidirectional DC-DC converter that could potentially be employed in modular SST that connects LV-DC grid to MV-AC grid. This chapter provides final conclusion and discussion points from the thesis is presented which answers the research questions presented at the beginning of the thesis and some points that can be further improved are presented which can be further researched and explored.

- **Chapter 1** - This chapter gave an introduction to the project and its background information. The motivation for this research topic was also discussed here. Finally, the research questions are formulated and stated.
- **Chapter 2** - This chapter dealt with various DC-DC converter topologies. A comparison was done among various isolated bidirectional DC-DC converter topologies to select the most optimal one for SST application. Among all, CLLC and DAB were selected for further comparison. Due to the simple control that can be implemented and the less sensitivity to circuit parameters, DAB was selected. Further comparison was made between 1-phase DAB and 3-phase DAB. Due to the complexity involved in transformer design and the economic feasibility, 3-phase DAB was eliminated. Finally, 1-phase DAFB was selected as the final topology to be implemented in this thesis. Further in this chapter, the basic principle of operation of DAB was discussed and finally, the system-level representation of SST was shown.
- **Chapter 3** - Control of DAB was discussed in this chapter. First various types of controls were discussed and out of all, SPS was selected for implementation in the thesis. The phase shift control is done on the secondary side and the primary switches operate with a fixed duty cycle. Hence the only signal that needs to be transferred from the system controller to the primary side controller in the case of SPS is the enable/disable function key (which needs to be synchronized). This ensures the least data transfer between the

isolation barrier. Later in the chapter, ZVS considering magnetizing inductance was discussed in detail. Thereafter, feed-forward control and the droop control limits were also discussed along with their PLECS simulation results. Finally, the system level control of SST was performed in PLECS, and the results of which were analyzed.

- **Chapter 4** - This chapter dealt with the DAB design and parameter selection. The DAB with PT script, which was developed as a part of the thesis, was explained in this chapter. The focus was on the script objectives, constraints and the results. The number of turns of the transformer (18), the operating frequency of the converter (160 kHz), and various other parameters were identified based on the script results. Further in this chapter, the power rating of single cell DAB (12 kW) and the DC-link capacitor ratings (500 μF) were finalized. Finally, the input EMI filter design was discussed in this chapter.
- **Chapter 5** - This chapter discussed the design and effectiveness of planar magnetics in the project. The first part of the chapter covered the design aspects of PT where the purpose of various shields was discussed. Thereafter, the termination of the semiconductive shield was discussed and field grading using bushing was finalized as the best-suited method. Finally, the analytical method of estimating the leakage inductance of the PT was elaborated and the leakage inductance was estimated to be 31 μH In the next section, the effectiveness of planar magnetics was analyzed by comparing conventional wire-wound inductor to the planar inductor which proved to show more efficiency and better thermal properties.
- **Chapter 6** - This chapter discussed the way to have an epoxy coating of a certain thickness on the PCB. The steps involved to cure the epoxy of required dimensions were discussed. Partial discharge tests were conducted on the secondary winding with and without epoxy coating. A lower inception voltage was observed in the test conducted with epoxy coating. This can be attributed to the fact that the air gap between the epoxy and core had more field concentration due to the difference in electric permittivities proving that concentrating the fields inside the epoxy is essential. Further, the leakage inductance measured was found to be 38.4 μH which was slightly higher than the analytical value of 31 μH. Thereafter, the hardware developed for the prototype version is explained. Finally, the developed DAB converter was tested with fixed phase shifts of 0.1238 and 0.33 in which the output DC voltage was observed to be 5 V and 10.2 V, respectively.

7.1. Research Questions

The research questions stated in section 1.3 are answered in this thesis. The answers corresponding to the research questions are answered as follows:

1. **What is the most feasible DC-DC converter topology that can be implemented to develop a modular MV SST?**

   Various isolated bi-directional DC-DC converters are available in the literature. Out of all, single phase dual active full bridge converter qualifies to be the most feasible converter for modular MV SST application. This is because DAB can be designed for high power levels, it has inherent bidirectional quality, ZVS is possible for all the switches in

a good range of operation and a simple control technique (SPS) can be implemented with a slight compromise on efficiency. Also, it is not very sensitive to converter parameters as in the case of the CLLC converter hence making it easy to manufacture for modular purposes.

2. **What is the most simple yet effective method of controlling this converter on a module and system level and its implementation?**

   On a system level, the DC-DC converter is designed to control the DC-link voltage and match it to the DC grid voltage and maintain a 1:1 voltage ratio during both directions of power flow. The inverter controls the current flow and also adjusts the modulation for the grid connection. The single phase shift method proved to be the most simple yet effective control method to control the DC-link voltage of the DAB converter. Though this method results in higher RMS currents and hence higher losses, it qualifies as the better solution compared to other advanced control strategies due to the fact that there is only 1 control variable and the phase shift control can be implemented on the secondary side full bridge while the primary side full bridge operates with a constant duty cycle of 0.5. This ensures minimum data transfer between the primary and secondary sides, thereby minimizing the requirement for additional optoisolators.

3. **How to optimally select the parameters of the finalized topology with planar magnetics integration and what are the constraints involved?**

   It is observed that, once the power rating of the converter is fixed, all the major parameters of DAB with PT design depend on the number of turns of the PT, the operating frequency, and core material and dimensions. Hence an optimization script can be developed with various core data, frequency and number of turns as variables. The optimization can be done with various constraints and the ones identified in this thesis being limits of the maximum per switch loss, core loss, effective core utilization and core saturation, switch currents, and transformer winding current limits (due to restricted window width).

4. **How to design and implement planar magnetics for the selected topology with high isolation and evaluate its effectiveness in comparison to non-planar magnetics?**

   Designing a planar transformer for DAB with high isolation requirements involves basic parameter selection like the number of turns, track width, core material and dimensions, etc. Along with these, additional emphasis is needed to contain the electric fields caused due to high voltages in a material with high breakdown strength. In this thesis, the secondary winding which is at a high potential compared to protective earth, is covered with epoxy of enough thickness. However, a semiconductive paint is needed to ensure the concentration of electric fields inside the epoxy. Termination of this semiconductive layer is also important and needs proper attention. Field grading can be used for this purpose. Another important aspect of designing a PT is the shielding. It is needed to contain all the electric fields in the high breakdown strength material and therefore avoid unaccounted partial discharges or breakdowns. Also, the winding configuration can be adopted to minimize the impact of parasitic capacitances. Various normal wire wound inductors are compared with a planar inductor and it is proven that the planar magnetics

have better thermal properties and also lower losses for the same core utilization. Also since the core can be mounted on the heatsink, higher powers can be delivered with lower core volume. Thus planar magnetics are more effective compared to conventional wire-wound magnetics.

7.2. Future Developments

This thesis provided a comprehensive introduction to the MV SST design and more specifically the design of an isolated bidirectional DC-DC converter with high isolation. However, the design presented here is fundamental and further improvements can be made. Some of the recommendations for future work based on this work are presented below.

1. **Hardware testing with control loops**: In this thesis, open loop tests were conducted by giving a fixed phase shift between the full bridges. Further work can focus on a single-cell level full power testing with the proposed control strategy along with feedforward control. Though thorough converter models were developed and tested in simulation software, practical hardware tests would give further results which can provide new insights mainly with respect to the thermals and EMI of the converter.
2. **Implementing advanced control techniques**: This thesis focused on SPS control techniques which is good enough for prototyping. However with the use of some additional resources, advanced control techniques mentioned in chapter 3.3 can be implemented to study the efficiency improvements on the converter.
3. **Improvements in protection system**: The software embedded in the converter model does not have any protection system. Further protection modules can be added as software or external hardware packages to ensure the reliability of the entire system.
4. **Breakdown tests**: After implementing the semiconductive shielding, repeated breakdown tests can be performed on the transformer.
5. **Complete SST testing**: Once the cascaded inverter network is tested, a combined 18-cell model can be tested for control functionality, fault tolerance, and grid connection.

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A

PCB Designs

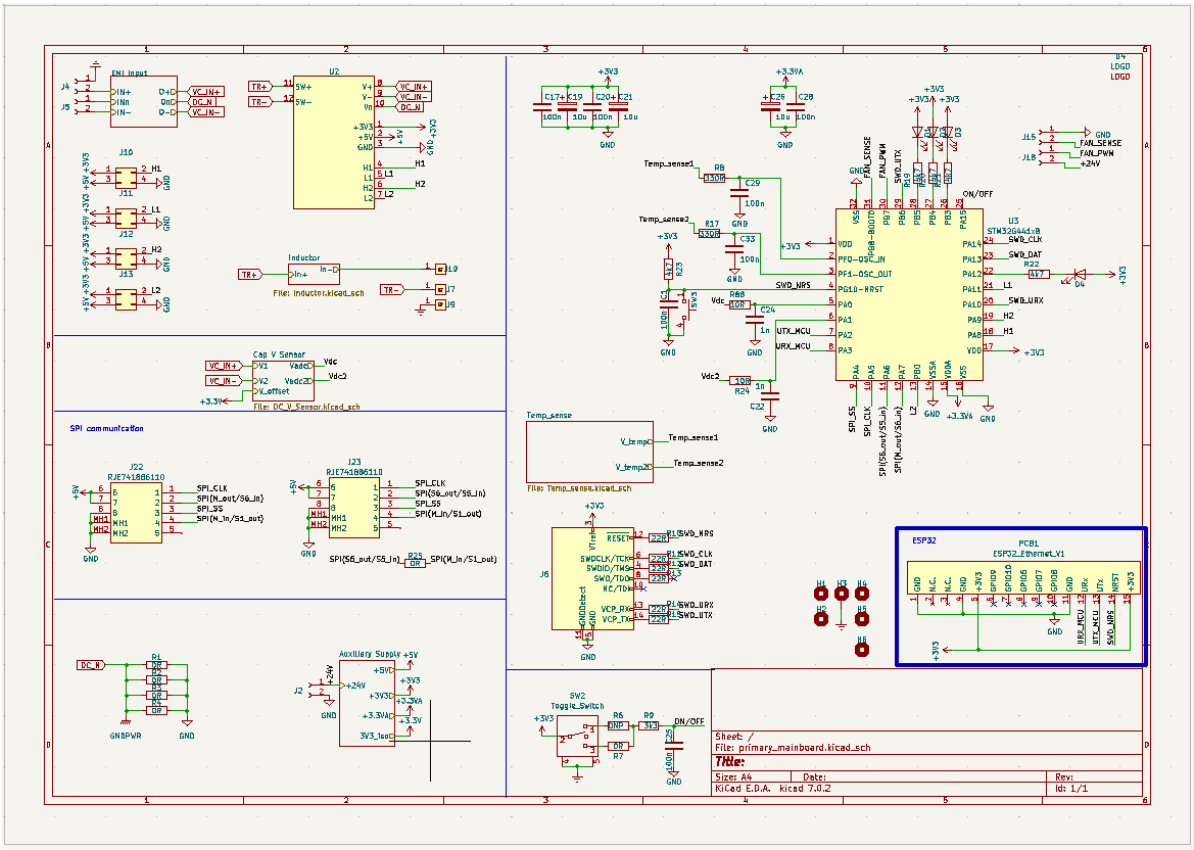

Figure A.1: Schematic of DAB primary board

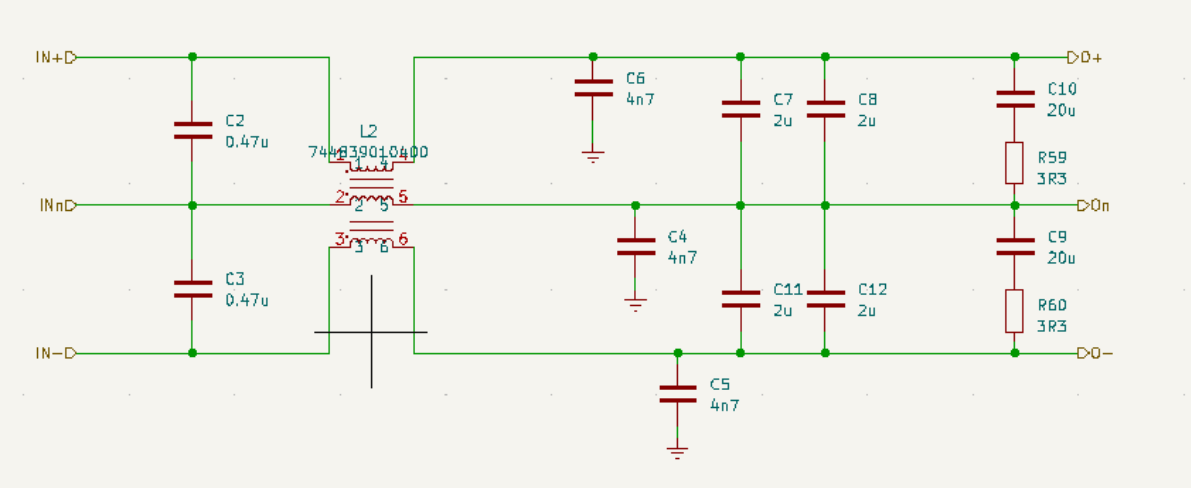

Figure A.2: EMI filter schematic

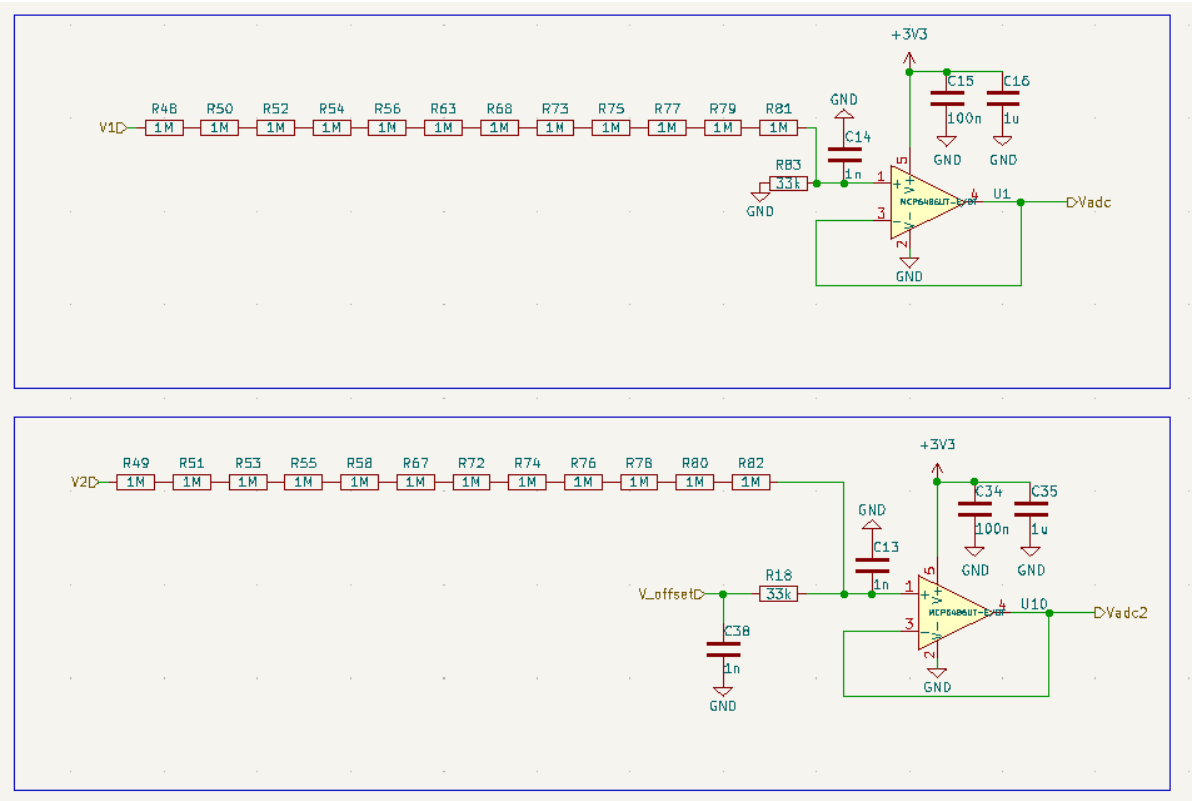

Figure A.3: Voltage divider schematic for DC grid voltage measurement

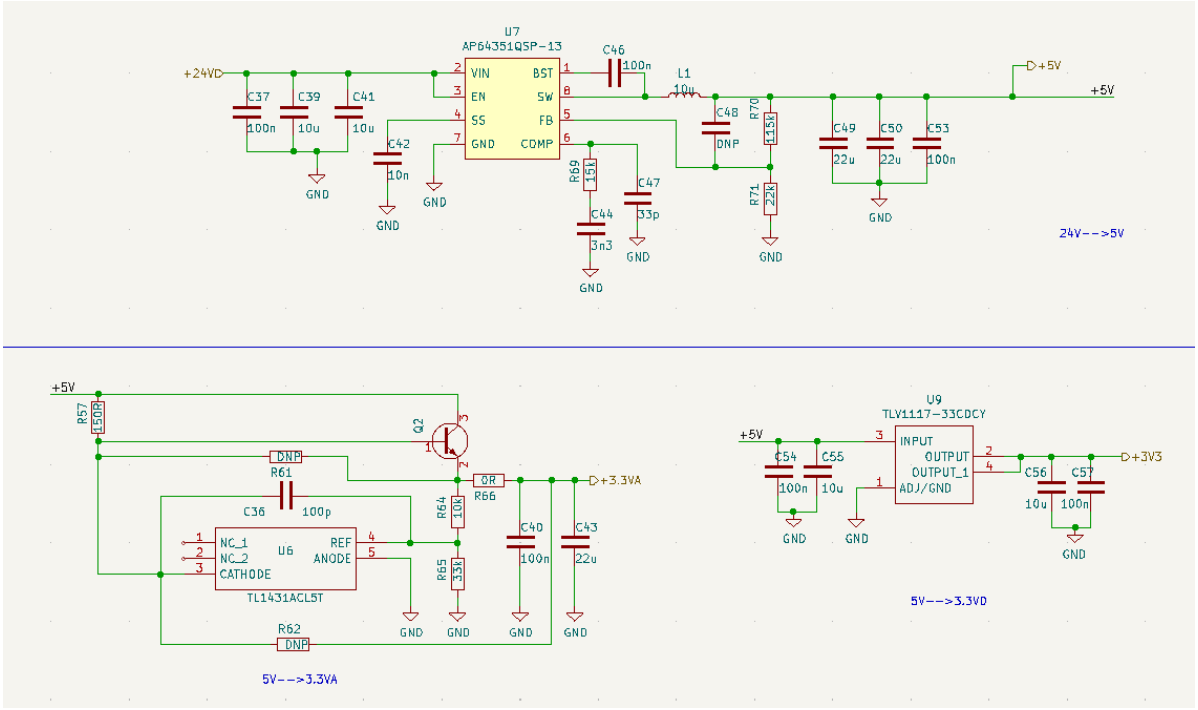

Figure A.4: Auxiliary supply schematic

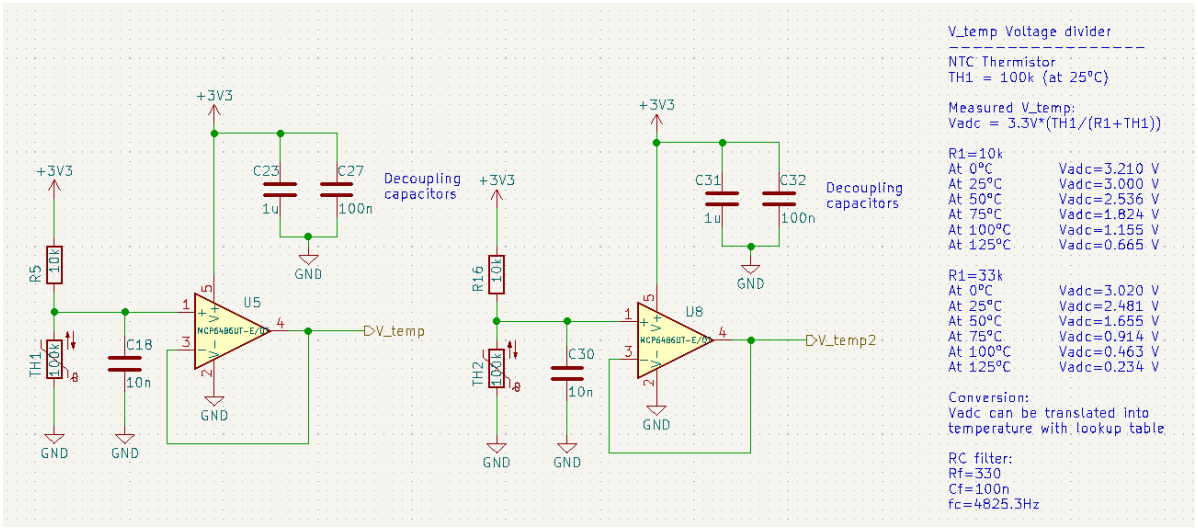

Figure A.5: Temperature sensor schematic

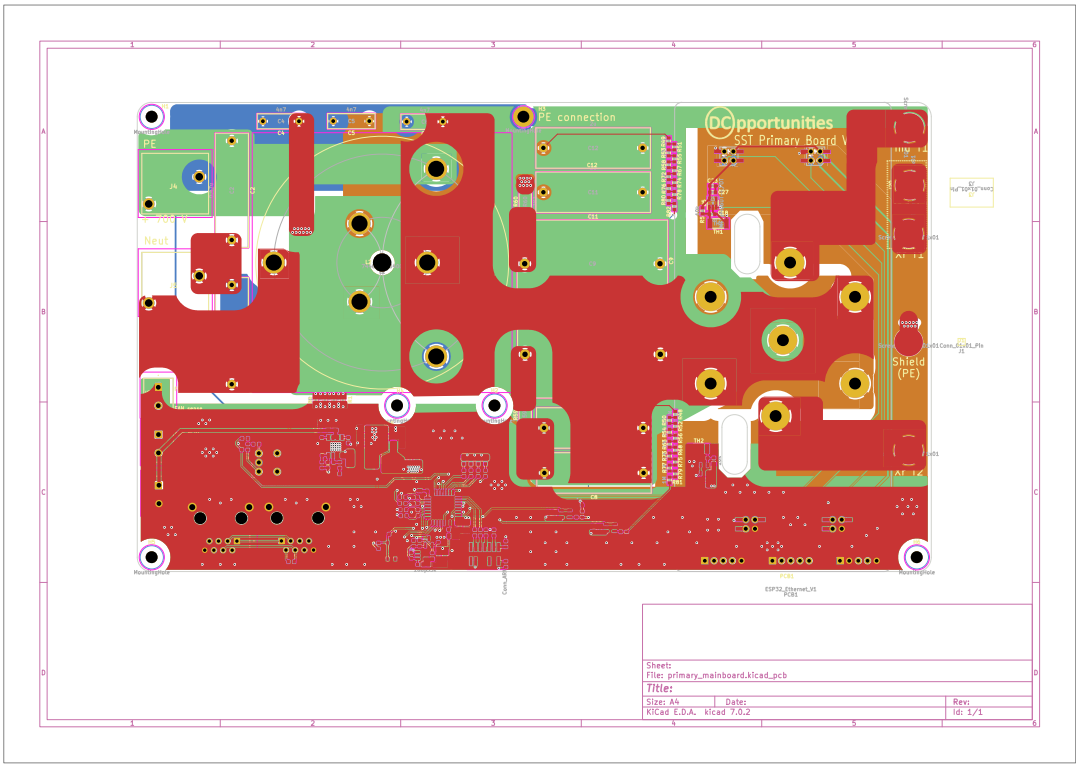

Figure A.6: Layout of DAB primary board

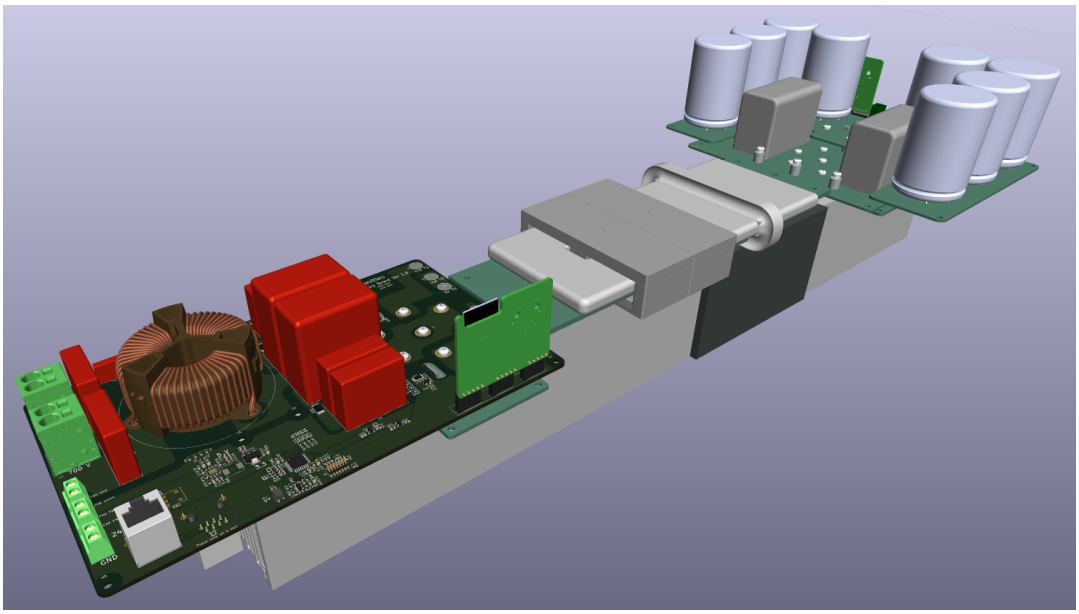

Figure A.7: Single cell 3D view

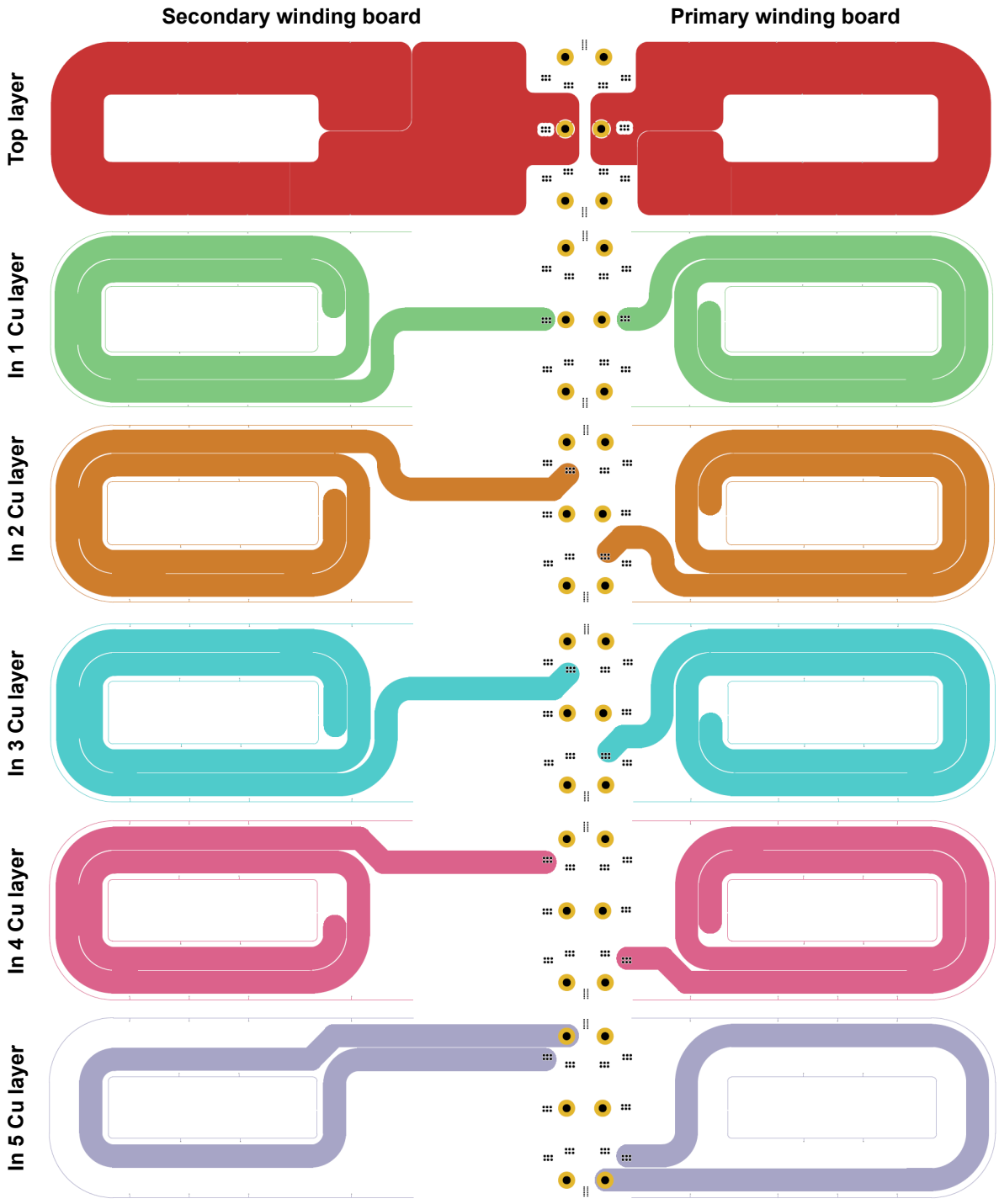

Figure A.8: Planar transformer winding design layer 1-6

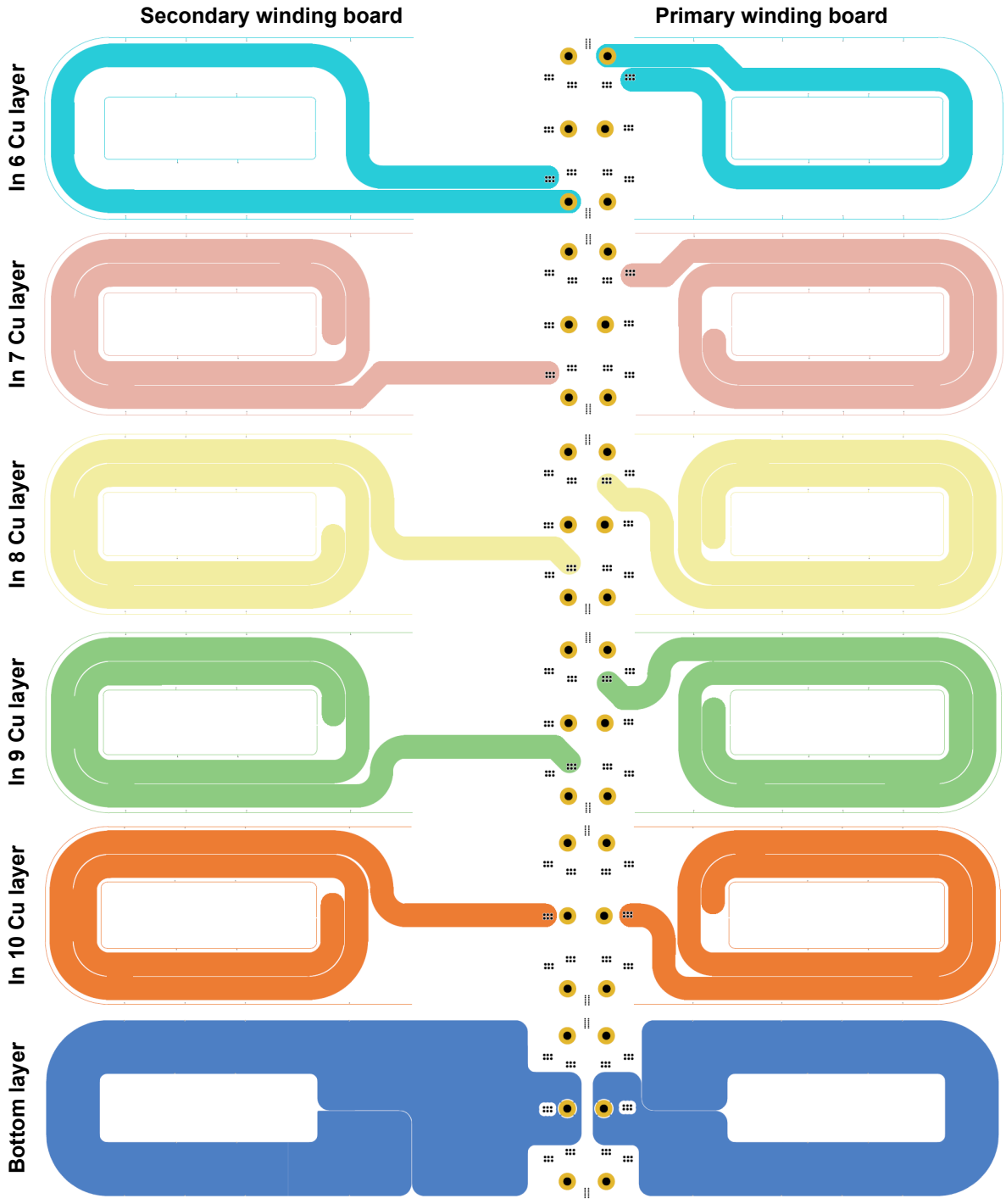

Figure A.9: Planar transformer winding design layer 7-12

B

Derivation of Maximum Possible Power Transfer

Equation 3.51 is derived below based on other equations discussed in the thesis.

From equation 4.32 and 4.34, it can be derived that,

$$I_o = \frac{2P_{SST_{max}}\sqrt{2}}{\sqrt{3}V_{ll(rms)}\pi} \tag{B.1}$$

$$I_o = \frac{P_{DAB}}{V_{sec}} \tag{B.2}$$

From equation B.1 and B.2,

$$\frac{V_{ll(rms)}}{V_{sec}} = \frac{2P_{SST_{max}}\sqrt{2}}{\sqrt{3}\pi P_{DAB}} \tag{B.3}$$

$$P_{SST} \leq \frac{V_{ll(rms)}\sqrt{3}\pi P_{DAB}}{2\sqrt{2}V_{sec}} \tag{B.4}$$

Substituting equation 3.1 in equation B.4,

$$P_{SST} \leq \frac{V_{ll(rms)}\sqrt{3}\pi}{2\sqrt{2}V_{sec}} . \frac{nV_{pri}V_{sec}\phi(1-\phi)}{2f_sL_s} \tag{B.5}$$

Considering maximum power transfer in DAB (equation 3.4),

$$P_{SST} \leq \frac{V_{ll(rms)}\sqrt{3}\pi}{2\sqrt{2}} . \frac{nV_{pri}}{8f_sL_s} \tag{B.6}$$

Upon rearranging,

$$P_{SST} \leq \frac{V_{ll(rms)} n V_{pri} \sqrt{3}\pi}{16\sqrt{2} f_s L_s}. \tag{B.7}$$

It can be seen that the amount of power transfer that is possible in the SST is dependent on both DC grid voltage and the AC grid voltage. Hence the droop for this application would be a double droop that is explained in section 3.3.2