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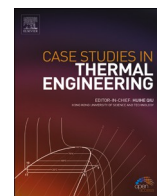
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Double-sided numerical thermal modeling of fan-out panel-level MOSFET power modules

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A B S T R A C T

Double-sided packages for heat dissipation are an efficient thermal management mechanism for power semiconductor devices. A fan-out panel-level packaging (FOPLP), as one of the double-sided forms, exhibits excellent electro–thermal characteristics and provides low stray inductance and thermal resistance. Besides, the temperature at each point within the structure is closely related to its thermo–mechanical properties and device reliability. However, thermal resistance is limited in describing the temperature distribution. Finite element analysis (FEA) requires time-consuming construction of 3D models. Therefore, to depict the temperature distribution of FOPLP rapidly and accurately, a numerical heat transfer model was proposed for the double-sided package structure. The solution was obtained from the steady-state thermal balance Laplace equation using the separation of variables method. Several boundaries were analyzed to determine the specific parameters in the model. Finally, the temperature field predicted by the derived numerical model was compared with finite element simulation results. The proposed model was consistent with both Silicon (Si) and Silicon Carbide (SiC) FOPLP structures within the error of 15 % at the center of the device, which verified the validity and accuracy of the numerical model for double-sided heat dissipation. The proposed models and results could contribute to the development of effective thermal design tools for double-sided thermal power modules.

1. Introduction

The power semiconductor module is a crucial energy conversion link in power electronic devices and is the primary heat generator because of losses generated during chip operation [1]. SiC Metal Oxide Semiconductor Field Effect Transistors (MOSFET) have become strong competitors for silicon-based semiconductors because of their low on-resistance, high switching speed, and high thermal conductivity [2]. The high junction temperature of SiC (>300 °C [3]) results in several possibilities for application in electrical devices [4]. The highest junction temperature range listed in ROHM's SiC MOSFET data manual is 150–200 °C [5]. Currently, because of packaging materials, packaging structure, cost, and reliability issues, the junction temperature of devices is typically limited to 175 °C [6]. Temperature affects the mechanical and thermal properties of the device [7]. Higher temperatures may cause bonding wires and chips thermally breakdown. In addition, the thermal stress problems caused by the mismatch of coefficient of thermal expansion exist

not only between different materials, but also within the same material. These potential failures are caused by heat in the device [8]. Therefore, thermal management is critical in the application of SiC power modules [9,10]. Accurate prediction and rapid simulation are essential in the design verification process [11].

Conventional lead frame power module packaging only has one heat dissipation channel because the silicone gel on the upper surface of the module provides excellent thermal insulation [12,13]. The heat generated by the chip is transmitted to the heat sink through heat conduction and ultimately transferred to the environment through convection. With the development of the higher power density chip, the double-sided heat dissipation structure provides an efficient heat transfer mechanism [14]. FOPLP is a miniaturized structure that achieves electrical connections in the distribution layer. Hou et al. [15] and Regnat et al. [16] studied FOPLP for chip lateral and vertical distribution, respectively. Chen et al. [17] fabricated another version with the epoxy molding compound. However, Chen et al. used FEA and the thermal cycling test to characterize the thermal characteristics of the module. Finite element simulation has high requirements for simulation equipment, and the grid is large and time-consuming to solve. Therefore, the development of a fast, accurate, and efficient thermal characteristic testing method is crucial.

Currently, thermal modeling of power modules can be performed using two methods. One method is the thermoelectric network model, that is, the conventional Foster or Cauer model. In this method, thermal resistance and heat capacity are used to form an RC thermal equivalent circuit and establish a thermal impedance equation to equivalent the power module to a one-dimensional heat transfer path. This model provides concise expression and fast calculation speed [18]. An et al. [12] obtained the model parameters using two methods to establish the Cauer thermal network models of the IGBT module. However, the lateral heat transfer of the chip cannot be calculated and the junction temperature is underestimated. To achieve an accurate description of thermal diffusion coupling under various operating conditions, Lachello et al. [19] proposed a three-dimensional (3D) fourth-order Foster-type thermal network in which the thermal coupling effect between the IGBT and diode is considered. Fu et al. [20] proposed two 3-D RC-lumped thermal network models with few adjustable thermal resistances for the reliability analysis of the fan-cooled plate-fin heatsink. Li Jianfeng et al. [21] and Mingyao et al. [22] proposed a 3D third-order Cauer-type thermal network in which the thermal coupling effect between various bridge arms of chips is considered. However, the RC parameters in the network were obtained through finite element dynamic simulation, which requires a long time to solve. The precise model has numerous RC parameters, high recognition complexity, and low computational efficiency.

Another method to characterize the thermal behavior is numerical analysis in which the lateral heat conduction process is considered during the solution process. Delouei et al. [23] summarized the various methods for numerically calculating heat conduction. Muzychka et al. [24] proposed a general solution of the thermal spreading performance of eccentric heat sources on a rectangular flux channel. The steady temperature distribution of a rectangular double-layer structure is available for multi-chip modules. Chen Daolong et al. [25] obtained the optimal chip size and multi-chip module layout by combining the optimization algorithm from the derived equation. Geer et al. [26] extended the numerical model to multilayer structures and considered the scenario in which the thermal resistance of the contact surface leads to temperature step changes. Desai et al. [27] investigated numerical mothed to find the most effective fin configuration. The flexibility of application scenarios increases the difficulty of solving Fourier coefficients. To solve this problem, Choudhury [28] proposed a steady-state thermal modeling with an arbitrary number of layers containing an arbitrary number of rectangular heat sources on its topmost surface. The difference between the simplified process of the model and the actual thermal performance was discussed. Kangjia et al. [29] solved the transient thermal model. Furthermore, imperfect contact was considered. Several models were analyzed under the validation of FEA and numerical models. The distribution of multi-chip thermal coupling in various layouts was critically analyzed and discussed by Tang et al. [30]. Long et al. [31] analyzed the influence of variable convection coefficients in the working scenario. Rangarajan et al. [32] reduced the junction temperature of the device and improved the temperature uniformity by using the genetic algorithm and artificial neural network (ANN). Jakani et al. [33] extracted the time constants with a model order reduction technique based on the Ritz vector approach. In addition to describing the thermal performance of electronic devices [34], bio-thermal studies for the temporal and spatial variation of temperature in a 3D triple-layer skin tissue under laser heating were analyzed through this methodology [35]. However, the studies are focused on the numerical modeling of conventional single-sided cooling power modules, and the numerical heat dissipation solution of double-sided cooling modules is yet to be studied. To evaluate the temperature characteristics of double-sided heat dissipation quickly and accurately, a numerical heat dissipation solution model should be established for double-sided heat dissipation. A numerical method without 3D modeling can be applied to evaluate the thermal characteristics of a device quickly and efficiently at the preliminary design period. Moreover, the proposed double-sided numerical thermal modeling completes the analytical modeling of power modules in various packages.

In this study, steady-state double-sided numerical thermal modeling of a multilayer structure is proposed. This method is then applied to a 30 V Si FOPLP and a 1200 V SiC FOPLP. The rest of the paper is organized as follows: Section II introduces the procedure of numerical theoretical modeling. The distribution of thermal power and the multilayer numerical modeling are illustrated. Section III discusses the process of simplifying models in numerical methods. In Section IV, the temperature distribution of the numerical model, the simplified FEA model, and the unsimplified model at various cross-sectional cutoffs are obtained to verify the feasibility and accuracy of the numerical model of the proposed double-sided heat dissipation. Finally, Section V summarizes the previous section on model building and validation discussion.

2. Numerical theoretical modeling

In this section, both the fundamental model of double-sided heat dissipation and the multilayer structure heat dissipation model are developed.
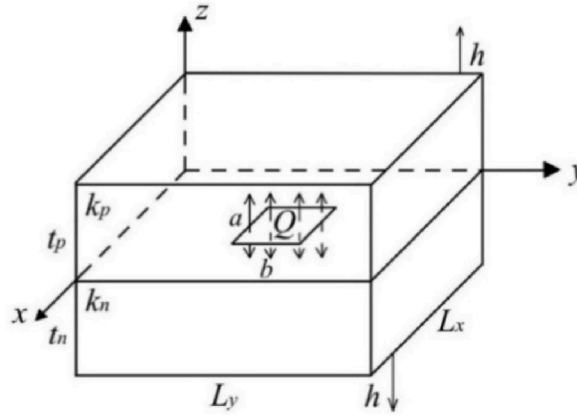
Fig. 1. Isotropic double-sided plate with eccentric heat source.

2.1. Numerical modeling of the basic theoretical model for double-sided heat dissipation

Fig. 1 shows the basic model of double-sided heat dissipation. The rectangular structure represents the overall structure of the power module. The rectangular area inside is a heat source. In the power module, the chip functions as a heat source and conducts heat in both upward and downward directions. Therefore, we simplified the chip of the model as a thin film structure with length a, width b, and area A_s. The longitudinal heat transfer zone is an area with length L_x, width L_y, and area A_c. The power loss provided by the chip is Q, and the z-axis origin is in the plane in which the chip is located. Since the selected MOSETs in this paper have a maximum junction temperature of 175 °C, this limits the temperature range of the entire package. However, radiative heat transfer is generally more important at high temperatures above 300 °C. Therefore, radiative heat transfer can be ignored in this study. To simplify the calculations, it is assumed that the water-cooling situation is the same for the top and bottom. The convective heat transfer coefficient of the top and lower surfaces is h. The specific value can be determined according to the actual application. The thermal conductivity of the top and lower materials are k_p and k_n respectively. The coordinates of the chip center are (x_c, y_c), and the lengths of the upper and lower conduction paths are t_p and t_n, respectively.

The temperature distribution function of the structure is $T(x, y, z)$. The ambient temperature is T_{air}. The Laplace's equation of steady-state heat conduction can be expressed as follows:

$$\nabla^2 T = \frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} = 0 \tag{1}$$

The general solution is typically expressed as $\theta(x, y, z) = X(x) * Y(y) * Z(z)$, where $\theta(x, y, z) = T(x, y, z) - T_{air}$. Due to the thinness of the entire structure, the side area is small compared to the heat dissipation area of the upper and lower surfaces. Besides, there is no forced convection at the sides. To simplify the calculation it is assumed that the surrounding area is adiabatic. The boundary conditions of the above are as follows:

$$\left. \frac{\partial T}{\partial x} \right|_{x = 0, L_x} = 0 \tag{2}$$

$$\left. \frac{\partial T}{\partial y} \right|_{y = 0, L_y} = 0 \tag{3}$$

The general solution of Laplace's equation can be obtained as follows:

$$\theta(x, y, z) = A_0 + B_0 z + \sum_{m=1}^{\infty} cos(\lambda x)[A_1 \ cosh(\lambda z) + B_1 \ sinh(\lambda z)]$$

$$+ \sum_{n=1}^{\infty} cos(\delta y)[A_2 \ cosh(\delta z) + B_2 \ sinh(\delta z)]$$

$$+ \sum_{m=1}^{\infty} \sum_{n=1}^{\infty} cos(\lambda x)cos(\delta y)[A_3 \ cosh(\beta z) + B_3 \ sinh(\beta z)] \tag{4}$$

where $\lambda = m\pi/L_x$, $m = 1, 2, 3\cdots$, $\delta = n\pi/L_y$, $n = 1, 2, 3\cdots$, $\beta = \sqrt{\lambda^2 + \delta^2}$, and $B_i = \varphi(\xi)A_i$, $i = 1, 2, 3$.

The boundary conditions for convective heat transfer between the upper and lower interfaces and air are as follows:

$$\frac{\partial T}{\partial z}\bigg|_{z\,=\,t_p} = -\frac{h}{k_p}\left[T(x,y,t_p)-T_{air}\right] \tag{5}$$

$$\frac{\partial T}{\partial z}\bigg|_{z\,=\,-t_n} = \frac{h}{k_n}\left[T(x,y,-t_n)-T_{air}\right] \tag{6}$$

Because of the opposite direction of heat transfer between the positive and negative directions on z-axis, the Fourier coefficients of the convective heat transfer at interface $z = t_p$ and $z = -t_n$ should be solved.

For heat conduction in the positive direction, the Fourier coefficient can be expressed as follows:

$$\varphi(\xi) = -\frac{\xi\sinh(\xi t_p) + \dfrac{h}{k_p}\cosh(\xi t_p)}{\xi\cosh(\xi t_p) + \dfrac{h}{k_p}\sinh(\xi t_p)} \tag{7}$$

For heat conduction in the negative direction, the Fourier coefficient can be expressed as follows:

$$\varphi(\xi) = \frac{sin\,h(\xi t_n) + h/k_n\,cosh(\xi t_n)}{\xi\,cosh(\xi t_n) + h/k_n\,cosh(\xi t_n)} \tag{8}$$

where ξ is replaced by λ, δ, or β.

The heating of the chip is performed in both directions, but the power transmitted in both directions differs considerably. Therefore, the power distribution of the heat source should be considered, which is analyzed in detail after the formula derivation is completed. The total power generated by the chip was set to $Q = Q_1 + Q_2$. The surface power input Q_1 on the chip in the positive direction is analyzed first. At this stage, the boundary of the chip layer consists of the following two parts:

Within A_s, $\frac{\partial T}{\partial z}\big|_{z\,=\,0} = -\frac{Q_1/A_s}{k_p}$.

Outside A_s area, the total amount of heat conducted is the total amount of heat dissipated from the negative surface, which can be expressed as follows:

$$\iint\limits_{A_c\not\supset A_s} k_n\frac{\partial T}{\partial z}\bigg|_{z\,=\,0} = \iint\limits_{A_c} h\theta_{Q_1}(x,y,-t_n) \tag{9}$$

The general solution coefficient can be obtained through the a forementioned boundary conditions as follows:

$$
\begin{aligned}
A_1 &= \frac{\int_0^{L_x}\frac{\partial\theta_{Q_1}}{\partial z}\bullet\frac{1}{\varphi(\lambda)\lambda}\bullet cos(\lambda x)dx}{\int_0^{L_x}cos^2(\lambda x)dx}\\[6pt]
&= \frac{\int_{x_c-\frac{a}{2}}^{x_c+\frac{a}{2}}\frac{-Q_1/A_s}{\varphi(\lambda)\lambda k_p}cos(\lambda x)dx + \int_{else}\frac{\partial\theta_{Q_1}}{\partial z}\bullet\frac{1}{\varphi(\lambda)\lambda}cos(\lambda x)dx}{\int_0^{L_x}cos^2(\lambda x)dx}\\[6pt]
&= \frac{-2Q_1\cos(x_c\lambda)\sin\left(\frac{\lambda}{2}a\right)\left(\dfrac{1+h\dfrac{t_p+t_n}{k_n}}{A_c-A_s}+\dfrac{2}{A_s}\right)}{L_x\varphi(\lambda)\lambda^2 k_p}
\end{aligned} \tag{10}
$$

$$
\begin{aligned}
A_2 &= \frac{\int_0^{L_y}\frac{\partial\theta_{Q_1}}{\partial z}\bullet\frac{1}{\varphi(\delta)\delta}\bullet cos(\delta y)dy}{\int_0^{L_y}cos^2(\delta y)dy}\\[6pt]
&= \frac{\int_{y_c-\frac{b}{2}}^{y_c+\frac{b}{2}}\frac{-Q_1/A_s}{\varphi(\delta)\delta k_p}cos(\delta y)dy + \int_{else}\frac{\partial\theta_{Q_1}}{\partial z}\bullet\frac{1}{\varphi(\delta)\delta}cos(\delta y)dy}{\int_0^{L_y}cos^2(\delta y)dy}\\[6pt]
&= \frac{-2Q_1\,cos(y_c\delta)sin\left(\frac{\delta}{2}b\right)\left(\dfrac{1+h\dfrac{t_p+t_n}{k_n}}{A_c-A_s}+\dfrac{2}{A_s}\right)}{L_y\varphi(\delta)\delta^2 k_p}
\end{aligned} \tag{11}
$$

$$A_3 = \frac{\int_0^{L_x} \int_0^{L_y} \frac{\partial \theta_{Q_1}}{\partial z} \bullet \frac{1}{\varphi(\beta)\beta} \bullet cos(\lambda x)cos(\delta y)dxdy}{\int_0^{L_x} \int_0^{L_y} cos^2(\lambda x)cos^2(\delta y)dxdy}$$

$$= \frac{\int_{x_c - \frac{a}{2}}^{x_c + \frac{a}{2}} \int_{y_c - \frac{b}{2}}^{y_c + \frac{b}{2}} \frac{-Q_1/A_s}{\varphi(\beta)\beta k_p}cos(\lambda x)cos(\delta y)dxdy + \iint_{else} \frac{\partial \theta_{Q_1}}{\partial z} \bullet \frac{1}{\varphi(\beta)\beta}cos(\lambda x)cos(\delta y)dxdy}{\int_0^{L_x} \int_0^{L_y} cos^2(\lambda x)cos^2(\delta y)dxdy} \tag{12}$$

$$= \frac{-8Q_1 \, cos(x_c\lambda)sin\left(\frac{\lambda}{2}a\right)cos(y_c\delta)sin\left(\frac{\delta}{2}b\right)\left(\frac{1 + h\frac{t_p + t_n}{k_p}}{A_c - A_s} + \frac{2}{A_s}\right)}{A_c\lambda\delta\varphi(\beta)\beta^2 k_p}$$

For power Q_1 conducted in the positive direction of the z-axis, $A_0 = \frac{Q_1}{2A_s}\left(\frac{1}{h} + \frac{t_p - t_n}{k_p}\right)$, $B_0 = -\frac{Q_1}{A_s k_p}$.

For power Q_2 conducted in the negative direction of the z-axis, $A_0 = -\frac{Q_2}{2A_s}\left(\frac{1}{h} + \frac{t_p - t_n}{k_n}\right)$, $B_0 = \frac{Q_2}{A_s k_n}$. The parameters of the surface power input Q_2 on the chip in the negative direction can be written as:

$$A_1 = \frac{\int_0^{L_x} \frac{\partial \theta_{Q_2}}{\partial z} \bullet \frac{1}{\varphi(\lambda)\lambda} \bullet cos(\lambda x)dx}{\int_0^{L_x} cos^2(\lambda x)dx}$$

$$= \frac{\int_{x_c - \frac{a}{2}}^{x_c + \frac{a}{2}} \frac{Q_2/A_s}{\varphi(\lambda)\lambda k_n}cos(\lambda x)dx + \int_{else}\frac{\partial \theta_{Q_2}}{\partial z} \bullet \frac{1}{\varphi(\lambda)\lambda}cos(\lambda x)dx}{\int_0^{L_x} cos^2(\lambda x)dx} \tag{13}$$

$$= \frac{2Q_2 \, cos(x_c\lambda)sin\left(\frac{\lambda}{2}a\right)\left(\frac{1 + h\frac{t_p + t_n}{k_p}}{A_c - A_s} + \frac{2}{A_s}\right)}{L_x\varphi(\lambda)\lambda^2 k_n}$$

$$A_2 = \frac{\int_0^{L_y} \frac{\partial \theta_{Q_2}}{\partial z} \bullet \frac{1}{\varphi(\delta)\delta} \bullet cos(\delta y)dy}{\int_0^{L_y} cos^2(\delta y)dy}$$

$$= \frac{\int_{y_c - \frac{b}{2}}^{y_c + \frac{b}{2}} \frac{Q_2/A_s}{\varphi(\delta)\delta k_p}cos(\delta y)dy + \int_{else}\frac{\partial \theta_{Q_2}}{\partial z} \bullet \frac{1}{\varphi(\delta)\delta}cos(\delta y)dy}{\int_0^{L_y} cos^2(\delta y)dy} \tag{14}$$

$$= \frac{2Q_2 \, cos(y_c\delta)sin\left(\frac{\delta}{2}b\right)\left(\frac{1 + h\frac{t_p + t_n}{k_p}}{A_c - A_s} + \frac{2}{A_s}\right)}{L_y\varphi(\delta)\delta^2 k_n}$$

$$A_3 = \frac{\int_0^{L_x} \int_0^{L_y} \frac{\partial \theta_{Q_2}}{\partial z} \bullet \frac{1}{\varphi(\beta)\beta} \bullet cos(\lambda x)cos(\delta y)dxdy}{\int_0^{L_x} \int_0^{L_y} cos^2(\lambda x)cos^2(\delta y)dxdy}$$

$$= \frac{\int_{x_c - \frac{a}{2}}^{x_c + \frac{a}{2}} \int_{y_c - \frac{b}{2}}^{y_c + \frac{b}{2}} \frac{Q_2/A_s}{\varphi(\beta)\beta k_p}cos(\lambda x)cos(\delta y)dxdy + \iint_{else} \frac{\partial \theta_{Q_2}}{\partial z} \bullet \frac{1}{\varphi(\beta)\beta}cos(\lambda x)cos(\delta y)dxdy}{\int_0^{L_x} \int_0^{L_y} cos^2(\lambda x)cos^2(\delta y)dxdy} \tag{15}$$

$$= \frac{8Q_2 \, cos(x_c\lambda)sin\left(\frac{\lambda}{2}a\right)cos(y_c\delta)sin\left(\frac{\delta}{2}b\right)\left(\frac{1 + h\frac{t_p + t_n}{k_p}}{A_c - A_s} + \frac{2}{A_s}\right)}{A_c\lambda\delta\varphi(\beta)\beta^2 k_n}$$

At this stage, the numerical model derivation and solution of the rectangular module with double-sided heat dissipation embedded in the heat source are complete. However, the power distribution of heat conduction between the top and bottom of the chip should be discussed. The average surface temperature of the chip to represent the junction temperature is T_j. The average temperature of the top
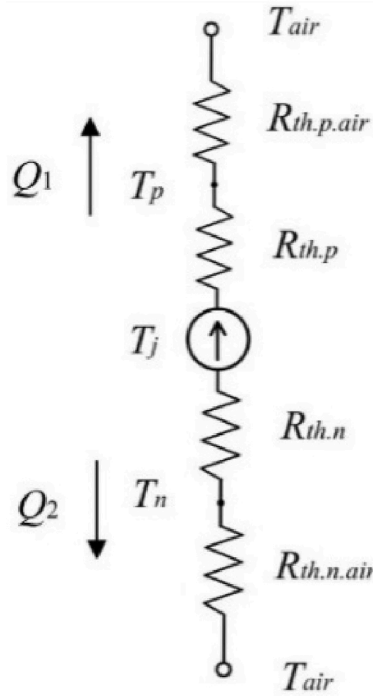
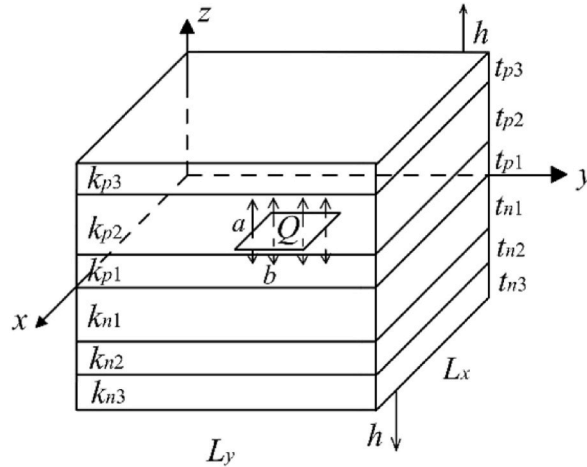**Fig. 2.** Thermoelectric network of double-sided heat dissipation.

Fig. 3. Isotropic multi-layer double-sided plate with eccentric heat source.

and bottom surfaces of the structure are T_p and T_n, respectively. $R_{th.p.air}$ and $R_{th.n.air}$ represent the convective thermal resistance between the surfaces and the environment. $R_{th.p}$ and $R_{th.n}$ represent the thermal resistance between the surfaces and the die. The temperature transfer of heat conduction can be described using a thermoelectric network, as shown in Fig. 2.

Because of the fixed ambient temperature, the upward and downward power transmission can be considered as parallel shunting. Specifically, Q_1 and Q_2 should be distributed by the thermal resistance through rectangular conduction and the convective thermal resistance with air. Therefore, the thermal resistance should be first calculated.

Thermal resistance is a physical quantity that is determined by the size of the material structure and is independent of the power level. Therefore, when discussing the thermal resistance in both positive and negative directions, thermal resistance can be calculated separately. However, the thermal resistance depends on the increase in temperature. The temperature difference is used to deduce the size of thermal resistance. The difference between the average temperature of the chip surface and the ambient temperature is used to represent the temperature difference between the junction temperature and the environment, which can be expressed as follows:

$$R_T = \frac{\overline{\theta}}{Q} \tag{16}$$

According to the Laplace equation, when the heat conduction outside the heat source area of the chip layer is not considered, it is equivalent to the general solution of one-sided heat dissipation. At this stage, the steady-state heat solution in the positive direction can be expressed as follows:

$$A_1 = \frac{\int_0^{L_x} \frac{\partial \theta}{\partial z} \bullet \frac{1}{\varphi(\lambda)\lambda} \bullet cos(\lambda x)dx}{\int_0^{L_x} cos^2(\lambda x)dx} \tag{17}$$

$$A_1 = Q_1 C_1 \tag{18}$$

$$A_2 = \frac{\int_0^{L_y} \frac{\partial \theta}{\partial z} \bullet \frac{1}{\varphi(\delta)\delta} \bullet cos(\delta y)dy}{\int_0^{L_y} cos^2(\delta y)dy} \tag{19}$$

$$A_2 = Q_1 C_2 \tag{20}$$

$$A_3 = \frac{\int_0^{L_x} \int_0^{L_y} \frac{\partial \theta}{\partial z} \bullet \frac{1}{\varphi(\beta)\beta} \bullet cos(\lambda x)cos(\delta y)dxdy}{\int_0^{L_x} \int_0^{L_y} cos^2(\lambda x)cos^2(\delta y)dxdy} \tag{21}$$

$$A_3 = Q_1 C_3 \tag{22}$$

where, C_1, C_2 and C_3 represent the parameter in the thermal resistance general solution.

The difference between chip junction temperature and ambient temperature can be expressed as follows:

$$\overline{\theta_{Q_1}} = \frac{1}{A_s} \int_{x_c-\frac{a}{2}}^{x_c+\frac{a}{2}} \int_{y_c-\frac{b}{2}}^{y_c+\frac{b}{2}} \theta(x,y,0)dxdy = A_0 + 2\sum_{m=1}^{\infty} A_1 \frac{cos(x_c\lambda)sin\left(\frac{\lambda}{2}a\right)}{\lambda a} + 2\sum_{n=1}^{\infty} A_2 \frac{cos(y_c\delta)sin\left(\frac{\delta}{2}b\right)}{\delta b}$$
$$+4\sum_{m=1}^{\infty}\sum_{n=1}^{\infty} A_3 \frac{cos(x_c\lambda)sin\left(\frac{\lambda}{2}a\right)cos(y_c\delta)sin\left(\frac{\delta}{2}b\right)}{\lambda a \delta b} \tag{23}$$

The positive thermal resistance can be expressed as follows:

$$R_{th.p} + R_{th.p.air} = \frac{\overline{\theta_{Q_1}}}{Q_1} = C_0 + 2\sum_{m=1}^{\infty} C_1 \frac{cos(x_c\lambda)sin\left(\frac{\lambda}{2}a\right)}{\lambda a} + 2\sum_{n=1}^{\infty} C_2 \frac{cos(y_c\delta)sin\left(\frac{\delta}{2}b\right)}{\delta b}$$
$$+4\sum_{m=1}^{\infty}\sum_{n=1}^{\infty} C_3 \frac{cos(x_c\lambda)sin\left(\frac{\lambda}{2}a\right)cos(y_c\delta)sin\left(\frac{\delta}{2}b\right)}{\lambda a \delta b} \tag{24}$$

For negative thermal resistance, the input power direction and φ should be replaced with a negative coefficient. The power distribution can be split by the parallel relationship of thermal resistance as follows:

$$\frac{Q_2}{Q_1} = \frac{R_{th.p} + R_{th.p.air}}{R_{th.n} + R_{th.n.air}} \tag{25}$$

After power transmission in two directions is calculated separately, because of the linear superposition of temperature, the temperature distribution of the double-sided cooling infrastructure can be expressed as follows:

$$T(x,y,z) = \theta_{Q_1}(x,y,z) + \theta_{Q_2}(x,y,z) + T_{air} \tag{26}$$

2.2. Numerical modeling of multilayer double-sided heat dissipation

Because of the required electrical connections between the chips in the module package, a copper layer is introduced. Moreover, a solder is also required between the chip and the heat dissipation layer. Therefore, the double-sided heat dissipation structure is composed of multiple layers of material as shown in Fig. 3. For the sake of analysis, the thickness and thermal conductivity of the structure above the chip are denoted as t_{pi} and k_{pi}. The thickness and thermal conductivity of the structure below the chip are denoted

as t_{ni} and k_{ni}. Assuming an existing rectangular structure with six layers of materials stacked, the chip as a heat source is simplified as a thin film structure, located between the third and fourth layers, and functions as the origin plane of the z-axis coordinate system.

The heat conduction function [Eq. (4)] of each layer is independent, since the boundary conditions are both [Eq. (2)] and [Eq. (3)]. Therefore, in order to determine the specific solution, it is necessary to determine the parameters according to the boundary conditions. Firstly, based on the boundaries of the chip layer shown in [Eq. (9)] and the boundaries of the top and bottom surface layers of the multilayer structure shown in [Eq. (5)] and [Eq. (6)], the Fourier coefficient φ for the surface layers and the A for the chip layer can be written as:

$$\varphi_{psurface}(\xi) = -\frac{\xi \sin h(\xi t_{psum}) + h/k_{p3} \cos h(\xi t_{psum})}{\xi \cos h(\xi t_{psum}) + h/k_{p3} \sinh(\xi t_{psum})} \tag{27}$$

$$\varphi_{nsurface}(\xi) = \frac{\xi \sin h(\xi t_{nsum}) + h/k_{n3} \cos h(\xi t_{nsum})}{\xi \cos h(\xi t_{nsum}) + h/k_{n3} \sinh(\xi t_{nsum})} \tag{28}$$

$$A_{1.p1} = \frac{2Q_1 \cos(x_c\lambda)\sin\left(\frac{\lambda}{2}a\right)\left(\frac{1+h\frac{t_{sum}}{k_n}}{A_c - A_s} + \frac{2}{A_s}\right)}{L_x\varphi(\lambda)\lambda^2 k_p} \tag{29}$$

$$A_{1.n1} = \frac{2Q_2 \cos(x_c\lambda)\sin\left(\frac{\lambda}{2}a\right)\left(\frac{1+h\frac{t_{sum}}{k_p}}{A_c - A_s} + \frac{2}{A_s}\right)}{L_x\varphi(\lambda)\lambda^2 k_n} \tag{30}$$

$$A_{2.p1} = \frac{2Q_1 \cos(y_c\delta)\sin\left(\frac{\delta}{2}b\right)\left(\frac{1+h\frac{t_{sum}}{k_n}}{A_c - A_s} + \frac{2}{A_s}\right)}{L_y\varphi(\delta)\delta^2 k_p} \tag{31}$$

$$A_{2.n1} = \frac{2Q_2 \cos(y_c\delta)\sin\left(\frac{\delta}{2}b\right)\left(\frac{1+h\frac{t_{sum}}{k_p}}{A_c - A_s} + \frac{2}{A_s}\right)}{L_y\varphi(\delta)\delta^2 k_n} \tag{32}$$

$$A_{3.p1} = \frac{8Q_1 \cos(x_c\lambda)\sin\left(\frac{\lambda}{2}a\right)\cos(y_c\delta)\sin\left(\frac{\delta}{2}b\right)\left(\frac{1+h\frac{t_{sum}}{k_n}}{A_c - A_s} + \frac{2}{A_s}\right)}{A_c\lambda\delta\varphi(\beta)\beta^2 k_p} \tag{33}$$

$$A_{3.n1} = \frac{8Q_2 \cos(x_c\lambda)\sin\left(\frac{\lambda}{2}a\right)\cos(y_c\delta)\sin\left(\frac{\delta}{2}b\right)\left(\frac{1+h\frac{t_{sum}}{k_p}}{A_c - A_s} + \frac{2}{A_s}\right)}{A_c\lambda\delta\varphi(\beta)\beta^2 k_n} \tag{34}$$

where $\varphi_{psurface}(\xi)$ is the Fourier coefficient of the top layer. $\varphi_{nsurface}(\xi)$ is the Fourier coefficient of the top layer. t_{sum} represents the total thickness of all structures of the package. $A_{i.p1}$ represents the value of A_i (i = 1, 2 and 3) in the analytic solution of the first layer in the positive direction. $A_{i.n1}$ represents the value of A_i (i = 1, 2 and 3) in the analytic solution of the first layer in the negative direction.

The boundary conditions for heat conduction between layers are as follows:

$$\theta_{t_{pi}}(x, y, z_i) = \theta_{t_{p(i+1)}}(x, y, \theta_{t_i}) \tag{35}$$

$$\theta_{t_{ni}}(x, y, z_i) = \theta_{t_{n(i+1)}}(x, y, \theta_{t_i}) \tag{36}$$

$$k_{pi}\frac{\partial\theta_{t_{pi}}}{\partial z}|z_i = k_{p(i+1)}\frac{\partial\theta_{t_{p(i+1)}}}{\partial z}|z_i \tag{37}$$

$$k_{ni}\frac{\partial\theta_{t_{ni}}}{\partial z}|z_i = k_{n(i+1)}\frac{\partial\theta_{t_{n(i+1)}}}{\partial z}|z_i \tag{38}$$

According to the boundary conditions [Eq. (37)] and [Eq. (38)] the relationship between the parameters of different layers can be determined. The Fourier coefficient for each layer from top to bottom is expressed as follows:

$$\varphi_{pi}(\xi) = \frac{\kappa\left[\sin h(\xi t_{sum}) + \varphi_{p(i+1)}(\xi)\cosh(\xi t_{sum})\right] \bullet \cosh(\xi t_{sum}) - \left[\cosh(\xi t_{sum}) + \varphi_{p(i+1)}(\xi)\sinh(\xi t_{sum})\right] \bullet \sinh(\xi t_{sum})}{\left[\cosh(\xi t_{sum}) + \varphi_{p(i+1)}(\xi)\sinh(\xi t_{sum})\right] \bullet \cosh(\xi t_{sum}) - \kappa\left[\sin h(\xi t_{sum}) + \varphi_{p(i+1)}(\xi)\cosh(\xi t_{sum})\right] \bullet \sinh(\xi t_{sum})}$$

(39)

where $\varphi_{pi}(\xi)$ is the Fourier coefficient of the ith layer in the positive direction. t_{psum} represents the total thickness of all structures above the chip. and $\kappa = k_{p(i+1)}/k_{pi}$.

$$\varphi_{ni}(\xi) = \frac{\kappa\left[-\sin h(\xi t_{sum}) + \varphi_{n(i+1)}(\xi)\cosh(\xi t_{sum})\right] \bullet \cosh(\xi t_{sum}) + \left[\cosh(\xi t_{sum}) - \varphi_{n(i+1)}(\xi)\sinh(\xi t_{sum})\right] \bullet \sinh(\xi t_{sum})}{\left[\cosh(\xi t_{sum}) - \varphi_{n(i+1)}(\xi)\sinh(\xi t_{sum})\right] \bullet \cosh(\xi t_{sum}) + \kappa\left[-\sin h(\xi t_{sum}) + \varphi_{n(i+1)}(\xi)\cosh(\xi t_{sum})\right] \bullet \sinh(\xi t_{sum})}$$

(40)

where $\varphi_{ni}(\xi)$ is the Fourier coefficient of the ith layer in the negative direction. t_{nsum} represents the total thickness of all structures below the chip and $\kappa = k_{n(i+1)}/k_{ni}$.

$$A_{i.pj} = A_{i.p(j-1)}\frac{\cosh(\xi t_{psumi}) + \varphi_{p(i-1)}(\xi)\sinh(\xi t_{psumi})}{\cosh(\xi t_{psumi}) + \varphi_{pi}(\xi)\sinh(\xi t_{psumi})}$$

(41)

$$A_{i.nj} = A_{i.n(j-1)}\frac{\cosh(\xi t_{nsumi}) + \varphi_{n(i-1)}(\xi)\sinh(\xi t_{nsumi})}{\cosh(\xi t_{nsumi}) + \varphi_{ni}(\xi)\sinh(\xi t_{nsumi})}$$

(42)

where $A_{i.pj}$ represents the value of A_i (i = 1, 2 and 3) in the analytic solution of the jth layer in the positive direction. $A_{i.nj}$ represents the value of A_i (i = 1, 2 and 3) in the analytic solution of the jth layer in the negative direction.

As for the power distribution in the multiples layers structure, it is similar to the two-layer structure. Both are assigned based on the thermal resistance of the two sides as shown in [Eq. (25)]. $R_{th.p}$ represent the sum of the thermal resistance in the positive direction. $R_{th.n}$ represent the sum of the thermal resistance in the negative direction. The junction temperature is solved at the chip level regardless of the number of layers in the structure. Therefore, the analytical parameters [Eq. (17)] - [Eq. (25)] for the calculation of the junction temperature in a two-layer structure are also applicable to the calculation of the thermal resistance in a multilayer structure.

Therefore, the theoretical model of double-sided heat dissipation was developed, and the temperature distribution at any position can be calculated by using the aforementioned numerical model.

3. Numerical model solution for the FOPLP structure

Fig. 4 shows the double-sided heat dissipation of both SiC MOSFET FOPLP and Si MOSFET FOPLP structures. The thermal properties of components used in the FOPLP structures are listed in Table 1. Both FOPLPs were composed of MOSFET die, redistribution layer (RDL), solder, solder pad, and molding. Source and gate pads of die were connected to corresponding solder pads through RDL. The difference existed in two aspects except for the material characteristics. First, a copper heat sink was missing on the top surface of the Si device. Second, an additional FR-4 molding layer was present above the internal RDL in the Si device. During the numerical solving, simplifying the model to a regular rectangular block stacking structure with the same cross-sectional area is critical. The radiator, plastic sealing layer, solder, and substrate are included in the model according to the actual thickness of the structure. In the RDL layer, both copper materials and molding materials are present for electrical connections, insulation, and mechanical support. Therefore, the material parameters of this part should be re-identified.

Fig. 5 describes the detailed thermal resistance model of RDL layer. Considering a via or molding around a via as a cellular structure, each resistor represents a small cellular structure. Combining cellular of the same material in the thermoelectric network reduces the nonhomogeneity layer to two thermal resistances of different materials [Eq. (43)]. and [Eq. (44)] describe the process of merging the cellular thermal resistance. Combining cellular of the same material in the thermoelectric network reduces the non-homogeneity layer to two thermal resistances of different materials The cross-sectional area in the thermal resistance equation is converted into a volume parameter consisting of that cross-section and the thickness of that nonhomogeneity structure. Thus, the equivalent thermal conductivity of the nonhomogeneity layer can be derived by the conversion of the volume fraction.

$$R_{th.comi} = \frac{t_{com}}{k_i A_i} = \frac{t_{com}^2}{k_i V_i}$$

(43)

$$R_{th.com} = \frac{1}{\dfrac{1}{R_{th.m1}} + \dfrac{1}{R_{th.v1}} + ... + \dfrac{1}{R_{th.mi}} + \dfrac{1}{R_{th.vi}}} = \frac{t_{com}^2}{k_m V_m + k_v V_v} = \frac{t_{com}^2}{k_{com} V_{com}}$$

(44)

where the number of vias in the longitudinal direction is *i*. $R_{th.comi}$ represents the hybrid thermal resistance of the *i* th structure in the hybrid structure, $R_{th.com}$ represents the total thermal resistance of the hybrid structure, t_{com} indicates the thickness of this mixing layer, and k_i denotes the thermal conductivity of the *i* th structure. Furthermore, A_i denotes the cross-sectional area of the *i* th structure, V_i is the volume of the *i* th structure, and $R_{th.vi}$ denotes the thermal resistance of the *i* th via. $R_{th.mi}$ denotes the thermal resistance of the *i* th molding structure parallel to the via. Furthermore, k_m and k_v are the thermal conductivities of the molding and via materials,
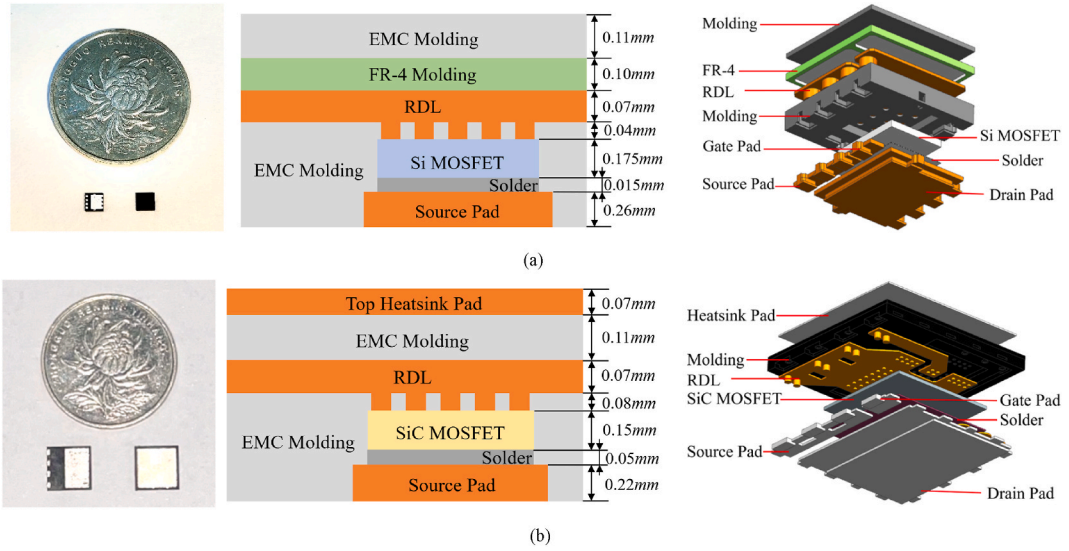
(a)

(b)

Fig. 4. Scheme of the fan-out panel-level packaging (FOPLP) structure [17]: (a) Si MOSFET FOPLP; (b) SiC MOSFET FOPLP.

Table 1
The thermal properties of components used in the FOPLP structures.

Components	Modulus E (GPa)	Poisson ratio v	Coefficient of thermal expansion α (ppm/K)	Thermal conductivity k (W/mK)
SiC MOSFET	400	0.142	5.1	150
Si MOSFET	131	0.3	4.1	124
FR-4	20.4	0.11	12.5	0.38
Cu	110	0.34	18	401
Sn5Sb Solder	49	0.38	31	70
EMC molding	15	0.38	9	1.5

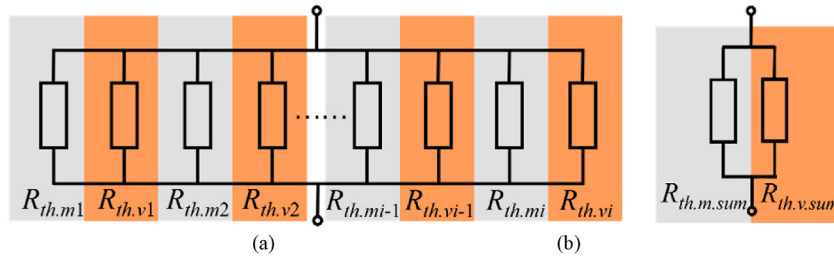(a)   (b)

Fig. 5. (a) Thermal resistance network of **nonhomogeneity** layers;
(b) Schematic of the thermal resistance of the same material after merging and combining.

respectively. V_m and V_v are the volume of the molding and via materials, respectively. $R_{th.m.sum}$ and $R_{th.v.sum}$ are the total thermal conductivities of the molding and via materials, respectively. The bottom substrate is similarly subjected to a volume fraction conversion of its thermal conductivity for precise temperature prediction.

4. Model validation

The FEA of various FOPLP cases is used to verify the accuracy of the numerical calculations.

4.1. Case 1: Si MOSFET FOPLP

In this case, the material component distribution of the Si device in Fig. 4 (a) is used. FOPLP packaging is equivalent to a six-layer structure, with four layers above and two layers below the chip. The package parameters are substituted into the numerical model built above. Si FOPLP adopts a resin with a thermal conductivity of 0.65 W/(m*k). Considering the aforementioned details, the numerical thermal solution of the Si FOPLP with a package size of 3 mm × 3 mm and a chip size of 1.44 mm × 1.9 mm under 10 W heat power is shown in Fig. 6. The numerical method took 2.7 s with 20 Fourier Series superimposed. The Si MOSFET FOPLP model was imported in COMSOL FEA software. During the simulation, the chip was set as a heat source. The top and bottom surfaces were set as convective
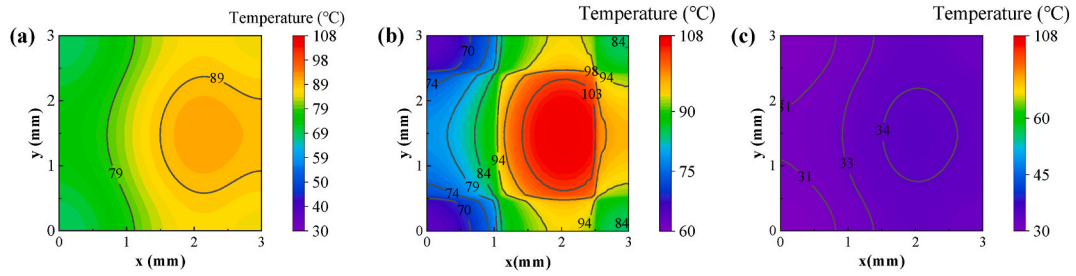
Fig. 6. Numerical prediction of temperature distribution of Si FOPLP (a) on the bottom surface; (b) on the chip layer; (c) on the top surface.
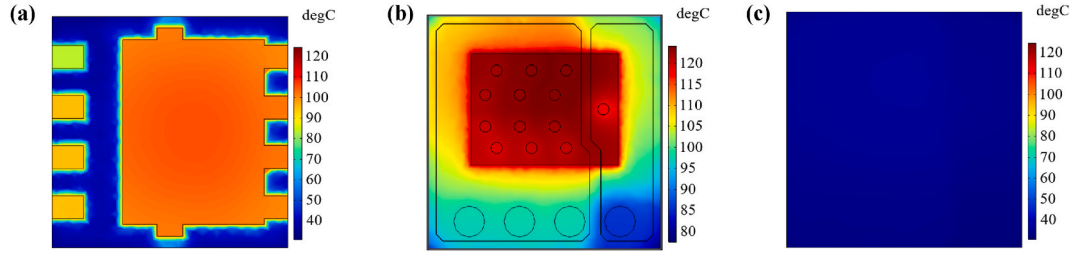

Fig. 7. Unsimplified FEA temperature distribution of Si FOPLP (a) on the bottom surface; (b) on the chip layer; (c) on the top surface.

boundaries. The study object is a 3D model of the actual Si FOPLP structure. 15251 meshes are delineated and 1.58 G of memory is occupied. The FEA method took 5 s to solve the temperature distribution. It is true that numerical modeling is a little faster than finite element calculations. Meanwhile the numerical modeling does not require the construction of a 3D model of the device, which saves time in the analysis process. The use of numerical methods allows the subsequent optimization process to be more specific in terms of the parameters involved. This is not possible with finite element simulation. Fig. 7 shows the FEA results.

For this case, the poor thermal conductivity of the molding material will result in poor heat transfer due to the absence of metal heat sinks on the top surface of the Si FOPLP. This is considered in the numerical calculations. Fig. 8 depicts the Si FOPLP temperature and error distribution for numerical and FEA models. Because a simplified FOPLP model is used in the numerical calculations, identifying the source of the inaccuracy is difficult. Therefore, the simplified model is input to the FEA method to determine whether the numerical derivation or the equivalence of the complex structure is contributing to the error. From the solid line on the graph, the simplified model can reflect the general behavior of the temperature distribution of the original model. However, the temperature step caused by the lateral stacking of various materials cannot be well represented on both the numerical and simplified FEA models. For the bottom side of the structure, molding material is required to electrically isolate and fill the metal gap between the source, drain, and gate pads. Because of the difference in thermal conductivity, the temperature of the large source area becomes notably higher than that of the molding part. The inconsistencies of the package edge material visualized in Fig. 7 (a) can explain the origin of this error. Therefore, the error curve 1 reveals that the numerical errors in the calculation are larger at the edges of the package. The difference from the numerical model exists in the treatment of the chip. Because the numerical model and the simplified FEA model do not consider the chip thickness, the temperature at the chip layer is considered as the temperature of the whole die in the vertical direction. The temperature difference between the simplified and unsimplified models at the chip location in Fig. 8 (g) can be attributed to the solid thickness of the unsimplified chip. As shown in error curve 2, the error curve values are under 15 % overall, and under 5 % at the chip location. Specifically, at the center of the chip, the error is within 2 %. This demonstrates the validity of numerical derivation. The number of expansions of the Fourier series is one of the error sources. For the unsimplified model, the errors in the numerical results are large and within 19 % for the chip position. The overall temperature profile has the same trend, but the lateral stacking of different materials in the actual model is the main reason for this error.

4.2. Case 2: SiC MOSFET FOPLP

The simplified SiC MOSFET FOPLP FEA model was developed to evaluate the accuracy of the numerical model. SiC devices were increased in size. In this case, the package was 8 mm × 8 mm with a die size of 5 mm × 5 mm. Distinct from Si molding materials, epoxy resin with a thermal conductivity of 1.5 W/(m*k) was used for the molding material. Copper was used in the RDL and the metal pads. The material settings were kept consistent with the numerical calculations. With the assumption that the total output power of the chip was 50 W, the numerical temperature distribution of the chip layer was obtained as depicted in Fig. 9(b), with the maximum junction temperature of 77.75 °C. Fig. 9 (c) depicts the temperature distribution on the top surface of SiC FOPLP, and the maximum temperature was 44.36 °C. The temperature distribution on the bottom surface is shown in Fig. 9 (a), and the maximum temperature was 75.96 °C. The calculation time is 4.8 s with 20 Fourier Series superimposed. Fig. 10 shows the resulting temperature distributions at various interfaces based on unsimplified FEA. The temperature at the center of the chip layer was 84.88 °C. The top and bottom surface center
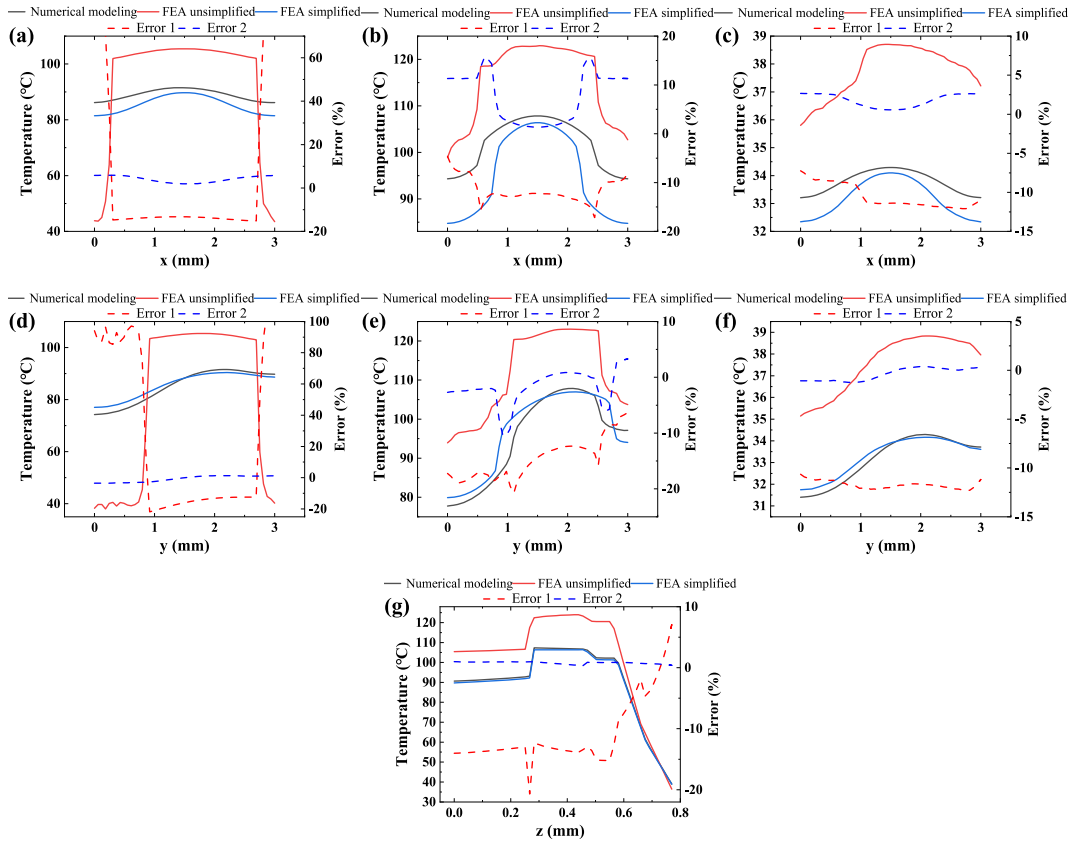
Fig. 8. Si FOPLP temperature and error distribution for numerical model, unsimplified FEA model and simplified FEA model on the bottom layer, the die layer and the top layer of the package with the (a) line paralleled to the x-axis on the bottom layer; (b) line paralleled to the x-axis on the die layer; (c) line paralleled to the x-axis on the top layer; (d) line paralleled to the y-axis on the bottom layer; (e) line paralleled to the y-axis on the die layer; (f) line paralleled to the y-axis on the top layer; (g) line paralleled to the z-axis. Each temperature data is obtained from the x-, y-, and z-axes intercepts through the center of the chip. Error 1 refers to the error between the numerical model and the unsimplified FEA model. Error 2 refers to the error between the numerical model and the simplified FEA model.

temperatures were 47.46 and 83.44 °C, respectively. During the solution process, a total of 28368 meshes are delineated and 1.79 G of memory is occupied. This simulation consumes 11 s.

Fig. 11 shows the data of the truncated line temperature for the three methods in two directions at three locations. The temperature trend of SiC devices was consistent with that of Si. The SiC chip was thinner than the Si chip, but the general thickness of the device and the thickness of the substrate at the bottom of the chip were the same. However, the error at the center of the device reduced to 10 % because of the increase in size. The temperature error at the edges was smaller than that of the Si FOPLP. In the *x*-direction, the unsimplified model exhibited a centrosymmetric temperature distribution because of the uniform material arrangement. A temperature difference of ± 2 °C exists in the numerical model compared with the simplified FEA model. A temperature difference of approximately 7 °C exists between the simplified FEA model and the unsimplified FEA model because of structural differences. In the y-direction, a step temperature decrease existes between the source pad and molding materials on the bottom surface because of the non-uniform electrode arrangement in the structure. In the z-direction, the overall trend of the longitudinal temperature change is consistent for the results from three methods. The error curve 2 drifts within 10 % in each image. The maximum error between the numerical model and the simplified model is 1.98 % on the intercept line parallel to the z-axis through the center of the chip. This error decreased as the number of Fourier series iterations in the numerical calculation increased. This case also validated the consistency in describing the temperature distribution between numerical modeling and FEA modeling.

5. Conclusion

To evaluate the thermal performance of double-sided heat sink power modules quickly, a numerical heat conduction model was constructed to solve the double-sided heat dissipation of FOPLP. The model could be adjusted to the size and the characteristics of the structure material. Both Si FOPLP and SiC FOPLP cases validated the proposed model. In the numerical model of double-sided heat dissipation with multi-material vertical stacking, the temperature at each location can well reflect the actual temperature data in a single and uniform material distribution of each layer. The simplified FEA model and the proposed model revealed strong consistency within an acceptable error of 15 % horizontally and 2 % vertically. A larger error occurred between the unsimplified FEA model and the proposed model. This phenomenon could be attributed to the longitudinal interleaving of various materials in the unsimplified FEA
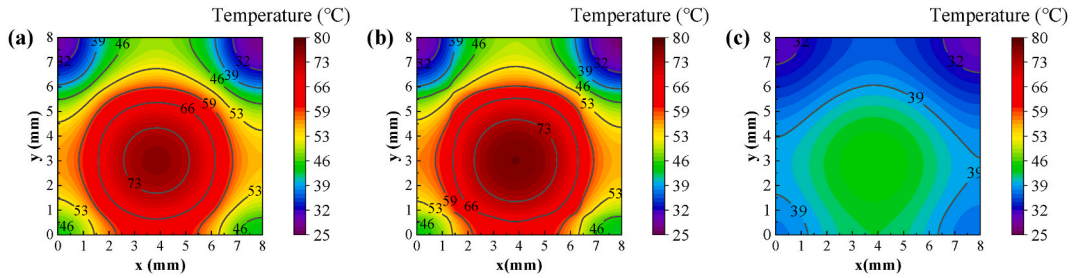
Fig. 9. Numerical prediction of temperature distribution of SiC FOPLP (a) on the bottom surface; (b) on the chip layer; (c) on the top surface.
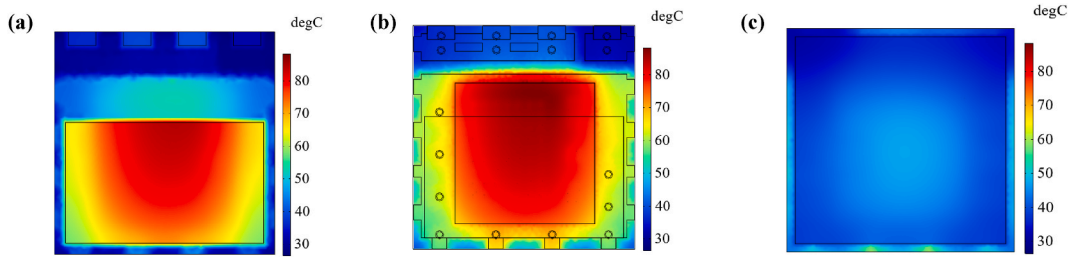

Fig. 10. Unsimplified FEA temperature distribution of SiC FOPLP (a) on the bottom surface; (b) on the chip layer; (c) on the top surface.
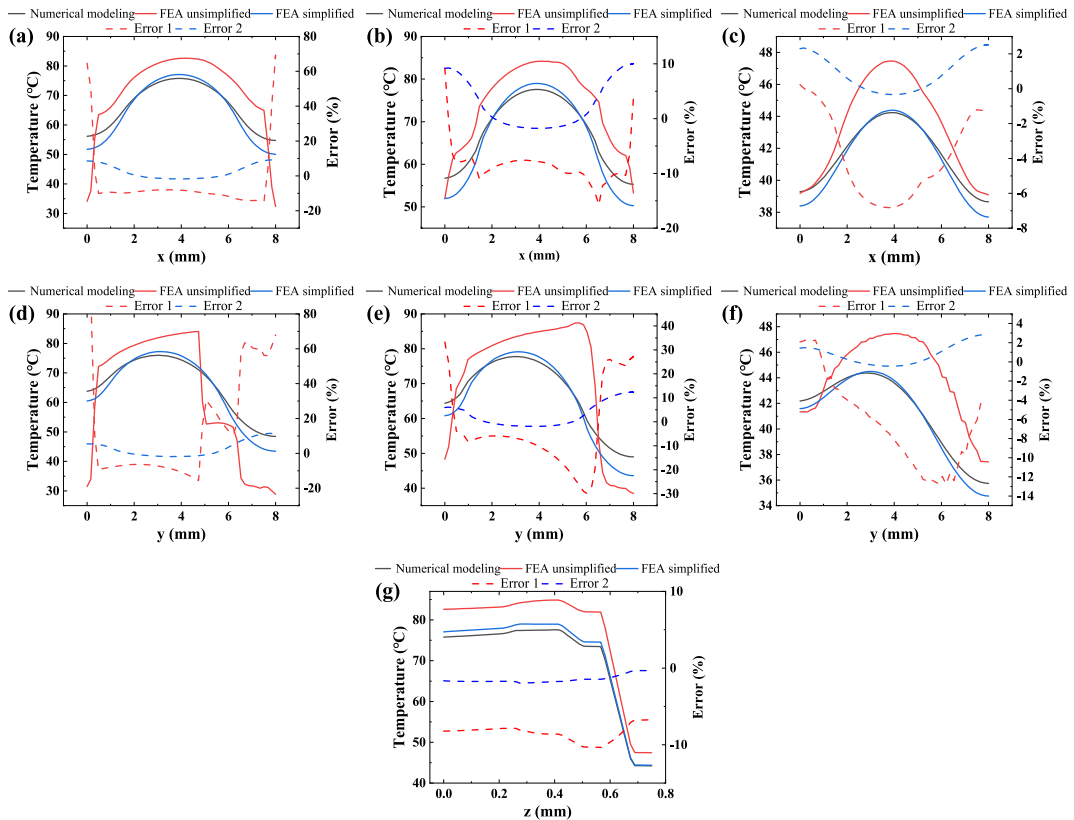

Fig. 11. SiC FOPLP temperature and error distribution for numerical model, unsimplified FEA model and simplified FEA model on the bottom layer, the die layer and the top layer of the package with the (a) line paralleled to the x-axis on the bottom layer; (b) line paralleled to the x-axis on the die layer; (c) line paralleled to the x-axis on the top layer; (d) line paralleled to the y-axis on the bottom layer; (e) line paralleled to the y-axis on the die layer; (f) line paralleled to the y-axis on the top layer; (g) line paralleled to the z-axis. Each temperature data is taken from the x-, y-, and z-axes intercepts through the center of the chip. Error 1 refers to the error between the numerical model and unsimplified FEA model. Error 2 refers to the error between the numerical model and simplified FEA model.

model. The numerical model proposed in this paper can be used for the investigation of rapid design iterations for the electro–thermal optimization of multilayer structures.

Author statement

Wenyu Li: Experiments, data collection and analysis; writing—original draft preparation.
Wei Chen: Simulation and analysis; writing—review and editing.
Jing Jiang: Sample preparation.
Hongyu Tang: Technical supports on simulation; writing—review and editing.
Guoqi Zhang: Supervision.
Jiajie Fan: Conceptualization; methodology; writing—review and editing; project administration; funding acquisition; supervision.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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References

[1] F. Hou, W. Wang, L. Cao, J. Li, M. Su, T. Lin, G. Zhang, B. Ferreira, Review of packaging schemes for power module, IEEE J. Emerg. Selected Topic. Power Electron. 8 (2020) 223–238, https://doi.org/10.1109/JESTPE.2019.2947645.

[2] J. Chen, X. Du, Q. Luo, X. Zhang, P. Sun, L. Zhou, A review of switching oscillations of wide bandgap semiconductor devices, IEEE Trans. Power Electron. 35 (2020) 13182–13199, https://doi.org/10.1109/TPEL.2020.2995778.

[3] X. Zhong, X. Wu, W. Zhou, K. Sheng, An all-SiC high-frequency boost DC-DC converter operating at 320 degrees C junction temperature, IEEE Trans. Power Electron. 29 (2014) 5091–5096, https://doi.org/10.1109/TPEL.2014.2311800.

[4] R. Kibushi, T. Hatakeyama, K. Yuki, N. Unno, M. Ishizuka, IEEE, Comparison of Thermal Properties between Si and SiC Power MOSFET Using Electro-Thermal Analysis, 2017, pp. 188–192.

[5] SiC MOSFET Datasheet, ROHM Semiconductor, 2021. https://www.rohm.com/datasheet.

[6] P. Gorecki, M. Mysliwiec, K. Gorecki, R. Kisiel, Influence of packaging processes and temperature on characteristics of Schottky diodes made of SiC, IEEE Trans. Compon. Packag. Manuf. Technol. 9 (2019) 633–641, https://doi.org/10.1109/TCPMT.2019.2894970.

[7] F. Pourfattah, M. Sabzpooshani, Thermal management of a power electronic module employing a novel multi-micro nozzle liquid-based cooling system: a numerical study, Int. J. Heat Mass Tran. 147 (2020), 118928, https://doi.org/10.1016/j.ijheatmasstransfer.2019.118928.

[8] X. Jiang, J. Wang, J. Lu, J. Chen, X. Yang, Z. Li, C. Tu, Z. Shen, Failure modes and mechanism analysis of SiC MOSFET under short-circuit conditions, Microelectron. Reliab. 88–90 (2018) 593–597, https://doi.org/10.1016/j.microrel.2018.07.101.

[9] J. An, M. Namai, H. Yano, N. Iwamuro, Investigation of robustness capability of-730 V P-channel vertical SiC power MOSFET for complementary inverter applications, IEEE Trans. Electron. Dev. 64 (2017) 4219–4225, https://doi.org/10.1109/TED.2017.2742542.

[10] Y. Chen, B. Li, X. Wang, Y. Yan, Y. Wang, F. Qi, Investigation of heat transfer and thermal management system integrated with vapour chamber for IGBT power module, Therm. Sci. Eng. Prog. 10 (2019) 73–81, https://doi.org/10.1016/j.tsep.2019.01.007.

[11] H. Liu, J. Yu, R. Wang, Dynamic compact thermal models for skin temperature prediction of portable electronic devices based on convolution and fitting methods, Int. J. Heat Mass Tran. 210 (2023), 124170, https://doi.org/10.1016/j.ijheatmasstransfer.2023.124170.

[12] T. An, R. Zhou, F. Qin, Y. Dai, Y. Gong, P. Chen, Comparative study of the parameter acquisition methods for the cauer thermal network model of an IGBT module, Electronics 12 (2023), https://doi.org/10.3390/electronics12071650.

[13] R. Wu, T. Hong, Q. Cheng, H. Zou, Y. Fan, X. Luo, Thermal modeling and comparative analysis of jet impingement liquid cooling for high power electronics, Int. J. Heat Mass Tran. 137 (2019) 42–51, https://doi.org/10.1016/j.ijheatmasstransfer.2019.03.112.

[14] C. Ding, H. Liu, K. Ngo, R. Burgos, G. Lu, A double-side cooled SiC MOSFET power module with sintered-silver interposers: I-design, simulation, fabrication, and performance characterization, IEEE Trans. Power Electron. 36 (2021) 11672–11680, https://doi.org/10.1109/TPEL.2021.3070326.

[15] F. Hou, W. Wang, R. Ma, Y. Li, Z. Han, M. Su, J. Li, Z. Yu, Y. Song, Q. Wang, M. Chen, L. Cao, G. Zhang, B. Ferreira, Fan-out panel-level PCB-embedded SiC power MOSFETs packaging, IEEE J. Emerg. Selected Topic. Power Electron. 8 (2020) 367–380, https://doi.org/10.1109/JESTPE.2019.2952238.

[16] G. Regnat, P.-O. Jeannin, G. Lefevre, J. Ewanchuk, D. Frey, S. Mollov, J.-P. Ferrieux, IEEE, Silicon Carbide Power Chip on Chip Module Based on Embedded Die Technology with Paralleled Dies, 2015, pp. 4913–4919.

[17] W. Chen, J. Jiang, A. Meda, M. Ibrahim, G. Zhang, J. Fan, A thin and low-inductance 1200 V SiC MOSFET fan-out panel-level packaging with thermal cycling reliability evaluation, IEEE Trans. Electron. Dev. (2023), https://doi.org/10.1109/TED.2023.3263150.

[18] Z. Wang, W. Qiao, A physics-based improved cauer-type thermal equivalent circuit for IGBT modules, IEEE Trans. Power Electron. 31 (2016) 6781–6786, https://doi.org/10.1109/TPEL.2016.2539208.

[19] M. Iachello, V. De Luca, G. Petrone, N. Testa, L. Fortuna, G. Cammarata, S. Graziani, M. Frasca, Lumped parameter modeling for thermal characterization of high-power modules, IEEE Trans. Compon. Packag. Manuf. Technol. 4 (2014) 1613–1623, https://doi.org/10.1109/TCPMT.2014.2353695.

[20] H. Fu, J. Chen, H. Wang, Z. Liu, H. Sorensen, A. Bahman, 3-D-Lumped thermal network model for the reliability analysis of fan-cooled plateplate-fin heatsink, IEEE J. Emerg. Selected Topic. Power Electron. 11 (2023) 3480–3491, https://doi.org/10.1109/JESTPE.2023.3237717.

[21] J. Li, A. Castellazzi, M.A. Eleffendi, E. Gurpinar, C.M. Johnson, L. Mills, A physical RC network model for electrothermal analysis of a multichip SiC power module, IEEE Trans. Power Electron. 33 (2018) 2494–2508, https://doi.org/10.1109/TPEL.2017.2697959.

[22] Mingyao Ma, Weisheng Guo, Xuesong Yan, Shuying Yang, Wenjie Chen, Guoqing Cai, Compact thermal network model for thermal analysis of power modules in electric vehicle, Proc. Chin. Soc. Electr. Eng. 40 (2020) 5796–5804.

[23] A. Delouei, A. Emamian, H. Sajjadi, M. Atashafrooz, Y. Li, L. Wang, D. Jing, G. Xie, A comprehensive review on multi-dimensional heat conduction of multi-layer and composite structures: analytical solutions, J. Therm. Sci. 30 (2021) 1875–1907, https://doi.org/10.1007/s11630-021-1517-1.

[24] Y. Muzychka, J. Culham, M. Yovanovich, Thermal spreading resistance of eccentric heat sources on rectangular flux channels, J. Electron. Packag. 125 (2003) 178–185, https://doi.org/10.1115/1.1568125.

[25] D. Chen, T. Chen, P. Yang, Y. Lai, Thermal resistance of side by side multi-chip package: thermal mode analysis, Microelectron. Reliab. 55 (2015) 822–831, https://doi.org/10.1016/j.microrel.2015.02.016.

[26] J. Geer, A. Desai, B. Sammakia, Heat conduction in multilayered rectangular domains, J. Electron. Packag. 129 (2007) 440–451, https://doi.org/10.1115/1.2804094.

[27] A.N. Desai, A. Gunjal, V.K. Singh, Numerical investigations of fin efficacy for phase change material (PCM) based thermal control module, Int. J. Heat Mass Tran. 147 (2020), 118855, https://doi.org/10.1016/j.ijheatmasstransfer.2019.118855.

[28] K.R. Choudhury, D.J. Rogers, Steady-state thermal modeling of a power module: an N-layer fourier approach, IEEE Trans. Power Electron. 34 (2019) 1500–1508, https://doi.org/10.1109/TPEL.2018.2828439.

[29] K. Wang, Z. Pan, An analytical model for steady-state and transient temperature fields in 3-D integrated circuits, IEEE Trans. Compon. Packag. Manuf. Technol. 6 (2016) 1028–1041, https://doi.org/10.1109/TCPMT.2016.2574897.

[30] H.-Y. Tang, H.-Y. Ye, X.-P. Chen, C. Qian, X.-J. Fan, G.-Q. Zhang, Numerical thermal analysis and optimization of multi-chip LED module using response surface methodology and genetic algorithm, IEEE Access 5 (2017) 16459–16468, https://doi.org/10.1109/ACCESS.2017.2737638.

[31] L. Zhou, M. Parhizi, A. Jain, Theoretical modeling of heat transfer in a multilayer rectangular body with spatially-varying convective heat transfer boundary condition, Int. J. Therm. Sci. 170 (2021), https://doi.org/10.1016/j.ijthermalsci.2021.107156.

[32] S. Rangarajan, Y. Hadad, L. Choobineh, B. Sammakia, ASME, Optimal Arrangement of Multiple Heat Sources in Vertically Stacked Two-Layer 3-D IC Using Genetic Algorithm, 2020.

[33] A. Jakani, R. Sommet, F. Simbelie, J. Nallatamby, Understanding the thermal time constants of GaN HEMTs through model order reduction technique, Electronics 10 (2021), https://doi.org/10.3390/electronics10243138.

[34] L. Choobineh, A. Jain, Determination of temperature distribution in three-dimensional integrated circuits (3D ICs) with unequally-sized die, Appl. Therm. Eng. 56 (2013) 176–184, https://doi.org/10.1016/j.applthermaleng.2013.03.006.

[35] B. Partovi, H. Ahmadikia, M. Mosharaf-Dehkordi, Analytical and numerical temperature distribution in a 3-D triple-layer skin tissue subjected to a multi-point laser beam, J. Eng. Math. 131 (2021), https://doi.org/10.1007/s10665-021-10185-5.