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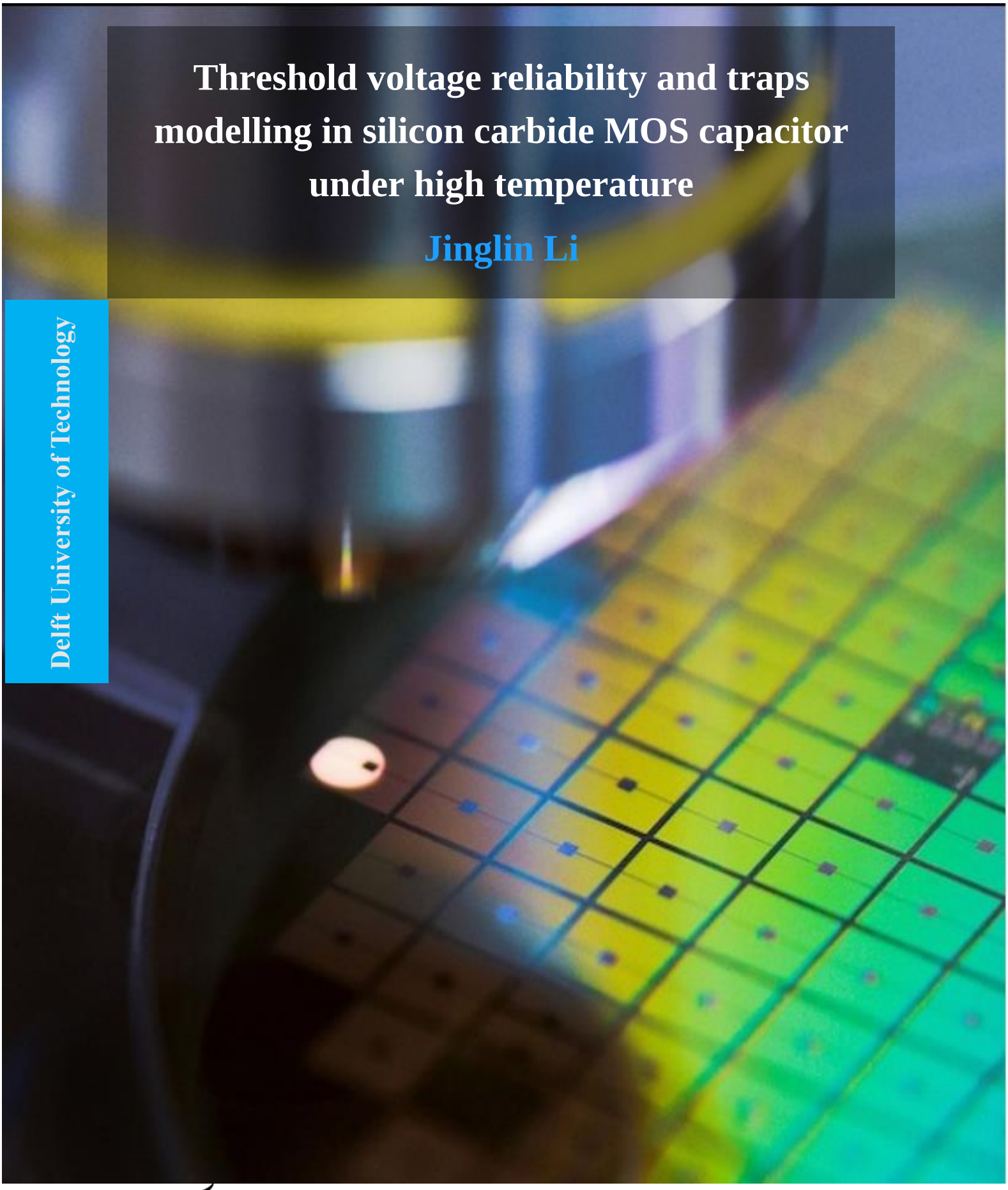

TU Delft

Threshold voltage reliability and traps modelling in silicon carbide MOS capacitor under high temperature

by

Jinglin Li

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Abstract

To extend Moore's law, silicon carbide devices attend the researcher's attention due to their irreplaceable advantages such as high critical breakdown electrical field, wide bandgap and excellent thermal conductivity without sacrificing too much charge carrier mobility. However, the defects on the SiC-oxide interface degrades the performance of the device and even get worse at high temperature, such as the threshold voltage shifting problems, limiting the design of the integrated circuits. The thesis models, characterise, analyses, measures and extracts the traps of SiC MOSCAP, to understand the trapped charge transportation and unreliability mechanism under high temperature.

Effectively using SiC materials necessitates the need to understand the physical properties itself. Due to the large bandgap, the inversion layer cannot be observable in low frequency C-V measurement. The electrical field, space charge region, surface potential and C-V curve in SiC devices all differ from Si devices. More importantly, the trapped charges fluctuate the surface potential of the SiC devices. To give insight into the mechanism governing the trapped charges, the mathematical solution of the trapped charges in the whole bandgap is solved.

To be specific, the trap behaviour at a single energy level is then followed. A nonzero transient current is generated due only to the capture and release of the trapped charges when the equilibrium condition is broken. The trapped charges with high energy are thermalized and an equivalent admittance is obtained which further be split into a capacitance and a conductance.

Rising temperature activates the dopant atoms that are not ionised, and the Fermi level shifts towards the midband. The variation of equivalent circuit components and physical parameters responds to the temperature. High temperature expands the SiC crystal and the trapped charges are easy to receive energy from phonons so that the interaction between traps and the conduction band is enhanced and more empty states are waiting for the recombination of the charge carriers.

Preface

The thesis is concerned with the physical modelling and characterisation of the near interfacial traps in silicon carbide devices. From perplexity to familiarity, I will not forget the nights in the library, the time in the measurement laboratory and the leisure time at weekends riding bike in Delfseland. For the moment, I am grateful to all of you who help me to finish the research.

I wish to express my thanks to Prof. Kouchi Zhang and Prof. P. M. Sarro who provided a wonderful place and enthusiastic atmosphere for me to explore. In particular, I would like to express my gratitude to my supervisor Dr. S. Vollebregt, for his guidance, encouragement and constructive ideas about how to characterise the interface. He also saved my life when I struggled in finding a “non-existent” inversion layer and the maximum point from the conductance curve without removing oxide capacitance. I am especially indebted to my daily supervisors Yaqian Zhang and J. Romijn for providing the moment I felt welcomed, inspired and assisted abundantly. Also, it is a pleasure to acknowledge F. Simjanoski who taught and trained me how to use the probe stations.

Thanks are also expressed to Jiarui Mo, who discussed the MOS physics with me, read the manuscript and opened the door for me every Saturday. In addition, I also wish to thank Pengyuan Su who checked the presentation slides and rehearsal for my presentation. The hospitality of my friends such as J. He, Y. Shen, Q. Lu, J. Gu and H. Guan, who also helped me to create new ideas and regained the confidence to move forward. Finally, I wish especially to thank my parents and my family for their support and assistance in various ways.

Jinglin Li

10/10/2022

Abbreviations and Symbols

N_A (N_D)	Acceptor (donor) atoms concentration at substrate, for complete ionisation
N_c (N_v)	Available states at conduction (valance) band edge
σ	Band tail decay energy
E_g	Bandgap
ΔC	Capacitance gap induced by interfacial traps
C_{it}	Capacitance induced by traps
G_{it}	Conductance induced by interfacial traps
C_{HF} (C_{LF})	C-V measurement under high (low) frequency
L_D	Debye length
C_s	Depletion capacitance
W_{dep}	Depletion region width
$F(x)$	Electrical field at position x
$n_n(x)$	Electron concentration at position x
e_n (c_n)	Electron emission (capture) cross section
φ_{FB}	Fermi potential
V_{FB}	Flat band voltage
GaN	Gallium nitride
p_{p0} (n_{n0})	Hole (electron) concentration in substrate
N_A^- (N_D^-)	Incomplete ionised concentration for acceptor (donor) atoms
D_{it}	Interfacial trap density
p_i (n_i)	Intrinsic hole (electron) concentration
$\tau(E,x)$	Lifetime of the trapped charges at energy level E and position x
Δf (Δn)	Occupancy probability (electron concentration) variation
$f(E,T)$	Occupancy probability at energy level E and temperature T
$\varphi_p(x)$	Potential drop at position x
SiC	Silicon carbide
Q_s	Space charge density
A	Surface area of the sample
φ_s	Surface potential, band bending at surface
i_n	Transient current induced by trap capture and release
D_{edge}	Trap density near the band edge
Q_{it}	Trapped charge density

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1. Introduction

Moore's law has successfully predicted, guided and stated the trend of semiconductor development: the density of transistors in integrated circuits doubles around every two years [1]. However, it comes to the end and the limitation of silicon makes the transistor cannot be further scaled down. To extend Moore's law, a new trend "More than Moore" nowadays requires a new material to tolerant high electrical field and low leakage current [2] and improve the functionality of electronic instrumentations. Wide bandgap materials with fast switch speed and low on-resistance [3], such as gallium nitride (GaN) and silicon carbide (SiC), are extensively researched. However, the growth of high quality and large size of GaN seed crystal is challenging, since more than half an hour is spent heating metal gallium in air reaction, making GaN products uneconomical. As an alternative and emerging material, the SiC has irreplaceable advantages, such as ease of fabrication, high critical breakdown electrical field and excellent thermal conductivity, which successfully resolves the abovementioned problems and suits for high voltage and high temperature applications.

1.1 The silicon carbide and polytypism

The SiC devices overcome the limitations of conventional silicon materials, and more importantly, the combination of carbon atoms and silicon atoms in the spatial structure of the SiC lattice determines its electrical property. The commonly used polymorphs of silicon carbide are 3C-SiC, 4H-SiC and 6H-SiC. To begin with, a SiC cell with tetrahedron structure is established in Fig. 1.1 (a), where four carbon atoms locate at vertexes and a silicon atom is in the centre. The bond between the central silicon atom and the nearest carbon atom is 1.89Å and the distance between nearby carbon atoms is 3.08Å [5]. The arrangement of tetrahedron cells in 1-D direction forms double stack layers. Fig. 1.1 (b) gives the possible stacking sequences of SiC crystal cells, with three available positions. The 3C-SiC structure is defined where silicon atoms are all parallel (Cubic Zincblende). On the contrary, the silicon atoms in 6H-SiC and 4H-SiC are non-parallel stacking (Hexagonal), and both of them are named by their stacking periodic.

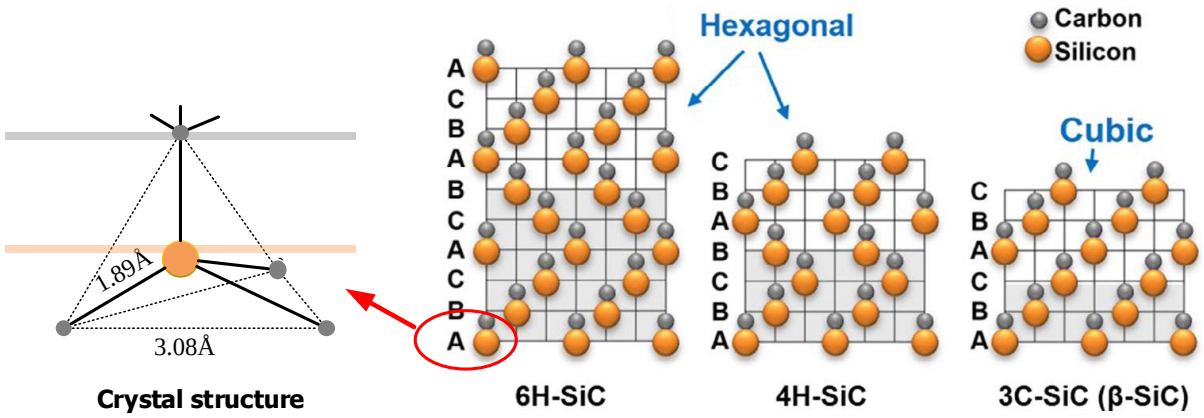

Fig. 1.1. (a) SiC crystal cell; (b) structures of 6H-SiC, 4H-SiC and 3C-SiC [6].

Table. 1.1 reports and compares the material properties of Si, GaN, 3C-SiC, 4H-SiC and 6H-SiC. Benefiting from the high energy Si-C bond, the SiC and its polytypism provide wide bandgap. Because of that, the SiC crystal structures keep stable even at extreme temperature and make it possible for high temperature applications.

The potential of silicon is constrained, especially under harsh environment. So far for the SiC, the large ionisation energy of electron-hole pairs due to the wide bandgap effectively increases the critical breakdown electrical field in SiC, which is approximately 10 times that of silicon. A large critical electrical field allows for a thinner and higher doped junction, effectively reducing on-resistance and power dissipation and increasing the switching frequency.

The physical properties of SiC also suit the application at high temperature. The thermal conductance of SiC is three times that of Si so that the self-generated heat in SiC can be efficiently removed, releasing the cooling systems. The saturation velocity in SiC is doubled, thus the switching frequency is correspondingly improved. Because of the irreplaceable advantages, SiC devices now become ideal alternatives to conventional silicon devices.

Other wide bandgap compound semiconductors, such as GaN, are also rapidly developed. The fabrication of SiC is similar to Si, whereas growing high quality GaN crystal is time-consuming. In addition, an excellent insulator layer (silicon dioxide) can be automatically formed by thermal oxidation in SiC, which is the ease of design of the MOSFET device. However, for GaN devices, not only did the GaN substrate needs to grow on a silicon base, but also an extra aluminium oxide layer should be deposited to form the insulator layer.

Table. 1.1. Properties of 4H-SiC comparing with others at room temperature [7].

	Si	GaN	3C-SiC	4H-SiC	6H-SiC
Intrinsic carrier conc. [cm^{-3}]	1.5×10^{10}	2×10^{-10}	6.9	8.2×10^{-9}	2.3×10^{-6}
Bandgap [eV]	1.12	3.39	2.23	3.26	3.00
Thermal conductivity [$Wcm^{-1}K^{-1}$]	1.5	1.3	4.9	4.9	4.9
Critical electrical field [MV/cm]	0.3	5	1.2	3	2.4
Electron mobility [$cm^2V^{-1}s^{-1}$]	1350	800	1000	1140	600
Hole mobility [$cm^2V^{-1}s^{-1}$]	480	350	40	120	80
Saturation velocity [$10^5 m/s$]	1	2.2	2	2	2

However, so far the mechanism of SiC transistors reliability problems has not been fully investigated, especially at high temperatures. Because of that, the fluctuation of electrical characteristics such as threshold voltage, attract the researchers' attention. To improve the performance of SiC electronics, the degradation of SiC devices at high temperature necessitates the need to understand the charge mechanisms behind them. The following summarises the state-of-the-art research on SiC high temperature reliabilities.

1.2 High temperature reliability problems on silicon carbide devices

Research and applications in SiC devices originated from 1997 when P. M. Shenoy firstly designed SiC UMOSFET (U-shaped trench MOSFET) with 350V blocking voltage and $18\text{m}\Omega\cdot\text{cm}^2$ on-resistance [8]. The interface quality, channel mobility and operation voltage were being improved continuously from that time. In 1997, L.A. Lipkin reported N_2O as oxidant during thermal oxidation and effectively reduced interface states at the band edge [9]. In addition, the authors in [10] designed a 4H-SiC vertical MOSFET reducing the on-resistance to $8.5\text{m}\Omega\cdot\text{cm}^2$ in 2004. The SiC products were commercially manufactured, and it is reported in 2011 in [11] that a high voltage (up to 1500V) and low on-resistance MOSFET ($3.9\text{m}\Omega\cdot\text{cm}^2$) were achieved by S. Ryu in Cree, a world leading company in SiC research. SiC devices gained large acceptance and attention in DC-DC converters [12], charging systems and electrical vehicles [13].

Although various SiC devices and products were developed and investigated intensively, the integrated circuit design in SiC is still challenging and only a few of them are commercially available. Although the SiC MOSFETs can operate at 300°C [14], the reliability in ultra-high temperature (500°C) and high electrical field cannot be guaranteed. Two main problems at high temperature are well recognised: low channel mobility due to interface quality and device parameter drift.

At present, the interface trap density in the SiC/SiO_2 system reaches $10^{11}-10^{12}\text{cm}^{-2}/\text{eV}$, whereas the interface trap density in the Si/SiO_2 system is only $10^{10}-10^{9}\text{cm}^{-2}/\text{eV}$ [15]. In thermal oxidation process of SiO_2 from SiC, carbon atoms must be removed, in either CO_2 or CO form. In contrast to thermal oxidation from Si, the carbon atoms are trapped near the interface and form carbon clusters which block the movement of charge carriers [16]. The channel mobility thus is degraded and becomes unstable in high temperature, leading to large on-resistance and reliability problems.

Various literature reported that the device parameters shift in harsh environment, especially for the threshold voltage, which is a critical parameter in both analogue circuits and power switches. To evaluate the degradation, Lelis et al. [17] first measured the transfer characteristics of typical SiC MOSFETs at room temperature, and observed that the SiC device suffers from threshold voltage hysteresis. Accurately measuring the property of the interface traps and parameter shift would give them insight, and several threshold voltage stability tests were performed in [18] and [19] by directly measuring the transfer characteristics. Advanced testing methods and extraction methods, such as the C-V measurement [20], transient current measurement [21] and transient capacitance measurement [22] was performed to determine the hysteresis, interface traps and slow traps, respectively. Although numerous testing methods are available, the currently used testing method such as direct C-V measurement is erratic and underestimates the density of the trap state [20]. Standard testing, parameter extraction and characterisation method still has to be established.

After measurement, the reliability problems necessitate the requirement to understand the mechanism behind it. In the early stage of SiC research, the focus points are the optimisation of channel mobility and device fabrication. The commonly accepted hypothesis includes interfacial traps [23], tunnelling [24] and oxide traps [25] mechanisms. In 2018, the authors in [26] explained the phenomenon of interfacial traps, and they believed that the interface traps can capture the electrons from the conduction band directly, and those charges are trapped causing a nonzero voltage drop. In addition, the analysis proved that the positively charged oxide traps, created by electron emission, would assist the hole tunnelling process [24]. The group of Lelis concentrated on oxide traps induced reliability problems, and his work [25] identified oxygen vacancy (*O*) caused by weak Si-Si bond is the precursor site for the oxide traps. Only 1.14eV activation energy can activate those bonds to oxide traps [25]. For now, although various reliability measurements of threshold voltage at high temperature have been presented, the theoretical explanations of mechanisms are absent and incomplete, and cannot cover the ultra-high temperature.

1.3 Previous work on threshold voltage stability and summary

Various physical models and charge transport mechanisms have been published recently and they reveal that the interface traps and oxide traps were frequently expressed as the core reasons for threshold voltage hysteresis. The authors in [34] explained the phenomenon of threshold voltage hysteresis measurements. Once upward sweeping starts, the Fermi level is driven into the non-steady state, and after sufficient observation time when reaching steady states again, a stretch-out of the C-V measurement curve was observed. In [35], the researchers explained detailed behaviour of threshold voltage shift under high electrical stress, and observed a positive shift occurs under positive stress and a negative shift appears when negative stress is applied [35]. In [25], the group of Lelis calculated the minimum activation energy to weak Si-Si bonds, which is $1.14eV$.

Interface traps near the SiC-oxide have been already proven to be the core reason for the threshold voltage instability problem. Therefore, accurately measuring the property of the interface traps and its density within the band would give an insight into charge transportation. Z. Peng et al in 2018 applied integrated C-V measurement to determine interface traps induced threshold voltage shift and C-V curve hysteresis [36]. By dramatically changing the applied voltage, the near interface trapped charge tunnels through the oxide layer, leading to a measurable transient current [24]. H. A. Moghadam et al firstly introduced the transient current method to extract the density of interface traps and trapped charges using an n-type MOS capacitor [21]. Additionally, the capacitance variations are observed by the authors [22] when they applied the transient capacitance method to investigate slow traps near the oxide-semiconductor interface. The MOSCAP was firstly biased at accumulation to charge the slow traps inside, within a certain time interval T_{trap} . Afterwards, the applied voltage is then switched to flat band condition, trigging the de-trapping process. This process causes an observable transient capacitance variation, reflecting the behaviour of the de-trapping process of slow traps.

1.4 Problem formation and research goals

Due to the fact that the mechanism of reliability problems on SiC devices at high temperature is not fully explained, the aim of the thesis will firstly be the modelling of the SiC MOSCAP with non-idealities and compare it with standard Si devices. Based on that, the second research goal is to model the interfacial traps, as the core reason for unreliability, which is required to be methodically modelled and systematically extracted to describe the quality of the semiconductor-oxide interface. Furthermore, another research goal includes the explanation of the high temperature effect and temperature dependency analysis.

1.5 Structure of the thesis

In chapter 2, beginning with ideal MOS capacitor, the interfacial electrical field, space charge and differential capacitance will be clearly calculated. By adding non-idealities, the physical parameters in nonideal SiC devices will be extensively analysed and compared with silicon. In addition, the origination of interfacial traps will be discussed based on the existing literature.

In chapter 3, the mathematical solution of interfacial traps in the whole bandgap will be provided. The results suggest that the electrical properties of traps are temperature dependent. In particular, the characterisation and extraction methods employed to determine the distribution of interfacial traps will be established, and after the comparison, the characterisation accuracy, measurement conditions and extraction errors will be highlighted.

To obtain a deep understanding, a physical model analysing the behaviour of trap states from conservation of energy and equivalent circuit will be covered in chapter 4. Based on Shockley, Hall and Read capture and release theory, the lifetime and trapped charges induced current will be solved. During C-V measurement under certain frequency, this chapter mainly focuses on the response of charge carriers and the mechanism of charge transportation under a sinusoidal small signal. Following the conservation of energy, a nonzero admittance must be introduced and an equivalent circuit considering all trap states in the whole bandgap will be provided.

Afterwards, chapter 5 gives another perspective to understand the charge transport mechanism at high temperature. It presents the behaviour of the band diagram when the system is pushed into non-equilibrium. In particular, the temperature effects including ionisation, Fermi level shift and probability function variation are analysed. Among these discussions, it follows by the variety of circuit components in equivalent circuit derived in chapter 4.

The following chapter 6 will provide experimental evidence of trap behaviour and temperature effects. After COMSOL simulation, the outcomes of the measurements including trap distribution, lifetime analysis and their relation to threshold voltage instability are discussed. Those will be all compared with theoretical analysis for verifications. Finally, in chapter 7, a project summary with both theoretical and experimental results is provided. Future research and application of the project will be used to end the thesis.

2. Metal Oxide Semiconductor (MOS) Devices

Based on the fact that most reliability problems originate from surface conditions, as one of the most useful devices for studying the semiconductor-oxide surface, the metal-oxide-semiconductor (MOS) structure is an irreplaceable tool to investigate electrical property and characterisation. Although the simplest MOS structure is the MOS capacitor (MOSCAP), even if it is not widely used in real-world applications, the modelling and measurement of the MOSCAP is a reliable method to determine the quality of interfaces. The following establishes the information obtained from MOSCAP.

- Flat band voltage and surface potential from oxide interface to semiconductor substrate, V_{FB} and φ_s.
- Doping concentration in the substrate, N_A.
- Space charge distribution Q_s and differential capacitance C_s.
- Interface traps density with respect to energy location in the whole bandgap, $D_{it}(E)$.

An ideal MOSCAP can be considered as a voltage-controlled variable capacitor, whose cross-section in particular, in depletion mode is shown in Fig. 2.1. The fabrication process is shown below: upon $350\mu m$ SiC substrate, the doped regions are formed by n-well and p-well after $1700^{\circ}C$ annealing for 30 minutes. The n-type region is doped by N^+ implantation with the concentration of $5\times10^{15}cm^{-3}$, whereas Al^+ is implanted for the p-type region until reaching the concentration of $10^{16}cm^{-3}$. Thermal oxidation is then followed, resulting in $50nm$ gate oxide and $400nm$ field oxide [27]. The designed circular MOSCAP with radius r has surface area of $A=\pi r^2$, fabricating on $350\mu m/100mm$ 4H-SiC wafer. Starting from standard silicon MOSCAP structures, the real SiC MOSCAP is obtained by adding the non-idealities and presented together to highlight the differences between them.

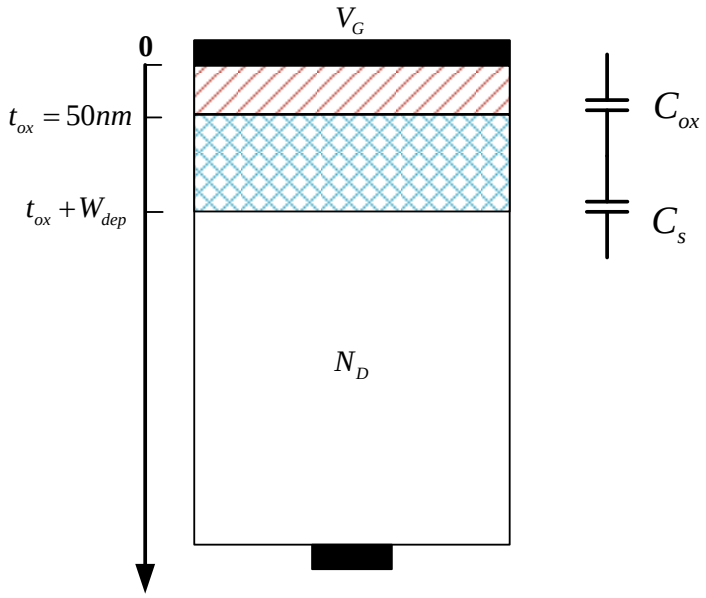

Fig. 2.1. Cross section of MOSCAP structure in depletion region.

2.1 Ideal MOSCAP

Taking n-type substrate MOSCAP as an example, the band diagram at flat band condition (without band bending) is illustrated in Fig. 2.2. Flat band voltage is the voltage that the energy bands are exactly flat all over the substrate. In this case, the ideal MOSCAP reaches this condition without applying gate voltage. Assuming that,

- There is no interface trapped charges nor oxide trapped charges ($D_{it} = 0$).
- The insulator layer is perfect that zero current flows through. In other words, the resistivity of the oxide is infinitely high.
- The gate electrode is regarded as infinitely high conductivity.
- Doping profile is uniform, continuous and fully ionised in substrate.
- The difference between metal work function and semiconductor work function is zero.

$$\varphi_{ms} = \varphi_m - \left(\chi + \frac{E_g}{2q} - \varphi_{FB} \right) = 0\text{eV} \tag{2.1}$$

where φ_m is the electron affinity for polysilicon gate, χ is the electron affinity of 4H-SiC, $E_g = 3.26\text{eV}$ represents the bandgap of SiC and $\varphi_{FB} = 1.41\text{eV}$ stands for the Fermi level in the substrate when doping concentration is $5\times10^{15}\text{cm}^{-3}$. A sample of SiC MOSCAP with n-type substrate are illustrated in Fig. 2.2 with all parameters indicated.

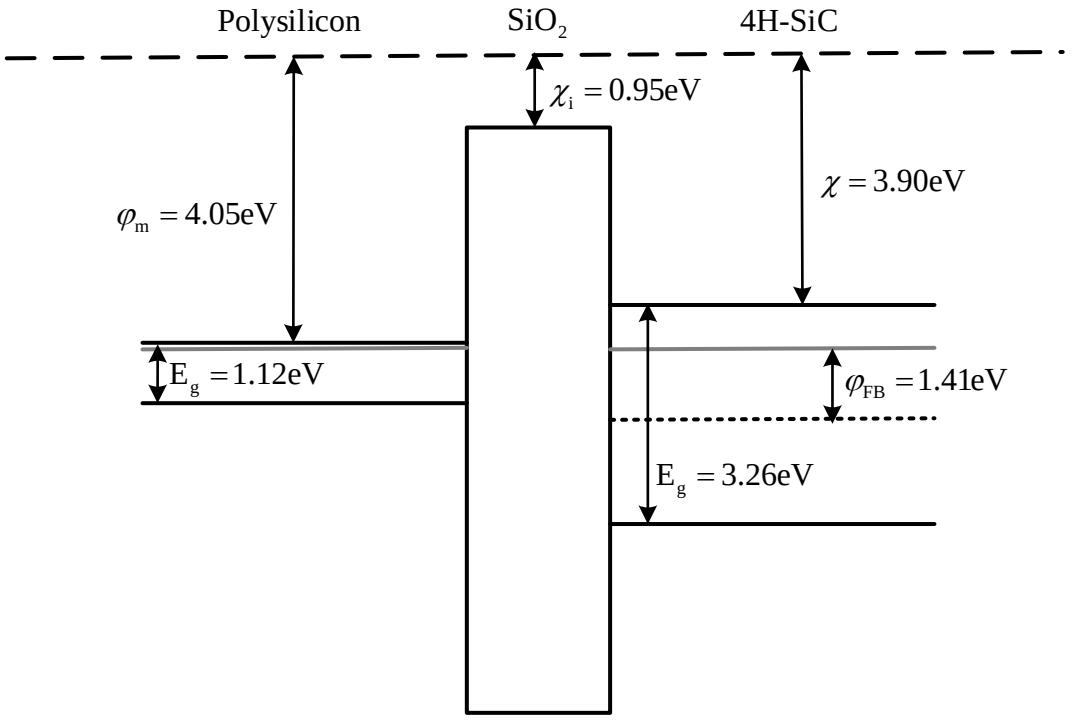

Fig. 2.2. Energy band diagram at flat band condition, with n-type doping concentration of $5\times10^{15}\text{cm}^{-3}$ in substrate and n-type polysilicon gate.

Given midband $E_i = 0.5(E_c + E_v)$ and an n-type substrate MOSCAP, in the case of $V_g > 0$, the majority carrier electrons in n-type substrate accumulates at the interface, causing the band bending of E_i away from Fermi level. On the other hand, when $V_g < 0$, the majority carriers are repelled away to the bulk and the space charges are left alone, resulting in a depletion region. The midband energy level E_i bends to the Fermi level, whose band diagram in depletion is illustrated in Fig. 2.3. The calculated Fermi potential is $\varphi_{FB} = 1.41\text{eV}$ corresponding to the doping concentration of $5\times10^{15}\text{cm}^{-3}$ at room temperature. For -type substrate MOSCAP, the band bending is flipped around.

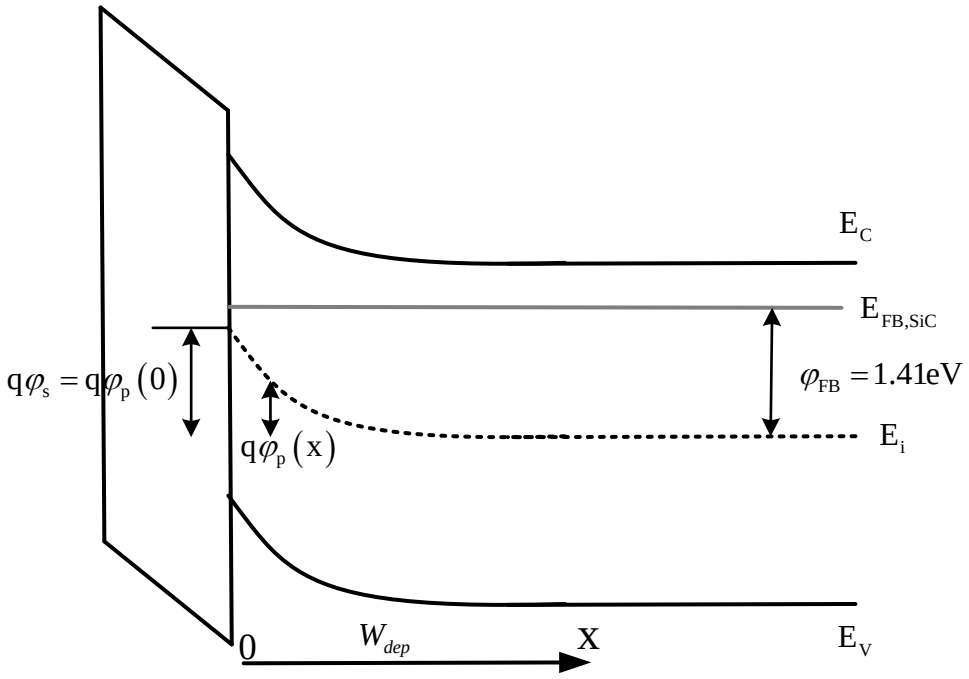

Fig. 2.3. Band diagram of ideal n-type substrate SiC MOSCAP for depletion condition.

Define a potential drop $\varphi_p(x)$ at position x, with respect to the midband potential at infinite far away,

$$\varphi_p(x) = -\frac{E_i(x) - E_i(\infty)}{q} \tag{2.2}$$

From the semiconductor-oxide surface to infinite far away, $\varphi_p(0) = \varphi_s$ is defined as surface potential, which is an indication of band bending, also shown in Fig. 2.3. It is worthwhile to note that the band bending is referring to the interface.

The operational modes of an n-type MOSCAP are classified as follows.

- Accumulation of electrons occurs when $\varphi_s > 0$, band bending downwards near interface.
- Flat band condition occurs at $\varphi_s = 0$.
- Depletion region forms when $-\varphi_{FB} < \varphi_s < 0$, band bending upwards near interface.

In silicon, an inversion layer generates when $\varphi_s < -\varphi_{FB}$, where minorities (holes) dominate in the channel. However, in SiC, the inversion layer is not observable without excess carrier activation. That is because in SiC, the concentration of the intrinsic charge carrier is so low ($n_i = 8\times10^{-9}\,cm^{-3}$) and the minority generation time is so long that the inversion layer cannot be activated by only thermal excitation at room temperature. Due to the large bandgap, the generation and recombination time for electron-hole pairs in SiC is also longer than silicon. The emission time constant for minority carriers is modelled by,

$$\tau = \frac{1}{\sigma_n \nu_{th} N_c}\exp\left(\frac{E_c - E}{kT}\right) \tag{2.3}$$

where σ_n represents the capture cross section, ν_{th} stands for thermal velocity, N_c is effective allowed density of state in conduction band, E_c is the energy at the conduction band edge, k is Boltzmann constant and T represents temperature. Provided SiC parameters that the capture cross section $\sigma_n = 10^{-15}\,cm^{-2}$ and $E_c - E = 1eV$, the emission time at room temperature is approximately $10^5 s$, which is two days long. For this reason, only sufficiently external sources, such as high power and short wavelength of light illumination (50W and below 200nm UV light source) and heating, may help the activation of minority carriers. Due to the limitation of measurement equipment, UV light illumination will not be performed in this project.

The following calculates the electrical field in the substrate at any position x. For an n-type substrate MOSCAP, consider Poisson's equation in one dimension,

$$\frac{d^2\varphi_p(x)}{dx^2} = -\frac{\rho(x)}{\varepsilon_{SiC}} \tag{2.4}$$

where $\varepsilon_{SiC} = 9.7$ is the permittivity of SiC, and the net charge density at position x is,

$$\rho(x) = q\left[N_D^+ - N_A^- + p_p(x) - n_n(x)\right] \tag{2.5}$$

where $q = 1.6\times10^{-19}C$ represents elementary charge, N_D^+ and N_A^- are ionised donors and acceptors, respectively. $p_p(x)$ and $n_n(x)$ stand for the density of freely moved holes and electrons at position x. Taking the neutral region concentration $p_p(\infty)$ and $n_n(\infty)$ infinite far away in the substrate as a reference, the following equations calculate $p_p(x)$ and $n_n(x)$ as a function of potential drop φ_p,

$$p_p(x) = p_p(\infty)\exp\left(-\frac{q\varphi_p(x)}{kT}\right) \tag{2.6}$$

$$n_n(x) = n_n(\infty)\exp\left(\frac{q\varphi_p(x)}{kT}\right) \tag{2.7}$$

where the neutral region concentration $p_p(\infty)$ and $n_n(\infty)$ is controlled by doping concentration. For simplicity, all holes and electrons originate from ionised atoms, which leads to $p_p(\infty) = p_{p0}$ and $n_n(\infty) = n_{n0}$ replacing holes and electrons in substrate infinite far away, respectively. It is straightforward to obtain them,

$$p_{p0} = p_i \exp\left(-\frac{q\varphi_{FB}}{kT}\right) \tag{2.8}$$

$$n_{n0} = n_i \exp\left(\frac{q\varphi_{FB}}{kT}\right) \tag{2.9}$$

where p_i and n_i are the density of intrinsic carriers. Due to the large bandgap, the intrinsic concentration is extremely small compared with silicon. The fermi potential φ_{FB} is controlled by doping concentrations,

$$\varphi_{FB} = \frac{kT}{q}\ln\left(\frac{N_D^+}{n_i}\right) \tag{2.10}$$

To hold charge neutrality at infinitely far in the substrate, zeroing equation (2.5) and combining equation (2.6) (2.7),

$$\rho(+\infty) = 0 \;\Rightarrow\; N_D^+ - N_A^- = n_{n0} - p_{p0} \tag{2.11}$$

Inserting this equation into equation (2.4) gives,

$$\frac{d^2\varphi_p(x)}{dx^2} = -\frac{q}{\varepsilon_{SiC}}\left(n_{n0} - p_{p0} + p_p - n_n\right) \tag{2.12}$$

$$\frac{d^2\varphi_p(x)}{dx^2} = -\frac{q}{\varepsilon_{SiC}}\left[n_{n0} - p_{p0} + p_{p0}\exp\left(-\frac{\varphi_p(x)}{V_t}\right) - n_{n0}\exp\left(\frac{\varphi_p(x)}{V_t}\right)\right] \tag{2.13}$$

Here, thermal voltage $V_t = kT/q$ is used for simplification. The calculation details are shown in Appendix I, and the solution of the electrical field as a function of position x is,

$$F(x) = \pm\frac{\sqrt{2}V_t}{L_D}\sqrt{\frac{p_{p0}}{n_{n0}}\left[\exp\left(\frac{-\varphi_p(x)}{V_t}\right) - \frac{\varphi_p(x)}{V_t} - 1\right] + \left[\exp\left(\frac{\varphi_p(x)}{V_t}\right) - \frac{\varphi_p(x)}{V_t} - 1\right]} \tag{2.14}$$

where $L_D = \sqrt{V_t\varepsilon_{SiC}/qn_{n0}}$ is called the Debye length.

The electrical field pointing right is represented by a positive sign. For a negative biased voltage, negative $\varphi_p(x)$ in Fig. 2.3 gives minus sign $F(x)$. Because of that, the sign function $\mathrm{sgn}(\varphi_p(x))$ can replace "$\pm$" in front in following section for sign conservation.

2.2 Space charge, differential capacitance and surface potential

The electrical field $F(x)$ is a function with respect to position x and minority-majority charge carriers ratio p_{p0}/n_{n0}, which is obtained by equation (2.8) and (2.9) and controlled by doping. Examining $F(x, p_{p0}/n_{n0})$, the electrical field in ideal MOSCAP has two special cases, discussed as follows in detail.

- Wide bandgap semiconductor.

For SiC devices, the inversion layer is not possible at room temperature without extra source, such as light illumination, according to the long generation time in equation (2.3). Another evidence is due to the wide bandgap, the intrinsic carrier concentration compared with doping concentration is negligible, so that $p_{p0}/n_{n0} \to 0$. In that case, taking n-type SiC substrate as an example, it is reasonable to use that as an alternative,

$$F_{SiC}(x,0) = \mathrm{sgn}(\varphi_p(x))\frac{\sqrt{2}kT}{qL_D}\sqrt{\exp\left(\frac{\varphi_p(x)}{V_t}\right) - \frac{\varphi_p(x)}{V_t} - 1} \tag{2.15}$$

where the ratio $p_{p0}/n_{n0} \to 0$ is valid at room temperature.

- Electrical field at oxide-semiconductor interface.

The electrical field at the surface determines the property of the interface. The applied gate voltage controls the surface potential φ_s (band bending), and further influences the electrical field at the interface.

$$F\left(0, \frac{p_{p0}}{n_{n0}}\right) = \mathrm{sgn}(\varphi_s)\frac{\sqrt{2}kT}{qL_D}\sqrt{\frac{p_{p0}}{n_{n0}}\left[\exp\left(-\frac{\varphi_s}{V_t}\right) - \frac{\varphi_s}{V_t} - 1\right] + \left[\exp\left(\frac{\varphi_s}{V_t}\right) - \frac{\varphi_s}{V_t} - 1\right]} \tag{2.16}$$

For SiC devices, similarly,

$$F_{SiC}(0,0) = \mathrm{sgn}(\varphi_s)\frac{\sqrt{2}kT}{qL_D}\sqrt{\exp\left(\frac{\varphi_s}{V_t}\right) - \frac{\varphi_s}{V_t} - 1} \tag{2.17}$$

Based on that, the total space charge per unit area in silicon expressed using Gauss's law is,

$$Q_{s,Si} = -\varepsilon_s F\left(0, \frac{p_{p0}}{n_{n0}}\right) \tag{2.18}$$

Similarly, for SiC, the space charge per unit area turns out to be,

$$Q_{s,SiC} = -\varepsilon_{SiC} F_{SiC}(0,0) \tag{2.19}$$

The following illustrates the space charge density as a function of band bending φ_s. The dashed line is silicon whereas the solid line stands for 4H-SiC. For an n-type substrate, the band bending $\varphi_s > 0$ leads to an exponential increment, according to equation (2.16), which corresponds to the accumulation mode. When band bending is $\varphi_s < 0$, the exponential terms approach 0, and the square root dominates until reaching the "threshold band bending $-2\varphi_{FB}$". For silicon, the inversion layer generates when the exponential term dominates again and $p_{p0} / n_{n0} \approx 10^{-10}$ is eliminated. However, in SiC devices the ratio $p_{p0} / n_{n0} \approx 10^{-47}$ so that the minimum band bending is $\varphi_s \approx 2.814\text{eV}$ to compensate, which is impossible to achieve.

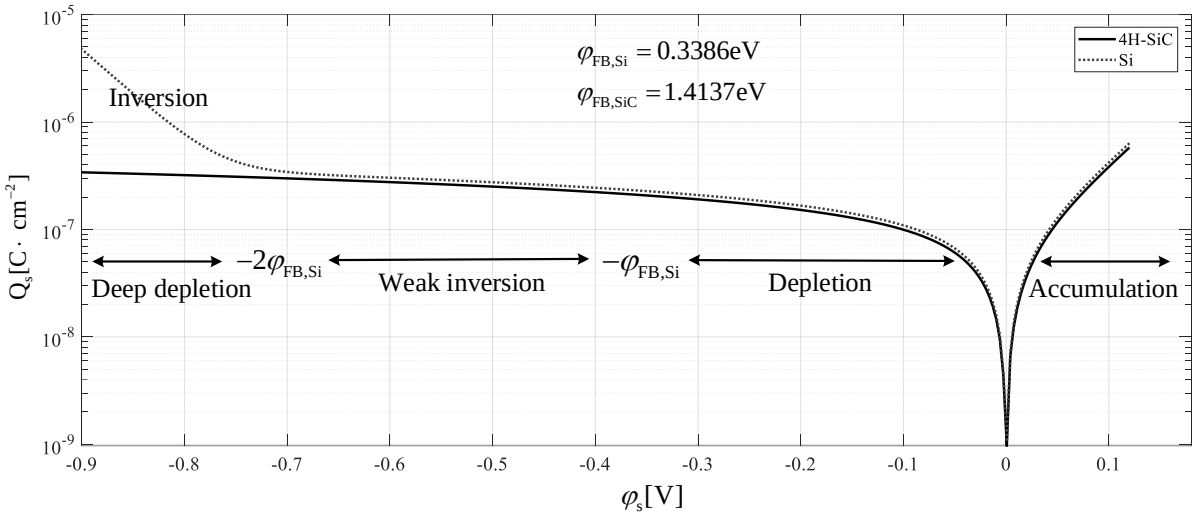

Fig. 2.4. Space charge density as a function of band bending for n-type substrate MOSCAP; Dashed line represents Si, while solid line stands for SiC. The doping concentration at substrate is $5\times10^{15}\text{cm}^{-3}$, and temperature is set to 300K.

Charge motion in a certain region results in a differential capacitance, which can be easily observed by changing the applied voltage. Since capacitance is always positive, charge density should take the absolute value, and taking derivative,

$$C_s = A\frac{d|Q_s|}{d\varphi_s} \tag{2.20}$$

where A is the surface area of the MOSCAP. The observable total capacitance in C-V measurement should take both oxide and differential capacitance into account, so that,

$$C_{tot} = \frac{C_{ox}C_s}{C_{ox}+C_s} \tag{2.21}$$

where C_{ox} is the oxide capacitance with the unit of Farad, expressed as follows.

$$C_{ox} = \frac{A\varepsilon_0\varepsilon_{SiO_2}}{t_{ox}} \tag{2.22}$$

where ε_0 stands for the vacuum permittivity, $\varepsilon_{SiO_2} = 3.9$ represents the relative permittivity of the oxide and t_{ox} stands for the oxide thickness. Note that the differential capacitance is positively proportional to the absolute value of slope in the curve in Fig. 2.4.

Performing derivatives in equation (2.20) gives the depletion capacitance for SiC,

$$C_s = A\frac{\varepsilon_{SiC}}{\sqrt{2}L_D}\frac{\exp(\varphi_s / V_t)-1}{F_{SiC}(0,0)} \tag{2.23}$$

where $F(0,0)$ is the electrical field at surface for SiC, in equation (2.17).

The following illustrates the theoretical total capacitance curve with respect to band bending φ_s. A general expression of the normalised curve is shown in Fig. 2.5. Positive band bending induced accumulation of the electrons leads to a large capacitance. That large capacitance is parallel with oxide results in the oxide capacitance domination. Before band bending $-2\varphi_{FB}$, for ideal MOSCAP ($D_{it}=0$), these curves coincide with each other. When pushing the band bending further downward, for SiC, based on equation (2.23), the total capacitance decreases continuously into deep depletion as expected, instead of retaining a certain constant or rising again.

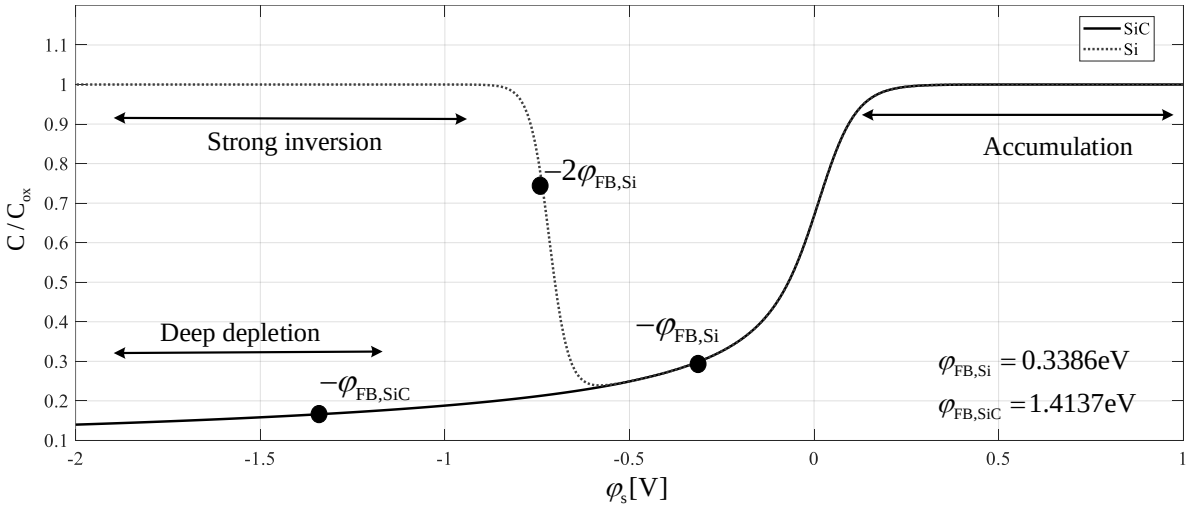

Fig. 2.5. Normalised total capacitance as a function of band bending for n-type substrate MOSCAP; Dashed line represents Si, while solid line stands for SiC. The doping concentration at substrate is $5\times10^{15}cm^{-3}$, and temperature is set to 300K.

Due to charge neutrality, taking n-type substrate MOSCAP as an example, any charges at the gate electrode will result in a unique response in the substrate, either in the inversion layer for silicon or depletion region deep depletion in SiC. When in inversion mode ($\varphi_s < -2\varphi_{FB}$), for silicon devices, inversion layer charges provide positive charges to neutralise the increment of negative charges at the gate electrode. However, for SiC devices, the generation time of the minority carriers is too long for measurement to observe so that only depletion charges respond to the applied voltage. The depleted charges originate from ionised doping impurities, whose concentration is considered to be uniform ideally. Based on that, the depletion width must be broadened and the electrical field at the surface also increases. In practice, the doping profile is not uniform and cannot be fully ionised at room temperature in SiC devices, and that will be discussed in detail in chapter 5.

The band bending, or surface potential φ_s has a close relationship with surface electrical field and applied voltage. All measurements should transfer applied voltage into surface potential because it contains the basic information of the semiconductor-oxide interface, and even reflects the fluctuation caused by interface traps. Beginning with ideal MOSCAP, the applied voltage can be expressed by a voltage divider,

$$V_{gs} = \varphi_s + V_{ox} \tag{2.24}$$

where V_{ox} is the potential crossing the oxide. Assuming net charges exist inside the oxide in ideal MOSCAP is zero, according to Gaussian's law, electrical flux flowing through the oxide-semiconductor interface is zero, so that

$$\varepsilon_{SiO_2} F_s\left(0^-\right) = \varepsilon_S F_s\left(0^+\right) \tag{2.25}$$

where ε_{SiO_2} and ε_S are the permittivity of oxide and semiconductor, respectively. $F_s\left(0^-\right)$ is the electrical field on the interface in the oxide side, and $F_s\left(0^+\right)$ is from the semiconductor side. Combining all, the relation between the applied voltage and surface potential should be,

$$V_{gs} = \varphi_s + V_{ox} = \varphi_s + \frac{\varepsilon_S}{\varepsilon_{SiO_2}} F\left(0, \frac{p_{p0}}{n_{n0}}\right) t_{ox} \tag{2.26}$$

where $F\left(0, p_{p0} / n_{n0}\right)$ is the electrical field at semiconductor surface in equation (2.16).

Figure. 2.6 illustrates the calculated $\varphi_s - V_{gs}$ relation in silicon device and zoom-in version of both silicon and SiC devices at different temperatures. The inversion layer in Si flattened the $\varphi_s - V_{gs}$ curve when $\varphi_s < -2\varphi_{FB}$. In the depletion region in the zoom-in version, due to the large minority carrier generation time, more voltage should be applied for SiC devices to reach the same surface potential as silicon devices. That is because, with a certain negative applied voltage, the depletion region should be extended to compensate and keep charge neutralisation.

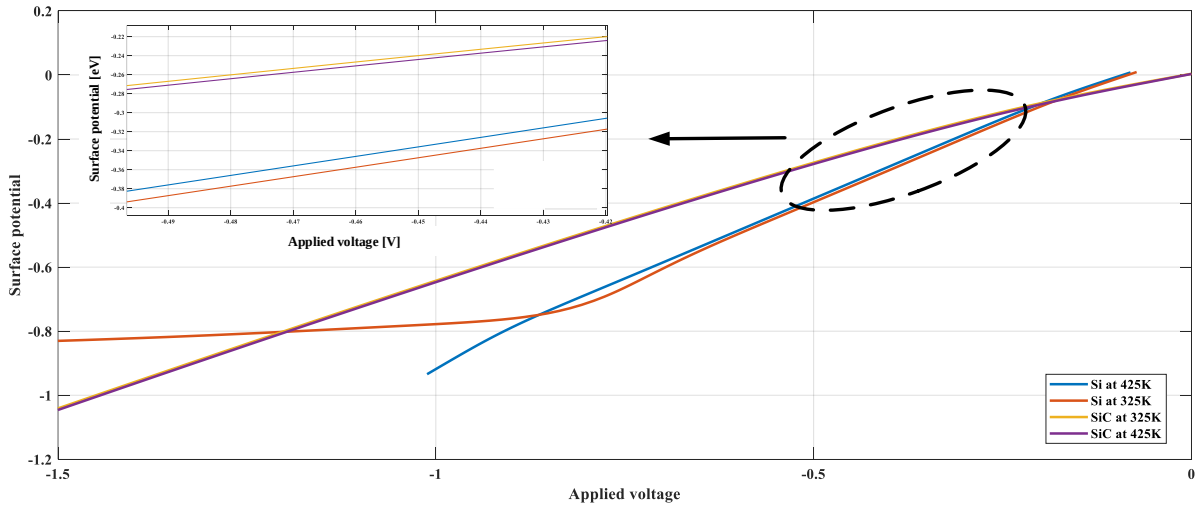

Fig. 2.6. Surface potential as a function of applied voltage for n-type substrate MOSCAP; The doping concentration at substrate is $5\times10^{15}\,\mathrm{cm}^{-3}$, calculated by equation (2.26).

2.3 Real MOSCAP and SiC interface

Various non-idealities in real-world systems affect the behaviour of MOSCAP, expressed as follows, in Fig. 2.7 (a).

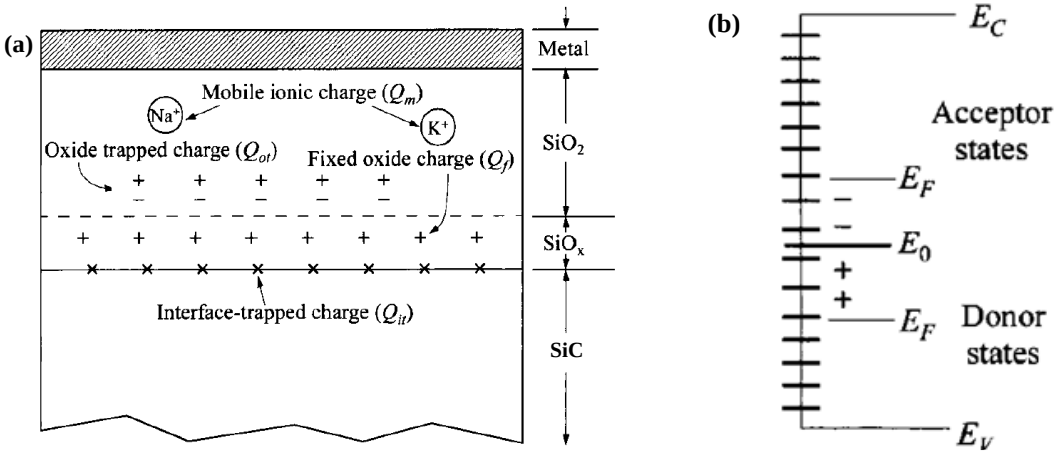

Fig. 2.7. (a) Cross section of a SiC MOSCAP considering non-idealities: the interfacial trapped charges, oxide charges, fixed charges and mobile charges [28]. (b) Interfacial states in band diagram.

- Nonzero work function differences between metal and semiconductor. The work function difference is determined by both the doping concentration in substrate and materials. In that case, equation (2.1) no longer holds.

- Fixed charges inside the insulator (Q_f). Fixed charges locate at the SiC-oxide interface, originated from oxidation and annealing processes. It forms a thin charge layer and is independent of doping, oxide thickness and any other external conditions [28]. This charge layer causes an extra potential drop applied to fixed charges, causing a horizontal shift in C-V measurement curve.

- Mobile charge inside the insulator (Q_{mo}). Under extremely high temperature ($800^\circ C$) [29], these charges are activated and the conductive ions respond to the bias signal, perpendicularly moving inside the oxide. The movement of the contaminations including ions (K^+ and Na^+) results in clockwise hysteresis of CV measurement.

- Oxide charges (Q_{ox}). Both holes (positive) and electrons (negative) charges can be trapped inside the oxide. The dominant defects in the SiC-oxide system are carbon atoms replaced by oxygen atoms (noted by $C-O(C)$ bond) and O (oxide vacancy) [30], which are both weak bonds [25]. At moderate temperature ($175^\circ C$), the defects then gain the ability to trap after jumping $1.1eV$ barrier [25]. As a result, the trapping of holes or electrons leads to the negative and positive shift of threshold voltage, respectively. In addition, oxide traps assist holes in conduction band tunnelling into the oxide layer [17]. The closer to the SiC-oxide surface, the more degradation they will cause. According to Gaussian's law, with oxide thickness t_{ox}, the voltage shift in C-V curve of charge density ρ_{ox} should be,

$$\Delta V_{ox} = \frac{1}{C_{ox}} \frac{1}{t_{ox}} \int_0^{t_{ox}} x \rho_{ox} dx \tag{2.27}$$

Based on that, the flat band voltage is not zero, and extra voltage should be applied to compensate for the effects mentioned before. The flat band voltage now is,

$$V_{FB} = \varphi_{ms} - \frac{Q_{fix}}{C_{ox}} - \frac{Q_{mo}}{C_{ox}} - \frac{1}{t_{ox}} \int_0^{t_{ox}} x\rho_{ox} dx \tag{2.28}$$

The fixed charges, mobile charges and oxide charges that are far from the interface cannot respond to the bias signal at moderate temperature. The real C-V curve can be shifted from an ideal C-V, by superimposing the defects in equation (2.28) and replacing V_G by $V_G - V_{FB}$.

However, one critical defect, near interface traps D_{it} cannot be cancelled by simply shifting the C-V curve. The near interface traps are considered the main source of reliability problems for SiC devices [30], which limits their applications in harsh environments. The large density of the interface traps in SiC devices is a commonly recognised explanation of low quality of SiC-oxide interface. However, the main mechanisms of interface traps are not fully explained, the hysteresis in the state of the art includes:

- Dangling bonds.

The periodical crystal structure in the substrate abruptly stops at the Oxide-SiC interface, where the unpaired electrons exist at the surface. In Si, the interfacial traps mainly originate from dangling bonds on the silicon side, whose density can reach $10^9 - 10^{10} cm^{-2} eV^{-1}$ [15]. In contrast, in SiC the typical interfacial trap density is $10^{12} - 10^{13} cm^{-2} eV^{-1}$ [15], and high trap density gives the SiC detection signal by electron-paramagnetic-resonance (EPR) different from Si [31]. The spread of energy levels and orientations indicated that C dangling bonds exist and the Si dangling bonds are not dominating. In addition, the experimental evidence that H_2 annealing cannot reduce the density of defects [31] also supports the analysis before.

- C clusters.

During the thermal oxidation process, the SiC reacts with oxide forming SiO_2 layer at the top of the SiC substrate and exhaust CO and CO_2. The diffusion of the carbon atoms is not ideal and the carbon atoms form "graphite-like" structure or carbon cluster [31, 32], which cannot be further oxidized. These traps can be electrically activated at high temperature, forming an unsaturated bond (Sp2) [33], which results in high interface density. The SiC substrate and oxide layer are not a "brick wall" shaped model, in fact, the transition layer observed from experiments by Afanasev [32], who tells that the "graphite-like" cluster appears in the whole bandgap, whereas the Sp2 bonded cluster dominates from band edge to midband.

- Shallow traps.

In the band diagram, those traps which are close to the conduction band can interact with the channel and oxide without overcoming too much energy barrier and are more active than the traps in the middle of the band diagram. Authors in [32] emphasise that near interface defects are responsible for interface traps, and in MOS devices, these kinds of traps are commonly acknowledged reason for instability and are named near interface traps (NITs) in short. Deep traps located inside the midband are not easily activated, and cannot change the mobility in the channel.

To describe and classify the interface traps, in the energy band diagram, the upper half of the band traps show as acceptors and capture surface electrons, whereas the traps behave like donors situating in the lower band, and unoccupied traps are electrically charged, illustrated in Fig. 2.7 (b) [28].

Fig. 2.8 illustrates the interface state density as a function of energy inside the bandgap of various semiconductors, including 4H-SiC, 3C-SiC, 6H-SiC and Si, with all contributions illustrated. It is clearly observable in Fig. 2.8. (a) that the density of near interface traps (NITs) increases dramatically at the conduction band edge. When external condition changes such as temperature and applied gate voltage, the Fermi level at the SiC-oxide surface responds, thus the occupation of NITs varies. As a result, NITs are regarded as the main reason for threshold instability and oxide quality degradation under high temperature.

Rather than NITs, the Sp2 bonds induced by dangling bonds in Fig. 2.8 (b) and graphite-like carbon clusters far away from the conduction band edge are not sensitive without external conditions. This indicates these types of trap states are not easily activated as NITs and are considered to be “fixed charges” for simplicity, called “deep level traps”. For interface traps induced by Sp2 bonded clusters, the traps are distributed mainly near the valance band edge. Together with the NITs, the trap density dramatically increases near the band edge.

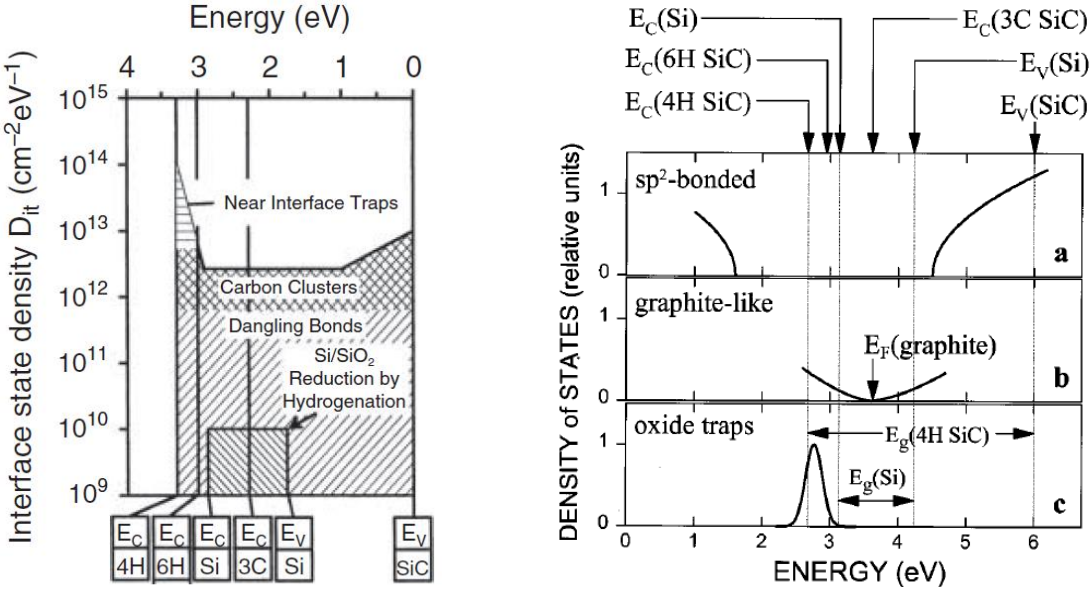

Fig. 2.8. Interface states distribution and contribution in bandgaps of different materials, with respect to 4H-SiC, 3C-SiC, 6H-SiC and Si [32].

For those interfacial traps that capture and release the charges from the conduction band, they interact charges with the channel and further affect the channel mobility and on-resistance. For those traps occupied by holes or electrons, define a quantity D_{it} representing the density of trapped charges, modified from equation (2.5) and shown below

$$\rho(x) = q\left(N_D^+ - N_A^- + p_p - n_n\right) \pm qD_{it} \tag{2.29}$$

For interface traps that capture holes (release electrons), minus sign should be applied and a positive sign employed for acceptor traps (accept electrons or release holes).

Considering interface traps, the Poisson equation (2.4) should be modified, with extra potential fluctuation caused by interface trapped charges,

$$\frac{d^2\varphi_{it}(x)}{dx^2} = \frac{q\rho_{it}(x)}{\varepsilon_{SiC}} \tag{2.30}$$

where $\varphi_{it}(x)$ represents the extra potential drop induced by interface traps. This extra potential drop is superimposed into band bending φ_s, which depends on the distance to the oxide-SiC interface. The surface potential fluctuation $\varphi_{it}(x)$ can also be observed in extremely high frequency C-V measurement, when no charge carriers can follow the signal.

The sensitivity to external conditions and interface trap distribution are not uniform in SiC substrate. The interfacial traps exponentially distribute near the conduction band edge, indicating that the shallow traps have a large probability to interact with charges in the channel or oxide layer. As a result, the interface traps induced surface potential fluctuation $\varphi_{it}(x)$ and electrical field near the interface dominates the behaviour. Details are calculated in chapter 3. In this chapter, for simplicity, the total trapped charges inside the bandgap (inside substrate) are quantified by Q_{it}, and the interface trap induced capacitance is defined as C_{it}.

Considering interface traps, the equivalent circuit of the MOSCAP system is shown in Fig. 2.9. In this schematics, oxide capacitance is C_{ox}, C_{it} and C_s represents interface trapped capacitances and depletion capacitance, respectively. The interface trapped capacitance is also differential capacitance, similar to equation (2.20), expressed by,

$$C_{it} = A\frac{d|Q_{it}|}{d\varphi_s} \tag{2.31}$$

Another view of interface traps induced capacitance is the ability to hold trapped charges since capacitor is a device holding charges for certain times. More importantly, it suggests that extra band bending and extra energy are required to push the electrons out of the traps, and that surface potential fluctuation causes a stretch out of C-V curve. A Comparison made with ideal MOSCAP is shown as follows in Fig. 2.10.

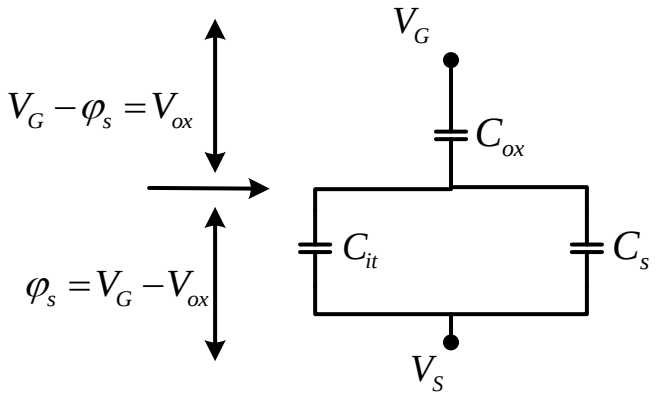

Fig. 2.9. Equivalent circuits for real MOSCAP, considering interface trapped capacitance only.

Extra surface potential fluctuation due to interface traps will be analysed, with the equivalent circuit of the real MOSCAP (without series resistance and trap induced conductance) in Fig. 2.10. The dashed line represents the stretch out of the C-V curve, for both SiC and Si.

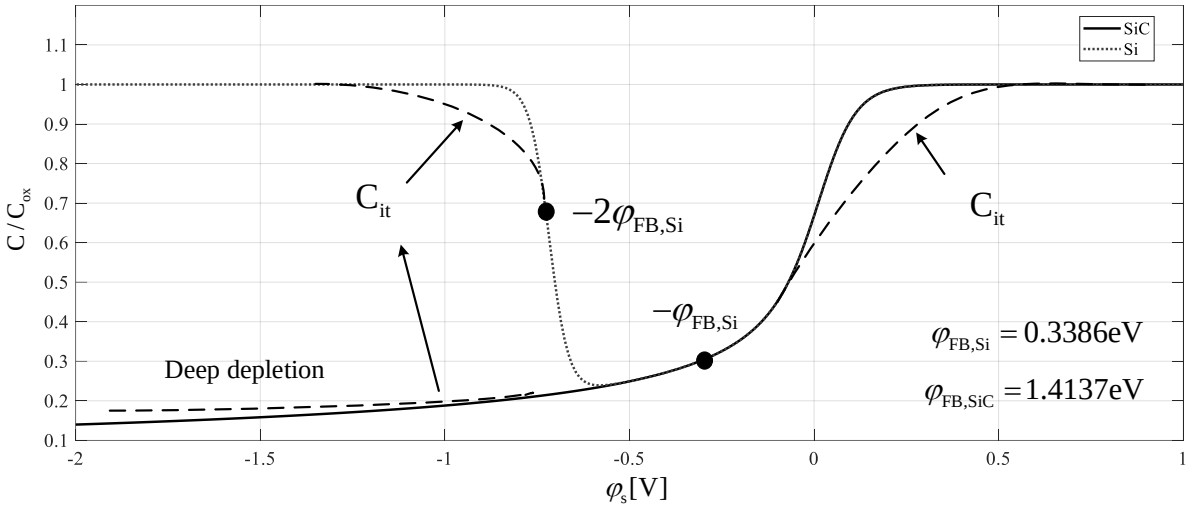

Fig. 2.10. Normalised total capacitance as a function of band bending for n-type substrate MOSCAP; Dotted line represents Si, solid line stands for SiC while dashed line is interface trapped condition. The doping concentration at substrate is $5\times10^{15}\mathrm{cm}^{-3}$, and temperature is set to 300K.

The potential drop from gate to substrate electrodes is V_{gs}, assuming all voltages are DC values. Here, the charge neutrality must be applied, and the charges in the gate electrode must equal oxide and substrate. Based on that, simply write,

$$Q_G = -\left(Q_s + Q_{it}\right) \tag{2.32}$$

where Q_G represents applied external gate charges, Q_{it} and Q_s stand for the interface trapped charges and space charges in the depletion region, respectively. Note gate electrode charges Q_G is equivalent expressed by,

$$C_{ox}\left(V_G - \varphi_s\right) = -\left(Q_s + Q_{it}\right) \tag{2.33}$$

Differentiating both sides gives,

$$C_{ox}\left[\, d\left(V_G\right) - d\left(\varphi_s\right)\right] = -d\left(\varphi_s\right)\left[\, -C_s\left(\varphi_s\right) - C_{it}\left(\varphi_s\right)\right] \tag{2.34}$$

Here, C_{it} and C_s are both functions of band bending φ_s. In this case, $d\left(V_G\right) - d\left(\varphi_s\right)$ are positive numbers, to guarantee right-hand side positive, minus sign must be added if removing the absolute value in equation (2.20).

Rearrange the equation (2.34), obtaining,

$$\frac{d\left(\varphi_s\right)}{d\left(V_G\right)} = \frac{C_{ox}}{C_s\left(\varphi_s\right) + C_{it}\left(\varphi_s\right) + C_{ox}} < \frac{C_{ox}}{C_s\left(\varphi_s\right) + C_{ox}} \tag{2.35}$$

The depletion capacitance $C_s(\varphi_s)$ with respect to band bending is shown in equation (2.23). The $d(\varphi_s)/d(V_G)$ cannot exceed the upper limit (envelop) $C_{ox}/(C_s(\varphi_s)+C_{ox})$, which is the ideal MOSCAP without minority carriers and interface traps. In accumulation mode, where $C_s(\varphi_s) >> C_{ox}$, the $d(\varphi_s)/d(V_G)$ is approaching zero, and means that the band bending does not respond to the applied voltage. That is why we will focus more on depletion mode.

However, for an ideal SiC device without interface traps, in the depletion region, $C_s(\varphi_s)$ gradually decreases until reaching $C_s(\varphi_s) << C_{ox}$, thus the approximation value of $d(\varphi_s)/d(V_G)$ is 1, plotted by the dotted line. For silicon devices, $C_s(\varphi_s)$ rises again and physically, it is the minority charges in the inversion layer that responds to the charges in the gate, the electrical field and surface potential cannot grow more with respect to gate voltage, plotted in the dashed line. In SiC, when applying large voltage, it pushes the Fermi level at the oxide-SiC surface to the band edge, so that $C_{it}(\varphi_s)$ should dominate. As a result in equation (2.35), the $d(\varphi_s)/d(V_G)$ is dropped below 1, where the dotted line is flattened, illustrated by the solid line, and the gap between them represents the effect of near interface traps.

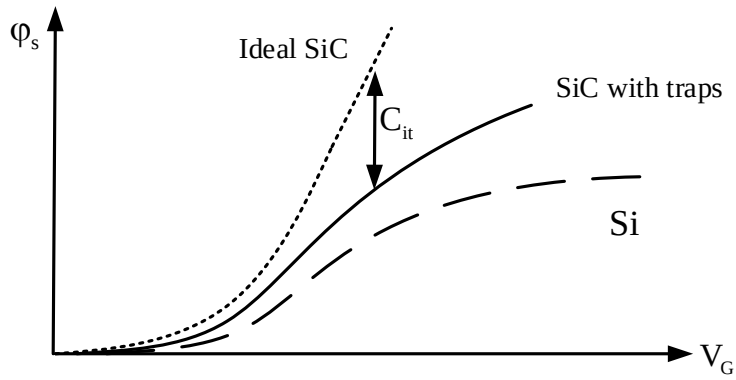

Fig. 2.11. Illustration of band bending as a function of applied voltage; Dotted line, ideal SiC MOSCAP without C_{it}. Solid line, real SiC MOSCAP with C_{it}. Dashed line, real Si MOSCAP.

In parameter extractions, it is worthwhile to obtain the trap distribution inside the bandgap, so that energy-surface potential relation should be highlighted as follows.

$$\frac{E_C - E_T(V_G)}{q} = \frac{E_g}{2q} + \varphi_s(V_G) - \varphi_{FB} \tag{2.36}$$

where E_g is the bandgap, $\varphi_s(V_G)$ represents the surface potential as a function of applied voltage, and φ_{FB} stands for the Fermi level at a certain doping concentration. The aforementioned equation is a bridge between the surface potential and energy position of the trap, once $\varphi_s(V_G)$ is known. For doping concentration of $5\times10^{15}\text{cm}^{-3}$, $E_g/2q - \varphi_{FB} = 0.216\text{V}$, and that is the reason why interested region of the interface trap distribution in literatures is $[0.2\text{eV}, 0.6\text{eV}]$ away from conduction band edge.

In conclusion, starting from ideal MOSCAP, this chapter derives the electrical field, surface potential, surface charge and capacitance, and highlights the differences between silicon and silicon carbide devices. The generation time for minorities in SiC devices is so long that no inversion layer forms and the C-V curve can only be pushed into deep depletion rather than inversion, where the capacitance value drops gradually.

3. Electrical characterisation methods

Effectively using SiC materials in integrated circuits necessitates the need to understand charge transport within them, for effectively modelling and explaining of stability problems. Electrical characterisation methods investigating the properties of the devices, by extraction of the measured results from testing MOSCAP structures, promote the understanding of temperature stability problems. This chapter mainly characterises interface trap distribution in SiC-oxide surface.

3.1 The measurement setup

The C-V measurement is commonly used method for electrical characterisation, to determine the response of charge carriers. The high frequency C-V measurement is employed to test the behaviour when minority carriers and trapped charges cannot follow the high frequency signal. In SiC devices, because of the slow response of trapped charges, quasi-static CV measurement (QSCV) is used to guarantee the MOSCAP system to be steady state.

For high frequency C-V measurement, the sample is detected by cascade probe station and processed by KEYSIGHT 4294A impedance analyser. With a DC sweeping signal, a sinusoidal small signal ac input is applied to the gate electrode of DUT (device under test), and the total voltage can be split into linear part and ac part,

$$V_{app} = V_{sweep} + \upsilon_{ac} \exp(j\omega t) \tag{3.1}$$

where υ_{ac} is the amplitude of small signal, ω is signal frequency, and $j = \sqrt{-1}$.

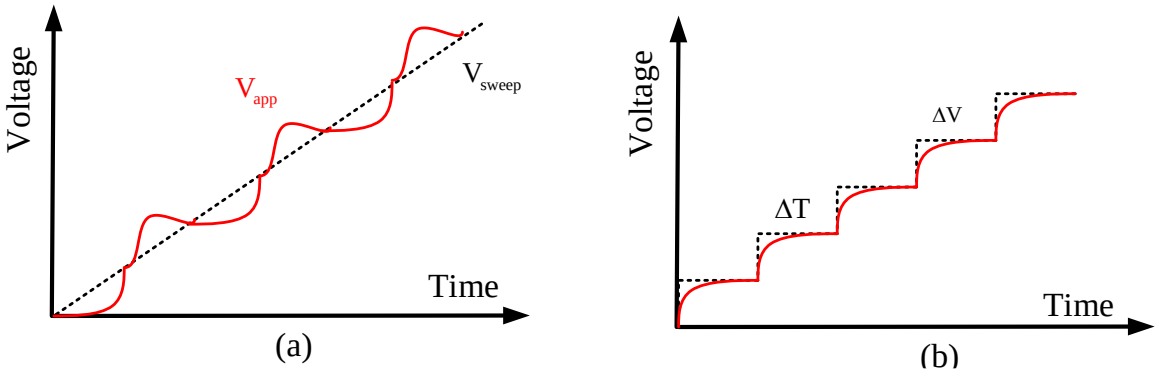

Fig. 3.1. Applied waveforms for (a) High frequency C-V measurement, with a superimposed ac signal (with certain frequency) on sweeping linear signal. (b) QSCV measurement, the step function and charging voltage (red solid line).

Figure. 3.1 illustrates the waveform and principle of high frequency C-V measurement and QSCV measurement. In QSCV measurement, a B1500A semiconductor device analyser is applied and ΔT should be sufficiently large to fully charge the MOSCAP system. The capacitance can be derived below if the charging current is known,

$$C = Q / V = I \times \Delta T / \Delta V \tag{3.2}$$

3.2 Threshold voltage characterisation

Threshold voltage V_{th}, defined as the applied gate voltage at which the band bending is twice the Fermi level, is the most important parameter for MOS devices. Since the channel current will increase dramatically when $V_G > V_{th}$, any small variation of threshold voltage will cause a large change of channel current. Accurately modelling threshold voltage, especially under the harsh environment such as high temperature, attracts researchers' attention recently.

The threshold voltage of SiC devices including all defects is composed of an ideal part and non-idealities, expressed by [28],

$$V_{th} = \varphi_{ms} + 2\varphi_{FB}(T) + \frac{\sqrt{4\varepsilon_{SiC} q N_A \varphi_{FB}}}{C_{ox}} - \frac{Q_{it}(T) + Q_{fix} + Q_{mobile}(T) + Q_{ox}}{C_{ox}} \tag{3.3}$$

Where $\varphi_{FB}(T)$ represents temperature dependent Fermi level, ε_{SiC} stands for the permittivity of SiC, N_A is the doping concentration of the substrate, and φ_{ms} is metal-semiconductor work function difference. The first three terms are threshold voltage in ideal MOSCAP, similar to the textbook formula. The last term including interfacial trapped charges (Q_{it}), fixed charges (Q_{fix}), mobile charges (Q_{mobile}) and oxide charges (Q_{ox}) are all nonideal terms, discussed in the previous chapter.

There are more than 20 methods to extract threshold voltage. In silicon devices, the threshold voltage locates at the lowest point in low frequency C-V (LFCV) measurement curve. However, in SiC devices, the threshold voltage is not clear enough to be observable from C-V curve. From $I_d - V_g$ transfer curve, both linear region and saturation region can be used for extraction [37]. From the linear region, one commonly used method is to take linear extrapolation of the sloppiest (maximum first derivative) point, where the threshold voltage is the intersection point on the horizontal axis [38]. This method may suffer from parasitic resistance and mobility degradation at high temperature [39].

More accurate methods for extracting threshold voltage from the linear region of $I_d - V_g$ curve include: the constant current method [38, 40], the transconductance change method [40, 41], and the second derivative method [42]. Instead of directly finding them in $I_d - V_g$ curve, they mapped threshold voltage to another parameter which is easy to calculate and well-defined, such as constant current and transconductance. Additionally, from the saturation region, one popular method is taking $\sqrt{I}$ and determining the intersection point with V_g axis. Besides, G_1 function method [43] developed by Garcıa prevented the threshold voltage extraction process from series resistance and mobility degradation, as mentioned in [39].

3.3 Interface trapped charges in bandgap

The interface trapped charges Q_{it}, as the name suggests, are the charges trapped by near interface states and sensitive to external conditions, such as thermal activation (temperature) and applied voltage. Those charges consume extra energy to trap (de-trap) and fluctuate the surface potential, so that threshold voltage shift will be observed in the C-V curve, as shown in Fig. 2.9 in chapter 2. Although the behaviour of those traps is temperature dependent, in this section, we only focus on the characterisation and physical model of it. Several assumptions are stated here,

- Although in SiC the dopants are not fully ionised, the doping profile is still considered as a uniform distribution. Details including ionisation will be discussed in chapter 5.
- Charge carriers are captured instantaneously at the trapping site.
- The trapping and releasing of charge carriers are thermally controlled.

It is also important to classify the traps by means of locations. Fig. 3.2 shows the band diagram of interface traps and the distribution as a function of energy levels. Based on the location in the band diagram, the traps near the band edge are called shallow traps ($E_{t,1}$ and $E_{t,2}$), whereas the traps located deeply inside are called deep traps ($E_{t,3}$). For shallow traps, the ability of capturing and releasing charge carriers is stronger than deep traps, indicating that the charge transport between the conduction band and shallow traps is much more frequent than deep traps. The deep traps, instead, can be regarded as fixed charge. In addition, another reason why shallow traps are more active is that, the density of trap states D_{it} increases exponentially at the band edge. For conduction band edge [44],

$$D_{it}(E) = D_{it0} + D_{edge} \exp\left(-\frac{E_C - E}{\sigma}\right) \tag{3.4}$$

where D_{it0} represents the midband trap density (also deep traps), D_c stands for the conduction band edge trap density, σ is the band tail decay energy, and E_C is conduction band edge.

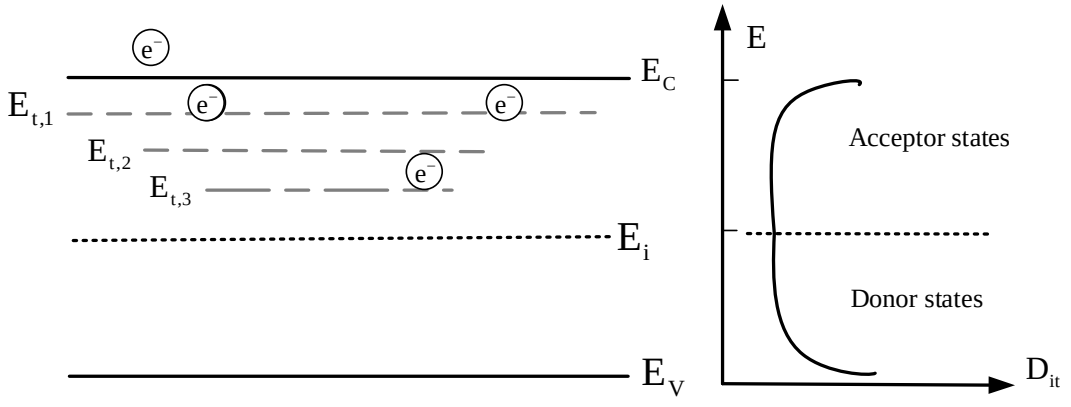

Fig. 3.2. Illustration of interface traps inside the bandgap, using band diagram; The exponential distribution function is also shown on the right hand side.

Any MOS system with interface traps can be expressed by an ideal MOS with defects, including both acceptor traps and donor traps. The acceptor trap is neutral when it is empty and negative when it is full and accepts electrons. The donor trap is neutral when full, and positive when it releases electrons (or captures holes). The Oxide-SiC interface has both types of traps, but only one type dominates, depending on the substrate doping level. For n-type substrate, acceptor traps are dominant; whereas donor traps exist in p-type substrate.

Here, the Fermi-Dirac statistic is applied to describe the occupation probability of electrons and holes. The probability of the acceptor and donor interface traps capturing charge carriers at certain energy E is,

$$f_A(E,T) = \frac{1}{1+g_D \exp\left[(E-E_F)/kT\right]} \tag{3.5}$$

$$f_D(E,T) = 1 - \frac{1}{1+g_A \exp\left[(E-E_F)/kT\right]} \tag{3.6}$$

where E_F is the Fermi level, k is Boltzmann constant and T represents temperature. The ground-state degeneracy is $g_D = 2$ and $g_D = 4$ for n-type doping and p-type doping [45], depending on spin quantum number itself.

Taking the n-type substrate as an example, electrons dominate and acceptor traps capture electrons from the conduction band, and equation (3.5) should be applied. Hole concentration is so low that equation (3.6) can be reasonably ignored so that the interface trapped charge mainly locates on the upper half of the band. The interface trapped charge inside the bandgap can be effectively modelled by the integral considering the upper band, and the minus sign in front represents it is the electrons that are captured or released.

$$Q_{it}(E,T) = -q\int_{E_i}^{E_C} D_{it}(E) f_A(E,T)\,dE \tag{3.7}$$

where E_i and E_C are midband ($E_g/2$) and conduction band edge. Substitute equation (3.4) and split equation (3.7) into two part, in which the first part represents the charge trapped near midband, giving,

$$Q_{it,Mid}(E,T) = -q\int_{E_i}^{E_C} D_{it0} f_A(E,T)\,dE \tag{3.8}$$

The second part stands for the trapped charge density of the band edge traps, which is increased exponentially and easily expressed below,

$$Q_{it,Edge}(E,T) = -q\int_{E_i}^{E_C} D_c \exp\left(-\frac{E_C - E}{\sigma}\right)\cdot f_A(E,T)\,dE \tag{3.9}$$

The integral steps can be simplified if we rearrange the Fermi-Dirac probability function in equation (3.5) with respect to $E - E_C$. To eliminate the Fermi energy E_F, and assuming that the electrons mostly originate from ionised doping atoms,

$$n = N_C \exp\left(\frac{E_F - E_C}{kT}\right) = N_D \tag{3.10}$$

where N_C is density of available states at conduction band edge, and N_D represents the concentration of donors. The Fermi-Dirac distribution now with respect to $E - E_C$ becomes,

$$f_A(E,T) = \frac{1}{1 + g_D \cdot (N_C / N_D) \cdot \exp\left[(E - E_C)/kT\right]} \tag{3.11}$$

The details of solving equation (3.4) and (3.7) are provided in Appendix 2 and 3. For n-type SiC substrate, in upper half band, integrating from midband to conduction band edge gives the midband trapped charges,

$$Q_{it,Mid}(E,T) = -\frac{qD_{it0}N_D}{4n_i}\left\{\frac{E_g}{2} + \frac{kTN_D}{4n_i}\ln\left[1 + \frac{2N_C}{N_D + 2N_C}\left(\exp\left(\frac{-E_g}{2kT}\right) - 1\right)\right]\right\} \tag{3.12}$$

where E_g is the bandgap, N_C is the density of states at the conduction band edge. The density of trapped charge at the midband is a function of midband trap density D_{it0}, substrate doping concentration N_D, and temperature T. The equation (3.12) in nature is the plot area covered by equation (3.5). When temperature goes up, the Fermi level approaches to midband, since intrinsic charge increases and dopant are ionised, and the area covered reduces. It indicates the fact that the increased temperature activates the trapped charges, even near midband, which are released to the conduction band.

However, the charge release at high temperature is slow, since the occupation probability in equation (3.5) only drops at the conduction band edge. $Q_{it,Mid}$ is regarded as deep traps, which cannot give enough response to the external environment. Providing constant midband trap density D_{it0}, only the Fermi-Dirac function is responsible for temperature change so that for the region near midband, these traps calculated in equation (3.12) are deep traps.

The interface trapped charge near the band edge shows different properties. Several reasonable assumptions are applied in SiC material: the band tail decay energy should never be less than thermal energy $\sigma > kT$. In appendix 3, the total trapped charges between energy $[E_i, E_C]$ is solved and shown in equation (3.13).

$$Q_{edge}(E,T) = -\frac{q\sigma D_{edge}}{\sqrt[b]{a}}\frac{\pi / b}{\sin(\pi / b)} \tag{3.13}$$

where, for simplicity, the density of state at the conduction band is larger than doping level, equivalently saying that $a = 2N_C / N_D$ is a large positive number. In addition, $b = \sigma \backslash kT > 1$ applies in SiC devices.

The density of trapped charge at the conduction band edge is a function of the band edge trap density D_{edge}, band tail decay energy σ, doping concentration N_D and temperature T. The temperature T shows up in a and b, directly dominating the behaviour of trapped charges. It is easy to draw the conclusion that conduction edge trapped charges are more sensitive to the external environment than midband trapped charges.

Equation (3.12) needs to be simplified. Using the fact that $a = 2N_C / N_D >> 1$ and substituting equation (3.11), the midband trapped charges after first order approximation now is,

$$Q_{it,Mid}(E,T) = \frac{qD_{it0}kT}{4a^2}\exp\left(\frac{E_C - E_F}{0.5kT}\right) \tag{3.14}$$

The parameter b in equation (3.13) boosts the trapped charges near the band edge, compared with equation (3.14), where a^2 in denominator compresses the trapped charges near midband $Q_{it,Mid}$. It is illustrated in Fig. 3.3 that the total trapped charge inside the upper band $[E_i, E_C]$ are plotted, simulating the results from both equation (3.12) and (3.13) from 300K to 500K.

At room temperature $T = 300K$, the trapped charges accumulate near the conduction band edge ($E_{t,1}$), peaking at $E = 3.0eV$, whereas deep level trap states are uniformly distributed inside with lower density. When rising temperature, for the trapped states near midband ($E_{t,3}$), the trapped charges are "stubborn", since the Fermi-Dirac probability function at deep level does not vary too much, even at $T = 500K$. Instead, the temperature dependency is totally different at the band edge. After absorbing sufficient energy at high temperature, the trapped charges are emitted into the conduction band, leading to a dramatic drop of trapped charges at the conduction band edge. More empty interfacial trap states are ready and available to capture the electrons from the conduction band, and frequently interact with the conduction band resulting in reliability problems in devices.

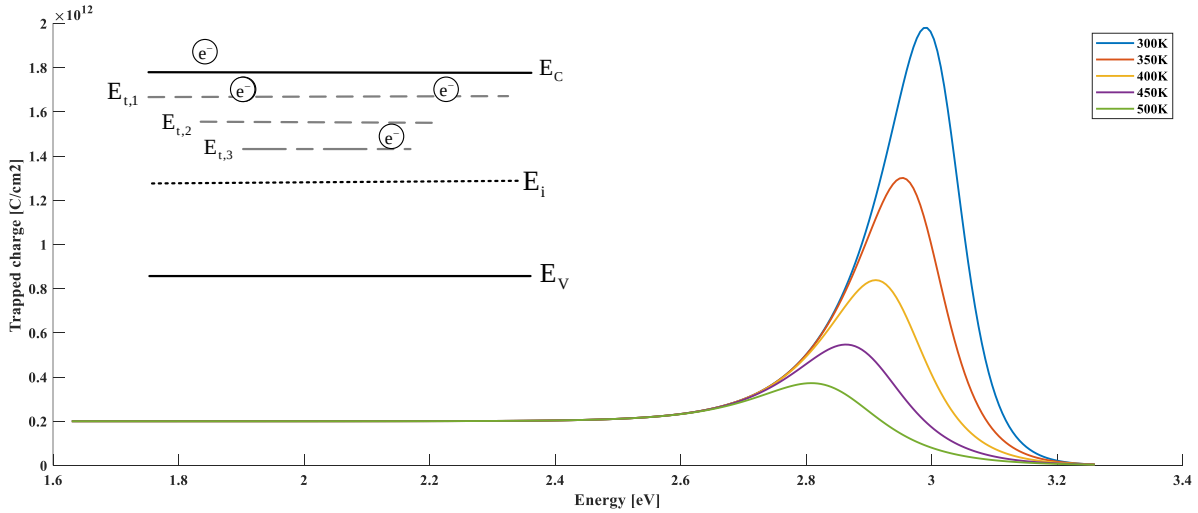

Fig. 3.3. Illustration of interface trapped charge inside the whole bandgap, a plot of equation (3.7); Temperatures are chosen from 300K to 500K, calculated for n-type substrate MOSCAP with doping concentration of $5\times10^{15}cm^{-3}$.

3.4 Interface traps density by experimental characterisation and extraction

The density of states of interface traps is characterised and extracted commonly from C-V measurement. As one of the most powerful techniques for semiconductor research, C-V measurement contains plenty of device information, including substrate doping concentration, trap density, flat band voltage, and surface potential. The measured capacitance is automatically calculated by the detected voltage and current. In general, a DC signal is the sweeping signal applied to the gate of the MOSCAP, superimposed to an AC signal with small amplitude (500mV), and the testing frequency can be adjusted for different types of measurement.

High frequency is defined when the minority charge carriers cannot follow the small AC signal, and typically 1MHz is sufficiently high. Instead, to investigate the slow traps and minority carriers (no generated minority carriers exist in SiC), all of the charge carriers should be able to follow the low frequency AC signal and QSCV is often applied. In chapter 2, the trapped charges degrade the ideal CV curves, with the trapped capacitance C_{it} $[\text{eV}^{-1}\text{cm}^{-2}]$,

$$C_{it} = qD_{it} \tag{3.15}$$

where D_{it} (unit $[\text{eV}^{-1}\text{cm}^{-2}]$) is trap density in equation (3.4) and q is elementary charge. Here the unit of C_{it} should be explained. In most cases, the energy unit is expressed by eV rather than J. The elementary charge q is unit-less, rather than $1.69\cdot 10^{-19}\text{C}$.

The capacitance model of the MOSCAP will be introduced as follows, considering interfacial trap induced capacitance, in figure 3.4. In high frequency measurement, none of the trapped charges can follow the high frequency measurement signal. Hence, the traps induced charges have no contribution to C-V curves so that the ideal curve can be obtained when $f \to +\infty$.

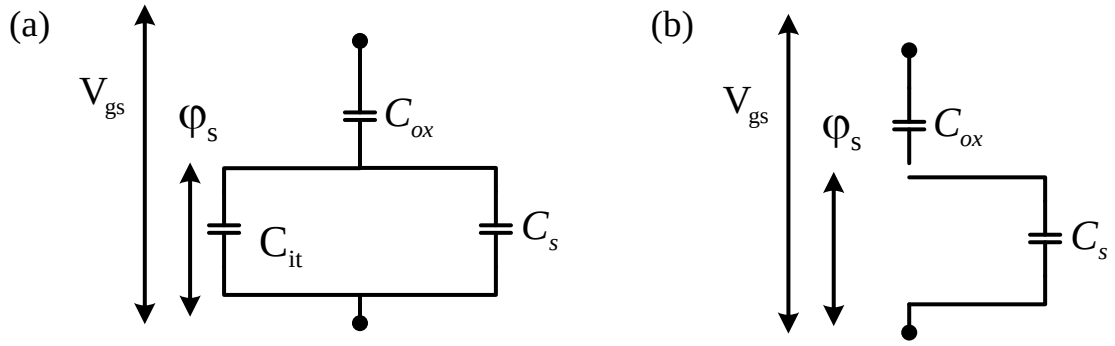

Fig. 3.4. Equivalent capacitance model of SiC MOSCAP and potential drop; (a) low frequency condition, (b) high frequency condition and ideal case.

The high frequency measurement capacitance and low frequency measured capacitance are shown as follows, based on the equivalent circuit diagram,

$$C_{HF} = \frac{C_{ox}C_s}{C_{ox}+C_s} \tag{3.16}$$

$$C_{LF} = \frac{C_{ox}\left(C_s+C_{it}\right)}{C_{ox}+C_s+C_{it}} \tag{3.17}$$

The following introduces the methods for the extraction of interface traps.

3.4.1 Terman method

This method is firstly developed by Terman, also called high frequency method or differentiation method [46]. The theoretical analysis in Fig. 2.5 clearly shows the ideal capacitance in the depletion region ($C_{HF}-\varphi_s$), and in experimental C-V measurement, the C-V relation is referred to as applied voltage ($C_{HF}-V_{gs}$) suffering from "stretch-out". This method gets $\varphi_s - V_{gs}$ by comparing the high frequency measured data with the theoretical calculated curve, since for sufficient high frequency, the trapped charges do not respond to the AC signal and the "stretch-out" is recorded. However, the extracted $\varphi_s - V_{gs}$ curve is also distorted, and that is because trapped charges follow the slow DC sweeping signal. The mapping method taken as an example of n-type substrate MOSCAP is illustrated in figure 3.5.

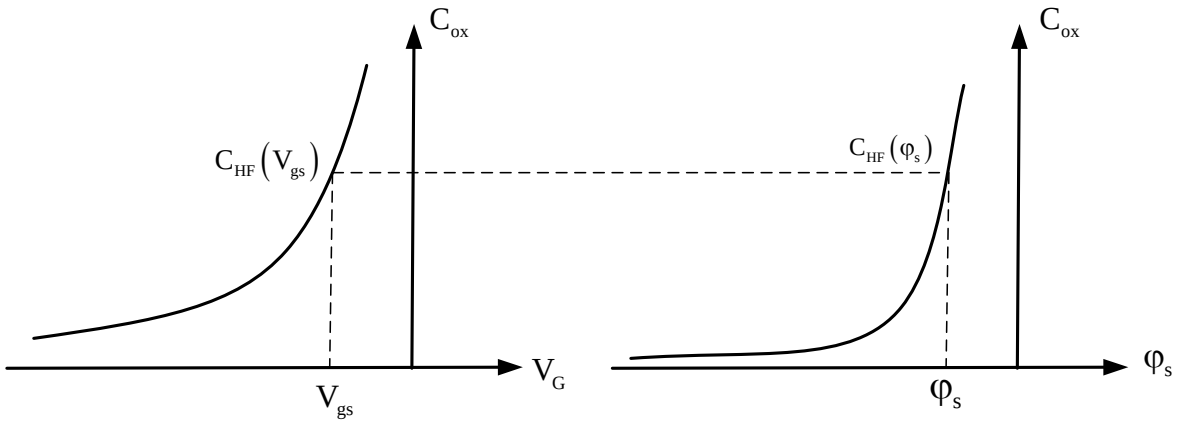

Fig. 3.5. Terman method maps the applied voltage to surface potential, using high frequency measurement data alone.

Once obtained the relation $\varphi_s - V_{gs}$, the voltage divider in equation (2.35) based on the capacitance model in figure 3.4 gives,

$$\frac{d\varphi_s}{dV_{gs}} = \frac{1/\,j\omega\left(C_s + C_{it}\right)}{1/\,j\omega\left(C_s + C_{it}\right) + 1/\,j\omega C_{ox}} = \frac{C_{ox}}{C_s + C_{it} + C_{ox}} \tag{3.18}$$

Recalling $C_{it} = qD_{it}$ and substituting into equation (3.18), the density of traps D_{it} is,

$$D_{it}\left(V_{gs}\right) = \frac{C_{ox}}{q}\left[\left(\frac{d\varphi_s}{dV_{gs}}\right)^{-1} - 1\right] - \frac{C_s}{q} \tag{3.19}$$

where $D_{it}\left(V_{gs}\right)$ is traps density as a function of applied voltage and q is the elementary charge. The depletion capacitance C_s can be extracted from high frequency measurement C-V curve in equation (3.16), and the differential part $d\varphi_s / dV_{gs}$ is calculated from equation (3.18). However, this method would underestimate trap density, and the extracted results are only reliable when $D_{it} > 10^{10}\,cm^{-2}eV^{-1}$ [47]. In addition, due to the limitation of equipment (1MHz for 4284A), it is hard to guarantee none of the carriers can follow.

3.4.2 Low-frequency method

The low frequency method is firstly used by Bergland [48], as a more accurate method to find trap density. Instead of differentiating $d\varphi_s / dV_{gs}$, this method determines the $\varphi_s - V_{gs}$ by integration. Rewriting equation (3.18),

$$\frac{d\varphi_s}{dV_{gs}} = \frac{C_{ox}}{C_s + C_{it} + C_{ox}} = 1 - \frac{C_s + C_{it}}{C_s + C_{it} + C_{ox}} = 1 - \frac{C_{LF}}{C_{ox}} \tag{3.20}$$

Note that the low frequency measured capacitance in equation (3.17) is applied. Based on the measured low frequency capacitance $C_{LF}(V_{gs})$, the surface potential can be integrated by selecting the proper range,

$$\varphi_s(V_{gs}) = \int_{V_2}^{V_{gs}} 1 - \frac{C_{LF}(V_{gs})}{C_{ox}} dV_{gs} + C \tag{3.21}$$

where C represents the integration constant, and V_2 is the selected integral limit.

It is necessary to select a starting point where φ_s has a weak dependency on V_{gs}, such as the accumulation region and flat band voltage. As illustrated in figure 3.6, the shaded area coloured with red represents the surface potential. Let V_2 start from accumulation, and when reaching flat band voltage $V_{gs} = V_{FB}$, the band bends at interface $\varphi_s(V_{FB}) = 0$. The integral constant C can be easily determined, which is the integration from accumulation to flat band voltage with minus sign in front.

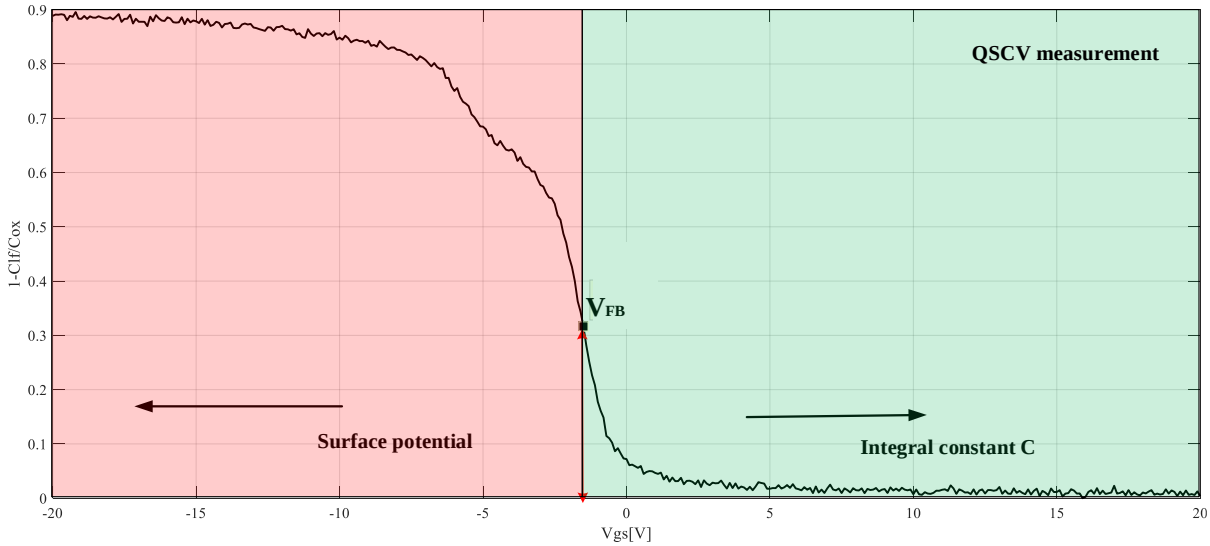

Fig. 3.6. Bergland integration and QSCV for MOSCAP with n-type substrate at room temperature. The green shaded area stands for the integral constant -A, which should be subtracted from whole integral. As a result, the area covered in red shaded region represents the $\varphi_s - V_{gs}$ relation.

This method requires high accuracy LFCV measurement and flat band voltage, but extraction of flat band voltage has uncertainty. The wider sweeping range of the signal voltage, the more accurate integrated results will be. However, large applied voltage may break down the device and bring a large leakage current, so this method is not applicable in SiC devices measurement.

3.4.3 High-Low method

The high-low method combined both HFCV and LFCV, firstly proposed by Castagne and Vapaille [49]. In contrast to using HFCV or LFCV alone, this method does not request any theoretical curve. Since the traps cannot follow the high frequency signal in HFCV, but be able to follow the LFCV, the traps induced capacitance C_{it} can be expressed by the difference between them. The following expression shows the relation,

$$C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}} \right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}} \right)^{-1} \tag{3.22}$$

where the second term is the depletion capacitance derived from high frequency C-V curve,

$$C_s = \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}} \right)^{-1} \tag{3.23}$$

Rearrange equation (3.22) giving,

$$C_{it} = C_{ox} \left(\frac{C_{LF}}{C_{ox} - C_{LF}} - \frac{C_{HF}}{C_{ox} - C_{HF}} \right) \tag{3.24}$$

Define the capacitance gap $\Delta C = C_{LF} - C_{HF}$, which is induced by interfacial traps. The difference equation (3.24) can be rearranged to a multiplication equation,

$$C_{it} = \Delta C \left(\frac{1}{1 - C_{HF} / C_{ox}} \right) \left[\frac{1}{1 - (\Delta C + C_{HF}) / C_{ox}} \right] \tag{3.25}$$

It is also worthwhile to note that the low frequency measurement curve is $C_{LF} = \Delta C + C_{HF}$, substituting them we get,

$$C_{it} = \Delta C \left(\frac{1}{1 - C_{HF} / C_{ox}} \right) \left(\frac{1}{1 - C_{LF} / C_{ox}} \right) \tag{3.26}$$

The capacitance induced by interface traps can be effectively extracted by using both normalised (to C_{ox}) high frequency curve and low frequency curve simultaneously. The interface trap density is directly proportional to the capacitance gap. The capacitance is a judgement of ability of holding charge carriers, and in a system, the larger capacitance is, the stronger charge holding ability it has. The traps captured by near interface traps cannot follow the measurement signal, and in fact, the response time of trapped charge (will be calculated in chapter 6) is slower than the majority charge carriers. Once the interface traps induced capacitance C_{it} with respect to applied voltage V_{gs} is determined, applying the $\varphi_s - V_{gs}$ relation obtained in the previous section (either from the Terman method or the low frequency method), the trap density with respect to band bending φ_s is easily extracted.

3.4.4 $C_d - \varphi_s$ method

This method is a modified version of the high-low method, firstly applied by Yoshioka [50]. Theoretically calculated depletion capacitance C_s in equation (2.23) is identical with the measurement result when applied frequency approaches infinite, at which frequency neither trapped charges nor minorities can follow. For trapped charges, the lower measurement frequency is; the more trapped charges can follow the measurement signal. For a large holding time in QSCV measurement (10s is used in the experiment, corresponding to 0.1Hz), all trapped charges can track the signal. Figure. 3.7 illustrates the capacitance as a function of surface potential under different sweeping frequencies.

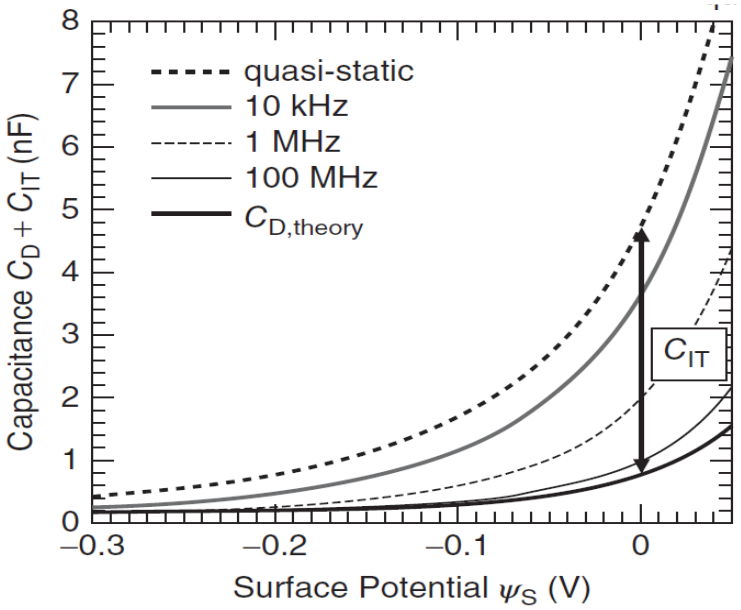

Fig. 3.7. C-V measurement under various measurement frequencies for SiC devices. The theoretical calculated capacitance is high frequency limit (infinite large frequency), whereas quasi static is the signal whose frequency approaches to zero approximately [50].

The capacitance gap between different applied frequencies is induced by interfacial traps. At high frequencies, no response can be observed and the trapped charges are "fixed charges" in this case. High frequency capacitance in equation (3.16) states the high frequency limit (bold line in Figure. 3.7 as follows,

$$\lim_{f\to+\infty}\frac{C_{HF}}{C_{ox}-C_{HF}}=\frac{C_s}{C_{ox}} \tag{3.27}$$

This equation can be inserted into (3.24), so that the traps density is determined by,

$$C_{it}=C_{ox}\left(\frac{C_{LF}}{C_{ox}-C_{LF}}-\frac{C_s}{C_{ox}}\right) \tag{3.28}$$

In depletion region, where in SiC devices $C_{ox} >> C_{LF}$, the interface capacitance is rounded by,

$$C_{it}\approx C_{LF,meas}-C_{s,theory} \tag{3.29}$$

3.5 Strength and weakness of extraction methods

To sum up, high frequency method, low frequency method, high-low method and $C_d - \varphi_s$ method are introduced to extract the distribution of interfacial trap states. Charge pumping method [51], subthreshold $I_d - V_{gs}$ method [52] and conductance method [53], will be analysed in detailed combining with physical model. Once $D_{it} - \varphi_s$ is known, the trap states distribution inside the band ($D_{it} - E$) can be obtained by equation (2.36).

In high frequency method, although the trapped charges cannot respond to the AC signal anymore, they can follow the DC sweeping signal which results in surface potential fluctuation and C-V curve "stretch out". As a result, the comparison with theoretical curves contains the trap information in $\varphi_s - V_{gs}$. However, this method is not accurate enough and leads to a large error for insufficiently high measurement frequency. That measurement error will be transferred into $\varphi_s - V_{gs}$ curve without any suppression. In addition, this method assumes uniform doping profile, and it means any out-diffusion or non-uniform doping causes error which is not controllable.

For the methods involving low frequency curve, also QSCV measurement, the ease of measurement and wide energy range promote these methods intensively. However, the QSCV requires the current measurement, which is extremely small (typically 10^{-15} A), to ensure quasi-equilibrium. The thin gate oxide may lead to leakage current, bringing error to the measurement. The thermal noise during measurement is also problematic. Fig. 3.8 compares the applicable energy range of various methods, taken from [54].

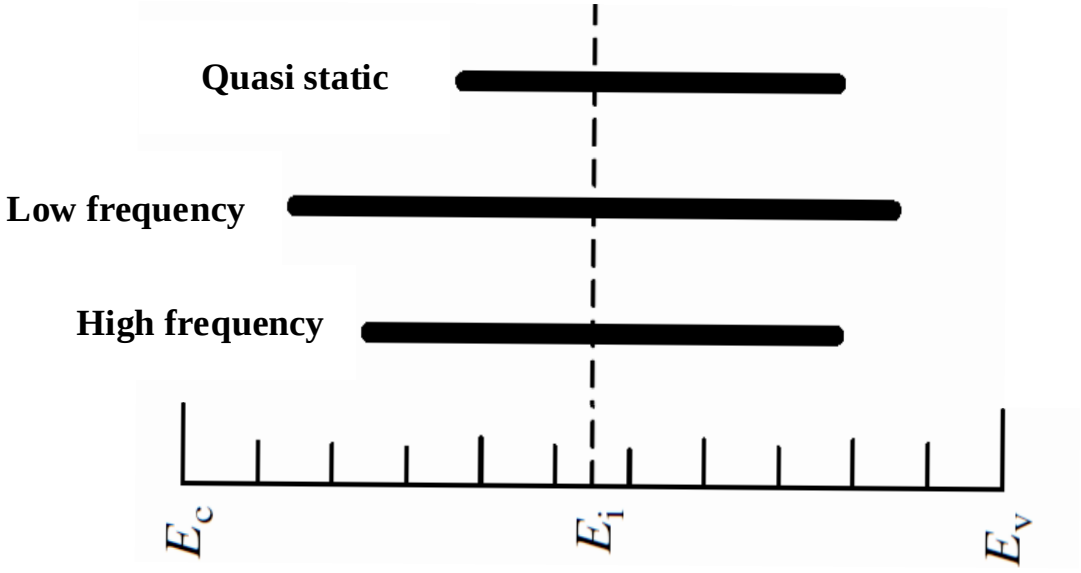

Fig. 3.8. Comparison of available energy range by different extraction method, to determine the trap state distribution in SiC devices [54].

4. Physical modelling of interface traps

Accurately modelling interface traps in SiC materials requires understanding charge transport within them, for effectively explaining of the reliability problems. The previous section has calculated the total interface trapped charge in the whole bandgap but leaves the behaviour of single traps at single energy level unknown. The total interface trapped charges are the statistical phenomenon of single energy level traps so that the abovementioned characteristic methods are limited and cannot explain single trapped charge behaviour. That brings obstacles of understanding the behaviour of interface traps and charge interaction mechanisms.

Although the poison's equation describes the charge distribution in real 3-dimentional system, the analysis of interfacial traps is based on the energy band diagram (k-space) which is energy space. The target of this chapter is to build a link between real world model and energy band diagram, build a detailed model using equivalent circuit, and describe the behaviour of single trap using Shockley-Read-Hall generation and recombination theory (SRH).

4.1 Interface traps in C-V measurement with LF small sinusoidal signal

The SRH theory, as its name indicated, was firstly investigated by Shockley, read and Hall in short. It successfully modelled the transition of a charge carrier between bands to localised states --- traps in our model. Several assumptions are provided for the validity of SRH theory.

- The generation and recombination process is instantaneous.
- Only one charge carrier can be occupied or released by one trap state.
- Doping profile is uniform and continuous in substrate.
- Charge interaction between trap to trap can be ignored.

There are four modes of charge interaction: electron capture from the conduction band, electron emission from the trap state; hole capture from the valance band and emission from traps, and all components contributes a nonzero current from gate to substrate. The n-type substrate MOSCAP is analysed as an example in this section. It is also worthwhile to note that in n-type substrate acceptor traps are dominant in the upper band, those who are neutral when accepting an electron, and show trap property when it is empty. Equivalently saying, for acceptor traps, the capture of electrons annihilates the traps, whereas the emission of electrons creates trap states. Fig. 4.1 illustrate the process of electron capture and emission for n-type substrate, exactly at energy level E_t, where the E_C and E_V are the conduction and valance band edge. The following shows the dynamic of charge interaction,

$$e^- + n_{it}^+ \Leftrightarrow n_{it}^o \tag{4.1}$$

where e^- represents electrons, n_{it}^+ stands for empty trap state with positive property, and the combination of them negatively charges the traps, which is neutralised n_{it}^o.

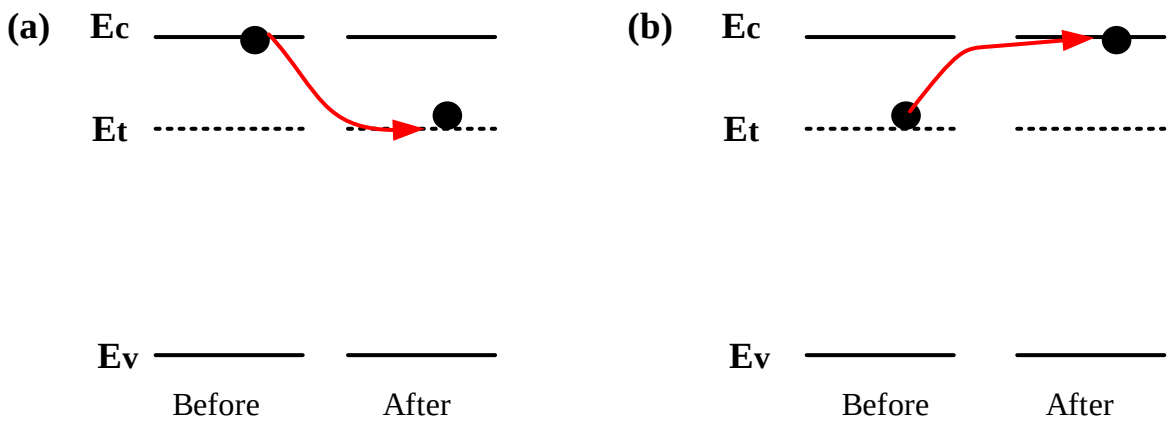

Fig. 4.1. Illustration of electron capture and emission in n-type substrate. (a) The electron at conduction band is captured by a trap state, then the trap state is neutralised and annihilated. (b) The trapped electron is emitted to conduction band, where the trap state becomes positively charged.

Provided that the occupancy probability of acceptor traps at a certain energy level E in equation (3.10), which is Fermi-Dirac statistics,

$$f = \frac{1}{1 + g_D \cdot \left(N_C / N_D\right) \cdot \exp\left[\left(E - E_C\right)/kT\right]} \tag{4.2}$$

Let the electron density in the depletion layer at surface be n_0, and the density of trap stats at energy level E is denoted by $D_{it}(E)$. The density of traps that are not occupied by electrons is $(1-f)D_{it}(E)$. The rate of electron capture is proportional to them, which turns out to be,

$$r_{n,c} = c_n n_0 (1-f) D_{it}(E) \tag{4.3}$$

where $r_{n,c}$ is the rate of electron capture (in the unit of $cm^{-3}s^{-1}$), representing left-hand side process in Fig. 4.1 (a), and c_n stands for capture cross section constant.

However, the emitted electrons only come from the occupied trap state, so for the density of traps which is full of electrons $fD_{it}(E)$, similarly, the rate of electron emission is proportional to the density of occupied traps,

$$r_{n,e} = e_n f D_{it}(E) \tag{4.4}$$

where $r_{n,e}$ is the rate of electron emission, and e_n represents emission cross section constant. This process is illustrated in right-hand side Fig. 4.1 (b).

The electron generation and recombination induced current by traps can be expressed by,

$$i_n(E) = q\left(r_{n,c} - r_{n,e}\right) \tag{4.5}$$

$$i_n(E) = qD_{it}(E)\left[c_n n_0 (1-f) - e_n f\right] \tag{4.6}$$

Ideally, in equilibrium, there is no vertical current flowing through the system, and $i_n = 0$. However, the external energy, for instance, the gate voltage and changing temperature, pushes the system into non-equilibrium. One method commonly used is C-V measurement, which applies a small ac signal superimposed to a dc sweeping signal, and brings non-equilibrium into the system. In that case, extra energy applies and breaks the balance of generation and recombination, leading to a nonzero current flowing from interface to substrate.

A sinusoidal small signal is applied to gate electrode, which can be split into dc and ac part,

$$V_{app} = V_{sweep} + \upsilon_{ac} \exp(j\omega t) \tag{4.7}$$

where υ_{ac} is the amplitude of small signal, ω is signal frequency, and $j = \sqrt{-1}$.

Since the concentration of the charge carrier n_0 at the surface is controlled by the applied voltage, and thus the Fermi level and occupancy probability are also varied. All relations are listed below, split into dc and ac part,

$$f = f_{dc} + \Delta f \tag{4.8}$$

$$n_0 = n_{dc} + \Delta n \tag{4.9}$$

To get non-equilibrium current, substituting equation (4.8) and (4.9) into (4.6) gives,

$$i_n(E) = qD_{it}(E)\left\{c_n(n_{dc} + \Delta n)\left[1 - (f_{dc} + \Delta f)\right] - e_n(f_{dc} + \Delta f)\right\} \tag{4.10}$$

Equation (4.10) is further expanded and ignoring the second order ac components,

$$i_n(E) = qD_{it}(E)c_n\left[n_{dc}(1 - f_{dc}) + \Delta n(1 - f_{dc}) - n_{dc}\Delta f\right] - qD_{it}(E)\left[e_n(f_{dc} + \Delta f)\right] \tag{4.11}$$

The dc component of the electron current should be zero since we have assumed an ideal oxide. To get dc part, set $\Delta f = \Delta n = 0$, and no current flowing through. Based on that,

$$i_n(E) = qD_{it}(E)\left[c_n n_{dc}(1 - f_{dc}) - e_n f_{dc}\right] = 0 \tag{4.12}$$

Simplifying equation (4.12), the following identity is obtained and used in equation (4.11),

$$c_n n_{dc}(1 - f_{dc}) = e_n f_{dc} \tag{4.13}$$

Substituting equation (4.13) back to equation (4.11) to eliminate e_n,

$$i_n(E) = qD_{it}(E)c_n\left[\Delta n(1 - f_{dc}) - n_{dc}\Delta f - n_{dc}(1 - f_{dc})\Delta f / f_{dc}\right] \tag{4.14}$$

The final result of transient current in non-equilibrium is,

$$i_n(E) = qD_{it}(E)c_n\left[\Delta n(1 - f_{dc}) - n_{dc}\Delta f / f_{dc}\right] \tag{4.15}$$

4.2 Admittance of single level interface trap

Recall the operational principle of the C-V measurement: the superimposed sweeping signal is applied to the DUT, where the response current is then detected and recorded, and the admittance/conductance (depending on which algorithm is chosen) is automatically calculated. This section will calculate the single state interface traps induced admittance when testing using low frequency C-V measurement.

Based on that, focusing on the single trap at certain energy level E, the admittance of single level interface trap can be expressed by,

$$i_n(E) = Y_n(E)\Delta\varphi_p(x) \tag{4.16}$$

Here $\varphi_p(x)$ is the band bending at position x, and this current is only due to the ac small signal induced trapped charge transportation. The following will prove that ac term of electron concentration Δn and occupancy probability Δf is proportional to the ac applied voltage.

Return to equation (2.7), the electron concentration at x is modelled by band bending,

$$n_n(x) = N_D \exp\left(\frac{q\varphi_p(x)}{kT}\right) \tag{4.17}$$

Differentiating equation (4.17) with respect to $\varphi_p(x)$ gives,

$$\Delta n_n(x) = \frac{qN_D}{kT}\Delta\varphi_p(x)\exp\left(\frac{q\varphi_p(x)}{kT}\right) = \frac{q}{kT}\Delta\varphi_p(x)n_n(x) \tag{4.18}$$

where $\varphi_p(x)$ is the band bending at position x, N_D is doping concentration at temperature T and $n_n(x)$ represents the electron concentration. Since the doping concentration at position x is fixed, in that case, the sinusoidal term $\Delta\varphi_p(x)$ [with the unit of V^{-1}] gives $\Delta n_n(x)$ a sinusoidal variation.

In particular, at the interface where $x = 0$, the variation of the electron concentration is,

$$\Delta n = \frac{q}{kT}\Delta\varphi_s n_0 \tag{4.19}$$

Equation (4.19) shows that the response of electron concentration to a sinusoidal applied voltage is sinusoidal. The ac applied signal υ_{ac} periodically attracts and repels the electrons at the interface. When in negative cycle, for n-type substrate, more positive charges are required and the system is more depleted. The band bends more and thus the Fermi level shifts downwards to midband accordingly. It suggests the occupancy probability also responds to the applied voltage. The definition of Fermi level is in equation (2.10), calculating derivative,

$$\Delta E_{FB} = \frac{1}{n_i}\frac{\Delta n_n(x)}{n_n(x)} = \frac{q}{kT}\frac{1}{n_i}\Delta\varphi_p(x) \tag{4.20}$$

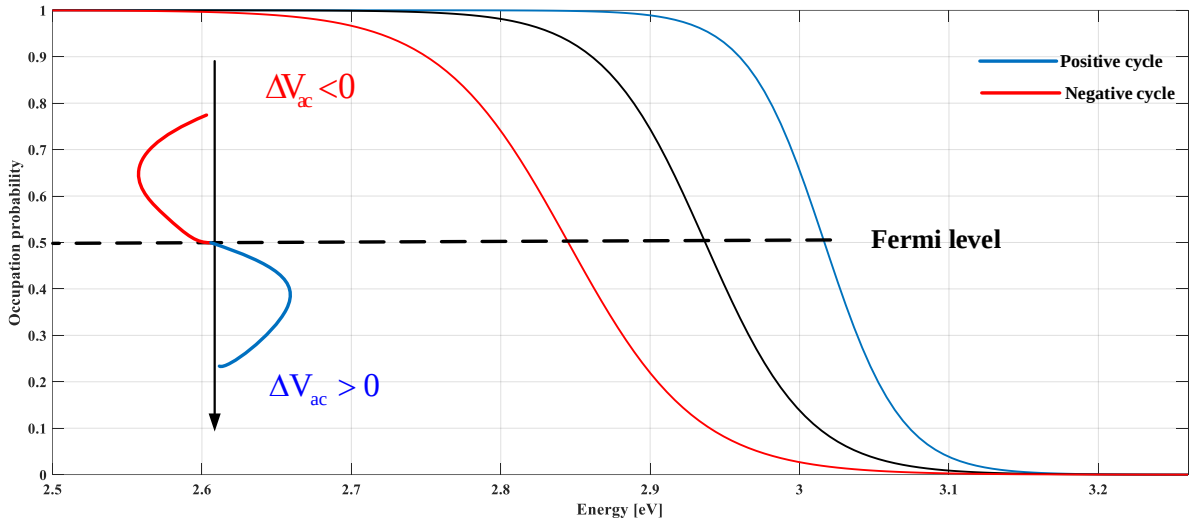

Fig. 4.2. Illustration of occupancy probability in bandgap from 2.5eV to 3.26eV, in n-type substrate, with doping concentration $5\times10^{15}\text{cm}^{-3}$. The Fermi level is labelled at which probability is exactly 0.5. If negative small signal is applied, the MOSCAP becomes more depleted than before, so that the Fermi level shifts towards midband.

The transient current equation in (4.15) is a function of energy level E and more importantly, it is also time dependent based on the applied sinusoidal signal. The transient current all comes from the electron capture and release of the occupied interfacial traps, whose dynamic density can be expressed by,

$$\text{i}_\text{n}\left(\text{E}\right)=\frac{\text{dQ}_\text{it}\left(\text{E}\right)}{\text{dt}}=\text{qD}_\text{it}\left(\text{E}\right)\frac{\Delta\text{f}}{\Delta\text{t}} \tag{4.21}$$

To eliminate the unknown terms, the time t, which is involved in the time dependent terms Δf, Δn and $\text{i}_\text{n}\left(\text{E}\right)$, now becomes the bridge between them. The occupation probability Δf has sinusoidal variation, so that,

$$\Delta\text{f}=\text{f}_\text{x}\exp\left(\text{j}\omega\text{t}\right) \tag{4.22}$$

where f_x is the amplitude of sinusoidal response.

The time derivative of the occupation probability is,

$$\frac{\Delta\text{f}}{\Delta\text{t}}=\text{j}\omega\text{f}_\text{x}\exp\left(\text{j}\omega\text{t}\right)=\text{j}\omega\Delta\text{f} \tag{4.23}$$

Focusing on the equation (4.21) and combining with equation (4.15), we solve the time derivative of the occupancy probability,

$$\frac{\Delta\text{f}}{\Delta\text{t}}=\text{j}\omega\Delta\text{f}=\text{c}_\text{n}\left[\ \Delta\text{n}\left(1-\text{f}_\text{dc}\right)-\text{n}_\text{dc}\Delta\text{f}\ /\ \text{f}_\text{dc}\right] \tag{4.24}$$

Substituting Δn from equation (4.18) and solving for Δf gives,

$$\Delta f = \frac{c_n \Delta n (1 - f_{dc})}{j\omega + c_n n_{dc} / f_{dc}} = \frac{q}{kT} \frac{c_n (1 - f_{dc}) \Delta \varphi_p (x) n_n (x)}{j\omega + c_n n_{dc} / f_{dc}} \tag{4.26}$$

Substituting Δf in equation (4.26) and Δn in equation (4.18) into transient current equation (4.15), yields,

$$i_n (E) = \frac{q^2}{kT} D_{it} (E) c_n \Delta \varphi_p (x) (1 - f_{dc}) n_n (x) \left(\frac{j\omega f_{dc}}{j\omega f_{dc} + c_n n_{dc}} \right) \tag{4.27}$$

For a fixed frequency ω, for any single state traps at energy level E and position x, the response of the small signal current is sinusoidal and expressed by equation (4.27). The current is proportional to the band bending variation $\Delta \varphi_p (x)$. The admittance caused by traps is defined in equation (4.16), expressed by,

$$Y_n (E) = \frac{q^2}{kT} D_{it} (E) c_n (1 - f_{dc}) n_n (x) \left(\frac{j\omega f_{dc}}{j\omega f_{dc} + c_n n_{dc}} \right) \tag{4.28}$$

In particular, at oxide-semiconductor interface, where $x = 0$,

$$Y_n (E) = \frac{q^2}{kT} D_{it} (E) (1 - f_{dc}) \left(\frac{1}{j\omega f_{dc}} + \frac{1}{c_n n_{dc}} \right)^{-1} \tag{4.29}$$

When oscillation frequency $\omega \to 0$, the admittance is zeroed and no dc component exists. Furthermore, the admittance can be divided into the real part and the imaginary part, where the real part is conductance G [in Siemens], and the imaginary part represents susceptance B [also in Siemens] or capacitance C [in Farads].

$$Y = G + Bj = G + j\omega C \tag{4.30}$$

Splitting the admittance in equation (4.29) gives the real part conductance,

$$G_{it} (E) = \frac{q^2}{kT} D_{it} (E) (1 - f_{dc}) \left(\frac{1}{c_n n_{dc}} + \frac{c_n n_{dc}}{\omega^2 f_{dc}^2} \right)^{-1} \tag{4.31}$$

This conductance has a maximum when frequency $\omega \to \infty$, when the energy loss is minimised,

$$\lim_{\omega \to \infty} G_{it} (E) = \frac{q^2}{kT} D_{it} (E) (1 - f_{dc}) c_n n_{dc} \tag{4.32}$$

To find out the imaginary part, the trap induced capacitance is,

$$C_{it} (E) = \frac{q^2}{kT} D_{it} (E) (1 - f_{dc}) f_{dc} \tag{4.33}$$

4.3 Band diagram, capacitance and conductance in single state

At a fixed temperature (no extra charge carrier is activated) and without UV light illumination, the only reason pushing the system into non-equilibrium is the applied voltage. The following section establishes the band diagram and traps occupation analysis after a negative voltage are applied to n-type substrate 4H-SiC, to find out the energy loss during electrons capture and release process.

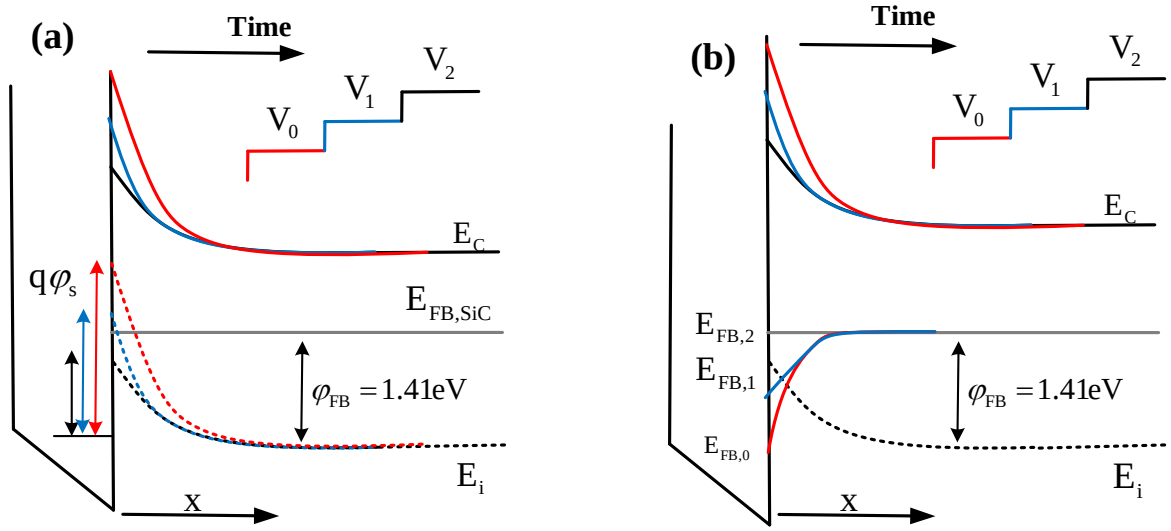

Fig. 4.3. Upper band diagram of n-type substrate 4H-SiC when different gate voltages applied, with doping concentration $5\times10^{15}\,\mathrm{cm}^{-3}$ and 300K temperature. (a) Using $E_{FB,SiC}$ reference; (b) Using E_i reference.

The band diagram of n-type substrate MOSCAP is shown in Fig. 4.3, biased in depletion. To begin with, given an initial negative voltage V_0, the voltage then increases to $V_2 > V_1 > V_0$. In this case, the negative charges are demanded, and the MOSCAP is less depleted than before and fewer electrons are repelled to the bulk. The band bends less at V_2 than the initial condition V_0. It has been proved in equation (4.18) that the concentration of the surface charge carrier is controlled by the applied voltage, also proportional to the Fermi energy $E_{FB}-E_i$, which is illustrated by the dashed line on the left-hand side in Fig. 4.3 (a). The E_i in band diagram in Fig. 4.3 (a) is plotted using the reference of $E_{FB,SiC}$, where $E_{FB,SiC}$ retains as constant. The right-hand side band diagram establishes an equivalent illustration whose reference is E_i, keeping $E_{FB}-E_i$ identical to the left-hand side diagram. Both of them are equivalent but used a different reference.

The Fermi level represents the hypothetical energy of electrons in a system, at which state the occupancy probability is exactly 50%. That means the Fermi level can be solved if let $f=0.5$ in equation (4.2). The hypothetical energy of electrons is the average energy of electrons, which is a description of electron activity. The electron gains higher energy and may be easier to react, break the bonds or interact with other atoms. Typically, breaking bonds, electron-hole pairs and emission electrons from trap centres consume energy from SiC lattice.

Given exponentially distributed trap states in the band diagram, plotted blue solid line in Fig. 4.4, the trap occupancy subjects to the applied voltage is discussed. Taking n-type substrate MOSCAP as an example, it is the acceptor trap dominating in the upper band, which shows positive when empty; and becomes neutral when the trap is full of electron. Fig. 4.4 also plots the band diagram in the depletion region when biased in a negative voltage, and the Fermi level coloured red stands for a negative ac voltage variation. Since more positive charges are required, which are ionised from dopant atoms so that the band bends more, more electrons are pushed away and the depletion region expands. The occupation of trap states, illustrated by the red shaded area, also reduces due to negative ac small signal. The empty states instead, which show the trap property, are increased. That is because more empty states are ready to capture the electrons from the conduction band, and the device is more unstable. Because of the exponentially distributed trap states, the trap induced capacitance C_{it} is more sensitive near the flat band voltage, where the covered area is exponentially dropped. This phenomenon is also confirmed in Fig. 3.7 [50], where larger capacitance gap is observed near the flat band voltage than the deep depletion region.

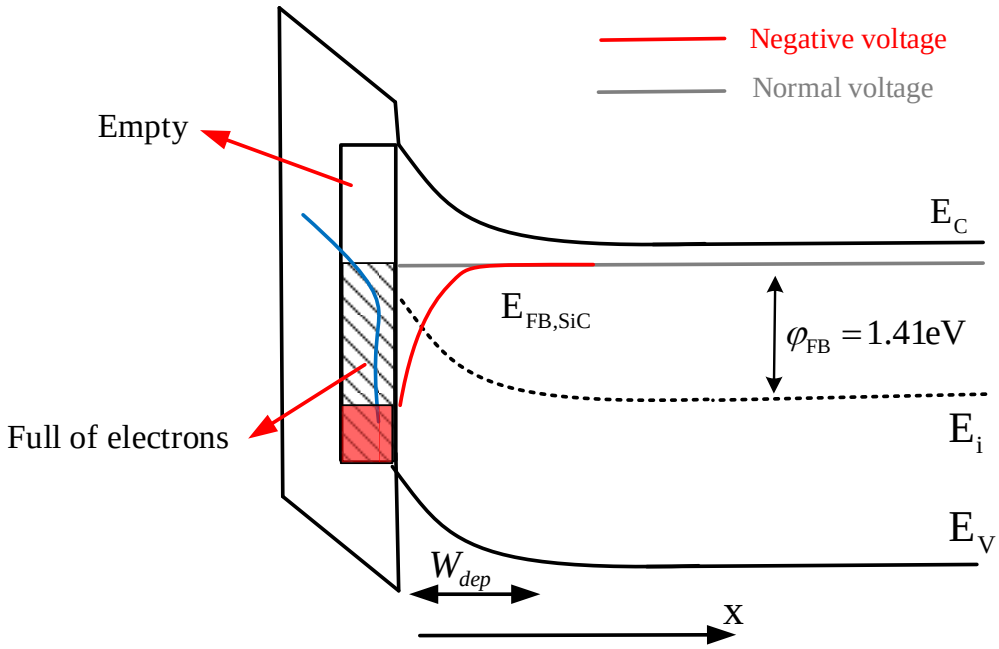

Fig. 4.4. Band diagram of n-type substrate 4H-SiC, with doping concentration $5\times10^{15}\,cm^{-3}$ and 300K temperature. The shaded area is the acceptor traps in band that full of electrons. The blue curve represents the exponentially distributed traps.

After examining the traps induced capacitance, the following analyses the finite conductance in equation (4.31), which suggests a nonzero energy loss. Here, we analyse the dynamic before the steady state. At the instance when an ac signal is applied, the system receives energy from the power supply. In the 4H-SiC substrate, there are two types of charges that respond: majority carriers from dopant atoms and trap states capture or release. However, the response time of them differs, and typically trap states response are slower than the majority charges. The consequence is that the variation of the shaded area (trap occupation) cannot follow the red Fermi level (majority charges). The received energy immediately ionises the dopant atoms, but the trapped charges are left behind.

For an n-type substrate 4H-SiC, biased in deep depletion, when negative cycle ac small signal is applied, the dopant atoms are ionised immediately, breaking the electron-dopant pair. However, the emission of the trapped electrons from the phonons lags behind, taking longer time to thermalize and stabilise in the substrate again, illustrated in the shaded black area in Fig. 4.4. In Fig. 4.1 (b), the emitted trapped electrons are pushed to the conduction band, with higher average energy than the electrons at interface that not released (red shaded area). More importantly, the average energy of the emitted trapped electrons is above the electrons in the substrate. During this period, these electrons firstly receive energy from the phonons to de-trap, and then overcome the barrier and lose energy ($q\varphi_s$) until they stabilise and reach the average electron energy in the substrate again. The trapped electrons decelerate and lose energy, probably due to the Coulomb collision and electron-phonon collision, and the wasted energy turns to the heat upon the SiC lattice, and modelled by equation (4.31).

The frequency of the applied ac signal also dominates. If the frequency is so high that the trapped charges cannot respond to the alternative Fermi level, the phonons cannot supply energy to the trapped electrons and the journey from interface is terminated beforehand. As a result, the energy loss is less and the equivalent conductance drops, supporting equation (4.31).

As a result, it is reasonable to introduce a finite conductance to model the energy loss for the interfacial traps. The time spent from the initial condition to the final stabilised state is the time constant or the lifetime of the travelling charge carriers $C_{it}R_{it}$ [with the unit of second]. The trapped charges can only follow the signal whose frequency is below $\left(C_{it}R_{it}\right)^{-1}$, and for frequency above that, the transportation terminates and the trapped charges return. The lifetime is from equation (4.31) and (4.32), with respect to energy level E and position x,

$$\tau_{it}\left(E,x\right)=\left(C_{it}R_{it}\right)^{-1}=\left(C_{it}/G_{it}\right)^{-1}=\frac{c_n n_{dc}\left(x\right)}{f_{dc}\left(E\right)} \tag{4.34}$$

The equivalent circuit of the single state interface traps can be considered as a RC system, and further converted by admittance $Y_p=G_p+j\omega C_p$ in parallel, which is illustrated in Fig. 4.5.

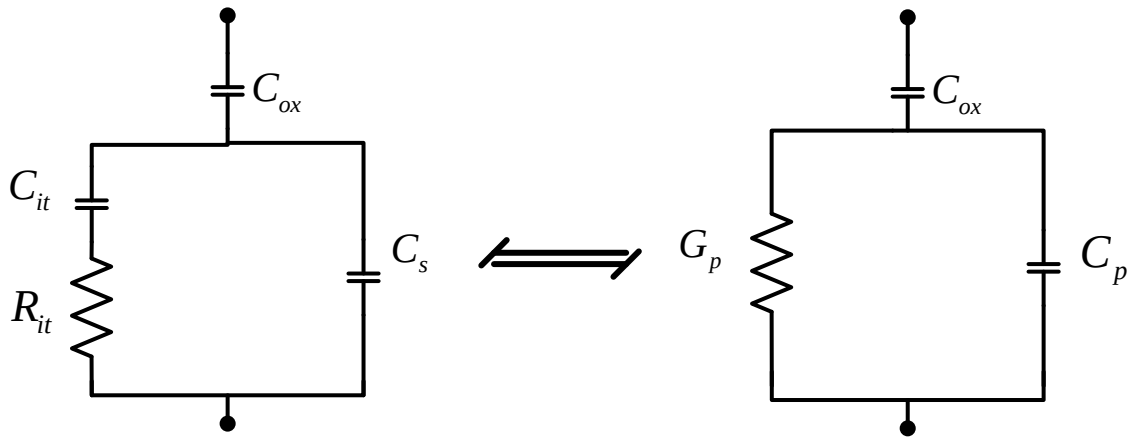

Fig. 4.5. Equivalent circuit of single state of interface traps in low frequency; left: RC system and right: admittance system.

The left-hand side diagram has the impedance (without gate capacitance),

$$\left(R_{it} + \frac{1}{j\omega C_{it}} \right) \Bigg\| \frac{1}{j\omega C_s} = Z_p = \frac{1}{Y_p} \tag{4.35}$$

This equation is simplified to,

$$\left\{ \frac{\omega^2 C_{it} \tau_{it}}{1+\omega^2 \tau_{it}^2} + j\omega \left(\frac{\omega^2 \tau_{it}^2 C_s + C_s + C_{it}}{1+\omega^2 \tau_{it}^2} \right) \right\}^{-1} = Z_p = \frac{1}{Y_p} \tag{4.36}$$

It is straightforward to get trap induced capacitance and conductance by measurement,

$$G_p = \frac{\omega^2 C_{it} \tau_{it}}{1+\omega^2 \tau_{it}^2} \tag{4.37}$$

$$C_p = \frac{\omega^2 \tau_{it}^2 C_s + C_s + C_{it}}{1+\omega^2 \tau_{it}^2} = C_s + \frac{C_{it}}{1+\omega^2 \tau_{it}^2} \tag{4.38}$$

where C_s is depletion capacitance, theoretically calculated in equation (2.23).

Rearrange conductance in equation (4.37) and divide by signal frequency ω,

$$\frac{G_p}{\omega} = \frac{\omega C_{it} \tau_{it}}{1+\omega^2 \tau_{it}^2} \le \frac{C_{it}}{2} \tag{4.39}$$

The function G_p / ω with respect to ω has a peak $C_{it}/2$ at $\omega = \tau_{it}^{-1} = \left(C_{it} R_{it} \right)^{-1}$. It suggests that the time constant (lifetime) of trapped charge is clearly measured by extracting the maximum point of G_p / ω, using frequency sweeping of the C-V measurement.

Remember that the gate oxide capacitance is excluded in equation (4.36). To get fully measured capacitance and conductance,

$$\frac{1}{G_p + j\omega C_p} + \frac{1}{j\omega C_{ox}} = Z_m = \frac{1}{Y_m} \tag{4.40}$$

where Y_m represents the measured admittance from impedance analyser. Splitting it into real part and imaginary part yields, both of them have the gate oxide capacitance C_{ox},

$$G_m = \frac{\omega^2 G_p C_{ox}}{G_P^2 + \omega^2 \left(C_{ox} + C_p \right)^2} \tag{4.41}$$

$$C_m = \frac{\omega^2 \tau_{it}^2 C_s + C_s + C_{it}}{1+\omega^2 \tau_{it}^2} \tag{4.42}$$

4.4 Equivalent circuit and trap states for multiple energy levels

Equation (4.25) and (4.28) in previous sections describe the transient current and admittance induced by single trap state at energy level E. For exponentially distributed trap states in the bandgap, the equivalent circuit should be modified into a paralleled combination of RC systems, which is shown in Fig. 4.6. All traps located at the same energy level belong to the same RC network so that the interfacial traps with same index i all contribute to the trap induced capacitance $C_{it,i}$ and conductance $G_{p,i}$.

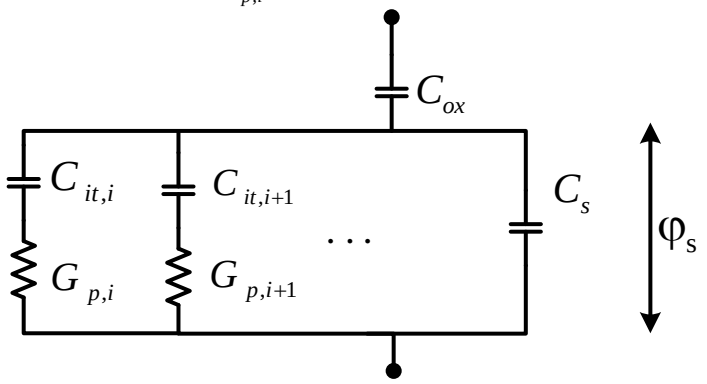

Fig. 4.6. Equivalent circuits for multiple traps at multiple energy levels, illustrated the energy level E_i and E_{i+1}.

Taking an n-type substrate MOSCAP as an example, focusing on the whole interface, in that system, the small signal transient current originates from the capture and release of electrons. Based on equation (4.5) and (4.15), the charge variation near the interface $Q_{it}(E)$ at the energy level E with respect to time equals to,

$$\frac{dQ_{it}(E)}{dt} = i_n(E) = qD_{it}(E)c_n\left[\Delta n(1-f_{dc}) - n_{dc}\Delta f / f_{dc}\right] \tag{4.43}$$

The total charge variation at the interface comes from the depletion region and interface traps so that the net charge variation is the sum of them,

$$dQ_{Total} = dQ_s + \sum dQ_{it}(E) = dQ_s + q\sum D_{it}(E)\Delta f \tag{4.44}$$

where Q_s is the depletion charge calculated in equation (2.19) and plotted in Fig. 2.4. $Q_{it}(E)$ represents the trapped charges inside the bandgap at a certain energy level E, which is referred to equation (3.7).

The total transient current considering all interfacial traps among the bandgap can be calculated by combining equation (4.43) and (4.44) together. However, the parameters in equation (4.43) such as capture rate c_n, are hard to extract and model. To solve that problem, the circuit components G_{it} and C_{it}, which are measurable and observable in the equivalent circuit in Fig. 4.6, are substituted back to simplify equation (4.43).

The key step solving the transient current is to find Δf , which is already given in equation (4.26),

$$j\omega\Delta f = c_n\left[\ \Delta n\left(1-f_{dc}\right)-n_{dc}\Delta f\ /\ f_{dc}\right] \tag{4.45}$$

Here we use conductance equation in (4.32) to eliminate the first term and time constant in equation (4.34) for the second term, and rearrange them giving,

$$\Delta Q_{it}\left(E\right)=\Delta f\left[\ qD_{it}\left(E\right)\right]=\frac{C_{it}\left(E\right)G_{it}\left(E\right)\Delta\varphi\left(x\right)}{j\omega C_{it}\left(E\right)+G_{it}\left(E\right)} \tag{4.46}$$

Equation (4.46) represents the trapped charges at certain energy level, and the sum of them should be,

$$\sum\Delta Q_{it}\left(E\right)=\sum\frac{C_{it}\left(E\right)G_{it}\left(E\right)}{j\omega C_{it}\left(E\right)+G_{it}\left(E\right)}\Delta\varphi\left(x\right) \tag{4.47}$$

It is worthwhile to note that the denominator is $Y_P\left(E\right)=j\omega C_{it}\left(E\right)+G_{it}\left(E\right)$, which is the admittance at a certain energy level E. For the energy level near the conduction band edge, where the occupancy probability $f_{dc}\rightarrow 0$ and D_{it} is exponentially increased, the conductance G_{it} is so large that the equation (4.47) can be simplified to,

$$\sum\Delta Q_{it}\left(E\right)=\sum C_{it}\left(E\right)\Delta\varphi\left(x\right) \tag{4.48}$$

Equation (4.48) suggests that the trapped charge fluctuates both C-V curve and the $\varphi_s - V_{gs}$ curve. If the deflection $\Delta\varphi\left(x\right)$ is independent for each energy level E, it is easy to rewrite,

$$C_{Total,it}=\sum C_{it}\left(E\right)G_{it}\left(E\right)Y_p^{-1} \tag{4.49}$$

The final step is to find the expression of depletion charges dQ_s. Recall equation (2.20),

$$dQ_s=-C_s\Delta\varphi\left(x\right) \tag{4.50}$$

The total transient current now is expressed by circuit components in the equivalent circuit. Since the current is time dependent, transferring to the frequency domain simplifies the analysis. The depletion capacitance in equation (4.50) is added, and the response of the net electron current under sinusoidal signal is,

$$i_n\left(E\right)=-j\omega\left(C_{Total,it}+C_s\right)\Delta\varphi\left(x\right) \tag{4.51}$$

At low frequency, since the single level trap response $j\omega C_{it}\left(E\right)$ approaches zero, the net trapped charge in equation (4.47) is proportional to $\sum C_{it}\left(E\right)$. From equation (4.49) and (4.47), the net trap induced capacitance is added up to the depletion capacitance C_s, since all traps can follow the low frequency signal. The trapped charge can be expressed by equation (4.48), which is exactly identical to the trapped charge at the conduction band edge when $f_{dc}\rightarrow 0$.

For high frequency, the finite conductance is negligible compared with $j\omega C_{it}(E)$ and Y_P shows capacitance properties. The total interface induced capacitance $C_{Total,it}$ is completely eliminated, leaving the depletion capacitance C_s alone. That is the reason why the difference between low-high C-V measurement curves gives information on interfacial traps.

For mid-frequency signals, also the range of interest, Y_P is not pure where the influence of conductance starts to dominate, and physically, it originates from the energy loss due to the interfacial trapped charges transportation. Fig. 4.7 illustrates the equivalent circuit combined with the energy band diagram.

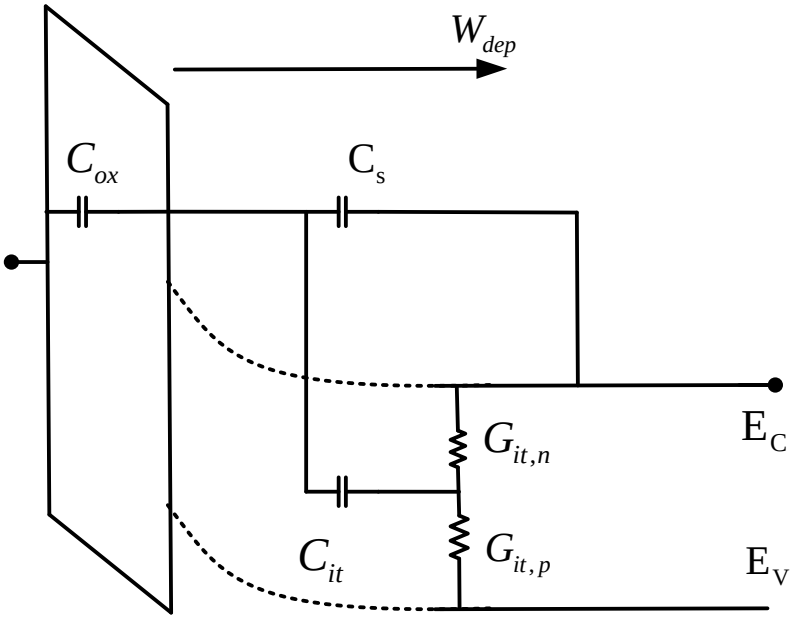

Fig. 4.7. Equivalent circuit combines with energy band diagram. The oxide capacitance, depletion capacitance, trap capacitance and conductance are labelled.

The equivalent circuit shows how an electron passes from gate electrode to the substrate with thermal equilibrium, and how an electron transports from trap states to conduction band until stabilised. From SiC-oxide interface to substrate electrode, there are two possible pathways: one contributes to the depletion capacitance, which is responsible for majority charge carriers with extremely short response time; another is the capture and release of interfacial traps, involving the finite conductance induced by energy losses with long time constant $\tau_{it}(E,x)$.

The band bending (dashed line) at the surface ($q\varphi_s$) is controlled by the external signal. Since in n-type substrate, the upper part of the bandgap is occupied by acceptor traps and electrons, the electron terminates to the conduction band edge. As a result, the trapped charges inside the bandgap activated from the trapping centre with high energy are decelerated by the conductance $G_{it,n}$. For the oscillation frequency above $\tau_{it}^{-1}(E,x)$, the trapped charge cannot follow the alternative Fermi level, which returns to the interface before being thermalized, and only part of the conductance takes effect and generates heat.

Similarly, in p-type substrate where holes and donor traps dominate, the terminal of charge transportation is valance band edge. The dynamic of holes' transportation is

$$h^+ + n_{it}^o \Leftrightarrow n_{it}^+ \tag{4.52}$$

The following studies the movement of holes, when the electron-holes pair breaks, the donor traps give and donate electrons, equivalently saying, capture holes from the valence band, leading to a positive state, and the state is empty; on the other hand, the capture of electrons (emission of holes) neutralise the state, where it is full.

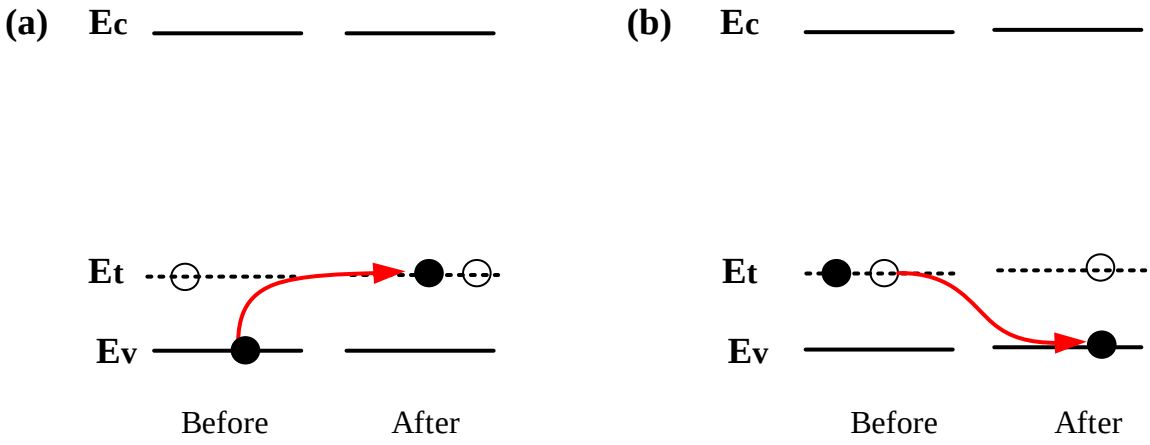

Fig. 4.8. Illustration of holes' capture and emission in p-type substrate. (a) The electron at valance band is captured by donor trap state, and the trap is full then the trap state is neutralised and annihilated. Equivalently, hole is released. (b) The electron-hole pair is broken and electron is emitted to conduction band, equivalently hole is captured, and the trap state is empty, where the trap state becomes positively charged.

The capture of holes, essentially, is due to the emission of electrons to the valance band. This rate is proportional to the occupied trap states $fD_{it}(E)$, and given hole concentration p_0 and hole capture rate c_p, the rate of hole capture should be,

$$r_{p,c} = c_p p_0 f D_{it}(E) \tag{4.53}$$

Similarly, the rate of hole emission comes from the capture of electron, which is proportional to the empty states, which turns out to be,

$$r_{p,e} = e_p(1-f)D_{it}(E) \tag{4.54}$$

The hole induced transient current is expressed by,

$$i_p(E) = q\left(r_{p,c} - r_{p,e}\right) \tag{4.55}$$

$$i_p(E) = qD_{it}(E)\left[\, c_p p_0 f - e_p(1-f)\,\right] \tag{4.56}$$

Split the occupancy frequency and holes concentration as before, and the hole induced transient current now becomes,

$$i_p(E) = qD_{it}(E)c_p\left[\Delta n f_{dc} - p_{dc}\Delta f/(1-f_{dc})\right] \tag{4.57}$$

Carefully comparing the electron and hole contributed current in equation (4.6) and (4.55) respectively, the hole induced current in equation (4.56) can be obtained by substituting f_{dc} by $1-f_{dc}$, since the occupation relation of holes and electrons is complimentary.

The occupancy probability variation is also dependent with applied small signal, substituting f_{dc} to $1-f_{dc}$ yields,

$$\Delta f = \frac{q}{kT}\frac{c_p f_{dc}\Delta\varphi_p(x)p_p(x)}{j\omega + c_p p_{dc}/(1-f_{dc})} \tag{4.58}$$

The holes induced admittance now can be determined by,

$$Y_n(E) = \frac{q^2}{kT}D_{it}(E)c_p f_{dc} p_p(x)\left(\frac{j\omega(1-f_{dc})}{j\omega(1-f_{dc}) + c_p p_{dc}}\right) \tag{4.59}$$

where the conductance and capacitance extracted from admittance are,

$$G_{it}(E) = \frac{q^2}{kT}D_{it}(E)f_{dc}c_p p_{dc} \tag{4.60}$$

$$C_{it}(E) = \frac{q^2}{kT}D_{it}(E)(1-f_{dc})f_{dc} \tag{4.61}$$

Since the holes are imaginary positive charge carriers, it is the electrons that actually transport and interact with the valance band, so that the occupancy of electrons is substituted by $1-f_{dc}$. Note that the induced capacitances for both n-type substrate and p-type substrate are identical, suggesting that the charge holding ability is independent of doping types.

The time constant (lifetime) for emitted holes from traps is,

$$\tau_{it}(E,x) = (C_{it}R_{it})^{-1} = (C_{it}/G_{it})^{-1} = \frac{c_p p_{dc}(x)}{1-f_{dc}(E)} \tag{4.62}$$

In conclusion, donor traps and acceptor traps exist at the same time in the Oxide-semiconductor interface. However, in 4H-SiC devices whose minority and intrinsic charge carriers are not comparable with trapped charges and majority carriers, it is approximated that only one type of conductance appears in equivalent circuit. The equivalent circuit components, used to describe the physical transportation of the trapped charge, are controlled by oscillation frequency and its own energy level. The nonzero conductance represents the net energy loss during the transportation when the trapped charges reach thermal equilibrium.

5. Temperature effects analysis and modelling

Chapter 4 highlights the response current and admittance under sinusoidal small signal, especially the interfacial traps induced conductance and capacitance in quasi-static condition, under QSCV measurement. This section covers the behaviour and measurable phenomenon under non-equilibrium conditions. One of the most commonly encountered situations is changing temperature, due to either external environment or internal heat, causing reliability problems and even crashing the devices. Common circumstances that push the system into non-equilibrium are listed in the following.

- Temperature variation.

When temperature varies, the equilibrium condition no longer holds. Both oxide-semiconductor interface and semiconductor substrate are affected. For example, the excess carriers are generated, the doping atoms are further ionised, and the trap distribution are altered, which change the Fermi level and occupancy probability accordingly.

- Applied voltage.

Chapter 4 has analysed and modelled the response under external voltage with various frequencies. The occupancy frequency and concentration of free mobile charge carriers are proportional to the amplitude of the applied signal. In addition, the response is also sensitive to the oscillation frequency. For low frequency measurement, the trapped charges experience a complete journey from interface to substrate until they are decelerated and thermalized. Although, under high frequency measurement which is hard for trapped charges to follow, the traps also fluctuate the C-V curve and a clear “sketch-out” can be observed.

- UV light illumination.

UV light illumination can generate sufficient excess charges, thus increasing the concentration of minority charge carriers to form an inversion layer. However, the power (300W), irradiation angle and wavelength of exposure light (256nm) should be strictly controlled to create a “Si-like” low frequency C-V [55]. However, the equipment in C-V measurement probe station, unfortunately cannot support a high power UV light source for SiC, and in this project, the analysis of UV light illumination is not covered.

It can be concluded that any applied external source such as temperature increment or applied signal, results in the redistribution of occupation probability, and the device moves from equilibrium to non-equilibrium. As the dominating components, the depletion region capacitance C_s, reflecting the movement of majority charges and the ionisation of the doping atoms, should be determined first in next section.

5.1 Doping impurities ionisation

The majority charge carriers originate from the ionization of dopant atoms so the depletion capacitance C_s is a temperature dependent parameter. The 4H-SiC sample used in project is doped by N^+ implantation in n-type substrate [27], where the nitrogen atoms substitute the carbon atoms with ionisation energy of $61.4meV$ [56]. The p-type substrate is doped by Al^+, replacing the silicon site with the ionisation energies of $197.9meV$ and $201.3meV$ [56], respectively. Due to the high ionisation energy and wide bandgap, the doped aluminium atoms cannot fully ionise in SiC at room temperature, also called the "freeze out" effect.

The dopant atoms give electrons or holes only when they receive sufficient energy, and that energy comes from either the applied voltage source or external heating environment. A proper bias voltage creates a depletion region, in which dopant atoms are fully ionised even at room temperature, since the band bends enough in the space charge region and the electrical field pushes the charge carriers away. For the region not affected by the external applied electrical field, the temperature variation breaks the steady state. The following calculates the dependency between ionisation rate and charge carrier concentration with respect to temperature.

Assume that the intrinsic charge carrier concentration is negligible ($n_i << N_D^- \le N_D$), where N_D is doping concentration when fully ionised, and $N_D^- = n$ represents the concentration of the atoms that are already ionised. The concentration of donor atoms can be expressed by [57],

$$N_D^- = \frac{N_D}{1 + g_D \exp\left(\frac{E_{FB} - E_D}{kT}\right)} \le N_D \tag{5.1}$$

where E_{FB} is the Fermi energy, E_D represents the energy state for donor and $g_D = 2$ stands for the electrons ground-state degeneracy [45].

In SiC, all dopant atoms in the space charge region can be considered depleted, since the ionization rate is dramatically boosted by the external electrical field. For n-type substrate with donor atoms under a certain applied voltage V_{app}, the ionization rate now turns out to be,

$$\frac{N_D^-}{N_D} = \frac{1}{1 + g_D \cdot \left(n / N_C\right) \cdot \exp\left(\frac{E_C - E_D + qV_{app}}{kT}\right)} \tag{5.2}$$

where $V_{app} < 0$ reduces the barrier for donor electron to be activated into the conduction band, and just $V_{app} = -2.51V$ can fulfil the gap and provide sufficient energy to ionize the dopant atoms in the space charge region, which is achievable when the MOSCAP is biased in depletion mode.

Using similar method substituting equation (3.10) to eliminate the Fermi energy E_{FB} leads to the electron concentration as a function of the energy barrier $E_C - E_D$,

$$N_D^- = \frac{N_D}{1 + g_D \cdot (n / N_C) \cdot \exp\left(\frac{E_C - E_D}{kT}\right)} = n \tag{5.3}$$

where n is the electron concentration in the substrate and N_C represents the available states on the conduction band. Equation (5.3) is a solvable quadratic equation: $N_D = n(1 + Mn)$. Given the ionisation energy $E_C - E_D = 61.4meV$, the computable temperature dependent parameter $M(T)$ now becomes,

$$M(T) = \frac{g_D}{N_C} \exp\left(\frac{E_C - E_D}{kT}\right) \tag{5.4}$$

The solution of free electron concentration in the quadratic equation yields doping concentration for the single level ionisation state. Only for the positive solution,

$$n = \frac{\sqrt{1 + 4MN_D} - 1}{2M} \tag{5.5}$$

The ionisation rate of donors is temperature dependent, and the following Fig. 5.1 simulates the free electron concentration normalized to N_D as a function of temperature, calculated by equation (5.5). The substrate doping concentration in n-type sample used in this project is $5 \times 10^{15} cm^{-3}$, and the ionisation rate is above 90% even at room temperature. For substrate with large doping concentration, the ionisation rate drops, suggesting that the ionisation rate is sensitive to both doping concentration and temperature. That is because the electrons from dopant atoms at high temperature with higher energy are easier to jump through the barrier.

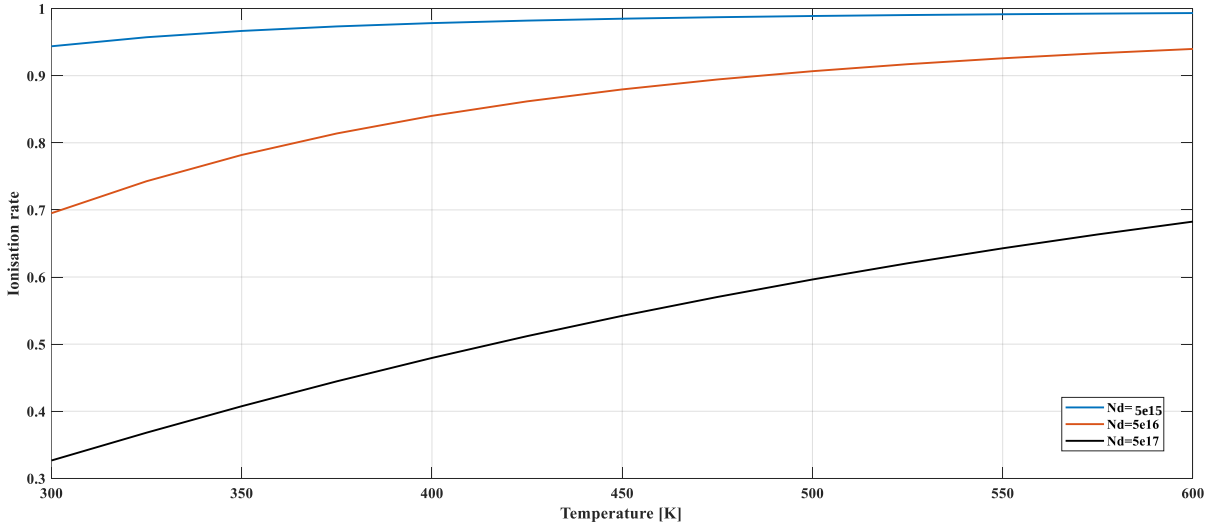

Fig. 5.1. Simulation of ionisation rate of n-type substrate doping by N^+ implantation with concentration of $5 \times 10^{15} cm^{-3}$, $5 \times 10^{16} cm^{-3}$ and $5 \times 10^{17} cm^{-3}$, from 300K to 600K.

In contrast, acceptor atom Al^+ has double ionisation energy states, whose barriers are also larger than donor atoms N^+, with ionisation energy states of $E_{A1}-E_V=197.9meV$ and $E_{A2}-E_V=201.3meV$, respectively [56]. The sum of ionised atoms at both states should be the net concentration when completely ionised, $N_A=N_{A1}+N_{A2}$. The holes' concentration in substrate turns out to be,

$$p=\sum_{i=1,2}\frac{N_{Ai}}{1+g_A\cdot\left(p/N_V\right)\cdot\exp\left(\frac{E_{Ai}-E_V}{kT}\right)}=N_A^- \tag{5.6}$$

where N_A^- is the concentration for incomplete ionisation, and the hole ground-state degeneracy is $g_A=4$ [45]. The ionisation barriers to overcome from the acceptor states to the valance band are $E_{Ai}-E_V$. However, the numerical expression is not straightforward for equation (5.6), which is a cubic equation, so that only the computer calculated results of ionisation rate with respect to temperature are shown for the sample $1\times10^{16}cm^{-3}$ in Fig. 5.2.

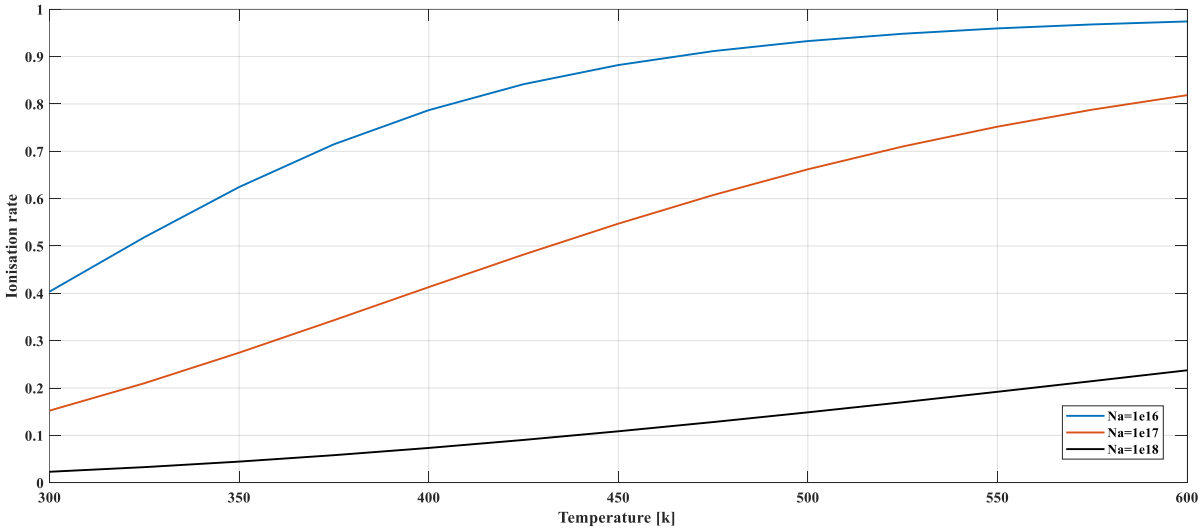

Fig. 5.2. Simulation of ionisation rate of p-type substrate doping by Al^+ implantation with concentration of $1\times10^{16}cm^{-3}$, $1\times10^{17}cm^{-3}$ and $1\times10^{18}cm^{-3}$, from 300K to 600K.

The simulation gives the results when $N_{A1}=1/3N_A$, and it suggests that fewer acceptor atoms than donors are activated at room temperature. Clearly, the temperature sensitivity in the p-type substrate 4H-SiC device is worse than the n-type device. The following calculates the temperature dependency of the Fermi level.

Taken n-type substrate as an example,

$$\varphi_{FB}(T)=\frac{kT}{q}\ln\left(\frac{N_D(T)}{n_i(T)}\right) \tag{5.7}$$

where $N_D(T)$ is the concentration of ionised dopant atoms which is temperature sensitive considering ionisation, and $n_i(T)$ represents the concentration of the intrinsic carriers.

The temperature dependence is obtained by calculating the derivatives,

$$\frac{\partial \varphi_{FB}}{\partial T} = \frac{k}{q} \ln\left(\frac{N_D(T)}{n_i} \right) - \frac{kT}{q} \frac{d\left(\ln\left(n_i\right)\right)}{dT} \tag{5.8}$$

where n_i is a strong function of temperature,

$$n_i(T) = \sqrt{N_c N_v} \exp\left[-\frac{E_g}{2kT} \right] \tag{5.9}$$

where N_c and N_v are the density of allowed states at the conduction and valence band edge, respectively. Both of them are also temperature dependent parameters,

$$N_c = 2\left(\frac{2\pi m^* kT}{\hbar^2} \right)^{\frac{3}{2}} \tag{5.10}$$

where m^* is effective mass of electrons, and $\hbar$ is the reduced Plank constant.

Since N_c and N_v are both proportional to $T^{1.5}$, the intrinsic carrier concentration in equation (5.9) now updates to,

$$n_i = GT^{\frac{3}{2}} \exp\left[-\frac{E_g}{2kT} \right] \tag{5.11}$$

where constant G is a temperature independent constant.

Substituting equation (5.11) back to (5.8), the sensitivity of intrinsic charge carrier should be,

$$\frac{d\left(\ln\left(n_i\right)\right)}{dT} = \frac{3}{2T} + \frac{E_g}{2kT^2} \tag{5.12}$$

The temperature dependency of Fermi level in equation (5.8) now is,

$$\frac{\partial \varphi_{FB}}{\partial T} = \frac{k}{q} \left\{ \ln\left[\frac{N_D(T)}{n_i(T)} \right] - \frac{E_g + 3kT}{2kT} \right\} \tag{5.13}$$

Investigating equation (5.13), for 4H-SiC with $E_g = 3.26\text{eV}$ and moderate doping concentration, $\partial \varphi_{FB} / \partial T < 0$. Although more charge carriers are ionised from the dopant atoms at high temperature, the Fermi level still drops away from the band edge. That is because the rising temperature cannot compensate for the effect of large bandgap $E_g = 3.26\text{eV}$. At room temperature, $\partial \varphi_{FB} / \partial T = -6.345\text{eV/K}$. As a result, the Fermi level has a negative temperature coefficient, and it is pushed towards the midband E_i. The conclusion is also valid for the p-type substrate, and the Fermi level approaches towards the midband if rising temperature.

5.2 Intrinsic threshold voltage temperature dependency

The previous section 3.3 discussed the threshold voltage considering non-idealities in real MOSCAP, with interface trapped charges, fixed charges and mobile charges This section calculates the temperature sensitivity of the ideal part of the threshold voltage. Taken n-type substrate SiC as an example and the ideal part taken from equation (3.3) with all temperature related terms are highlighted,

$$V_{th,ideal}(T) = \varphi_{ms} + 2\varphi_{FB}(T) - \frac{\sqrt{\left|4\varepsilon_c q N_D(T)\varphi_{FB}(T)\right|}}{C_{ox}} \tag{5.14}$$

where the temperature sensitive coefficient Fermi level is given by equation (5.7), and $N_D(T)$ represents the concentration of the ionised atoms as a function of temperature.

Find the derivative of the ideal part of the threshold voltage in equation (5.8) with respect to temperature giving that,

$$\frac{\partial V_{th,ideal}}{\partial T} = 2\frac{\partial \varphi_{FB}}{\partial T} - \frac{\sqrt{4\varepsilon_{SiC} q N_D}}{2C_{ox}\sqrt{|\varphi_{FB}|}}\frac{\partial \varphi_{FB}}{\partial T} \tag{5.15}$$

The temperature sensitivity of the Fermi level obeys equation (5.8). Substituting it back to equation (5.15) gives the temperature dependency of the threshold voltage,

$$\frac{\partial V_{th,ideal}}{\partial T} = \frac{k}{q}\left(2 - \frac{\sqrt{4\varepsilon_{SiC} q N_D}}{2C_{ox}\sqrt{|\varphi_{FB}|}}\right)\left\{\ln\left[\frac{N_D(T)}{n_i(T)}\right] - \frac{E_g + 3kT}{2kT}\right\} \tag{5.16}$$

It is worthwhile to note that for moderate doping concentration, the variation of threshold voltage is always negatively proportional to the Fermi level. As a result, the ideal threshold voltage part has a positive temperature coefficient. Taken n-type substrate with doping concentration $5\times10^{15}\,cm^{-3}$ as an example, at room temperature,

$$\ln\left[\frac{N_D(T)}{n_i(T)}\right] - \frac{E_g + 3kT}{2kT} = -9.8244 < 0 \tag{5.17}$$

For n-type substrate whose ionisation rate reaches over 90%, the donor concentration N_D is stable and the ratio $N_D(T)/n_i(T)$ drops dramatically at high temperature. Substituting all parameters into equation (5.16) at room temperature $T = 300K$, the threshold voltage temperature dependency in this sample is,

$$\left.\frac{\partial V_{th,ideal}}{\partial T}\right|_{T=300K} = 0.002(V/K) \tag{5.18}$$

The intrinsic threshold voltage as a function of temperature in equation (5.14) is simulated in Fig. 5.3, from 300K to 500K. The intrinsic threshold voltage at room temperature is equal to $-3.7323V$ and further increases to $-3.3207V$ when the temperature rises to $T=500K$. From the figure, the sensitivity on average is $0.002058V/K$, which supports the theoretical calculation in equation (5.18). More importantly, the threshold voltage has good linearity, which gives the potential for temperature sensor design.

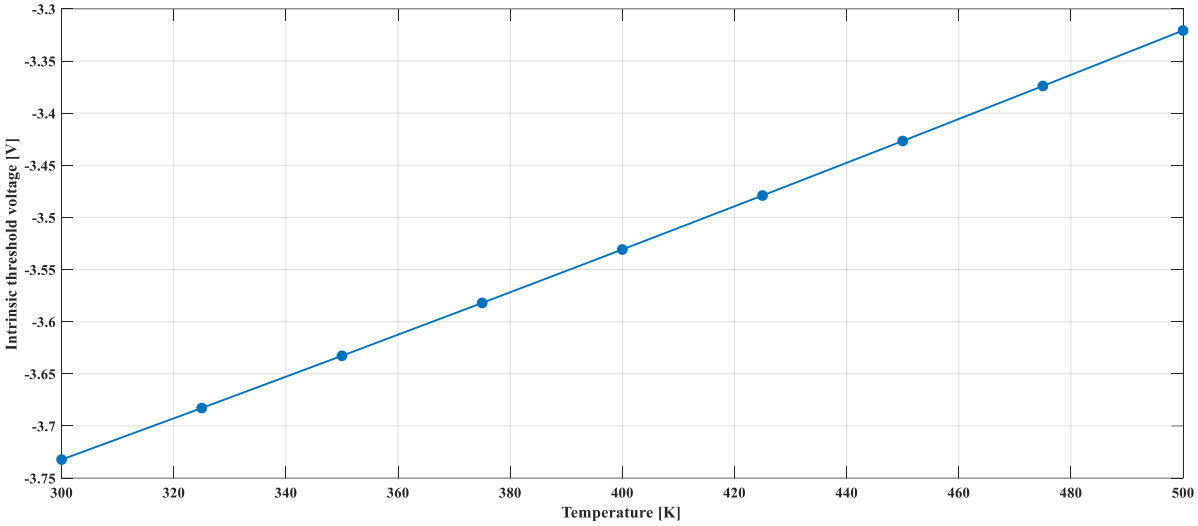

Fig. 5.3. Simulation results of intrinsic threshold voltage of n-type substrate MOSCAP, with doping concentration of $5\times10^{15}cm^{-3}$, from 300K to 500K.

The threshold voltage in p-type substrate is positive, and the ionisation of acceptor atoms is more sensitive to temperature due to the large activation energy gap. The minus sign in equation (5.14) turns to positive sign, leading to a negative temperature coefficient. From $300K$ to $350K$, the density of ionised atoms increases dramatically so that the nonlinearity shows up in that range. The MOSCAP with n-type substrate is more reliable compared with p-type MOSCAP, especially at moderately high temperature.

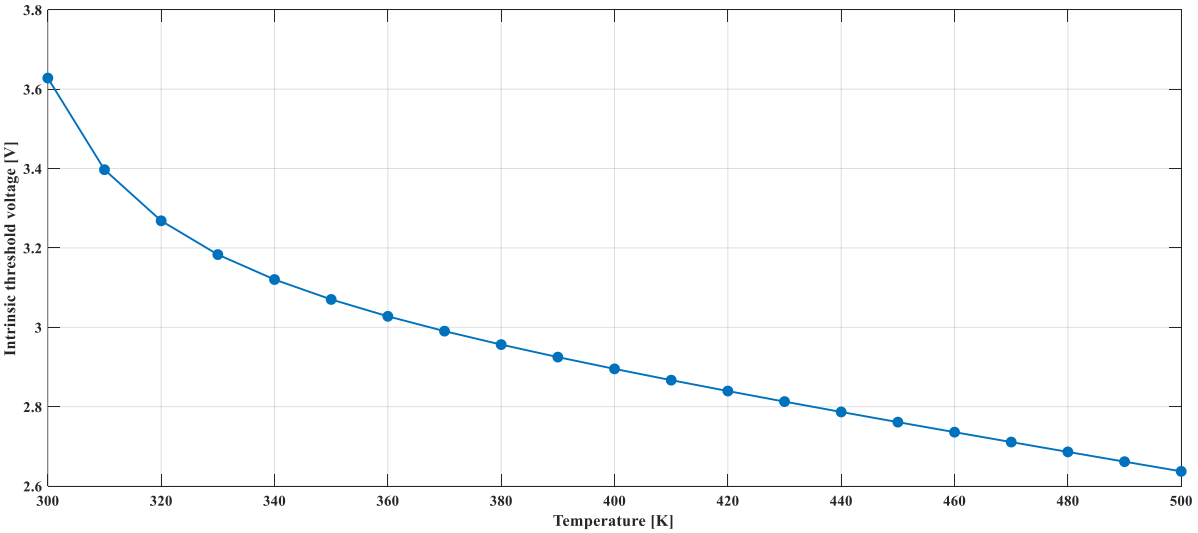

Fig. 5.4. Simulation results of intrinsic threshold voltage of p-type substrate MOSCAP, with doping concentration of $1\times10^{16}cm^{-3}$, from 300K to 500K.

5.3 Depletion region, occupancy probability and trapped charges at high temperature

The circuit components in chapter 4 that were used to represent the mechanism of the charge transportation, include depletion capacitance, trap capacitance and conductance for energy losses. This section analyses their temperature degradation of them, to explain the reason for threshold voltage instability behind it.

The property of the depletion region is analysed first, based on the ionisation rate mentioned in the previous section. The depletion capacitance in equation (2.20) can be estimated by the depletion region width $C_s = \varepsilon_{SiC} / W_{dep}$. Since the Fermi level has a negative temperature coefficient, shown in equation (5.17), at high temperature, the Fermi level is pushed away and the band bends less. The number of depleted atoms in the space charge region should increase to compensate for the electrical field. The following numerically shows the depletion region as a function of temperature.

Assume the substrate is uniformly doped, and for an n-type SiC biased in the depletion region, the surface charge $Q_{s,SiC}$ is obtained by substituting the electrical field in equation (2.19),

$$Q_{s,SiC} = \sqrt{-2\varepsilon_{SiC} q \varphi_s n_{n0}} = qN_D W_{dep} \tag{5.19}$$

where n_{n0} is the electron concentration in the substrate, $\varphi_s < 0$ is the band bending at the oxide-semiconductor surface, which keeps unchanged no matter how temperature varies. That is because, in equation (2.26), the surface potential φ_s is determined by the electrical field at the interface. The electrical field at the oxide-SiC interface $F_{SiC}(0,0)$ is temperature independent since all temperature related parameters are cancelled out. For example in depletion mode when $\varphi_s < 0$, in equation (2.17), the electrical field at surface $F_{SiC}(0,0) \propto \sqrt{-\varphi_s}$, and the thermal voltage term "V_t" is fully eliminated.

The right-hand side part, N_D represents the density of ionised atoms in the space charge region, where all donor atoms are fully activated by the electrical field induced by the applied voltage if $V_{app} < -2.51V$, shown in equation (5.2). It means these atoms cannot be further ionised even if at high temperature. Based on that, the depletion width W_{dep} increases at high temperature, since more electrons are activated due to ionisation.

For the substrate whose dopant atoms are not fully ionised, at moderate temperature, the depletion capacitance is dropped since for an expanded depletion region, the differential capacitance $C_s = \varepsilon_{SiC} / W_{dep}$ reduces. For moderate high temperature and the intrinsic carrier concentration is still negligible $n_i << N_D$, neither dopant atoms ionised electrons are further generated, and the depletion region capacitance cannot decrease more. When heating to extremely high temperature that the intrinsic carrier dominates, the electron concentration increases again, the analysis is similar to the Si device. In that case, the electrical field is enhanced, the depletion width is narrowed, and the depletion capacitance increases.

Fig. 5.5 illustrates the band diagram of n-type MOSCAP biased in depletion and takes incomplete ionisation into account. The red line represents the Fermi level under high temperature, which is pushed away from the conduction band according to equation (5.13). In addition, a depletion width expansion at high temperature is also illustrated. The electrical field at the SiC-oxide interface keeps unchanged when temperature varies, and that is the reason why the slope of Fermi levels at the interface in Fig. 5.5 are identical.

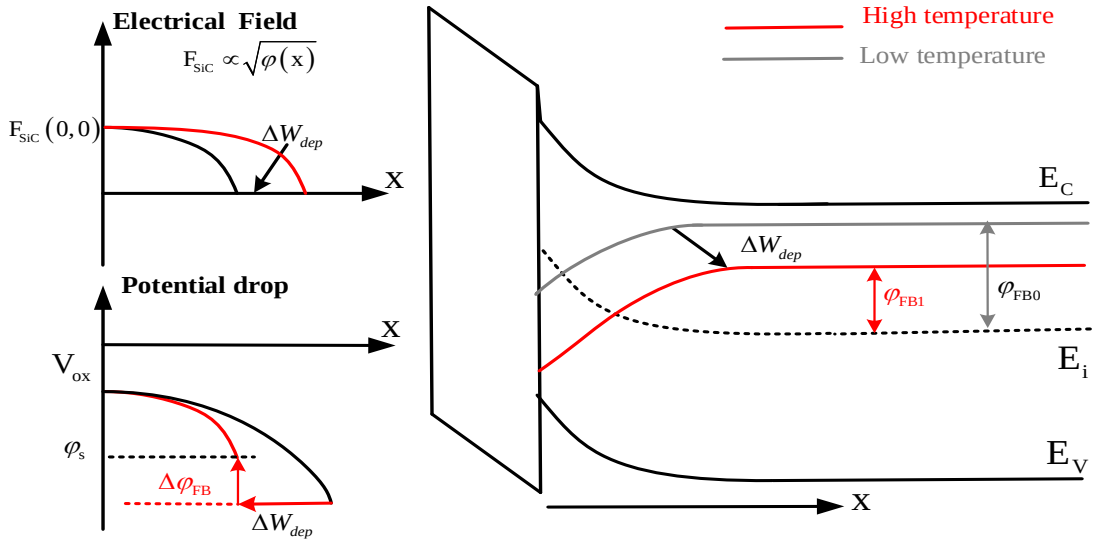

Fig. 5.5. Band diagram variation when temperature rises (coloured with red curve). The Fermi level at substrate approaches to band edge, and surface bending is extended.

The occupancy of trapped charge is already concluded in chapter 4 and it is proportional to the applied voltage. More importantly, the occupancy probability is also sensitive to temperature, since the high temperature activated charge carriers in the substrate are energetic and interact more with trap states. Fermi level is the energy level where the occupancy probability is exactly 50%, and equation (5.13) calculates the temperature dependency of it. The reduction of the Fermi level indicates a decrement of trapped state occupancy probability, and Fig. 5.6 simulates the occupancy probability at different energy levels, from 300K to 700K. The lower occupancy probability is, the more empty states waiting for electrons to capture electrons from the conduction band. As a result, high temperature degrades the quality of the SiC-oxide interface.

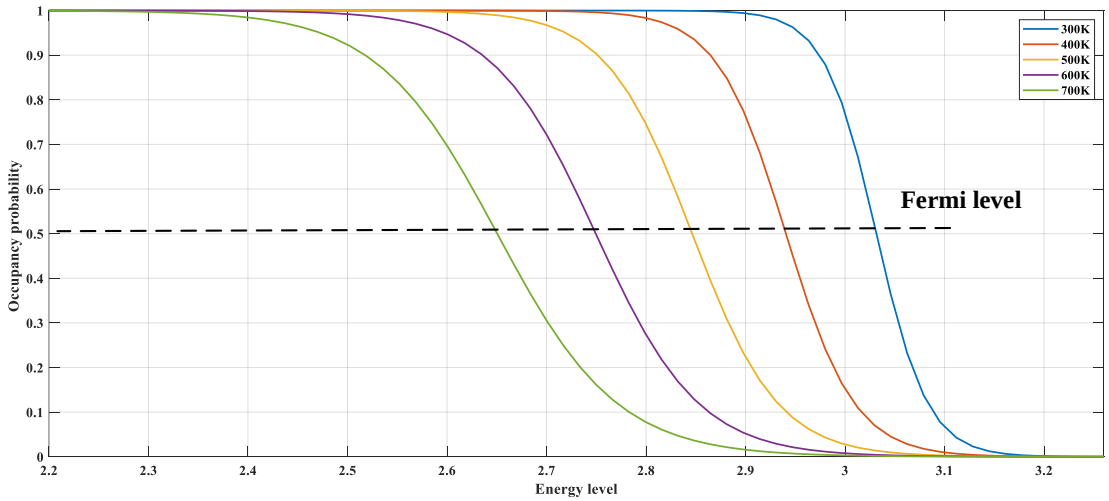

Fig. 5.6. Illustration of probability of a trap occupied by an electron, inside upper band.

The trap induced transient current also increases, suggesting that the SiC-oxide interface has frequent charge interaction between trap centres to the conduction band. According to equation (4.6), rearranging it gives,

$$i_n(E) = qD_{it}(E)\left[c_n n_0 - f(c_n + e_n) \right] \tag{5.20}$$

where the occupancy probability f has a negative temperature. Hence, the induced transient current increases at high temperature.

Examining a 4H-SiC MOSCAP at high temperature, the dc component of the transient current should be zero when the system is in equilibrium. Equation (4.13) states the relation between capture and release of electrons,

$$c_n n_{dc}(1 - f_{dc}) = e_n f_{dc} \tag{5.21}$$

The left-hand side describes the capture process, enhanced by high temperature due to the positive temperature coefficient $1 - f_{dc}$. To guarantee the identity, the emission cross section e_n should dramatically increase to compensate for the reduction of occupancy probability.

The diagram Fig. 5.7 also illustrates the temperature dependency of the trapped charges inside the upper part of the bandgap, by integrating the $Q_{it} - E$ curve. After heating, although fewer charge carriers are trapped in unit time, the capture and emission processes are both enhanced. The rising temperature breaks the equilibrium condition, hence more trapped charges are transported and more empty trap states are ready for recombination, resulting in an observable transient current from trap centres to substrate. As a consequence, the SiC-oxide interface degrades more.

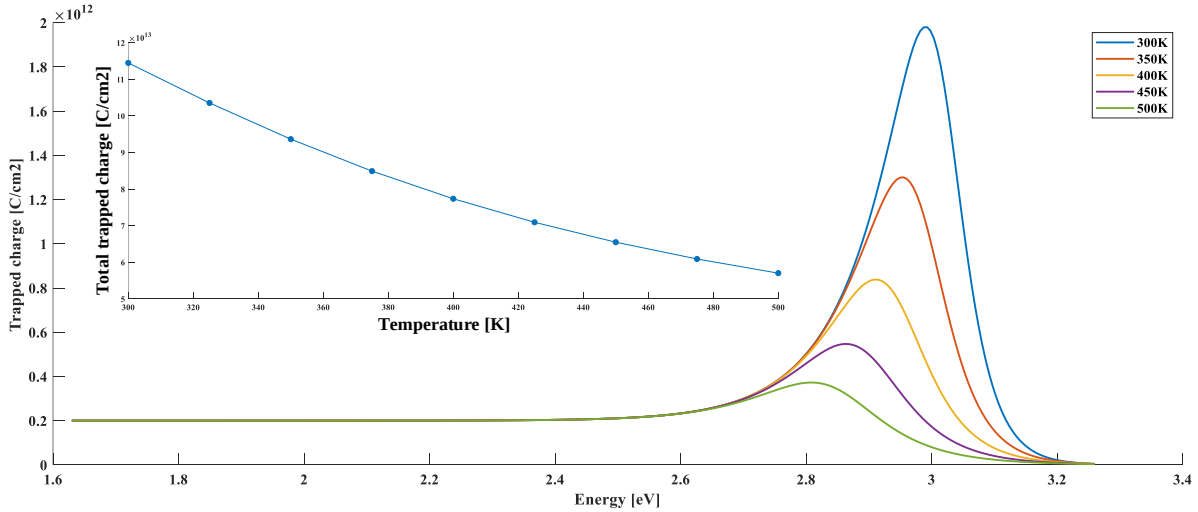

Fig. 5.7. Illustration of interface trapped charge; Temperatures are chosen from 300K to 500K, calculated for n-type substrate MOSCAP with doping concentration of $5 \times 10^{15} cm^{-3}$. The trapped charges as a function of temperature is also shown.

5.4 Charge transportation and equivalent circuit at high temperature

The variation of the depletion region Δn and occupancy probability Δf at high temperature breaks the steady-state. The transient current, determined by Δf and Δn in equation (4.15), is clearly temperature dependent. Taken MOSCAP with an n-type substrate as an example, this section analyses the charge transportation at high temperature in the interface.

Equation (5.22) taken from (4.18) states the temperature dependency of the electron concentration $n_n(x)$, with "$1/V_t$" in front, and the increment of the ionisation rate cannot compensate for the reduction of "$1/V_t$" once the dopant atoms are fully ionised. As a result, Δn is a negative temperature coefficient at high temperature. The higher temperature is, the less density of positive charges achieves, and the Δn reduces and is negatively proportional to the temperature.

$$\Delta n_n(x) = \frac{q}{kT}\Delta\varphi_p(x)n_n(x) \tag{5.22}$$

The occupancy probability Δf and Fermi level variation also have negative temperature dependency, according to Fig. 5.6. The variation of occupancy probability leads to trapped charge transportation from interface to substrate, and causes an observable transient current induced by trapped charges $i = dQ_{it}/dt$. The band diagram after heating the device is illustrated in Fig. 5.8, with exponentially distributed trap states indicated.

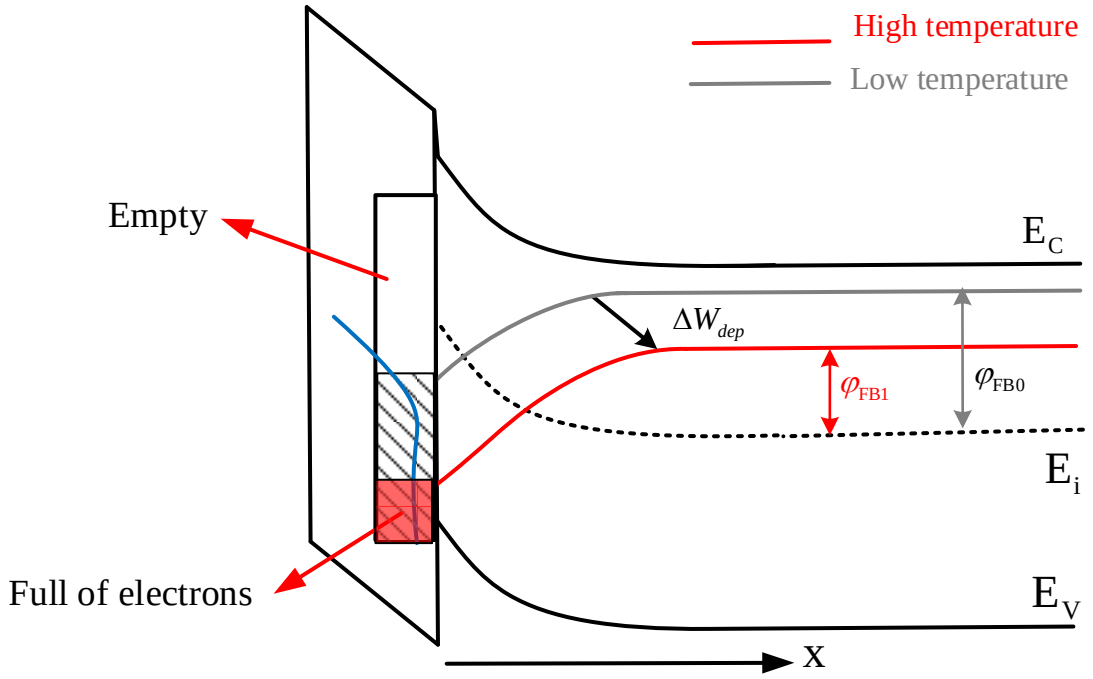

Fig. 5.8. Band diagram of n-type substrate 4H-SiC, with doping concentration $5\times10^{15}cm^{-3}$. The high temperature is coloured red, and the shaded black area represents the electrons whose average energy is above the Fermi level.

The majority charges (electrons) induced Fermi level variation is instantaneous, which is faster than the response time of trapped charges. At the instant when temperature rises, the Fermi level coloured red drops but the trapped charges lag behind. The steady-state is broken since the average energy of the electrons that are still trapped (black shaded area) are higher than the average energy of the electrons in the substrate. Those electrons with higher energy tend to have a lower energy state until they are thermalized. As a consequence, the released electrons from trap centres overcome the barrier (the band bending), decelerate and generate heat. It is worthwhile to note that the Fermi level in substrate also reduces at high temperature, reducing the barrier between interface and substrate, which makes the emitted electrons easier to stabilise. Also at high temperature, the SiC lattice vibrates more, the SiC crystal cell expands and the Coulomb collision are enhanced. For a reduced barrier, the time consumed to be thermalized (lifetime of trapped charges) should decrease.

The analysis of equivalent circuit equations in chapter 4 also gives self-consistent conclusions. For the trapped charges induced capacitance, taken from equation (4.32), both f_{dc} and $1/V_t$ has negative temperature coefficient, and the temperature dependency of $(1-f_{dc})f_{dc}$ is calculated as follows,

$$\frac{d\left[(1-f_{dc})f_{dc}\right]}{dT}=(1-2f_{dc})\frac{df_{dc}}{dT} \tag{5.23}$$

For the region $f_{dc}<0.5$, which is the region near the band edge, equation (5.23) is negative and the term $(1-f_{dc})f_{dc}$ reduces when temperature increases. It is straightforward that the trap induced capacitance in equation (5.23) has a negative temperature coefficient, especially for the energy level above the Fermi level where the density of traps is exponentially distributed. In addition, the charge holding ability of trap centres also decreases due to frequent charge interaction, which indicates the decrement of trap induced capacitance as well.

$$C_{it}(E)=\frac{q^2}{kT}D_{it}(E)(1-f_{dc})f_{dc} \tag{5.24}$$

The theoretical analysis of temperature dependency of the trapped charge lifetime also supports the analysis before. Based on the occupancy probability function in equation (4.2) and the electron concentration in equation (4.17), since $E-E_C<0$ and $\varphi_p(0)<0$ for n-type substrate MOSCAP, the time constant in the following has a negative temperature coefficient.

$$\tau_{traps}=C_{it}G_n^{-1}=\frac{f_{dc}}{c_n n_{dc}} \tag{5.25}$$

At high temperature, the interaction between the trap centres and SiC lattice site enhances, and the smaller time constant, reduced barriers and occupancy probability bring more trap centres into the conduction band. More traps are involved, degrading the quality of the interface and damaging the reliability of the MOS system.

6. Experimental results and discussions

The charge transportation and mechanism of unreliability problems under high temperature require measurable evidence to verify. Starting from the simulation results from COMSOL, this chapter confirms the existence of traps, extracts the physical parameters and analyses the distribution and lifetime of the interfacial traps from experimental characterisations, and further uses them to explain the threshold voltage stability at high temperature.

6.1 COMSOL simulation of MOSCAP and interface traps

COMSOL Multiphysics is a powerful tool to solve partial differential equations (PDEs) with physical based interface by finite element computations. Since rarely models are found in circuit simulation software/environment, the SiC model employed is built by following the fabrication procedures in chapter 2.

The COMSOL model is in 1-D due to its circular structure, where the directions around the other axis are identical. The following establishes the 1-D COMSOL model and the cross sections of circular MOSCAP as well. The gate voltage is applied to the "thin insulator gate" under the "semiconductor (semi)" tab, representing the gate electrode. The amplitude and frequency of the applied signal are user-defined, with $\upsilon_{ac} = 1\text{mV}$ and $f = 50\text{Hz}$ are specified. The silicon dioxide thickness is 50 nm, where the semiconductor-oxide interface is then defined. In COMSOL, the "Continuity/Heterojunction" tab is applicable at the interface, and the "trap assisted recombination" is also selected. Additionally, the substrate is simulated by the "Analytic doping model" with all doping concentrations taken from [27]. Finally, the substrate terminated at depth of 350 nm is connected to metal contact.

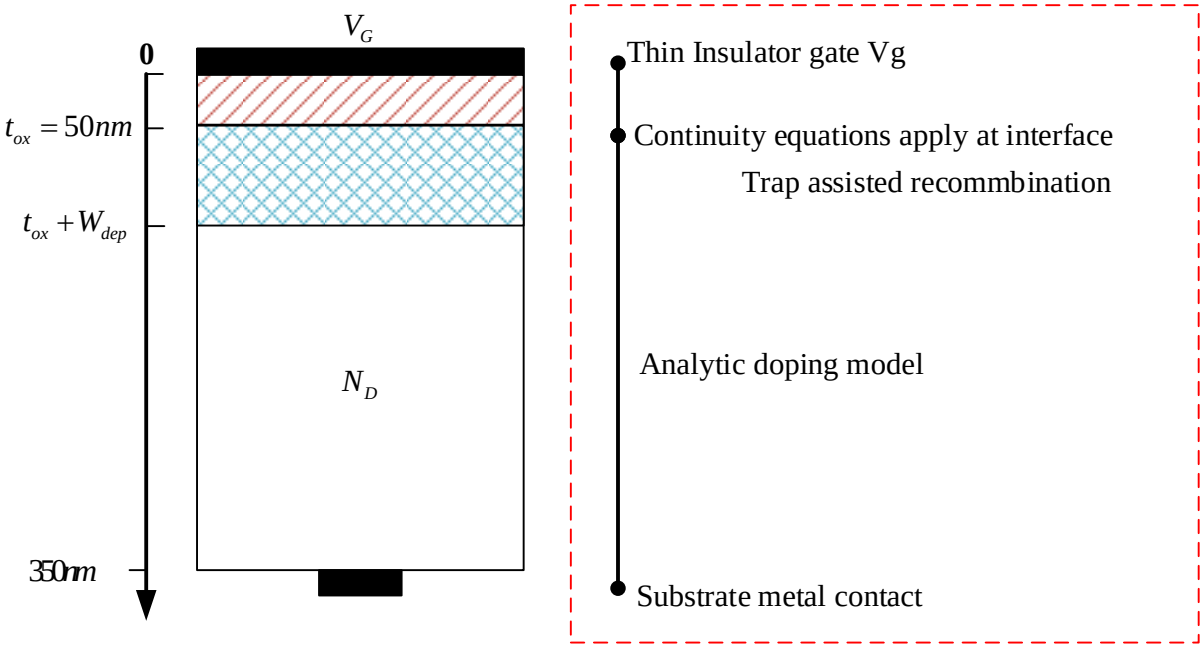

Fig. 6.1. Cross section of MOSCAP structure and COMSOL 1-D model.

The simulation results of the bias voltage sweeping at $f = 50Hz$ are performed to support the analysis of the physical parameter response to the applied voltage, as discussed in chapter 4. The stationary study "semiconductor equilibrium" is selected first and the "frequency domain perturbation" under the frequency domain study is then chosen to plot the C-V curves and physical parameters variation when sweeping.

The following illustrates the simulated C-V curve sweeping from $+1V$ to $-5V$, at the frequency of $f = 50Hz$. The simulated capacitance is derived from the derivative between the surface charge and applied small signal voltage,

$$C_m = \text{lindev(semi.Q0\_2)/Vac} \tag{6.1}$$

where the "lindev" function is to evaluate the variation of surface charge under ac signal, and the command "semi.Q0_2" represents the surface charge density in the semiconductor. In addition, the conductance can be obtained by evaluating the real part of the impedance,

$$G_m = \text{Re}(Y_m) = \text{Re}[\text{semi.iomega*lindev(semi.Q0\_2)/Vac}] \tag{6.2}$$

where the operator "semi.iomega" represents the quantity "$i\omega$" in acoustic analysis. Fig. 6.2 clearly shows the "bulge" on the C-V curve induced by interfacial traps with density of $2\times10^{11}cm^{-2}eV^{-1}$. The capacitance in accumulation (top right blue curve) is $1.86pF$, which verifies the calculation in equation (2.22). In addition, the conductance coloured green with a peak at $-3V$ suggests the surface condition where the interfacial traps affect most.

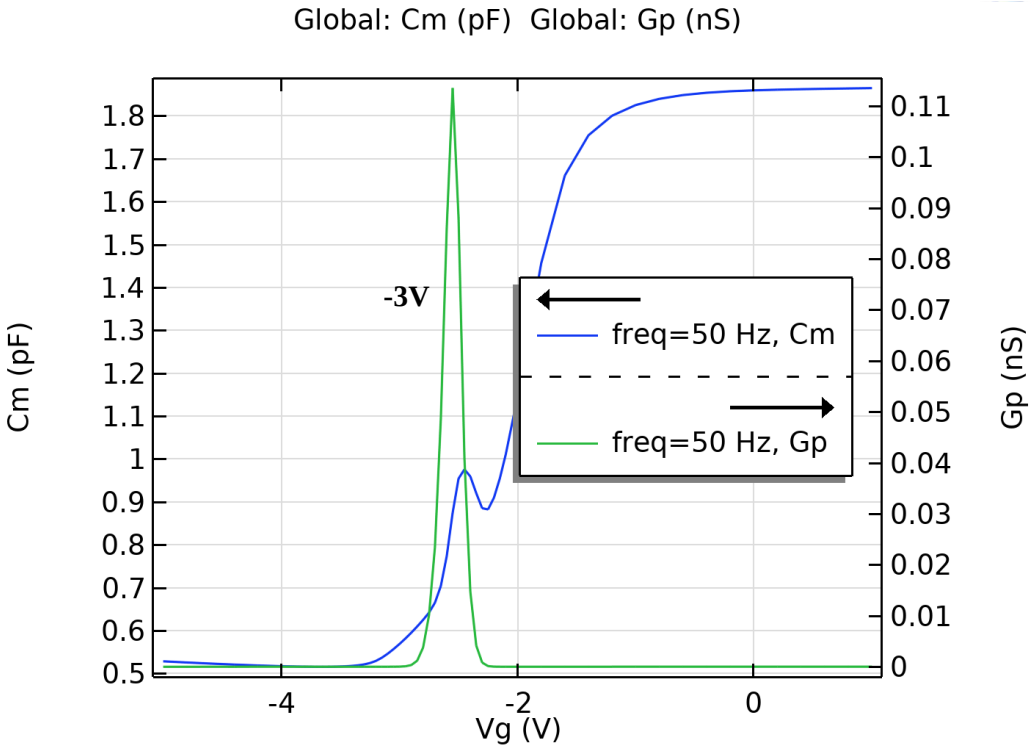

Fig. 6.2. COMSOL simulation results of 1-D SiC MOSCAP model, with n-type substrate whose doping concentration is $5\times10^{15}cm^{-3}$ and surface trap density $2\times10^{11}cm^{-2}eV^{-1}$.

The SiC MOSCAP with the p-type substrate is also simulated, as is shown in Fig. 6.3. The required voltage to bias the device into the accumulation region now is negative, and a "bulge" also appears at the peak of the conductance curve where the device suffers from interfacial traps worst. The "bulge" in the C-V curve for the p-type substrate is smaller than the n-type, partially because of the doping centration differences. More importantly, the conductance in the p-type substrate is less than the substrate doped by donor atoms.

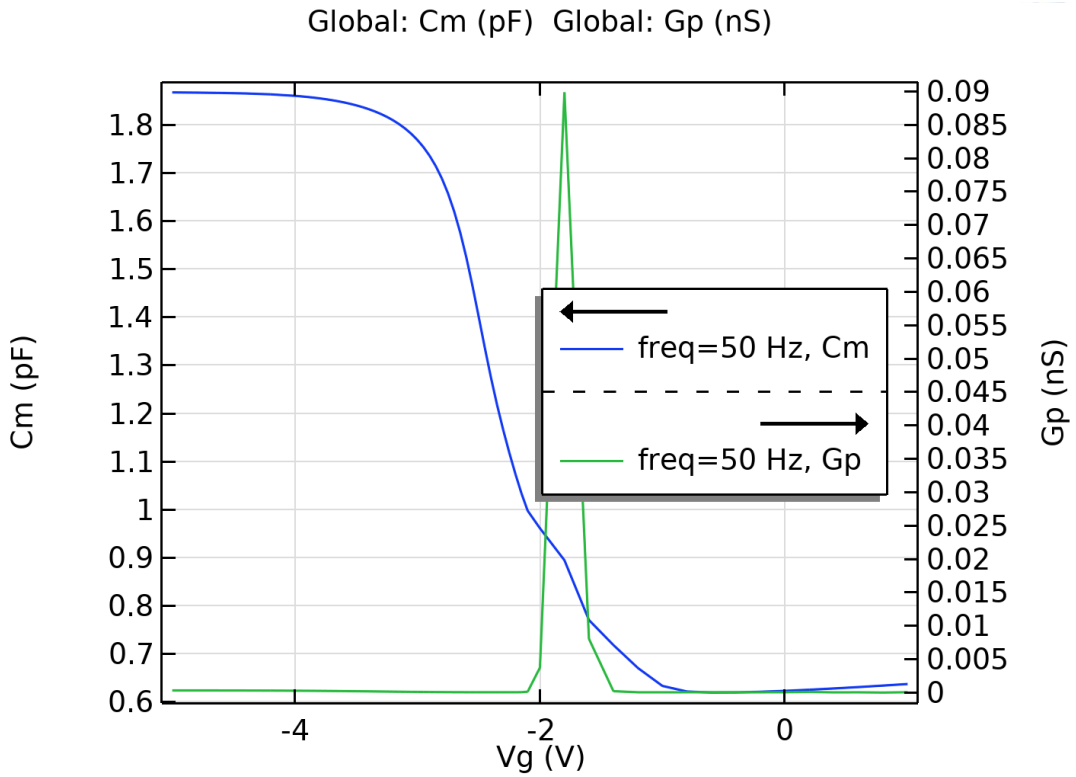

Fig. 6.3. COMSOL simulation results of 1-D SiC MOSCAP model, with p-type substrate whose doping concentration is $1\times10^{16}\,\mathrm{cm}^{-3}$ and surface trap density $2\times10^{11}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$.

To get insight into reliability problems, the band diagram and surface potential are simulated to verify the phenomenon after breaking the steady-state. The study "semiconductor equilibrium" and "frequency domain perturbation" tabs are selected, where the bias voltage and frequency are specified inside. The electrons and holes concentration, surface potential as a function of applied voltage and band diagram simulations are all obtained.

The band bending sweeping from $-5\mathrm{V}$ to $+5\mathrm{V}$ is simulated in Fig. 6.4, in which the Fermi level is set on the original point ($0\mathrm{eV}$ energy level). At room temperature, over 90% of the donor atoms are ionised in the n-type substrate MOSCAP and the Fermi potential simulated result supports the calculation in equation (2.10). For an n-type substrate when applying a negative bias voltage, the positive ionised atoms are required in the space charge region, which increases the surface potential and the band bends more. To compensate for the band bending under a large negative bias voltage, the space charge region expands accordingly, which is also in Fig.6.4.

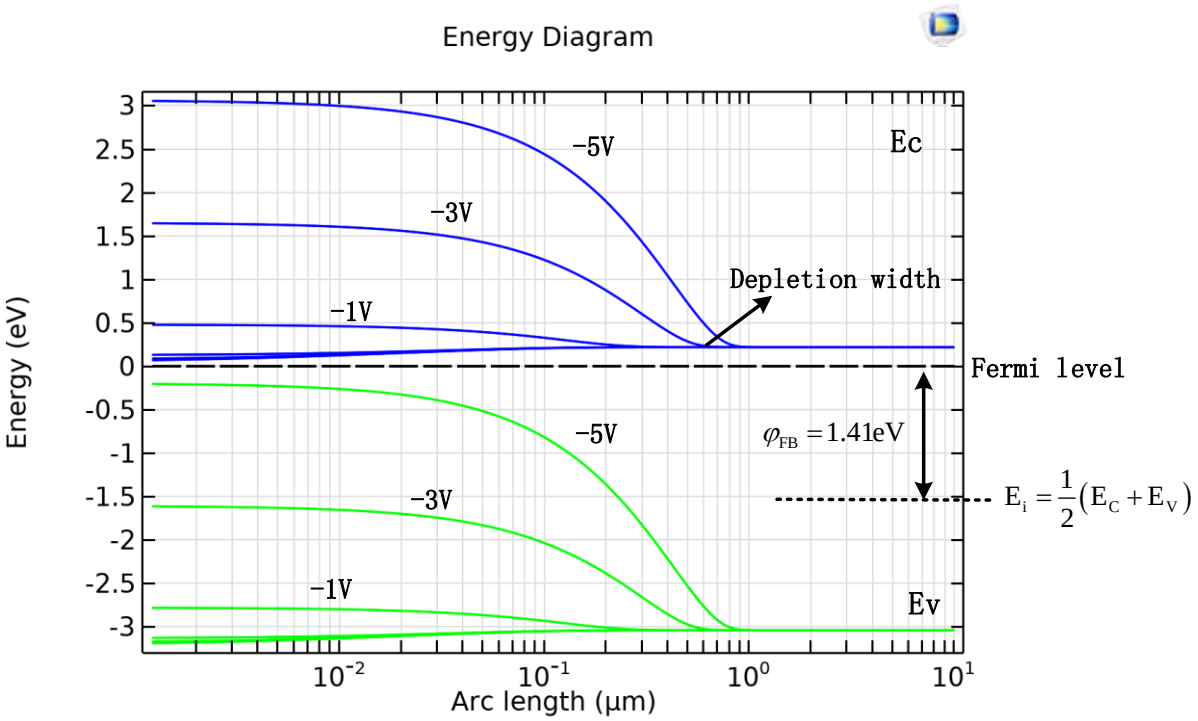

Fig. 6.4. COMSOL simulation results of 1-D SiC MOSCAP model, with n-type substrate whose doping concentration is $5\times10^{15}cm^{-3}$, sweeping from $-5V$ to $+5V$ at room temperature.

6.2 Experimental evidence of traps

The trap centres interact with the conduction band or valance band, releasing or capturing the charges from the SiC lattice, whose response time also lags behind compared with the majority charge carriers. Because of that, the C-V measurement varies if the frequency of the measurement signal changes and the traps are detectable when the sweeping direction or the frequency of the applied signal alters.

The hysteresis of the C-V measurement is evidence of traps and is used to examine the quality of the oxide-semiconductor interface. The forward sweeping is identical to reverse sweeping for an ideal MOSCAP. However, due to the long response time of the trapped charges, hysteresis occurs. Taken an n-type substrate SiC MOSCAP as an example, when sweeping from depletion to accumulation, the band bends from downwards to upwards. When pre-set to depletion, the trapped charges are ejected to the conduction band, and especially for HFCV measurement, the measurement gives the curve without traps. However, the reverse sweeping stabilises in the accumulation mode, where the trap centres are full of electrons. Since the pre-charged traps cannot respond to the high frequency signal, the C-V curve suffering from trapped charges gives an observable deflection when sweeping back, shown in Fig. 6.5 as follows.

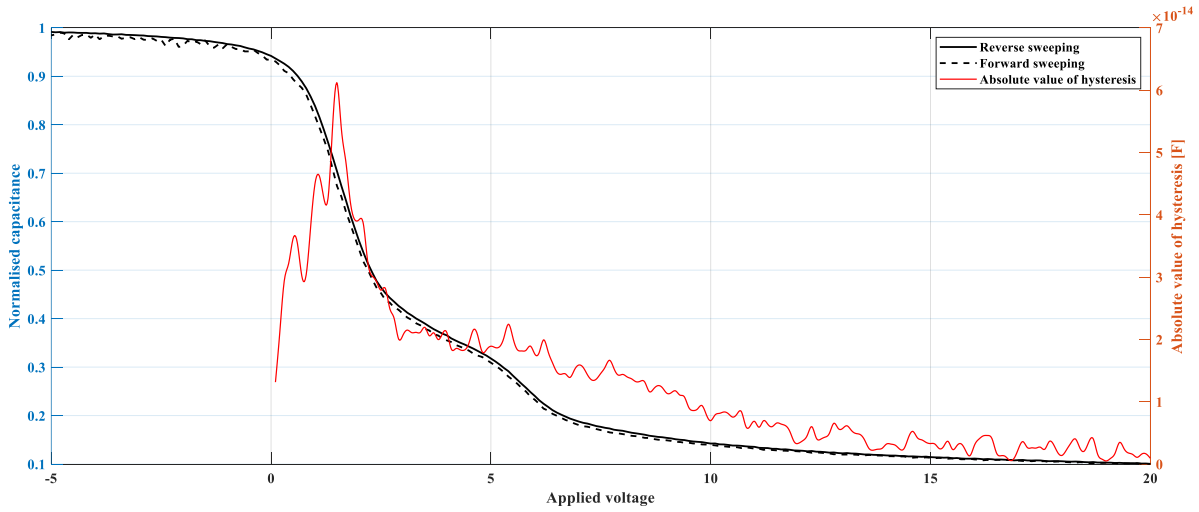

Fig. 6.5. Hysteresis in HFCV measurement at room temperature, using SiC MOSCAP with n-type substrate. The forward sweeping is from depletion to accumulation, whose curve is trap free.

The sweeping ranges from -20V to $+20\text{V}$, where the band bends sufficiently from depletion to accumulation, and the trapped charges within the band bending are detected by the hysteresis. The authors in [57] presented a trapped charges extraction method using hysteresis,

$$D_{it} = \frac{1}{qA}\int \left|C_{rev} - C_{for}\right| dV \tag{6.3}$$

The capacitance gap coloured red represents the absolute value of hysteresis, and the integration of it is expressed by the area underneath. From the Fig. 6.6, the integration from accumulation to depletion is $6.356\times10^{-13}\left[\text{CV}\right]$, leading to $D_{it} = 1.4049\times10^{11}\text{eV}^{-1}\text{cm}^{-2}$.

According to the fact that the trapped charges only follow moderate frequency signal, these trapped charges can be distinguished by sweeping the frequency of the signal, thus according to equation (3.26), the trap density is a function of both normalised capacitances and capacitance gap. The following illustrates the normalised capacitance as a function of applied voltage, for both QSCV and HFCV measurements at room temperature, using p-type substrate SiC MOSCAP. The trapped charges only give a response to slow signals, which contributes to a nonzero capacitance gap, and will be extracted in the next section. The higher signal frequency is applied, the fewer trapped charges can follow so that an infinitely high frequency leads to theoretical C-V curve.

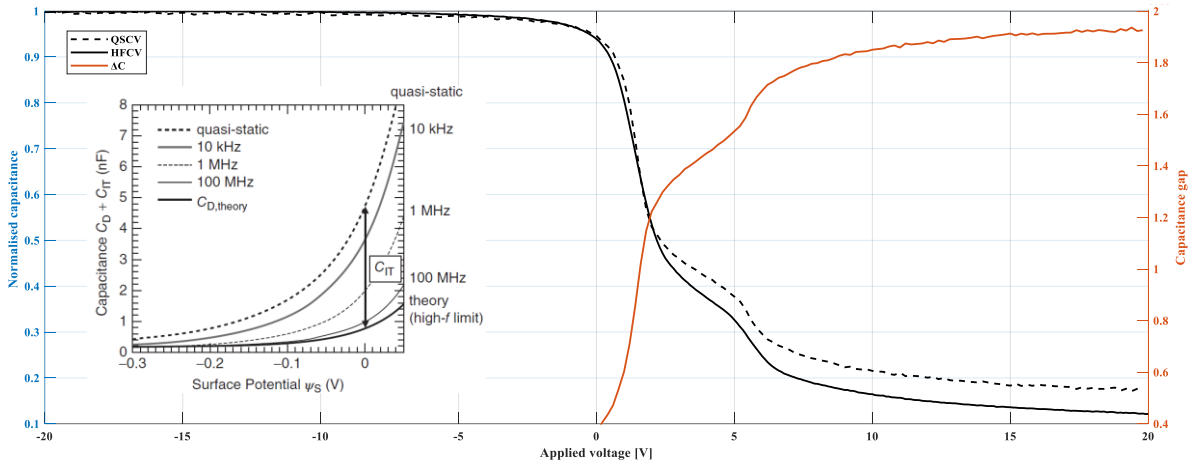

Fig. 6.6. Experimental evidence of interfacial traps comparing HFCV and QSCV measurement together at room temperature.

Using the HFCV measurement or QSCV measurement alone also verifies the existence of the trapped charges and their temperature behaviours. The occupancy of trap states is temperature dependent, thus the trap induced capacitance is temperature sensitive. The following shows the HFCV measurement of an n-type substrate from room temperature to $200^{\circ}C$. The high temperature reduces the occupancy probability and lower capacitance is observed due to large density of empty trap states, so that the interaction between interface to channel are enhanced.

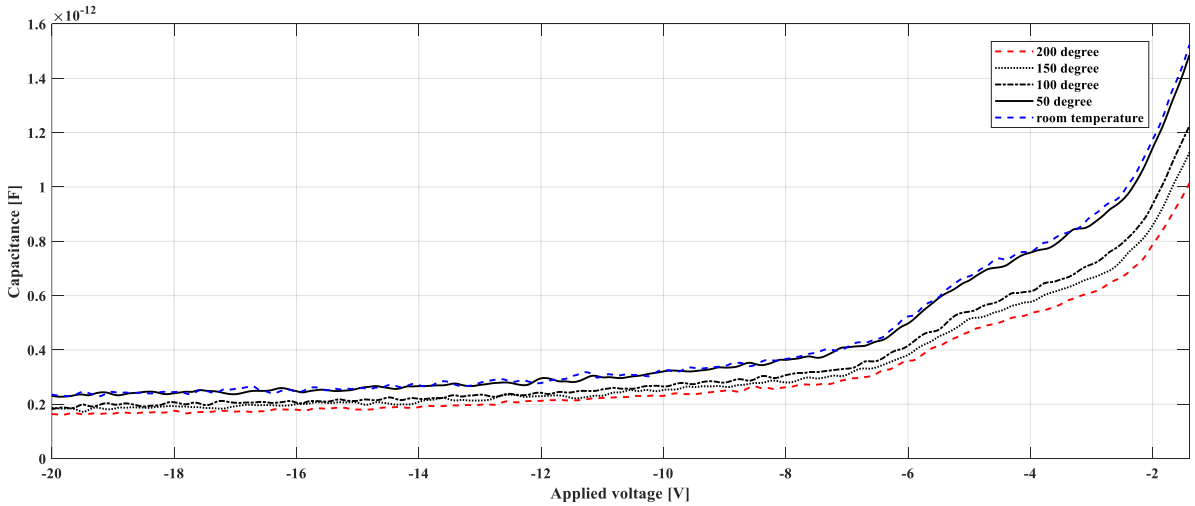

Fig. 6.7. Experimental evidence of interfacial traps using HFCV measurement high temperature.

6.3 Interface traps information extracted from electrical characterisation

Accurately extracting the distribution of traps promotes the analysis of the interface and temperature effect of them. The extraction methods introduced in chapter 3 are all applied to find the distribution of interfacial traps from experimental measurements.

The Terman method in section 3.4.1 already shows how to determine the trapped charges using HF measurement alone, by comparing the high frequency measurement with theoretical $\varphi_s - V_{gs}$ curves. Although the trapped charges cannot follow the high frequency signals, the surface potential ($\varphi_s - V_{gs}$) fluctuations induced by the traps is also observable. Equation (2.30) and (2.35) both show how the surface potential φ_s is flattened by trapped charges and the experimental C-V curve deflected by interfacial traps is shown as follows in Fig. 6. 8.

Since the capacitance C_{HF} is one-to-one corresponding to φ_s in theoretical curve and the measurement result gives correspondence to V_{gs}, equalising the capacitance C_{HF} in both curves maps the applied voltage V_{gs} to the surface potential φ_s. With a measured $\varphi_s - V_{gs}$, the equation (3.19) gives the distribution of interfacial traps $D_{it}(V_{gs})$. The trap distribution in bandgap $D_{it}(E)$ can be obtained by mapping the $D_{it}(V_{gs})$ via $\varphi_s - V_{gs}$ and equation (2.36).

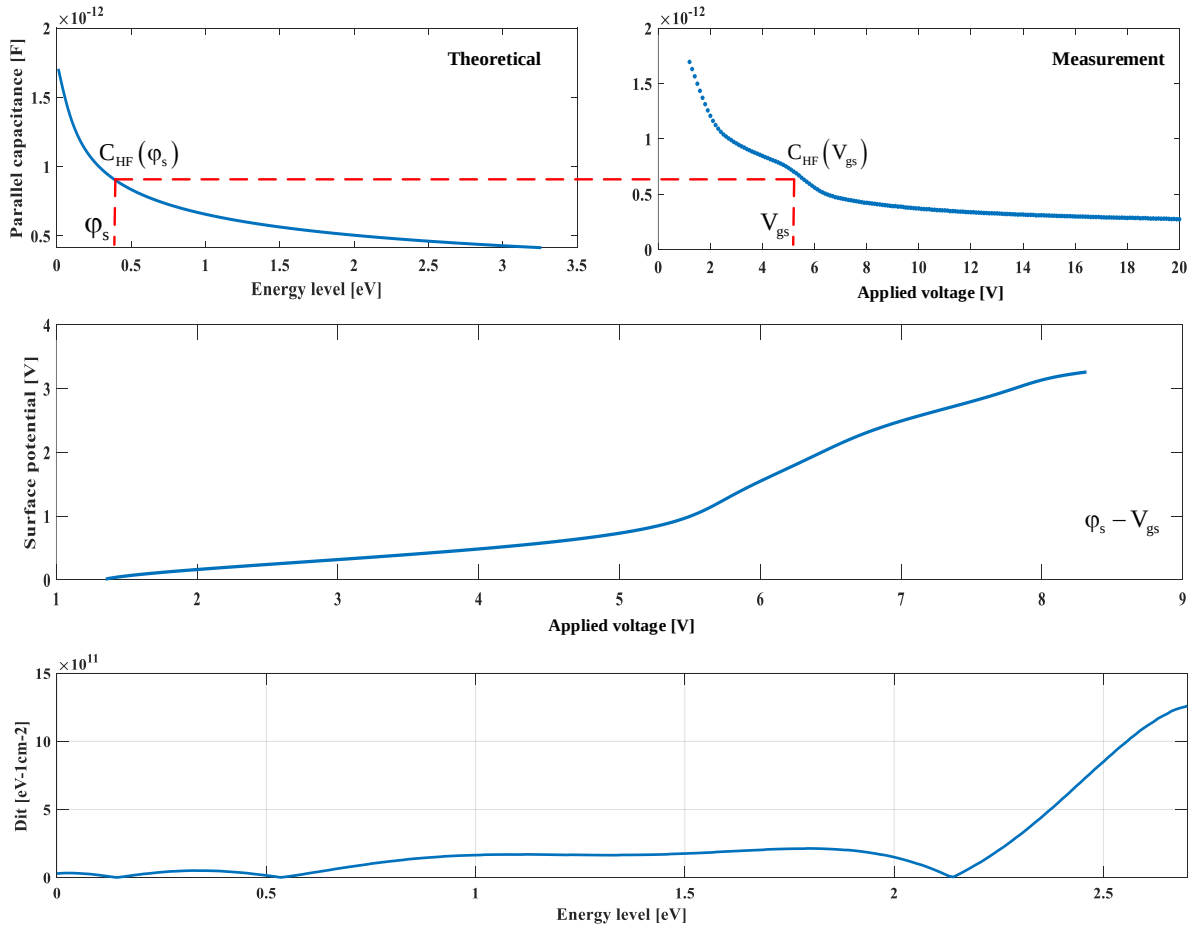

Fig. 6.8. Experimental evidence of interfacial traps using HFCV measurement. The measurement C-V curve of n-type substrate is clearly degraded by traps, so that the $\varphi_s - V_{gs}$ fluctuation appears even though the traps cannot follow the HF signal.

From Fig. 6.8, the density of traps increases dramatically near the conduction band edge for SiC MOSCAP with an n-type substrate. Similar interface trap distribution can be obtained by QSCV measurement alone in Fig. 6.9. Instead of differentiating, the $\varphi_s - V_{gs}$ relation is given by the integration of the low frequency measurements according to equation (3.21).

The integration constant C in equation (3.21) need to be carefully selected. In chapter 3 we already determined the integration constant C by calculating the area covered from accumulation to flat band voltage, where the theoretical flat band capacitance C_{fb} (with the unit of F/m^2) is defined as follows.

$$C_{fb} = \frac{\varepsilon_0 \varepsilon_{SiC} \varepsilon_{ox}}{L_d \varepsilon_{ox} + t_{ox} \varepsilon_{SiC}} \tag{6.4}$$

where L_d is the Debye length and t_{ox} represents oxide thickness. The flat band voltage is the closest sweeping voltage leading to flat band capacitance C_{fb} calculated by equation (6.4). However, there may be a large error ($\pm 1V$) if simply performing equation (6.4).

Another method to determine the integration constant C is to plot the measured depletion capacitance $1/C_s^2 - V_{gs}$ as a function of applied voltage. The measured $1/C_s^2$ is expected to be linear since $1/C_s$ in SiC devices is a square root function. Based on that, the extraction of the flat band voltage is avoided and C locates at the intersection point of the horizontal axis in $1/C_s^2 - V_{gs}$ curve, exactly no flat band voltage is involved.

After obtaining $\varphi_s - V_{gs}$ from integration, the distribution of traps is extracted in Fig. 6.9, following the procedures used in high frequency method. The effective extracted energy ranges from the valance band edge to the conduction band edge when sweeping the gate voltage from accumulation to deep depletion.

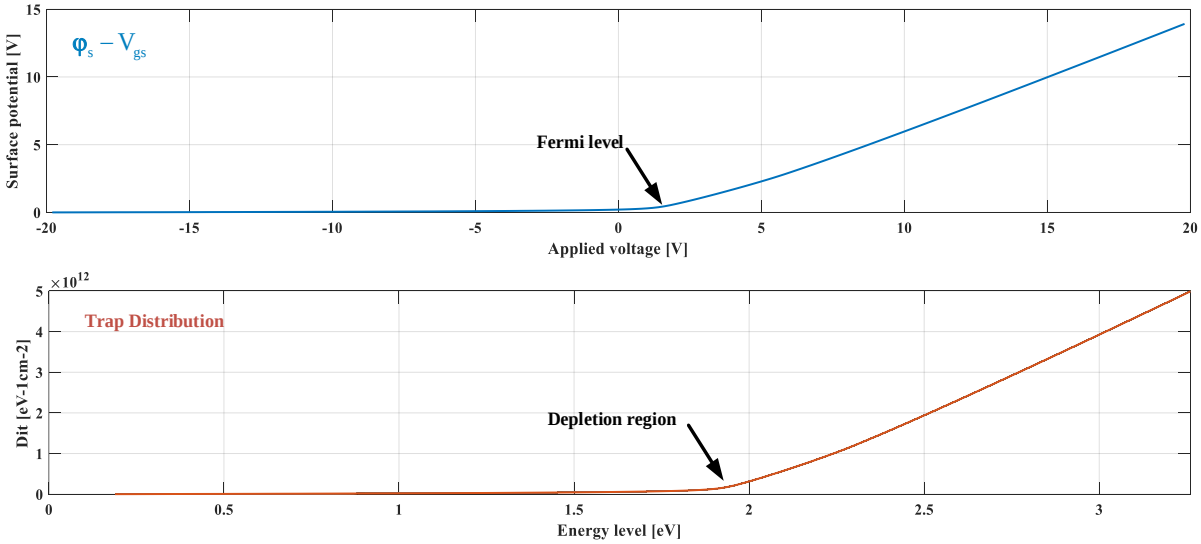

Fig. 6.9. Experimental evidence of interfacial traps using QSCV measurement. The $\varphi_s - V_{gs}$ curve is integrated and the trap distributed exponentially near band edge.

To simplify the procedures of finding flat band voltage, as an alternative, the high-low method and $C_d - \varphi_s$ has been both introduced in section 3.4.3 and 3.4.4. These methods focusing on the capacitance gap induced by interfacial traps are straightforward and ease of extraction, only with sufficiently high frequency to exclude all effects of traps. The following illustrates the capacitance gap and trap distribution extracted by the $C_d - \varphi_s$ method.

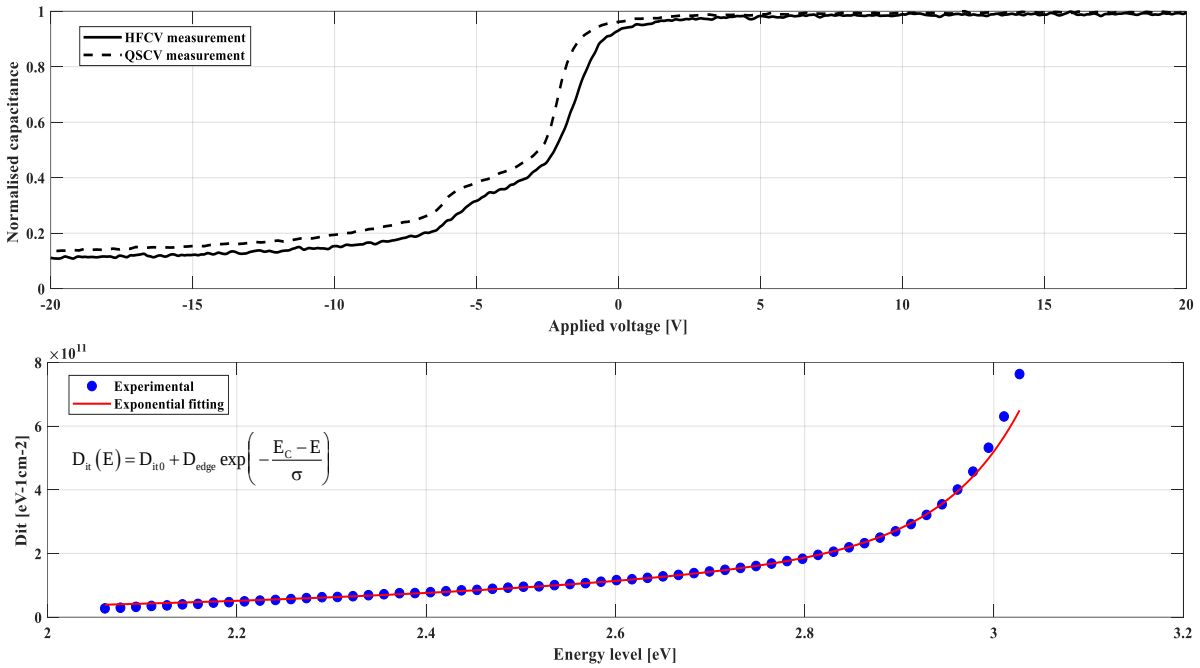

Fig. 6.10. Experimental extraction interfacial traps comparing HFCV and QSCV. The capacitance gap is due to the interfacial traps, which is also proportional to the density of traps at that energy level.

Fig. 6.10 verifies the exponentially distributed interfacial traps in a MOSCAP with an n-type substrate. Taken the conduction band edge as an example, from $[2.1\text{eV}, 3.05\text{eV}]$, the extracted results under double exponential fitting give the band tail energy and band edge trap density,

$$\frac{1}{\sigma} = 1.954\text{eV}^{-1} \tag{6.5}$$

$$D_{\text{edge}} \cdot \exp\left(-\frac{3.26}{\sigma}\right) = 6.984\times10^{8}\text{eV}^{-1}\text{cm}^{-2} \tag{6.6}$$

where σ represents the band tail energy which is equal to 0.512eV, and the trap density near band edge is $D_{\text{edge}} = 4.079\times10^{11}\text{eV}^{-1}\text{cm}^{-2}$. Both of them are temperature sensitive parameters. The band tail energy is the "spread" of the exponential curves. As its name suggested, for a large σ, the exponential curve is flattened and the "tail" of the curve near midband is expanded. For the sample in this project, the band tail energy σ is around 0.5eV, which is ten time of the sample in [58]. That is because the interface in our sample is processed by NO, enhancing the quality of interface and further reducing the density of traps in the bandgap.

6.4 Measurement and analysis of trap response time

After analysing the static profile of interfacial traps, the dynamic transportation of trapped charges is characterised by the measurement of trapped charges response time (lifetime). These high energy trapped charges emitted from the trap centres are thermalized till equilibrium is reached in the substrate. The response time measurement can not only extract the trap distributions, but also link them with the equivalent circuit in chapter 4, to verify the temperature effect discussed before.

The equation (4.38) states that the conductance of single energy level traps has a peak $C_{it}/2$ at frequency $\omega=\tau_{it}^{-1}=\left(C_{it}R_{it}\right)^{-1}$. As a result, the trapped charge lifetime can be reached by varying the measurement frequency until finding the maximum out. The KEYSIGHT 4294A impedance analyser can measure the conductance automatically, and Fig. 6.11 shows the measurement under $1MHz$ frequency at room temperature.

It is also worthwhile to note that the output from the impedance analyser always includes the oxide capacitance C_{ox} and series resistance so the parallel conductance must be split from measured conductance using equation (4.40). The series resistance containing the extra resistance from the measurement setup and device should be eliminated [59]. In the accumulation region, the conductance is $Y_{m,acc}=G_{m,acc}+j\omega C_{m,acc}$, whereas the impedance is $Z_{m,acc}=1/Y_{m,acc}=R_s+1/j\omega C_{ox}$. Combining them to solve the series resistance yields,

$$R_s=\frac{G_{m,acc}}{G_{m,acc}^2+\omega^2C_{m,acc}^2} \tag{6.7}$$

Fig.6.11 illustrates the parallel capacitance and conductance measurement as a function of applied voltage of n-type substrate SiC MOSCAP under $1MHz$ oscillation frequency at room temperature. The parallel conductance plot is divided by the measurement frequency to reach the G_p/ω plot as a function of applied voltage.

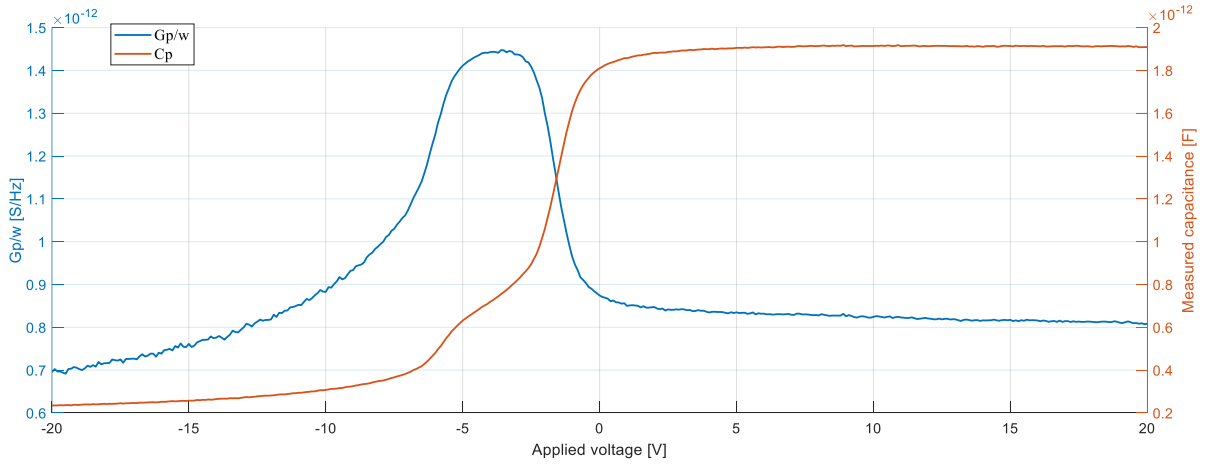

Fig. 6.11. Capacitance and conductance of n-type SiC MOSCAP at room temperature as a function of applied voltage, and the oxide capacitance is removed.

Repeating the procedure but only changing the oscillation frequencies gives a set of G_p/ω at certain bias voltages and oscillation frequencies. In turn, a plot of G_p/ω as a function of oscillation frequency derived from $G_p/\omega - V_{gs}$ curve from measurement can be obtained. From that, the trap profile is reachable when the $G_p/\omega - \omega$ shows a clear peak. The author in [61] expressed the paralleled capacitance and conductance for continuous distributed trap, by integrating the single level trap distribution from equation (4.40).

$$C_p = C_s + qD_{it}\frac{\arctan(\omega\tau_{it})}{\omega\tau_{it}} \tag{6.8}$$

$$\frac{G_p}{\omega} = \frac{qD_{it}}{2}\frac{\ln(1+\omega^2\tau_{it}^2)}{\omega\tau_{it}} \tag{6.9}$$

where the time constant τ_{it} has already been defined in equation (4.33). The curve should have a global maximum since the rate of change of $\omega\tau_{it}$ is slower than $\ln(1+\omega^2\tau_{it}^2)$ at small frequency, and larger than $\ln(1+\omega^2\tau_{it}^2)$ in high frequency measurement. Fig. 6.12 plots the measured paralleled capacitance and conductance with respect to the oscillation frequency at room temperature, under various bias voltages.

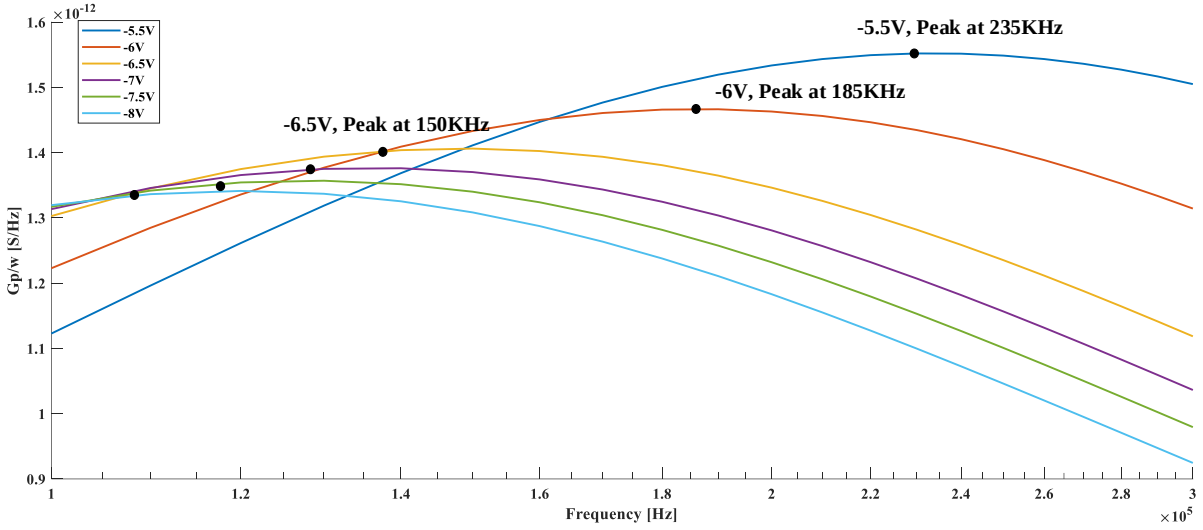

Fig. 6.12. G_p/ω measurement of n-type SiC MOSCAP at room temperature as a function of oscillation frequency, with all peak points and corresponding frequencies indicated.

Taking the bias voltage $-5.5V$ as an example, the peak value $1.552\times10^{-12}S/Hz$ shows up at $f = 235KHz$. The effective trap density extracted when the bias voltage is $-5.5V$, is calculated as follows,

$$D_{it}\big|_{-5.5V} = 10^{-4}\cdot\left[\left(\frac{G_p}{\omega}\right)_{max}/qA\right] = 8.521\times10^{11}eV^{-1}cm^{-2} \tag{6.10}$$

where A is the cross section of the circular MOSCAP, calculated by $A=\pi r^2$ with radius $r=30\mu m$, and the factor "10^{-4}" in front is to match the unit "cm^{-2}". The trap density extracted value matches the extraction methods discussed before. In addition, the frequency that the peak locates reveals the time constant of the trapped charges. In that case, the maximum lifetime of the trapped charges is $4.347\mu s$ at room temperature, when the bias voltage is $-5.5V$. The table in the following establishes the trap information extracted at room temperature, measured by n-type substrate with $r=30\mu m$ and a doping concentration of $5\times10^{15}cm^{-3}$.

Table. 6.1. Experimental trap information extracted by n-type substrate SiC MOSCAP, at room temperature.

Biased voltage [V]	$\max\left(G_p/\omega\right)$ [S/Hz]	D_{it} [$eV^{-1}cm^{-2}$]	τ_{it} [μs]
-5.5	1.552×10^{-12}	8.521×10^{11}	4.347
-6	1.466×10^{-12}	8.101×10^{11}	5.500
-6.5	1.406×10^{-12}	7.770×10^{11}	6.667
-7	1.476×10^{-12}	7.604×10^{11}	7.143
-7.5	1.357×10^{-12}	7.499×10^{11}	7.692
-8	1.314×10^{-12}	7.261×10^{11}	8.333

For an n-type substrate, when a negative signal is applied, the majority carriers are repelled away so that the interface is more depleted. The Fermi level bends more and the electrical field inside also releases the trapped charges. In addition, the trapped charge lifetime rises with a reduction of the bias voltage. That is because, in equation (4.33), τ_{it} is inversely proportional to the occupancy probability, and the occupancy probability is reduced when the interface becomes more depleted. The trap density and lifetime as a function of applied voltage measured by the n-type substrate sample is plotted in Fig. 6.13.

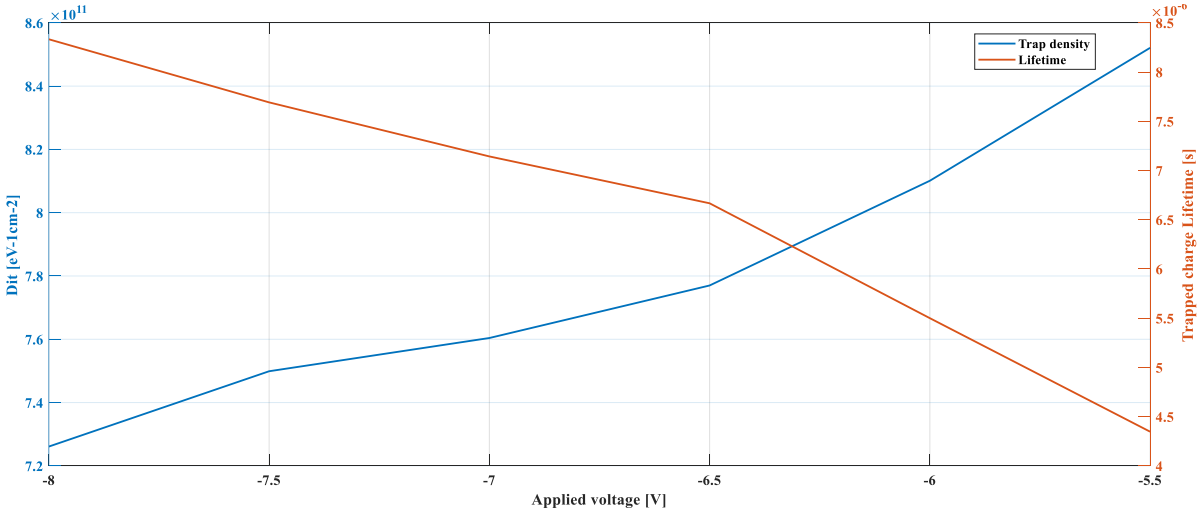

Fig. 6.13. Measured trap density and lifetime as a function of applied voltage at room temperature.

6.5 Temperature analysis of traps

The equilibrium state is broken due to the temperature variation induced Fermi level shift. As a consequence, the variation of occupancy probability at the Oxide-SiC interface results in the charge interaction between trap centres and the SiC lattice. The trapped charge density, distribution and response time are all sensitive to temperature accordingly.

Literature has reported the temperature effects on trap distribution, since the thermal energy term "kT", energy tail "σ" and the band edge trap density "$D_{it,edge}$" are all temperature dependent parameters in equation (3.13). The following establishes the temperature variation by electrical characterisation introduced before. The following presents the trap distribution extracted using the $C_d - \varphi_s$ method at $50^{\circ}C$, $100^{\circ}C$, $150^{\circ}C$ and $200^{\circ}C$ respectively, and compares them with the trap profile at room temperature.

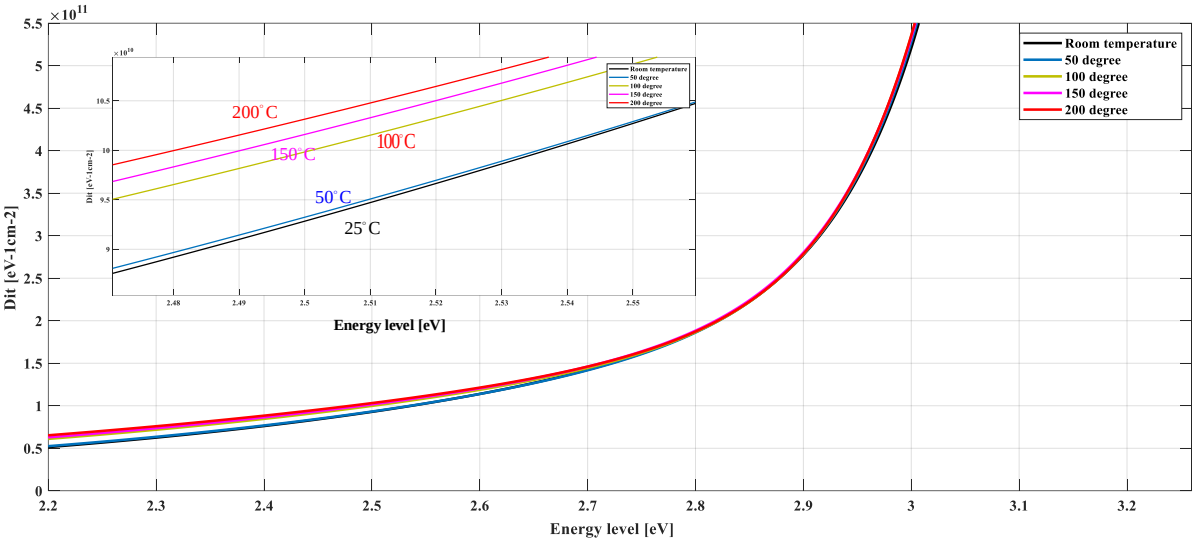

Fig. 6.14. Measured trap distribution in SiC band diagram under $50^{\circ}C$, $100^{\circ}C$, $150^{\circ}C$ and $200^{\circ}C$. The zoom-in plot clearly shows the temperature effects on the trap density.

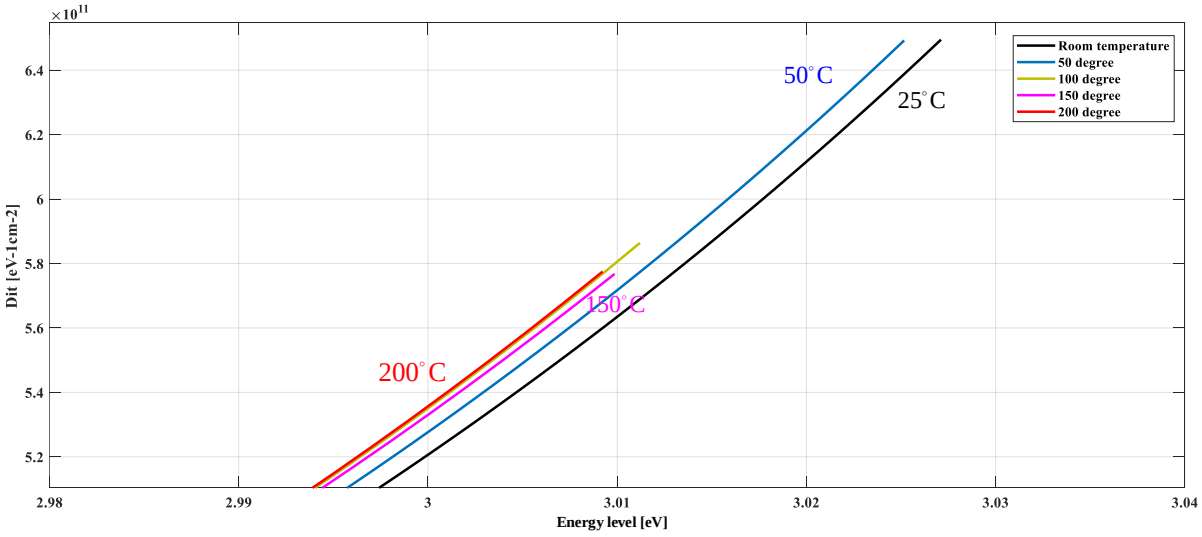

Fig. 6.15. Zoom in version of trap distribution to show the bandgap narrowing.

The trapped charges with high temperature gain sufficient energy to de-trap so that the density of trapped charges drops. In addition, the narrowing of the upper limit of the extractable ranges also suggests the shrinkage of the bandgap at high temperature. The high temperature bandgap narrowing can be modelled as follows [62],

$$\Delta E_g = C_{n,p}^{BGN}\left(F+\sqrt{F^2+0.5}\right) \tag{6.11}$$

where $F = \ln\left\lfloor \left(N_A + N_D\right)/N_{n,p}^{BGN} \right\rfloor$, $C_n^{BGN} = 0.02\text{eV}$ and $N_n^{BGN} = 10^{17}\,\text{cm}^{-3}$ for n-type 4H-SiC, and the bandgap narrowing $C_p^{BGN} = 9\times10^{-3}\text{eV}$ and $N_p^{BGN} = 10^{17}\,\text{cm}^{-3}$ for p-type 4H-SiC.

The exponential fitting reveals the temperature effects on the physical parameters, which are shown in table. 6.2. The bandgap narrowing ΔE_g is referred to room temperature.

Table. 6.2. Extraction of trap information for temperature effect analysis.

Temperature [°C]	$D_{it,edge}[\text{eV}^{-1}\text{cm}^{-2}]$	σ[eV]	ΔE_g[eV]
25	4.079×10^{11}	0.512	0
50	3.920×10^{11}	0.526	0.002
100	3.403×10^{11}	0.617	0.016
150	2.641×10^{11}	0.634	0.015
200	2.208×10^{11}	0.664	0.017

When temperature increases, the defects on the SiC-oxide interface are less occupied by the majority charge carriers after receiving sufficient energy. As observed in Fig. 6.15, although the trapped charge density increases inside the bandgap, the traps $D_{it,edge}$ exactly at the conduction band edge reduced at high temperature, from 4.079×10^{11} to 2.208×10^{11} when temperature increases to 200°C. The increment of temperature causes bandgap narrowing in 4H-SiC device, so that the trap states inside the bandgap are compressed and result in a higher density. The bandgap narrowing effect in SiC devices dominates more than silicon.

Physically, for a SiC crystal formed by silicon and carbon atoms, the crystal volume expands at high temperature and the distance of the adjacent atoms are broadened. The expansion of the crystal atoms leads to a reduction of the probability wave function. That is because the integration of the normalised periodic wave function is 1. In SiC, the atomic level does not simply correspond to one specific energy state due to the hybrid of valance band. As a result, the extension of atom distance at high temperature broadens the energy levels in between, thus the bandgap has a negative temperature coefficient. From another point of view, the bandgap represents the minimum required energy barrier to excite a free electron from the SiC lattice, which is reduced at high temperature, so that it suggests the narrowing of the bandgap at high temperature.

The charge transportation between the trap centres and SiC lattice is also temperature sensitive. The parallel conductance measurement G_p/ω tells the trap density and response time as a function of oscillation frequency, and the high temperature effects are added to verify the mechanism analysed in chapter 5.

Fig. 6.16 illustrates the G_p/ω measurement at $50^{\circ}C$ as an example to determine the trap behaviour at high temperature. The peak values at high temperature shift towards higher frequency, indicating a reduction of the lifetime of the trapped charges. With the known peak values from measurements, the trap density at that temperature and biased voltage is extractable.

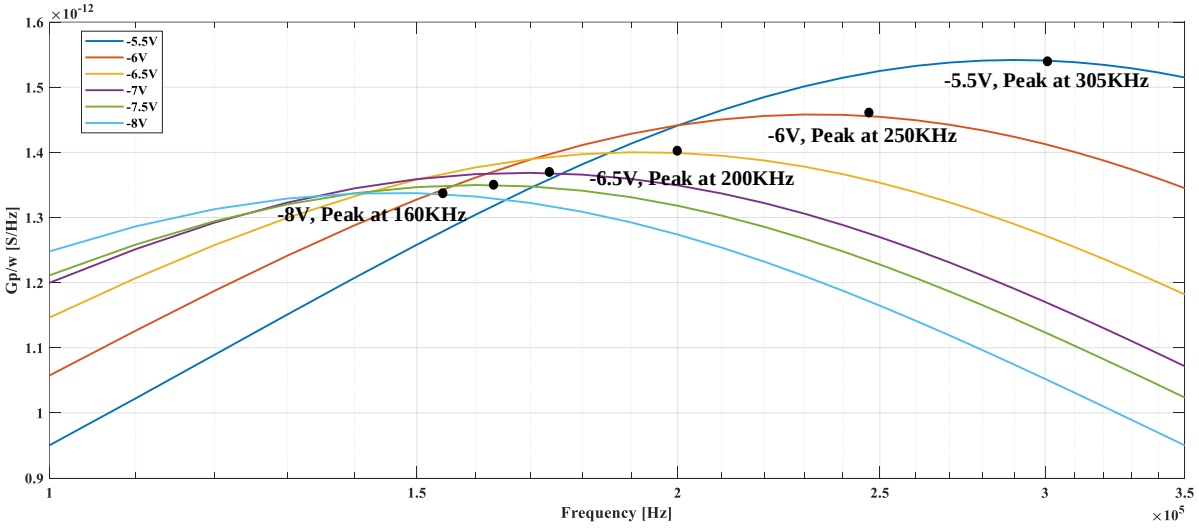

Fig. 6.16. G_p/ω measurement of n-type SiC MOSCAP at $50^{\circ}C$ as a function of oscillation frequency, with all peak points and corresponding frequencies indicated.

In addition, the trap information at $50^{\circ}C$ is listed in table. 6.3 to compare with the interface condition at room temperature. It includes the trap density and lifetime when biased in depletion region with various voltages. If the device approaches the depletion region, the energy level is pushed away from the band edge with an exponential decrement, which supports the analysis in chapter 4.

Table. 6.3. Experimental trap information extracted by n-type substrate SiC MOSCAP, at $50^{\circ}C$.

Biased voltage [V]	$\max\left(G_p/\omega\right)$ [S/Hz]	D_{it} [$eV^{-1}cm^{-2}$]	τ_{it} [μs]
-5.5	1.542×10^{-12}	8.466×10^{11}	3.279
-6	1.458×10^{-12}	8.057×10^{11}	4.000
-6.5	1.400×10^{-12}	7.737×10^{11}	5.000
-7	1.369×10^{-12}	7.565×10^{11}	5.556
-7.5	1.350×10^{-12}	7.460×10^{11}	5.882
-8	1.337×10^{-12}	7.388×10^{11}	6.250

The trap density D_{it} slightly reduces at $50^{\circ}C$ comparing with the profile at room temperature. The high temperature expands the SiC crystal so that the defects on the SiC-oxide interface are also widened. The D_{it}, defined as the number of defects at a certain energy level in unit volume, descends at high temperature when the SiC crystal expands. However, the measurement results tell that under -8V biased voltage, the trap density is 7.388×10^{11} at $50^{\circ}C$ which is higher than the trap density 7.261×10^{11} at room temperature. That measurement error may be caused by the noise generated by the heating setup, since the cooling and heating systems operate simultaneously to generate moderate heat.

The lifetime of the trapped charges also decreases at high temperature. The high temperature shifts the Fermi level towards the midband, so that more empty trap centres appear and the charge interaction between the traps and SiC lattice is enhanced. When increasing temperature, the trapped charges receive energy from phonon, which is enhanced by high temperature. As a result, more trapped charges are emitted and overcome a lower barrier from the interface to where they are thermalized.

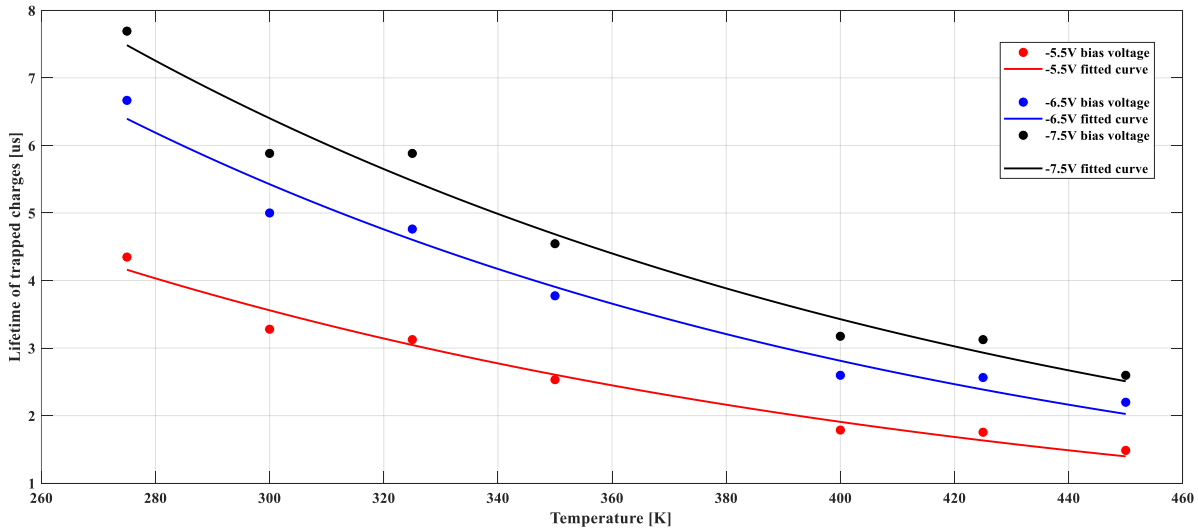

Fig. 6.17. Measurement and fitting results of the lifetime of the trapped charge, from room temperature to 473K, selected bias voltage from $-5.5V$ to $-7.5V$.

Fig. 6.17 illustrates the measurement results of the lifetime of the trapped charges in n-type substrate MOSCAP and the results of the exponential fitting. All measurements are in Appendix 4. A negative voltage increases the electrical field at the interface, so that the energy obtained from external source is higher. In that case, the trapped charges require more time to be stabilised. In addition, the lifetime of the trapped charges is reduced at high temperature. At the SiC-oxide interface where all dopant atoms are ionised, the electrical concentration cannot vary too much. In equation (5.25), the variation of the lifetime at high temperature is proportional to the occupancy probability variation. Exponential fitting is selected since,

$$f \approx a\cdot \exp\left[\, b\cdot \left(E-E_C\right)\right] \tag{6.12}$$

where $a=\left(N_D/g_D N_C\right)\cdot \exp\left(E_C/kT\right)$ and $b=-1/kT$.

6.6 Temperature reliability problems on threshold voltage

The threshold voltages in SiC MOSFETs are extracted under high temperature to explain the reliability problems induced by trapped charges. In contrast to the circular MOSCAP device, the MOSFET used for $I_d - V_{gs}$ transfer characteristics measurement is rectangular, and the cross section area of them is normalised to reduce the extraction error.

To begin with, the NMOS devices are biased at $V_{ds} = 0.2V$ and $V_{ds} = -2V$ for PMOS devices. The sweeping voltage starts from $-14V$ to $+14V$, where the drain current, gate leakage current and substrate current are all recorded. The high temperature $I_d - V_{gs}$ transfer characteristics such as $100^{\circ}C$ and $200^{\circ}C$ are measured, are shown as follows.

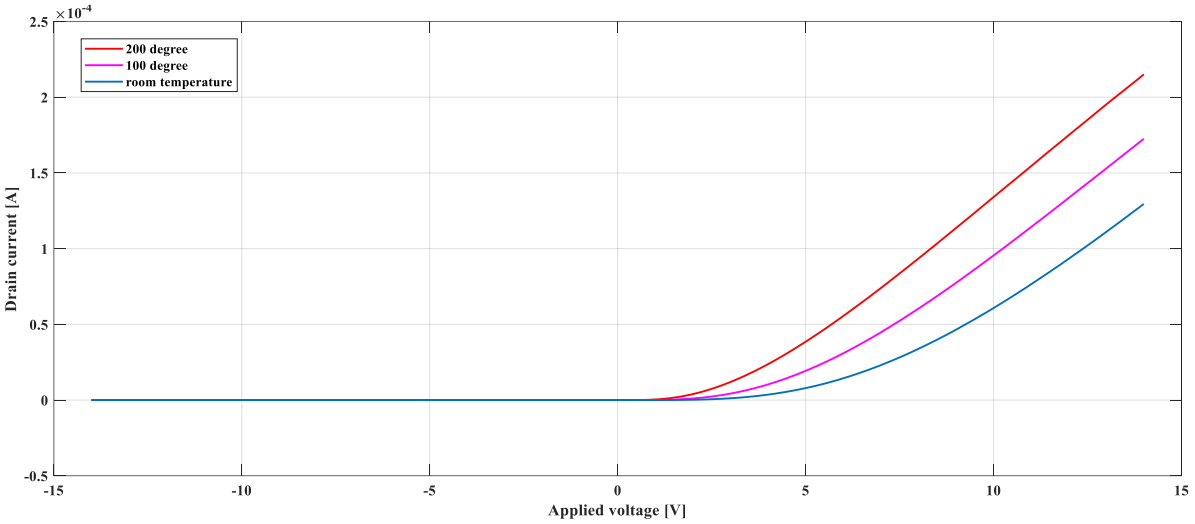

Fig. 6.18. $I_d - V_{gs}$ transfer characteristics sweeping for NMOS device, with various temperature ranges measured.

The second order derivative method (SD) is utilised for the threshold voltage extraction. One significant advantage of the SD method is to avoid the effect of series resistance [37], whereas the linear extrapolation method finding the maximum slope might overestimate the threshold voltage, due to the drain source series resistance and mobility degradation.

The second order derivative of the transfer characteristics comes from the slope of the transconductance, since $g_m = d(I_d)/d(V_{gs})$. The linear region of the drain current equation for the MOSFET is,

$$I_D = \mu_n C_{ox}(W/L)\left[(V_{gs} - V_{th,n})V_{ds} - V_{ds}^2/2\right] \tag{6.13}$$

where μ_n represents the n-channel mobility. For simplicity, during the $I_d - V_{gs}$ sweeping if $V_{gs} < V_{th,n}$, the drain current I_D is approached zero. When $V_{gs} > V_{th,n}$, the equation (6.13) applies and the first order derivative $g_m = d(I_d)/d(V_{gs})$ becomes a positive constant. Ideally, the first order derivative of $I_d - V_{gs}$ transfer curve is a step function, with an infinite slope at exactly the threshold voltage point. In reality, the infinite cannot be reached and the threshold voltage point is represented by the global maximum point in the second derivative curve.

The following figure illustrates the NMOS transfer characteristic and its second order derivative at room temperature. The global maximum point occurs at exactly $V_{gs} = 5.6V$, suggesting that the threshold voltage point which is $5.6V$ at room temperature. The threshold voltages of the sample MOSFET at high temperature are extracted, which are $3.64V$ at $100^{\circ}C$ and $1.96V$ at $200^{\circ}C$.

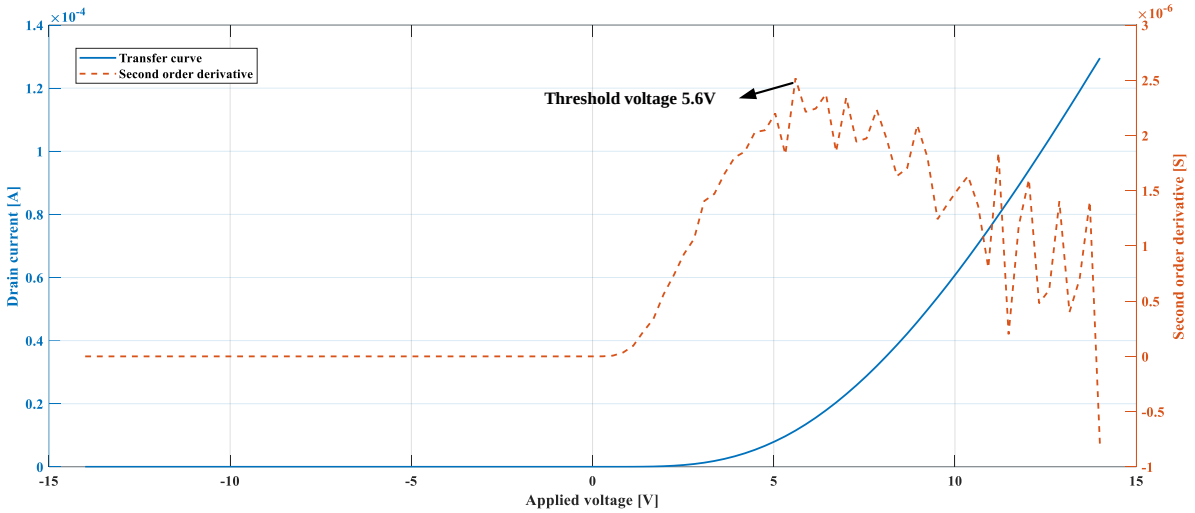

Fig. 6.19. $I_d - V_{gs}$ transfer characteristics for NMOS device, and second order derivative method to determine the threshold voltage.

The following discusses how the temperature influences the threshold voltage of a SiC device. The SiC itself is a temperature sensitive material, the trapped charges fluctuate the electrical field inside the SiC substrate, shifting the threshold voltage of the device, and the ionisation of the dopant atoms also increases the concentration of the majority charge carriers. Fig. 6.20 plots the threshold voltage variation under high temperature, with all non-idealities highlighted. The trap information is from table. 6.2, extracted from the exponential distribution.

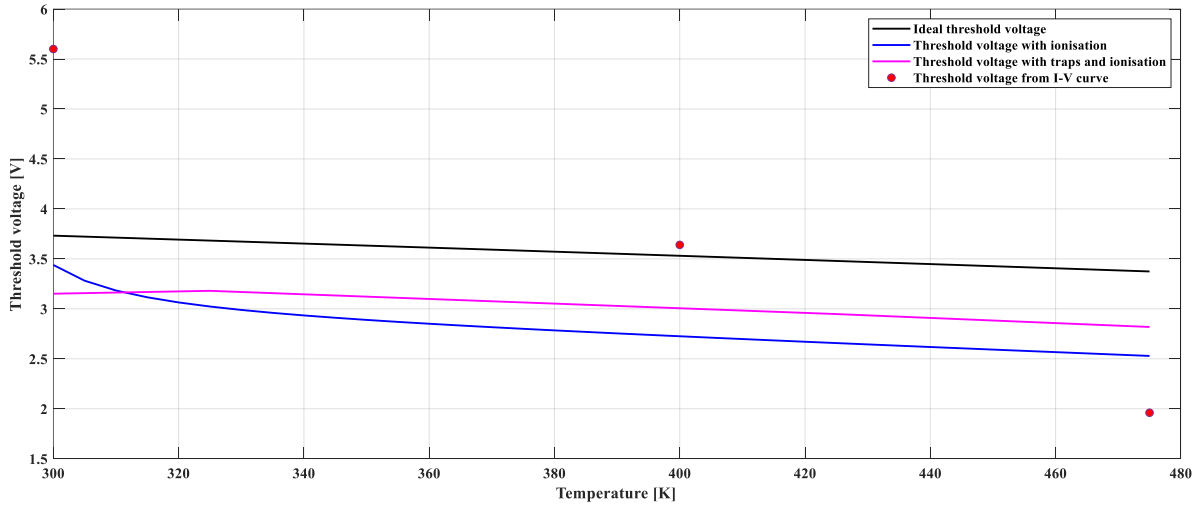

Fig. 6.20. The temperature reliability of intrinsic threshold voltage and the trap involved threshold voltage plot. Example is the p-type substrate (n-channel).

For the device with an n-type channel (p-type substrate), it is the donor trap located in the lower half of the energy band. Since the occupancy probability and trap distribution are both temperature dependent, the threshold voltage variation is also temperature sensitive. Due to the expansion of the SiC crystal at high temperature, although the trap density is higher, the traps at the band edge and the trapped charges are fewer. Equivalently saying, the charge transportation between the interface and channel is enhanced. The variation of the threshold voltage considering incomplete ionisation from $273K$ to $473K$ is only $0.607V$. However, the threshold voltage with traps shifts from $3.151V$ to $2.818V$, using the trap density in Table. A5.1 in Appendix 5. When adding trap properties, the threshold voltage shifts $-0.333V$ from room temperature to $200^{\circ}C$. The mismatch between the measurement and theoretical prediction is partially due to the defects inside the oxide layer, such as the oxide charges and leakage current.

The I-V characteristics used for extracting threshold voltage of the n-type substrate (p-channel) is shown in Fig. 6.21. The second order derivative method is applied again, with threshold voltages $-6.16V$ at $200^{\circ}C$, $-6.72V$ at $100^{\circ}C$ and $-7V$ at room temperature.

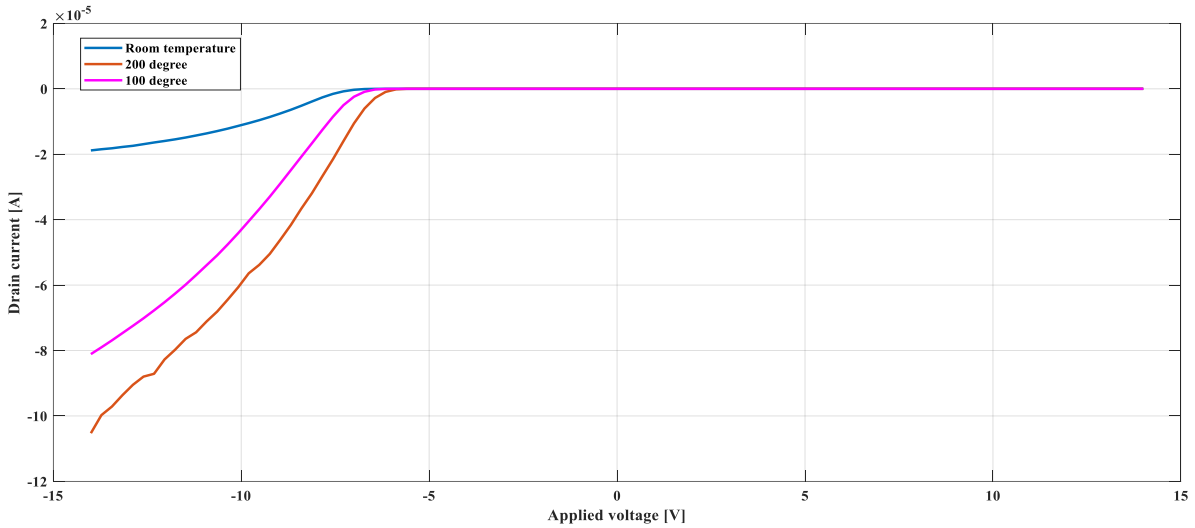

Fig. 6.21. $I_d - V_{gs}$ transfer characteristics sweeping for PMOS device.

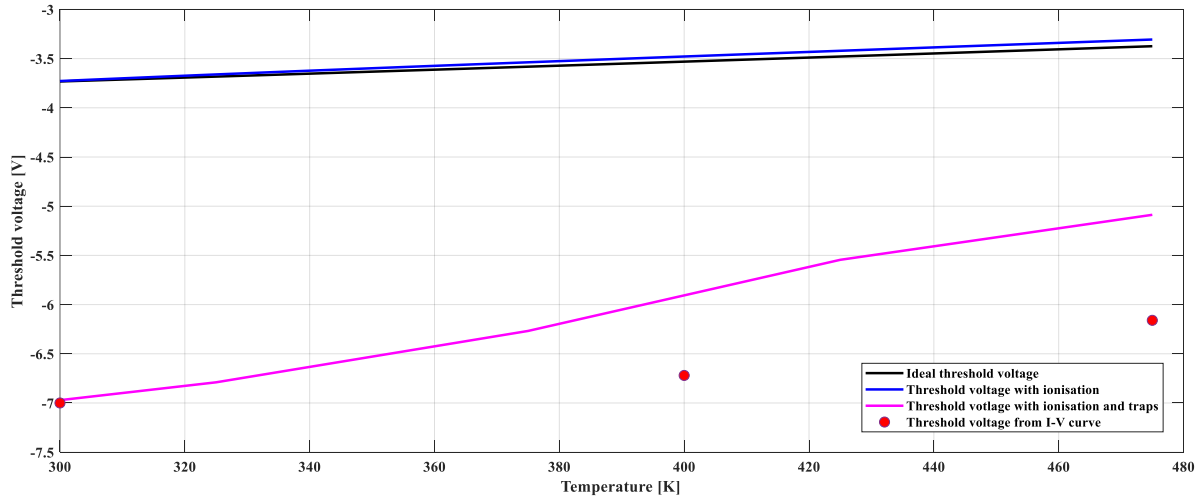

Fig. 6.22. The temperature reliability of intrinsic threshold voltage and the trap involved threshold voltage plot. Example is the n-type substrate (p-channel).

Fig. 6.22 illustrates and compares the ideal threshold voltage with incomplete ionisation and trapped charges affected threshold voltages, from room temperature to $200^{\circ}C$. Since the ionisation energy required is only $61.4meV$ for n-type substrate device, over 90% of dopant atoms are activated even at room temperature so that the ionisation cannot vary the threshold voltage too much. However, the traps near the n-type semiconductor is active. Compared with the threshold voltage with traps, the ideal threshold voltage needs to shift $-3.963V$ at room temperature and shifts $-1.782V$ at $200^{\circ}C$ to get the threshold voltage that under trapped charges. Although the dopant atoms are not fully activated at room temperature for p-type device, the threshold voltage is more stable than n-type device. The trapped charges need extra applied voltage to compensate so that the threshold voltage is shifted far away from the ideal curves.

In conclusion, the traps degrade the quality of the interface and further affects the performance of the device. Due to the slow response time of the trapped charges, the C-V curve hysteresis and capacitance gap are observable, as evidence of existence of the traps. The trap distribution can be extracted from both high and low C-V measurement, and the band edge trap density are extracted using exponential distribution. More importantly, the lifetime of the traps can be determined by sweeping the oscillation frequency and spotting out the global maximum.

The high temperature behaviour of the trapped charges is highlighted. The bandgap narrowing is observed in 4H-SiC due to the expansion of the SiC lattice. In addition, the trapped charges receive more energy from phonon are emitted into the conduction band, resulting in the more states empty, enhancement of the charge interaction and lifetime shortening. All of them are verified in experimental results..

7. Conclusions and future works

The final chapter quickly looks through the research questions and solutions of the project. Several recommendations and research directions are posed for the future.

7.1 Conclusions to the project

The theory in Si devices is not completely applicable to SiC devices. Due to the large bandgap, the minority generation time is so large that no inversion layer can be observed without excess charge carrier activation. Because of that, the capacitance in quasi-static C-V measurement in the depletion region is pushed into deep depletion rather than inversion. The defects, especially interfacial traps are then added to the ideal MOSCAP. Although the traps cannot follow the high frequency measurement signal, the devices still suffer from surface potential fluctuation and "stretch out" during C-V measurement.

Accurate characterisation of the device under test is essential for SiC modelling and parameter extractions. After introducing extraction methods of the threshold voltage, the electrical characterisation methods including the Terman method, low frequency method and $C_d - \varphi_s$ method are presented. In addition, the mathematical solutions of the trapped charges near the band edge and midband are both examined and analysed.

Beginning with the operational principle of the C-V measurement, the SiC MOSCAP under a sinusoidal signal is analysed. The modelling is based on the Shockey-Read-Hall generation and recombination theory, aiming to determine how the trap centres affect the charge transportation between the trap states and SiC lattice. Since the equilibrium condition does not hold, an observable transient current is generated, flowing from the Oxide-SiC interface to the substrate, where all the non-equilibrium charge carriers are stabilised. An equivalent circuit model is also built for a deep understanding of energy loss, which successfully links the energy space to real world three dimensional space. The capacitance is defined and calculated to show the charge holding ability of the trap centres, and the conductance represents the energy losses during stabilisation. The ratio of them with a unit of seconds, explains the average travel time that the trapped charges are thermalized.

The abovementioned equivalent circuit components are analysed again when the temperature is varying. The ionisation of dopant atoms in SiC lattice differs from Si, which is sensitive to temperature for acceptor dopant atoms, and that causes the Fermi level to shift towards the midband. First of all, the majority charge carriers respond and the depletion region is widened. More importantly, the occupancy probability changes accordingly, so that more trapped charges received energy from phonon are ejected into the conduction band at high temperature. As a result, the trap induced capacitance and conductance are changed accordingly. Chapter 5 summarises and analyses the behaviour of the traps in the band diagram, which supports the prediction calculated in chapter 4.

The COMSOL simulations and experimental evidences of traps and temperature effects are measured, extracted, compared and then analysed. The hysteresis analysis gives the insight to the trapped charges who cannot follow the sweeping signal, which is $1.4049\times10^{11}\mathrm{eV}^{-1}\mathrm{cm}^{-2}$. Although using the high frequency method or low frequency method alone can give the trap density, errors still are not negligible and the $C_d-\varphi_s$ extracts the trap distribution successfully, with the band edge density $4.079\times10^{11}\mathrm{eV}^{-1}\mathrm{cm}^{-2}$. The trapped charges are also sensitive to applied voltage. Due to the Fermi level shifting, the trap charges are pushed into substrate until they are thermalized, and the trapped charge density reduces from $8.521\times10^{11}\mathrm{eV}^{-1}\mathrm{cm}^{-2}$ to $7.261\times10^{11}\mathrm{eV}^{-1}\mathrm{cm}^{-2}$.

The high temperature measurement up to $200^{\circ}\mathrm{C}$ is performed. Although the high temperature leads to bandgap narrowing which suppresses the trap profiles, the band edge trap density also reduces from $4.079\times10^{11}\mathrm{eV}^{-1}\mathrm{cm}^{-2}$ to $2.208\times10^{11}\mathrm{eV}^{-1}\mathrm{cm}^{-2}$. The lifetime measurement also suggests the enhanced charge interaction under high temperature, since more trapped charges are released. Furthermore, the threshold voltages are extracted from the MOSFET by finding the maximum in the second order derivative, where the effect of traps and temperature sensitivity are indicated. The devices with n-type substrate degrade more since $+2.181\mathrm{V}$ threshold voltage shifting is obtained, whereas the threshold voltage in p-type only reaches $-0.893\mathrm{V}$.

7.2 Recommendations for future work

Due to the limitation of the experiment setup, the high temperature C-V measurement is only up to $200^{\circ}\mathrm{C}$. The reliability mechanism under extreme high temperature is attracting the researchers' attention recently. More defects and high temperature induced non-idealities are included, such as the tunnelling, charge pumping and crystal deformation. The first principle calculation may be a suitable tool to calculate the traps behaviour at atomic level.

For the traps in the SiC devices, there are two research directions. Researchers and engineers have been focusing on how to improve the quality of interface and reduce the trap density for decades. However, the interface quality in SiC cannot be comparable with silicon device. The annealing, thermal oxidation and new oxide material now are not well explored yet.

Another point of view is to utilise the threshold voltage variation and the trapped charges. Due to the tolerance of the high temperature, SiC is a potential material for temperature sensor. In addition, the trapped charges induced hysteresis in C-V measurement store the information, which have great prospect in memory devices.

Appendix

1. Mathematical solution of Poisson's equation

This section solves the differential Poisson's equation, referring to equation (2.12),

$$\frac{d^2\varphi_p(x)}{dx^2} = -\frac{q}{\varepsilon_{SiC}}\left[-p_{p0} + n_{n0} + p_{p0}\exp\left(-\frac{\varphi_p(x)}{V_t}\right) - n_{n0}\exp\left(\frac{\varphi_p(x)}{V_t}\right)\right] \tag{1}$$

Here, thermal voltage $V_t = kT/q$ is used for simplification. Multiply $d\varphi_p(x)$ on both sides and note that electrical field $F(x) = -d\varphi_p(x)/dx$, for the left hand side,

$$\int_0^{\frac{d\varphi_p(x)}{dx}} \frac{d\varphi_p(x)}{dx} d\frac{d\varphi_p(x)}{dx} = \int_0^{F(x)} -F(x)d(-F(x)) = \frac{F^2(x)}{2} \tag{2}$$

For the right hand side, the integral should be,

$$\frac{q}{\varepsilon_{SiC}}\int_0^{\varphi_p(x)}\left\{ p_{p0}\left[\exp\left(-\frac{\varphi_p(x)}{V_t}\right) - 1\right] + n_{n0}\left[\exp\left(\frac{\varphi_p(x)}{V_t}\right) - 1\right]\right\} d\varphi_p(x) \tag{3}$$

Solve that and combining both sides together,

$$\frac{F^2(x)}{2} = \frac{qV_t}{\varepsilon_{SiC}}\left\{ p_{p0}\left[\exp\left(-\frac{\varphi_p(x)}{V_t}\right) - \frac{\varphi_p(x)}{V_t}\right] + n_{n0}\left[\exp\left(\frac{\varphi_p(x)}{V_t}\right) - \frac{\varphi_p(x)}{V_t}\right]\right\} + M \tag{4}$$

where M is the integration constant, with the unit of V^2m^{-2}.

With the boundary condition $x \to +\infty$, where $\varphi_p(x) = 0$ and $F(+\infty) = 0$, previous electrical field is,

$$F^2(+\infty) = \frac{2qV_t}{\varepsilon_{SiC}}(p_{p0} + n_{n0}) + M = 0 \tag{5}$$

Substituting the integral constant back, the electrical field inside the substrate is,

$$F(x) = \pm\frac{\sqrt{2}kT}{qL_D}\sqrt{\frac{p_{p0}}{n_{n0}}\left[\exp\left(-\frac{\varphi_p(x)}{V_t}\right) - \frac{\varphi_p(x)}{V_t} - 1\right] + \left[\exp\left(\frac{\varphi_p(x)}{V_t}\right) - \frac{\varphi_p(x)}{V_t} - 1\right]} \tag{6}$$

where $L_D = \sqrt{\frac{V_t\varepsilon_{SiC}}{qn_{n0}}}$ is called Debye length.

2. Mathematical solution of interface trapped charges at midband.

The section shows the detailed steps of the solution of interface trapped charges. Referring equation (2.16), the trapped charges around midband should be,

$$Q_{it,Mid}\left(E,T\right)=-q\int_{E_i}^{E_C}D_{it0}f_A\left(E,T\right)dE \tag{1}$$

Substituting probability function back,

$$Q_{it,Mid}\left(E,T\right)=-q\int_{E_i}^{E_C}\frac{D_{it0}}{1+2\cdot\left(N_C/N_D\right)\cdot\exp\left[\left(E-E_C\right)/kT\right]}dE \tag{2}$$

Let $x\left(E\right)=\frac{1}{2}\exp\left(\frac{E-E_C}{kT}\right)$, so that $x\left(E_C\right)=\frac{1}{2}$ and $x\left(E_i\right)=\frac{1}{2}\exp\left(\frac{-E_g}{2kT}\right)$.

Note the relation,

$$d\left[x\left(E\right)\right]=\frac{x}{kT}dE \tag{3}$$

Rearrange that to find,

$$dE=kT\frac{dx}{x} \tag{4}$$

Equation (2) can be rewritten into,

$$Q_{it,Mid}\left(E,T\right)=-qkTD_{it0}\int\frac{dx}{x\left(1+4\cdot\left(N_C/N_D\right)\cdot x\right)} \tag{5}$$

The integral can be simplified into,

$$Q_{it,Mid}\left(E,T\right)=-\frac{qkTD_{it0}}{4}\frac{N_D}{n_i}\int\frac{1}{x}-\frac{1}{\left(1+4\cdot\left(N_C/N_D\right)\cdot x\right)}dx \tag{6}$$

$$Q_{it,Mid}\left(E,T\right)=-\frac{qkTD_{it0}}{4}\frac{N_D}{N_C}\left[\ln\left(x\right)-\frac{N_D}{4N_C}\ln\left(1+4\cdot\left(N_C/N_D\right)\cdot x\right)\right] \tag{7}$$

Substituting boundary condition into equation (7),

$$Q_{it,Mid}\left(\frac{1}{2}\right)=-\frac{qkTD_{it0}}{4}\frac{N_D}{N_C}\left[\ln\left(\frac{1}{2}\right)-\frac{N_D}{4N_C}\ln\left(1+\frac{2N_C}{N_D}\right)\right] \tag{8}$$

$$Q_{it,Mid}\left(x\left(E_i\right)\right)=-\frac{qkTD_{it0}}{4}\frac{N_D}{N_C}\left[\frac{-E_g}{2kT}+\ln\left(\frac{1}{2}\right)-\frac{N_D}{4N_C}\ln\left(1+\frac{2N_C}{N_D}\exp\left(\frac{-E_g}{2kT}\right)\right)\right] \quad (9)$$

The midband interface trapped charge now is determined,

$$Q_{it,Mid}\left(E,T\right)=-\frac{qD_{it0}}{4}\frac{N_D}{n_i}\left\{\frac{E_g}{2}+\frac{kTN_D}{4n_i}\left[\ln\left(\frac{N_D+2N_C\exp\left(-E_g/2kT\right)}{N_D+2N_C}\right)\right]\right\} \quad (10)$$

Rearranging that, equation (10) is equivalent to,

$$Q_{it,Mid}\left(E,T\right)=-\frac{qD_{it0}N_D}{4n_i}\left\{\frac{E_g}{2}+\frac{kTN_D}{4n_i}\ln\left[1+\frac{2N_C}{N_D+2N_C}\left(\exp\left(\frac{-E_g}{2kT}\right)-1\right)\right]\right\} \quad (11)$$

Note the relation in SiC, $N_C/N_D>>1$, and the Taylor series of $\ln\left(1+x\right)$ is,

$$\ln\left(1+x\right)=x-\frac{x^2}{2}+\frac{x^3}{3}-\frac{x^4}{4}... \quad (12)$$

Since $E_g=3.26eV$ and $kT=0.026eV$, $\exp\left(\frac{-E_g}{2kT}\right)-1$ approaches to -1.

$\frac{2N_C}{N_D+2N_C}\left(\exp\left(\frac{-E_g}{2kT}\right)-1\right)$ approaches to $-\frac{2N_C}{N_D+2N_C}=-1$

For first approximation of Taylor series, equation (11) turns out to be,

$$Q_{it,Mid}\left(E,T\right)=-\frac{qD_{it0}N_D}{4n_i}\left(\frac{E_g}{2}-\frac{kTN_D}{4n_i}\right) \quad (12)$$

The doping concentration comparing with intrinsic carrier in SiC shows $\frac{E_g}{kT}<<\frac{N_D}{n_i}$

As a result, $Q_{it,Mid}\left(E,T\right)=\frac{qD_{it0}kT}{16n_i}\left(\frac{N_D}{n_i}\right)^2$

Substituting $n_i=N_C\exp\left(\frac{E_F-E_C}{kT}\right)$ and $a=2\left(N_C/N_D\right)$

$$Q_{it,Mid}\left(E,T\right)=\frac{qD_{it0}kT}{4a^2}\exp\left(\frac{E_C-E_F}{0.5kT}\right)$$

3. Mathematical solution of interface trapped charges near band edge.

Referring equation (2.17), the trapped charges around midband should be,

$$Q_{it,Edge}(E,T) = -q\int_{E_i}^{E_C} D_c \exp\left(-\frac{E_c - E}{\sigma}\right)\cdot f_A(E,T)\,dE \tag{12}$$

Substituting probability function back,

$$Q_{edge} = -qD_{edge}\int_{E_i}^{E_C} \exp\left(\frac{E - E_c}{\sigma}\right)\frac{1}{1+\frac{2N_C}{N_D}\exp\left(\frac{E - E_c}{kT}\right)}\,dE \tag{13}$$

Let $z = \exp\left[(E - E_c)\backslash\sigma\right]$, for $E \in (E_i, E_C)$ satisfying $z \in \left(\exp(-E_g \backslash 2\sigma), 1\right)$, so that the exponential terms $m = \exp(-E_g \backslash 2\sigma)$ approaches to 0, thus $z \in (0,1)$.

For the following steps, we use a large positive number $a = 2(N_C / N_D)$, arbitrary positive number $b = \frac{\sigma}{kT} > 1$ and $z \in (0,1)$ to simplify the expression.

Note the relation,

$$dz = \exp\left(\frac{E - E_c}{\sigma}\right)\frac{dE}{\sigma} \tag{14}$$

Rearrange that to obtain,

$$dE = \sigma\frac{dz}{z} \tag{15}$$

The exponential relation holds,

$$\exp\left(\frac{E - E_c}{kT}\right) = \exp\left(\frac{E - E_c}{\sigma}\cdot\frac{\sigma}{kT}\right) = z^b \tag{16}$$

Replacing exponential terms by z gives,

$$Q_{edge} = -qD_{edge}\int_0^1 \frac{\sigma dz}{1 + a\cdot z^b} \tag{17}$$

Let $t = \frac{1}{1+az^b}$, for $z \in (0,1)$, satisfying $t \in (0,1)$

Rearrange to express z as a function of t.

.

$$z=\left[\frac{1}{a}\left(t^{-1}-1\right)\right]^{\frac{1}{b}}=\frac{1}{\sqrt[b]{a}}\left(1-t\right)^{\frac{1}{b}}t^{-\frac{1}{b}} \tag{18}$$

Find the derivative with respect to t,

$$dz=-\frac{1}{\sqrt[b]{a}}\left(1-t\right)^{\frac{1}{b}-1}\frac{1}{b}t^{-1-\frac{1}{b}}dt \tag{19}$$

Substituting into equation (17),

$$Q_{edge}=\frac{q\sigma D_{edge}}{\sqrt[b]{a}\cdot b}\int_{1}^{0}t^{-\frac{1}{b}}\left(1-t\right)^{\frac{1}{b}-1}dt \tag{20}$$

The function with respect to t is called beta function $B(P,Q)$, which is defined as,

$$B(P,Q)=\int_{0}^{1}x^{P-1}\left(1-x\right)^{Q-1}dx \tag{21}$$

where P and Q are arbitrary positive number. The Beta function has the property, for $P+Q=1$, the integration is called Euler integral of the first kind,

$$B\left(-x+1,x\right)=\frac{\pi}{\sin\left(\pi/x\right)} \tag{22}$$

The integral in equation (21) can be expressed by Beta function as follows,

$$\int_{0}^{1}t^{-\frac{1}{b}}\left(1-t\right)^{\frac{1}{b}-1}dt=B\left(-\frac{1}{b}+1,\frac{1}{b}\right)=\frac{\pi}{\sin\left(\pi/b\right)} \tag{23}$$

Based on that, equation (21) can be solved by,

$$Q_{edge}=-\frac{q\sigma D_{edge}}{\sqrt[b]{a}}\frac{\pi/b}{\sin\left(\pi/b\right)} \tag{24}$$

4. Conductance measurement results at high temperature

- Conductance measurement at $75^{\circ}C$

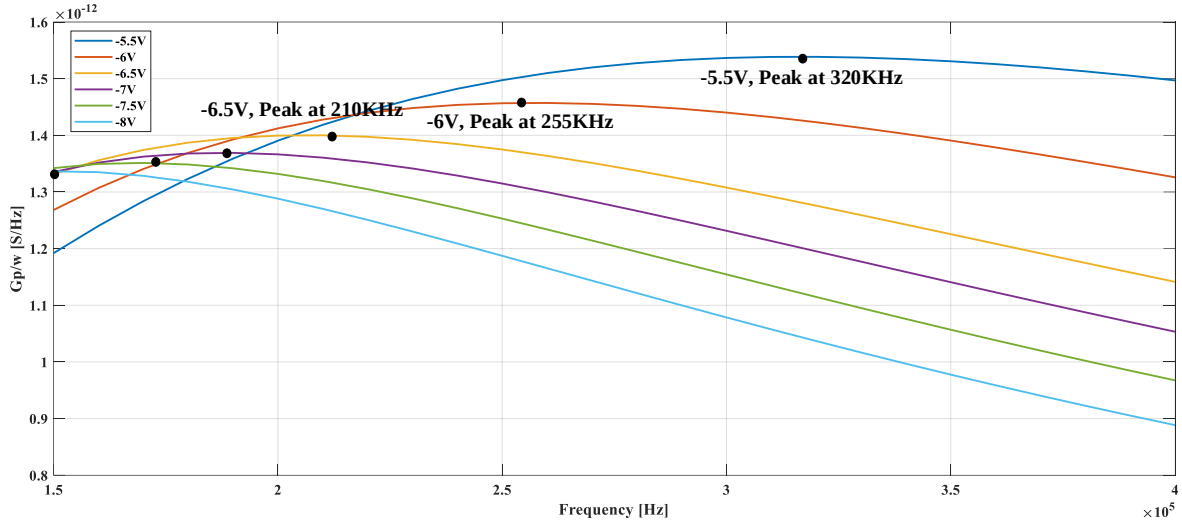

Fig. A4.1. G_p / ω measurement of n-type SiC MOSCAP at $75^{\circ}C$ as a function of oscillation frequency, with all peak points and corresponding frequencies indicated.

Table. A4.1. Experimental trap information extracted by n-type substrate SiC MOSCAP, at $75^{\circ}C$.

Biased voltage [V]	$\max\left(G_p / \omega\right)$ [S / Hz]	D_{it} [$eV^{-1}cm^{-2}$]	τ_{it} [μs]
-5.5	1.539×10^{-12}	8.504×10^{11}	3.125
-6	1.457×10^{-12}	8.052×10^{11}	3.922
-6.5	1.400×10^{-12}	7.738×10^{11}	4.762
-7	1.369×10^{-12}	7.565×10^{11}	5.263
-7.5	1.351×10^{-12}	7.466×10^{11}	5.882
-8	1.336×10^{-12}	7.383×10^{11}	6.000

- Conductance measurement at $100^{\circ}C$

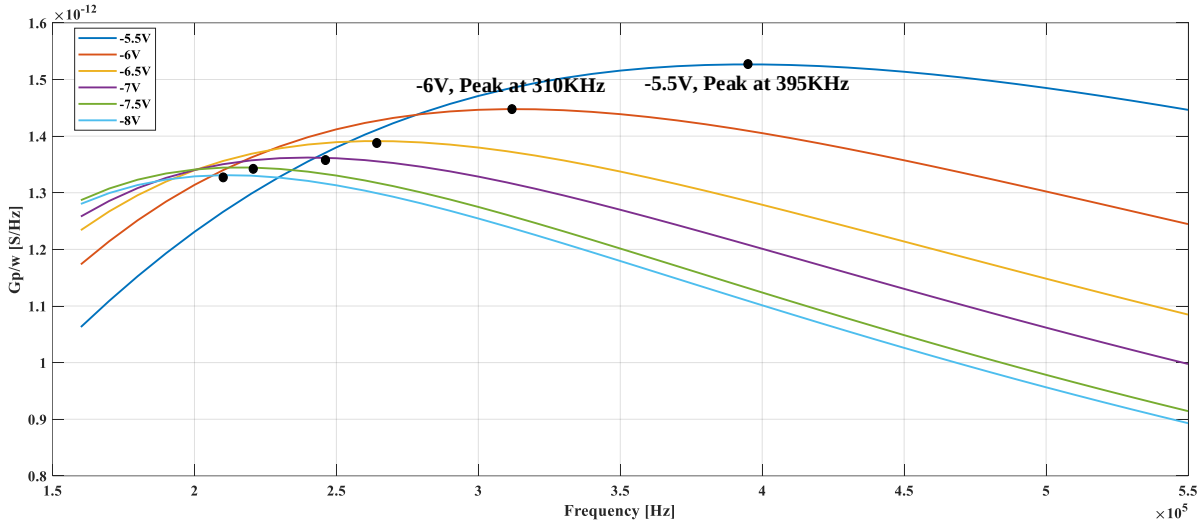

Fig. A4.2. G_p / ω measurement of n-type SiC MOSCAP at $100^{\circ}C$ as a function of oscillation frequency, with all peak points and corresponding frequencies indicated.

Table. A4.2. Experimental trap information extracted by n-type substrate SiC MOSCAP, at $100^{\circ}C$.

Biased voltage [V]	$\max\left(G_p / \omega\right)$ [S / Hz]	D_{it} [$eV^{-1}cm^{-2}$]	τ_{it} [μs]
-5.5	1.527×10^{-12}	8.439×10^{11}	2.532
-6	1.447×10^{-12}	7.996×10^{11}	3.226
-6.5	1.391×10^{-12}	7.687×10^{11}	3.774
-7	1.362×10^{-12}	7.527×10^{11}	4.164
-7.5	1.345×10^{-12}	7.433×10^{11}	4.545
-8	1.330×10^{-12}	7.350×10^{11}	4.762

- Conductance measurement at $150^{\circ}C$

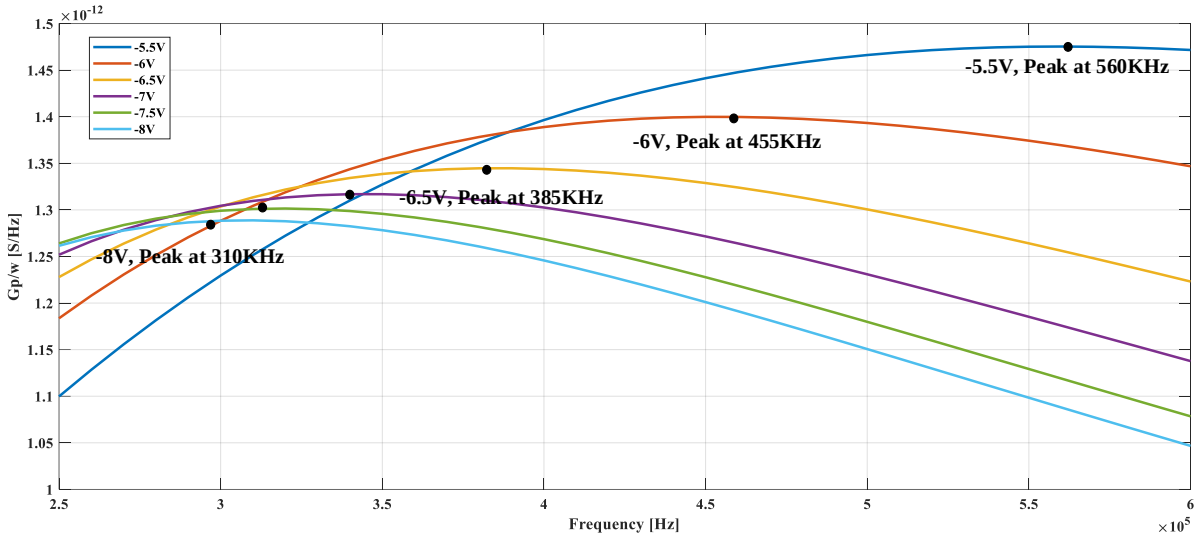

Fig. A4.3. G_p / ω measurement of n-type SiC MOSCAP at $150^{\circ}C$ as a function of oscillation frequency, with all peak points and corresponding frequencies indicated.

Table. A4.3. Experimental trap information extracted by n-type substrate SiC MOSCAP, at $150^{\circ}C$.

Biased voltage [V]	$\max\left(G_p / \omega\right)$ [S / Hz]	D_{it} [$eV^{-1}cm^{-2}$]	τ_{it} [μs]
-5.5	1.475×10^{-12}	8.151×10^{11}	1.786
-6	1.400×10^{-12}	7.737×10^{11}	2.198
-6.5	1.345×10^{-12}	7.433×10^{11}	2.597
-7	1.317×10^{-12}	7.278×10^{11}	2.941
-7.5	1.301×10^{-12}	7.190×10^{11}	3.175
-8	1.289×10^{-12}	7.123×10^{11}	3.226

- Conductance measurement at $175^{\circ}C$

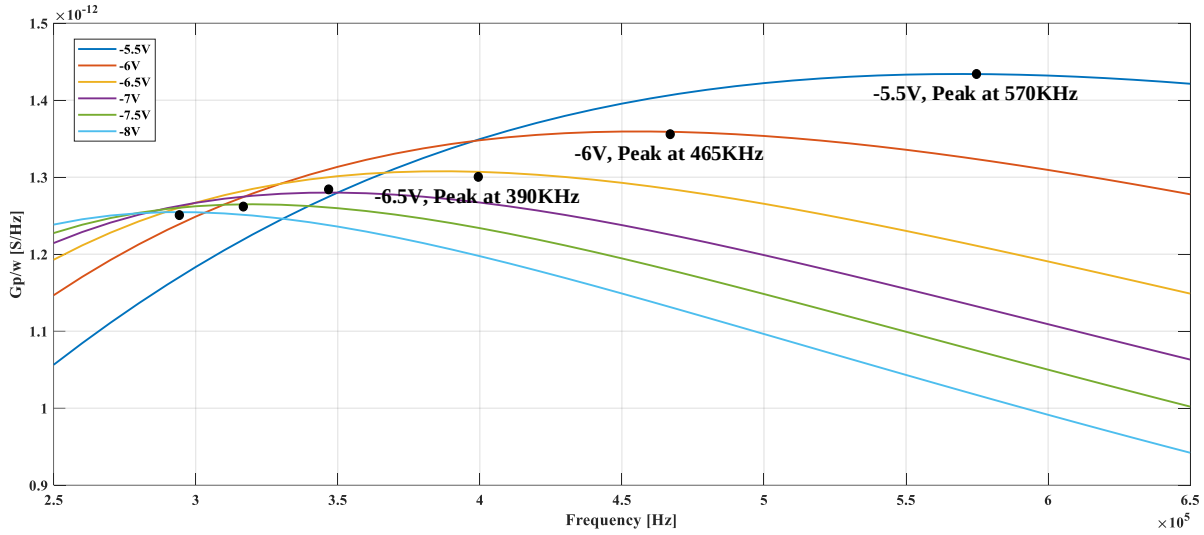

Fig. A4.4. G_p / ω measurement of n-type SiC MOSCAP at $175^{\circ}C$ as a function of oscillation frequency, with all peak points and corresponding frequencies indicated.

Table. A4.4. Experimental trap information extracted by n-type substrate SiC MOSCAP, at $175^{\circ}C$.

Biased voltage [V]	$\max\left(G_p / \omega\right)$ [S / Hz]	D_{it} [$eV^{-1}cm^{-2}$]	τ_{it} [μs]
-5.5	1.434×10^{-12}	7.925×10^{11}	1.754
-6	1.359×10^{-12}	7.510×10^{11}	2.151
-6.5	1.308×10^{-12}	7.228×10^{11}	2.564
-7	1.280×10^{-12}	7.074×10^{11}	2.899
-7.5	1.265×10^{-12}	6.991×10^{11}	3.125
-8	1.255×10^{-12}	6.935×10^{11}	3.448

- Conductance measurement at $200^{\circ}C$

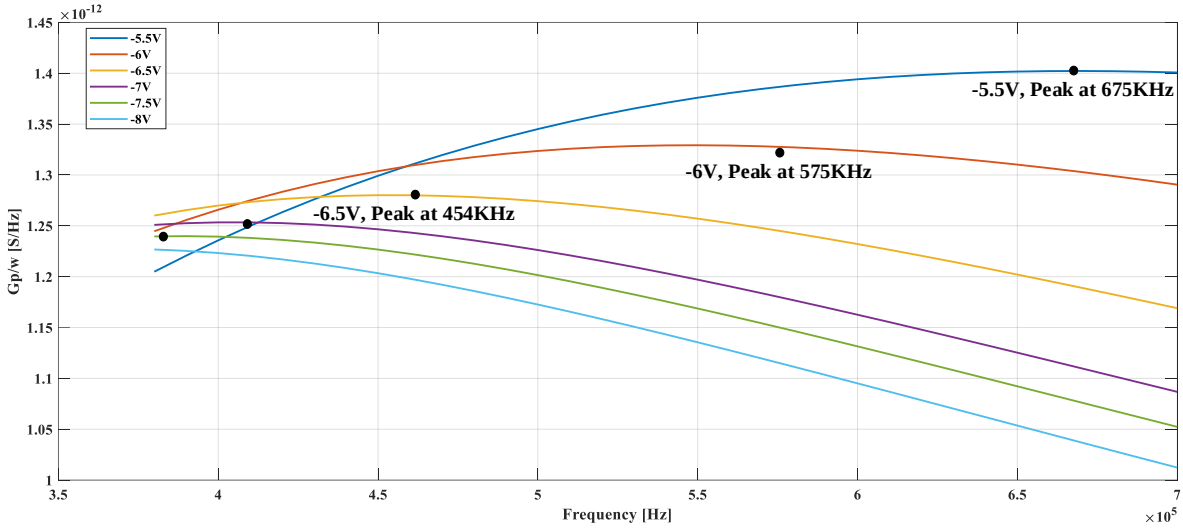

Fig. A4.5. G_p / ω measurement of n-type SiC MOSCAP at $200^{\circ}C$ as a function of oscillation frequency, with all peak points and corresponding frequencies indicated.

Table. A4.5. Experimental trap information extracted by n-type substrate SiC MOSCAP, at $200^{\circ}C$.

Biased voltage [V]	$\max\left(G_p / \omega\right)$ [S / Hz]	D_{it} [$eV^{-1}cm^{-2}$]	τ_{it} [μs]
-5.5	1.402×10^{-12}	7.748×10^{11}	1.485
-6	1.329×10^{-12}	7.344×10^{11}	1.739
-6.5	1.280×10^{-12}	7.074×10^{11}	2.198
-7	1.253×10^{-12}	6.924×10^{11}	2.410
-7.5	1.240×10^{-12}	6.853×10^{11}	2.597

5. Trap distribution near the valance band edge

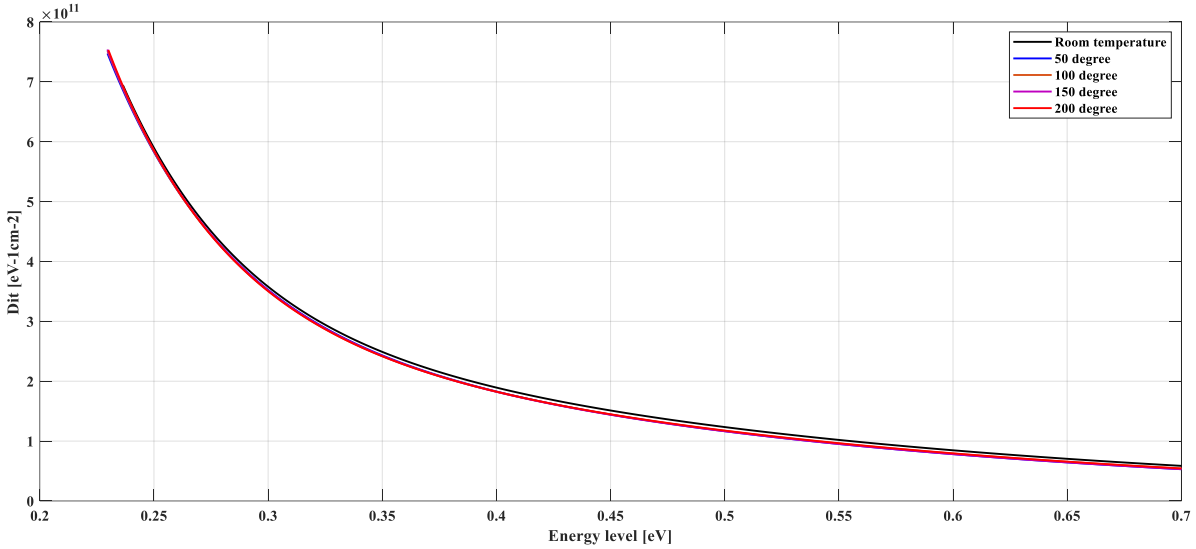

Fig. A5.1. Measured trap distribution in band diagram under $50^{\circ}C$, $100^{\circ}C$, $150^{\circ}C$ and $200^{\circ}C$.

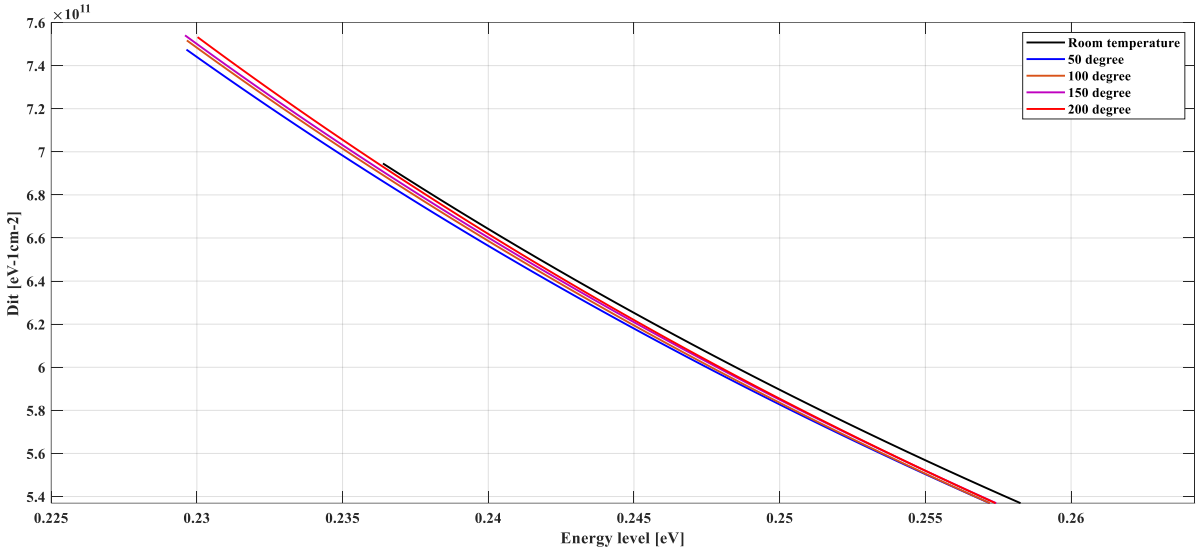

Fig. A5.2 Zoom in version of trap distribution the temperature dependency.

Table. A5.1. Extraction of trap information for temperature effect analysis.

Temperature [$^{\circ}C$]	$D_{it,edge}[eV^{-1}cm^{-2}]$	σ[eV]
25	9.422×10^{10}	1.343
50	1.31×10^{11}	1.711
100	1.301×10^{11}	1.815
150	1.301×10^{11}	1.776
200	1.252×10^{11}	1.824

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