Improvement on the short-circuit Performance of SiC MOSFET with different shapes and materials of the dielectric layer

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***Abstract*—In this paper, the effect of thermal stress on the reliability of the gate dielectric layer of SiC MOSFET at high short-circuit temperature is studied. By modeling and simulation, different shapes and materials (SiO_2, BPSG, Si_3N_4) of the dielectric layer were compared regarding their stress distribution effects. Results indicate that elliptical gate structures and dual-layer ILD configurations perform better under thermal stress than conventional designs, particularly with Si_3N_4 as the inner layer and BPSG as the outer layer. This optimization scheme aims to enhance the reliability of SiC MOSFETs.**

Keywords—Silicon Carbide (SiC), Short-Circuit failure, Reliability, Thermal stress

I. INTRODUCTION

Third-generation wide bandgap semiconductor devices are entering a phase of robust development, with SiC gaining widespread attention due to its exceptional material properties [1], [2], [3]. The penetration of SiC MOSFETs in various fields is increasing; however, reliability issues have become a significant bottleneck hindering the broader adoption and application of SiC MOSFETs. The stress on the gate dielectric layer at high temperatures directly impacts the reliability of SiC MOSFETs, and excessive stress generated under short-circuit conditions can lead to device failure [4], [5]. Thus, researching the stress in the gate dielectric layer at high temperatures is a crucial direction for enhancing the reliability of SiC devices.

This paper models the gate dielectric layer based on the unit cell structure of mainstream SiC MOSFETs and simulates its thermal stress under short-circuit high temperatures. Subsequently, the simulation is performed by altering the shape and materials of the gate dielectric layer, followed by a comparative analysis of thermal stress levels, ultimately proposing strategies to improve the stress in the gate dielectric layer.

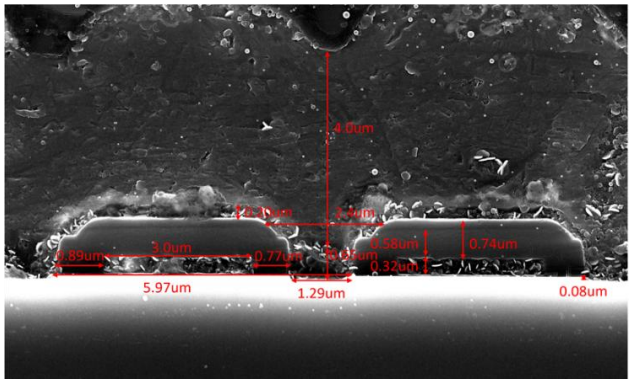

Fig.1 Cross-sectional SEM image of SiC MOSFET cell

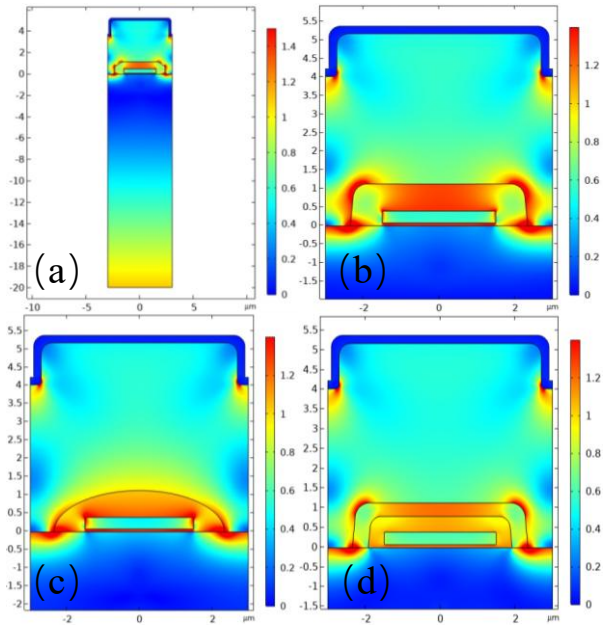

Fig.2 Gate modeling of different ILD layer shapes

The second part introduces the design parameters of the cell structure and the model modification scheme. The third part introduces the gate-source short-circuit mechanism of SiC MOSFET. In the fourth part, we simulate the thermal stress of the model by COMSOL simulation. At the same time, COMSOL simulation software is used to analyze the stress of different shapes of dielectric layers. It is found that by improving the shape and material of the gate dielectric layer, the stress distribution of the dielectric layer can be improved. In the fifth part, the thermal stress simulation results and mechanism analysis of different dielectric shapes and materials are given. Finally, the sixth part summarizes the conclusion of this paper.

II. DEVICE STRUCTURE

Fig.1 shows the SEM image of Cree's C3M0040120K power device. This is a 1.2kV commercial SiC planar MOSFET power device. Its cell structure data was observed and measured by SEM, and its cell size was simulated and modeled by COMSOL.

Some scholars have found that the unique gate failure mode characterized by a sudden increase in gate voltage occurs earlier than the standard runaway mode [6], [7], [8]. This kind of gate failure mode is unique, and it occurs in a very short time after aluminum metal melts after a short circuit [3]. Therefore, this paper mainly studies the influence of high temperature generated by the device under short circuit current on its stress level. Therefore, the influence of other than current heat on the ILD layer damage is ignored, so the test temperature is set to 1040K junction temperature, and the source Al metal layer reaches the melting point (933K) to conduct simulation, and this condition is used to explore the high temperature generated during short circuit. According to the design size of Cree's C3M0040120K device, the stress distribution of the ILD layer is improved and optimized on this basis, and the stress is analyzed and compared after the shape of the ILD layer is changed, and then the stress is analyzed and compared after the material of the gate ILD layer is changed. Finally, on the basis of the trapezoidal gate shape, the ILD layer of the gate was changed to two layers, and the stress was analyzed and compared. In this paper, COMSOL was used for modeling, and Fig.2 shows the modeling for this series of comparisons.

III. THERMAL STRESS MECHANISM

SiC MOSFET short-circuit failure is divided into thermal failure, degradation failure, and gate-source short-circuit failure. Among them, this paper mainly studies the gate-source short-circuit failure. The active region of the device with gate-source short-circuit failure will burn out in a large area, because the current concentration near the gate leads to extremely high temperature, and the thermal expansion coefficients of silicon dioxide, silicon carbide and polysilicon are different. At high temperatures, the dielectric layer is damaged due to the thermal stress caused by the large deformation of these materials. The damage to the gate structure causes the melted source metal to penetrate into the gate dielectric layer and the gate medium, resulting in a short circuit between the gate and the source. After the short-circuit failure of the gate-source, the device will lose the ability to control the channel, and there will be a direct current between the source and the drain stage. The electron and hole current generated by thermal excitation cannot be reduced through the combination, but positive feedback will be formed with the increase in temperature, and the device will eventually burn out due to excessive temperature.

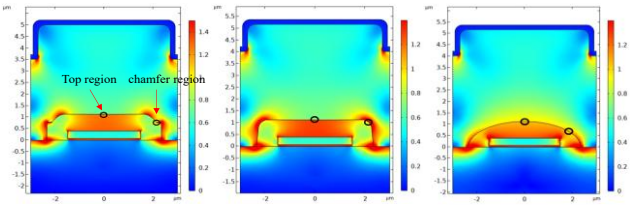

Fig.3 Measure the stress on vulnerable region of ILD layer with different shapes.

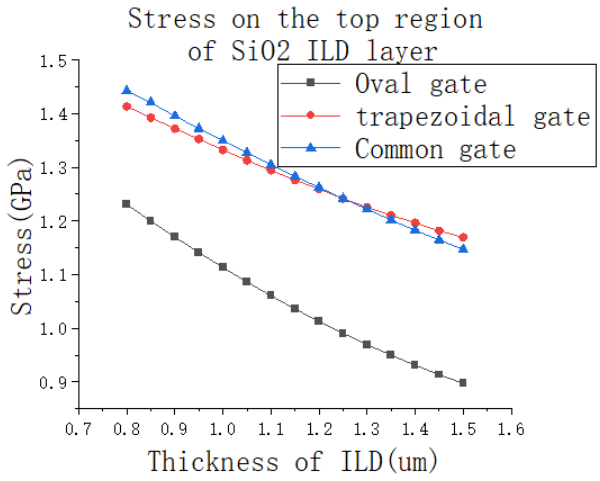

Fig.4 The stress on the top region of ILD layer with different shapes.

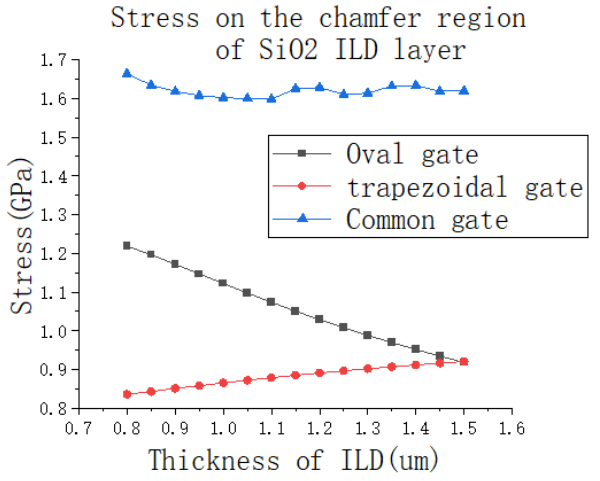

Fig.5 The stress on the chamfer region of ILD layer with different shapes.

The relationship between the ILD layer and stress is an important research topic in integrated circuit manufacturing because stress will affect the performance and reliability of the device; stress sources are divided into three kinds: internal stress, thermal stress, and external stress, internal stress is caused by the nature of the material itself, such as the lattice mismatch during the film growth process, thermal expansion coefficient difference and other forms of stress. Thermal stress is due to the different coefficients of thermal expansion of different materials in the manufacturing process, and external stress is the stress caused by external mechanical forces or environmental factors. In this paper, the thermal stress is mainly analyzed.

IV. SIMULATION RESULTS AND ANALYSIS

We measured and analyzed the thermal stress in two vulnerable regions in ILD layers of different shapes and materials.

A. Multi-physics model

In the study of thermal expansion, the relationship between temperature change and dimensional variation is quantitatively expressed by the equation:

$$\Delta L=\alpha L_0 \Delta T \tag{1}$$

Where ΔL denotes the change in length, α represents the coefficient of linear expansion specific to the material, L_0 is the initial length of the material, and ΔT indicates the change in temperature. This equation illustrates how materials expand or contract in response to temperature fluctuations, providing critical insights for applications in engineering and materials science. Understanding these principles is essential for designing structures and components that can withstand thermal variations without compromising integrity.

Since this paper focuses on the study of the gate-source short-circuit failure mode, the temperature is set to the temperature when Al melts (933K), which is the time node when the gate-source short-circuit failure occurs. In addition, periodic conditions are applied to the physical fields on both sides of the cell to better simulate the stress of the periodic cell in the device.

B. Simulation result analysis

Fig.3 shows three different structures of the SiO_2 ILD layer. For the three different ILD layer shapes, we select two points from left to right to analyze the stress size under different ILD layer thicknesses, measure the stress size of the points, and compare the stress size of the three different ILD layer shapes. Fig.4 and Fig.5 show the variation of pressure in different regions of the three shapes with the thickness of the ILD layer.

Through the analysis of the two line diagrams, it can be found that the ILD layer of the ordinary gate shape is not conducive to withstand the stress due to excessive chamfer, and it can be seen from the curve that the stress performance of the two measured areas is poor. The ILD layer of the trapezoidal gate has less chamfering and larger curvature than the ordinary gate so the stress can be dispersed, and the stress performance is better than the ordinary gate. When the ILD layer thickness was 1.2um and 1.25um, the stress distribution of the ILD layer was the most uniform. In addition, proper thickening of the ILD layer could improve the insulation. Therefore, it is more appropriate to set the height of the ILD layer of the elliptical gate at 1.25um. Therefore, the stress can be more evenly distributed throughout the ILD layer, but because the side source (Al) and gate (Poly) thickness of the elliptical ILD layer are thinner than that of the trapezoidal ILD layer and the ordinary ILD layer, the electrical insulation performance of the elliptical ILD layer may be worse than that of the other two kinds of ILD layers.

Then, we replaced the materials of the ordinary gate, trapezoidal gate, and elliptical gate ILD layers, replaced SiO_2

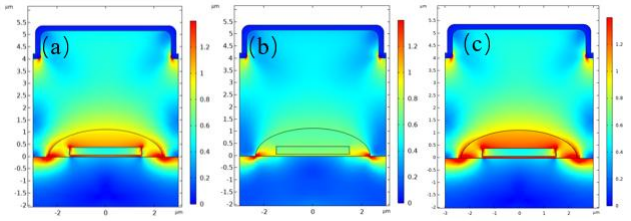

Fig.6 Simulated the stress of ILD layer (a) use BPSG as the ILD (b) use Si_3N_4 as the ILD (c) use SiO_2 as the ILD.

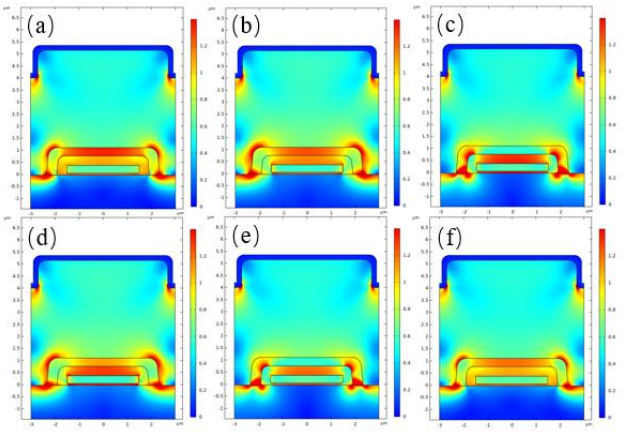

Fig.7 Simulated the stress of ILD layer (a) use SiO_2 (outer) and Si_3N_4 (inner) as the ILD (b) use SiO_2 (outer) and BPSG (inner) as the ILD (c) use Si_3N_4 (outer) and SiO_2 (inner) as the ILD (d) use Si_3N_4 (outer) and SiO_2 (inner) as the ILD (e) use Si_3N_4 (outer) and BPSG (inner) as the ILD (f) use BPSG (outer) and Si_3N_4 (inner) as the ILD.

with BPSG and Si_3N_4, and carried out stress analysis under the same conditions.

After our comparison of the thermal stress of each shape of ILD layer using different materials. We found that the thermal stress performance when using the elliptical ILD layer was still better than that of the other two shapes. This is the same as the performance when SiO_2 was used as the ILD layer material before. Therefore, in this paper, we only present the thermal stress modeling results of different materials in the elliptical ILD layer. Fig.6 shows that the overall stress in the whole ILD layer when BPSG and Si_3N_4 are used is smaller than that when SiO_2 is used. At the same time, the strength of Si_3N_4 is much higher than that of SiO_2 and BPSG so the probability of gate-source short-circuit failure will be greatly reduced when Si_3N_4 is used. The results obtained through simulation modeling are as follows: Without considering the process difficulty and cost, when SI3N4 is used as the ILD layer material, its thermal stress performance is better. Therefore, the possibility of gate-source short-circuit failure will be greatly reduced.

Compared with the ordinary ILD layer, the stress in two regions of the elliptical ILD layer decreased by 19.2% and 35.3% respectively, greatly alleviating the thermal stress generated at its short-circuit temperature. Moreover, research has shown that gate source short circuit failure can cause the device to fail about 2us before normal short circuit failure, and the use of a smaller stress ILD layer shape can avoid gate source short circuit failure. Therefore, its theoretical short circuit withstand time is increased by about 2us.

Finally, for the double-layer ILD layer, after our comparison after modeling different shapes. Ultimately, we found that for the thermal stress performance of the double-layer ILD layer, the performance of the trapezoidal ILD layer was superior to that of the other two shapes. So in the end, we used the trapezoidal ILD layer as the overall shape for analysis and compared it by changing the material and thickness distribution of the double-layer. The material of the ILD layer consisted of SiO_2, BPSG, and Si_3N_4, and the thickness was changed by 0.05um each time. As shown in Fig.7 (a), Fig.7 (b), Fig.7 (c) and Fig.7 (d), the performance of SiO_2 material in double-layer ILD layer is poor.

The stress performance is optimal when the inner layer is Si_3N_4, the outer layer is BPSG, and the inner layer thickness is between 0.35um and 0.45um.

V. The Thermal Stress Mechanism Analysis

The above simulation results show that ILD layer thickness and material will directly affect the size and distribution of thermal stress at high short-circuit temperatures, thus affecting the reliability of the device. There may be many factors affecting the thermal stress of the ILD layer, but the thickness and material are the two most important factors. From the thickness level, the first is that the increase of film thickness will increase the stress accumulation; with the increase of ILD layer thickness, if the stress exceeds a certain threshold, it will lead to cracking or warping of the film. Secondly, the thermal stress is directly related to the thickness of the film; the greater the thickness, the more obvious the thermal stress effect, especially between materials with large differences in thermal expansion coefficients; that is, the greater thermal stress concentration will be generated at the chamfer of the ILD layer. By changing the shape of the ILD layer, the thermal stress concentration caused by the more drastic material transition and the larger geometry change at the chamfer can be greatly alleviated.

For an ordinary gate ILD layer, there are many chamfers, and the stress is easy to concentrate at the chamfer, which leads to cracks in the gate ILD layer of the device at high temperature, and the source metal that reaches the melting temperature penetrates into it, and finally leads to the gate-source short-circuit failure before the device burns out in a large area at high short-circuit temperature. Through simulation, it is found that the stress distribution of the conventional gate is not uniform, and the stress is larger at high temperatures, while the trapezoid and oval gate have more uniform stress distribution and less internal stress, and the ILD layer of the gate has better reliability because of the smoother geometry change.

As for the impact of materials, after investigating the SiC MOSFET devices of various companies on the market, it is found that among the existing products, BPSG (borosilicate glass) and Si_3N_4 (silicon nitride) are the most commonly used interlayer dielectric materials to replace SiO_2, so these two materials are also used in this paper for simulation.

BPSG has several advantages; the first is that the fluidity of BPSG is very good; BPSG has good fluidity at high temperatures and can effectively fill complex grooves and voids, improving the coverage and flatness of the process. Secondly, the deposition temperature of BPSG is low, usually below 400°C, which is advantageous for heat-sensitive devices and metal layers. Finally, BPSG can

effectively relieve stress; adding boron and phosphorus can relieve the stress and reduce the mechanical stress inside the film layer, thus reducing the risk of stress-induced failure of the device. However, at the same time, BPSG also has some disadvantages, such as poor stability under wet chemical conditions, BPSG is more unstable in wet chemical environments, and is prone to water erosion, resulting in deterioration of the material. Second, the electrical insulation properties of BPSG for Si_3N_4 and SiO_2, the dielectric constant is low (about 4.5), may lead to higher parasitic capacitance.

In comparison, the first advantage of Si_3N_4 is excellent electrical insulation; Si_3N_4 has a very high dielectric constant (about 7.5) and shows excellent electrical insulation performance in high-frequency applications, which can reduce parasitic capacitance. Secondly, the mechanical strength and hardness of Si_3N_4 are very high, which helps to protect the underlying structure from mechanical damage. Finally, with good chemical stability, Si_3N_4 has excellent stability in various chemical environments and is not easy to be corroded by chemical reagents. However, Si_3N_4 also has some disadvantages; first of all, the deposition temperature of Si_3N_4 is high, usually above 700°C, and its fluidity is poor; Si_3N_4 has no artifact characteristics during the deposition process, and it is not as easy as BPSG to fill complex structures and trenches. Therefore, the use of Si_3N_4 as an ILD layer material has high requirements for the process, and the density and flatness of Si3N4 have high requirements, and the substandard Si_3N_4 can not show its good electrical and mechanical properties.

Comprehensive comparison of BPSG and Si_3N_4. Among them, BPSG has good fluidity, flatness, low-temperature process, and stress relief characteristics, but at the same time, its stability in a wet chemical environment is worse than Si_3N_4. Si_3N_4 has excellent electrical insulation, high mechanical strength, and chemical stability, but its high process requirements are its disadvantages. Generally, BPSG is suitable for applications that require good filling and low-temperature processes, especially in complex structures and heat-sensitive devices. Si_3N_4 is suitable for applications requiring high mechanical strength and excellent electrical insulation properties. It is also suitable for use in high-frequency devices and environments requiring high chemical stability.

In general, for single-layer materials, it is found through simulation that the stress performance of an elliptic gate is better than that of an ordinary gate and trapezoidal gate, the stress distribution of an elliptic gate is more uniform, and the total stress is smaller. In terms of material, Si_3N_4 was chosen because of its high mechanical strength; its stress performance will be better. However, through the investigation of devices on the market, it is found that almost all of them use BPSG to replace SiO_2 as the ILD layer material. This may be due to the fact that the hardness and brittleness of Si_3N_4 which is difficult to overcome when the temperature changes will cause the device to be easily damaged due to the rapid change in temperature leading to the damage of ILD layer, so BPSG is used as the material of ILD layer. BPSG has excellent hole-filling ability due to its loose structure and fluidity under high-temperature conditions. It can improve the flattening of the surface of the whole ILD layer and provide a larger process range for lithography and post-processing.

For double ILD layers, the use of Si_3N_4 in the inner layer can ensure the electrical insulation near the gate is well protected, while the use of BPSG with fluidity in the outer layer can effectively improve the disadvantage of Si_3N_4 in hardness and brittleness, which greatly alleviates the stress problem caused by temperature.

VI. CONCLUSION

By comprehensive comparison of various structures of the ILD layer, for the single-layer ILD layer, the stress distribution of the elliptical gate ILD layer is more uniform than that of the ordinary gate and trapezoidal gate, and the total stress is smaller. From the perspective of stress, the use of Si_3N_4 instead of SiO_2 can reduce the stress to the greatest extent. Using BPSG as ILD layer material in practical applications will improve the overall performance of the device. For a double ILD layer, the trapezoidal gate is used, the inner layer is Si_3N_4, the outer layer is BPSG, and the stress performance is optimal when the inner layer thickness is between 0.35um and 0.45um, and the advantages of both Si_3N_4 and BPSG materials can be taken into account when the double ILD layer is used. The ILD layer has both excellent electrical insulation and stress relief characteristics.

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