Combined Capacitance and Temperature to Digital Converter

Master of Science Thesis

For the degree of Master of Science in Electrical Engineering at Delft University of Technology

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The undersigned hereby certify that they have read and recommend to the Faculty of Electrical Engineering Mathematics and Computer Science (EEMCS) for acceptance a thesis entitled
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by
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Abstract

This thesis describes the design and measurement of an IC which can digitize both capacitance and temperature. Capacitance sensing functionality is added to an existing Temperature to Digital Converter (TDC)−without adding significant die area. Two kinds of baseline capacitance compensation techniques have been investigated and their performance has been simulated at the system level. While adding capacitance sensing functionality to the TDC, the capacitive DAC and sigma-delta zoom ADC of the existing design have been reused. Dynamic element matching has been applied to ensure that mismatch in the capacitive DAC will not give rise to discontinuities between the sub-ranges of the ADC. Measurements show that the chip is functional and achieves the targeted capacitance-sensing resolution at a FOM of 1.87pJ/step.

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Chapter 1
Introduction

The goal of this thesis is to design a multi-sensor ADC (Analog to Digital Converter), where one sensor is a temperature sensor and the other one is a capacitive sensor. Before going into the main motivation behind this thesis, a brief explanation about the present day sensor interfaces will be given.

For every day-to-day use sensor interfaces, the transducer output, which depends on measurands like temperature, humidity and pressure, is converted into a digital form using an ADC. The major reason why the sensor data is processed in the digital domain instead of the analog domain, is that digital signals have stronger immunity towards noise than analog signals. Also digital signals can be post-processed, stored and transmitted easily.

1.1 Motivation

In many humidity and pressure sensors, temperature must also be measured so as to compensate for the cross sensitivity towards temperature changes. Also temperature is an important measurand in many applications. Instead of having two separate sensor ADCs, one measuring temperature and another measuring capacitance (humidity and pressure changes can be converted into capacitance change [8]), a single ADC is used for measuring both temperature and capacitance. One major advantage of using a single ADC here in this application is area reduction. Thus the main aim of this thesis is to design and test an IC which can digitize temperature and capacitance. The IC will work in two modes, one which can digitize capacitance, i.e., function like a CDC (Capacitance to Digital Converter), and the other which can digitize temperature, i.e., function like a TDC (Temperature to Digital Converter).

1.2 Summary of previous research

The ADC along with the sensor interfaced to it affects four key performance parameters. They are resolution, inaccuracy, power consumption and conversion time. Resolution is the smallest change in the input so as to get a detectable change in the output. Inaccuracy is the difference between the target value and the measured value (filtering out the noise of the system).

Nowadays lots of research and development has been done in order to improve the

resolution and accuracy; and minimize the power consumption and die area. Looking into the prior research, reference [4] describes about a capacitive pressure sensor IC, that is also able to digitize temperature. It was able to resolve capacitance changes of 300 ppm (in the capacitance range from 20-120pF), temperature changes to ±0.1°C, consumes 200μW of power and the die area is around 4mm^2. There are capacitance and temperature to digital converter ICs manufactured by Analog Devices (AD 7745, AD 7746, AD 7747). In the CDC mode, these ICs are able to attain a resolution of 2aF in 60ms conversion time and a current consumption of 0.7mA [2,3]. However, for both the above designs the operating temperature range is from -40°C to +125°C. In the chip designed for this thesis, the operating temperature range is wider, i.e., from -55°C to +125°C, and the die area of this chip is around 1.2mm^2.

Looking into the recent CDC designs, the one implemented in [6] consists of a ring oscillator powered by a charged capacitance and the number of clock cycles has a linear relationship with respect to the capacitance value. This design is very energy efficient. The CDC architecture implemented in [5] uses a principle of 2nd order Zoom ADC (Zoom ADC operating principle will be discussed in the next chapter), which is also a good choice for energy efficiency. The design implemented in [10] also uses Zoom ADC principle but the order is 3. This makes the conversion time smaller compared to that of [5].

In this thesis, the capacitance sensing functionality is added to an existing TDC design (designed by Kamran Souri, with operating temperature range -55°C to +125°C) and the die is made as small as possible. Table 1.1 shows the target specifications to be achieved in the CDC mode.

Table 1.1 : Target specifications in the CDC mode.

Specification	**Value**
Resolution	7.5 aF
Conversion time	20 ms
Current consumption	< 10μA
Capacitance range	0 – 1.8 pF
Die area	< 150000 μm^2
Vdd	1.5 V

1.3 Outline of this thesis

The TDC architecture uses BJT as a temperature sensing element. In the next chapter, a detailed overview on how temperature sensing and a ratiometric measurement can be

made will be discussed. An overview of the TDC design will also be given. This will be followed by a detailed theory on the CDC, explaining the capacitance sensing method and its interfacing.

In chapter 3, a noise analysis of the CDC will be presented, followed by system-level simulation on the two CDC architectures, which is done on the basis of noise performance, effect of leakage on integrators, and the need for Dynamic Element Matching (DEM).

In chapter 4, interfacing the capacitance and temperature sensing front ends to a common ADC will be discussed, and the problems/difficulties encountered while interfacing both will be discussed in detail.

In chapter 5, a list of measurements done on the CDC mode and their results regarding the functionality, resolution, supply dependency and an experimental result to check the effect of DEM will be discussed. At the end of this chapter these results will be compared with the state of the art designs.

In the final chapter, the thesis will be concluded by a list of major findings and suggestions for future work.

Chapter 2
System-level overview

In this chapter a detailed overview on the TDC architecture used in the Combined Capacitance and Temperature to Digital converter design will be given. After an overview of the architecture, the extension of the TDC with CDC functionality will be discussed in detail.

2.1 Temperature to digital converter architecture

The TDC architecture uses BJTs (Bipolar Junction Transistors) as the sensing element [1]. Before going into further details of the TDC architecture, an overview of how BJTs can be used as a temperature sensor and how a ratio-metric measurement (shown in Figure 2.2) can be performed using this temperature sensor will be discussed (based on [6]).

Due to the dependence of the base emitter voltage (V_{be}) on absolute temperature.

$$V_{be} = \frac{kT}{q} \ln\left(\frac{I_e}{I_s}\right) \tag{2.1}$$

A BJT can be used as a temperature sensor where I_e is the emitter current used for biasing the BJT, I_s is the saturation current, k is the Boltzmann constant and q is the charge of an electron. This V_{be} has a typical temperature coefficient of -2mV/K. Due to its negative temperature coefficient it is also known as Complementary to Absolute Temperature (CTAT).

This V_{be} is however sensitive to process spread on I_s. In order to avoid this problem the difference between V_{be}'s (ΔV_{be}) of two BJTs biased with different emitter currents is taken for temperature measurement. This ΔV_{be} has a positive temperature coefficient (around 0.1 – 0.25 mV/K) and is also known as Proportional to Absolute Temperature (PTAT). Given two BJTs whose emitter bias currents have a ratio of 1: p and whose emitter areas have ratio of r:1. Then ΔV_{be} between both the BJTs is given by:

$$\Delta V_{be} = \frac{kT}{q} \ln\left(\frac{pI_1}{I_s}\right) - \frac{kT}{q} \ln\left(\frac{I_1}{rI_s}\right) = \frac{kT}{q} \ln(pr) \tag{2.2}$$

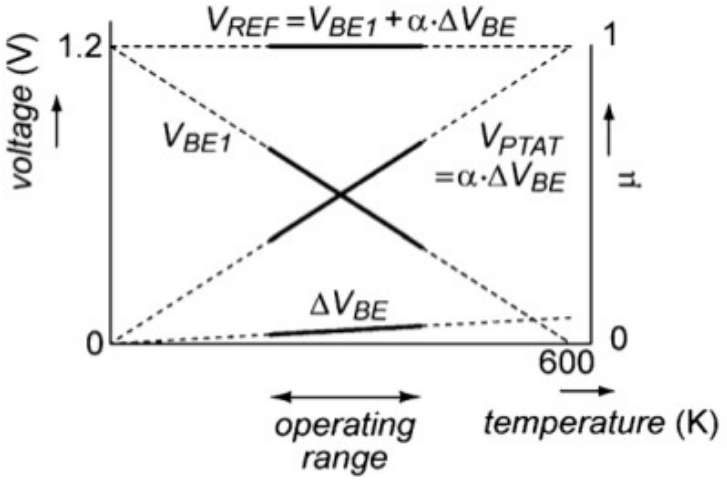


Figure 2.1: Relationship of V_{be}, ΔV_{be} and the reference voltage V_{REF} with respect to temperature [1]

The current sources used for biasing the BJTs, which generate V_{be} potentials are biased using a low power, self-biased chopped opamp and two auxiliary PNPs which will generate 90nA of bias current at (25 ºC). More details about the bias generating circuit are given in reference [1].

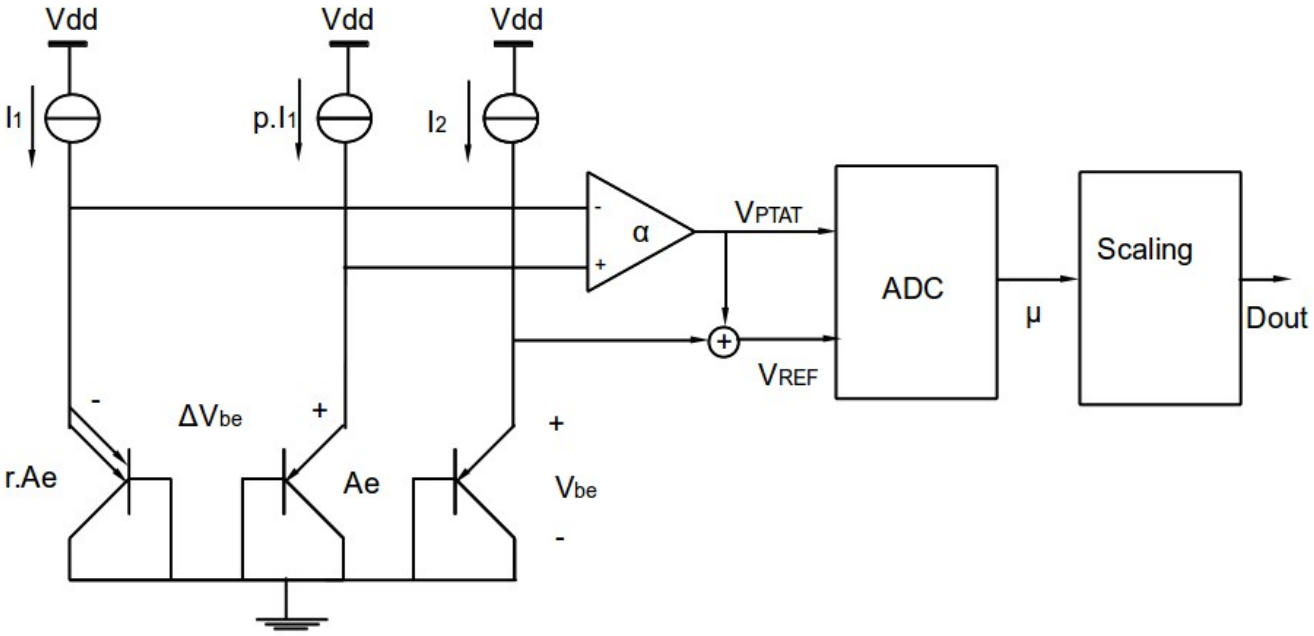


Figure 2.2 : Ratio-metric measurement using BJT temperature sensor [6]

Figure 2.2 shows how ΔV_{be} is digitized with respect to the temperature independent reference voltage V_{REF}. This kind of conversion is ratiometric in nature [2]. In figure 2.2, in order to generate a temperature independent reference, a linear combination of ΔV_{be} (PTAT) and V_{be} (CTAT) is used:

$$V_{REF} = V_{be} + \alpha \cdot \Delta V_{be} \tag{2.3}$$

Here α is chosen such that the sum of temperature coefficients are made zero and make V_{REF} temperature independent. This CTAT (V_{be}) is generated from a third BJT, biased using current source I_2.

$$V_{be} = \frac{kT}{q} \ln\left(\frac{I_2}{I_s}\right) \tag{2.4}$$

The ratio between V_{PTAT} and V_{REF} (i.e., μ) is digitized by an ADC.

$$\mu = \frac{V_{PTAT}}{V_{REF}} = \frac{\alpha \cdot \Delta V_{be}}{V_{be} + \alpha \cdot \Delta V_{be}} \tag{2.5}$$

μ has a linear relationship with respect to absolute temperature. This ratio μ is thus

converted to temperature in degrees Celsius using the relationship:

$$D_{out} = A \cdot \mu - B \tag{2.6}$$

with typical constants $A \approx 600$ and $B \approx 273$.

Certain non-idealities such as mismatches between the current sources biasing the BJTs, finite impedance of current sources, processing spreads and leakage current of MOS switches if connected to the BJTs, add to inaccuracy in temperature measurement. Various circuit techniques have been proposed in order to minimize the effects of these non- idealities [6].

In the TDC architecture, the ratio (X) of V_{be} and ΔV_{be} is digitized by the ADC [5], instead of μ. X has a non-linear relationship with respect to temperature. For the sake of flexibility μ, which has a linear relationship with respect to temperature, is calculated in the digital back-end using the relationship below :

$$\mu = \frac{\alpha}{\alpha + X} \tag{2.7}$$

The ADC, used for digitizing X, is a 2nd order zoom ADC. A zoom ADC is a two-step coarse-fine ADC whose coarse conversion is done by a SAR ADC and fine conversion is done by a sigma-delta modulator. During the coarse conversion, the SAR ADC approximates the ratio X (as shown in figure 2.3(a)). This is followed by a guard band step in which X is compared with $n+0.5$ (where n is the coarse conversion result). Based on the comparison result after the guard band step, the references for the 2nd order sigma-delta will be set, i.e, if $X > (n+0.5)$, the references for sigma-delta are $n \cdot \Delta V_{be}$ and $(n+2) \cdot \Delta V_{be}$. Otherwise the references are $(n-1) \cdot \Delta V_{be}$ and $(n+1) \cdot \Delta V_{be}$ as shown in figure 2.3(b). The advantage of using a zoom ADC is its improved quantization noise performance compared to regular sigma-delta modulator due to its smaller swing to the input of the sigma-delta modulator and smaller references used during the fine sigma-delta conversion.

Figure 2.4 shows the block diagram of 2nd order sigma-delta modulator. The sigma-delta modulator is an incremental sigma-delta modulator. An incremental sigma-delta modulator is quite different from a conventional sigma-delta modulator. It is mainly used in measurement and instrumentation application. In an incremental sigma-delta, the offset and gain errors are minimized compared to the conventional sigma-delta. They digitize signals close to DC frequency level. The decimation filters used for these kinds of sigma-delta modulators can be implemented using simple counter structures [12]. They can be set to the reset state after a conversion. And their conversion time depends on the frequency and number of clock cycles of the sampling clock based on the relation [7]:

$$t_{conv} = \frac{f_{clock}}{N} \tag{2.8}$$

where N is the number of clock cycles and f_{clock} is the sampling clock frequency.

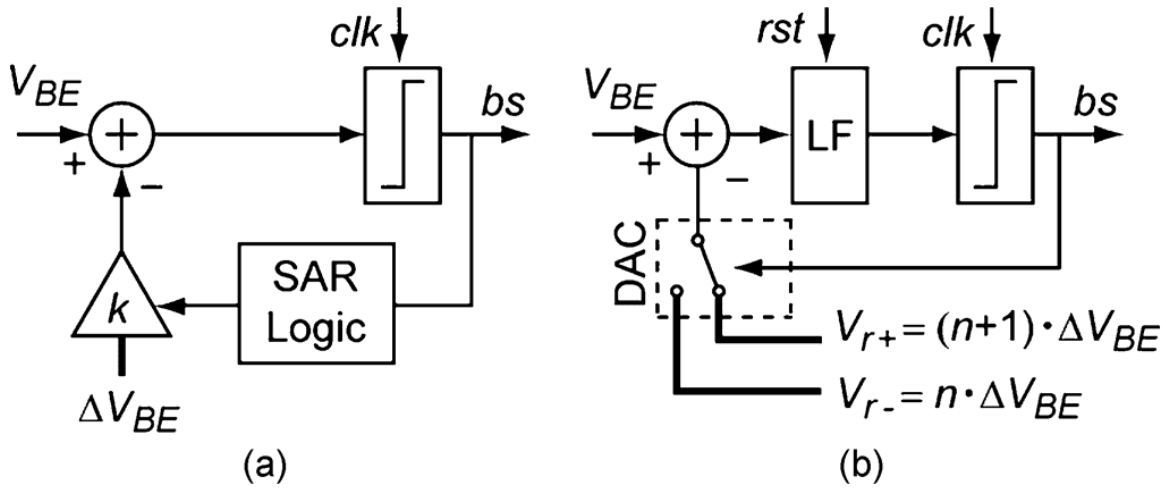


Figure 2.3:Block diagram of ADC during (a) coarse conversion (b) fine conversion [1]

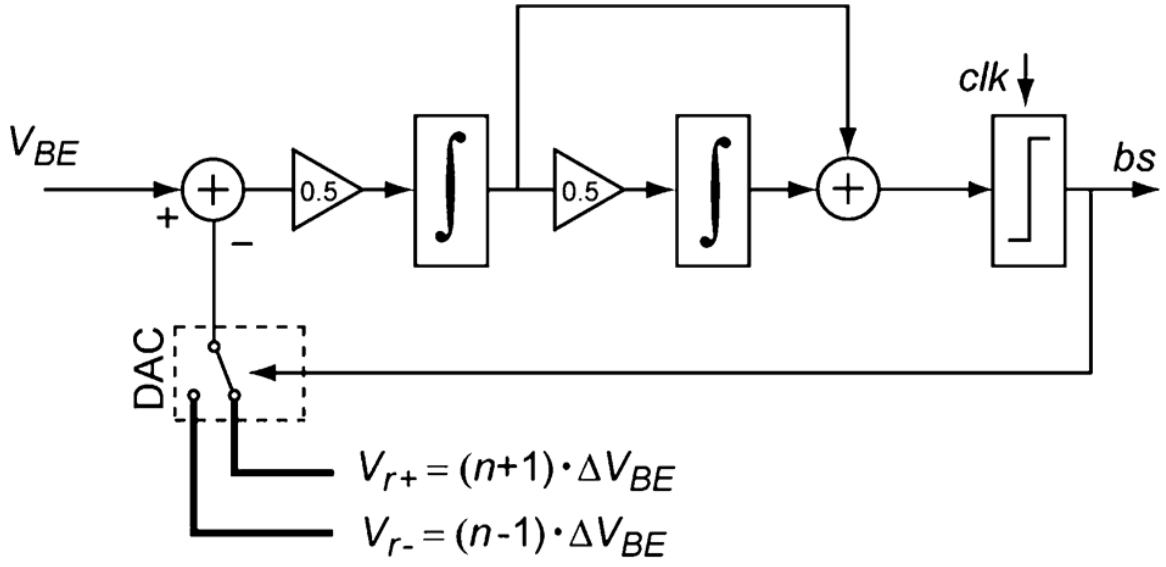


Figure 2.4:Block diagram of 2nd order sigma-delta ADC [1]

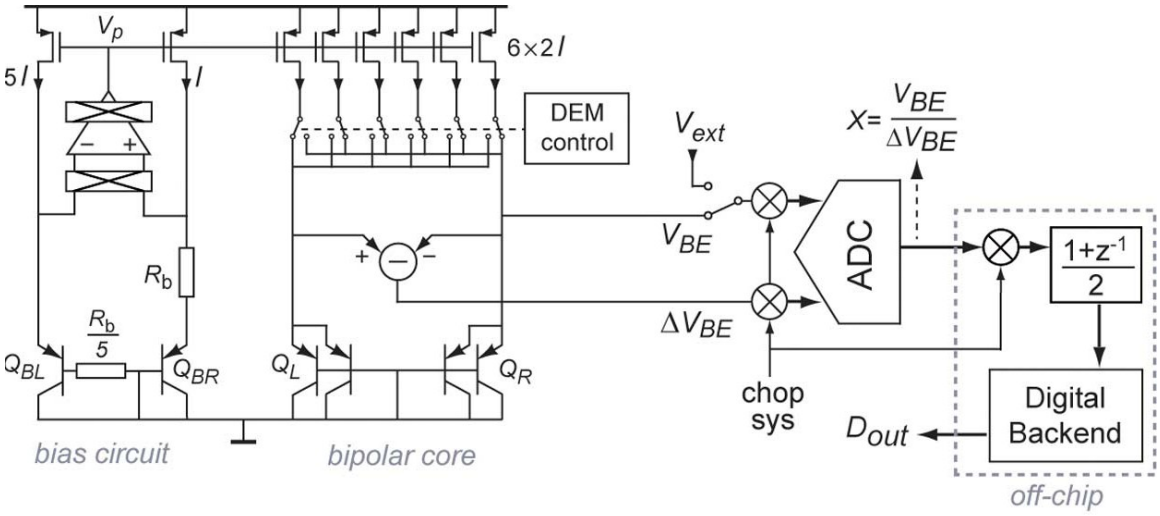


Figure 2.5: Block diagram of the temperature sensor [1]

Figure 2.5 shows the overall block diagram of the TDC design. The current sources used for biasing the bipolar core are changed in their positions (based on a DEM algorithm) for every clock cycle to minimize inaccuracy due to the mismatches between the current sources. Figure 2.6 shows the schematic of the Zoom ADC used in the existing TDC design. Capacitors C_{s1} to C_{s29} (each of value 128fF) are the unit capacitors of a capDAC and C_g (which is half the unit capacitor size) is used during the guard band step. A telescopic OTA (Operational Transconductance Amplifier) architecture with a DC gain of 76 dB is used in the 1st integrator and an inverter-based OTA with a DC gain of 44 dB is used in the 2nd integrator. Delayed clocks are used for bottom-plate sampling. System-level chopping is used in order to minimize the effect of offset caused by the ADC. See reference [1] for more details about the design.

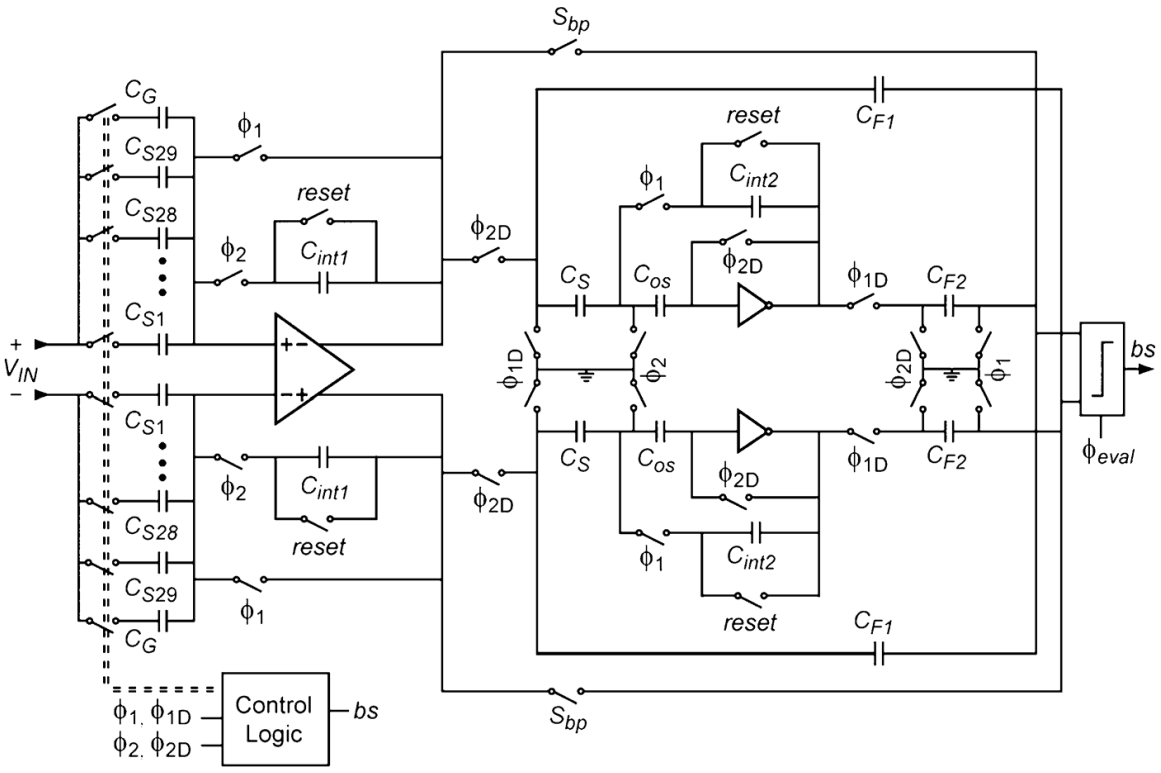


Figure 2.6: Schematic of 2nd order Zoom ADC used in the existing TDC design[1]

2-3 Capacitance to digital converter

In this part of the chapter, the focus is on the sigma-delta modulator for capacitive sensor interfaces. Before going into the details, a brief review about the working of capacitive sensors will be given.

2.3-1 Capacitive sensors

Capacitance across two parallel plates is given by:

$$C = \frac{\varepsilon \cdot A}{d} \tag{2.9}$$

Capacitance is dependent on ε (dielectric constant of the material or medium across the plates), A (area of the plates) and d (distance between the plates). It becomes a capacitive sensor if any one of the parameters (ε, A or d) are changed based on the measurand [8].

The mean of highest and lowest capacitance value of the sensor, which the interface can

take is called its baseline capacitance. In the upcoming sections, the major reason behind baseline capacitance compensation for sigma-delta modulator based CDCs will be explained.

2.3-2 Sigma-delta modulator based CDC

In many capacitive-sensor interfaces, measuring capacitance is done by measuring charge in the sensor when excited by a reference voltage source. In this thesis, the reference voltage source is a square wave and the interface uses a switched capacitor based sigma-delta architecture, for good energy efficiency.

Before getting into sigma-delta modulator based capacitance sensor interfaces, an example switched capacitor sensor interface (switched capacitor integrator) will be explained briefly. In a switched capacitor interface, at phase Φ_1 (or the sampling phase) the capacitor C_x is charged using a reference voltage source (it can be the supply V_{dd}) and in phase Φ_2 (integration phase), the charge is pushed into the integrating capacitor (or the feedback capacitor C_{int}), as shown in figure 2.4. During the sampling phase, the virtual node of the OTA is at common mode or ground potential, and during the integration phase its DC biasing point will be changed momentarily, which will be compensated by the feedback current through the integrating capacitor. A point to note here, is that Φ_1 and Φ_2 are non-overlapping clocks (shown in figure 2.4).

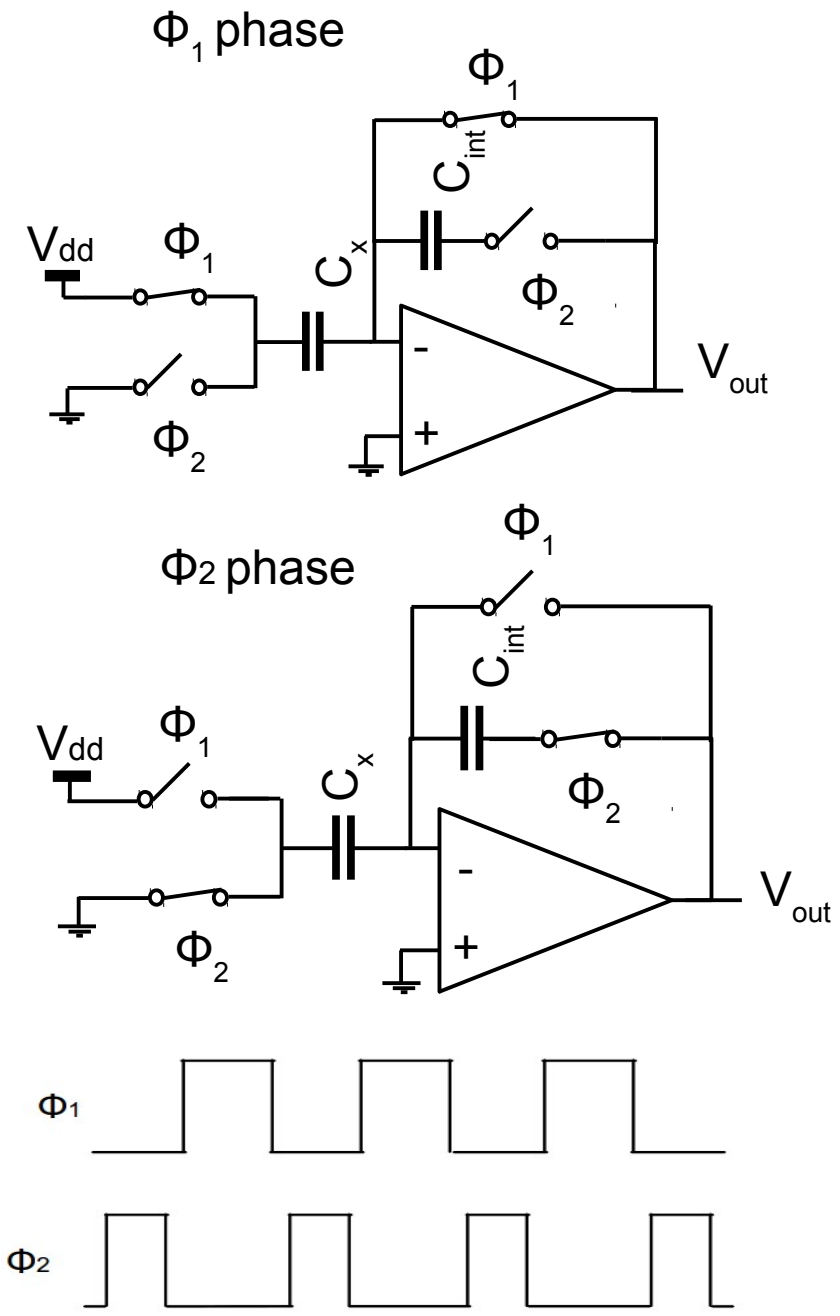


Figure 2.4: Switched capacitor integrator interface.

In a sigma-delta CDC interface, the reference charge is subtracted from the signal charge (that is the charge from the sensor capacitor). The value of this reference charge is

decided based on the bitstream *bs* (comparator decision). Figure 2.5 shows an example of a sigma-delta CDC. When *bs* = 1, then $V_{dd}\cdot(C_x-C_{ref1})$ error charge is sent to the integrating capacitor and when *bs* = 0, then $V_{dd}\cdot(C_x-C_{ref2})$ error charge is sent to the first integrator. This is very similar to the operation of a conventional sigma-delta ADC, but here the input and references are thought in terms of charges from the sensor and reference capacitors respectively.

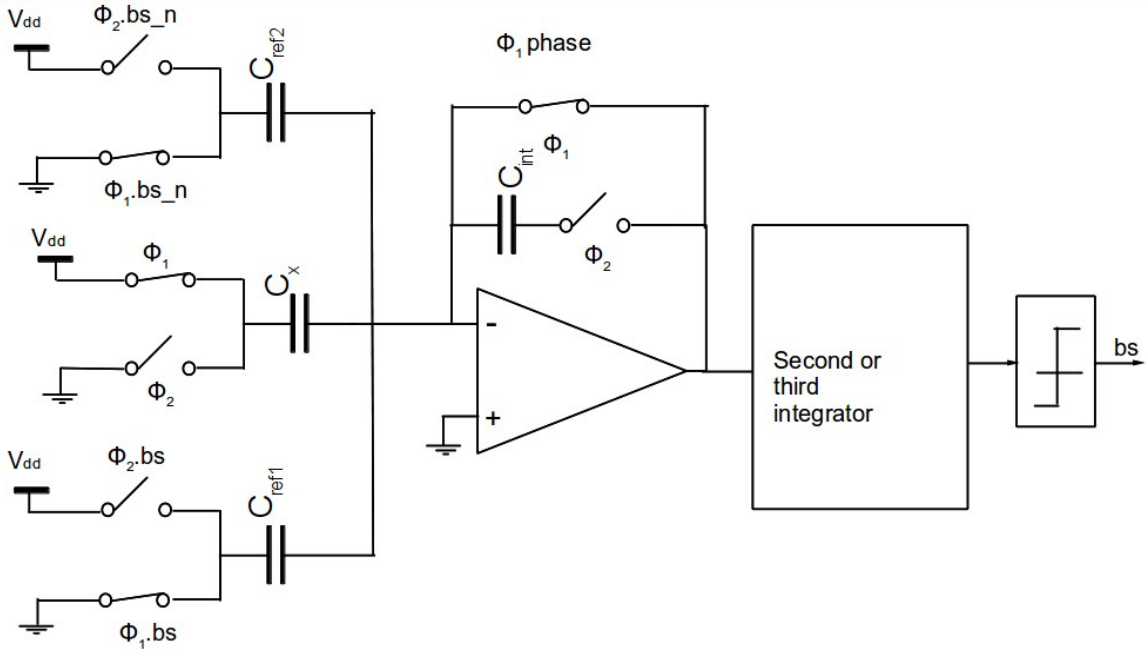


Figure 2.5 : An example of sigma-delta capacitance to digital converter.

2.3-3 Baseline capacitance compensation

Given a capacitive sensor, which has a large baseline capacitance ($C_{baseline}$) and the sensor capacitance varies ΔC_x around the baseline value. The value of reference capacitor should be at-least 1.33 times ($C_{baseline} + \Delta C_x/2$) for a stable 2nd order sigma-delta operation [8]. This will lead to larger error charge being dumped into the integrating capacitor leading to larger swing at the 1st integrator output, which creates clipping and slewing problem at the OTA output and increases in quantization noise. By means of baseline capacitance compensation, the value of the reference capacitance can be made smaller which leads to reduction in the error charge input to the integrating capacitor. To implement this baseline capacitance compensation has to be implemented, an additional capacitance equal to the $C_{baseline}$ value has to be switched in the opposite phase of the sensor capacitance (as shown in figure 2.6).

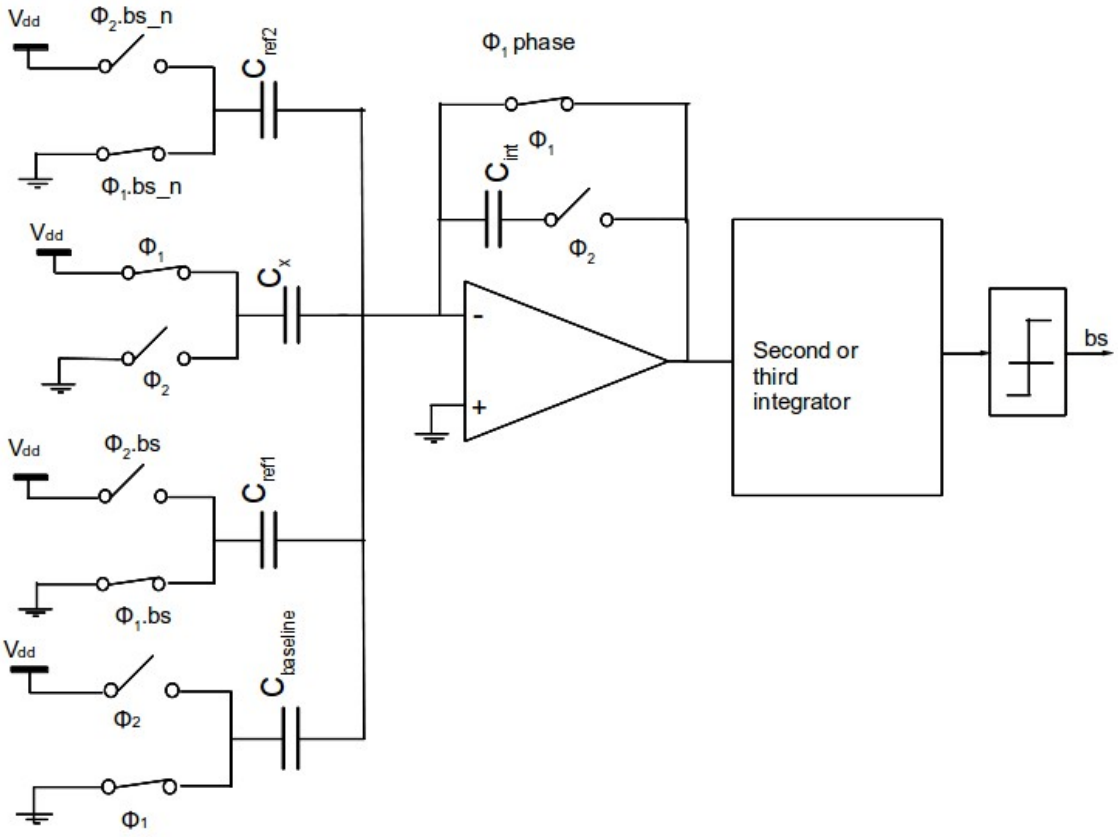


Figure 2.6 : Example of sigma-delta capacitance to digital converter with baseline capacitance compensation included.

2.3-4 Decimated value calculation

Since a sigma-delta CDCs work on the principle of charge balancing, the average charge fed into the 1st integrator of a sigma-delta approaches zero after a large number of clock cycles. The calculation of the decimated is value very similar to that of reference [8].

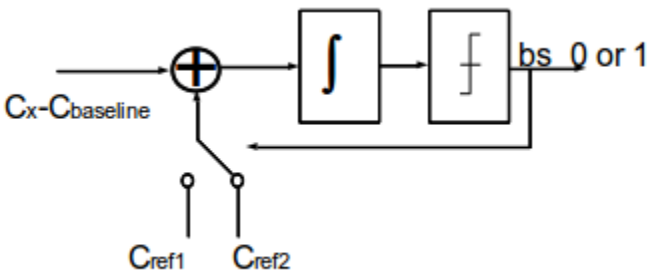


Figure 2.8 : Functional diagram of a sigma-delta CDC.

If bs = 0, C_{ref1} capacitor is chosen. And if bs = 1, C_{ref2} capacitor is chosen (as shown in figure 2.8) .

If the bitstream has given out 'm' number of 1's and 'n' number of 0's by the end of N clock cycles (N = m+n) , the average value $\mu = \frac{m}{(m+n)}$

Applying the principle of charge balancing:

$$\left(\frac{m}{m+n}\right)\cdot V_{dd}\cdot\left(C_x - C_{baseline} - C_{ref1}\right) + \left(\frac{n}{m+n}\right)\cdot V_{dd}\cdot\left(C_x - C_{baseline} - C_{ref2}\right) = 0 \qquad (2.10)$$

$$\mu\cdot\left(C_x - C_{baseline} - C_{ref1}\right) + \left(1-\mu\right)\cdot\left(C_x - C_{baseline} - C_{ref2}\right) = 0 \qquad (2.11)$$

$$C_x - C_{baseline} - C_{ref2} - \mu\cdot\left(C_{ref1} - C_{ref2}\right) = 0 \qquad (2.12)$$

Therefore, the average value is equal to :

$$\mu = \frac{C_x - C_{baseline} - C_{ref2}}{C_{ref1} - C_{ref2}} \qquad (2.13)$$

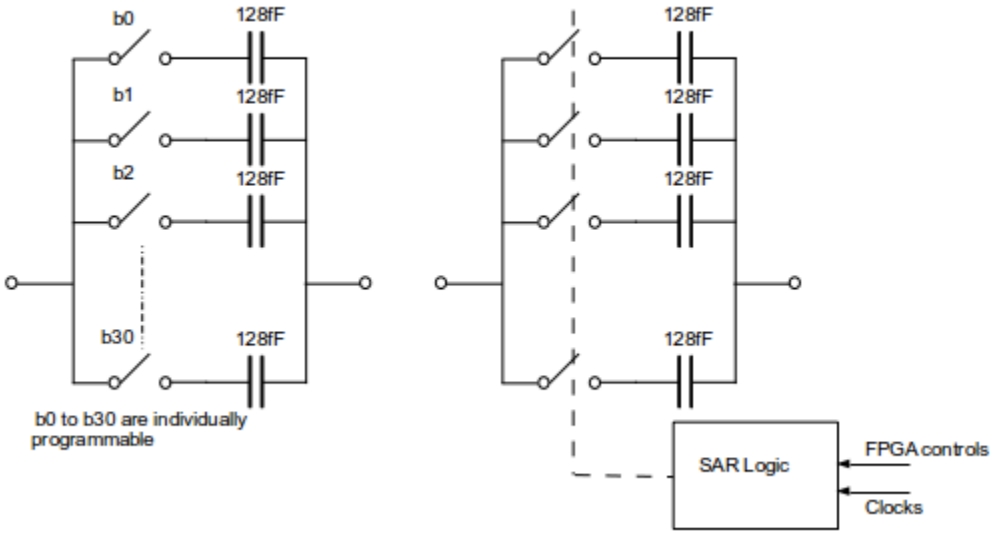
However the above relationship is an approximation because of the thermal noise added at the input of the sigma-delta, the switching of capacitors and the OTA of 1st integrator is not taken into account. This will be discussed further in the next chapter.

Chapter 3
System-level design

In this chapter, the aspects taken for system level design and system level simulation results will be discussed. First the baseline capacitance compensation techniques to be implemented will be discussed, followed by the noise analysis of a sigma-delta CDC. Three system-level simulations have been done and their results will be shown. The first two simulations are based on noise performance of the baseline capacitance compensation techniques and effects of integrator leakage. And the third one is about the need for Dynamic Element Matching (DEM).

3.1. Baseline capacitance compensation using trimming and using successive approximation

In this thesis, since the capDAC and the sigma-delta will be reused, the capDAC in the TDC will be used for programming the baseline capacitance. The baseline capacitance can be programmed in two ways: by trimming, where the selection bits of the capDAC are set to a fixed value (Trim CDC) or by programming the selection bits using a successive approximation algorithm (Zooming or Zoom CDC), as shown in figure 3.1.



(a) *(b)*

Figure 3.1: Baseline capacitance compensation in (a) Trim CDC case (b) Zoom CDC case

The operation of a Zoom CDC is very similar to that of a Zoom ADC, except that the input and references are both capacitances. During the coarse conversion phase, the SAR algorithm approximates ratio $n = C_x/C_u$ where C_u is the unit capacitor of the capDAC. And if the references are kept such that $\frac{C_x - C_{baseline}}{C_{ref}} \leq \pm 0.75$ (based on reference [7]), then this would reduce the input error charge into the 1st integrator during sigma-delta operation (fine conversion phase) which leads to improved performance in quantization noise. There will also be a guard band step similar to Zoom ADC case, which sets the references for fine conversion by comparing the actual ratio of C_x/C_u with $n+0.5$ (where n is the coarse conversion value), i.e., if the actual ratio is greater than $(n+0.5).C_u$ then the references for $bs = 0$ and $bs = 1$ are $n \cdot C_u$ and $(n+2) \cdot C_u$ respectively. Otherwise the references are $(n-1) \cdot C_u$ and $(n+1) \cdot C_u$. In the Zoom CDC case, the whole input range is divided into smaller sub-ranges by the coarse conversion and the fine sigma-delta CDC modulator will do the conversion of those sub-ranges. This unlike the Trim CDC case where the sigma-delta CDC modulator will digitize the whole input range.

The noise performance of both Zoom and Trim CDC will be discussed in the upcoming sections. It will be shown by system level simulations that a Zoom CDC has better

quantization noise performance than a trim CDC but the thermal noise performance for both the cases is nearly the same.

3.2. Noise analysis

Before moving to the architecture level simulation results, both quantization and thermal noise in a sigma-delta CDC will be discussed briefly. Also a derivation of the standard deviation in the decimated value due to thermal noise will be discussed.

Quantization Noise
When there is no thermal noise present in the ADC, the difference between the input and the output value of an ADC is the quantization error. For lower resolution (or the number of bits) the quantization error is pretty deterministic in nature and as the resolution is increased, then the quantization error becomes random in nature for a sufficiently busy input signal (referred to as quantization noise). The quantization noise power is $\frac{q^2}{12}$ (where q is the LSB step size of the ADC).

For an incremental sigma-delta modulator, since the input signal is at DC frequencies, maximum quantization error for the whole range of input capacitances is taken as measure. And this maximum quantization error will be taken into consideration for the system-level simulations.

Thermal Noise
In this thesis, since a square wave excited switched capacitor based sigma-delta CDC is implemented, the dominant thermal noise sources are the switches, connected to the sensor and baseline capacitors, and the input referred thermal noise of the 1st integrator. The noise sources after the output of the 1st integrator are ignored, since they will get shaped up and pushed to higher frequencies during the sigma-delta operation.

The thermal noise calculation is very similar to that reported in [8], but the only difference is that the thermal noise due to the switches of the baseline capacitance was not considered in [8].

Consider a sigma-delta CDC in which C_{ref1} is chosen as reference when the bit-stream $bs = 1$ and C_{ref2} is chosen as reference when $bs = 0$.
Then the input charge to the 1st integrator is

$$V_{dd}\left(C_x - C_{ref1} - C_{baseline}\right) \text{ when } bs=1 \text{ or } V_{dd}\left(C_x + C_{ref2} - C_{baseline}\right) \text{ when } bs=0$$

As per the principle of charge balancing, after N clock cycles the average accumulated charge at the input of the 1st integrator is:

$$Q_{acc} = Q_{ref1} + Q_{ref2} + Q_{noise} + Q_{signal} = 0 \tag{3.1}$$

where
Q_{ref1} is the charge accumulated due to switching of C_{ref1} when $bs = 1$.
Q_{ref2} is the charge accumulated due to switching of C_{ref2} when $bs = 0$.
Q_{noise} is the noise charge dumped due to thermal noise.
Q_{signal} is the average charge accumulated due to the switching of the sensor and baseline capacitors.

The total noise charge variance is

$$\overline{Q_{noise}^2} = \overline{Q_{n,ref1}^2} + \overline{Q_{n,ref2}^2} + \overline{Q_{n,sensor}^2} + \overline{Q_{n,baseline}^2} \tag{3.2}$$

$Q_{n,ref1}$ and $Q_{n,ref2}$ are noise charges dumped when $bs = 0$ and $bs = 1$ respectively.
$Q_{n,sensor}$ is the noise charge dumped due to switching of the sensor capacitor.
$Q_{n,baseline}$ is the noise charge dumped due to switching of the baseline capacitor.

One point to note here is that since the thermal noise due to the baseline and sensor capacitance are uncorrelated, so the squares of the noise charges can be added directly. Another point to note is that irrespective of whether the reference charge is added or subtracted from the charge of the sensor capacitor, $Q_{n,ref1}$ and $Q_{n,ref2}$ are uncorrelated and their squared noise voltages can also be added directly.

$$\overline{Q_{n,ref1}^2} = kT\mu N \xi C_{ref1} \tag{3.3}$$

$$\overline{Q_{n,ref2}^2} = kT(1-\mu) N \xi C_{ref2} \tag{3.3}$$

$$\overline{Q_{n,sensor}^2} = kT N \xi C_{sensor} \tag{3.4}$$

$$\overline{Q_{baseline}^2} = kT N \xi C_{baseline} \tag{3.5}$$

where $\xi = \dfrac{\frac{7}{3} + 2x}{1 + x}$ and $x = 2 g_m R_{on}$ where g_m is the transconductance of the 1st integrator OTA and R_{on} is the on resistance of the switches connected to the

capacitors. Settling errors and errors due to finite loop gain are assumed to be negligible while deriving ξ [9].

Therefore,

$$\overline{Q_{noise}^2} = kT\,N\,\xi\,[C_{sensor} + C_{baseline} + (C_{ref1} - C_{ref2})\,\mu + C_{ref2}] \tag{3.6}$$

Evaluating (3.1) and (3.6) ,

$$Q_{ref1} + Q_{ref2} + Q_{signal} = -Q_{noise} \tag{3.7}$$

$$V_{dd}\,\mu\,N\,(C_x - C_{off} - C_{ref1}) + V_{dd}\,(1-\mu)\,N\,(C_x - C_{off} + C_{ref2}) = -Q_{noise} \tag{3.8}$$

$$C_x - C_{off} + C_{ref2} - \mu\,(C_{ref1} + C_{ref2}) = \frac{-Q_{noise}}{V_{dd} * N} \tag{3.9}$$

Therefore the decimated value is

$$\mu = \frac{(C_x - C_{off} + C_{ref2})}{(C_{ref1} + C_{ref2})} + \frac{Q_{noise}}{V_{dd}\,N\,(C_{ref1} + C_{ref2})} \tag{4.0}$$

Last chapter, while deriving μ, the noise component was assumed to be zero in equation (2.11) but here the noise component is visible.

And the noise component in the decimated value is

$$\sigma_\mu = \frac{\sqrt{kT\,N\,\xi\,[C_{sensor} + C_{baseline} + (C_{ref1} - C_{ref2})\,\mu + C_{ref2}]}}{V_{dd}\,N\,(C_{ref1} + C_{ref2})} \tag{4.1}$$

3.3 Noise performance of Trim and Zoom CDC

The sigma-delta modulator used in the TDC design is also taken as the modulator for the CDC. In this section, the comparison of noise performance between a Trim and a Zoom CDC will be discussed. The input capacitance is swept from 1.2pF to 1.8pF and the baseline capacitance is assumed to be equal to 1.5pF for the Trim CDC case.

Equation (4.1), derived in the previous section, is used for evaluating the thermal noise performance (for system level simulations) of both Zoom and Trim CDC cases. The highest values of the sensor and baseline capacitance (which is determined by the SAR

logic) are used in thermal noise performance of the Zoom case. But for the trim CDC case, the baseline capacitance of 1.5 pF will be used.

The input referred thermal noise and quantization noise vs the number of clock cycles N is plotted in figure 3.2.

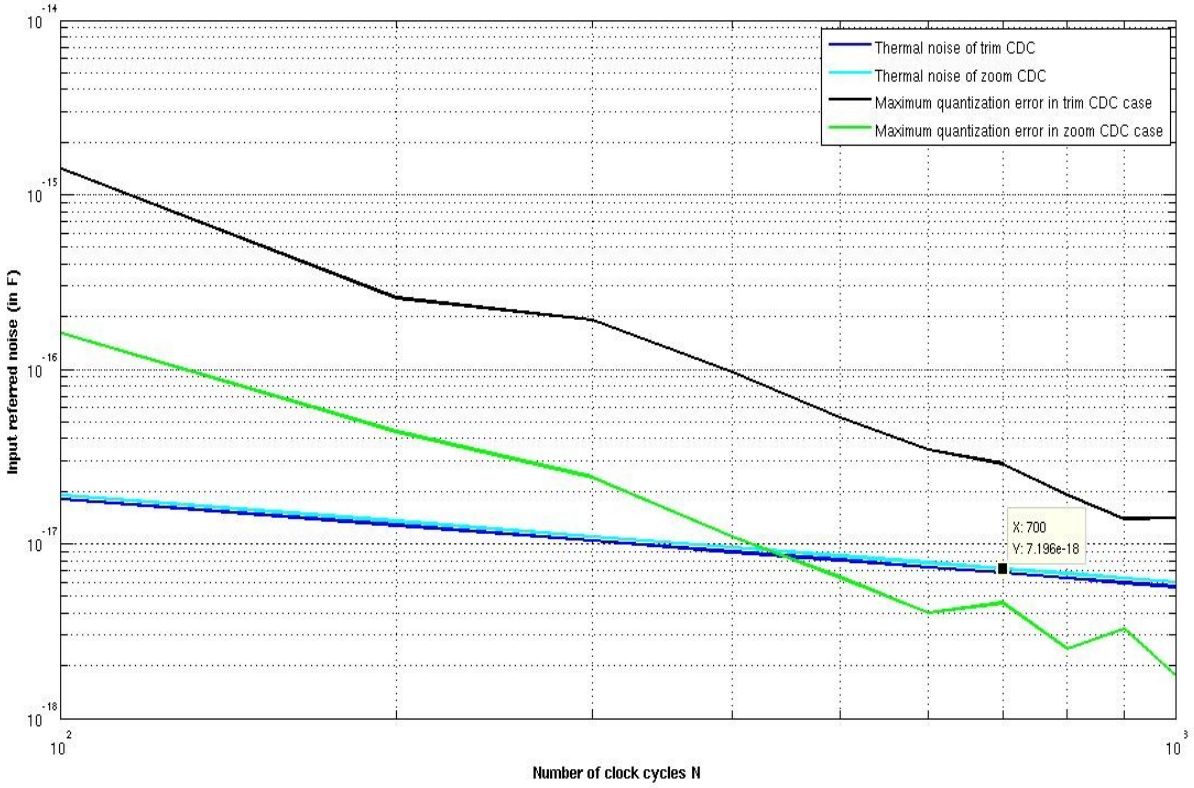


Figure 3.2: Noise performance of both the cases of CDC.

As it can be observed in figure 3.2, for a given number of clock cycles, the quantization noise performance of the Zoom CDC is around 10 times lower than that of Trim CDC. After 400 clock cycles, in the Zoom CDC case, the noise floor is dominated by thermal noise and the required resolution (7.5aF) is achieved at 700 clock cycles. It can be concluded from this system level simulation that the capDAC with Cu = 128 fF is enough to make the required resolution limited by thermal noise.

Another point to be observed based on the above system level simulation, the Zoom CDC does not give much improvement in the thermal noise performance.

3.3. Effects of leakage in 1st and 2nd integrator

In a real integrator, finite gain of the OTA, will lead to charge leakage at the integrating capacitor. This leakage causes limit cycles in the output bit-stream [6]. This leads to the same output value for a range of input values (i.e, dead zones). These dead zones add to non-linearity and degrade the ENOB of a sigma-delta[6].

The products of the gains of the 1st and 2nd integrator must be chosen such that these errors are well below the thermal noise. In this design, since the sigma-delta used in the TDC architecture will be re-used for the CDC also, the gains of the OTA used in 1st and 2nd integrator are 76 dB and 44 dB respectively. It is proved in the system level simulations (as per the plot in figure 3.3) that this is enough to make the noise floor dominated by thermal noise (within 700 clock cycles).

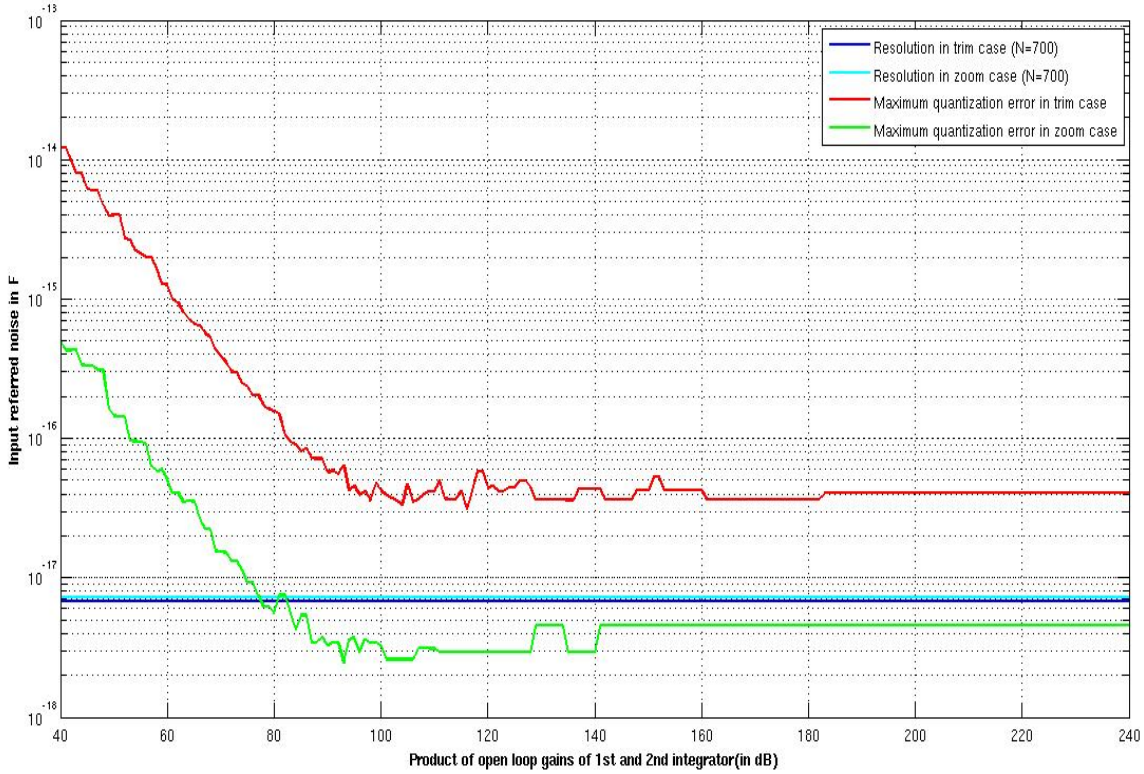


Figure 3.3:Noise performance of CDC for different open loop gain products.

3.4. Dynamic element matching

The capDAC unit capacitors will be subject to mismatch errors caused by fabrication tolerances. These errors in the unit capacitors of the capDAC will lead to discontinuities between the sub-ranges in the Zoom operation (shown in figure 3.4). In order to minimize these discontinuity errors, Dynamic Element Matching (DEM) is used. In this simulation DEM algorithm in reference [7] is used.

During each DEM cycle, the positions of the caps are changed as per a pattern. The error charges in all the DEM cycles are averaged out, which is done by the loop filter of the sigma-delta modulator. This will reduce the discontinuity from one sub-range to another. If the DEM cycles are in-complete, .i.e., not all the capacitors in the capDAC are equally used in the whole conversion cycle. Then this leads to a residual error in the INL. However the overall effect of this is not as impactful compared to the INL without DEM (as shown in figure 3.4).

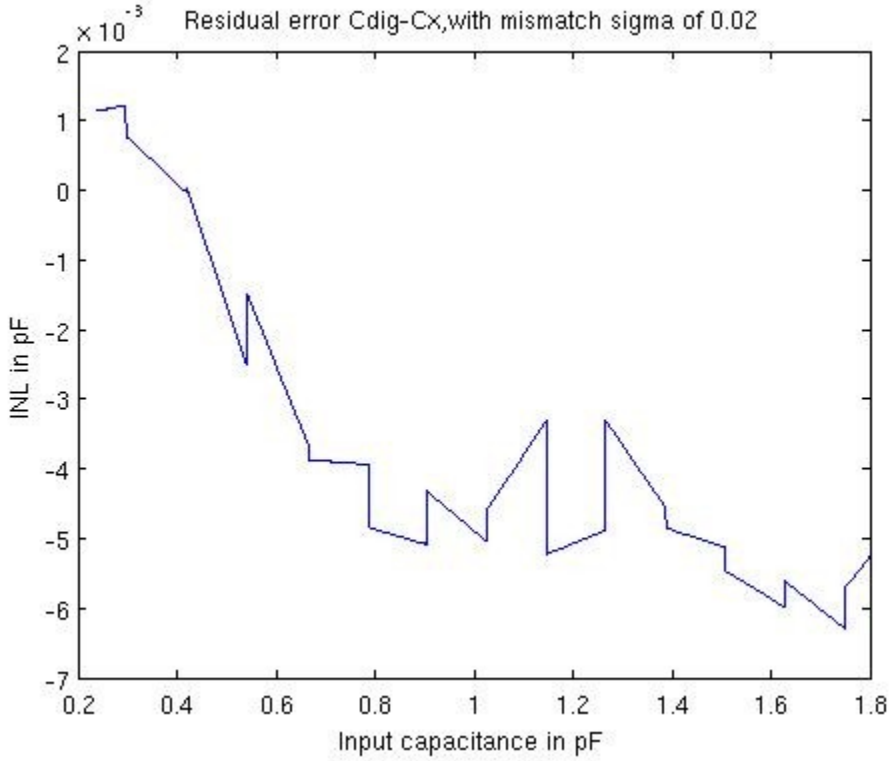


Figure 3.4 : INL of Zoom CDC without DEM.

As it can be observed that there are discontinuities at every step of a sub-range and which

gives rise to large values in the INL. But with DEM operation,these errors are minimized by a factor of 10^{-3} fF (as shown in figure 3.5).

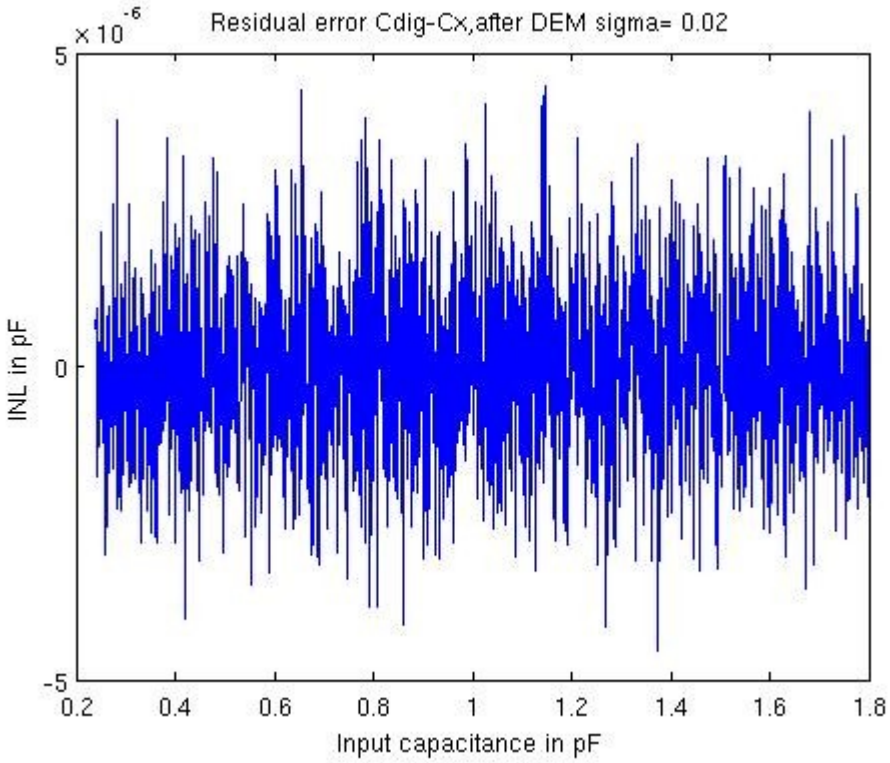


Figure 3.5: INL of Zoom CDC with DEM.

Chapter 4
Transistor-level design

In the 2nd chapter, an overview of the TDC architecture used in this design was given. In this chapter, more details on the TDC especially the Front-end interfacing of the Bipolar temperature core with the Zoom ADC will be discussed in detail. This is followed by the capacitance sensor interfacing and then the combined interfacing of both sensors to the Zoom ADC.

4.1. TDC architecture in detail

Figure 4.1 shows the interfacing of the Bipolar core with the OTA of the 1st integrator. Variable *K* is the number of sampling capacitors chosen from the capDAC. During phase Φ_1 (the sampling phase), the OTA is kept in unity gain feedback mode. During phase Φ_2 (the integration phase), the charge in the sampling capacitor (accumulated during Φ_1) is pushed into the feedback capacitor and the OTA is also made into an inverting amplifier. It is also shown in the figure, that the maximum peak to peak swing is 100mV[1].

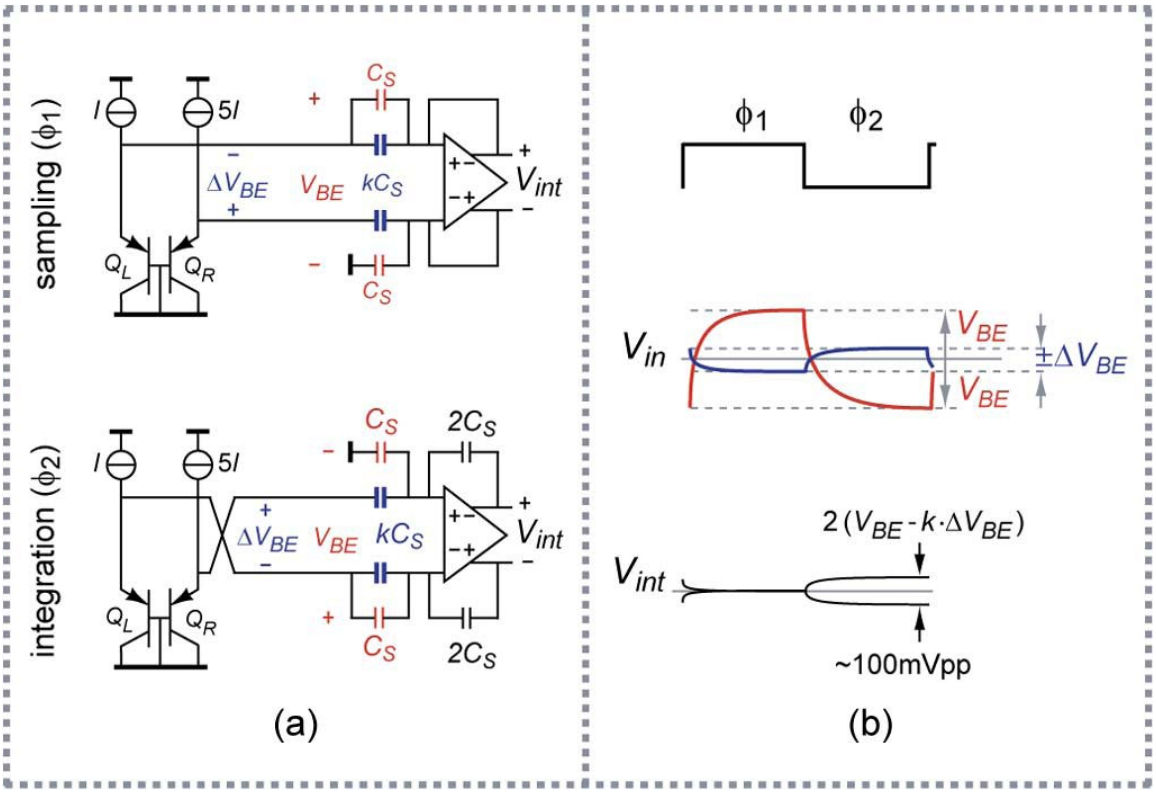


Figure 4.1:Integration proposed in the existing TDC design[1]

Figure 4.2 shows the simplified schematic of the TDC. It is shown in figure 4.2, that each element of the capDAC used in the TDC design consists of three switches connected to an unit capacitor. One switch for sampling V_{be} (CsB), the second one for sampling ΔV_{be} (CsA) and the third one (CsX) is connected to a dummy BJT (Q-dummy). The reason for having the latter is for reducing the settling time when sampling the V_{be} voltage of any BJT in the bipolar core again.

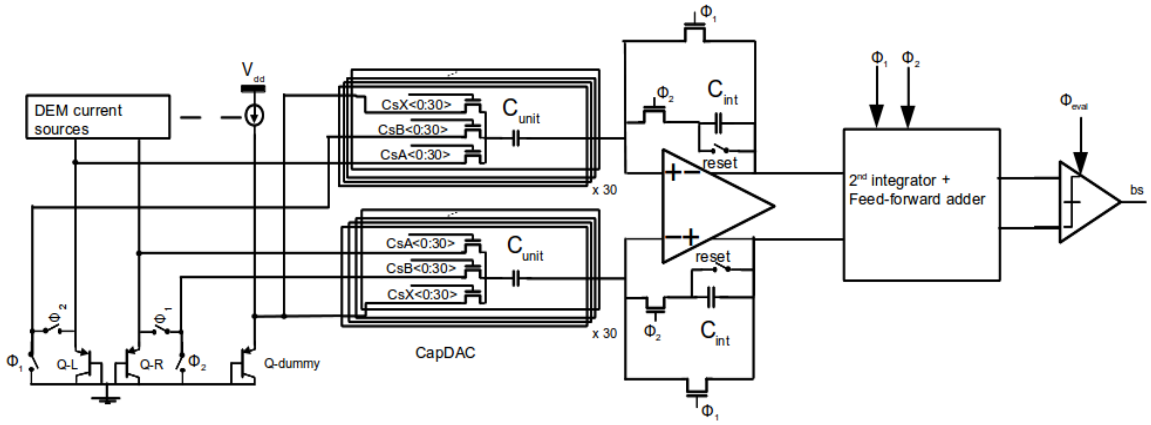


Figure 4.2 : Simplified schematic of the existing TDC design.[1]

In section 4.3, addition of the capacitance sensing functionality to the schematic in figure 4.2 will be shown and discussed. Before going to section 4.3, a proposed integration scheme for CDC operation will be shown in the next section.

4.2 Integration scheme for CDC operation

In this thesis, since the Zoom ADC will be reused for CDC operation, the capDAC will be used for programming the baseline capacitance during the coarse (or SAR) operation and setting the reference capacitances for the fine sigma-delta conversion.

Figure 4.3 shows the interfacing of the capacitive sensor and the capDAC with the OTA. During phase Φ_1, the OTA is in unity-gain feedback configuration; the sensor capacitance is charged to V_{dd} supply at one virtual ground and the baseline or reference capacitance ($K.C_s$), depending upon the SAR or sigma-delta conversion phase respectively, is charged to V_{dd} supply at the other virtual ground. During Φ_2 or integrating phase, the OTA is kept in inverting amplifier configuration and the charge sampled during Φ_1 is pushed into the integrating capacitor. In this switching scheme, since the sensor and baseline capacitor are switched between V_{dd} supply and gnd, this will increase the SNR of the CDC compared to the scheme where the capacitors are charged from gnd to common mode voltage and from common mode voltage to V_{dd} [7].

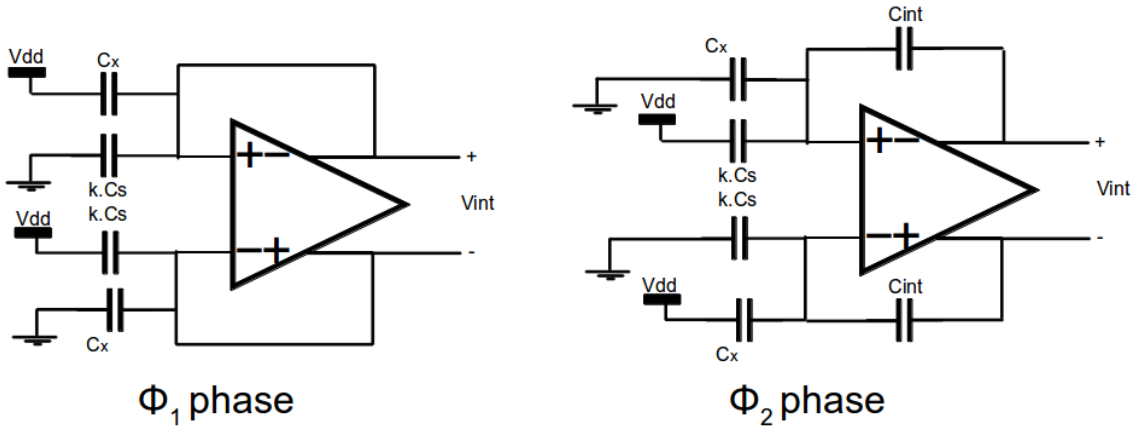


Figure 4.3: Proposed integration scheme for CDC.

4.3 Interfacing of temperature and capacitive sensor to a common ADC

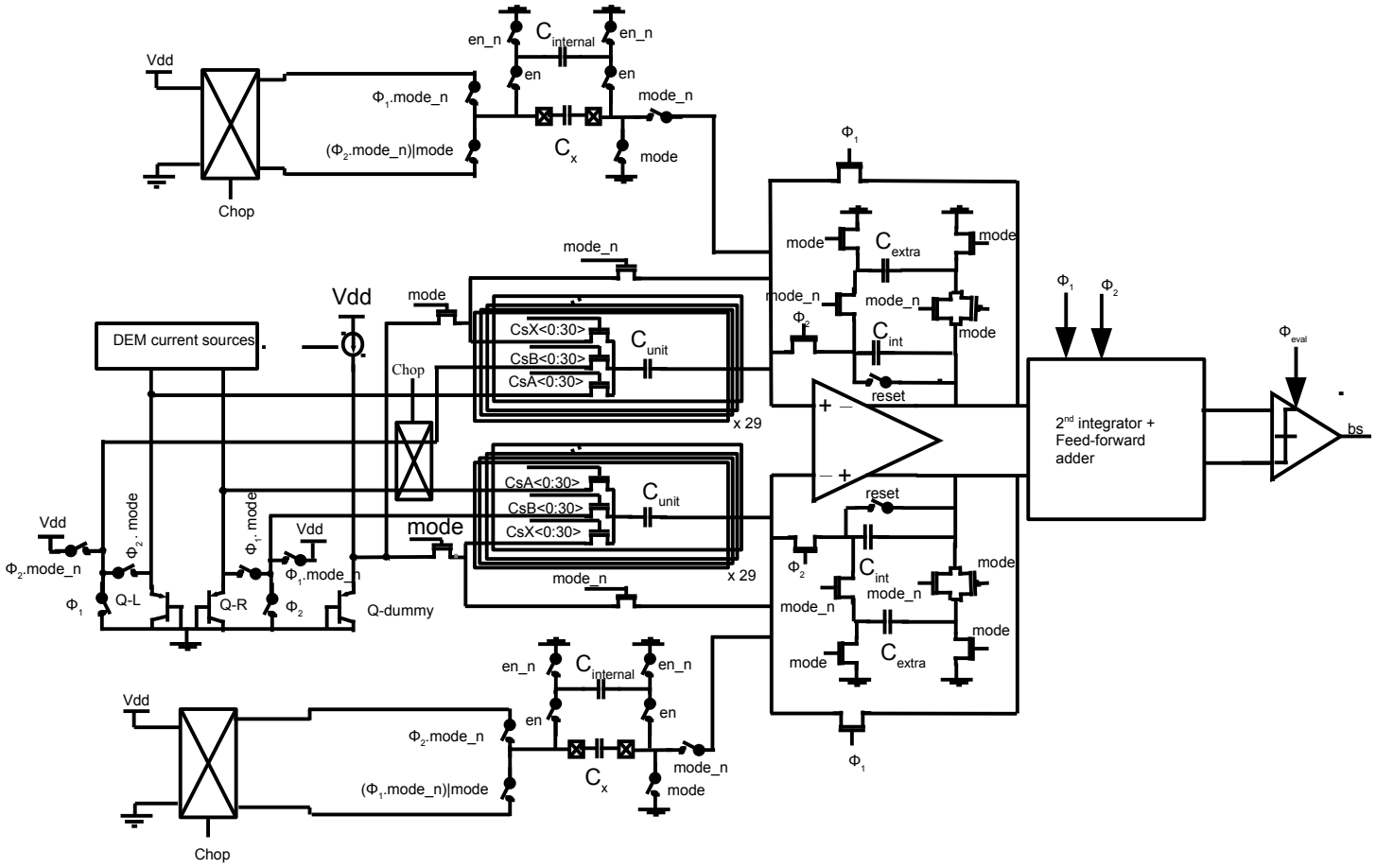


Figure 4.4: Combined capacitance and temperature to digital conversion interfacing

Figure 4.4 shows the combined interfacing of the temperature and capacitance sensor. While adding capacitance sensing functionality, following considerations are taken :

1. During the TDC mode, both ends of the sensor capacitor C_{sensor} (which is the external capacitor in this design) is grounded.

2. The capDAC will be used as baseline capacitance during CDC operation. The capDAC and the sensor capacitor switched between gnd and V_{dd} according to the integration scheme proposed in section 4.2.

3. The unused capacitors in the capDAC are connected to the virtual ground of the OTA at both the ends. As both the ends of those capacitors are shorted, this will not make them load the virtual node of the OTA and will not add to *kTC* noise charge during CDC mode.

4. During CDC mode, the output swing of the 1st integrator is large, i.e., if the value of *Cint = 2 * Cu,* the maximum output swing is 900mV, which would cause clipping at the OTA output. In order to reduce the output swing, the integrating capacitor value has to be increased by adding another capacitor parallel to the existing capacitance.

5. Leakage current due to turned off switches connected between the supply V_{dd} and the emitter node of the BJTs will degrade the inaccuracy of the temperature sensor. A 'T' switch (shown in figure 4.5) is used. During the TDC mode, the drain source potential of NM2 is nearly zero, so the leakage current through NM2 is minimized to a large extent.

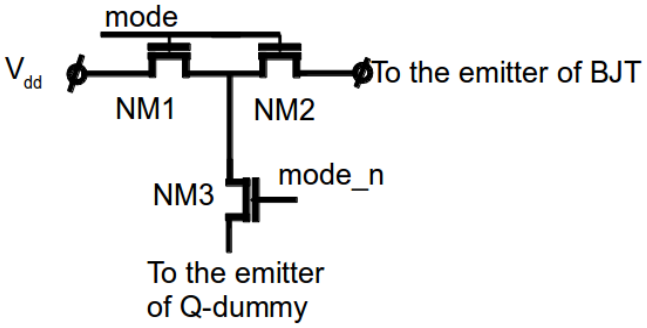


Figure 4.5: 'T' switch in order to minimize leakage current into bipolar transistor.

6. In order to minimize the external interference (due to the finite isolation of the switch connected between virtual ground of the OTA and external sensor capacitor pin) into the chip during the TDC mode, the switch connected between the virtual ground of the OTA and the sensor capacitor is made into a 'T' switch (shown figure 4.6) . This 'T' switch will minimize the leakage current through NM5. This will increase the resistance of across the source drain of transistor NM5, thus minimizing the external interference from the sensor capacitor pin.

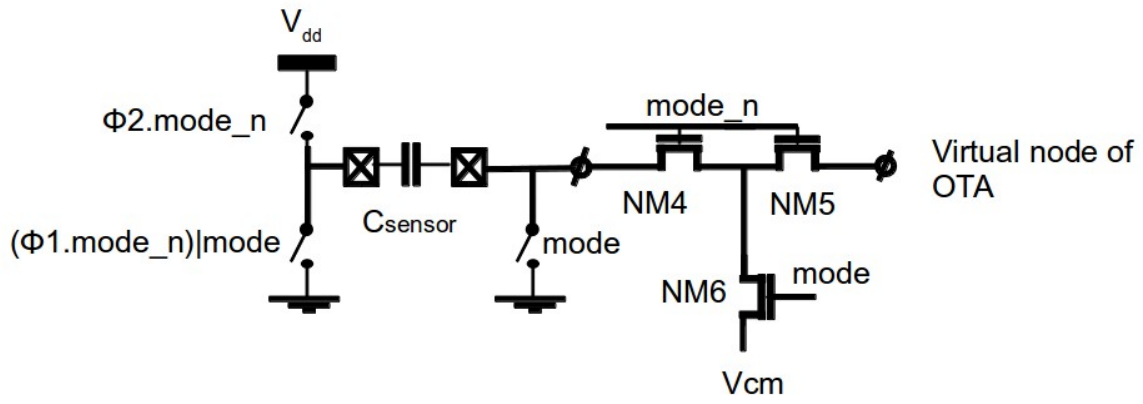


Figure 4.6: 'T' switch in order to minimize external interference during TDC mode.

7. System-level chopping has been used to minimize the effect of charge injection mismatch and supply dependency in the CDC mode.

4.4 Simulation results

In this section, certain schematic simulation results regarding the functionality of the CDC will be shown. Figure 4.7 shows the swing of the 1st integrator output which is $400mV_{p\text{-}p}$. This swing is enough to have sufficient headroom in the telescopic OTA.

Figure 4.8 shows the FFT plot of a bitstream output in the CDC mode with $C_x = 1.2pF$. Around 2483 points of the bitstream are taken for the FFT plot. It can be observed that the thermal noise is around -100 dB from the full-scale as expected.

Figure 4.9 show the FFT plot of the bitstream in the TDC mode at room temperature. Like the CDC case, the same 2483 bitstream points are taken for the FFT plot. It can be observed that the thermal noise is around -75dB to -80 dB from the full-scale as expected.

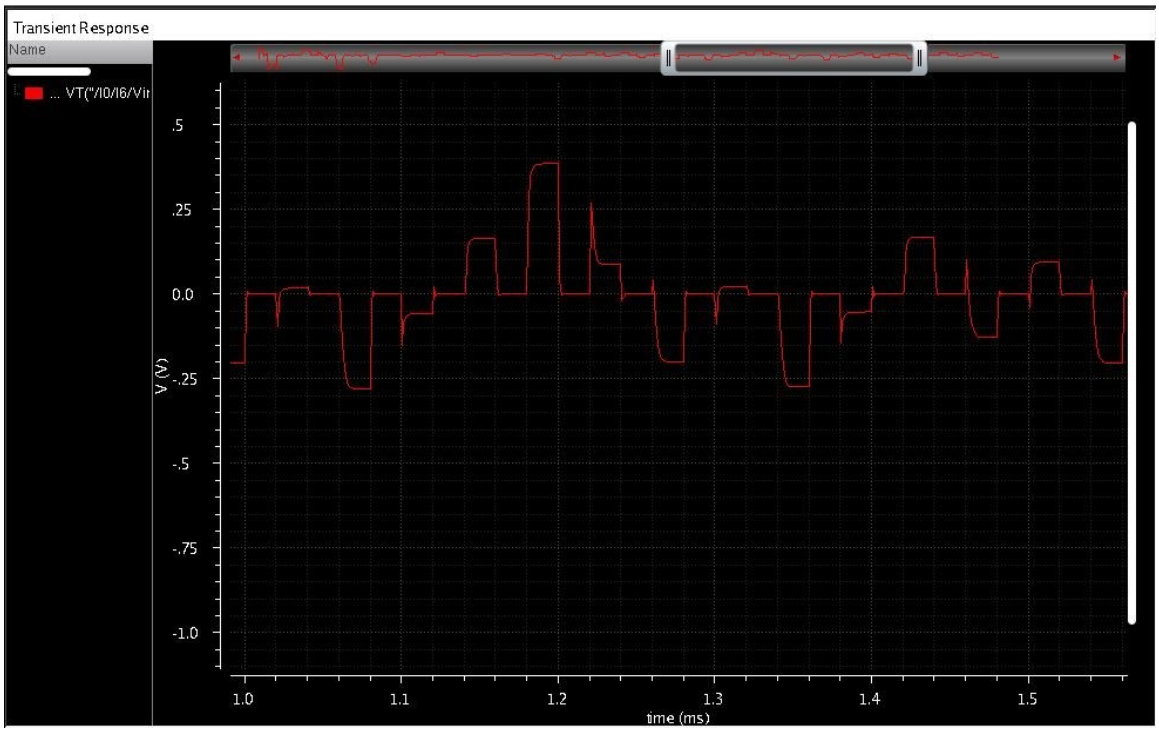


Figure 4.7: 1st integrator output swing during the CDC mode.

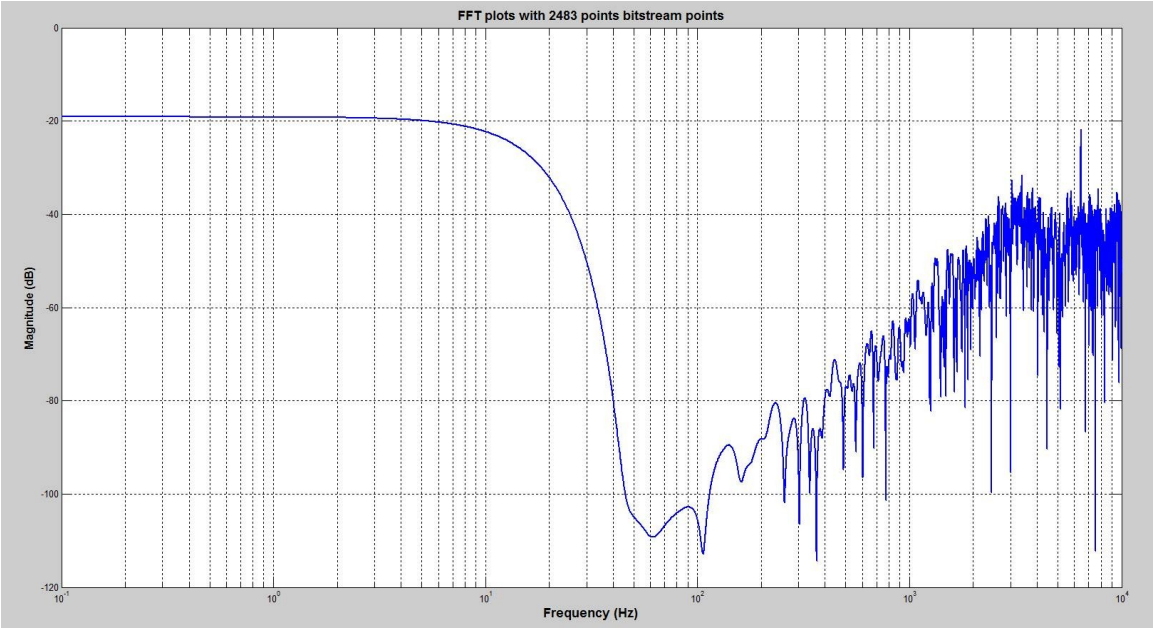


Figure 4.8: FFT plot of bitstream in CDC mode.

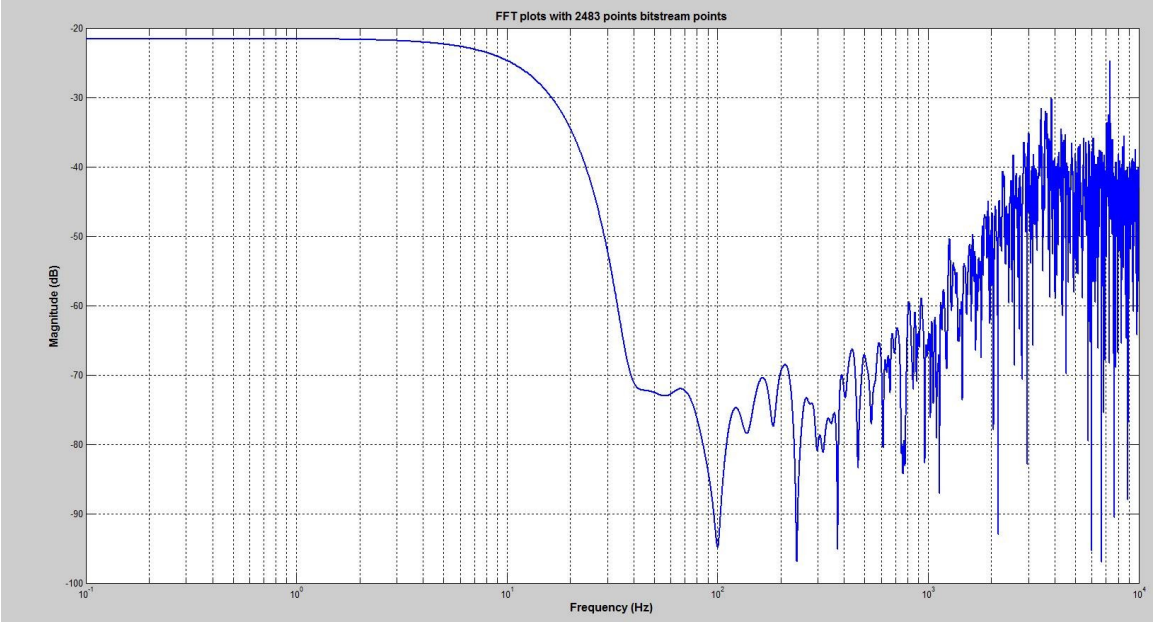


Figure 4.9: FFT plot of bitstream in TDC mode at room temperature.

4.5 Layout

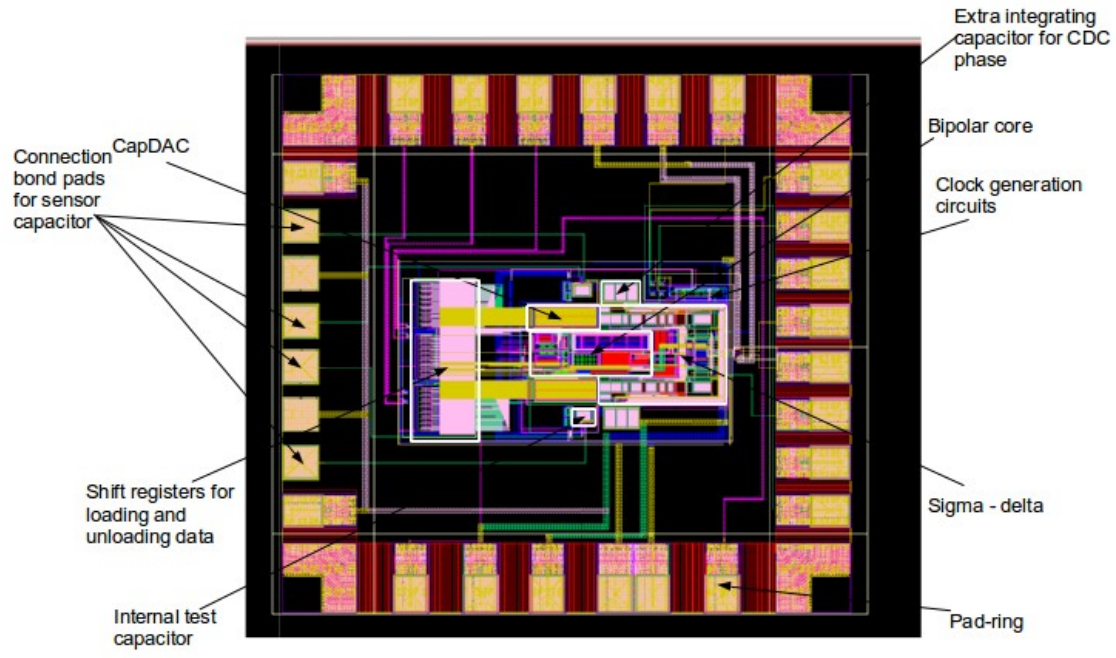


Figure 4.10: Layout of combined temperature and capacitance to digital converter chip.

Figure 4.10 shows the layout of combined capacitance and temperature to digital converter chip (area- 1136µm X 1136µm). The area of the system layout excluding the padring and free space is 300µm X 600µm. This is larger than the area of the existing TDC architecture (200µm X 400µm). In additional to the area of bipolar core and Zoom ADC, major amount of area has been occupied by the routing of metals (which can be optimized further) and the memory elements.

This chip is taped out in NXP C-14 technology (160nm process node).

Chapter 5
Measurement results

In this chapter, the measurements of the chip in CDC phase will be discussed. First an outline of the measurement setup will be given, followed by the measurements done in CDC phase: functional test of the CDC, resolution measurement, supply dependency and the effect DEM. The measurements of the TDC could not be done within the time frame of this thesis.

Figure 5.1 shows the chip micro-graph of the combined CDC and TDC chip. This chip has been taped out in NXP C14 technology (160nm process node). The die is bonded and packaged in a 28 pin ceramic DIL package. The area of the die is around 1.2 mm^2.

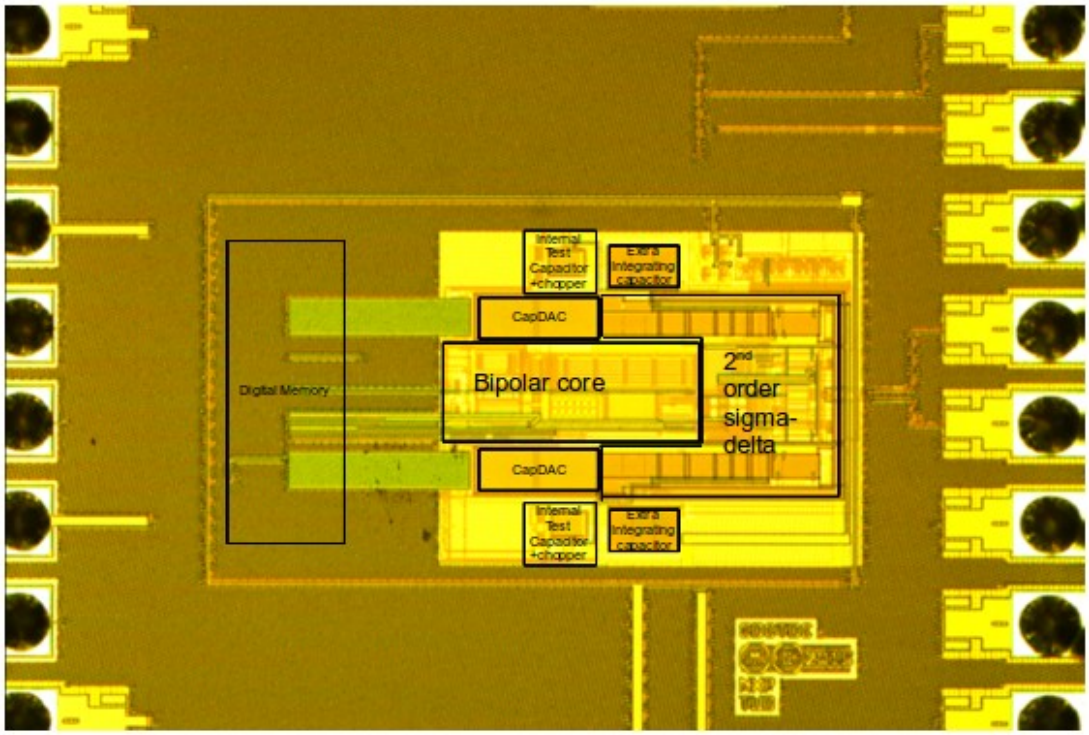


Figure 5.1: Chip-micrograph of the Combined Capacitance and Temperature to digital converter chip.

5.1 Measurement setup

The measurement setup (the block diagram of which is shown in figure 5.2) consists of a PCB (Printed Circuit Board) for interfacing the chip; an FPGA (Field Programmable Gate Array), which generates clock signals and programs the control bits of the chip; and a DAQ (Data Acquisition board) which takes signals such as trigger, clock and the bitstream from the FPGA and PCB, to capture the bitstream in a synchronized way and send it to a PC for post processing.

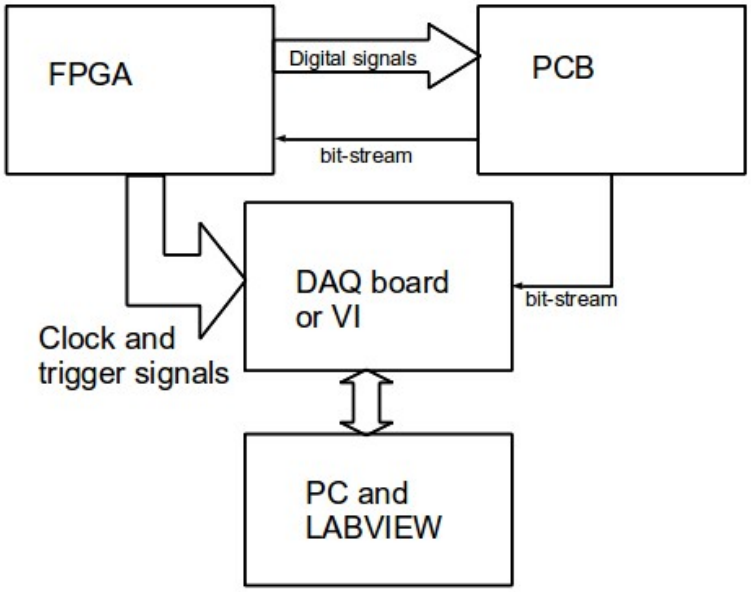


Figure 5.2:Block diagram of the measurement setup

Analog and digital supplies for the chip are generated on a PCB using a low-dropout regulator IC (LP38511MR). A separate IC (PSSI2021SAY) is used to generate bias currents for the buffers connected to the Analog Test Bus (ATB) pins. The sensor capacitors used here are external SMD capacitors, whose two ends are placed and pressed onto (for proper contact) a pair of metal strips, which are connected to the pins of the combined CDC and TDC IC.

Figure 5.3 shows a picture of the measurement setup. The PCB is placed inside a grounded metal box in order to shield it from external interference. Figure 5.4 shows the PC control interface through LABVIEW.

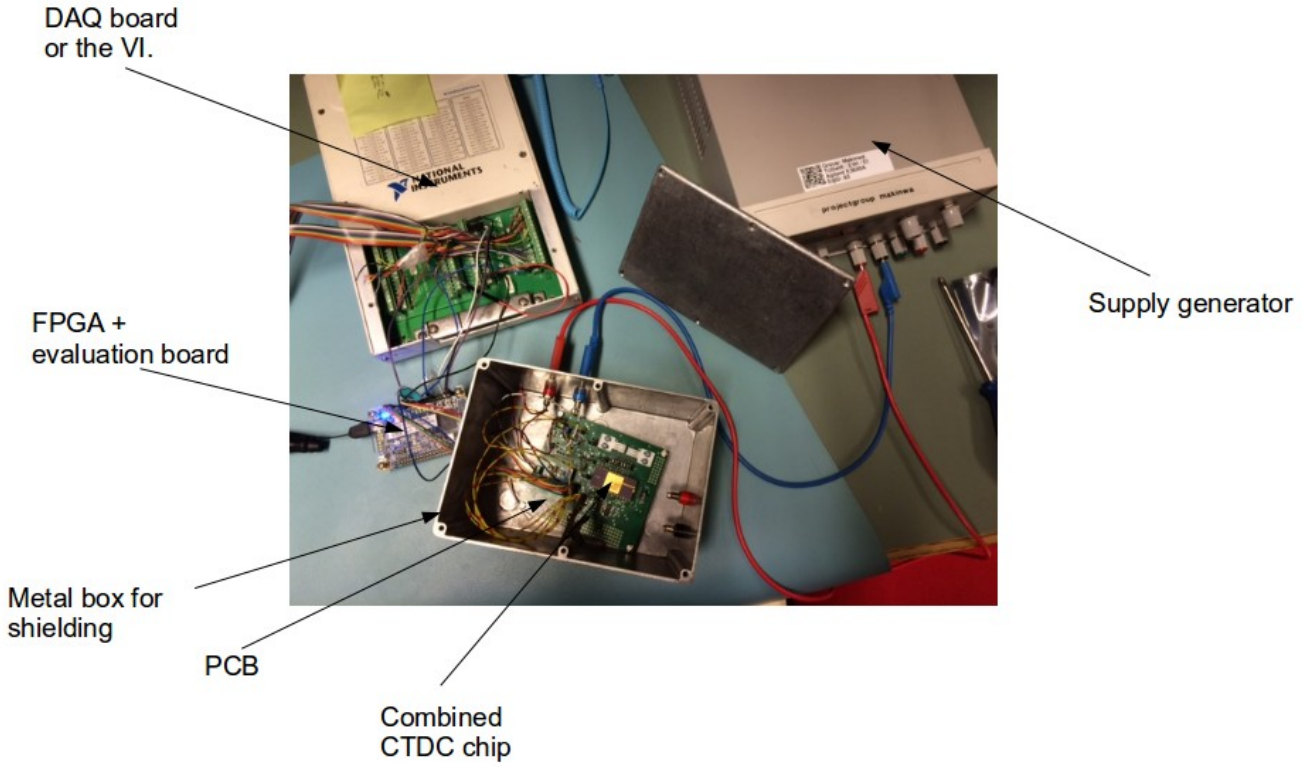


Figure 5.3: Measurement setup

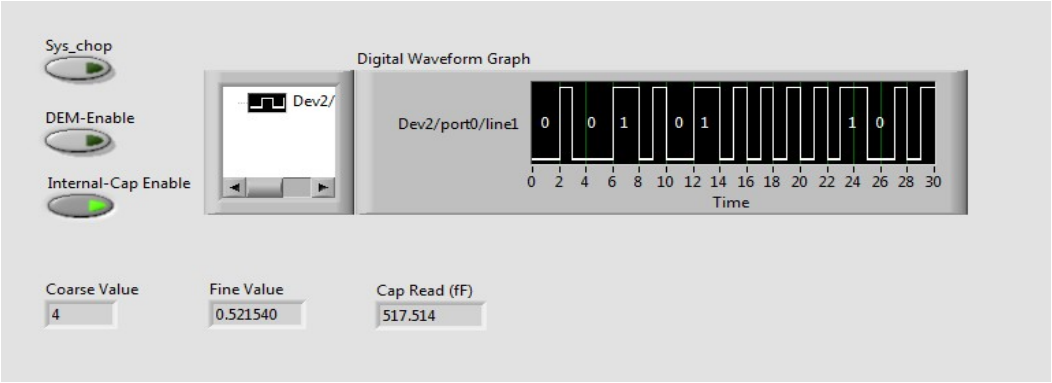


Figure 5.4 : PC control interface through LABVIEW.

5.2 Functionality tests and Resolution measurements

The first measurement done is the functionality test, to check whether the SAR and the sigma-delta modulator are operational. First the SAR (or coarse) mode approximates the ratio of C_x/C_{unit}, followed by the guard band step, which sets the references for the sigma-delta.

Figure 5.5 and figure 5.6 show the FFT (Fast-Fourier Transform) plots of the bit-stream for CDC mode obtained using on-chip capacitors (of nominal value of 360fF) and external capacitors (of value around 500fF). It can be observed from the plot, that the slope of quantization noise is around 40dB per decade, which signifies 2nd order sigma-delta CDC operation. Also the thermal noise floor at lower frequencies is around -100dB from full-scale. This shows that the chip is functional and the noise floor is at the expected value. This chip also measures the parasitic capacitance contributed by the PCB, which is around 165 fF (figure 5.7).

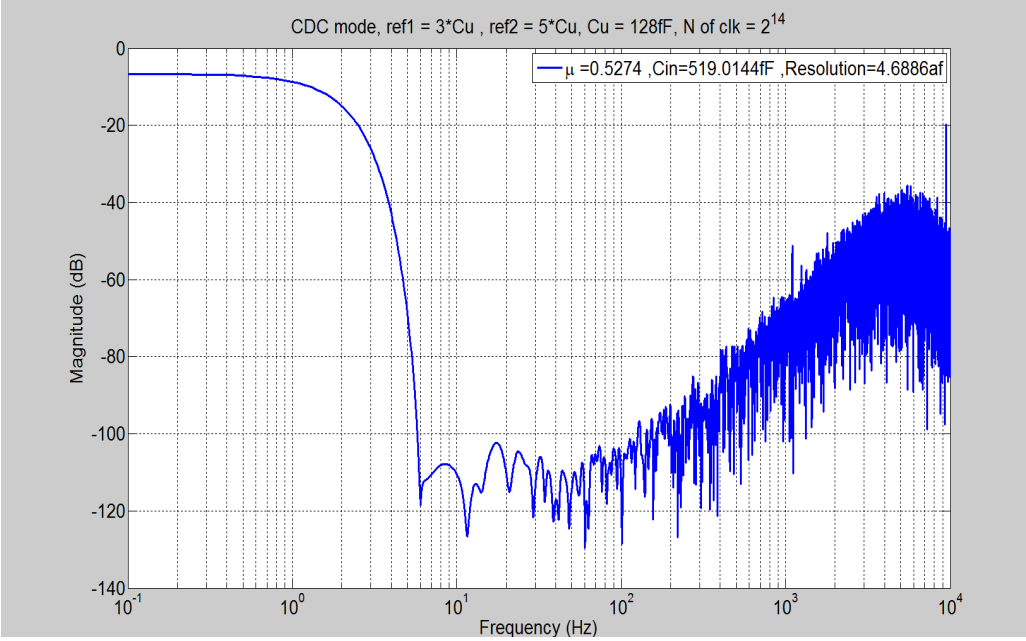


Figure 5.5 : FFT of CDC measurement done on on-chip capacitors including the parasitics of PCB.

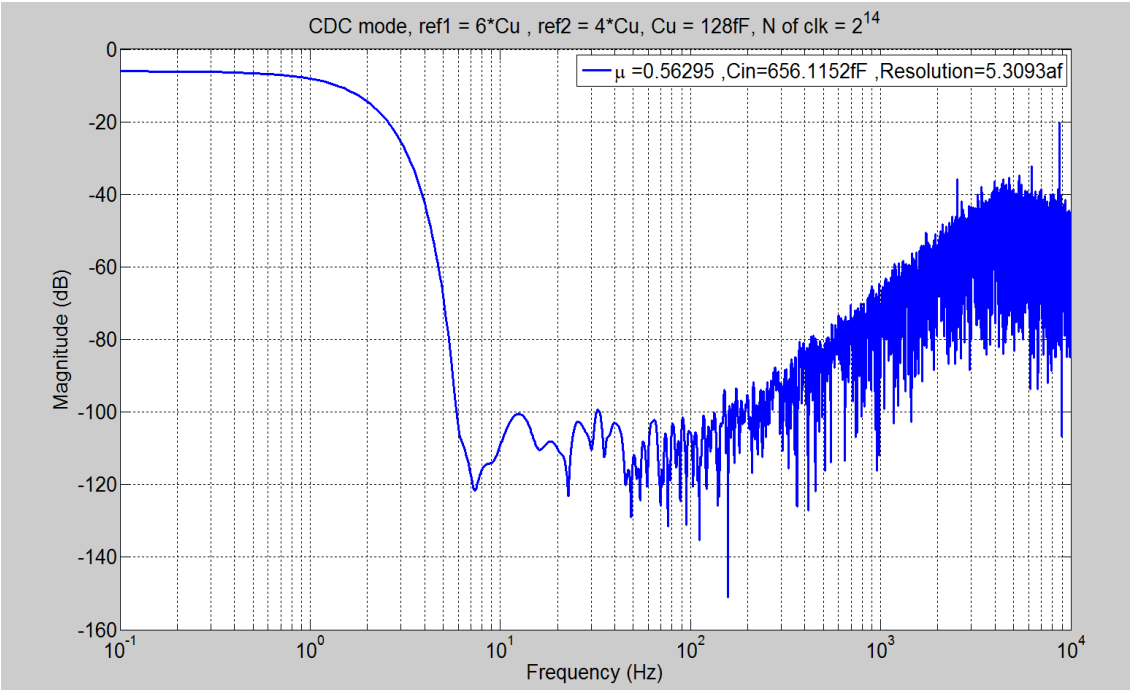


Figure 5.6 : FFT of CDC measurement done on external capacitor (of value 500fF) ,including the parasitics of PCB .

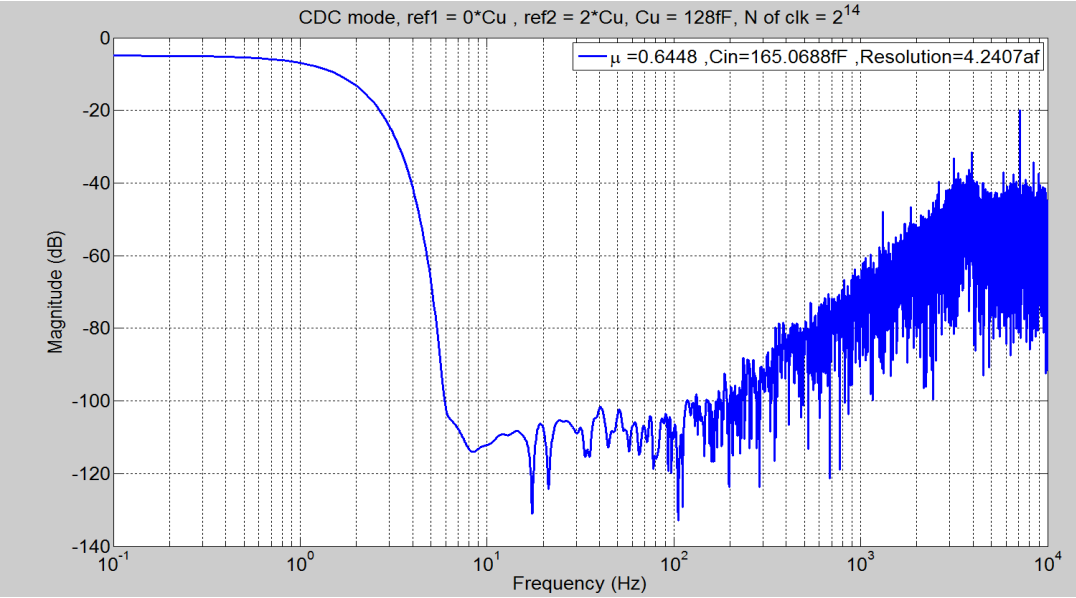


Figure 5.7 : FFT of CDC measurement done on parasitics contributed by the PCB

Resolution is defined as the smallest change at the input which leads to a detectable

change at the output. So the 'resolution' of the instrument is equal to the input referred noise (input referred quantization error or input referred thermal noise by the readout circuitry). In order to improve the resolution, the number of clock cycles N (used for sampling the input) must be increased. The resolution shown in the annotation in figures 5.5, 5.6 and 5.7 have been calculated by taking the standard deviation of 20 measurements.

Figure 5.12 and figure 5.13 show the resolution vs conversion time plot of a CDC measurement on external and on-chip capacitors respectively. For the $sinc^2$ filter case, at lower conversion time, the noise floor is dominated by the quantization errors. As the conversion time increases, quantization errors decrease and at one point, the noise floor is dominated by thermal noise. It is also shown in both the figures that it takes longer conversion for the sinc filter case than compared to that of $sinc^2$ filter. It can be observed in figure 5.12, that the resolution at 30ms conversion time and $sinc^2$ filter, is around 6.5aF.

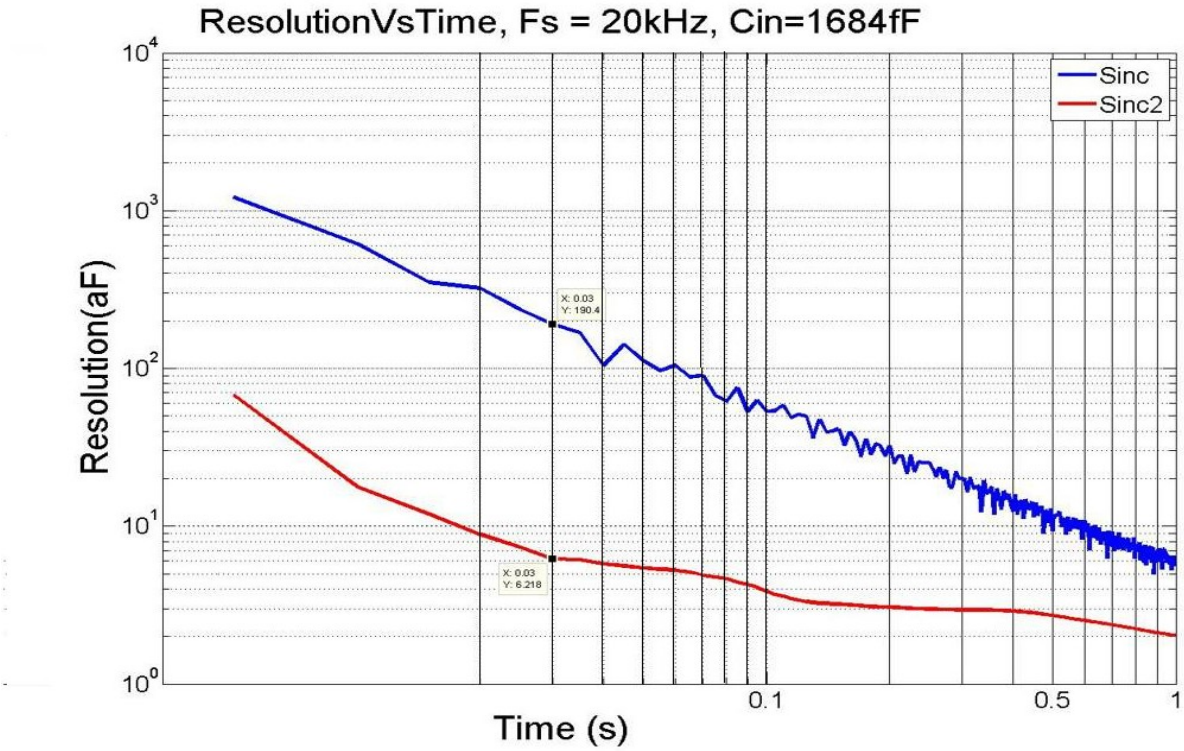


Figure 5.12: Resolution vs conversion time plot of measurement using external capacitors

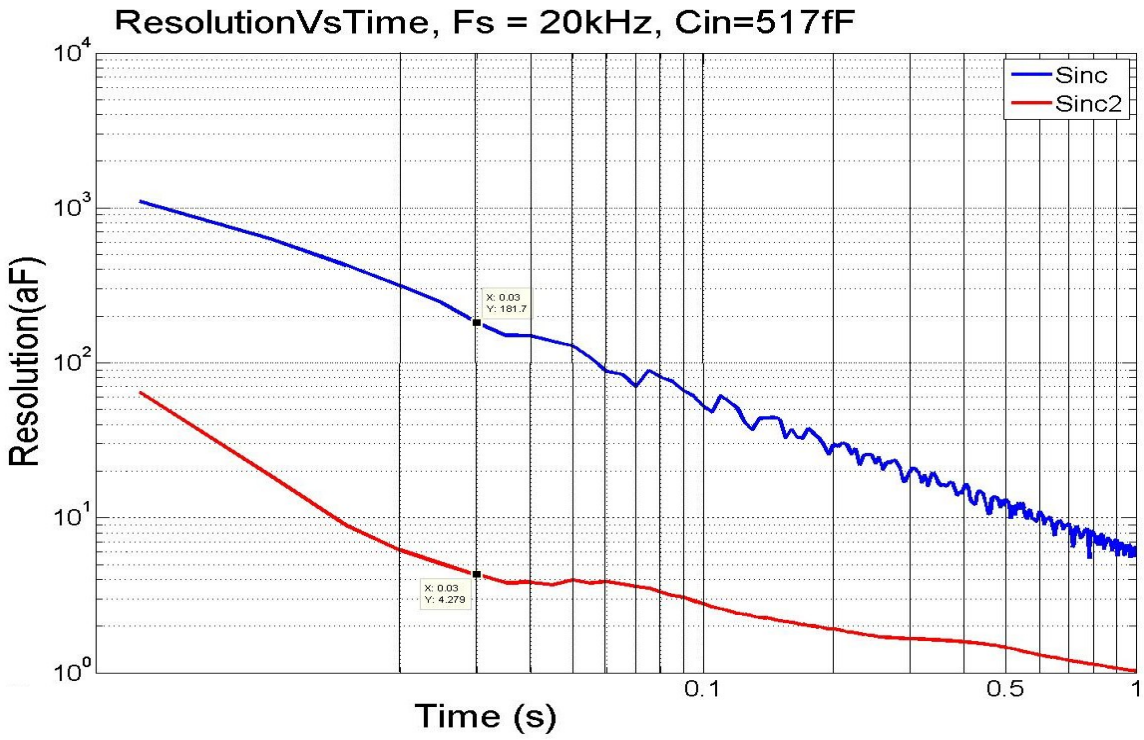


Figure 5.13: Resolution vs conversion time plot of measurement using on-chip capacitors

5.3 Supply dependency

The main motivation behind this experiment is to check whether chopping helps in minimizing the supply dependency on the output of the sigma-delta modulator CDC. The results are shown in figures 5.14 & 5.15.

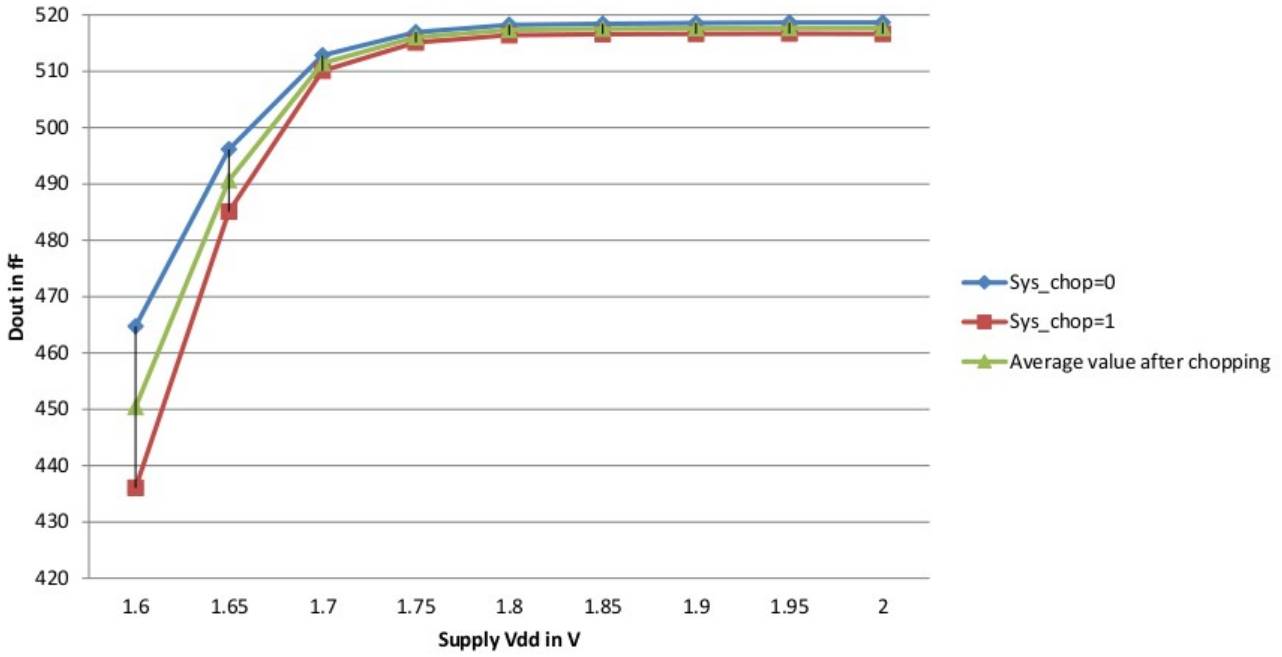


Figure 5.14: Digitized capacitance value vs Supply Vdd in V

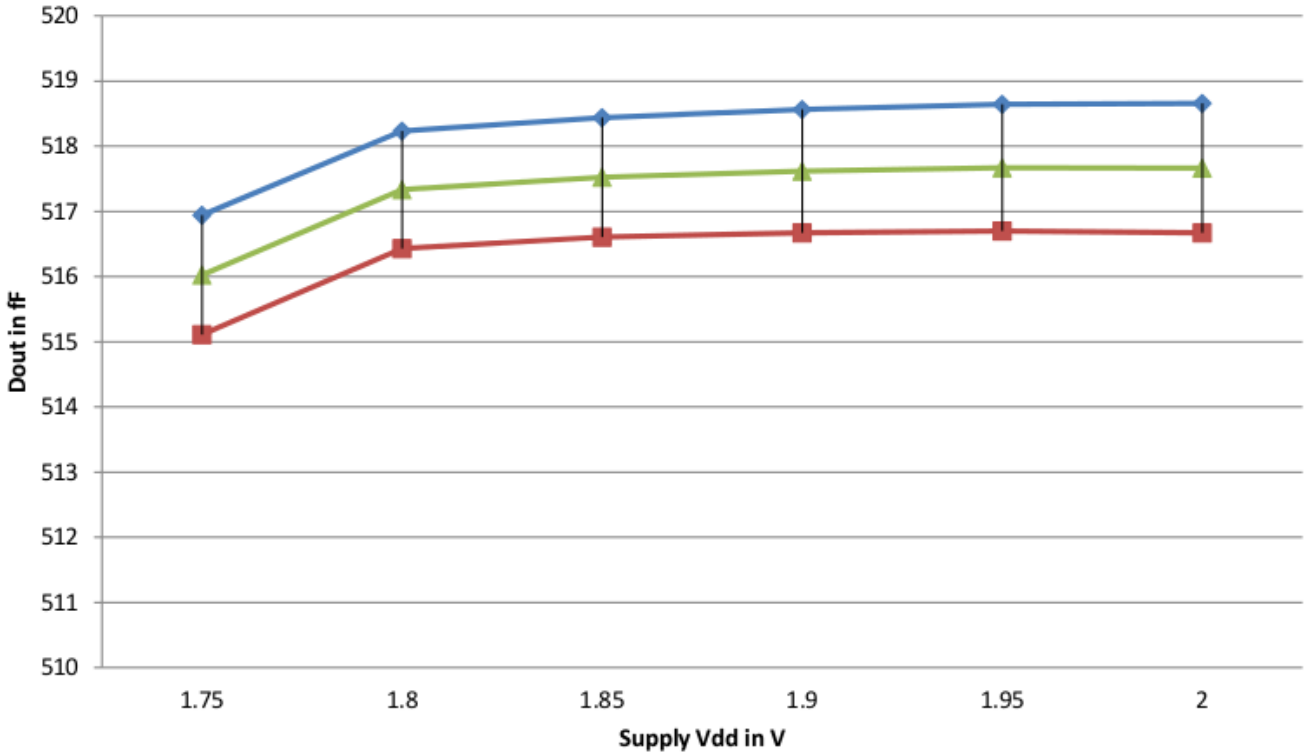


Figure 5.15: Digitized capacitance value for Vdd higher than 1.7 V.

At supply V_{dd} lower than 1.7V, certain analog blocks in the CDC are not properly functioning and figure 5.15 shows that at higher V_{dd}, chopping isn't minimizing the effect of supply dependency.

5.4 Effect of dynamic element matching

Two DEM algorithms have been implemented: one is the single-pointer barrel shifting DEM (shown in table 5.1) and other one is the double-pointer barrel shifting DEM (shown in table 5.2).

Table 5.1 : Single pointer barrel shifting DEM algorithm example

bs	Capacitors chosen
0	C_1 , C_2
1	C_3, C_4, C_5, C_6
1	C_7,C_8,C_9,C_{10}
0	C_{11},C_{12}
1	C_{13},C_{14},C_{15}, C_{16}
0	C_{17}, C_{18}
⋮	⋮
0	C_{30},C_1

Table 5.2 : Double pointer barrel shifting DEM algorithm example

bs	Capacitors chosen
0	C_1, C_2
1	C_1, C_2, C_3, C_4
1	C_5,C_6,C_7,C_8
0	C_3,C_4
1	C_9,C_{10},C_{11}, C_{12}
0	C_5, C_6
⋮	⋮
0	C_{29},C_{30}
0	C_1,C_2

Figure 5.16 and Figure 5.17 show the FFT plots of both the DEM schemes and it shows

that single pointer barrel shifting DEM algorithm adds tones and increases the thermal noise floor. Double pointer DEM algorithm shows favorable effect for the resolution in CDC phase.

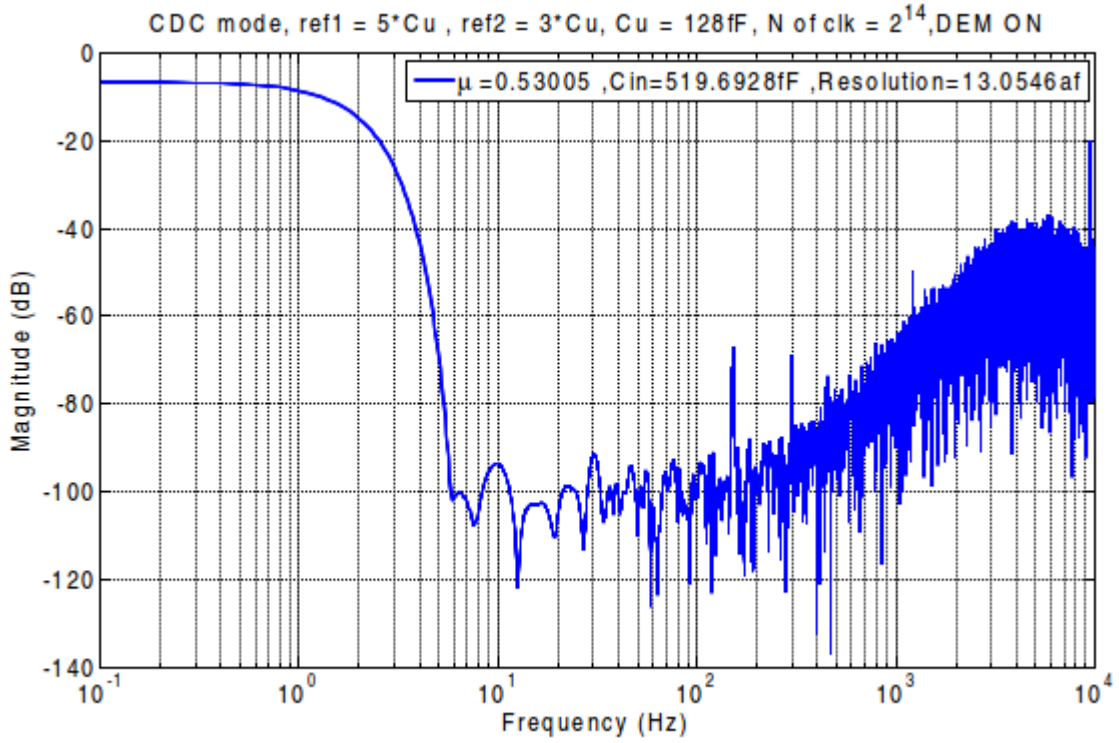


Figure 5.16: FFT plot of bitstream using single pointer DEM

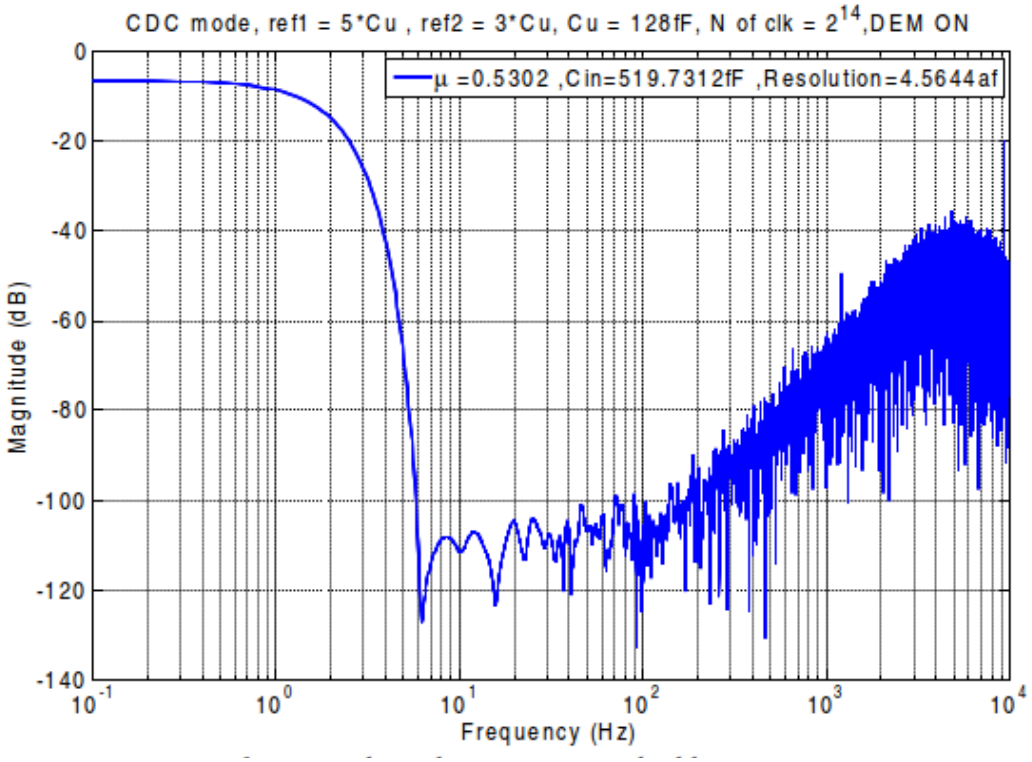


Figure 5.17: FFT plot of bitstream using double pointer DEM

To check the effect of DEM in minimizing the discontinuities between sub-ranges, the die is bonded to a pressure sensor (which converts pressure to capacitance). The setup is kept inside a pressure chamber, where the pressure is swept from 300mbar to atmospheric conditions. The measurement has been taken for one subrange and the result is shown in figure 5.18.

The change in the coarse value from 5 to 5.5 indicates that the Zoom CDC has been transitioned from one subrange to the next. The error in figure 5.18 is calculated by taking the difference between capacitance calculated in the CDC mode and its 5th order polynomial fit. The experiment is done with and without DEM. It is observed that the discontinuity is larger with DEM compared to the one without DEM, which contradicts the results based on system-level simulations. The reason behind this contradiction has to be investigated further.

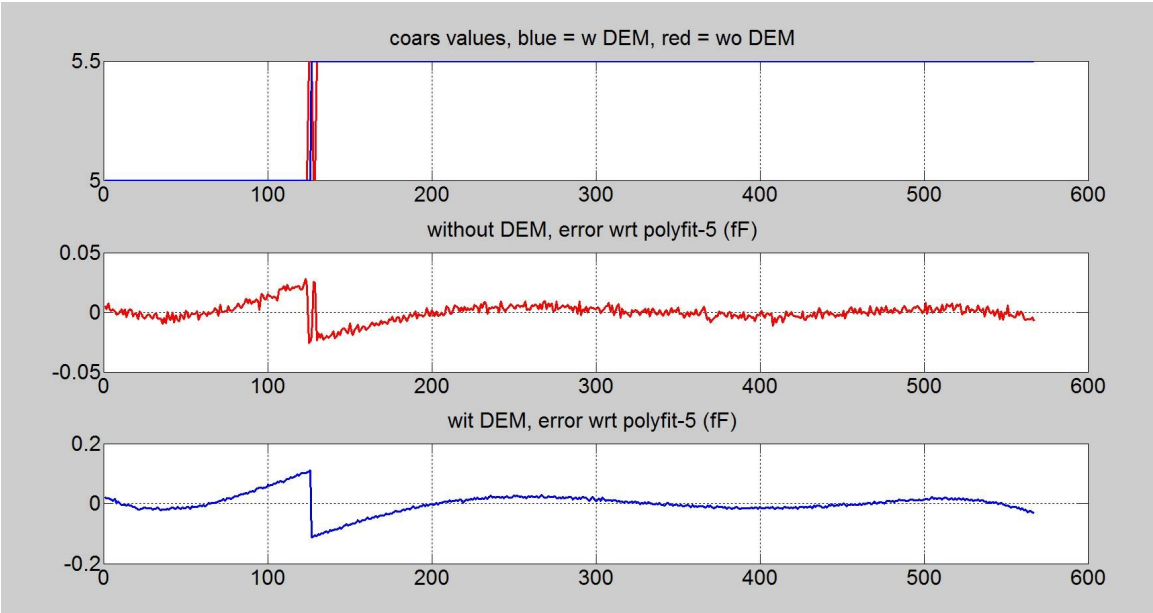


Figure 5.18: Plots of the coarse value and errors between the actual curve and the polynomial fit with (w) and without (wo) DEM case.(The X-axis shows the time elapsed)

5.5 Benchmarking

Table 5.3 shows a comparison of the specifications achieved by this CDC design compared to the state-of-the-art. Here ENOB is calculated based on the formula :

$$ENOB = \frac{SNR - 1.76}{6.02} \tag{5.1}$$

where SNR is given by the relation:

$$SNR = 20\log\left(\frac{C_{range}}{2\sqrt{2}\,C_{resolution}}\right) \tag{5.2}$$

where C_{range} is the maximum capacitance range of the CDC and the $C_{resolution}$ is the capacitance resolution.

FOM (Figure of Merit) is calculated based on the formula:

$$FOM = \frac{Energy\ per\ conversion}{2^{ENOB}} \tag{5.3}$$

Table 5.3 :Performance comparison of the current design to the state-of-the-art.

Design	Type	Supply Voltage	Current cons.	Meas. time	Capacitance range	ENOB	FOM
Current design	2nd order Zoom	1.8 V	3 µA	30 ms	1.8 pF	16.4 bit	1.87 pJ/step
[4]	SAR+ Sigma-delta	1.4V	24 µA	0.23 ms	24 pF	15.4 bit	0.18 pJ/step
[5]	Iterative Delay chain discharge	1 V	1.84 µA	0.01906 ms	1000 pF	8 bit	0.14 pJ/step
[10]	3rd order Zoom	1.5V	10 mA	20 µs	10 pF	17.2 bit	1.95 pJ/step

Chapter 6
Conclusion and Future work

6.1 Conclusion

The thesis is concluded with the following findings:

1. Capacitance functionality has been added to the existing TDC design. The present area of the combined CDC and TDC die can be further optimized with an additional active area (due to the capacitance sensing functionality) to around 30% .

2.The Combined Capacitance and Temperature to digital converter chip is functional.

3. A FOM 1.87pJ/step has been achieved in the CDC mode.

4.Single pointer barrel shifting DEM algorithm adds to tones and increases the noise floor in the spectrum. A better alternative would be to use double-pointer DEM.

6.2 Future work

Since the measurements for the thesis are in-complete, below are the list of things to be done as a future work. They are:

1.The advantage DEM, that is minimizing discontinuities between the sub-ranges has to be investigated.

2.More extensive TDC measurements have to be done in order to check that the addition of capacitance sensing to the existing TDC design hasn't affected the performance much (resolution and the accuracy performance should remain more or less the same).

Looking into the target specifications and the specifications achieved for CDC mode in this design, the parameter lagging behind is conversion time and the system is designed for supply V_{dd} of 1.8V. At 1.5 V supply, certain analog blocks are not properly functioning. So after the end of this project, in later future, the entire OTA (in 1^{st} integrator) has to be re-designed for 1.5V V_{dd} supply and lower settling time.

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