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Monolithic integration of a smart temperature sensor on a modular silicon-based organ-on-a-chip device

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ABSTRACT

One of the many applications of organ-on-a-chip (OOC) technology is the study of biological processes in human induced pluripotent stem cells (iPSCs) during pharmacological drug screening. It is of paramount importance to construct OOCs equipped with highly compact *in situ* sensors that can accurately monitor, in real time, the extracellular fluid environment and anticipate any vital physiological changes of the culture. In this paper, we report the co-fabrication of a CMOS smart sensor on the same substrate as our silicon-based OOC for real-time *in situ* temperature measurement of the cell culture. The proposed CMOS circuit is developed to provide the first monolithically integrated *in situ* smart temperature-sensing system on a micromachined silicon-based OOC device. Measurement results on wafer reveal a resolution of less than ±0.2 °C and a nonlinearity error of less than 0.05% across a temperature range from 30 to 40 °C. The sensor's time response is more than 10 times faster than the time constant of the convection-cooling mechanism found for a medium containing 0.4 ml of PBS solution. All in all, this work is the first step towards realizing OOCs with seamless integrated CMOS-based sensors capable to measure, in real time, multiple physical quantities found in cell culture experiments. It is expected that the use of commercial foundry CMOS processes may enable OOCs with very large scale of multi-sensing integration and actuation in a closed-loop system manner.

1. Introduction

Organ-on-a-chip (OOC) is an emergent technology in which a microfluidic perfusion platform for culturing human iPSCs is used to mimic a minituarized version of an explicit organ anatomy and physiology. This technology has been developed to substitute traditional *in vitro* and animal models that are often inaccurate to predict the human physiology [1,2]. Studies indicate that OOCs can play a transformative role in the drug development cycle by bridging the gap between preclinical studies and human trials, while reducing the pharmaceutical R&D costs to 10–26% [3].

For the construction of these OOC systems, various micro- and nano-fabrication technologies have been used, including soft lithography on elastomeric materials. The simplicity, fast turnaround time, and relatively low cost of this technique affords quick experimentation of new designs. Examples of such designs include OOCs for the heart [4], the liver [5], the kidney [6], the lung [7], and tumours [8,29]. On the other hand, shortcomings of such methods include limited device throughput which is a crucial feature for high-volume manufacturing.

To overcome this, MEMS (Microelectromechanical Systems) technology based on silicon wafer level processing proves to be a very efficient option for micromachining high-aspect ratio structures with submicrometer resolution, and over a wide range of materials [9]. Although dependent on highly specialized and expensive equipment, the high initial costs are counteracted when large production volume is anticipated. Additionally, MEMS processes often are compatible with CMOS (complementary metal oxide

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semiconductor) technology which allows monolithic integration of dedicated interface electronics for thermal, optical, pH, and label-free sensing necessary to design compact cell culture systems [10]. Furthermore, the *in situ* real-time analysis offered by these microelectronic systems could reveal new insights into intra- and inter-cellular signalling pathways.

Currently, the aforementioned analysis assumes that the pH, temperature (~37 °C), humidity (~95% RH) and gaseous atmosphere (CO_2/O_2 levels) around the cell culture medium are regulated by incubators. These parameters should be kept constant since they play a pivotal role in the optimal growth and maximum productivity of the cell culture [11]. However, variations do occur, which cause stress in the cells that can respond in various ways ranging from the activation of survival pathways to the initiation of senescence.

Especially, recurrent temperature variations in the cell culture should be carefully monitored as they may severely affect the experiments. Causes for such variations can be due to deviations between the incubator's temperature setpoint and the temperature of the cells, the frequency and duration of the incubator's door opening, and the duration the cells are outside the incubator for inspection [12]. Above all, time spent outside the incubator represents a larger, more variable, factor that is likely to impact cell health. A drop of the culture temperature to room temperature results in a considerable decrease in cell growth along with the accumulation of cells in the G1 phase [13,14]. In fact, the rate at which the temperature of the cell culture decreases outside the incubator is unknown to life science researchers. This has motivated us to construct a real-time CMOS temperature sensor to monitor the *in situ* temperature of the culture throughout the cell-division cycle.

A variety of electrical cell culture temperature sensing methods has been presented in previous literature: commercial T-type thermocouples made of copper and constantan wires [15], NTC (negative temperature coefficient) thermistors [16] or commercial PT-100 RTDs (resistance thermometer detectors) [17]. A common drawback of the aforementioned solutions manifests itself when interfacing the sensor's output with readout systems that are outside the culturing environment. In this scenario, with the sensor remote from readout electronics, various sources of errors (noise, interference, distortion, crosstalk, etc.) may be introduced over the channel and impair the measurement. Moreover, such commercial sensors are not very compact for OOC applications.

Non-electrical temperature sensing methods have also been reported, such as liquid crystal displays [18], fluorescent polymeric thermometers [19], and optoacoustic methods [20]. These solutions, however, are not very compact because they depend on expensive and bulky instrumentation laboratory equipment [21] to optically map the temperature of the culture. Moreover, these systems have poor resolution (~1 °C), do not easily allow the integration of closed-loop systems and do not offer the high throughput of silicon-based microsystems.

To tackle these shortcomings, we have fabricated a smart temperature sensor on the same silicon substrate used to construct our custom micromachined organ-on-a-chip device. As a consequence, the system is made more compact and the robustness to various sources of errors is enhanced. To accomplish this, we used a simple, robust, and custom in-house integrated circuit (IC) technology [22]. We have previously used this technology to design and characterize a suitable temperature sensor [23]. In this paper, we are presenting a complete, seamlessly integrated *in situ* smart temperature-sensing system on an OOC. To the best of the authors' knowledge this is the first time such integration is performed using a custom-designed sensing and conditioning circuit fabricated on the same silicon substrate as that of the OOC.

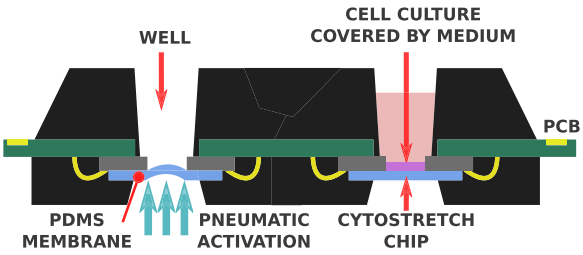

Fig. 1. Artistic impression of the Cytostrech system.

As opposed to a System-in-Package (SiP) approach, in which an outsourced ASIC (Application-specific Integrated Circuit) is heterogenously integrated on the OOC device, our solution avoids the use of chip mounting technology (e.g. wire and die bonding) that usually requires extra packaging protection of the assembled components. In contrast, our seamless integration minimizes the extra processing steps and precludes potential mechanical stresses caused by mismatches in the thermal expansion coefficient of the various dissimilar components and materials to be used in a SiP scenario. Finally, the holistic CMOS-MEMS co-design approach offers the possibility to conform and better accomodate the inclusion of CMOS electronics over various MEMS topologies.

2. Materials and methods

Our OOC platform, presented here as Cytostretch [24], is modular, customizable, silicon-based and microfabricated with cleanroom-compatible processes. The main components of the system are depicted in Fig. 1, where the Cytostretch chips are bonded to a PCB that includes a moulded multi-well plate for culturing the cells. The chips include a pneumatically-activated freestanding dog-bone-shaped PDMS membrane to accommodate the cell culture (module 1) while delivering mechanical stimuli to the cells in various in-vitro studies, additional features, such as through-membrane micro-pores for biological signal exchange (module 2), on-membrane grooves for cell alignment (module 3), in-membrane titanium nitride (TiN) microelectrodes for monitoring activity from electrically active cells (module 4), and titanium (Ti) strain gauges to measure the deformation of the PDMS membrane during inflation (module 5). More details on these specific modules can be found in [25]. The smart temperature sensor presented in this paper is the sixth module of this OOC platform. This module was accomplished thanks to the monolithic integration of this smart sensor on the backside of our OOC device. The temperature of the cells is sensed as a result of the heat transferred from the culture medium to the crystalline silicon through thermal conduction mechanisms associated with elastic vibrations of the lattice (i.e. phonons transport).

2.1. The smart temperature sensing module

The smart sensing module was designed to detect the *in situ* temperature of the culture and convert it into a periodic digital electronic signal, which carries the temperature information encoded in the time domain. To realize this, the system consists of two main blocks: a proportional to absolute temperature (PTAT) current generator (employing NPN bipolar transistors to sense the temperature information) and a relaxation oscillator (Fig. 2).

The circuit operation can be understood from the system diagram of Fig. 2. During start-up, the output of the comparator is set to a logic "0" which turns the CMOS switches ($\bar{\Phi}$) on for the comparison phase. As a result, a PTAT current is integrated in the capacitor and its voltage (V_c) is ramped up. When V_c equals voltage V_H, the output of the comparator toggles and turns the other pair of

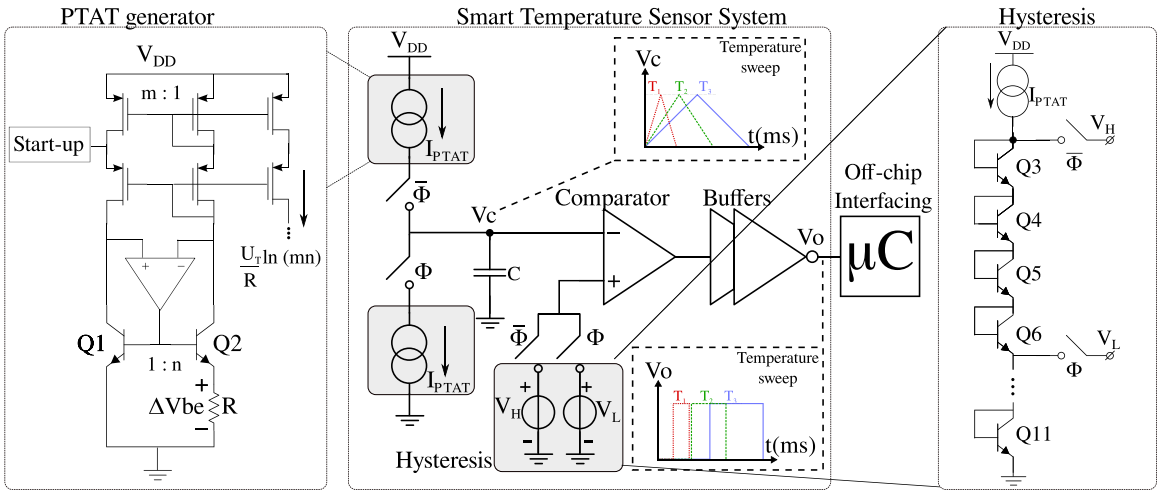

Fig. 2. Main blocks of the smart CMOS temperature sensor: a PTAT generator and a relaxation oscillator.

CMOS switches (Φ) on. The voltage V_c is now ramped down via the PTAT current sink until it reaches V_L ending the discharging cycle. Once started, this process continues indefinetely to yield a signal in which the period is PTAT according to the equation $T = C\Delta V/I_{PTAT}$, where ΔV is the difference between the threshold voltages V_H and V_L, C is the capacitance and I_{PTAT} is the PTAT current generated.

2.1.1. PTAT generator

The PTAT current generator yields a current that is proportional to the voltage drop (ΔV_{BE}) across the resistor R. Since this voltage is the difference of two base-emitter voltages, the current produced, $I = \Delta V_{BE}/R$, is PTAT. Current mirrors with a m:1 ratio convey the copy of this PTAT current to the capacitor. The collector voltages are forced to be equal, regardless of variations in the power supply or in the temperature, via the negative feedback loop that includes the opamp (Operational Amplifier), the bipolar devices (Q_1 and Q_2) and the resistor. The expression of the current across resistor R is:

$$I_{PTAT} = \frac{U_T}{R}\ln(mn), \tag{1}$$

where U_T is the thermal voltage (≈26 mV at room temperature), m is the current mirror ratio and n is the bipolar emitter area ratio. Hence, the responsivity of this block is mostly determined by the current mirror and emitter area ratios. In the design, values of 5 and 4 for m and n, respectively, were chosen. In addition, a start-up circuit for this PTAT cell was implemented to ensure its correct operating point.

2.1.2. Relaxation oscillator

The relaxation oscillator is realized by a feedback control performed by the comparator, the PTAT current source and the hysteresis circuit. Hysteresis is a functional requirement for the relaxation oscillator to work properly. The hysteresis circuit was implemented with nine stacked diode-connected bipolar devices biased with a copy of the PTAT current so as to produce the voltages V_H and V_L, at 37 °C, of 6 and 3.5 V, respectively. The hysteresis was made inversely proportional to the absolute temperature (CTAT) to increase the circuit responsivity with respect to the period.

2.2. Microfabrication on silicon substrate

The cofabrication of MEMS and CMOS on a single silicon substrate is typically adverse in terms of costs. This problem exacerbates in more advanced CMOS technologies due to the increased number of masks and processing steps required. For instance, adding high-performance vertical bipolar devices to a standard 0.18 μm CMOS technology can add up to 10–20 extra photolithographic masks and increase the costs by 20–30% [26].

Using a simpler CMOS process with fewer photomasks and process steps is more attractive. Our in-house CMOS process comprises seven photomasks which yields a more cost-effective solution (Fig. 3a–h) while offering a holistic CMOS-MEMS co-design. The cofabrication procedure uses a MEMS-last processing strategy [27]. In this approach, the MEMS structures are fabricated by depositing and micromachining CMOS-compatible materials on top of the fabricated CMOS electronics.

2.3. CMOS fabrication

A double-polished p-type silicon wafer with ⟨100⟩ of crystallographic orientation and 5 Ω cm of resistivity is used to start the alignment layer (zero layer) definition. A 2-μm thickness of p-type epitaxial layer was grown on the top of the silicon wafer with 1.0e16 ions/cm^3 of boron doping in order to obtain a precise p-dopant concentration required to include NPN bipolar transistors in the CMOS process.

A 20-nm barrier was formed using wet oxidation to screen co-implanted particles. The n-well and the collector area of the NPN bipolar transistor are patterned using the first photomask (Fig. 3a) with a 3.1 μm of photoresist thickness. A 5e12-dose of phosporus implantation at 150 keV of energy is followed by 415 min of annealing for doping redistribution. A 230-nm of oxide is created as a result. An oxide stripping is performed using a buffered hydrofluoric acid (BHF) solution with 1:7 of selectivity. Another dirt barrier oxide layer is grown to process the subsequent steps.

The second photomask is used to define the n-type diffusion areas for the CMOS transistors and the emitter area for the bipolar transistors (Fig. 3b) using 5.0e15 ions/cm^3 dose of arsenic at 40.0 keV of energy. The third photomask defines the p-type diffusion areas for the CMOS as well as the base area of the bipolars (Fig. 3c) using 4.0e14 ions/cm^3 of boron at 20.0 keV of energy. An optimal dose implantation should be investigated here due to the trade-off between the intrinsic current gain of the NPN bipolar devices and the current drive capacity of the PMOS devices.

Next, a threshold voltage adjustment is carried out using a net dose of 20e11 ions/cm^3 at 25.0 keV in the fourth quadrant of the wafer. Subsequently, the dirt barrier oxide is removed using a 1:7 BHF solution, followed by 9 min of wet oxidation for dopant activation and to create the 100-nm of gate oxide. After this step, the threshold voltages for the nMOS and pMOS transistors, in the fourth quadrant, are set to about 2.0 V and −2.5 V, respectively.

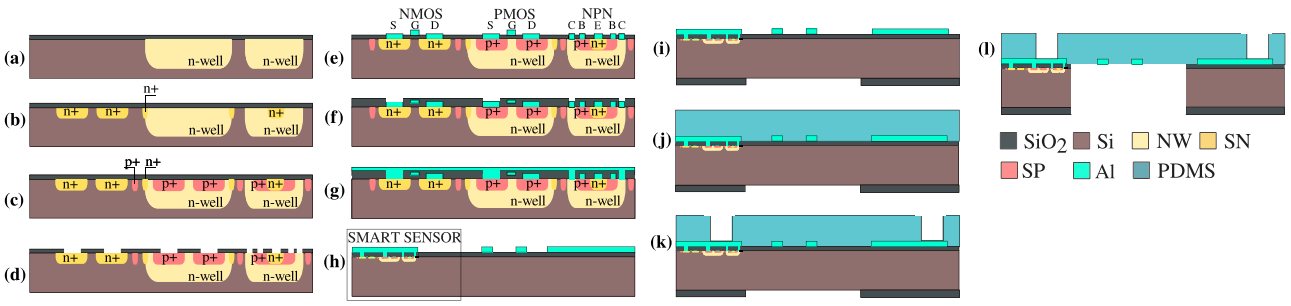

Fig. 3. Fabrication steps in a custom CMOS-MEMS technology for the smart sensor device on the Cytostretch platform. Not to scale.

In the next step (fourth mask), the contact openings are patterned and wet-etched with a 1:7 BHF solution (Fig. 3d). The interconnects and the gate material are created by sputtering 200 nm of AlSi (1%) and patterning with the fifth photomask (Fig. 3e). The 1% of silicon composition in the aluminum avoids spikes in the shallow metal-diffusion interfaces. The process follows with a deposition of 2-μm of SiO_2 using PECVD (plasma-enhanced chemical vapour deposition) at the frontside of the wafer to create at the same time the MIM (metal-insulator-metal) capacitor dielectrics and the stopping mask for the DRIE (deep reactive ion etching) step that defines the PDMS membrane area. To share this process step, a clear trade-off is to be made in the co-design phase. Ideally, the thinner the dielectric of the MIM capacitor the bigger the capacitance, thus, the higher the total capacitance per area. This results in a more area-saving solution. On the other hand, enough oxide thickness headroom should be provided in the DRIE step to ensure a reliable hard mask landing. As a consequence, during the co-design phase, a bigger silicon area has been granted to the MIM capacitor given a minimum of 2-μm thickness of SiO_2 to be used.

The vias are opened using plasma etching after patterning the sixth photomask (Fig. 3f) with photoresist. The second metallization (Fig. 3g) uses a 3.1-μm thickness of sputtered AlSi (1%). This step simultaneously patterns the second level of interconnects of the smart sensor together with the contact pads and the electrical interconnects outside the membrane area of the Cytostrech (Fig. 3h).

2.4. MEMS bulk micromaching

Following the last step of the smart sensor microfabrication (Fig. 3h), a 5-μm PECVD SiO_2 is deposited on the backside of the wafer to prepare the substrate for the DRIE step. The Cytostretch membrane area is then patterned on the same backside by dry etching (Fig. 3j). Subsequently, a 15-μm-thick PDMS layer is spun onto the front of the wafer at 3500 rpm for 30 s and cured for 1 h at 90 °C (Fig. 3j). Next, 300 nm of AlSi (1%) is sputtered at room temperature on top of the PDMS film created. The Al is masked with 4 μm of photoresist (PR) (AZ ECI 3027) and dry-etched (Fig. 3k). The lithography and etching processes used are optimized to circumvent issues caused by the difference between the expansion coefficients of the PDMS and the PR. Besides serving as a hard mask to later expose the electrical contacts, the Al layer reduces the effects of the differences in expansion coefficients by acting as a buffer layer between the PDMS and the PR.

Subsequently, the membrane is released removing the Si and the SiO_2 layers from underneath the membrane using DRIE and BHF, respectively (Fig. 3l). Finally, an etch mixture of phosporic/acetic/nitric acid (PES 77-19-04) is used to remove the aluminium on the top of PDMS and make the membrane fully transparent. This does not remove the Si from the AlSi (1%), though.

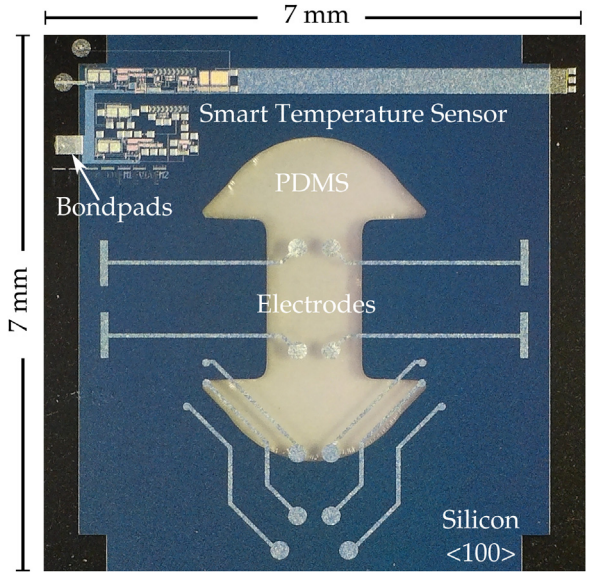

Fig. 4. Smart temperature sensor monolithically integrated on the Cytostretch chip.

3. Experimental

The microfabricated device is shown in Fig. 4. The total chip size is $7 \times 7\ mm^2$ and less than 15% of this area was used for the smart sensor.

Static and dynamic response measurements were carried out to characterize the sensor's performance. The resolution and linearity were extracted by means of a series of static response measurements in which the temperature was maintained constant with respect to time. The dynamic response measurement was used to characterize the sensor's response speed by applying a brief temperature pulse by means of a pre-heated PBS solution.

3.1. Static response: dry measurements

The static response measurements were carried out with a microprobe station which includes a thermal chuck to sweep the temperature of the wafer over the desired range. A commercial PT-100 temperature sensor was attached to the thermal chuck to set a well-calibrated reference and the 4-point probes method was used to measure its resistance changes.

A temperature sweep from 25 to 100 °C with 5 °C increment was carried out in order to measure the responsivity and the nonlinearity of the temperature-to-time conversion. The responsivity and the maximum nonlinearity error obtained from this measurement was 57.1 ns/°C and 0.26%, respectively (Fig. 5).

A temperature measurement over a shorter range (30–40 °C with 1 °C increment) was also performed in order to characterize

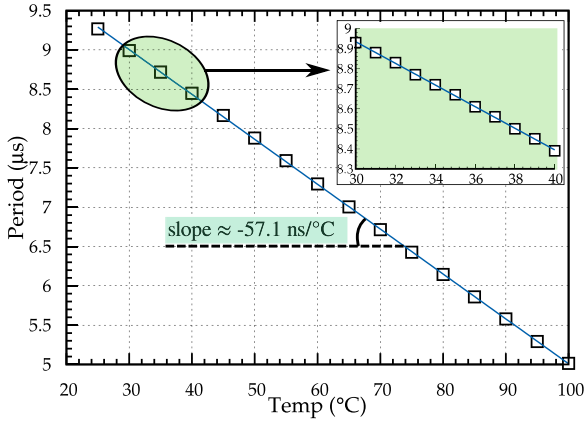

Fig. 5. Temperature-to-time conversion of the smart temperature sensor. The least-squares polynomial regression reveals a 57.1 ns/°C of responsivity.

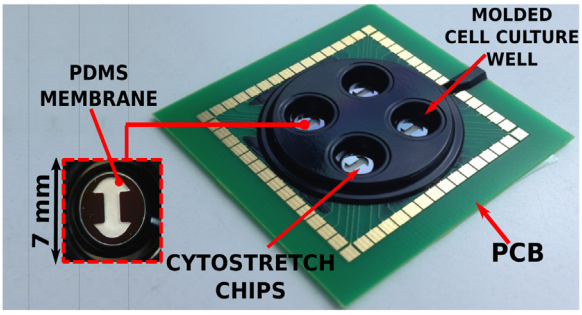

Fig. 6. Cytostrech chips mounted on a PCB containing wells for cell culture experiments.

the sensor's linearity within a temperature span that is closer to the cell culture application. A simple linear regression of the data over this temperature range reveals a 99.988% fit with the linear model. Hence, a 0.05% of maximum nonlinearity error was found over this range.

The jitter is a measure of the deviation of the periodic signal from its true periodicity and it affects the resolution that the sensor can achieve. The total root mean square (rms) jitter was measured at 37 °C for more than 50,000 samples and is equal to 2.78 ns. The sensor's resolution ($\mathcal{R}$) is calculated as the ratio of the jitter for 3σ and the responsivity, and equals:

$$\mathcal{R} = \frac{3 \times 2.78\,\text{ns}}{57.1\,\text{ns/°C}} = 0.15\,°\text{C}(3\sigma), \tag{2}$$

3.2. Dynamic response: wet measurements

To measure the sensor's dynamic response, the wafers were diced and four different dice were assembled on a semi-flexible PCB containing four different wells intended for cell culture experimentation (Fig. 6).

The measurements were initiated with the ambient temperature at 28 °C (±0.5 °C) and after approximately 15 s the wells were filled with 0.4 ml of PBS (Phosphate-buffered saline) solution pre-heated to a temperature of 32 °C. Here, three different time constants are involved in the heat transfer exchange (Fig. 7): (1) the time constant associated with the convection-cooling mechanisms between the medium and the ambient temperature (τ_1), (2) associated with the thermal conduction happening at the interface between the medium bulk and the silicon crystal lattice (τ_2), (3) and associated with the intrinsic delay between the silicon lattice and the sensor itself (τ_3).

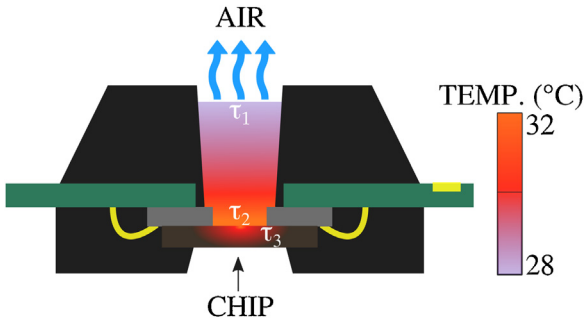

Fig. 7. Different time constants involved on the heat transfer of the system. Time constant τ_1 happens between the medium and the ambient temperature, τ_2 between the medium and the silicon lattice and, τ_3, between the silicon and the sensor.

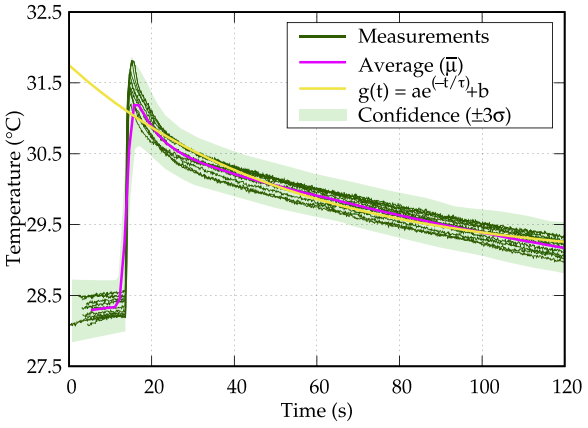

Fig. 8. Dynamic response of the sensor to a brief temperature pulse.

The result of this measurement is plotted in Fig. 8 for ten different measurements (dark green lines) taken at different times within a day. The pink line on this curve indicates the mean value calculated for these 10 samples, whereas the shaded light green regions encompasses the $\pm 3\sigma$ confidence level around the mean.

An exponential curve is also fitted on the data to indicate the tendency of the samples. From this curve, the time constant associated with the heat loss between the medium and the ambient (τ_1) has been extracted and it is roughly 50 seconds. The cumulative time constant ($\tau_2 + \tau_3$) associated with thermal conduction in the silicon and the sensor's response has also been derived from the slope in the curve around $t = 15$ s, and it is on average 1.5 s.

The ratio of the thermal resistances due to conduction between the medium and the silicon surface compared to the thermal resistance due to the heat loss mechanisms give an indication of the Biot number. This dimensionless quantity was calculated to be about 0.03 and it implies that the heat conduction inside the body is much faster than the heat convection away from its surface, and temperature gradients are negligible inside of it. Having a Biot number smaller than 0.1 labels a substance as "thermally thin", and temperature can be assumed to be constant throughout the material's volume.

4. Results and discussion

The results presented in the previous section demonstrate the capability of monolithically integrating CMOS functionality in silicon-based OOC devices for real-time *in situ* temperature measurements of the cell culture. Our in-house CMOS technology has been used as a research tool for the proof of concept. This has been the first step to realize OOCs with integrated CMOS functional-

ity for multi-sensing many other different physical quantities (pH, glucose, glutamate, growth factors, etc.) in the cell culture. As the number of sensors in the platform increases, more correlations can be performed for stoichiometric optimizations of the culture.

Previous literature has extensively used commercial sensors for this purpose, which are not compact, not scalable and do not allow for high density multi-sensing integration.

We expect that the use of more advanced CMOS technological nodes can enable very large scale of multi-sensing integration and actuation in a closed-loop system. To that end, the sensors shall yield the necessary accuracy and respond fast enough for the application.

For instance, the results obtained with the dynamic response measurements indicate that the sensor's response (≈1.5 s) is much faster than the time it takes to elapse one time constant (≈50 s) of the convection-cooling mechanism. In this case, the sensor could be incorporated in a closed-loop configuration with local heaters to keep the *in situ* temperature as close as possible to its reference for the maximum time when outside the incubator.

In addition, the curve obtained from the cooling mechanism indicates that the rate of heat loss in the medium where the cells are cultured tends to follow an exponential decay and it is proportional to the temperature difference between the medium and its surroundings. Such result is also a relevant information to the biologists during the time the culture is outside the incubator for inspection.

With respect to the results found in the static measurements, the sensor's resolution (0.15 °C and linearity suggest that the sensor can potentially monitor temperature increments of the culture that could give an indication of the metabolic growth rate as a result of the heat dissipated due to enthalpy changes [28].

It is important to notice that the sensor's circuit design is not optimized for best performance. Therefore, circuit improvements can be made to achieve better resolution or responsitivity, if needed. Regarding the microfabrication challenges, care must be taken when processing materials such as PDMS. After etching, residues may still remain at the surface which can hamper further system-level integration processes such as wire bonding. Non-selective over-etching, on the other hand, might partially or completely remove the materials beneath. Hence, process optimization during the etching phases is of paramount importance for the reliability and reproducibility of the end product.

5. Conclusions

Cell cultures are maintained at an appropriate temperature and gas mixture inside a cell incubator. Because the *in situ* culture conditions may vary, especially when the culture is outside the incubator, it is advantageous to construct OOCs that are equipped with sensors that can accurately measure in real-time the *in situ* conditions of the cells.

In this work, we investigated the monolithic integration of a CMOS smart temperature sensor in our MEMS OOC device. By combining CMOS and MEMS technology monolithically, it is possible to create OOCs to accommodate the cells over different MEMS structures while integrating high-density CMOS electronics for very compact systems that can measure *in situ* physical quantities in the culture medium.

The CMOS-MEMS cofabrication method used here yielded, for the first time, an OOC device with integrated CMOS sensing functionality for a real-time *in situ* temperature measurement of the cell culture. Our in-house CMOS technology has been used as a research tool for the proof of concept.

Moreover, as a result of sharing common process steps and by minimizing the number of CMOS masks used, a more cost-effective and scalable solution is obtained. In order to meet specific requirements of both technologies, a holistic co-design phase has been followed so the trade-offs between circuit performance and micromaching reliability are taken into consideration.

Measurement results of our smart temperature sensor indicate that temperature increments of 0.2 °C can be accurately monitored. This could potentially be used to give an indication of the metabolic growth rate when the culture is inside the incubator. The sensor's time response found was approximately 1.5 s which is much faster than the time it takes for the temperature of a 0.4 ml medium to drop by 1 °C.

This work is the first step towards constructing OOCs with integrated CMOS electronics for multi-sensing relevant information in the cell culture (O_2, CO_2, pH, glucose, glutamate, grow factors, etc.). It is expected that the use of more advanced CMOS nodes may enable powerful OOCs with a very large degree of multi-sensing integration and actuation in a closed-loop system manner.

Authors' contribution

Ronaldo Martins da Ponte: main investigator, writing – original draft preparation, conceptualization, methodology, measurements, formal analysis, data curation, visualization, funding acquisition. Nikolas Gaio: conceptualization, resources, methodology support, reviewing original draft. Henk van Zeijl: methodology support, resources, reviewing original draft. Sten Vollebregt: methodology support, resources, measurement support, reviewing original draft. Paul Dijkstra: resources. Ronald Dekker: conceptualization, resources, project administration. Wouter A. Serdjin: conceptualization, supervision, resources, funding acquisition, project administration, reviewing original draft. Vasiliki Giagka: conceptualization, supervision, resources, funding acquisition, project administration, reviewing original draft.

Conflicts of interest

There are no conflicts to declare.

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