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Investigations of SiC VDMOSFET With Floating Island Structure Based on TCAD

Hou-Cai Luo, Li-Ming Wang, Shao-Gang Wang, Chun-Jian Tan, Kai Zheng, Guo-Qi Zhang, *Fellow, IEEE*, Lu-Qi Tao, and Xian-Ping Chen, *Member, IEEE*

***Abstract*— Using TCAD simulations, the silicon carbide metal–oxide–semiconductor field-effect transistor with p-type floating islands (SiC FLIMOSFET) is systematically investigated in this paper. The doping concentration (N_{FLI}), length (L), and position (D1) of floating islands are optimized according to breakdown voltage (BV), electric field distribution, and on-resistance. The results show that $N_{FLI} = 1 \times 10^{17}$ cm^{-3}, L = 2.5 μm, and D1 = 9.0 μm are superior values for FLI structure considering tradeoff between BV and on-resistance. With the same BV capacity, the on-resistance of SiC FLIMOSFET is decrease by 32% comparing to the conventional SiC VDMOSFET. Besides, the dynamic property shows 16.5% reduction of FoM $R_{on} \cdot Q_{GD}$ in the SiC FLIMOSFET. Significantly, comparing to the conventional structure, the electro-thermal simulation indicates that the SiC FLIMOSFET has a higher robustness under short-circuit condition owing to the reduction of thermal stress in SiC/SiO_2 interface. All the results show that the SiC FLIMOSFET has a good potential in SiC power device.**

***Index Terms*— Breakdown voltage (BV), electro-thermal simulation, ON-resistance, silicon carbide metal–oxide–semiconductor field-effect transistor with p-type floating islands (SiC FLIMOSFET), TCAD.**

I. Introduction

SILICON carbide metal–oxide–semiconductor field-effect transistor (SiC MOSFET) has become one of superior candidates for replacing silicon insulated gate bipolar transistor (Si IGBT) due to its high critical field and wide bandgap [1]–[3]. These fascinating properties not only enable the SiC MOSFET at the voltages and power levels similar to Si IGBT but also make a capability with systems decrease in size and higher operation temperature [2], [4], [5]. In these years, SiC VDMOSFETs have been visual in SiC power electronic device markets due to the development of semiconductor manufacturing technology [6], [7]. However, many issues still need to be studied. The voltage capability of VDMOSFET structure is given by the breakdown voltage (BV) of the "P-based/N^- drift region" junction, meaning that a lowly doped and thick drift region are required to realize high voltage, whereas it leads to a large ON-resistance (R_{on}) [8], [9]. Besides, how to improve the robustness of gate oxide under extreme condition such as short-circuit is also a key issue for SiC VDMOSFET. Previous efforts show that the gate oxide is degraded from excess thermal stress located at SiC/SiO_2 interface, which is one of the primary failure mechanisms in series SiC VDMOSFET products under short-circuit [10]–[12].

Recently, VDMOSFET structure with floating islands (FLI) was proposed in silicon device in order to make a tradeoff between BV and R_{on} by inserting p-type doping floated islands in lightly doped region [13]–[15]. With the same doping concentration in drift region, FLIMOSFET can sustain higher BV than the conventional VDMOSFET. However, this structure has not received much attention due to development of silicon super junction MOSFET [16], [17]. The super junction structure exhibits more fascinating tradeoff between electrical performance and cost in silicon because of its mature epitaxial technology. But there are some differences in SiC. The epitaxial technology is immature and the cost is high [18]–[20], thus the FLI structure exhibits a good potential for high-voltage power device in SiC [14], [21]. Significantly, we noted that the investigation of SiC FLIMOSFET is not reported.

In this paper, the optimization and properties of SiC FLIMOSFET were systematically studied by Technology Computer Aided Designed (TCAD) simulations. The doping concentration, length, and position of FLI were optimized. Besides, the gate charge in SiC FLIMOSFET was also calculated to investigate its dynamic properties. Electro-thermal simulation was calculated to study the robustness of SiC FLIMOSFET under short-circuit.

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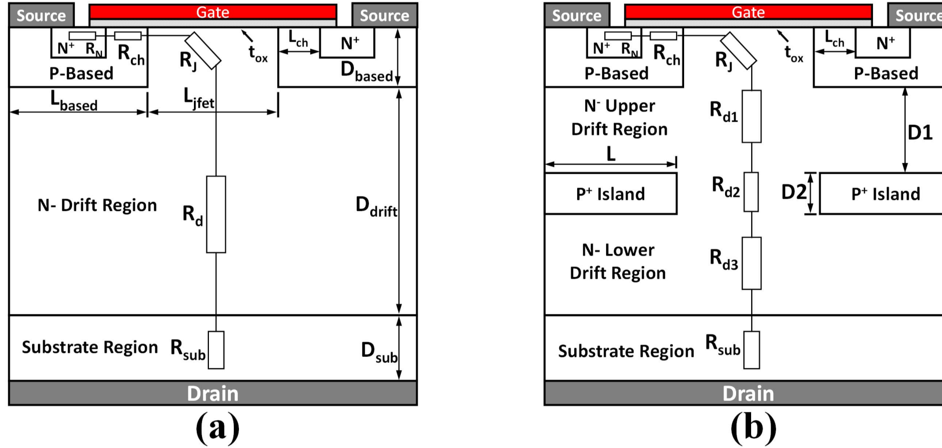

Fig. 1. Schematic structures of conventional (a) SiC VDMOSFET and (b) SiC FLIMOSFET used in simulations and their location of the on-resistance components.

TABLE I
OPTIMIZED STRUCTURE PARAMETERS OF SiC VDMOSFET USED IN SIMULATION

Parameter	Value
Thickness of N^- drift region, D_{drift}	16 μm
Doping concentration of N^- drift region, N_{drift}	$1e^{16}$ cm^{-3}
Thickness substrate region, D_{sub}	6 μm
Doping concentration of substrate region, N_{sub}	$1e^{19}$ cm^{-3}
Thickness of P-Based region, D_{based}	2 μm
Doping concentration of P-Based region, N_{based}	$1e^{18}$ cm^{-3}
P-Based length, L_{based}	2.6 μm
N^+ region concentration, Nn^+	$1e^{19}$ cm^{-3}
Chanel length, L_{ch}	0.5 μm
JFET width, L_{jfet}	2.8 μm
Thickness of gate oxide, t_{ox}	0.05 μm

II. DEVICE STRUCTURE AND SIMULATION

The schematic structures of conventional SiC VDMOSFET and novel SiC FLIMOSFET are shown in Fig. 1(a) and (b), respectively. For SiC FLIMOSFET, it has the same structural parameters with SiC VDMOSFET except the geometric parameters of the FLI. The additional geometric parameters contain doping concentration of p-type FLI (N_{FLI}), length (L), and position (D1) which is defined by the minimum distance between FLI and P-based junction. In order to make an easy comparison between SiC VDMOSFET and SiC FLIMOSFET, the diagrams of resistance in each region are presented in the photograph. In this paper, all parameters in SiC VDMOSFET are optimized in order to make a better investigation for FLI parameters, which are listed in Table I.

The two structures mentioned above are simulated using TCAD which is based on semiconductor theory, and the simulation results are mainly dependent on the selection of physical models [22]. In this paper, the simulated physical models included Schockley–Read–Hall (SRH) and the auger (AUGER) recombination model [23]. Considering high doping concentration in substrate and source region, the bandgap narrowing model (BGN) was implemented. The mobility models included Caughey Thomas analytic model (ANALYTIC) and the velocity-dependent mobility model (CVT) were also used. The incomplete ionization model was performed since the doped impurities in 4H-SiC material have larger activation energy than the thermal energy at normal temperature. The anisotropic impact model was also implied to calculate the breakdown characteristic. All the parameters of selected models are used from references [24]–[26].In addition, considering that the simulated SiC VDMOSFET and SiC FLIMOSFET both are power electronic devices, the self-heating effect was also employed in electro-thermal simulation [27]. The thermal boundary equals with environmental temperature, i.e., 300 K.

III. RESULTS AND DISCUSSION

In this section, we calculated the breakdown characteristic in conventional SiC VDMOSFET and extracted the peak electric field (E_{peak}) in semiconductor region during avalanche breakdown. According to the simulation results, the BV is about 1770 V and the E_{peak} is 2.82 MV/cm, as shown in Fig. 2(a). For the SiC FLIMOSFET, the N_{FLI} of FLI has a significant influence on BV and E_{peak}. In this paper, different N_{FLI} of FLI under conditions of $L = 2.0$ μm and D1 = 8.0 μm were simulated, seen in Fig. 2(a). Clearly, with the doping concentration increase from 0 to 5×10^{17} cm^{-3}, 0 means SiC VDMOSFET structure, the highest BV is 2840 V corresponding to $N_{FLI} = 1 \times 10^{17}$ cm^{-3}, in which the E_{peak} is about 3.02 MV/cm. An interesting phenomenon should be noticed that the E_{peak} is up to 3.04 MV/cm, while the BV is only 2250 V corresponding to $N_{FLI} = 5 \times 10^{16}$ cm^{-3}. It could be explained that the P-based junction is still the main region to sustain the electric field before avalanche breakdown while the FLI is useless. Thus, the E_{peak} is still at P-based junction at this case. In order to further investigate the E_{peak} location, the electric field distributions with series doping concentrations were extracted at X = 2.5 along y-axis from 0 to 24 μm, as shown in Fig. 2(b). Clearly, two gathering areas of electric field are located at P-based junction and FLI lower region respectively, corresponding to the peak values of electric field. Although the extracted location does not locate at the FLI

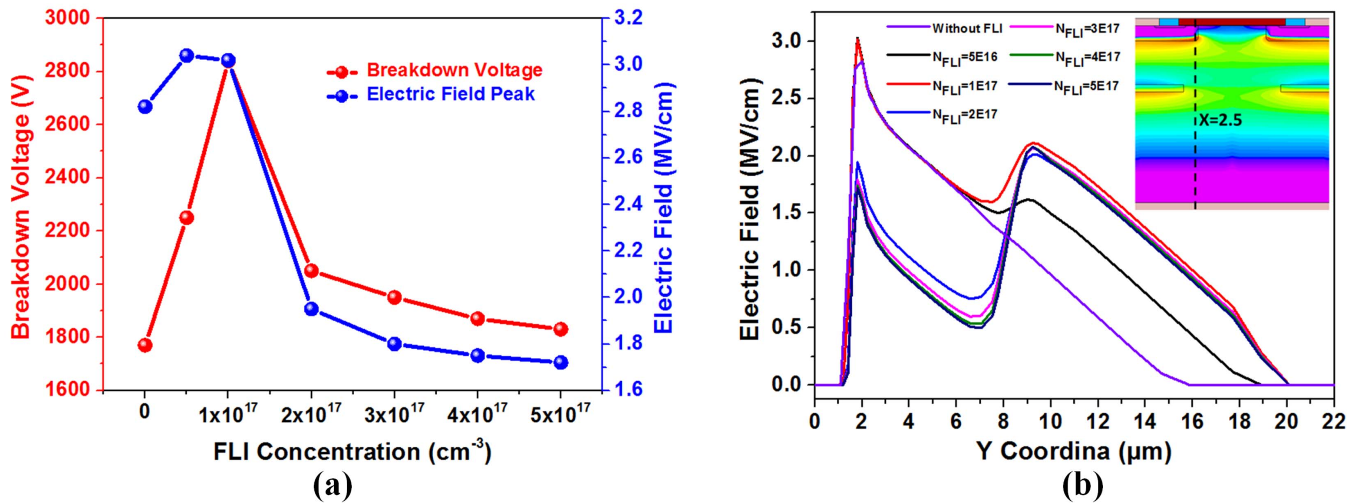

Fig. 2. (a) BV and E_{peak} of SiC FLIMOSFET for different FLI concentration. $N_{FLI} = 0$ corresponds to SiC VDMOSFET. (b) Electric field distribution of SiC FLIMOSFET along the *y*-direction at X = 2.4 μm at the avalanche BV. The inserted photograph corresponds to breakdown electric field formation for $N_{FLI} = 1e17cm^{-3}$.

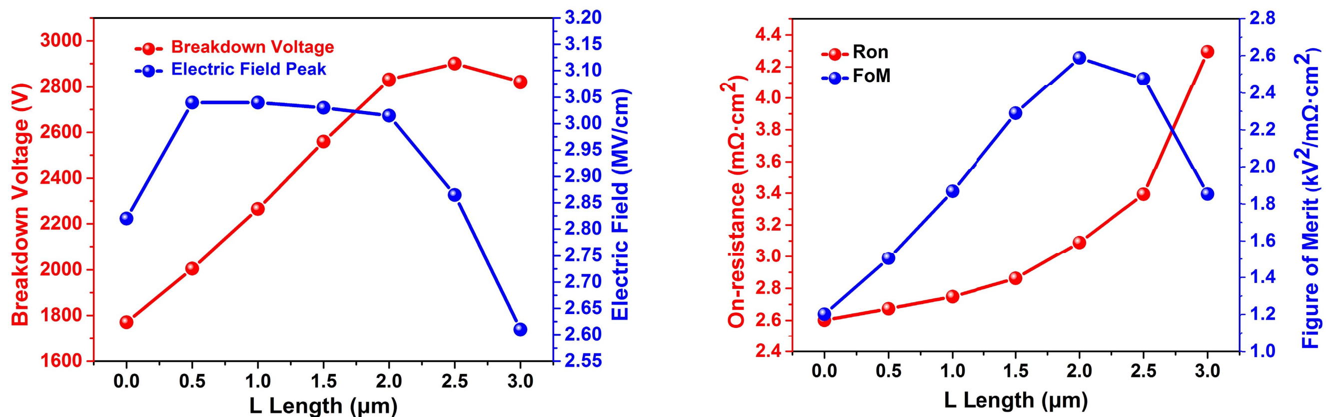

Fig. 3. BV and E_{peak} of SiC FLIMOSFET for different FLI length. $L = 0$ corresponds to SiC VDMOSFET structure.

Fig. 4. Figure of merit (FoM BV^2/R_{on}) of SiC FLIMOSFET for different FLI length.

region, the variation of E_{peak} is also interpretable. As seen in the photograph, the E_{peak} transfers from P-based junction to FLI junction with increase of N_{FLI}, corresponding to dramatic decrease of BV in Fig. 2(a). The reason is that the higher doping concentration means a thicker depletion width under zero bias condition, and the depletion boundary of these FLI junctions would increase high bias voltage. As a result, the electric field strength in P-based region dramatically decreases comparing to those of FLI with light doping concentration. According to the calculation, 1×10^{17} cm^{-3} is a suitable value for FLI doping.

In order to seek the optimal value of FLI length [i.e., L at Fig. 1(b)] in SiC FLIMOSFET, the BV and corresponded E_{peak} with series L values ranged from 0 to 3 μm under conditions of $N_{FLI} = 1 \times 10^{17}$ cm^{-3} and D1 = 8.0 μm were investigated. The results are shown in Fig. 3. Clearly, the BV increases with the increment of L from 0 to 2.5 μm, while it decreases at the case of $L = 3.0$ μm. The largest BV is revealed when $L = 2.5$ μm, which is about 2900 V corresponding to the E_{peak} of 2.86 MV/cm. However, the L of FLI has a significant influence on R_{on}. In order to seek a desirable trade-off between BV and R_{on}, the R_{on} and figure of merit (FoM BV^2/R_{on}) were also calculated, as shown in Fig. 4. As shown in Fig. 4, the R_{on} continually increases with increment of L. Notably, a sharp increment is appeared at $L = 3.0$ μm. It would be explained by that longer L means more narrow path of current at ON-state, leading to dominance of R_{d2} [see in Fig. 1(b)] in total resistance. The FoM BV^2/R_{on} calculation shows that a superior tradeoff between BV and R_{on} is exhibited when $L = 2.0$ μm. However, some discussions between $L = 2.0$ μm and $L = 2.5$ μm still need to be intensively analyzed.

The BV and the E_{peak} of SiC FLIMOSFET versus FLI position [i.e., D1 at Fig. 1(b)] at the avalanche point were calculated for $L = 2.0$ μm and $L = 2.5$ μm. Meanwhile, $N_{FLI} = 1 \times 10^{17}$ cm^{-3} was selected. The results are shown in Fig. 5(a). For the case of $L = 2.0$ μm, the highest BV about 2830 V is revealed at the position of D1 = 8.0 μm corresponding to the E_{peak} of 3.015 MV/cm. Besides, with the FLI position increase from 8.0 to 11.0 μm, the E_{peak} strength almost keeps in a constant about 3.03 MV/cm, while the BV decreases. However, in case of $L = 2.5$ μm, the BV increases with the increment of D1 arranged from 7.0 to 9.0 μm and

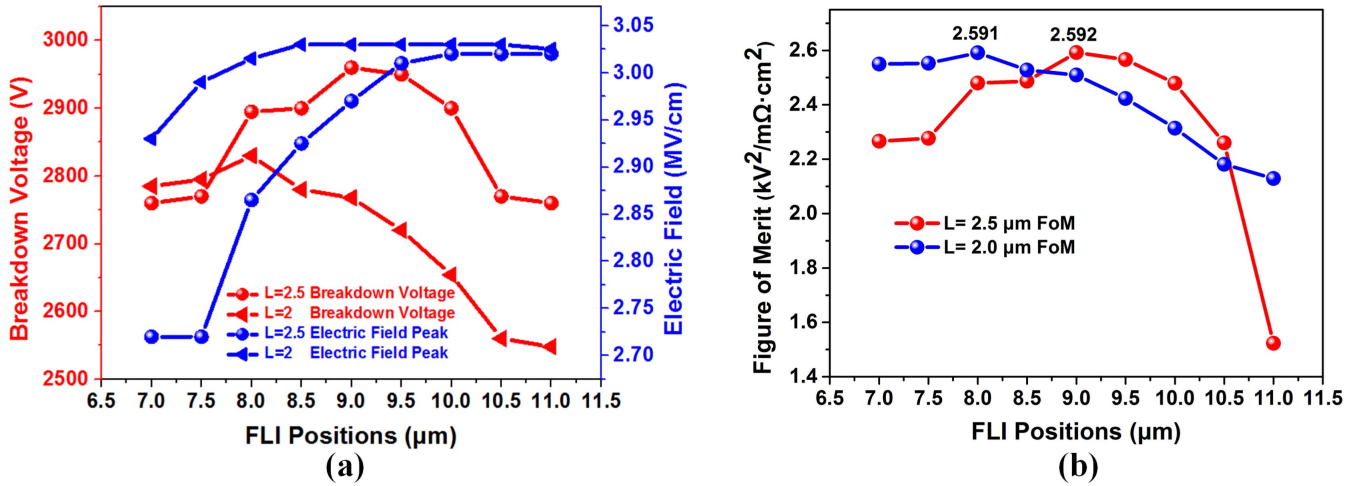

Fig. 5. (a) BV of SiC FLIVDMOSFET and electric field peak strength. (b) FoM (BV^2/R_{on}) for different FLI positions [D1 value in Fig. 1(b)] when $L = 2\ \mu$m and $L = 2.5\ \mu$m.

then decreases with the D1 growth. The E_{peak} is increased gradually in all positions of FLI. The highest BV about 2960 V corresponded to the E_{peak} of 2.97 MV/cm is revealed at D1 = 9.0 μm, which is about 130 V larger than that of $L = 2.0\ \mu$m. Furthermore, the FoM BV^2/R_{on} in the cases of different D1 are calculated when $L = 2.0\ \mu$m and $L = 2.5\ \mu$m, as shown in Fig. 5(b). The FoM BV^2/R_{on} for $L = 2.0\ \mu$m is revealed when D1 = 8.0 μm, which is 2.591 kV^2/m$\Omega\cdot$cm^2. However, an optimal FoM BV^2/R_{on} about 2.592 kV^2/m$\Omega\cdot$cm^2 in the case of $L = 2.5\ \mu$m is exhibited when D1 = 9.0 μm. Therefore, the doping concentration, length, and position parameters of the FLI in SiC FLIMOSFET are 1×10^{17} cm^{-3}, 2.5 μm, and 9.0 μm, respectively. Moreover, with the same BV capacity (i.e., BV = 2960 V in this paper), the R_{on} of conventional SiC VDMOSFET is 4.975 m$\Omega\cdot$cm^2, while the optimal SiC FLIMOSFET is 3.383 m$\Omega\cdot$cm^2, which is decrease by 32%.

In order to investigate the optimized structure of SiC FLIMOSFET in dynamic characteristics, the gate charge was calculated. Simultaneously, the gate charge of the conventional SiC VDMOSFET with the same voltage capacity, i.e., BV = 2960 V, was also calculated. All the results and the test circuit are presented in Fig. 6. The I_{out} is a constant current source which provides a constant dc current and the V_{in} represents a constant voltage source. Because of unidirectional conductivity of diode, the V_{in} only provides a 20 V potential. Thus, the current flow through drain to source is only from I_{out}. The charge of gate electrode can be calculated by the integration between gate current and test time. According to the simulation, the gate–drain charge of the conventional SiC VDMOSFET is smaller than that of SiC FLIMOSFET, which are 156.8 and 192.5 nC/cm^2, respectively. It is because a parasitic p-n junction capacitance is introduced by FLI, which leads to a larger capacitance in SiC FLIMOSFET comparing with the conventional SiC VDMOSFET. However, the FoM $R_{on} \times Q_{GD}$ is a critical parameter to estimate the tradeoff between switching frequency and switching loss. The

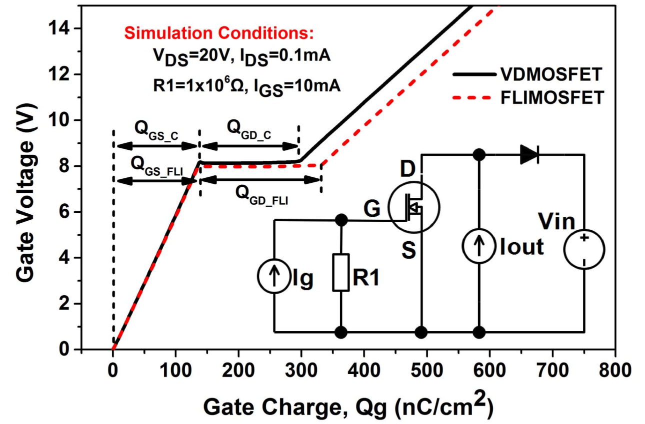

Fig. 6. Gate charge calculation of SiC FLIMOSFET and conventional SiC VDMOSFET structure.

FoM $R_{on} \times Q_{GD}$ for the SiC FLIMOSFET and conventional SiC VDMOSFET structure are 651.23 and 780.08 m$\Omega\cdot$nC, respectively. It is decreased by 16.5% in the SiC FLIMOSFET, meaning more excellent performance between switching frequency and switching loss.

Furthermore, thermal stress is one of the critical factors to be considered in power electronics. In order to investigate the effect of the FLI structure on thermal stress in SiC MOSFET, the electro-thermal simulation was calculated under short-circuit condition. The results are shown in Fig. 7(a). The inserted picture indicates the simulated schematic circuit, in which an 100-V dc voltage source, 10-nH inductance and 10-mΩ resistance are performed. A transient pulse is employed on gate to frequently drive the gate action. As shown in Fig. 7, the drain current has a large overshoot in start and then declines continually during operation. However, the device temperature almost keeps in constant lasted 0.5 μs during short-circuit, as labeled a and b in the picture, which is different from the conventional SiC VDMOSFET according to

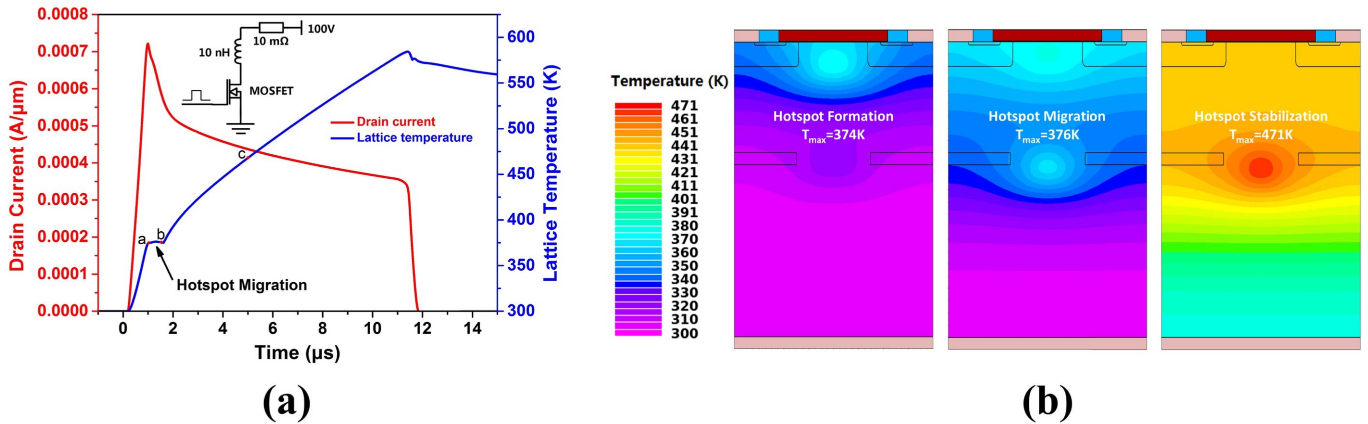

Fig. 7. (a) Drain current and lattice temperature for SiC FLIMOSFET under short-circuit condition. (b) Temperature distribution and hotspot positions at time of 1.0, 1.5, and 5.0 μs during short-circuit, respectively.

previous reports [12], [28]. A conjecture is proposed that during this period, a hotspot forming at JFET region migrates to the middle area of the two FLI regions and results in the highest temperature of the device almost remaining unchanged. In order to investigate the mechanism of hotspot migration, lattice temperature distributions at 1.0, 1.5, and 5.0 μs during short-circuit are extracted, as shown in Fig. 7(b), corresponding to points a, b, and c in Fig. 7(a), respectively. The phenomenon could be explained from the wider depletion boundary of FLI junction than P-based junction after gate turning on, and thus, the current density between two FLI regions is larger than that in JFET region. In other words, lower current density in JFET region means lower dissipation. It is different from the case of conventional SiC VDMOSFET that the hotspot migrates from JFET to gate oxide during short-circuit transient and increases thermal stress in SiC/SiO_2 interface [29]. As a result, the SiC FLIMOSFET structure has a higher robustness than the conventional SiC VDMOSFET under short-circuit owing to lower thermal stress in SiC/SiO_2 interface.

IV. Conclusion

In this paper, the silicon carbide MOSFET with FLI structure (SiC FLIMOSFET) is investigated by using TCAD simulations. Physical models included carrier recombination models, mobility models, impact model, and self-heating effect are considered to obtain considerable calculation accuracy. The parameters of FLI structure included doping concentration, length, and position are systematically analyzed. The results show that $N_{FLI} = 1 \times 10^{17}$ cm^{-3}, $L = 2.5$ μm, and D1 $= 9.0$ μm are the optimal values for SiC FLIMOSFET considering tradeoff between BV and ON-resistance. Significantly, SiC FLIMOSFET specific ON-resistance decreases by 32% compared to the conventional SiC VDMOSFET under condition of the same BV capacity. Besides, the FoM $R_{on} \times Q_{GD}$ is decreased by 16.5% in SiC FLIMOSFET meaning more excellent performance between switching frequency and switching loss. The electro-thermal simulation shows that the thermal stress at SiC/SiO_2 interface is reduced in SiC FLIMOSFET compared to the conventional structure under short-circuit condition.

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