Improving Metastability in Synchronous SAR ADCs

by

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Summary

This thesis focuses on the design and optimization of Successive-approximation (SAR) Analog-to-Digital Converter (ADC), with a primary focus on enhancing the Bit Error Rate (BER). SAR ADCs are widely used in various applications due to their power-efficient characteristics. The critical point addressed in this research is improving the BER of synchronous SAR ADCs without the necessity to reduce the sampling speed.

The primary innovation presented in this work is a modified SAR loop featuring a dual Digital-to-Analog Converter (DAC) structure. This architecture aims to reduce the probability of metastable errors in the output code, which occur when the comparator fails to resolve its input within the allocated time.

An in-depth analysis of the comparator, amplifier, capture latch, and DAC elements is conducted to identify and address non-idealities affecting the performance. The research demonstrates a significant reduction in BER by incorporating a metastability detection circuit with the dual-DAC architecture. This approach allows the system to solve metastable events parallel to the SAR loop, improving the overall reliability of the output code without slowing down the SAR loop.

Theoretical models are proposed to validate the proposed solutions' effectiveness, highlighting the practicality and feasibility of the design enhancements. The simulation results demonstrate a substantial improvement in BER. This thesis's implementation strategies and techniques provide a framework for designing Dual-DAC SAR ADCs.

In conclusion, this thesis contributes to the field of high-speed digital converters by presenting innovative solutions to enhance the BER of the SAR ADC. The findings improve our understanding of managing metastability in ADCs and pave the way for future advancements in ADC technology. The methodologies and insights gained have the potential to impact the development of more robust and efficient ADC systems.

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Acronyms

ADC Analog-to-Digital Converter. ii, v–vii, 1–3, 19, 21, 24–27, 43, 44, 48–52, 57, 58, 64

BER Bit Error Rate. ii, vii, 1–4, 8, 9, 20, 29, 43, 45–51, 53, 63, 64

CAP-DAC Capacitor DAC. 52, 56–59

DAC Digital-to-Analog Converter. ii, v–vii, 2, 3, 14–22, 24–27, 29, 33, 35, 37–46, 48–52, 56–64

DNL Differential Nonlinearity. 58

DR Dynamic Range. 52

FS Full-Scale. 43, 52

INL Integral Nonlinearity. 58

LSB Least Significant Bit. viii, 19, 21, 46–49, 53, 57–59

MOM-capacitor Metal-Oxide-Metal Fringing capacitor. 59

MSB Most Significant Bit. 19, 25, 46, 57–59

PDF Probability density function. 47

RS-latch Reset/Set Latch. 35–38

SAR Successive-approximation. ii, v–vii, 2–5, 8, 9, 13, 14, 17, 21, 22, 25, 26, 31, 32, 35, 39, 43, 44, 48, 49, 51, 52, 64

TI-SAR time-interleaved SAR. 2

Chapter 1

Introduction

In today's modern society, communication systems are inescapable. Almost every person interacts with these systems on a daily basis, often without even realizing it. Engagements such as Internet usage, sharing digital images, and scheduling appointments are fundamental to modern life. A world without these systems seems like a distant past. These everyday communication systems face numerous challenges due to the necessity to process analog signals despite being within inherently digital frameworks. An ADC is essential to bridge this gap in various applications. High-speed and high-resolution ADCs are critical components, frequently employed in Ethernet networks within data centers and even in residential environments where Ethernet is used for tasks such as printing or accessing networked files. Fundamentally, these systems comprise a transmission and reception apparatus, as depicted in Fig. 1.1.

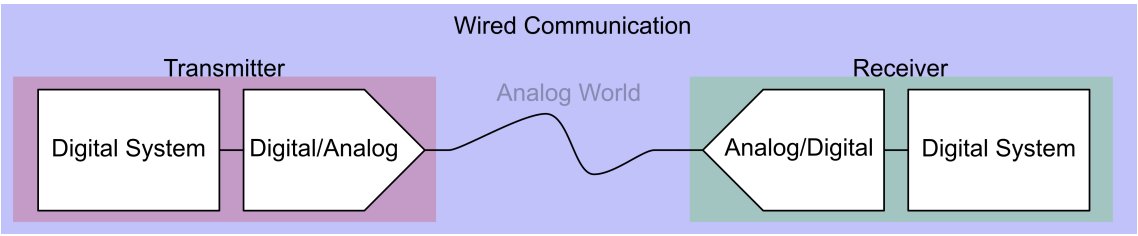


Figure 1.1: A one-way communication network between two digital systems

An essential requirement for all these communication systems is a good BER, which quantifies the number of bit errors relative to the total transmitted bits, indicating the integrity of the data. A system-level bit error occurs when the bit received in the digital domain at the receiver does not correspond to the digital code transmitted on the transmitter side. Maintaining a low BER is mandatory to ensure reliable communication. This necessity is particularly critical in applications

such as communication systems, where even minimal errors can significantly degrade operational performance.

Various types of ADCs are used to transition from the analog to the digital domain, each with strengths and weaknesses. One of the most popular architectures is SAR ADC. This architecture represents a robust architecture within the ADC landscape and is used in a broad spectrum of applications. Obtaining the lowest power consumption throughout the resolution range, as illustrated in Fig. 1.2. Focusing on high-speed and high-resolution ADCs, synchronous and asynchronous SAR ADCs are used as single ADC solutions. In recent years, there has been a transition from SAR-ADCs to time-interleaved SAR (TI-SAR) and pipelined-SAR ADCs for enhanced performance compared to the SAR-only architecture [1]. These architectures employ synchronous and asynchronous SAR-ADCs as fundamental systems components. Therefore, this study will focus mainly on improving BER of synchronous SAR ADCs, thus improving SAR ADCs and laying the foundation for new and improved pipelined and TI-SAR ADCs.

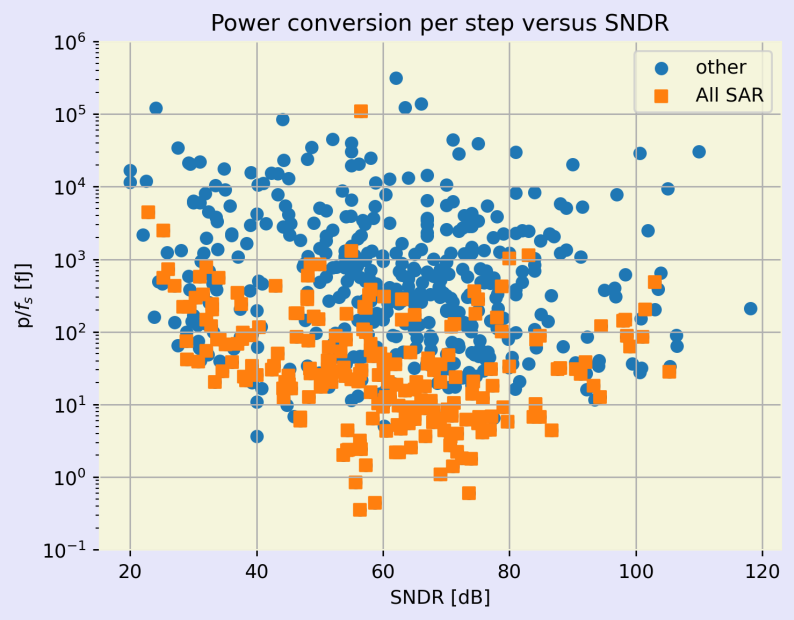


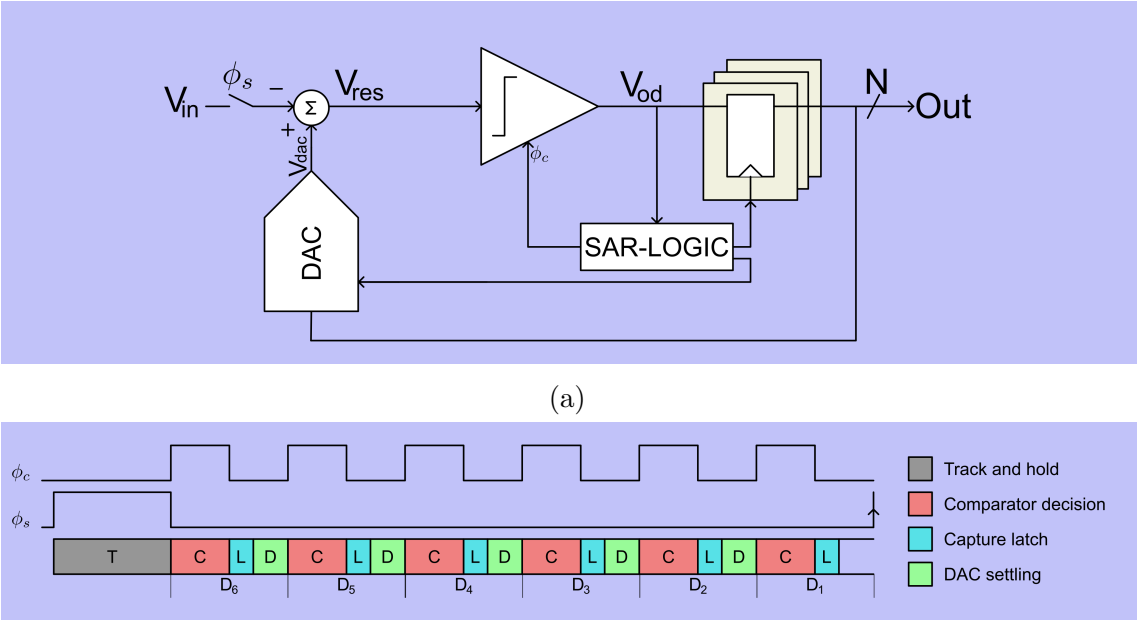
Figure 1.2: ADCs taken from [1], power consumption versus SNDR

1.1 Synchronous SAR ADC

A synchronous SAR ADC consists of four main building blocks: a sample and hold, a DAC, a comparator and the SAR logic/memory, as illustrated in Fig. 1.3a. In Fig. 1.3b shows the corresponding timing response of the building blocks.

The SAR cycle starts with the sampling phase, indicated by the gray-shaded region identified as the tracking period. Once the voltage has been sampled on the

DAC, the comparator makes a comparison, indicated by the red rectangle in Fig. 1.3b. The output of the comparator is copied to the corresponding capture latch, indicated by the blue rectangle. Finally, the green rectangle shows an incremental step on the DAC. This comparison cycle is repeated N times, with N being the number of bits of the SAR-ADC, Fig. 1.3a shows a 6-bit ADC.



(a)

(b)

Figure 1.3: (a) A synchronous SAR ADC block diagram. (b) Timing diagram of the synchronous SAR ADC.

A fundamental aspect of the system is the interaction between the building blocks. The comparator has a finite time to accumulate gain, during which the capture latch remains transparent to the output of the comparator. In the subsequent phase, the comparator undergoes a reset while the capture latch stores the digital output of the comparator in the latch. The DAC proceeds with a step if the comparator output is valid.

As stated above, BER serves as an important metric for the integrity of the system's data. To estimate BER for the synchronous SAR ADC, a case where a bit error occurs must be studied. As an initial approximation, the comparator and the capture latch can be modeled as positive feedback blocks [2], exponentially building up a gain over time. When the comparator input voltage, denoted by V_{res} in Fig. 1.3a, is close to the comparator tripping voltage. More time is required to accumulate sufficient gain for a valid output. Given the SAR-loop architecture, which inherently constrains the available time, insufficient time may result in a no-decision, yielding a bit error in the output code. Essentially, a BER can be led back to a finite time in which the comparator's input signal was too close to the tripping point, resulting in

no decision from the comparator. The next chapter will provide a comprehensive analysis of metastability within the comparator.

1.2 Scope of the report

This thesis aims to improve the overall BER for synchronous SAR ADCs by fundamentally creating more time inside the SAR-loop for metastable events without slowing down the overall SAR loop.

The remainder of this thesis is organized as follows. Chapter 2 will focus on the comparator. Chapter 3 discusses a method for detecting metastability of a comparator. Chapter 4 incorporates the metastability detection circuit within the SAR-loop to mitigate THE BER of the system. Chapter 5 elaborates on the operational constraints imposed by dual-DAC configurations. Chapter 6 provides an in-depth analysis of all the components of the specified system. Chapter 7 validates the proposed enhancements through both analytical analysis and experimental simulations. Chapter 8 emphasizes the design considerations in the implementation of the fabricated validation chip. Chapter 9 concludes this thesis and presents future research directions.

Chapter 2

Comparator

The comparator used in the SAR loop, as illustrated in Fig. 1.3a, has one main function: creating a large amount of gain in a short period of time, to achieve a complete (digital) decision. This gain is critical to accurately determine the polarity of the input signal, thereby ensuring the correct operation of the SAR loop. A clocked comparator creates the most gain in the shortest amount of time due to the use of positive feedback [2]. Given the intrinsic characteristics of a clocked comparator, the device has two distinct states: reset and active. The device is initialized to zero in the reset state, providing a consistent starting point for all conversions. In the active state, the comparator accumulates gain, determining the polarity of the input signal, as illustrated in Fig. 2.1. The comparator is active when the clock signal is high and enters the reset state with a low clock signal.

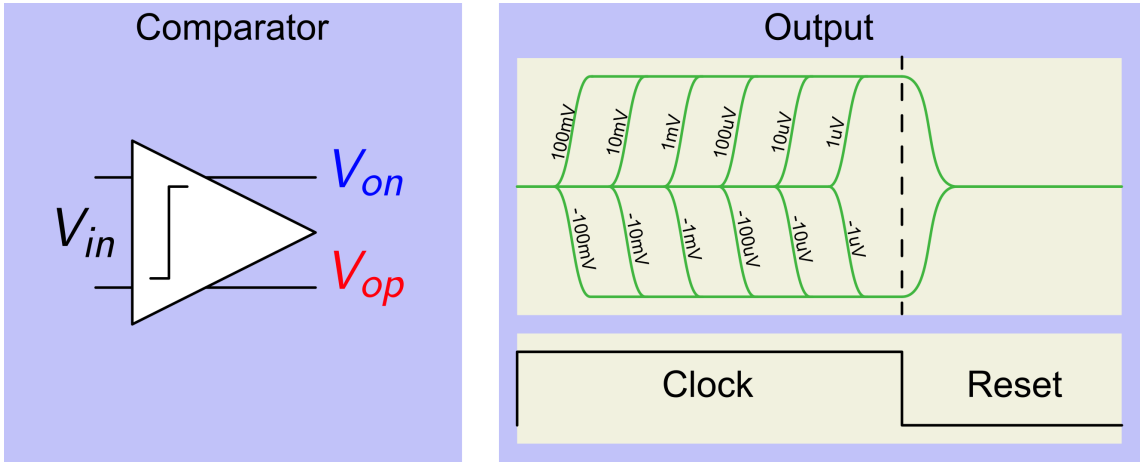


Figure 2.1: Transient of a clocked comparator with input signals varying from a μV to 100 mV, as indicated next to the curve.

During the time that the clock is high, the input signal is applied to the comparator. At the same time, the comparator enters the regeneration phase, accumulating

gain exponentially. Upon accumulating sufficient gain, the output voltage reaches the full digital logic voltage threshold, indicating a valid response. As illustrated in Fig. 2.1, the time required for a valid response depends on the magnitude of the input voltage, with more time required when the input voltage approaches zero.

During the regeneration phase, positive feedback is implied to maximize the accumulation of gain in the system. This positive feedback is created by two transconductances (g_m) whose outputs are cross coupled to the system's input. The comparator time constant and, thus, the device speed, are determined by the value of g_m of gm cells and the parasitic loading of the circuit (C_L), as illustrated in Fig. 2.2

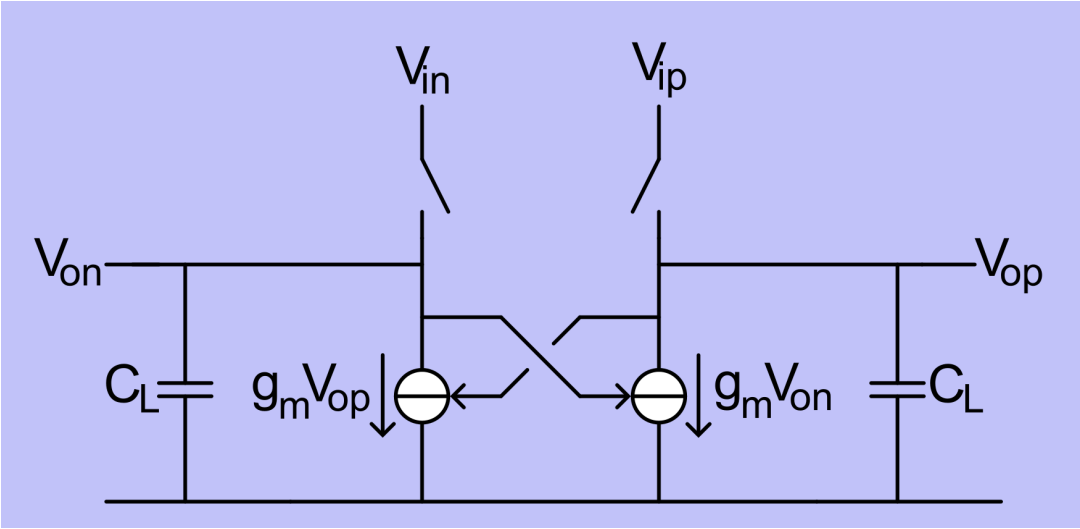


Figure 2.2: Exponential gain of the comparator with ideal transconductances.

During regeneration, the following equation holds:

$$V_{op} - V_{on} = (V_{ip} - V_{in}) \exp \frac{t}{\tau} \tag{2.1}$$

$$\tau = \frac{C}{g_m} \tag{2.2}$$

with τ being the time-constant of the circuit defined in Eq. 2.2, C being the parasitic loading capacitance, g_m the differential transconductance of the system, and V_{in}, V_{ip} the input nodes and V_{on}, V_{op} the output nodes of the system. At $t = 0$, the input differential is sampled on the output differential, creating a starting voltage of V_{id} for the exponential gain.

2.1 Comparator output

In Fig. 2.3, a comparator is shown that illustrates the differential output between the nodes V_{on} and V_{op}. Under the assumption of infinite available time for the

comparator, the differential output yields two primary digital codes, positive (1) or negative (0). However, limiting the available time of the comparator, a third region emerges. Within this region, the comparator does not accumulate enough gain; therefore, the differential output does not move significantly away from the initial starting point. With small input voltages, the gain of the comparator may be considerable, but the absolute voltage remains close to its initial value. When the output remains close to this initial value, the system cannot determine whether the output signal represents a digital 1 or a digital 0 and resides in the metastable state, as illustrated by the gray area in the output codes in Fig. 2.3.

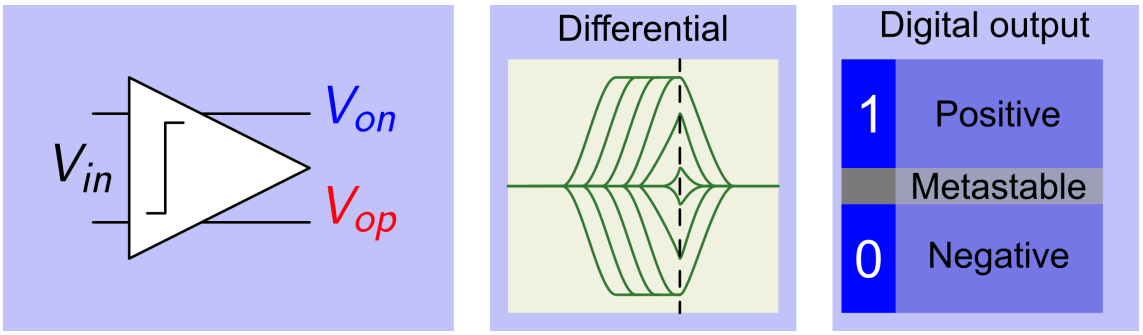


Figure 2.3: Differential output of a comparator.

2.2 Timing

To quantify the width of the metastable region, an analysis of the system's transient response is performed. Observing the transient output shown in Fig. 2.4, it is evident that the differential output remains close to zero at the end of the conversion, indicating a metastable comparator. Using Eq. 2.1, the equation can be reformulated to calculate the time required for a valid response, leading to the following:

$$t_{valid} = \tau \ln\left(\frac{V_{od}}{V_{id}}\right) \tag{2.3}$$

with V_{od}, V_{id} being the differential output and input voltage, respectively. From this equation, it can be shown that for small input values, more time is required to get to complete digital levels. In Fig. 2.4, the accumulated gain for various input values is illustrated. A small transitional region is present where the comparator is activated. The comparator accumulates a linear gain within this region while transitioning the output nodes into the regeneration phase. This linear gain is depicted by the asymptotic segment at the beginning of the gain plot. Once enough gain is accumulated, the clipping of the output nodes of the comparator to the supply rails results in plateauing of the gain-curve. If the input voltage is too close to zero, there is insufficient gain in the system.

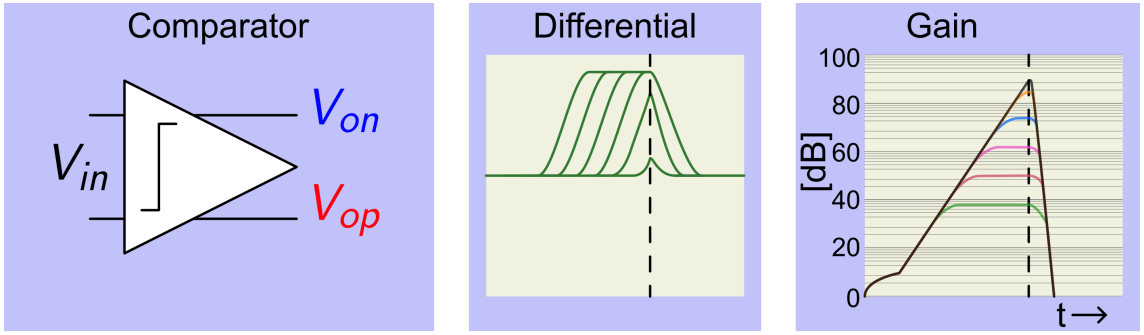


Figure 2.4: Differential output transient and gain of a comparator, with four valid and two metastable responses.

The device's time-constant is used to quantify the operational speed of the comparator. In Fig. 2.5, a comparator is depicted, demonstrating six input voltages of identical polarity, each separated by a decade. To calculate the additional time required to resolve an input signal that is an order of magnitude smaller, one can refer to Eq. 2.3, to find:

$$\Delta t = \ln(10) \cdot \tau \approx 2.3 \cdot \tau \equiv T10 \tag{2.4}$$

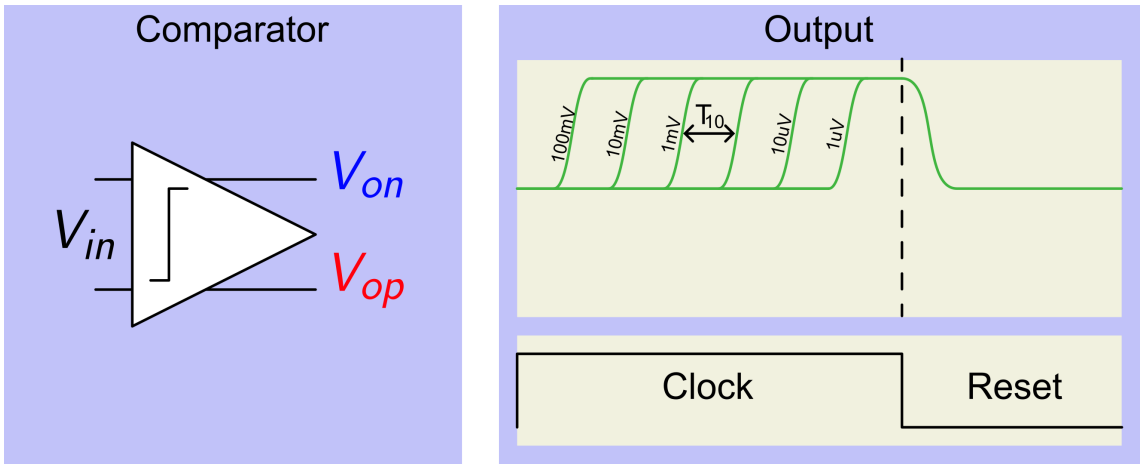


Figure 2.5: Output transient of a comparator, with input voltage steps taken a decade apart.

Due to the nature of the SAR loop, a limited time is available to the comparator. For example, if the time allotted to the regeneration phase is $6 \cdot T10$, the maximum resolvable input signal is $1\mu V$. Should the input signal fall below $1\mu V$, the output of the comparator becomes metastable, inducing an error within the SAR loop. These types of errors will be referred to as metastable bit errors. The proportion of bit errors to error-free instances is referred to as BER. This thesis aims to reduce the BER within the SAR loop without slowing down the speed of the SAR algorithm.

Chapter 3

Metastability

In a conventional SAR ADC, the output of the comparator is stored by the capture latch. The capture latch, implemented as an RS-latch, is also characterized by positive feedback, which enables the accumulation of additional gain during a metastable comparator decision while storing the comparator output for digital processing. At the end of the conversion, the capture latch effectively copies the output voltage of the comparator. As a result, it duplicates the metastable region of the comparator, only reducing its width by adding more gain, as illustrated in Fig. 3.1. The magnitude of this reduction is directly proportional to the additional time allocated to the capture latch.

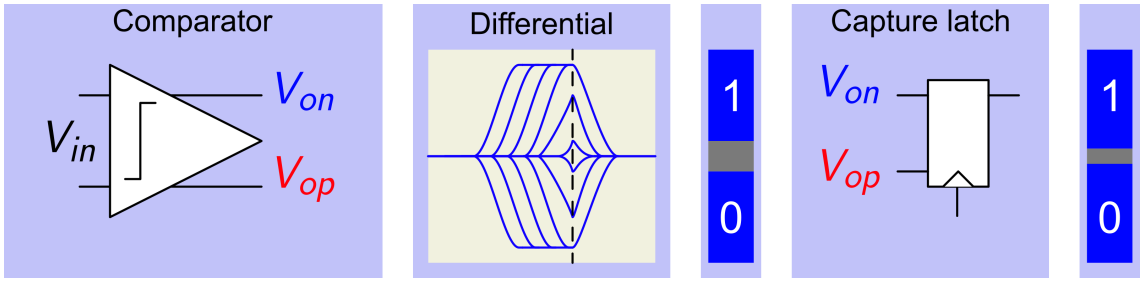


Figure 3.1: Metastable output voltages of the comparator and capture latch.

In the classical implementation of comparator and capture latch, only a single output from the comparator is used. Thus, only one bit of information can be retrieved per comparator conversion.

Rather than observing the comparator differentiatly, both output nodes can be examined independently. In the case of full decisions, both outputs are exactly opposite to each other, but in the case of metastability, their individual outputs are not the inverse of each other, and more information can be extracted from the comparator. This additional information will become a key to reducing BER, as will be described in this thesis.

For practical reasons, in this thesis we will use a "Strong arm' latched comparator [3]. In the following, we will characterize three distinct regions: startup, regeneration, and clipping, as illustrated in Fig. 3.2. Initially, the system begins in a known state, called the reset state of the device. For the strong-arm latch, both output nodes are placed at the upper supply rail in this region. Upon activation of the system, both outputs transition from the supply rail to the natural common-mode voltage of the latch, referred to as V_{meta}. During the regeneration phase, the comparator utilizes the positive feedback element and produces exponential gain over time. The clipping region is characterized by the outputs moving progressively slower as they approach the supply rails.

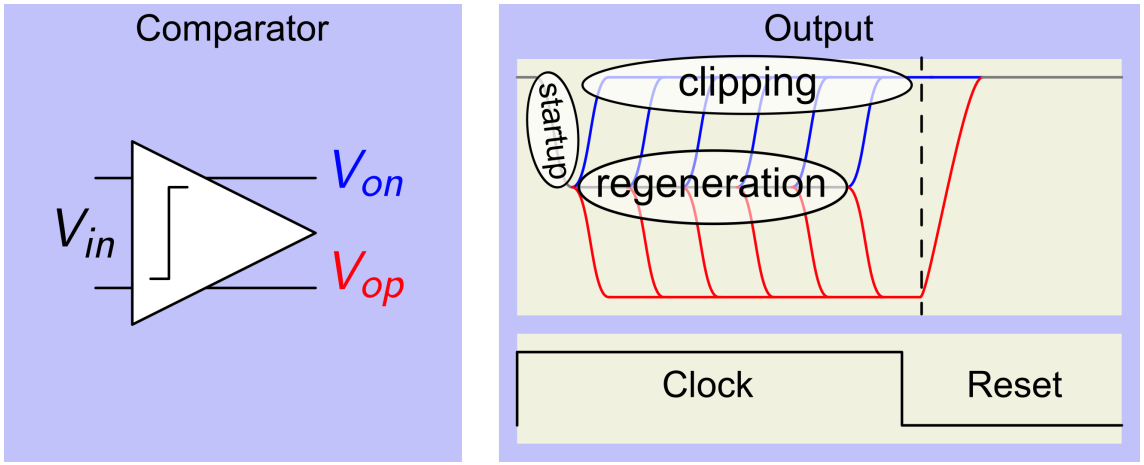


Figure 3.2: Input voltage sweep with the single-ended response of the comparator.

The system exhibits a metastable conversion when the comparator remains in the regeneration phase until the end of the cycle. Consequently, both output nodes remain close to V_{meta} due to insufficient gain accumulation, as illustrated in Fig. 3.3. For correct operations, it is required that both outputs are positioned at opposite supply rails.

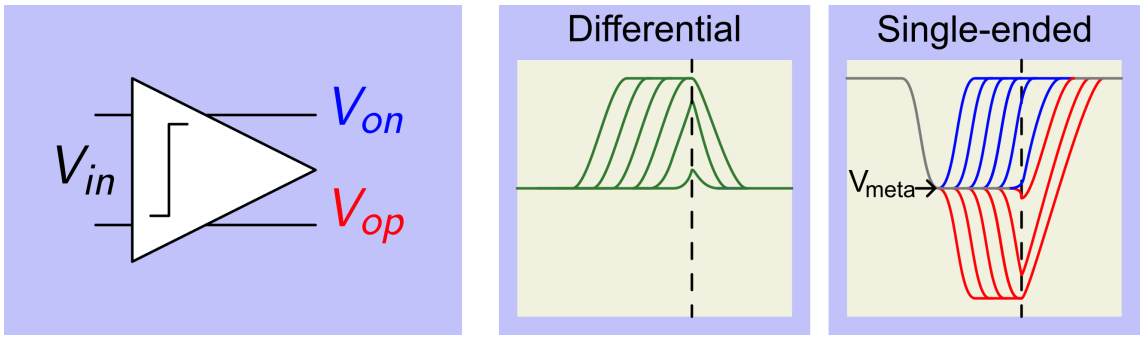


Figure 3.3: Transient output waveform of metastable and valid responses, with the same polarity input voltage.

By comparing this output voltage with V_{meta}, metastable events can be detected. By implementing a gain block after the primary comparator with a specified tripping voltage, a detection scheme can be created to identify instances of metastability. Within our system, both outputs initialize from V_{dd}. Setting the tripping voltage of the gain block above V_{meta} will induce a trigger during the initialization phase. In contrast, setting the tripping voltage below V_{meta} will ensure that only valid triggers occur during the conversion phase.

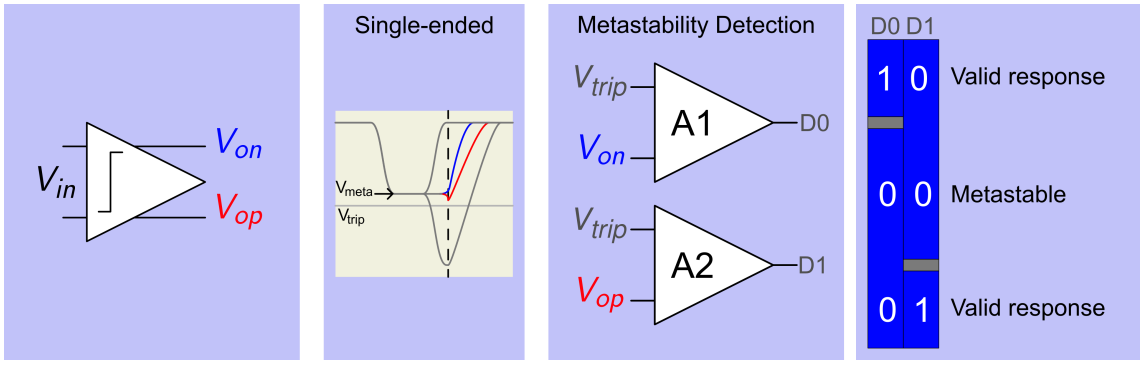


Figure 3.4: Metastability detection circuit for comparators

The various results of the metastability detection circuit are shown in Fig. 3.4. In case of an easy decisions, V_{on} or V_{op} will reside at opposite supply rails at the end of the conversion. Subsequently, the amplifiers following the comparator will saturate to the supply rails, resulting in a digital output of 1/0 or 0/1, as illustrated by the "Valid Response" in Fig. 3.5. In contrast, both output nodes remain at V_{meta} throughout the conversion in metastable scenarios. The input of the amplifier stabilizes at V_{meta} and V_{trip}, producing a differential voltage of V_{meta}-V_{trip}. Assuming the amplifier has sufficient gain, this scenario leads to an amplified output of V_{ss}, resulting in a digital combination of 0/0 at the output.

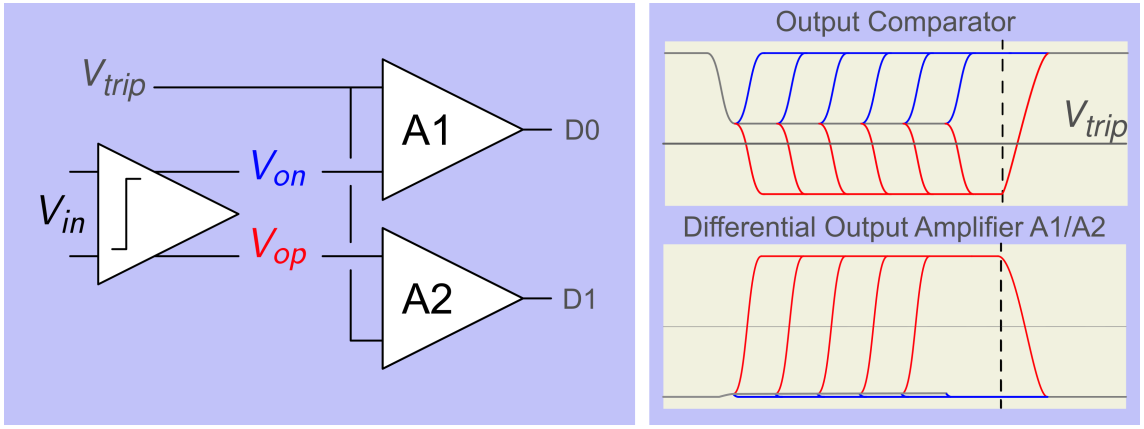


Figure 3.5: Transient response of amplifiers A1/A2 metastability detection circuit.

Although the initial comparator exhibited metastability and could not supply a full digital decision, the subsequent amplifiers do not exhibit metastability and solely provide supplementary gain to the system. This induces an offset of the metastable point of the comparator. However, when the output of the comparator comes closer to V_{trip} of the amplifier, even the output of the amplifier will not provide a full digital signal.

3.1 Dual capture latch

In the following section, we will make use of the additional information provided by the two outputs of the comparator. Two capture latches are required to store the two independent outputs of the amplifier. Both latches independently store the amplifier's digital value for digital processing. Given the symmetric nature around the voltage V_{meta} of the comparator, only one of the two amplifiers undergoes a polarity change during the conversion process. By giving each amplifier its own capture latch, as illustrated in Fig. 3.6, ensures that at any given time/voltage instance, only one of the two capture latches can be metastable.

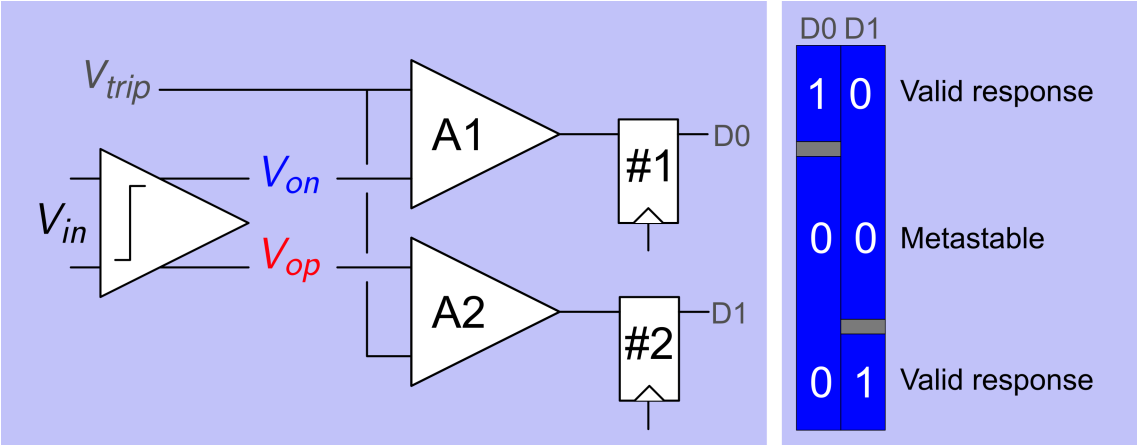


Figure 3.6: Output regions of the comparator, amplifier, and capture latch chain

One of the capture latches can experience metastability when the amplifier's output is aligned with the tripping voltage of the capture latch at the end of the cycle. Concurrently, the other amplifier maintains its output at V_{ss}, resulting in no change in the decision and thus ensuring a consistently valid response. The former three output regions of the single comparator are now segmented into five distinct regions: two metastable points of the capture latches and three valid regions. The width of the middle region, which produces a digital output of 0/0, is controlled by the voltage differential between V_{trip} and V_{meta}.

The following chapter will show that the principal role of this detection circuit is to take advantage of both outputs of the comparator to create more time for metastable events inside the SAR loop.

Chapter 4

Proposed SAR loop with improved BER

As an initial thought, one might think that the detection of metastable events implies the potential for their compensation. However, the existing literature indicates that attempts to mitigate metastable events merely displace these points, failing to reduce their occurrence and instead generating new metastable errors [4]. Metastability is critically important, yet often misunderstood in the context of comparators and ADCs [5, 6]. A fundamental principle in reducing metastability within comparators is to provide the comparator with more time.

The objective of incorporating the metastability detection circuit inside the SAR loop is to extend the duration available for the capture latches to resolve metastable events parallel to the normal operation of the SAR loop. Implementing the metastability detection circuit within the SAR loop requires two capture latches, each connected to two independent DAC elements per bit, each with half the value of the original DAC element. This architecture shall be called the dual DAC system, whereas the conventional SAR-loop will be called the single DAC system.

4.1 Switching scheme

A switching scheme is formulated based on the digital outputs, D0 and D1, of the metastability detection circuit, as illustrated in Fig. 3.4. For the valid responses 1/0 and 0/1, the DAC needs to move up or down, respectively. Upon entering the original metastable region of the first comparator, the voltage level on the DAC approaches zero, implying that no further steps are necessary. Specifically, before the end of the cycle, no voltage should have been added or subtracted from the DAC. This results in the switching scheme depicted in Fig. 4.1. The region denoted by 'DAC - no change' will henceforth be referred to as the dead-zone of the system.

A digital inversion has been incorporated into one of the two capture latches to facilitate system comprehension.

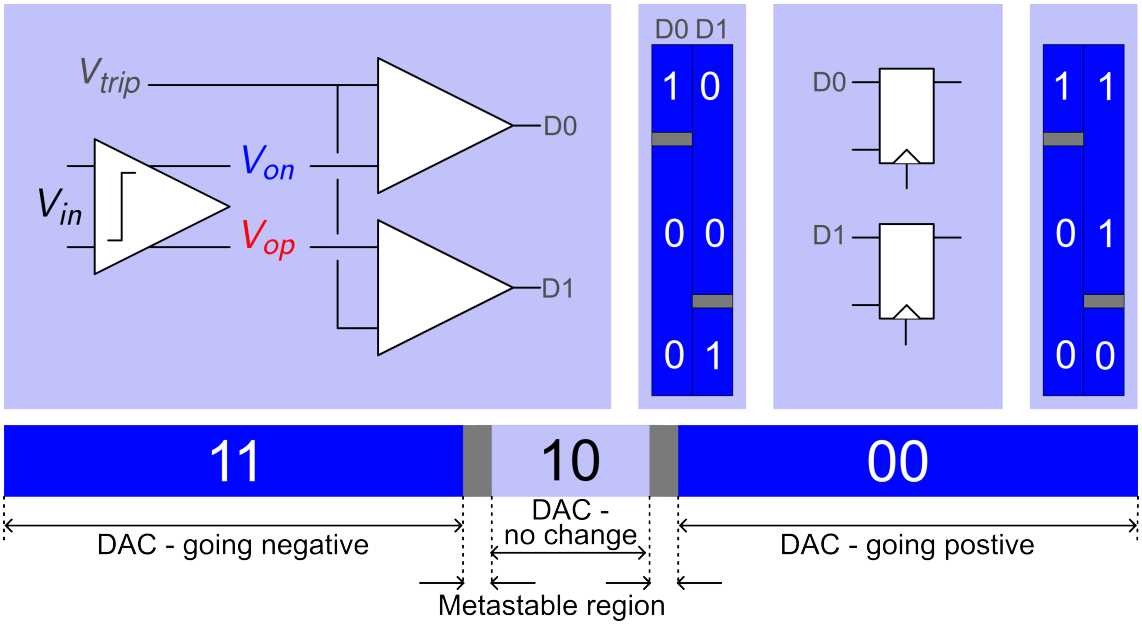


Figure 4.1: Metastability detection circuit of the comparator with the designated switching scheme. The capture latch connected to D1 has an additional inversion.

The conventional single-bit DAC structure is now replaced by a two-bit dual-DAC system, the original three distinct regions now are divided into five distinct regions comprising positive or negative DAC transitions, a dead-zone, and the two new metastable regions. These distinct regions are visualized by their respective DAC halves, as illustrated in Fig. 4.2. The digital inputs are located at the base of the DAC symbol, with the effective DAC voltage denoted at the top. The numeral inside the DAC symbol represents the differentiation between two DAC halves. The digital inputs of the DAC elements correspond to the digital outputs of the metastability detection circuit, specifically the output nodes of the capture latches. The initial state of the digital input is characterized by the reset value of 0.5. A transition of the digital input to 1 indicates a positive step on the DAC, and a transition to 0 denotes a negative step. Fig. 4.2 shows the reset and the 5 different possible situations.

The reset/sampling region serves as the starting point of a DAC element, where conversion states 1 and 5 correspond to a complete increment or decrement, respectively. Conversion state 3 represents the middle region, which does not produce an effective change in the DAC output. Both DAC units undergo complementary transitions during this state, resulting in a net zero change at the output. This phenomenon is explained through an analysis of the digital inputs; DAC 1 transitions from 0.5 to 0, taking a step down, while DAC 2 transitions from 0.5 to 1, taking a step up.

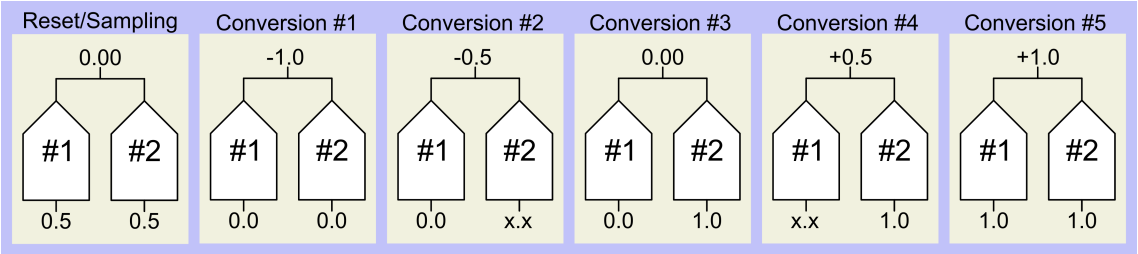


Figure 4.2: The different switching ranges of the complete DAC.

Conversion states 2 and 4 represent transient conditions in which one of the capture latches is metastable and actively resolves the metastability by building up more gain in the capture latch. Specifically, during conversion state 2, the capture latch affiliated with DAC 2 is metastable, while the capture latch linked to DAC 1 takes a decision. This puts a step onto the DAC by DAC 1, concurrently with DAC 2 actively resolving its metastability. Conversely, a similar scenario occurs in transition state 4, with the capture latch associated with DAC 1 being metastable while the other latch takes a decision. Since metastability is inherently time dependent, these transient states are temporary, with the result, given enough time, that the system always ends in one of the stable regions, namely conversion states 1, 3, or 5.

4.2 Dual-DAC ADC

Fig. 4.3 shows the switching scheme defined for a single bit. Every bit has two independent capture latches and two independent DAC units.

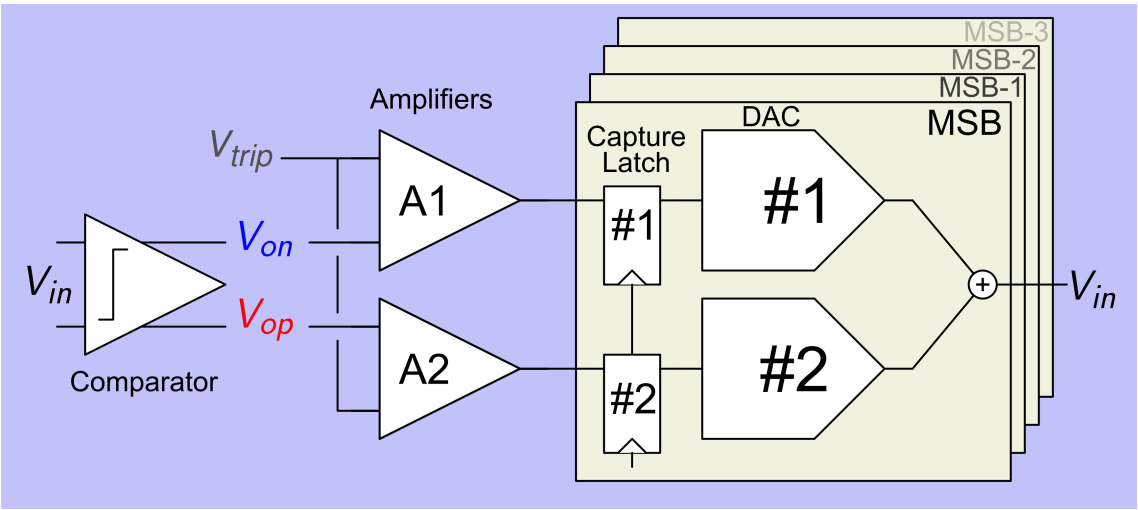


Figure 4.3: System overview of a 5-bit ADC, sampling circuit excluded.

Both amplifiers (A1 and A2) are connected directly to the two outputs of the comparator. The outputs of the amplifiers are connected to the capture latches

for the their corresponding bits. The SAR logic dictates the activation sequence of these capture latches, ensuring that the correct capture latches are transparent at the correct time intervals. The DAC unit is directly connected to the capture latch. Auxiliary logic is incorporated within the DAC element to ensure an idle state in the absence of valid signals. Consequently, both outputs of the DAC are directly connected to the input of the comparator, thus completing the SAR loop.

4.3 SAR cycle

Fig. 4.4 illustrates the conversion cycles of single and dual DAC ADCs. The upper section of the illustration shows the single DAC ADC, whereas the lower section illustrates the dual DAC version. The blue line represents the effective DAC voltage, starting from the system's level input voltage. The dotted vertical lines denote the end of the comparator's comparison phase, and the gray vertical lines signify the end of the cycle. The red boxes mark the required time for the comparator; in scenarios of metastable decisions, the red box spans half the cycle, fully utilizing the available time for the comparator. In contrast, a gap is observable between the comparator and the latch for an easy decision. The single DAC is characterized by a single capture latch depicted in gray, in contrast to the dual DAC, which employs two capture latches illustrated in gray and light blue, with the DAC settling depicted in green.

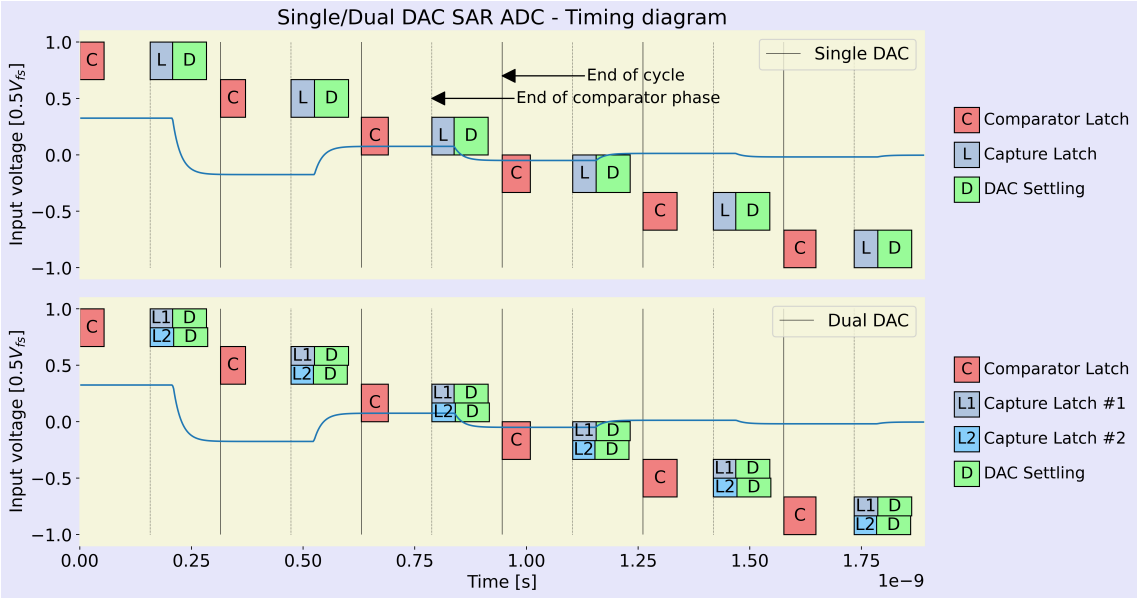


Figure 4.4: A 6-bit Dual and Single DAC conversion comparison with input voltage 0.32

The width of the depicted boxes accurately reflects the required time per component, according to simulation results. The settling time (green rectangle) of the

DAC is defined such that each step remains within ≤ 0.5 LSB, ensuring the absence of DAC settling errors. The DAC is directly driven by the capture latch output; consequently, the DAC follows immediately after the latch.

As in the dual DAC system, the metastable zones of the two latches are always separated by the dead-zone (4.1) and hence only one latch per bit can enter a metastable state. The harder decision inherently requires a longer time to resolve, causing a delay in the DAC response compared to an easy decision. When each decision is straightforward, as shown in Fig. 4.4, no step artifacts appear. In contrast, when the input voltage is close to the amplifier's V_{trip}, the complexity of the hard decision increases, extending the time required to resolve the (short) metastability. This phenomenon manifests itself as a step artifact on the DAC output before the end of the first cycle, as illustrated in Fig. 4.5.

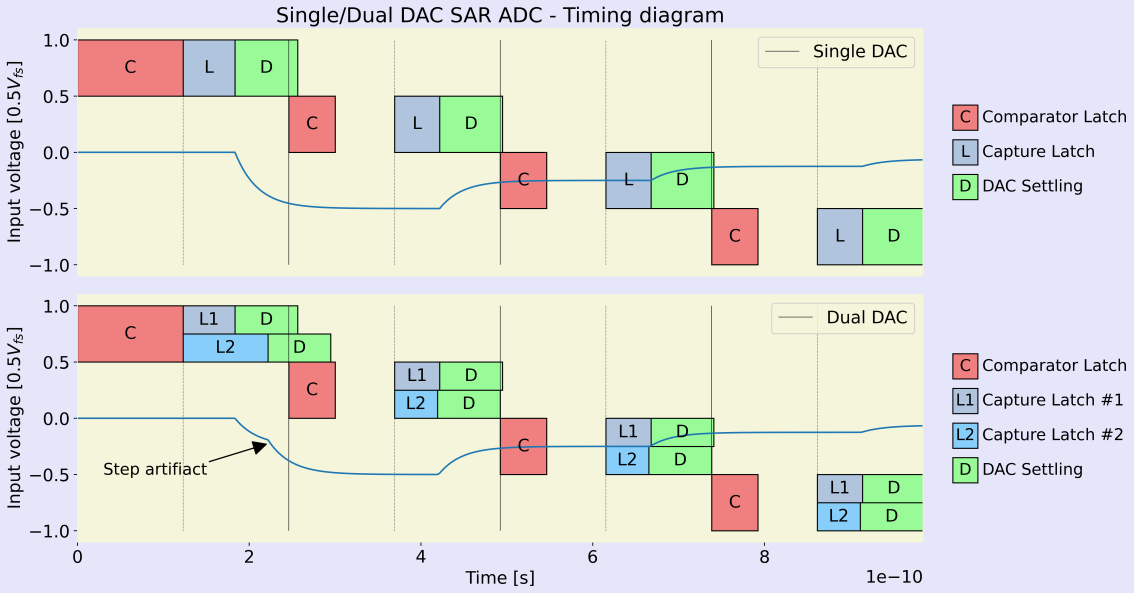


Figure 4.5: A 4-bit Dual and Single DAC ADCs comparison with the Dual DAC showing a step artifact.

4.4 Metastable events

To provoke a metastable event within the dual DAC system, the input voltage is moved closer to the tripping voltage of one of the amplifiers; see Fig. 4.6 (bottom image). The decision on capture latch 1 becomes increasingly difficult, requiring additional time to resolve the metastability. In contrast, capture latch 2 is not metastable, resulting in a discrete step on the DAC. Given that each DAC element is split into two equal halves, the magnitude of each step corresponds to the subsequent full-scale conversion step. This configuration facilitates an easy decision in the subsequent cycle in the presence of a metastable event, thereby avoiding a code error.

The Dual DAC is always capable of avoiding a code-error in this situation because the weight of the metastable half-DAC is equal to the weight of the next step in the SAR. Furthermore, the dual-DAC architecture attenuates the maximum metastable error from 2^{N-2} LSB to 2^{N-3} LSB.

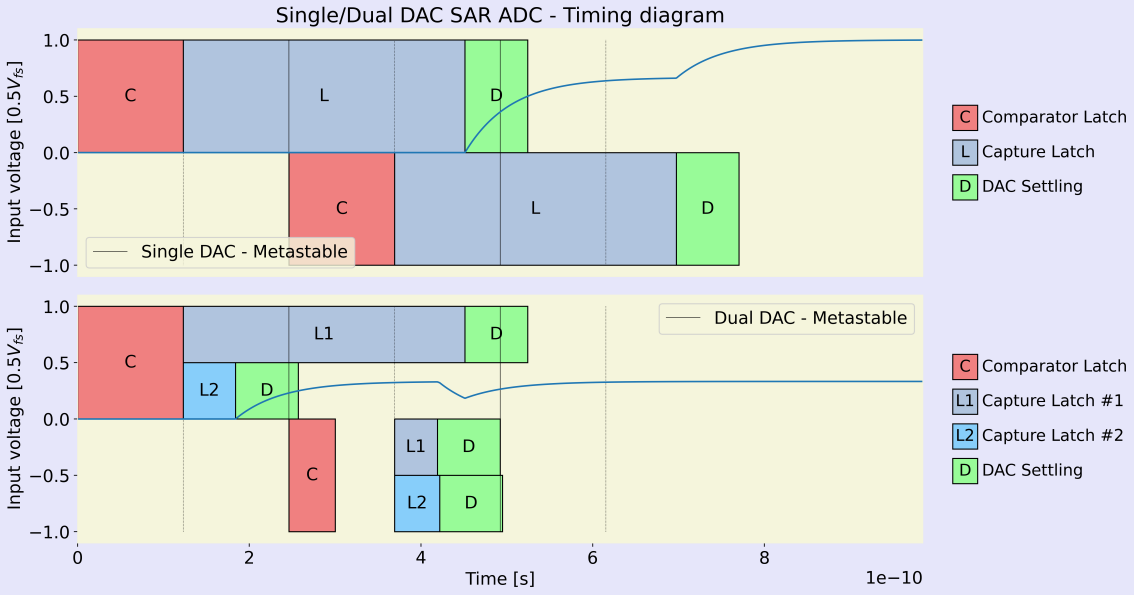


Figure 4.6: The first two bits of a Dual and Single DAC ADCs in the case of a metastable event.

When comparing metastable events between dual and single DAC configurations, it becomes evident that the dual DAC configuration exhibits an extended period of time to resolve metastable events. For the single DAC system, a metastable Most Significant Bit (MSB) decision sustains a metastable state in the MSB-1 decision due to a delay in the MSB decision. In contrast, in the dual DAC system, the DAC element connected to capture latch 2 makes a step, while capture latch 1 remains metastable in Fig. 4.6. Consequently, the DAC voltage transitions to -0.250 following the decision initiated by capture latch 2, facilitating a straightforward decision for the next conversion, while capture latch 1 remains metastable. The contribution of both MSB-1 DAC elements, each providing 0.125, combines to a total step of 0.250. The dual DAC system continues to function effectively, even with a metastable capture latch 1, without making a bit error.

In Fig. 4.7, two scenarios of 6-bit conversions in a dual DAC ADC are presented. In the upper section, a conversion is shown in which the metastability of capture latch 1 of the first bit is resolved before the beginning of the comparison phase of the third bit. This facilitates a straightforward decision for the third bit. Conversely, the lower section illustrated a conversion in which the metastable event at capture latch 1 resolves after the beginning of the comparison phase of the third bit. This

delayed step yields a hard decision for the third cycle, inducing an erroneous step and ultimately causing a bit error.

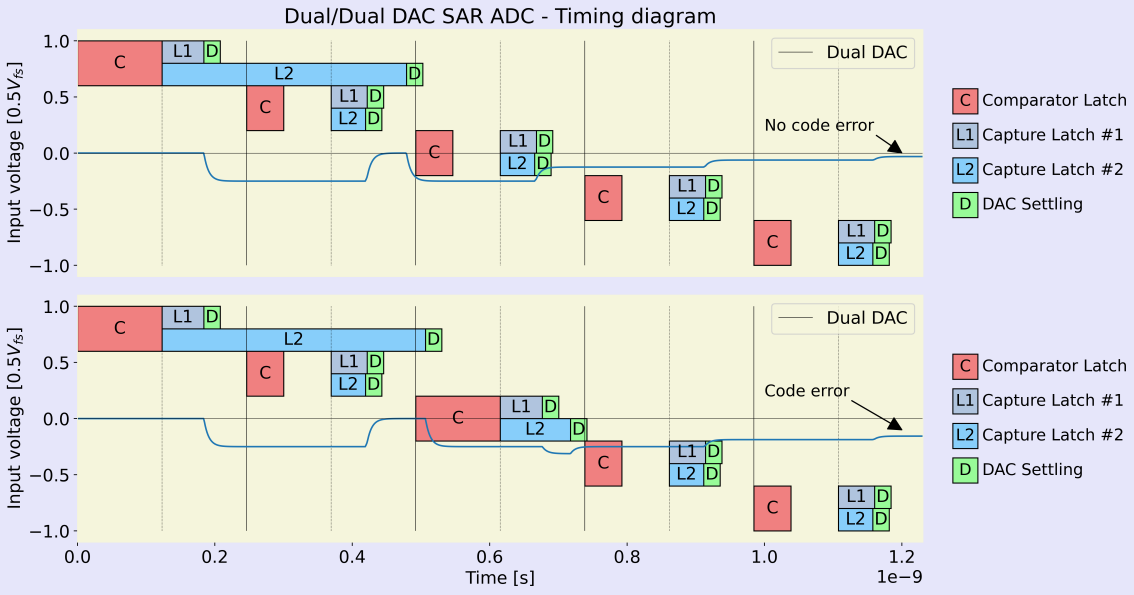


Figure 4.7: Two conversions of a dual DAC ADC. The upper conversion exhibits no bit error, but the lower conversion shows a bit error.

To quantify the time advantage gained by using the dual DAC system, the available time of the single DAC system needs to be known. Within an idealized and noise-free environment, a metastable initial decision implies that the capture latch has not resolved the input voltage before the next cycle, rendering the second decision inherently metastable. As a result, the single-DAC system is limited to one cycle for gain accumulation.

For the dual DAC system, if a capture latch is metastable throughout the entire cycle duration, a half step is introduced to the DAC. In the next cycle, this step is reversed, restoring the initial voltage on the DAC. Consequently, metastability is reinstated by the third cycle, perpetuating the previous loop. To disrupt this loop, the capture latch must resolve its metastability before the comparison phase of the third cycle.

A comparison of both systems reveals that, in contrast to the singular conversion cycle used for gain accumulation in the conventional design, the dual DAC system engages in two distinct cycles to accumulate gain, thus attenuating the BER of the system.

Chapter 5

Dual-DAC limits

With the advantages of the dual DAC configuration shown, the boundaries of the dual DAC SAR ADC will be analyzed. A test bench configuration comprising an ideal sampler, comparator, capture latches, and DAC units has been constructed to validate and quantify these boundaries. This test bench facilitates the quantification of code errors within the system and the capability to modulate system parameters and evaluate the system's effective response. A code error is the difference between the digital output and the analog input code, representing the error between these two values. Without non-idealities in the system, the output code should be within 0.5 LSB of the input signal. The constraint of 0.5 LSB arises from the quantization noise in the system.

A histogram has been constructed from code errors to analyze numerous input points, as shown in Fig. 5.1. Three distinct configurations of 10-bit ADCs are present: ideal, noisy, and metastable ADCs. With the ideal ADC, all code errors are confined within 0.5 LSB, thus indicating optimal system operation. With the introduction of noise in the comparator, uncertainty is introduced about the accuracy of the system, culminating in errors extending up to 4 LSB. An increase in noise levels directly amplifies these corresponding errors. Metastable errors arise from limiting the available time of the comparator, which consequently reduces the accumulated gain in the system. This constraint induces metastable events in the comparator, leading to exponential code errors with a power of 2.

The dual DAC ADC boundaries can be systematically investigated by this created test bench. The dead-zone is characterized as the voltage range in which the single SAR ADC was defined as metastable. In contrast, the dual DAC SAR ADC stops the effective DAC stepping within this region, as illustrated in Fig. 3.4. For optimal system performance, it is essential to define two limits corresponding to the lower and upper limits of the dead-zone.

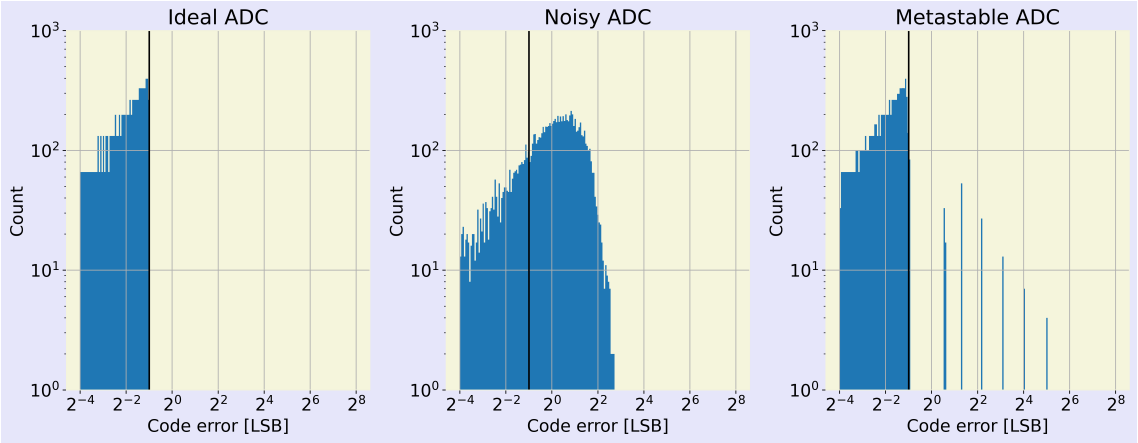


Figure 5.1: Histograms of three configuration ADCs

5.1 Upper limit dead-zone

Let's start with the upper limit of the dead-zone. Upon the comparator's input voltage entering the dead-zone, no steps will be made on the DAC. The system continues to operate with the remaining conversion, because in theory nothing is changed on the DAC-side the system thus will stay within the dead-zone, creating no further effective steps. Provided that the dead-zone is precisely defined below 0.5-LSBs, the resolution of the system will remain unaffected. This is because the DAC voltage resides within the system's quantization noise.

Increasing the dead-zone beyond 0.5-LSBs, for instance, to 8-LSBs, results in a corresponding loss of 8 LSBs of resolution. This is illustrated in Fig. 5.2, which depicts the code errors of two dual DAC SAR ADCs, with the distinguishing factor being the width of the dead-zone.

In the following, we will sweep the width of the dead-zone to fully understand the entire spectrum of the dead-zone width, enabling the comparison of multiple histograms. The histogram can be flattened and superimposed on an image for an adequate comparison, as demonstrated in Fig. 5.3. In this figure, the numerical information on the Y-axis in Fig. 5.2 is shown as a color code. Code errors are still represented on the X-axis, while the dead-zone width (input referred) is on the Y-axis.

Numerous phenomena are depicted in Fig. 5.3; the foremost is the possibility of attaining a resolution exceeding the system's quantization threshold. This assertion is proven by the majority of code errors below 0.5 LSBs for dead-zone widths. Furthermore, some code errors demonstrate an asymptotic trend that is converging toward the quantization noise threshold.

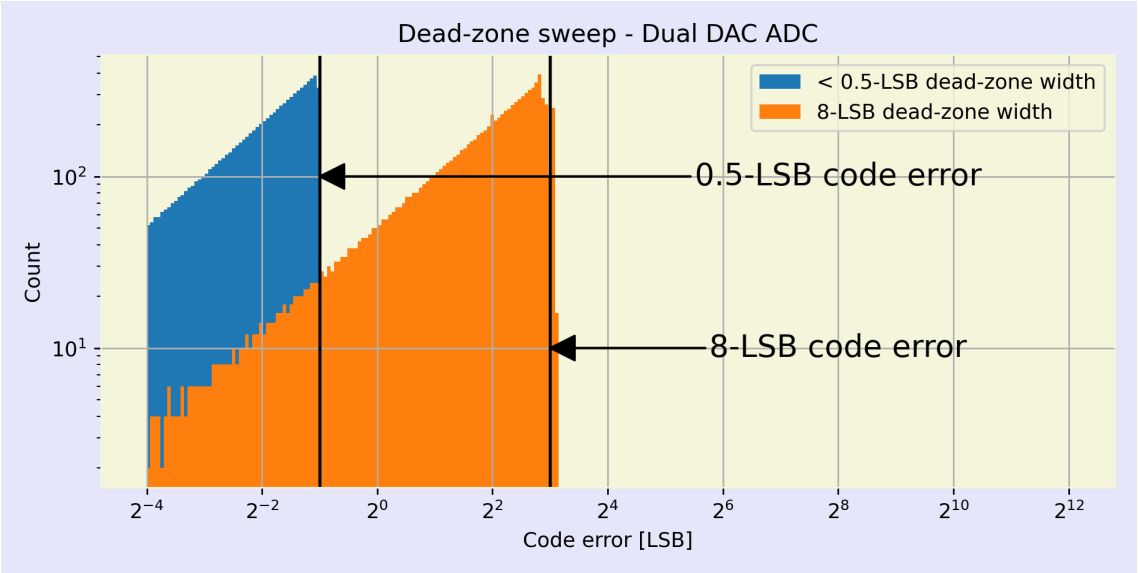


Figure 5.2: Code error using two dead-zone widths

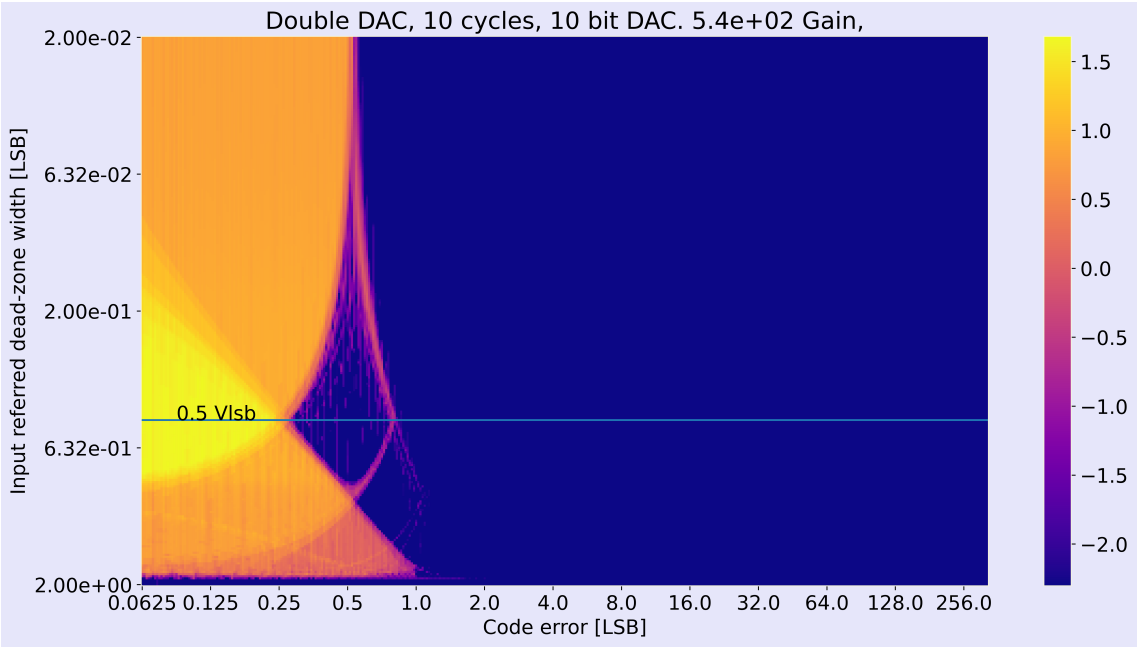


Figure 5.3: A showcase of quantization errors due to dead-zone limits

5.1.1 Increased ADC resolution

Focusing on the foremost artifact, the dual DAC system, as indicated by its name, employs two DAC segments, thereby facilitating intermediate steps. During each comparator comparison, two bits of data are retained instead of the conventional single bit, thus increasing the information per conversion. Typically, these two bits are complementary and do not impart additional information. However, when the voltage is within the dead-zone, these two bits provide additional insight into the input signal. The extent of this additional information depends on the width of the dead-zone, with a larger width allowing for more information acquisition. Should we create uniform region sizes, as illustrated in Fig. 5.4, a 1.5-bit system is shown, often used in pipeline ADCs [7].

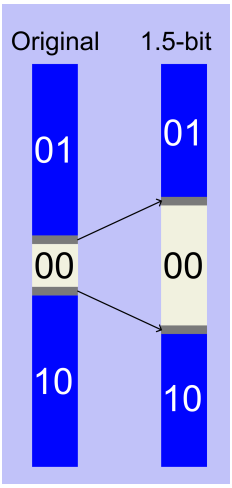
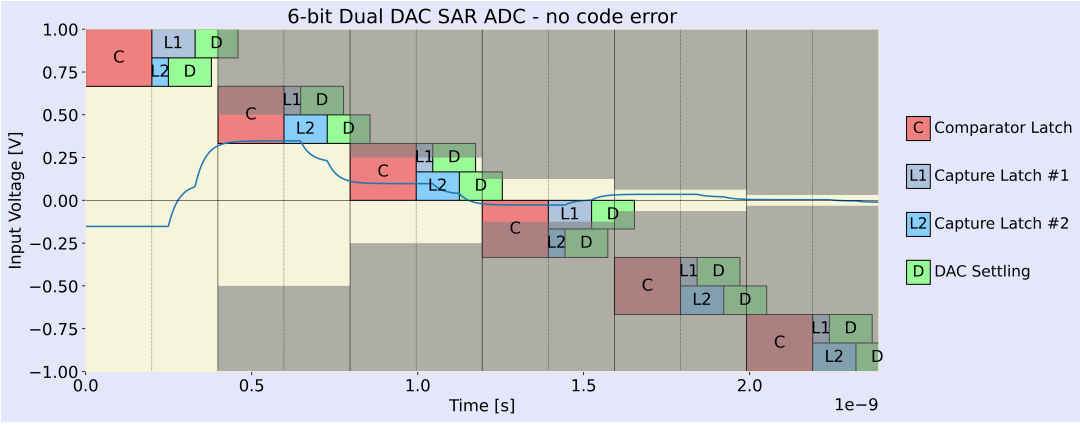


Figure 5.4: Dead-zone width modification to 1.5-bit system.

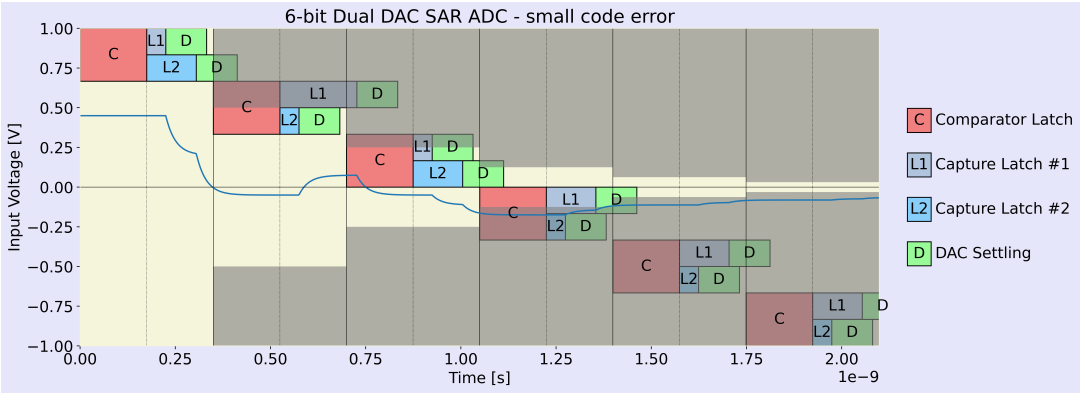
In the dual DAC system, the largest allowable dead-zone width is 0.5-LSB. At this specified width, the most additional information per conversion is stored when utilizing N+1 bit storage elements. Increasing the dead-zone width above this limit reduces the system's effective resolution.

5.1.2 DAC settling artifact

With the improved quantization noise explained, the minor fraction of code errors will be analyzed. Simulating multiple input values, an asymptotic behavior was found in the quantization noise of the system, as illustrated in Fig. 5.3 by the thin yellow line, curving between a code error of 1.3-LSB and down to 0.5-LSB. To focus on this phenomenon, the input values that show the corresponding code error are extracted. A new simulation is performed using these input values. In this simulation a 6-bit ADC will be used, to make it easier to see the voltage steps on the DAC, as illustrated in Fig. 5.5a.



(a)



(b)

Figure 5.5: 6-bit Dual DAC SAR ADC with a gray area indicating the available back-end ADC range, (a) correctly operating, input voltage does not enter the gray area. (b) false trigger of the dead-zone resulting in a code error.

The correct operation of the SAR ADC is illustrated in Fig. 5.5a; the shaded region denotes the voltage range of which the back-end ADC cannot correct anymore. The input voltage must remain outside this shaded region for accurate operation. In Fig. 5.5b, the activation of the dead-zone is false during the initial cycle, due to the incomplete DAC-settling. Consequently, this false activation leads the system to the shaded region by the fourth conversion, resulting in a small bit error.

Examining the underlying causes of this phenomenon, it can be seen that the system operates at its edge of operation, resulting in significant delays between both capture latches. This is attributed to the relatively small gain generated by the comparator, the large dead-zone width, and the large time constants of the system. For the MSB decision, capture latch 2 induces a substantial delay, culminating in a step artifact within the system. This step artifact positions the DAC voltage within the dead-zone for the MSB-1 conversion, as depicted in Fig. 5.6. Consequently, with the MSB-1 decision residing in the dead-zone, an erroneous step, in this case a

complete lack of a step is facilitated. This forced the input voltage into the shaded region of the conversion range in the MSB-3 decision, resulting in a small code error.

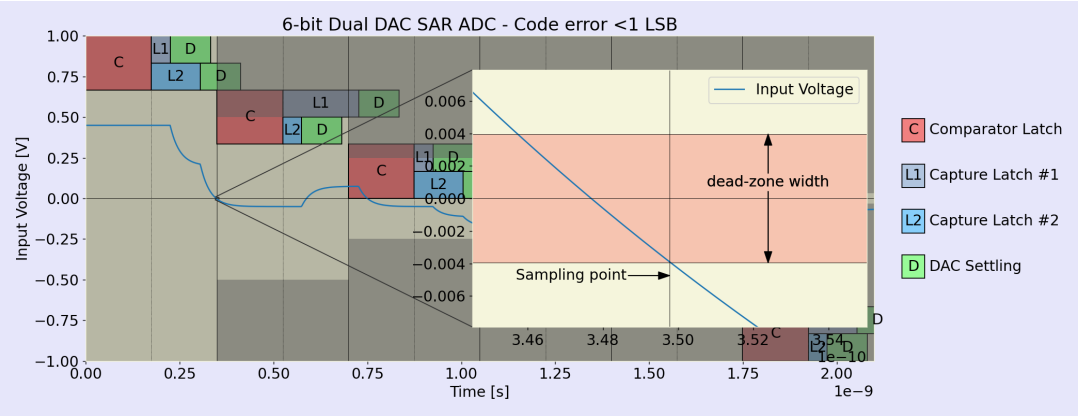


Figure 5.6: 6-bit dual DAC SAR ADC highlighting the false trigger of the dead-zone at the MSB-1 conversion.

Employing an N-bit storage element to accommodate (N+1)-bit data negates the benefits conferred by the increased dead-zone width. This is depicted in Fig. 5.7 for a 10-bit ADC, producing 11-bit data, of which only ten bits are stored. The DAC settling artifact persists within the system, resulting in an effective loss of system resolution. Consequently, the upper limit must be corrected to a lower value than the initially defined limit of 0.5-LSB.

5.2 Lower limit

With the upper limit of the dead-zone thoroughly examined, attention can now be directed to the lower limit. It is hypothesized that should the dead-zone diminish to zero, the system reverts to a single SAR ADC configuration. In this configuration, a single DAC SAR ADC structure requires that metastability is resolved prior to subsequent conversion; failure to achieve this will result in a metastability error. Reducing the dead-zone width gradually decreases the timing difference for a valid response between both capture latches, as illustrated in Fig. 5.8. Two horizontal limits indicate the available time for the single-latch and double-latch structures. The single latch threshold represents the time limit within which an easy decision must be valid, whereas the dual latch threshold corresponds to the interval allocated for a metastable decision, from which the latch can still create a valid response in time. The black curves are the time required for a valid response within the capture latch.

Should the duration for simple decisions exceed the timing limit of a single latch, the dual-latch functionality becomes compromised, leading to a metastable error

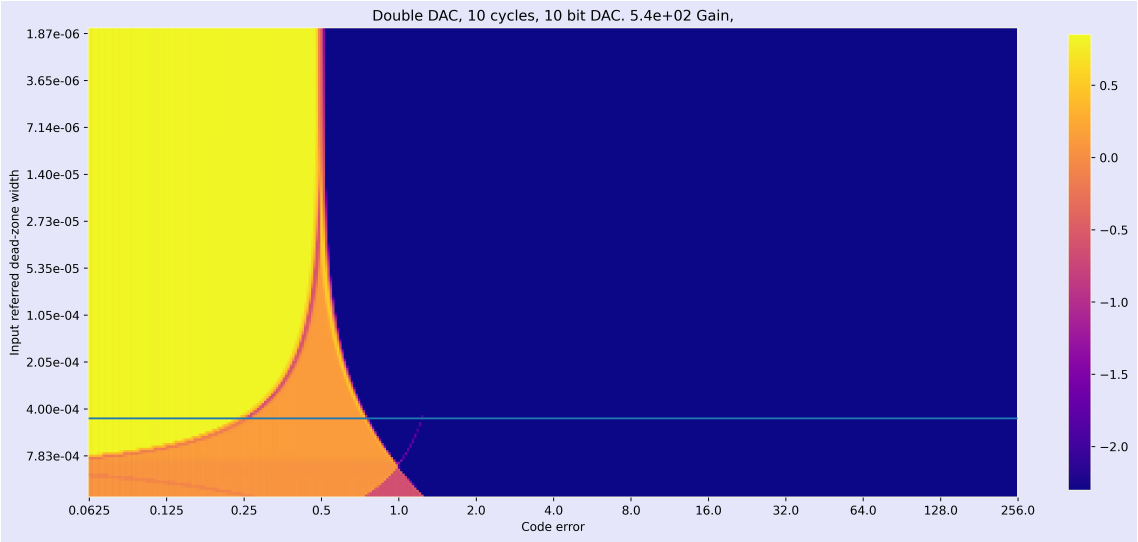


Figure 5.7: Dead-zone quantization for a 10-bit ADC using 10-bit storage (for 11-bit data).

in the output code. On the left-hand side, for input values in between the two peaks of the black curves, there is no separation between an easy and hard decision. Conversely, the right-hand side demonstrates correct operation, where both latches are sufficiently spaced, thereby ensuring a distinct separation between the easy and the hard decision.

The minimum width required is a function of the cumulative gain within the system. For the decision to be easy, a valid response is needed before the next cycle. If the dead-zone width is defined after the comparator, one must divide it by the gain of the comparator to calculate it back to the input. This resultant value is defined as V_{hyst}. The easy decision must have sufficient gain to resolve V_{hyst} to V_{dd}. If this is not possible within the available time, the dual DAC architecture reverts back to a single DAC functionality.

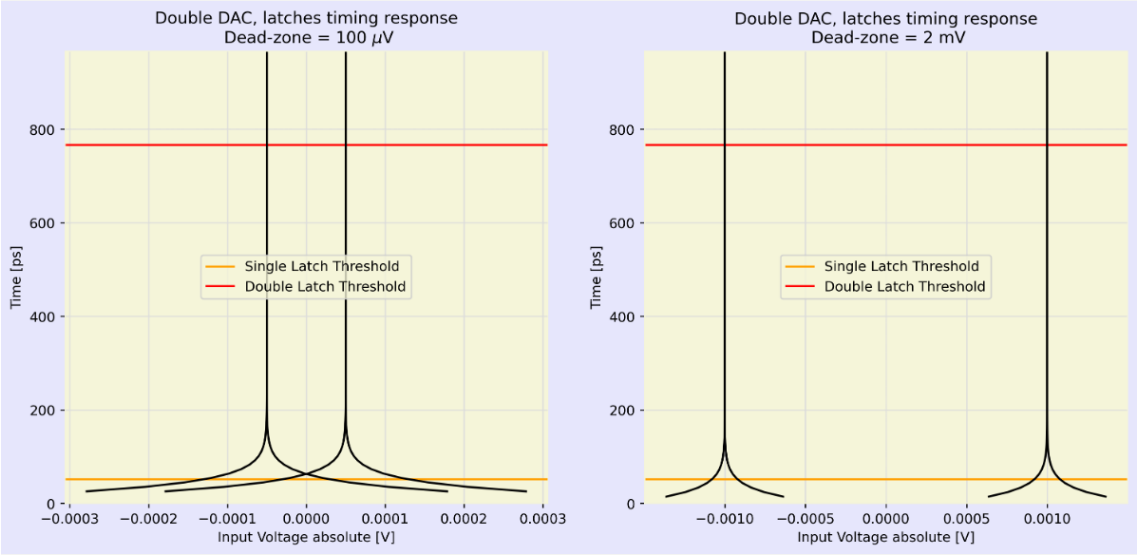


Figure 5.8: Timing response of capture latches, output comparator referred.

Chapter 6

System analysis

With all the components of the system identified, a complete analysis of the system will be performed, with the exclusion of the sampler circuit. Referring to Fig. 6.1, the analysis will begin with the comparator, followed by an examination of the amplifiers, capture latches, and the overall interaction between these components. Finally, the DAC element will be examined, with particular emphasis on the interaction between the DAC element and the RS-latches.

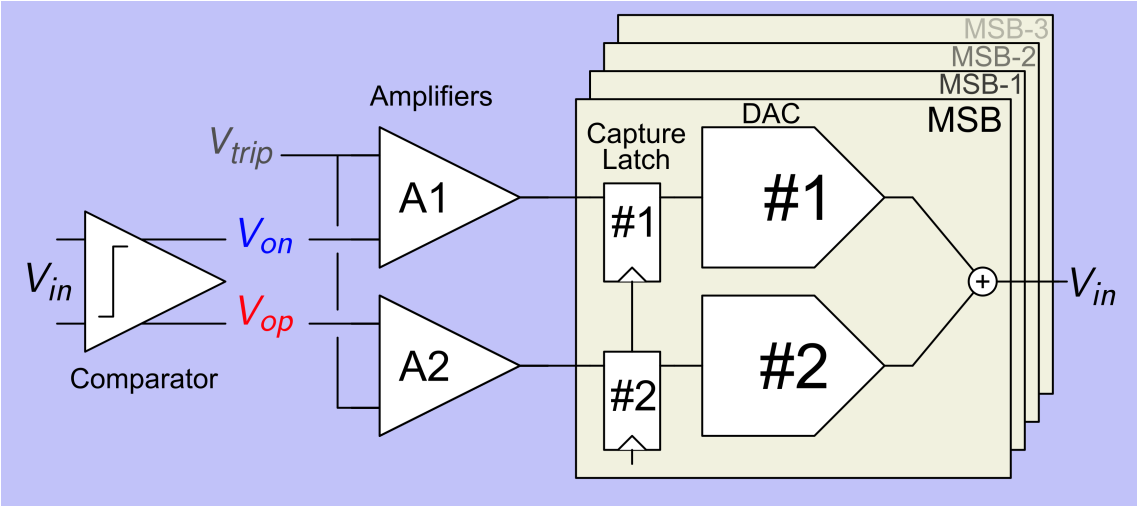


Figure 6.1: Comparator Chain including N-bit capture latches and DAC.

6.1 Clocked comparator

To define the BER of the SAR-ADC, an accurate model of the total gain built up in the chain is required. The first component in the chain is the clocked comparator, often only associated with exponential gain. The comparator has four distinct regions, consisting of the startup, regeneration phase, clipping regime, and reset, as illustrated

in Fig. 6.2. The regeneration phase is the only phase where the system builds up a gain exponentially [2].

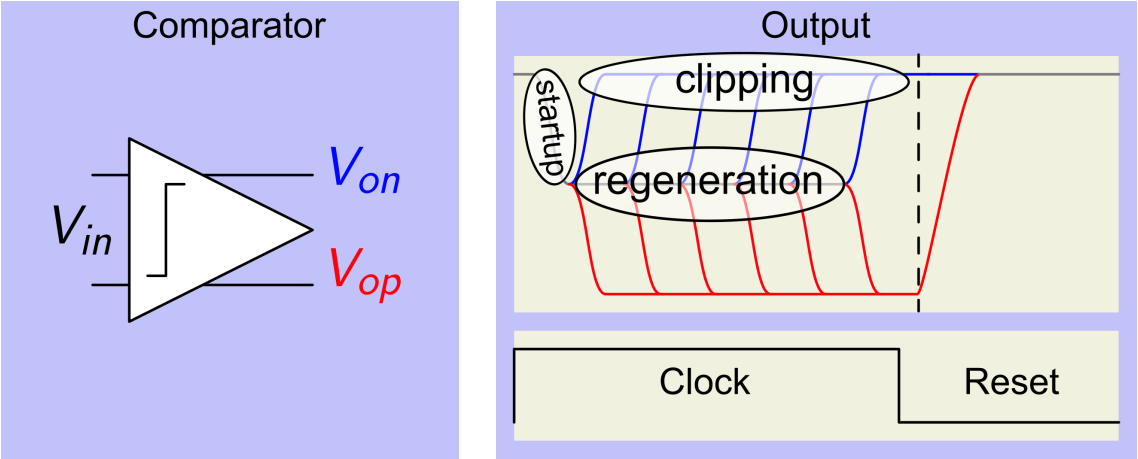


Figure 6.2: Differential and Single-ended outputs of a clocked comparator with the three regions of operation highlighted

For our system, a strong-arm latched comparator has been selected, as it is a very well-known architecture. The strong-arm latch comparator features a differential pair coupled with a tail current placed below the latch, ultimately reducing the supply voltage of the latch. Creating a pre-amplification once the comparator transistors between the reset state and the regeneration phase. The initial state of the comparator is the reset state, in which both outputs are shorted to V_{dd}, thus clearing the previous conversion from the outputs. The startup phase follows the reset phase. In this phase, the comparators transition between the reset state and the regeneration phase.

6.1.1 Time response

The total time required for a valid response depends on the magnitude of the input signal. When the magnitude of the input signal is close to the supply rails, a negligible gain is necessary for a valid response. However, the comparator still goes through the different regions of operation, inducing a minimal propagation delay within the system, referred to as t_{min}. Conversely, if the input signal is proximal to the tripping voltage of the comparator, more time is required to accumulate sufficient gain on the comparator side. As illustrated in Fig. 6.3, the time response of a comparator is shown.

In the following, we are going to construct a simple model for the time response of a comparator. For that, we need the time-constant τ of the comparator and the minimum propagation delay t_{min}. To define the time-constant of the system, the derivative of the slope in the regeneration phase can be calculated. The simulation

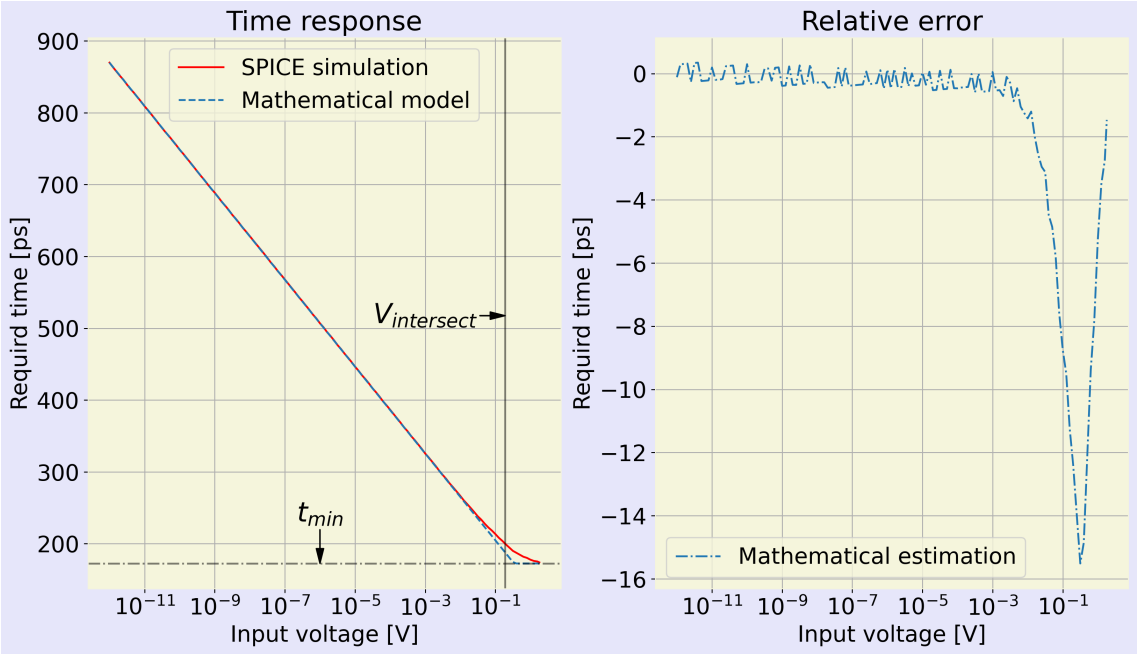


Figure 6.3: Comparator timing response over a large input range

results of Fig. 6.3 yield a time constant of 26 ps. From the same results, the propagation delay is calculated as 175 ps. With these time constants known, a model can be constructed for the different operational regions. Using t_{min} and τ, a linear function can be formulated:

$$t_{valid} = t_c + t_{min} \tag{6.1}$$

with:

$$t_c = \ln\left(\frac{V_{valid}}{V_{in}}\right) \cdot \tau \tag{6.2}$$

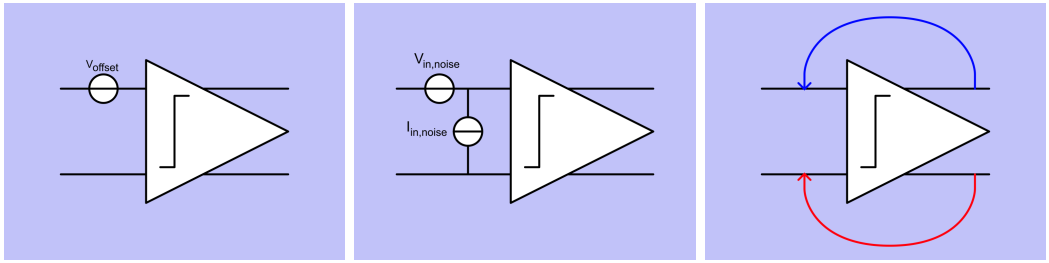
and V_{calid} denotes the full digital logic voltage. Using the above formula, an initial estimate can be made. It is observed that the mathematical model shows a deviation from the simulation results near the propagation delay of the comparator, as illustrated in Fig. 6.3 at the right-hand side where the relative error between the simulated curve and the linear model is shown. This minor deviation can be adjusted by using a fitting function. However, this deviation is inconsequential for metastable events of the comparator in synchronous SAR ADCs. In contrast, this model would prove to be inadequate if this had been an asynchronous SAR ADC, due to wrong estimations of the time required for easy decisions.

The propagation delay depends on the definition of a 'full' digital decision. If the full digital logic voltage is chosen below the clipping region, the propagation delay would be shorter. In the case of our simulation, an arbitrary valid response voltage of 0.95% V_{dd} was chosen.

A minimum-sized inverter is placed behind the comparator to reduce the loading of the comparator. This adjustment generates a trade-off between increasing the propagation delay of the system for faster τ. Incorporating a pre-amplifier preceding the comparator reduces several inherent non-idealities, albeit with an increased propagation delay within the comparator. Due to the simplicity of the constructed model, the additional propagation delay is easily accommodated, resulting in a precise and adaptable model.

6.1.2 Non-idealities

A clocked comparator has multiple error sources, including offset, noise, kickback, and hysteresis, as is modeled in Figs, 6.4a-6.4c, . In the case of SAR-ADCs that employ a single comparator, the offset is inconsequential; it simply introduces a system-wide offset without contributing to distortion or noise errors. The offset becomes a critical issue when using multiple comparators, potentially inducing distortion if the offset exceeds acceptable limits. Calibration techniques are frequently used to mitigate the offset between multiple comparators, reducing the distortion of the system.



(a) (b) (c)

Figure 6.4: (a) Offset visualization of a comparator. (b) Noise sources of a comparator. (c) kickback visualization of a comparator.

The noise generated by the comparator represents the primary source of error in high-resolution systems. The comparator's thermal and flicker noise components can be transposed to the system's input. Both noise sources do not exhibit a direct one-to-one relationship with the system's input [8]. Due to the deterministic nature of the SAR loop, there is a specific ratio between the input-referred noise of the comparator and the equivalent noise referred to the ADC. This ratio depends on the system parameters, with the comparator's noise typically ranging between 0.7 and 1, implying that 70% of the comparator's thermal noise manifests when referred to the system's input.

Once the comparator has decided, the output nodes are positioned at opposing supply rails. However, both outputs must reset to identical voltage levels, thus establishing a uniform starting point for the subsequent conversion. Switches are

interposed between the output nodes and V_{dd} to facilitate this equilibrium. In the reset state, these switches connect the output nodes to the upper supply rail. This results in an abrupt transition at the output nodes. Because of the parasitic coupling of the comparator's output and input, a corresponding step, known as the kickback of the comparator, manifests at the device's input. The magnitude of this step depends on the impedance present at the input of the comparator. Incorporating a pre-amplifier between the DAC and the comparator attenuates the kickback phenomenon caused by the diminished coupling factor from the output to the input.

In addition, when the reset is non-ideal, it is possible that the resulting output from V_{ss} falls marginally below V_{dd}, thus inducing a slight offset attributable to the preceding decision. A small offset relative to the positive output will be present when the positive output is at V_{ss}. In contrast, should the negative output be positioned at V_{ss}, the subsequent cycle will exhibit an offset relative to the negative output, creating a code-dependent error that leads to distortion.

6.2 Amplifier

With the comparator analyzed, the next component in the chain is the amplifier, which incorporates the tripping voltage in conjunction with one of the comparator outputs. This amplifier functions as a static gain block, amplifying the difference between the tripping voltage and a particular comparator output. This introduces an offset within the comparator chain with respect to the comparator metastable point.

Inverters are typically placed between the comparator and the capture latches, to reduce the loading of the comparator, and ensuring a digital output during the whole conversion. These inverters function analogously to open-loop amplifiers, amplifying the difference between the input voltage and the inverter's tripping voltage. By modulating this tripping voltage, an inverter can serve effectively as the amplifier within the signal processing chain, without adding any overhead.

The inverter tripping voltage is characterized by the input voltage at which the current through the NMOS transistor equals the current through the PMOS transistor. With the knowledge that the inverter is operating in strong inversion at this regime, the square law model applies, resulting in the following equation for the tripping voltage:

$$V_{trip} = \frac{V_{dd} - |V_{thp}| + V_{thn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} \tag{6.3}$$

with:

$$\beta_{n,p} = \mu_{n,p} C_{ox} \left(\frac{W}{L} \right)_{n,p} \tag{6.4}$$

and $\mu_{n,p}C_{ox}$ the device constants, $V_{thp,n}$ the threshold voltage of the NMOS and PMOS, $W_{p,n}$ the channel widths, and $L_{p,n}$ the channel lengths of the devices.

A clear correlation becomes evident between the inverter's tripping voltage and the sizing parameters of the device. By selecting a minimal channel length, the width can be modified, thereby influencing the tripping voltage with significant versatility, as illustrated in Fig. 6.5.

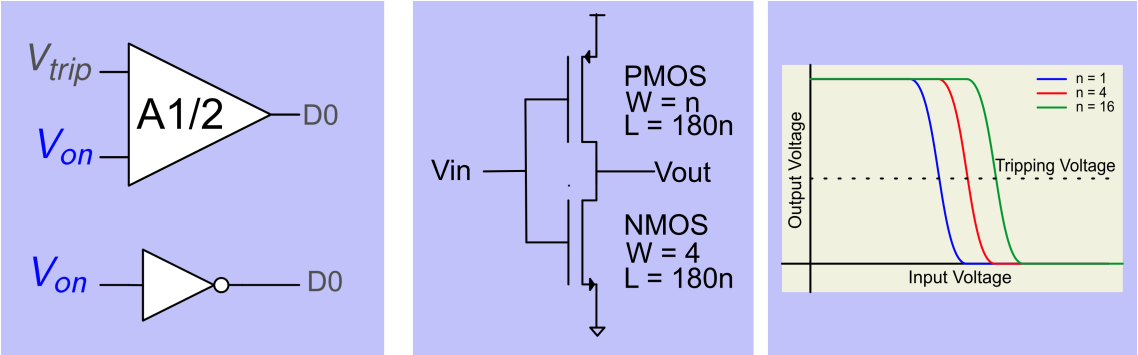


Figure 6.5: Inverter sizing, utilizing the internal tripping voltage.

Adjusting the inverter by altering the optimal ratio between NMOS and PMOS allows the tripping voltage to be placed below V_{meta}. The ratio of device constants, defined by μ_p/μ_n, is approximately 3 in the given technology. Consequently, for devices of equal strength, the PMOS must be three times larger than the NMOS. The comparator is designed to give the PMOS and NMOS devices equal strength making V_{meta} identical to the intrinsic tripping voltage of a 3/1 inverter. According to Eq. 6.3, positioning the tripping voltage below V_{meta} requires a larger NMOS than the baseline configuration.

Given that inverters are already present between the comparator and the capture latches, this approach eliminates the need for additional circuitry. Concurrently, it establishes a well-defined offset within the chain from the comparator to the capture latches, as shown in Fig. 6.6.

6.3 Capture latch

The primary function of the capture latch is to store the output of the comparator for subsequent digital processing. However, in cases of metastability within the comparator, the positive feedback of the capture latch increases the gain provided by the comparator, thus mitigating the likelihood of metastability-induced errors.

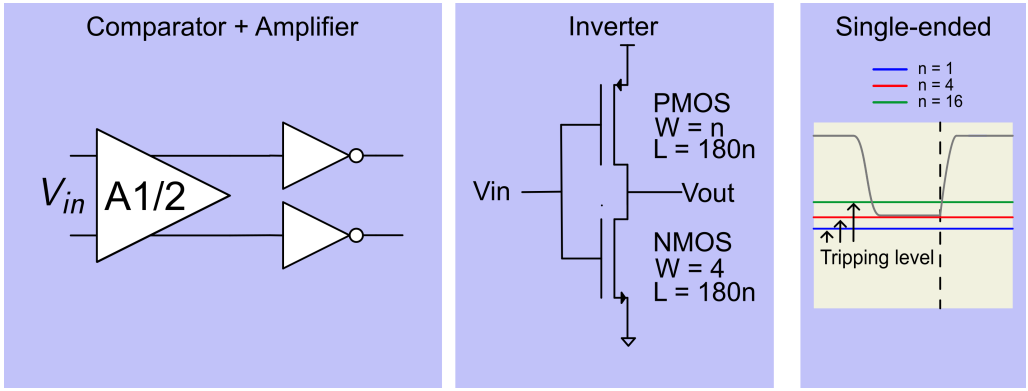


Figure 6.6: Comparator chain creating an offset between both outputs, with the gray line showing the transient response of a metastable comparator

The Reset/Set Latch (RS-latch) is a standard building block in IC design and can SET and RESET the corresponding output bit. The RS-latch consists of a latch created by two back-to-back inverters, creating positive feedback, and two pull-down switches to execute the SET and RESET operations. As illustrated in Fig. 3.1, all capture latches of the system are directly connected to the output of the comparator. Consequently, the necessity arises to mask the comparator's output via an enable signal, as demonstrated in the timing diagram in Fig. 6.7.

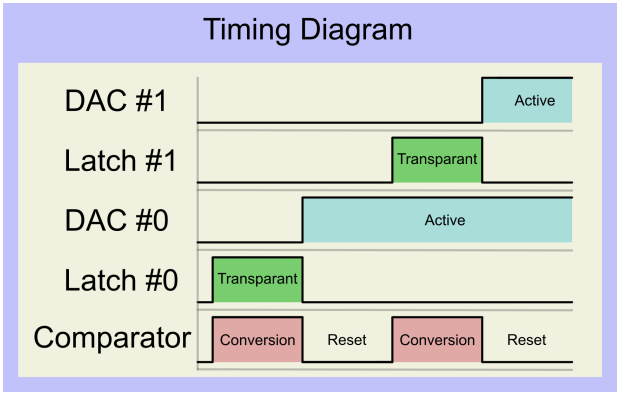


Figure 6.7: Timing diagram of a 2-bit SAR ADC.

During the comparator's conversion phase, the RS-latch is transparent following the output voltage of the comparator. Once the conversion is complete, the DAC is subsequently activated. The reset operation of the RS-latch can be executed asynchronously with the help of a reset signal generated by the SAR-logic. At the system level, an AND gate is required for masking the enable signal of the RS-latch. The inputs to the AND gate consist of the latch-enable signal and one of the comparator outputs, the latch-enable signal serving as the masking signal, as illustrated in Fig. 6.8.

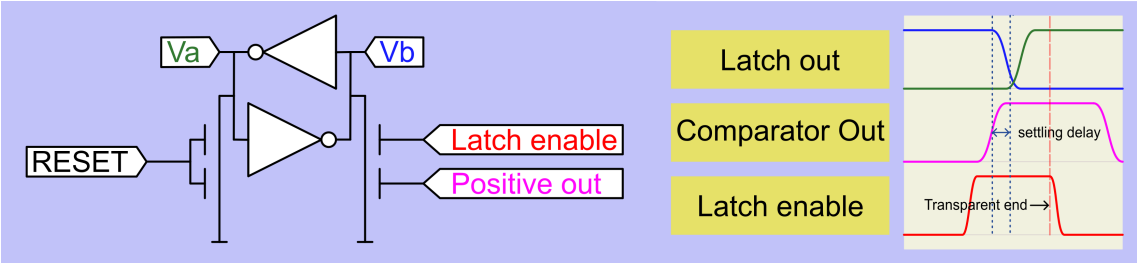


Figure 6.8: Voltage transients of an RS-latch.

On the left side, the RS latch is depicted. The pull-down mechanisms are used to RESET and SET the devices, where the SET operation incorporates an AND gate within the pull-down structure. The illustration on the right shows the transient response of the latch voltages, denoted by V_a, V_b, the comparator's output, and the latch-enable signal. The latch, analogous to the comparator, has three distinct regions: SET (positive out), RESET (negative out), and a metastable region.

The RS-latch, in its initial condition, resides in the reset state. To transition the RS-latch to the SET state, it is required that both inputs to the pull-down devices (Latch Enable and Positive Out) be at a high logic level, as shown in Fig. 6.9. The comparator output remains high during the transparent phase of the RS-latch. The dashed vertical red line highlights the end of the transparent phase. The propagation delay, or settling delay, is indicated by the two dotted lines, indicating the minimum required time for simultaneous activation of the latch-enable signal and the comparator's output latch. When both signals are active longer than this settling delay, the latch will transition to the SET state.

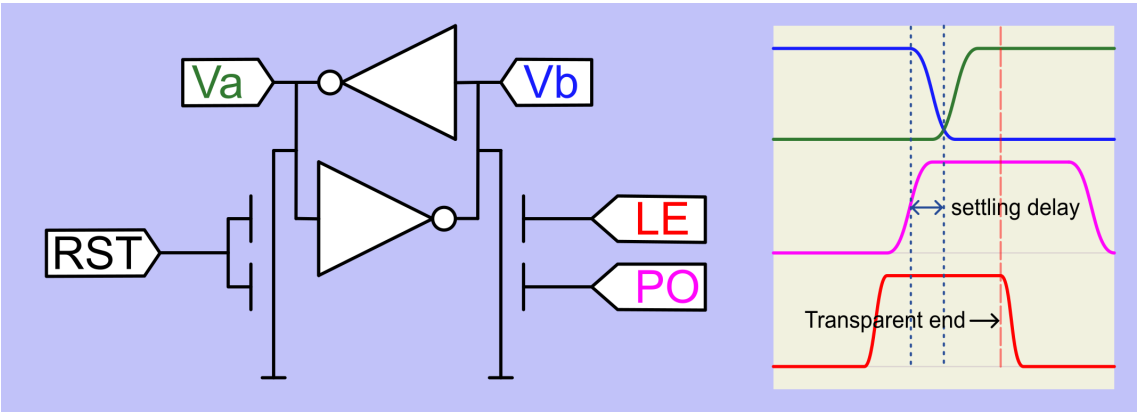


Figure 6.9: Setting of an RS-latch.

If the comparator has a harder decision, the output of the comparator will be valid. Therefore, the available time for both inputs of the AND gate to be valid is reduced. As illustrated in Fig. 6.10, the output of the comparator took too long to

obtain a valid response, leaving insufficient time to SET the latch. This is indicated by the settling delay lines ending later than the transparent phase.

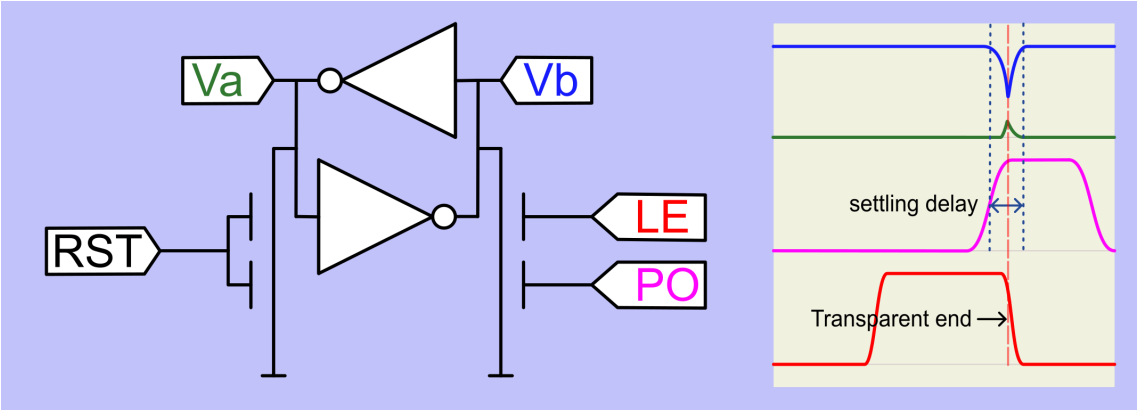


Figure 6.10: Not setting of an RS-latch.

In the case of metastability within the RS-latch, the endpoint of the settling delay coincides with the end of the transparent phase, as illustrated in Fig. 6.11. As a result of driving the RS-latch from a single side, the output node V_b is drawn below the V_{meta} threshold of the RS-latch. Once the transparent phase ends, both output nodes realign toward the device's intrinsic common mode voltage (V_{meta}), thus entering the regeneration phase of the latch, building up the gain to overcome the metastability.

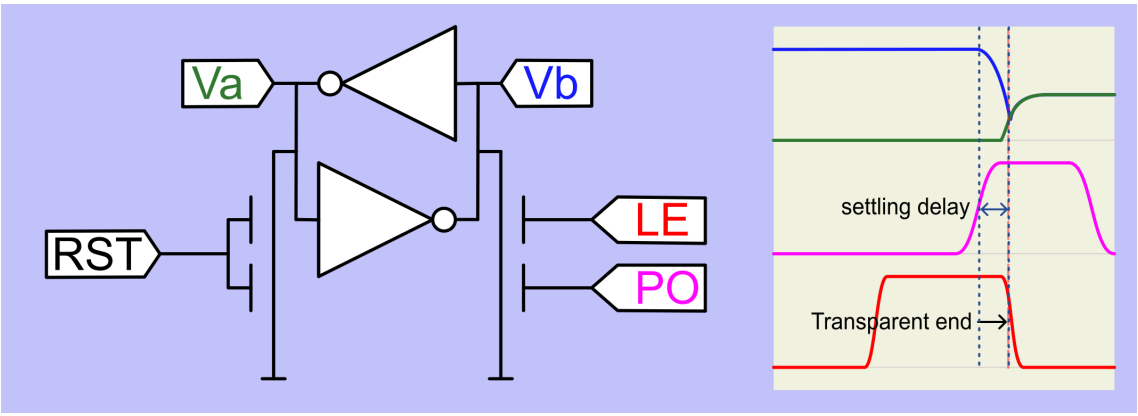


Figure 6.11: Metastability inside an RS-latch.

Minimizing settling delay will enhance the maximum accumulated gain of the comparator. To achieve a reduction in settling delay, the utilization of stronger (thus larger) pull-down devices is required. However, a downside of this approach arises as an increased time constant of the latch due to the larger pull-down devices, which results in more capacitive loading at the outputs. As indicated in Eq. 2.2, a larger capacitive load will reduce the τ of the system. In the Dual DAC ADC, the capture

latch benefits from the longest duration to resolve metastable errors. Degrading the timing constant of the latch to curtail the settling delay will reduce the cumulative gain across the entire chain, thereby deteriorating the BER.

6.4 Comparator Chain

A comprehensive analysis of the comparator in combination with the RS-latch chain can be performed by detailed examination of the individual components. Fig. 6.12, shows the total chain of a one-bit system.

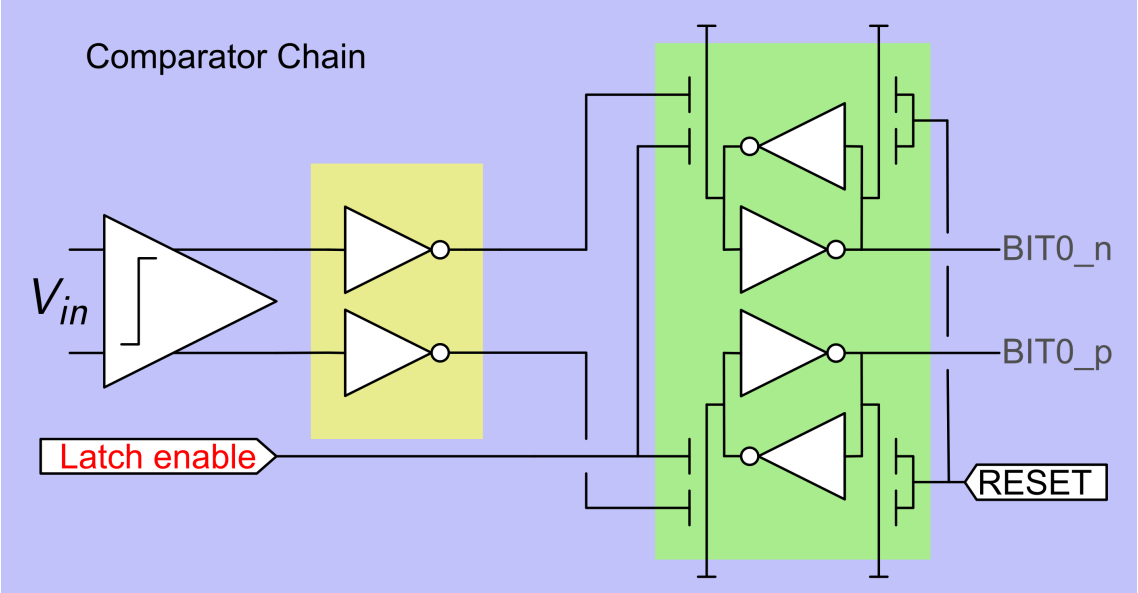


Figure 6.12: comparator followed by the skewed inverters (yellow) and two the capture latches (green).

Both outputs, indicated by $BIT0_n, BIT0_p$, are interfaced with their respective DAC elements (not shown in the figure). For an N-bit system, N times two capture latches will be placed and arranged in parallel, each accompanied by its distinct enable signals. The timing delays within the system have been characterized, including the comparator's delay t_{min}, the propagation delay of the inverter, and the latch settling delay. Together, these delays reduce the available time of the comparator, thus diminishing the effective gain. In addition, the interaction between the components moves the initial dead-zone, defined as the difference between the tripping voltage and V_{meta}, to a higher value due to the hystersis of the latch.

6.5 DAC element

The last components within the SAR loop are the DAC elements. The primary function of these elements is to generate voltage steps on the DAC, which facilitates the binary search algorithm of the SAR-ADC. For proper operation, each bit is associated with two DAC units that take half-steps in unison to achieve a complete step. In contrast, within the dead-zone, the steps of the units negate each other. Both DAC units must have their control signals directly from the two independent capture latches. Consequently, the DAC must wait until a valid response from the capture latch before executing a step, thereby creating additional time for the metastability to resolve itself.

Before going into the system-level intricacies of the DAC unit, it is necessary to select an appropriate switching scheme for the DAC. The constant common-mode monotonic switching methodology is employed in conjunction with top-plate sampling for the current analysis.

6.5.1 Constant common-mode switching scheme

A constant common mode monotonic switching scheme [9] is implemented, to keep the primary comparator at a consistent operational point throughout the conversion process. The monotonic switching scheme by itself does not constitute a constant common-mode configuration; it directly compares the input voltage after the sampling phase [10]. Based on the comparator outputs, the bottom plate of the capacitor connected to the positive or negative input are switched to V_{ss}, as illustrated in Fig. 6.13.

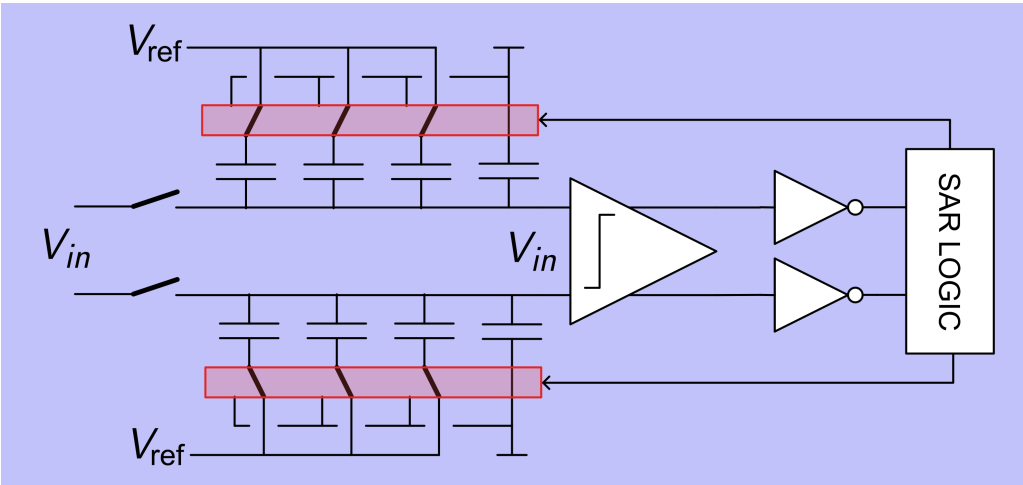


Figure 6.13: DAC switching monotonic.

By executing a discrete transition from V_{ref} to V_{ss} on the positive or negative node of the comparator, a reduction in the common-mode voltage from $V_{ref}/2$ to 0

is observed at the end of the cycle. To maintain a constant common mode operation, the capacitors can be split into half, applying the inverse step to the other input node of the comparator [9]. Using both outputs of the comparator alongside their complementary pairs, a 4-bit constant common mode monotonic switching DAC is illustrated in Fig. 6.14

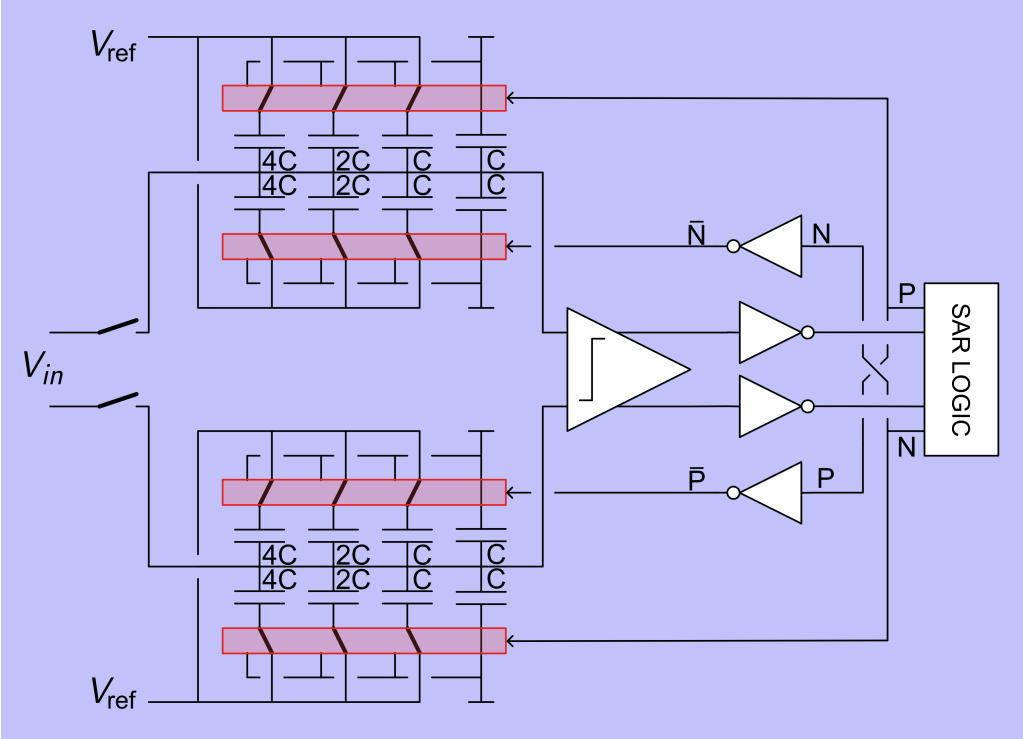


Figure 6.14: a 4-bit example of constant common mode monotonic switching scheme DAC.

During each decision, a voltage step is applied to the positive and negative sides of the DAC, thereby maintaining a constant common-mode voltage. This transforms the conventional monotonic switching scheme into a tri-level system with three distinct states: increment, decrement, and reset/sample. Note, a single bit is insufficient to represent a tri-level system. However, incorporating an enable signal facilitates the necessary switching logic of the DAC component.

6.5.2 DAC element

With the established switching scheme and defined requirements, the system-level design of the DAC element can be formulated. The enable signal, facilitated through (N)AND-gates, makes it possible to mask the control signal of the DAC. The identical physical capture latch employed within the comparator chain is also used inside the DAC element. As illustrated in Fig. 6.14, both control signals and their inverse are essential for the switching scheme. Using both outputs of the RS-latch, illustrated in

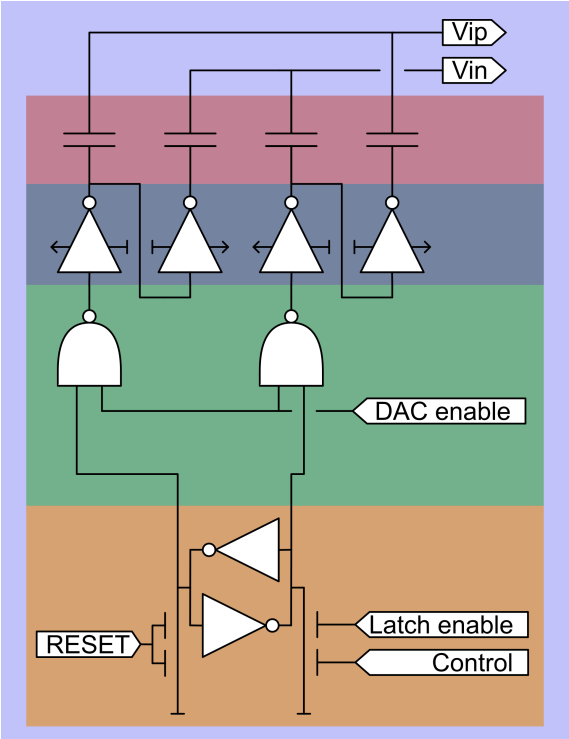


Figure 6.15: A single DAC unit with the required control signals.

Fig. 6.8, during a valid response, V_a and V_b are complementary, making it possible to use these outputs for nodes N and P, as shown in Fig. 6.14. Switches, implemented by inverters, enable the transition between V_{ss} and V_{ref}.

Fig. 6.15 shows the complete DAC element consisting of capacitors (red), switches (blue), DAC logic (green), and capture latches (orange). The capacitors and switches are standard devices. The DAC logic enables and disables the DAC-element.

In the reset/sample phase, the output of the DAC-element must be reset zero and exhibit a common mode of $0.5V_{ref}$. During this interval, the DAC enable signal remains low, thus producing a digital one at the output of the NAND gates. Following the chain, the leftmost inverter generates a digital 0 connected to V_{ip}, while the subsequent inverter produces a digital one connected to V_{in}. A sign inversion is incorporated on the right-hand side of the illustration to achieve the required conditions of the reset/sample phase. This inversion of the sign links the output of the first inverter to V_{in} and the second inverter to V_{ip}. Consequently, a differential zero is maintained during the reset/sample phase, with a common mode of $0.5V_{ref}$.

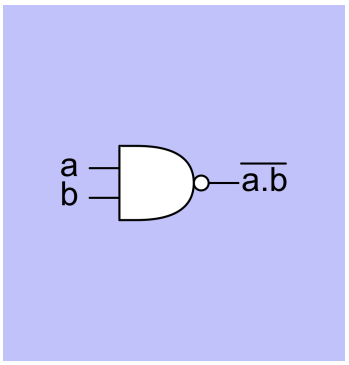
Once the DAC is enabled, the signals originating from the capture latch propagate through the NAND gates to the output of the DAC element. Only one of the two NAND gates undergoes switching during the transition. In case of metastability inside the capture latch, the DAC element must wait for a valid response before

proceeding with a transition. When the capture latch output nodes are at V_{meta}, the two digital NAND gates must remain high, creating the following truth table in Fig. 6.16a.

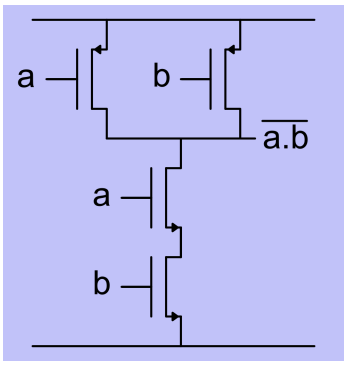
a	b	$\overline{a.b}$
0	0	1
0	1	1
1	0	1
0.5*	x	1
x	0.5*	1
1	1	0

* 0.5 representing V_{meta}

(a)



(b)



(c)

Figure 6.16: (a) Truth-table of modified NAND-gate. (b) System-level NAND-gate. (c) Transistor-level NAND-gate.

Upon deliberate skewing of the NMOS and PMOS dimensions within the NAND gate, the tripping voltage is elevated above V_{meta} of the capture latch. In the event of metastability, the digital NAND gate registers a digital 0 at its input. Despite the active DAC, the digital 0 of the capture latch keeps the DAC element in the reset/sample phase.

Chapter 7

Bit Error Rate

Following the analysis of the system-level enhancements of the dual-DAC ADC, a quantitative comparison can now be made between the systems. The Dual DAC ADC is designed so that the system's dead-zone is close to the lower limit of the system. Both systems utilize the same components, facilitating a direct comparison. The mathematical model of the comparator, as defined in Eq. 6.1, is used for both the capture latches and the comparator itself. The primary distinction between both components is the lack of t_{min} for the capture latch. The capture latch is placed directly between the supply rails, delivering the highest possible τ. In contrast, the strong-arm latch comparator features a differential pair coupled with a tail current placed below the latch, ultimately reducing the supply voltage of the latch. For simplicity , both systems' time constants are assumed to be equal.

7.1 System definitions

To construct a statistical model, it is essential to define the parameters of the system. A statistical model is defined in which the maximum gain accumulation that can be achieved is based on the proximity of that input signal to the closest trip-point and the input voltage distribution. For the case of a synchronous SAR ADC, the input distribution itself has a negligible effect on the BER [6]. Consequently, the ADC will operate with a uniform distribution equal to Full-Scale (FS) of the system.

The system may experience metastability up to N instances for an N-bit ADC. In scenarios where the DAC is waiting for a valid response from the ADC, the distinction between top-plate sampling and bottom-plate sampling becomes inconsequential. The comparator enters a metastable state when the input voltage is close to the tripping voltage of the comparator. By superimposing this regime on each possible decision, a map is made where the system exhibits metastability; see Fig. 7.1.

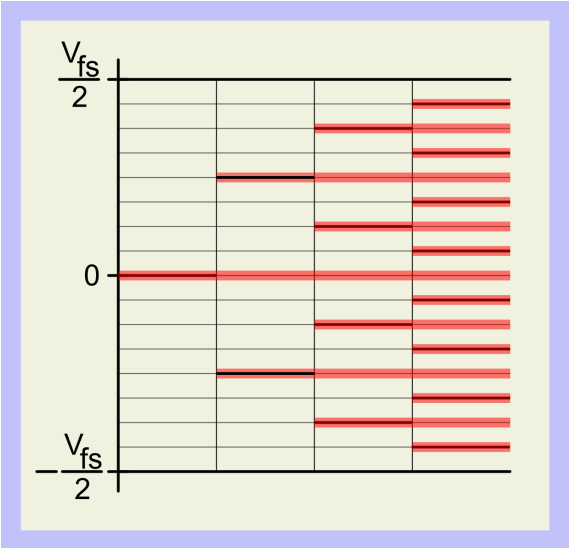


Figure 7.1: 4-bit ADC comparison regions with the metastable area highlighted in red.

The width of the red regions equals $V_{od,min}$, defined as the voltage of the supply rail divided by the total gain accumulated in the system. A single decision is available for the single-DAC ADC, whereas the dual-DAC ADC benefits ultimately from two cycles.

DAC settling is often considered a fixed delay element, which reduces the effective available time for the system to accumulate gain. However, DAC settling does not diminish the available time for a synchronous SAR ADC. To resolve metastability within this cycle, the subsequent cycle must be an easy decision for the comparator. Metastable decisions are characterized by an input voltage near the comparator's tripping point. In contrast, an easy decision is identified when the input voltage is distinctly not near this point, quantified as $>V_{od,min}$. Should metastability be resolved within the subsequent cycle, the DAC must adjust by no less than $>V_{od,min}$ to ensure an easy decision. Given that $V_{od,min}$ is presumed to be in maximum in the microvolt range, the time required for the DAC to settle to achieve $>V_{od,min}$ is insignificant.

The accumulation of gain is visualized in Fig. 7.2, where the capture latch and the comparator share the same τ. The transition between the capture latch and the comparator is executed seamlessly, thus eliminating any artifacts in the plot. The logic delay of the system, represented by t_{logic}, is illustrated at the end of the conversion process. The capture latch exclusively facilitates exponential gain, while the comparator exhibits a linear and exponential gain combination. The capture latch serves as the primary gain block in a dual-DAC system, because during a metastable decision the capture latch has a maximum of three times longer regeneration phase

to accumulate gain. In contrast, in a single-DAC configuration, the contributions of the comparator and capture latch are approximately equivalent. The comparator has a total of half a cycle to accumulate gain (including the pre-amplification phase), while the capture latch has a maximum of half a cycle to accumulate gain.

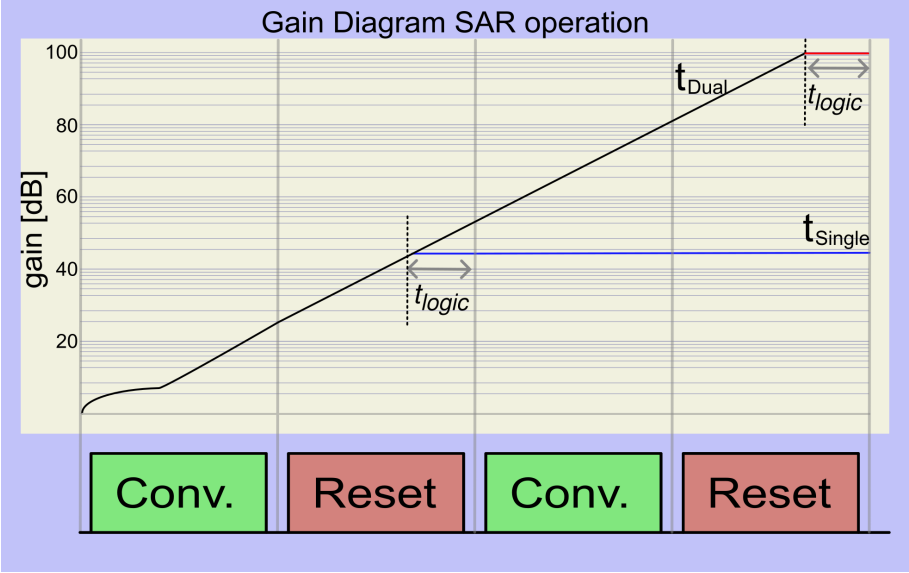


Figure 7.2: Gain accumulation in the chain Single and Dual DAC ADC.

Dual-DAC systems partition the initial metastable point into two different smaller metastable points. Calculating $V_{od,min,dual}$, the probability of falling within one of the two metastable regions is double, directly doubling the probability for the BER. as illustrated in Fig. 7.3.

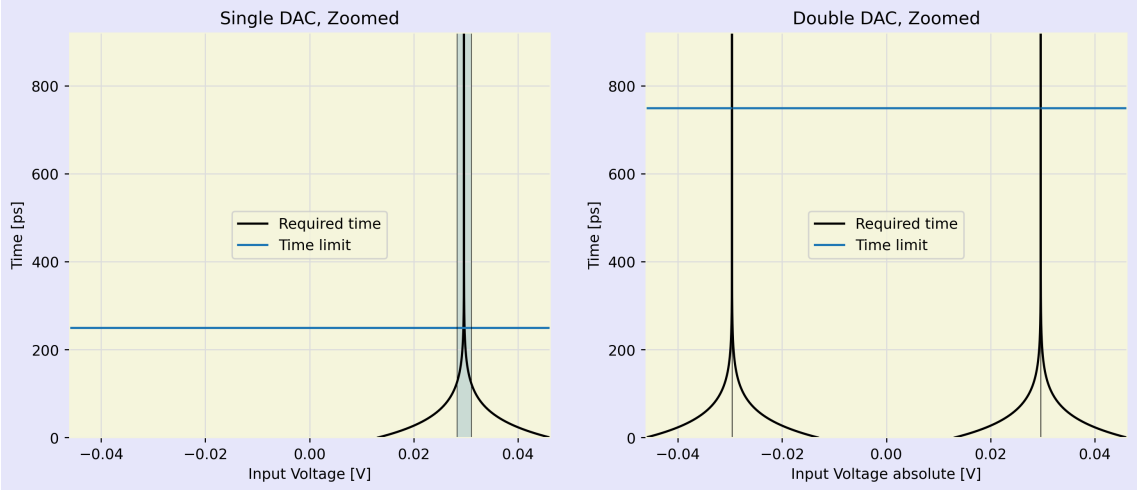


Figure 7.3: Available time versus needed time for a metastable decision.

7.2 Statistical model

The amount of possible metastable points in N conversions multiplied by $V_{od,min}$ creates a BER estimate for a uniform distribution.

$$P_{meta} = \frac{V_{od,min}}{V_{ref}}(2^N - 1) \tag{7.1}$$

This assumes that each metastable error exhibits the same level of catastrophic failure. However, in practical scenarios, metastable errors with a magnitude of a single LSB fall typically fall within the system's noise floor. In contrast, a metastable event in the MSB decision leads to a 2^{N-2} LSB error. It influences substantially the output code more than a metastable event occurring four bits below the MSB (MSB-4).

Only a single metastable conversion region is feasible for the MSB decision, as outlined in Fig. 7.1. In contrast, the MSB-1 decision has two discrete metastable regions, thus doubling the probability of encountering one of these metastable regimes. Extending this conceptual framework for an MSB-A decision, the conversion process covers 2^A metastable regions. Using this understanding, P_{meta} can be derived based on LSB errors, as shown in Tab. 7.1.

Table 7.1: p_{meta} with the LSB error amount.

LSB erorr	P_{meta}		P_{meta} cumulative sum	
	Dual DAC	Single DAC	Dual DAC	Single DAC
±256	2.56e-10	2.09e-05	2.56e-10	2.09e-05
±128	5.13e-10	4.17e-05	7.69e-10	6.26e-05
±64	1.03e-09	8.35e-05	1.80e-09	1.46e-04
±32	2.05e-09	1.67e-04	3.85e-09	3.13e-04
±16	4.10e-09	3.34e-04	7.95e-09	6.47e-04
±8	8.21e-09	6.68e-04	1.62e-08	1.31e-03
±4	8.21e-09	1.34e-03	2.44e-08	2.65e-03
±2	4.10e-09	1.34e-03	2.85e-08	3.99e-03
1	2.05e-09	6.68e-04	3.05e-08	4.65e-03

Notable attention is warranted for the LSB decision. A metastable error during the LSB conversion phase requires no additional DAC steps, confining the resultant code error to a maximum of 1 LSB. Suppose that the capture latches in the system are erroneously set to zero during the metastable state of the LSB decision, while they should have been zero, the digital output code remains correct. Consequently, it becomes feasible to generate exclusively positive or negative code errors dependent upon the initial states of the capture latches.

Furthermore, should the input signal exhibit a non-uniform distribution, it becomes imperative to integrate the input signal distribution around the region of metastable points, ensuring an integration width equal to $V_{od,min}$.

Metastability errors of 1-LSB have the highest probability of occurring when neglecting all noise sources in the system. However, noise does not eliminate metastable occurrences; instead, it delineates a convolution between Probability density function (PDF) of noise and metastable events [11]. A Gaussian distribution models the noise in the comparator; consequently, this noise can create erroneous decisions, culminating in a code error.

By simulation of an N-bit ADC, code errors can be extracted depending on the noise density of the comparator. The combined BER can be found by convolution of the respective PDFs. With an increased noise density within the system, more metastable points are obscured within the noise floor, as shown in Fig. 7.4. Consideration of three distinct noise values reveals that, for V_{n1}, only metastable points corresponding to 1 LSB reside within the noise floor. In contrast, for V_{n2} and V_{n4}, the errors associated with 2 and 4 LSBs due to metastability are encapsulated within the noise floor, respectively.

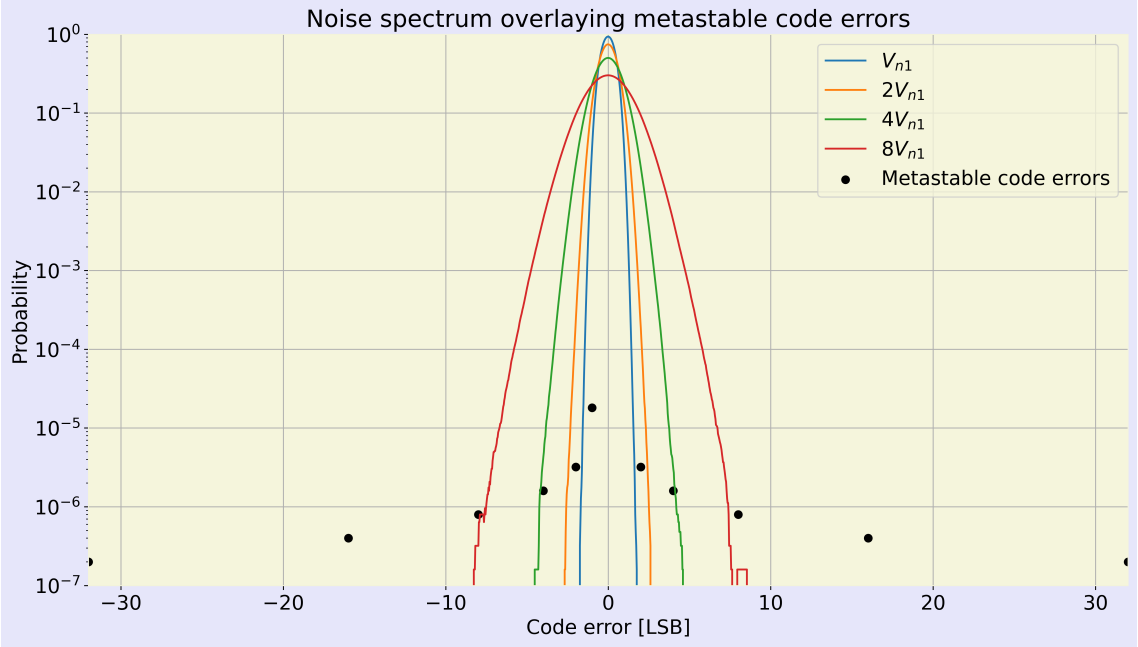


Figure 7.4: Three different noise values, hiding the metastable points inside the noise floor of the system.

As an initial thought, this appears to represent a trade-off between noise and metastable states. However, the application's noise requirements constrain the system's free variables for optimization. With the assumption that LSB errors of magnitudes 1 and 2 are hidden within the noise floor. The BER can be obtained

from Tab. 7.1 by examining the cumulative sum column up to an LSB error of 4, with a resulting BER of 2.65e-3 and 2.44e-8 for dual DAC ADC and single DAC ADC, respectively. This signifies an increase of 8e7 times of the BER.

7.3 Simulation results

An alternative to the statistical method is to implement a simulation model for the system and simulate a very large number of input points. The individual components have been analyzed in Chapter 6, together with the creation of their mathematical model. In the absence of noise within the system, the statistical analysis results are anticipated to correspond to the simulation results.

Using the same system parameters as in the Tab. 7.1, the simulation results show close to identical BER performance for both systems, as illustrated in Fig. 7.5. The red markers denote the calculated values of P_{meta} as presented in the Tab. 7.1. Beyond these calculated P_{meta} points, there are also points in between these points, be it with much lower probability. These metastable points represent metastable code errors with a power of three. Such errors arise when the capture latch of the N-th decision remains metastable during the comparator stage of the (N-2) decision, leading to an additional bit error.

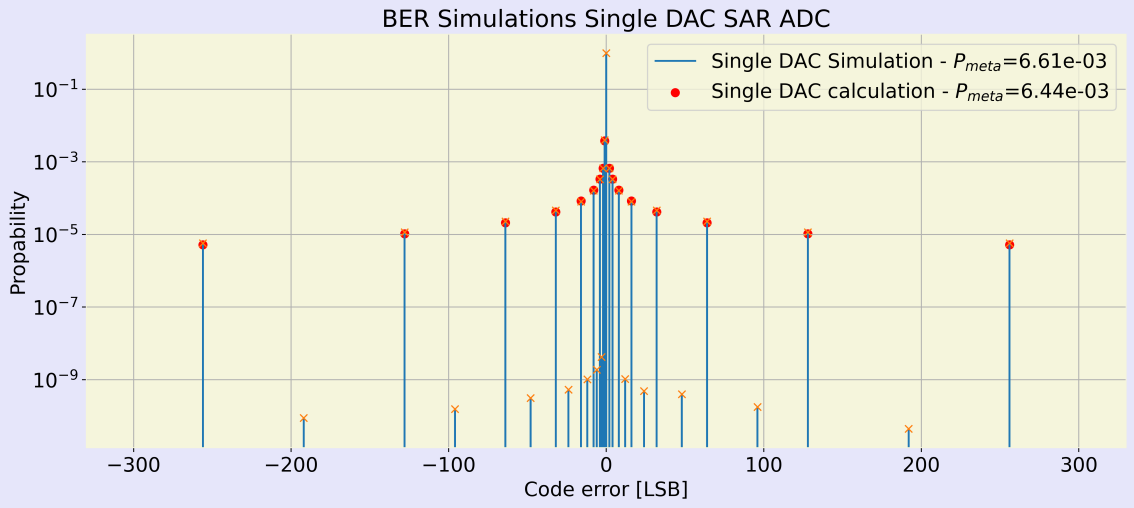


Figure 7.5: Single DAC SAR ADC BER measurement results.

As the likelihood of metastability in general is very low, all parameters have been tuned to increase the probability of a bit-error, in order to get meaningful results from the simulation. Hence, the system operates at the threshold of its capabilities to employ the simulation model and determine an effective BER for the dual DAC system. This implies a slow time constant relative to the clock period, thus necessitating a substantial dead-zone width to adhere to the lower boundary

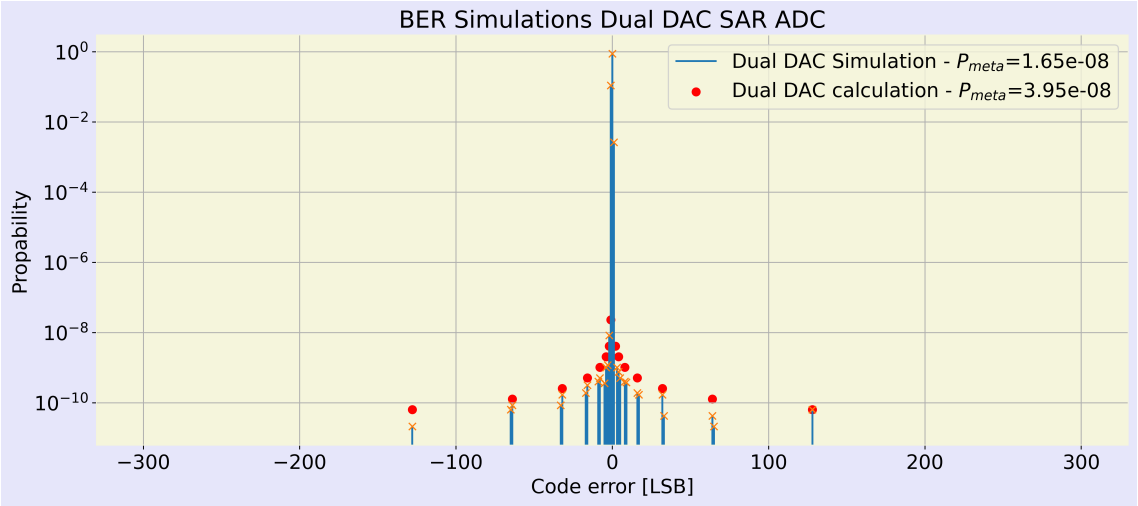


Figure 7.6: Dual DAC SAR ADC BER measurement results.

delineated in Chapter 5.2. Due to this considerable dead-zone width, the system functions in a domain where false triggers of the dead-zone occur due to the DAC settling phenomenon (as explained in Chapter 5.1.2). This induces additional 1-LSB code errors, which diminishes the effective resolution of the system. The dual DAC SAR ADC simulations are shown in Fig. 7.6.

A clear indication of the reduction in effective resolution was observed, characterized by a significant ± 1 LSB code error. Furthermore, the separation of dead-zone width defines metastablity induced code errors into two distinct bins. This partitioning of code errors is intrinsically linked to the dead-zone width of the system.

7.4 Comparison

A comparison between the single-DAC and dual-DAC systems reveals that the dual-DAC configuration results in substantially more accumulated gain during the conversion cycle, thereby reducing BER. In addition, the maximum potential code error that the dual-DAC system can incur is reduced by a factor of two compared to the single-DAC system. With both systems operating under identical conditions, the dual-DAC architecture demonstrably exceeds the performance of the single-DAC arrangement, as evidenced in Fig. 7.7.

Increasing the system's sampling frequency decreases the effective time available for both the latch and the comparator to achieve sufficient gain, thereby worsening the BER. At a theoretical sampling rate of 250 MSPS, the single-DAC system does not produce a code-error-free conversion, while the dual-DAC system achieves a BER of 10^{-6}. By dividing the BER of the dual DAC system against that of the single

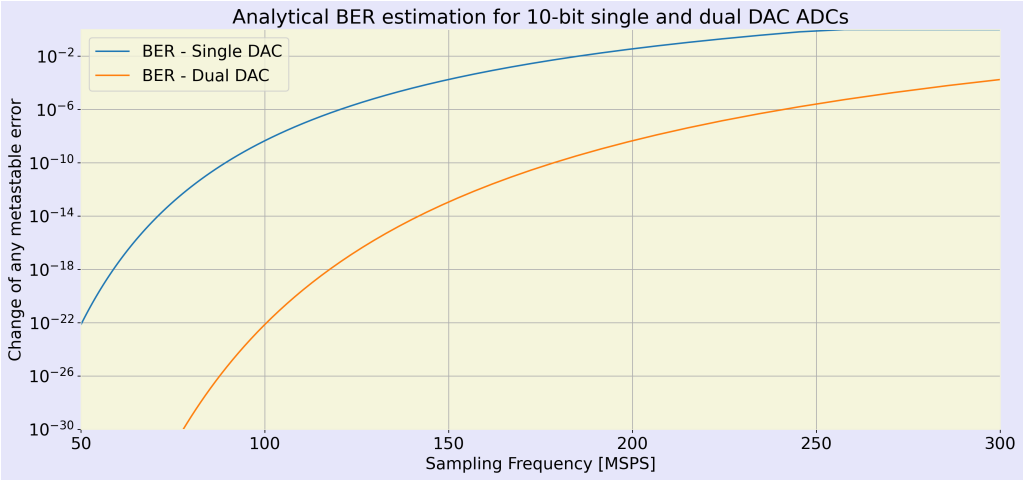


Figure 7.7: Analytical calculated BER comparison between a 10-bit single and dual DAC ADC swept over a sampling frequency.

DAC system, a quantifiable metric can be established to determine the enhancements. Using an identical time constant for the comparator and the latch, both systems display comparable exponential gain profiles over time.

As explained in Section 6.3, in most cases a capture latch exhibits a smaller τ than a comparator and a ratio could be inserted between these two time constants. Changing these time constants slightly affects the benefits of the system. However, the primary advantage of the the Dual-DAC system over the Single-DAC counterpart remains intact, as demonstrated in Fig. 7.8.

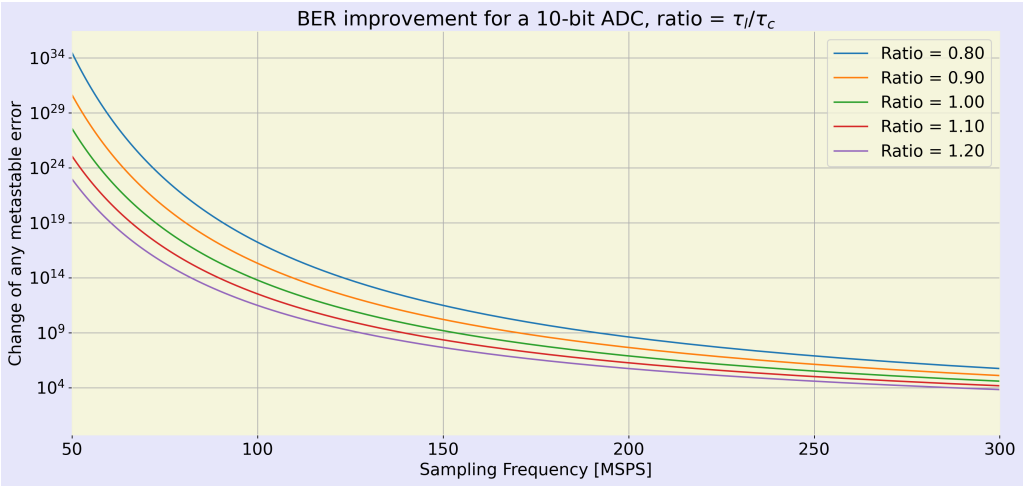


Figure 7.8: Normalized advantage between the single and dual DAC systems, with different timing constants between the comparator and the latch.

Chapter 8

Implementation of test-chip

Following a comprehensive system analysis, a test chip will be fabricated using 180-nm TSMC technology. Its primary objective is to validate the dual DAC SAR ADC enhancement compared to the single DAC SAR ADC. To prove this evaluation, the systems must function at the maximum achievable speed, increasing the likelihood of metastable events. This is because a bit error is so unlikely in normal circumstances that a reliable measurement of BER will take an extremely long time (multiple days or more). Additionally, the system should be able to transition between dual DAC and single DAC modes of operation, to accommodate a direct A-B comparison with the flick of a switch. The emphasis is not on achieving low power consumption or developing a high-performance ADC, which leads to different design choices for the system. A 10-bit ADC has been selected to balance noise, mismatch, and resolution requirements. This chapter will show an overview of the implementation on transistor level of the different blocks and their corresponding design choices. Implementing the system's components requires a high-level noise budgeting analysis.

8.1 Noise-Budget

Several system components contribute to noise, reducing the effective resolution of the ADC. Sampling noise, quantization noise, jitter, and thermal noise represent the primary sources of error within the system. By mitigating these noise factors, it becomes feasible to detect smaller metastable errors (1, 2, 4 LSB) up to the thermal noise floor.

The budget is chosen such that each noise source introduces approximately equivalent amounts of noise to the system. This facilitates the determination of the limit of the different noise sources.

8.1.1 Sampling noise

The allowable level of sampling noise depends on the Dynamic Range (DR) and FS of the ADC. An increase in the sampling capacitor will lead to a reduction in the sampling noise. The effective sampling capacitor intrinsic to the SAR ADC is equivalent to the total Capacitor DAC (CAP-DAC) value. A large CAP-DAC value will result in a larger settling time of the DAC for the same power consumption. The on-resistance of the switches influences the DAC's settling time in conjunction with the capacitor's size. An increase in the size of the CAP-DAC results in larger capacitive loads, which increases the settling time if the same switches are used. Consequently, the design goal is to minimize the sampling capacitor to achieve the highest feasible operating speed with minimal power consumption.

The minimum size sampling capacitor is calculate to be

$$C_{sampling} = \frac{8kT \cdot \text{margin}_{\text{noise}}\text{DR}^2}{V_{fs}^2} \tag{8.1}$$

with k the Boltzmann constant, T the temperature in Kelvin, V_{fs} the full-scale voltage, DR the wanted dynamic range, and $\text{margin}_{\text{noise}}$ the noise margin. The noise margin is a number that is used to make room in the budget for all sources of noise and is chosen to be equal to six. Maximizing the FS voltage of the systems mitigates the need for a large sampling capacitor. For a 10-bit system, a dynamic range of 1024 is achieved coupled with a FS voltage of 1.5 [V]. To satisfy the noise budget, a total sampling capacitance of 62 fF is required, generating a sampling noise of 260 μV_{RMS}.

8.1.2 Quantization noise

The ideal quantization process of the ADC introduces an irreversible error in the system's output code. The continuous-time analog signal is processed to a quantized output, with the quantization consisting of N-number of bits. The smallest step after quantization is equal to full-scale voltage V_{fs} divided by the dynamic range of the system. Increasing the number of bits will reduce the system's quantization noise. The quantization noise can be calculated using:

$$\overline{V_{q,noise}^2} = \frac{\Delta}{12} \tag{8.2}$$

with Δ equaling a single LSB, defined by FS/DR.

8.1.3 Thermal noise

To avoid hiding the small metastable errors by the inherent thermal noise of the system, the thermal noise should adhere to same fraction of the budgets as the

sampling noise. This parity facilitates the detection and quantification of a 1 LSB code error within the system, thereby enhancing the precision of BER assessments. Only more significant metastable errors remain detectable when minor metastable errors are submerged below the noise floor. The more prominent errors, which are less frequent, contribute to an improved BER, albeit complicating the validation of performance enhancements between dual-DAC and single-DAC configurations.

8.1.4 Other noise sources

Other noise sources, such as 1/f noise or jitter, will not be accounted for, as the noise sources that have been analyzed are the primary error sources of the system. The chosen noise-margin of six still builds in sufficient headroom for those additional noise sources.

8.2 Comparator Chain

The comparator chain, as depicted in Fig. 8.1, is one of the most critical components in the chain, determining the speed and reliability of the system. Many architectures are available for comparators, including widely utilized designs such as the strong arm latch [3] and the double tail comparator [12]. In this design, the strong-arm latch has been selected because of the comparable performance shown by both architectures within this specific technology node.

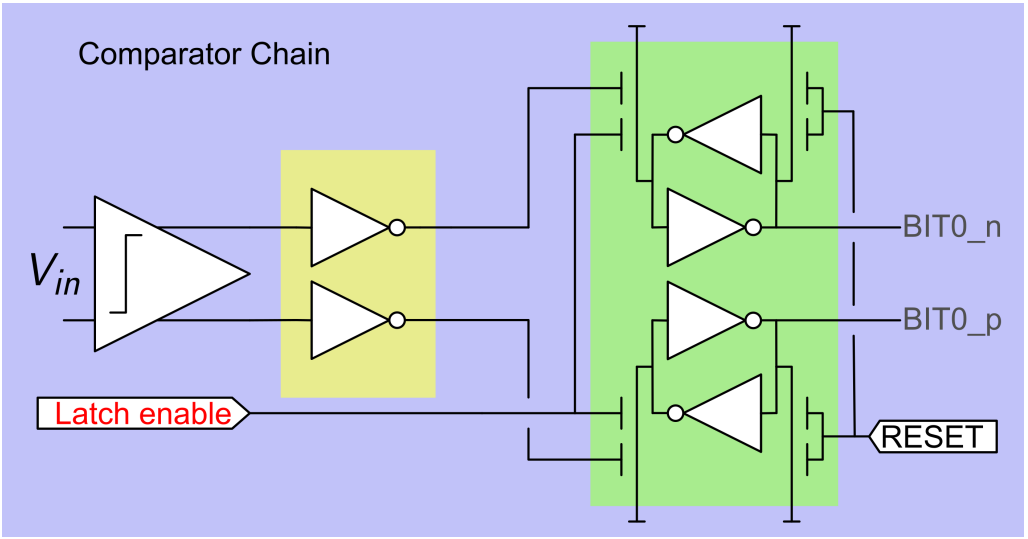


Figure 8.1: Comparator Chain

The strong-arm latch architecture consists of an integrated preamplifier coupled to the latch, as illustrated in Fig. 8.2. Due to several delay elements from the comparator to capture latch, the design of the comparator is optimized to achieve

minimal propagation delay and low time constant, with a primary emphasis on reducing propagation delay.

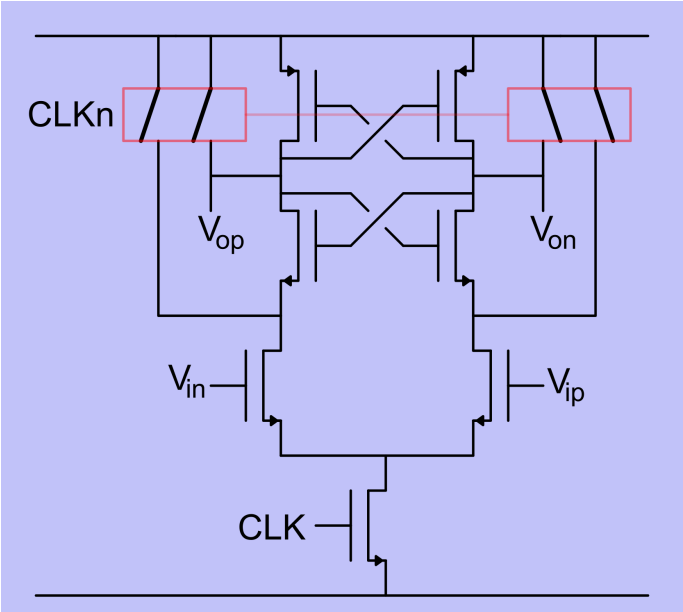


Figure 8.2: Strong arm latch comparator.

The kickback of the comparator depends, among others, on the parasitic capacitance from the output to the input of the comparator. The differential pair placed below the latch is optimized for maximum conversion speed, accompanied by the largest pre-amplification. Consequently, this configuration results in relatively large input pairs with significant parasitic capacitances, leading to considerable kickback during the reset phase. The magnitude of the kickback and the resulting common-mode and differential-mode variations depend on the impedance observed at the comparator's input. With the smallest impedance present, a smaller absolute voltage change will be present. To mitigate the absolute value of the voltage jump, it is necessary to decrease the impedance, which consequently increases the CAP-DAC. Alternatively, minimizing kickback could be achieved by reducing the parasitic capacitance from the output to the input.

Another important property of the comparator is its driving capability. The comparator, and by extension, the inverters behind the comparator, must drive (the number of bits) ten capture latches. An optimal configuration was determined with a fan-out of three inverters: the initial inverter in the chain is skewed to ensure that the tripping voltage of the device remains below V_{meta} of the comparator. The subsequent two inverters are optimized for minimal propagation delay given the required load. This results in an added delay of 30 ps in the chain.

The capture latches used are RS-latches. The latch is close to the minimum size to obtain the fastest time constant due to the smallest self-loading. The pull-down

transistors are sized such that the latch can always be SET and RESET over all corners and mismatch.

Two-time delays are observed in the sequence, as depicted in Fig. 8.3, for various input voltages. From the comparator to the output of the inverters, a propagation delay of 30 ps is incurred. Subsequently, an additional propagation delay of 40 ps is encountered from the inverter to the capture latch.

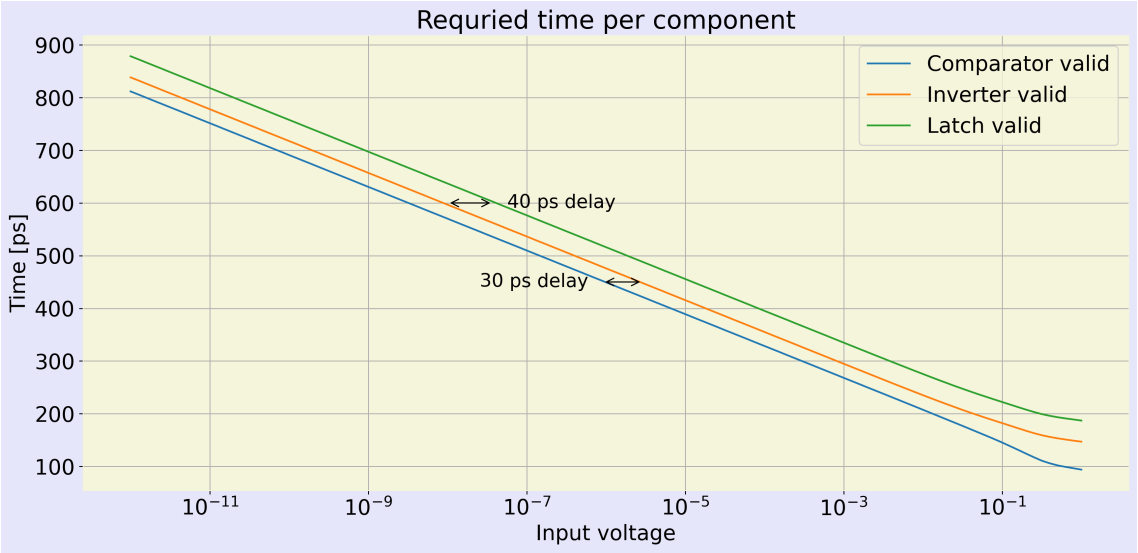


Figure 8.3: Required time for a valid response per component for the final design.

8.2.1 Validation

To validate the complete signal processing chain, a resettable SAR-ADC scheme was used [13]. The intrinsic non-idealities of the comparator, such as the hysteresis and offset, present significant challenges in accurately simulating the system's dead-zone. The dead-zone is created after the comparator with the help of the inverters; this makes it immune to the offset of the comparator. However, the comparator's hysteresis must be carefully considered, as it constitutes a code-dependent offset arising from the comparator's imperfect reset characteristics. In addition, depending on the width of the designed dead-zone, the hysteresis may be of the same order of magnitude as the width of the dead-zone. In addition, the hystersis of the capture-latch increase the dead-zone width, with respect to the inverter skewing.

The switching scheme presented in [13] facilitates the detection of an individual comparator's offset and hysteresis parameters. By employing this scheme for both capture latches, the hysteresis behavior in the vicinity of the dead-zone tripping points is precisely simulated. A Monte Carlo analysis encompassing 200 simulation points was performed to incorporate variations due to the spread of the device and corner conditions, as shown in Fig. 8.4.

Figure 8.4: Validation chain of the system running at 100 MSPS.

Permitting the system to operate at a diminished sampling frequency will result in a larger gain accumulation, thereby decreasing the width of the dead-zone.

8.3 Switching scheme

Various power-efficient switching schemes are presented in literature, The criteria for the switching scheme include maintaining a constant common-mode and achieving relative low power consumption. As mentioned above, power consumption is not critical for this design. However, a switching scheme with reduced power consumption facilitates a more straightforward reference design. Consequently, a constant common-mode monotonic switching scheme has been implemented.

8.4 Capacitve DAC

The CAP-DAC comprises both the DAC logic and the capacitive elements. To satisfy noise requirements, the total capacitance of the CAP-DAC must be at least 62 fF, adhering as closely as possible to this value. A small CAP-DAC value requires smaller switches, which require less power and facilitate a more convenient reference buffer, enhancing the overall sampling frequency. The capacitive values within the CAP-DAC can be designed orthogonally from the device mismatch [14]. The main drawback of improved mismatch performance is increased area consumption, following Pelgrom's law [15].

8.4.1 Capacitor Sizing

In addition to the noise requirements of the ADC, the practicality of the design significantly influences the sizing of the capacitor. Both the bootstrapped sampling switch and the comparator are directly connected to the top plates of the capacitors. These connections introduce additional parasitic loading, reducing the full-scale voltage of the system. Furthermore, the (nonlinear) kickback induces distortion on the CAP-DAC voltage, degrading the system's overall performance. A trade-off has been made to increase the total CAP-DAC value, keeping the distortion components from the kickback below the quantization noise of the system. Consequently, a new minimum capacitor value of 350 fF has been chosen.

A 10-bit binary ADC requires a total of $2^9 - 1$ units of capacitors, each having a capacitive value of 0.6 fF. Due to the switching scheme used, the requirement of the number of unit capacitors is doubled to maintain a constant common mode, resulting in $2 \cdot 2^9 - 1$ capacitors. In addition, the dual DAC requires two DAC elements per bit, doubling the required capacitors once more, resulting in $4 \cdot 2^9 - 1$ capacitors. This results in a unit size of 0.17 fF. It should be noted that a unit capacitor of 0.17 fF represents a diminutive capacitance in this specific technology;. Such a minuscule unit capacitance is associated with relatively significant parasitic top- and bottom-plate capacitors, ultimately diminishing the full-scale range of the device.

To increase the unit-capacitor value, the CAP-DAC can be split into two segments with a bridging capacitance, thereby creating a split-capacitor array CAP-DAC [16] (see Fig. 8.5). The CAP-DAC of a 6-bit single-ended ADC is shown, with the capacitor array partitioned into two segments, forming an MSB and LSB side. A capacitive division is present from the MSB side to the LSB side using a bridging capacitor. This bridging capacitor creates an attenuation between both sides, improving the unit capacitor value while maintaining the effective total CAP-DAC capacitance.

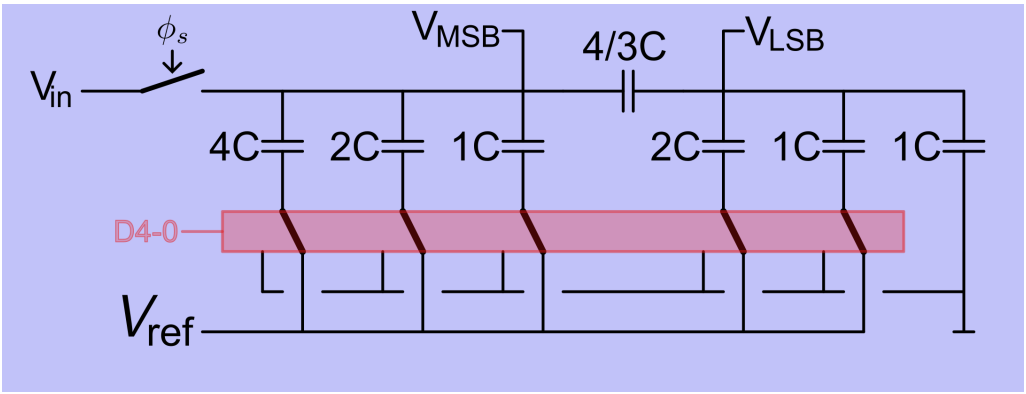


Figure 8.5: 6-bit ADC split capacitor-array network.

The attenuation depends on the bridging capacitor and all the (parasitic) attenuation capacitors placed on the LSB side. For a correct operation, this attenuation should be precisely defined. Any minor deviation of the attenuation capacitor leads to a wrong gain on the LSB side, thereby changing the effective voltage steps of the DAC for the LSB's. To control this attenuation factor, a two-step calibration is present in this design, consisting of a coarse and fine calibration. The coarse calibration is implemented by several unit capacitors placed on the LSB side, whose bottom plate can be grounded or left floating. This changes the effective attenuation on the LSB side, thereby adjusting the attenuation between the MSB and the LSB elements. Fine calibration is implemented by changing the reference voltage on the LSB or MSB side. Each capacitor array has an independent reference that can be tuned externally from the chip. Changing the reference voltage directly changes the values of the corresponding bits. Doing so for the MSB and LSB bits independently allows for fine calibration of the LSB values

For the design of a 10-bit ADC, a 9-bit DAC is required, resulting in 511 unit capacitors when a binary structure is used. Using the CAP-DAC split capacitor array yields a 5-MSB/4-LSB ratio of capacitors. Consequently, the MSB weights are [16, 8, 4, 2, 1], while the LSB weights are [8, 4, 2, 1]. The dominant capacitor segment, the MSB segment, requires only 31 units. Increasing the unit capacitance from 0.17 fF to 3 fF.

8.4.2 Mismatch

The mismatch can be systematically examined using the established CAP-DAC architecture along with the specified unit capacitor. The mismatch of the capacitors is directly linked to the accuracy of the CAP-DAC. For a correct operation, the requirements are defined to have both the Integral Nonlinearity (INL) and Differential Nonlinearity (DNL) of the system remain below 0.5 LSB. In the context of a binary DAC, DNL is defined as:

$$\text{DNL} < \sigma_{lsb} \cdot 2^{NOB/2} \tag{8.3}$$

with σ_{lsb} the standard deviation of the mismatch and NOB the number of bits of the system. Rewriting the formula to find the standard deviation requirements yields

$$\sigma_{lsb} = 0.5 \cdot 2^{-NOB/2} \tag{8.4}$$

For a 10-bit ADC with a dual DAC switching scheme, a mismatch requirement of 2.2% is required. However, the adoption of the split-array CAP-DAC alters the mismatch requirements. Monte Carlo simulations evaluating the mismatch characteristics of split-array CAP-DAC for a 10-bit ADC and 9-bit DAC configured with a

5/4 MSB/LSB ratio indicate an adjusted mismatch tolerance of 0.8%. The matching constants are derived from the Process Design Kit (PDK) to accommodate this mismatch specification, and the corresponding area of Metal-Oxide-Metal Fringing capacitor (MOM-capacitor) is computed.

8.4.3 Switches

For the CAP-DAC switches, the inverters will be isolated from the other circuitry to suppress digital noise. The reference voltage will be set to its maximum permissible value, minimizing the switch size necessary to achieve the desired DAC settling time. Due to the parasitic loading on the MSB side, substantial attenuation is inherent, reducing the effective full-scale range by 20%. Minimum-size inverters are employed for the DAC-elements up to 4-unit capacitors, while 8-unit capacitors are configured with two minimum-size inverters, and 16-unit capacitors utilize four minimum-size inverters.

8.4.4 DAC-logic

The required DAC logic for the system can be made using two NAND gates, as depicted in Fig. 8.6. As stated in Chapter 6, the DAC should wait for a valid decision from the capture latch. To accommodate this behavior, the NMOS/PMOS ratio has been skewed such that tripping voltage stays above V_{meta} of the comparator.

Different DAC elements use various switch sizes to ensure a constant delay from the capture latch to the DAC. The DAC-logic scales with the same ratio as the switches, with four DAC-logic cells in parallel for the 16-unit DAC.

8.5 Reference buffer

Two tune-able reference buffers are required for the calibration scheme used for the CAP-DAC split array. Due to the large free-chip area of the test-chip, a substantial decoupling capacitor is employed as the reference, optimizing power consumption at the expense of area utilization. For a 10-bit ADC, the decoupling capacitor must be 50 times the total capacitance of the CAP-DAC [17]. Furthermore, seperate references are maintained for both the LSB and MSB segments. This allows the decoupling capacitor on the MSB side to be charged to V_{ref} during LSB conversions and reciprocally, which mitigates the stringent demands on the decoupling capacitor.

Due to the ample free area, a decoupling capacitor 350 times the CAP-DAC value has been implemented.

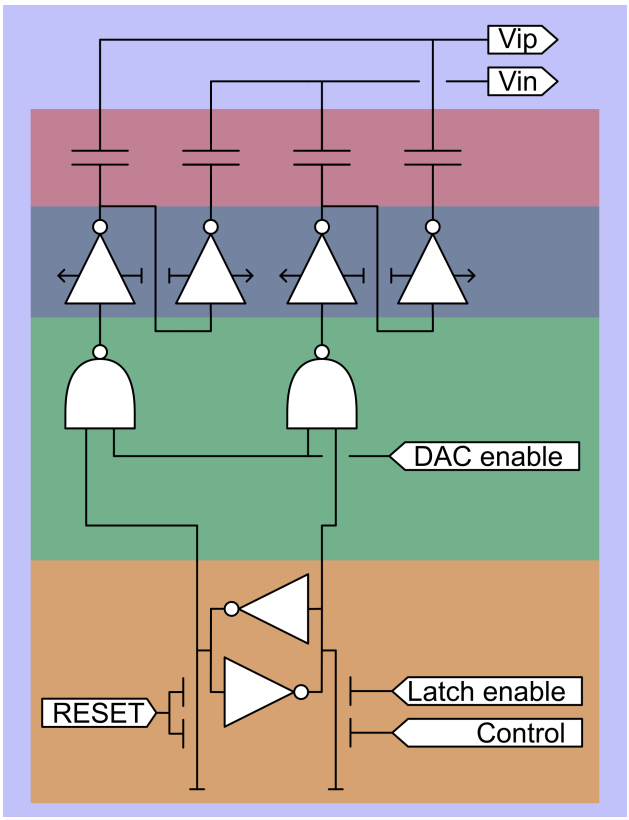


Figure 8.6: A single DAC unit with the required control signals.

8.6 Sampler

A bootstrapped switch is required to accommodate the full-scale voltage of 3 V_{pp} [18]. The configuration of the bootstrapped switch comprises five switches in conjunction with one NMOS device, as illustrated in Fig. 8.7. The operation can be divided into two phases: the charging and conducting. During the charging phase, the bootstrapped capacitor denoted as C_b, is charged to V_{dd}. In this phase, switches M1 and M4 are activated, effectively operating as short circuits.

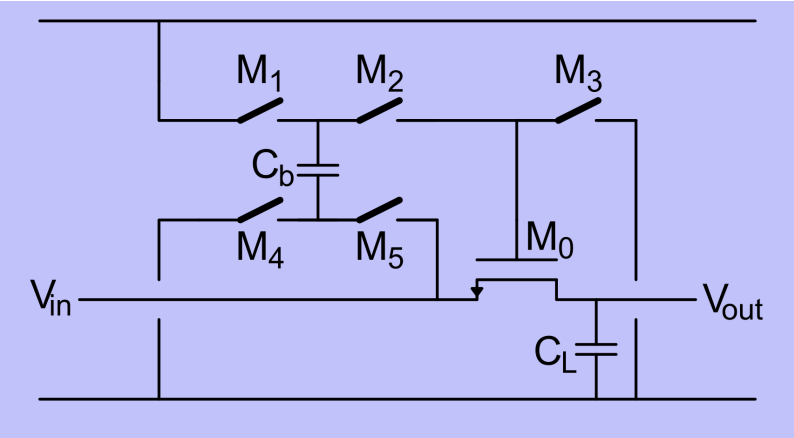


Figure 8.7: Bootstrapped switch.

The device enters the conducting phase when the input voltage must be sampled on the sampling capacitor. In this phase, switches M1 and M4 are deactivated, while M5, M2, and M3 are activated. The capacitor is positioned in parallel with the gate-source voltage of the NMOS transistor, resulting in a voltage of V_{dd} across the gate-source terminals of the NMOS. This constant voltage ensures that the on-resistance of the NMOS remains constant, thereby eliminating any dependency of on-resistance on the input voltage.

The implementation incorporates switches M1 and M2 that utilize PMOS devices, while switches M3, M4 and M5 employ NMOS devices. The gate voltage of device M0 will exceed the supply voltage; therefore, switches M2 and M3 are constructed using thick oxide devices, making them resilient to the substantial voltage fluctuations observed at the M0 gate.

8.7 Dual Single DAC Switch

A key component in validating dual DAC performance is the ability to switch between dual DAC and single DAC modes of operation. To enable this, an analog multiplexer is placed between the outputs of the inverters that drive the DAC elements and the capacitance associated with these DAC elements. In single DAC mode, it is required

that both DAC elements synchronize, thereby producing identical steps. This, in turn, prevents the possibility of complementary steps and eliminates the dead-zone within the system.

Upon activation of the single-DAC mode, one DAC-logic cell is bypassed, thereby producing a singular control signal and facilitating conventional operation through the mirroring of one DAC-logic cell by the other. Conversely, in the dual DAC mode, both DAC-logic cells are activated, resulting in two independent DAC-elements.

Chapter 9

Conclusion

The primary objective of this thesis is to improve BER of synchronous SAR ADCs. Through the use of an improved architecture, this was proven to be possible. We propose a modified SAR-loop utilizing a metastability detection circuit, creating so-called a dual-dac architecture for improved BER.

The overall SAR loop of the system was analysed, focusing on the interaction between the comparator and the capture latches. More information was found to be extracted from the comparator when using both output nodes of the comparator in combination with an amplifier. This combination allows for the detection of metastability within the comparator.

An improved SAR-loop was proposed, consisting of the metastability detection circuit in combination with two capture latches and two DAC elements per bit, termed the dual-DAC architecture. Using this dual-DAC architecture, we show that the time available to address metastable events increases without slowing down the system conversion speed, leading to a significant reduction in BER. This architecture accomplishes the solution of metastable events parallel to the SAR loop.

Comparing single and dual DAC architectures, shows that the BER was reduced several orders of magnitude. If the convential design achieves a $BER = BER_{single}$, the dual-dac system achieves a $BER_{dual} = BER_{single}^3$. This enhancement effectively doubles the maximum operating frequency for a given BER target, demonstrating the dual-DAC architecture's capacity to support higher data throughput.

Chapter 10

Future work

The subsequent phase of system validation includes the results of the experimental measurement of the fabricated test chip. The test chip, engineered during the course of this research, is intended to substantiate the simulation results obtained by the test bench, thus demonstrating silicon-level BER enhancements between dual and single DAC architectures.

10.1 Asynchronous SAR ADC comparison

The scope of the thesis was limited to evaluating the performance benefits of the dual-dac configuration in synchronous SAR ADCs. The asynchronous SAR architecture is often selected over the conventional synchronous architecture due to its enhanced BER performance compared to the synchronous counterpart. An analysis must be conducted on the asynchronous SAR ADC to determine when the dual DAC configuration becomes advantageous with respect to the BER. The asynchronous SAR ADC operates as a self-timed system, optimizing the use of time by minimizing the wasted time during conversion. Once the comparator presents a full digital logic response at the output, the system can continue directly by taking the corresponding DACs steps. In comparison to the synchronous SAR-ADC, when the comparator presents full digital logic at the output of the comparator, the system waits until the end of the comparison phase to continue the SAR-loop, thus wasting precious time, while the system does not provide anything to the SAR-loop.

Theoretically, only one cycle within the entire SAR conversion may exhibit metastability, this cycle requires more additional time to resolve the metastability. The easy decisions during the conversion process require less time for a valid response, thereby reducing inefficiencies and enabling operation at a higher sampling frequency while maintaining the same BER as its synchronous counterpart. The advantage of the asynchronous system is lost for ADCs consisting of a small number of bits.

A study is required to find the critical juncture between the dual-dac system and the asynchronous system. When comparing the asynchronous architecture and the dual-DAC architecture, a clear advantage presents itself within the DAC-settling of the system. For the asynchronous architecture, during the DAC-settling, the system does not accumulate further gain to reduce the BER, while the dual-DAC architecture does. In cases where DAC-settling of the system becomes the main limiting factor, the dual-DAC architecture will show a clear advantage over the asynchronous architecture.

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