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High-Speed Solid-State Circuit Breaker With Latching Current Limiter for DC Systems

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ABSTRACT The advancement of DC systems, especially in transportation applications, hinges on the development of effective protection mechanisms. Robust protection systems are crucial for enabling the widespread adoption of DC technologies in important transport modes, offering both operational and economic benefits. This paper introduces a high-speed solid-state circuit breaker designed for enhancing the protection of general DC systems. The upgraded breaker integrates the functionality of a latching current limiter, designed to minimize modifications to existing technologies. A custom gate driver and controller are developed and experimentally validated to support the circuit breaker. A scaled solid-state circuit breaker prototype is tested under various operational conditions to evaluate its performance. The breaker's behavior is simulated in SPICE to guide the experimental validation on a referential DC system. The results demonstrate high performance, with a clearing time close to 200 ns, effectively reducing system stress during short circuits. The current limiter functionality prevents unnecessary tripping during temporary overcurrents, keeping the current within safe parameters. The innovative gate driver simplifies the implementation of the latching current limiter, offering a practical and scalable solution. This work represents a significant step forward in DC protection technology, promoting the adoption of DC systems in transportation applications and beyond, by addressing critical protection challenges.

INDEX TERMS DC protection, DC systems, gate driver, latching current limiter, solid-state circuit breaker.

NOMENCLATURE

ΔT_{vj}	Virtual junction temperature rise.
$Z_{th(j-c)}$	Junction-case thermal impedance.
E_d	Dissipated energy.
I_D	Drain current.
i_{hall}	Hall-effect sensor current.
I_{max}	Maximum design short circuit current.
I_{nom}	Nominal design current.
I_{OFF}	Gate driver sink current.
I_{ON}	Gate driver source current.
i_{SC}	Short circuit current.
t_{LCL}	Latching current limiter time.
t_{max}	Maximum design clearance time.
V_{DS}	Drain-source voltage.
V_{GDF}	Forward voltage of gate driver diodes.
v_{GS}	Gate-source voltage.
$V_{L,max}$	Maximum inductance detection voltage.
V_{latch}	Latching current limiter reference voltage.
V_{max}	Maximum design voltage.
V_{nom}	Nominal design voltage.
$V_{overload}$	Overload reference voltage.
V_{th}	Threshold voltage.
C_d	Dampening capacitor.
C_{gs}	Gate-source parasitic capacitance.
ECSS	European Cooperation for Space Standardization.
ESR	Equivalent series resistor.

FET	Field-effect transistor.
HB_{CB}	Half-bridge circuit breaker.
HB_{LCL}	Half-bridge latching current limiter.
L_d	Dampening inductor.
LCL	Latching current limiter.
MOV	Metal-oxide varistor.
NL_{sw}	No-load switch.
Q_{gs}	Gate-source charge.
R_{DSON}	Equivalent channel on-resistance.
R_d	Dampening resistance.
$R_{G_{FET}}$	Gate resistance of a power switch.
R_{HiZ}	High impedance resistance.
R_{OFF}	Gate driver turn off resistance.
R_{OH}	Gate driver pull-up resistance in source mode.
R_{OL}	Gate driver pull-down resistance in sink mode.
R_{ON}	Gate driver turn on resistance.
SiC	Silicon carbide.

TABLE 1. Example of Commercially Available DC Circuit Breakers With Marine Certification, *Adapted From [20], With References to Prior studies [21], [22], [23]*

Type	Mechanical circuit breaker	SSCB	Solid-state bus-tie switch
Vendor	Schneider Electric	ABB	AstrolKWx
Reference	NW20HDC-C	SACE Infinitus	AA-10411-203
Rated voltage	1000 V	1000 V	1000 V
Breaking current	2000 A	2500 A	3000 A
Breaking time	30 ms	$\leq$ 25 µs	15 µs to 21 µs
Power losses	Not reported	1.3 kW@1 kA	6 kW@3 kA 0.67 kW@1 kA est.
Cooling solution	Air	Liquid	Liquid

I. INTRODUCTION

Transportation serves as the main backbone of modern society, requiring robust and efficient systems to support its critical role [1]. These systems are indispensable for global production lines, supply chains, and leisure industries [2]. However, the transportation industry faces a significant environmental challenge as its operations contribute to substantial carbon emissions [3], which exacerbate climate change and threaten sustainable living. Reducing the carbon footprint in transportation is imperative to minimize their environmental impact while preserving their vital role in the global economy [4], [5].

Ongoing efforts to decarbonize transportation focus on alternative fuels, improved efficiency, and broader electrification [5], [6], [7]. Examples include ammonia combustion, sustainable aviation fuel, and the use of fuel cells and batteries across various modes of transport. Electrification, particularly with DC systems, supports these goals by simplifying the integration of clean energy sources, improving efficiency, and significantly reducing emissions [8], [9], [10].

The widespread adoption of DC technologies in electric and more-electric transportation is based on the confidence of the stakeholders, which requires clear assurances of efficiency, reliability, and safety. Robust protection systems are critical to ensure the safety of involved personnel and the reliable operation of vehicles, ships and aircraft [11], [12], [13]. However, most existing protection systems rely on breaker-based designs, and current DC breaker technologies are not yet fully prepared to meet the demands of DC protection in multiple applications [14], [15]. Addressing these challenges is critical to unlocking the full potential of transport electrification.

Current circuit breaker technologies for DC systems face a trade-off as solid-state types are effective but inefficient, whereas their mechanical and hybrid counterparts are efficient but less effective [16], [17]. This concern is amplified by the severe risk posed by short circuits, which most existing DC circuit breakers struggle to contain effectively [18], [19]. For instance, certified DC circuit breakers capable of handling short circuits and robust fault clearance selectivity are both scarce and expensive [20].Table 1 summarizes the main parameters considered to assess commercially available DC circuit breakers, which is adapted from [20].

To unlock the potential of DC systems, it is essential to address the limitations of existing DC circuit breakers, focusing on improving their efficiency, effectiveness, and safety. Solid-state circuit breakers (SSCB), which employ semiconductors to achieve the breaking action, present a promising alternative, especially if their functionality is expanded beyond simply replacing AC circuit breakers. For example, a conventional SSCB can provide additional protection features such as Latching Current Limiter (LCL), designed to limit and hold current flow at safe levels during fault conditions, a technique already used in sensitive applications like aerospace [24], [25]. By preventing excessive current flow, the LCL enhances operational safety and protects downstream components [26].

LCLs mainly employ gate signal modulation to operate the power FET in its linear region, which ultimately limits the current by increasing the equivalent channel resistance R_{DSON} [24]. Available, certified-products, such as the AstrolKWx model in Table 1 and the Vacon NXP DC drive in [27], are primarily based on IGBTs, given the relatively high current ratings expected in heavy duty applications [16]. However, IGBTs are bipolar devices whose gate-turn-off characteristics are nonlinear, making them less effective when using the device's linear region to provide the LCL functionality [28]. Therefore, implementing the LCL into a conventional SSCB implies a paradigm shift towards FETs, where SiC MOSFETs or JFETs could become suitable replacements.

The key contribution of this work is a practical implementation of a LCL for DC systems that moves beyond conventional time-based selectivity [15]. This is achieved through a design based on the integration of two key elements: a custom three-level gate driver [29] and a high-speed analog controller. The three-level gate driver enables stable operation of SiC MOSFETs in their linear region, while the dedicated analog controller provides high-speed operation for breaking and current limiting. The resulting design offers a less complex

and more practical implementation compared to sophisticated LCL circuits (e.g., those used in space-rated applications), demonstrating a viable path to achieving current-based selectivity to prevent fault propagation and enhance the reliability of DC power systems.

A scaled-down prototype of a bidirectional SSCB with adapted LCL was tested. Experimental validation confirms that the device can effectively break the current during pole-to-pole short circuits while avoiding unnecessary interruptions during transient overloads. This work provides design guidelines for upgrading a conventional SSCB to include the LCL and demonstrates their potential as advanced protection devices for next-generation DC systems. The results strengthen the case for SSCBs not just as AC breaker replacements but as key enablers of more selective, compact, and reliable DC protection architectures.

The FET-based SSCB with the proposed custom gate driver and controller exhibits a breaking time approximately two orders of magnitude lower than the commercial models in Table 1. It performs breaking actions within 200 ns which can significantly decrease semiconductor stress by limiting the initial fault current, thus improving operational safety. This work serves as proof-of-concept for the upgraded SSCB, and future work should tailor the design to a specific application.

To showcase the contributions, the document is organized as follows: Section II describes the considered DC system, the reference SSCB, and the design of the dampening components. Section III presents the custom three-level gate driver designed to enable LCL functionality. Section IV details the control design that enables high speed breaking and effective current limiting, supported by simulation results for both protection modes. Section V shows a high-level summary of the SSCB design to facilitate visualization. The experimental validation of the designed SSCB showcasing its protection capabilities is presented in Section VI. Finally, Section VII summarizes the findings and draws the conclusions.

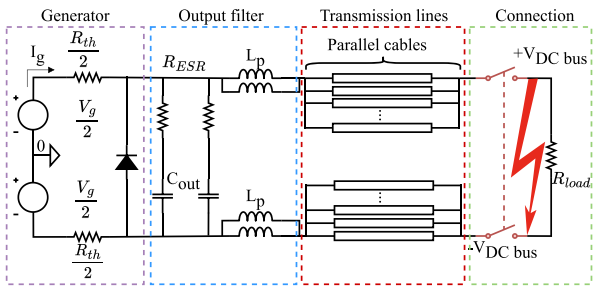


FIGURE 1. Simplified schematic of the DC system utilized in the study.

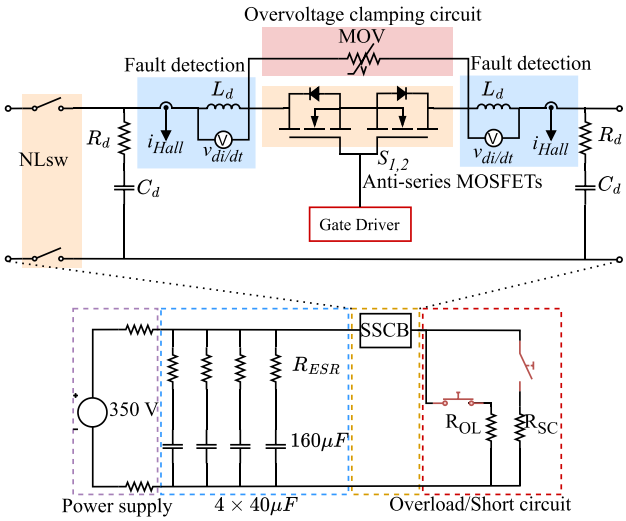


FIGURE 2. High-speed solid-state circuit breaker for DC systems. ***Upper side:*** Exploded view of the schematic with main components and zones. ***Lower side:*** Schematic of the tested DC system with floating ground with the SSCB.

II. SSCB CONSIDERATIONS

This section provides an overview of the simplified DC system circuit employed to test and design the SSCB with LCL. In addition, some basic design parameters and features of SSCB design, including fault-dampening components are discussed.

A. SINGLE-FEEDER SYSTEM

To simplify implementation and analysis, a generic, simple DC system is proposed. This single-feeder system, illustrated in Fig. 1, retains the essential elements of more sophisticated DC systems while reducing complexity. The circuit includes a power supply modeled as an equivalent DC source with an anti-parallel diode. The latter emulates the diodes of a generator or grid connection with a rectifier, or the output port of an isolated DC-DC converter. A large DC-link capacitor with low equivalent series resistance (ESR) serves as the output filter. Transmission lines, mimicking cabling or bus bars, connect the generator to a DC bus equivalent, which includes the load. For protection design, testing focuses on the bus connection point, where typical faults such as overloads and pole-to-pole short circuits are more likely to occur.

B. TOPOLOGY

Fig. 2 presents the schematic of the SSCB employed as baseline design, which is part of the single-feeder testing circuit for validation. This SSCB topology allows for bidirectional power flow and protection, while utilizing SiC MOSFETs facilitates power scalability [30]. This configuration is also convenient for unipolar DC systems, with floating or high impedance grounding, which can reduce the severity of pole-to-ground faults [12]. The SSCB should feature protection of the negative pole in applications that employ different grounding schemes and bipolar DC systems. Conceptually, these circuit breakers are not significantly different and can be sold separately when purchased off-the-shelf.

The development of DC protection requires a structured framework that covers aspects such as protection device design, transient current analysis during faults, and accurate modeling of SSCB components. Several guidelines, such as [17], [31], [32], [33], are available in the literature. These procedures guide the design of application-specific SSCBs

and include semiconductor selection, voltage clamping circuit or varistor, limiting inductance, component isolation, conventional gate driver and fault detection strategies.

When considering the upgraded design from Fig. 2, the key features of the SSCB are:

- *Decreased semiconductor stress:* High-speed detection prevents excessive current rising.
- *Time selectivity:* Current limiting keeps the current within safe values for relatively long periods.
- *Voltage oscillation attenuation:* The soft turn-off reduces possible voltage oscillations, avoiding sympathetic tripping.
- *No-load switch (NL_{SW}):* Provides circuit isolation.
- *RC damper (R_d C_d):* Enhances transient fault current behavior for better selectivity.
- *Dampening inductance (L_d):* Limits the current rate variation of a fault.
- *Fault detection $v\frac{di}{dt}$:* Monitors L_p voltage for fast short circuit detection.
- *Hall-effect current sensor (i_{HALL}):* Senses the current through the SSCB for the LCL functionality and serves as a secondary short circuit detector.
- *Power SiC semiconductor (SiC MOSFET)*: Manage bidirectional current flow, blocking and current limiting.
- *Metal-oxide varistor (MOV):* Provides overvoltage clamping across the semiconductors as a last resort.
- *Gate driver:* Customized to integrate LCL and high-speed breaking functionalities.

These elements collectively ensure robust and efficient operation of the SSCB, particularly under fault conditions requiring high-speed response.

The test circuit shown in Fig. 2 represents the single-feeder model of the primary DC system, including the power supply, capacitor bank, and fault branches. This configuration serves as a bridge between simulation and practical implementation.

Once the SSCB topology is known, the design of additional protection functionalities begins with an analysis of the fault conditions that require interruption and their associated behavior. Practical simplifications and assumptions guide the selection of passive components and power semiconductors in general. A detailed examination of DC short circuit currents, based on standards such as IEC 61660-1 for DC auxiliary systems [34] and IEC 62305-1 for lightning protection [35], leads to the development of fault response models. These models, described by (1) to (2), account for overdamped and underdamped current responses, respectively, forming the basis for the design and operation of the SSCB.

$$i_{SC}(t)=\frac{e^{-\alpha t}}{2\beta}\left[\frac{V_{nom}}{2L_p}\left(e^{\beta t}-e^{-\beta t}\right)+\beta I_g(0)\left(e^{\beta t}+e^{-\beta t}\right)\right] \tag{1}$$

$$i_{SC}(t)=e^{-\alpha t}\left[\frac{V_{nom}}{\omega_d L_p}\sin\omega_d t+I_g(0)\cos\omega_d t\right] \tag{2}$$

where $I_g(0)$ is the initial condition of the generator current, V_g is the generator voltage, which coincided with the rated SSCB voltage V_{nom}, L_p is the parasitic inductance of the output filter, and α, β and ω_d are (3) to (5) respectively.

$$\alpha=\frac{R_{ESR}}{4L_p} \tag{3}$$

$$\beta=\sqrt{\left(\frac{R_{ESR}}{4L_p}\right)^2-\frac{1}{L_pC_{out}}} \tag{4}$$

$$\omega_d=\sqrt{\frac{1}{L_pC_{out}}-\left(\frac{R_{ESR}}{4L_p}\right)^2} \tag{5}$$

C. RCL DAMPER DESIGN

The protection design focuses on reshaping the current waveform, particularly its rising characteristics. The RCL damper, shown in Fig. 2 as R_d, C_d and L_d acts as the first protection layer. During a fault, the initial pulse resembles a right triangle and can be approximated using a sawtooth model. This simplification allows the inductor to be designed based on (6), as described in [36].

$$2L_d=\frac{\sqrt{3}V_{nom}t_{max}}{I_{max}(t_{max})} \tag{6}$$

Equation (6) is valid when L_p, the inductance of the bus bar and the inductance of the transmission line are negligible. Otherwise, the equivalent inductance should be added, resulting in a lower L_d. The maximum current $I_{max}(t_{max})$ is a design objective, and should align with the maximum pulsed current rating of the semiconductor.

Given that L_d is commonly used in SSCB design as $\frac{di}{dt}$ limiter, care must be taken during its selection. L_d should guarantee that the normal dynamic performance of the system is not compromised and that the maximum design voltage of the SSCB (V_{max}) is respected as (7).

$$2L_{d,max}\leq\frac{v_{max}t_{max}}{I_{max}(t_{max})} \tag{7}$$

A well-designed detection circuit and signal conditioning can help to reduce the peak current, minimizing semiconductor stress and decreasing power dissipation. This approach enhances the overall lifetime of the device. The RC damper calculation complements the inductor selection and is derived from (8) and (9), based on the guidelines presented in [17], [36].

$$C_d >> \frac{t_{max}^2}{4\pi^2 2L_d} \tag{8}$$

$$2\sqrt{\frac{2L_d}{C_d}} < R_d < \frac{V_{L,max}}{I_{nom}} \tag{9}$$

where C_d and R_d are the dampening capacitor and resistance, respectively, I_{nom} is the nominal design current, $V_{L,max}$ is the maximum acceptable voltage across L_d for short circuit detection, approximated as (10).

$$V_{L,max}\approx\frac{2I_{nom}2L_d}{t_{max}} \tag{10}$$

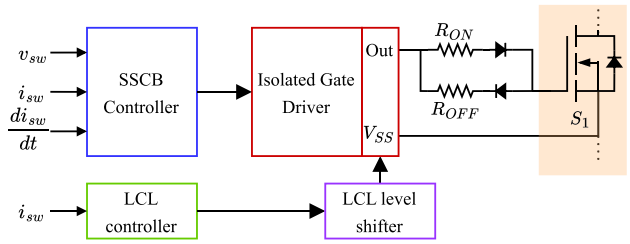


FIGURE 3. Functional blocks architecture of the integrated gate driver implemented for breaking and current limiting in the SSCB. *Adapted from* [42].

During SSCB commissioning, $V_{\mathrm{L,max}}$ must be recalibrated to ensure proper operation under the specific system conditions.

III. THREE-LEVEL GATE DRIVER DESIGN

After designing the SSCB parameters, focus shifts to the integrated three-level gate driver and its operation. Incorporating the LCL in the SSCB is particularly worthwhile in isolating faulted circuits while maintaining the functionality of the remaining system. This is valuable in satellites, where isolating a failed subsystem ensures the undisturbed operation of other payloads [37], [38]. A quick response to a fault reduces energy losses due to prolonged overcurrent or thermal damage, improving overall system efficiency and reliability [26], [37].

The work in [38] shows a LCL with a complex structure, segregating the controller, telemetries, and logic as building blocks in a photolithography-based construction. Moreover, the limited response time (milliseconds) and the overall burden of producing custom chips make this approach unfeasible. Although [24] shows a simpler design, the complications related to the analog design and the magnetic isolation remain substantial, while the response time falls within hundreds of microseconds. The design in [37] uses a conventional LCL with limited details about the control and internal electronics. The application is for a low voltage subsystem, in which the time response is close to 2 ms. Off-the-shelf, space-rated devices, like those described in [24], [39], require advanced control and measurement circuits that are not typically required for less demanding applications.

This research exploits existing gate drivers to achieve a simple and robust SSCB with integrated LCL. Research highlights the critical role of precise gate driver tuning in achieving safe and effective breaking action [40], [41], [42]. This is considered for the conceptual architecture of the integrated three-level gate driver, shown in Fig. 3, utilized for this work.

The SSCB controller integrates closely with the gate driver logic, monitoring the drain-source voltage of the power switch (v_{DS}), the drain current (i_{D}), and its rate of change $\frac{\mathrm{d}i_{\mathrm{D}}}{\mathrm{d}t}$. Short circuit protection is primarily governed by $\frac{\mathrm{d}i}{\mathrm{d}t}$ sensing, while average current serves as a supplementary parameter. The gate driver design can incorporate a commercially available component with an *enable* pin, paired with an isolation stage and a soft turn-off network. The proposed gate driver

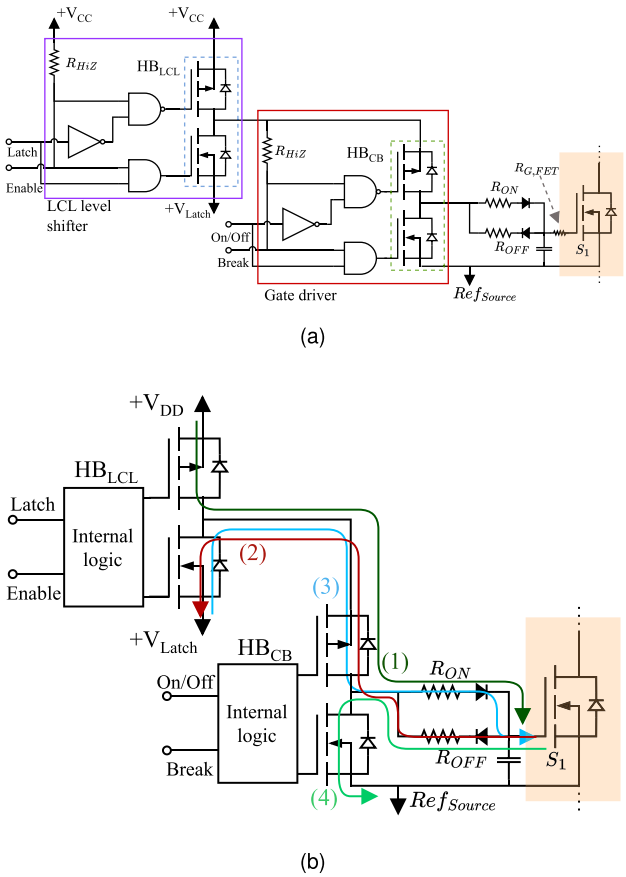


FIGURE 4. Proposed three-level gate driver topology with soft turn-off network for a SSCB with integrated LCL. (a) Implementation of the gate driver including internal logic circuitry. (b) Simplified schematic with current flow indications. *Path (1) is active when the SSCB is on, path (2) applies when the LCL starts, path (3) is used when holding the LCL gate voltage, and path (4) when the SSCB is breaking or turned off.*

topology, denoted as a three-level, employs two identical off-the-shelf gate drivers in cascaded disposition as depicted in Fig. 4(a).

The LCL half-bridge ($\mathrm{HB_{LCL}}$) acts as the power supply for the circuit breaker half-bridge ($\mathrm{HB_{CB}}$) that ultimately drives the power switch S_1. $\mathrm{HB_{LCL}}$ is the LCL level shifter, fed by $+V_{\mathrm{DD}}$ on the positive port, supplying normal gate voltage to S_1. The low-side voltage in $\mathrm{HB_{LCL}}$ defines the LCL voltage $+V\mathrm{LCL}$. The current paths in the gate driver for the different operation modes are illustrated in Fig. 4(b), where *path (1)* is active during normal turn-on and when the LCL turns-off, and *path (4)* for normal turn-off and breaking. *Paths (2)* and *(3)* are necessary for the LCL functionality. *Path (2)* becomes active when the LCL command signal is set on, then v_{GS} decreases from $+V_{\mathrm{DD}}$ to $+V_{\mathrm{LCL}}$, partially discharging the parasitic capacitor in the switch. Complementarily, *path (3)* allows the $+V_{\mathrm{LCL}}$ voltage to be maintained until the LCL signal is off. The *enable (and break)* pin adds an additional safety layer by forcing the gate driver into a high impedance, when the logic signal is off. Details about the controller are explained later in this section.

The proposed configuration facilitates precise tuning of the SSCB's dynamic behavior during turn-on and off, and current

limiting. Gate resistors R_{ON} and R_{OFF} are used to adjust the dynamic response of the gate driver. The sink-source capability of the gate driver depends on the gate loop resistance, determined by its output stage, diodes, and gate resistors, as formulated in (11) to (13). This setup ensures the SSCB operates reliably under varying conditions.

$$I_{ON} = \frac{V_{DD} - V_{GDF}}{\chi R_{OH} + R_{ON} + R_{G_{FET}}} \tag{11}$$

$$I_{OFF} = \frac{V_{DD} - V_{GDF}}{R_{OL} + R_{OFF} + R_{G_{FET}}} \tag{12}$$

$$I_{LCL} = \frac{V_{DD} - V_{GDF}}{R_{OH} + R_{OL} + R_{OFF} + R_{G_{FET}}} \tag{13}$$

where V_{GDF} represents the forward voltage of the gate diodes, R_{OH} is the pull-up resistance in source mode, R_{OL} is the pull-down resistance in sink mode, $R_{G_{FET}}$ denotes the gate resistance of the power switch, and χ is equal to 1 when the SSCB operates normally, and equal to 2 when the LCL is active. Both R_{OH} and R_{OL} are part of the gate driver, and are embedded in the transistors in HB_{LCL} and HB_{CB} for the high and low levels respectively.

The LCL controller in Fig. 3 modulates the gate signal during LCL operation. It monitors i_D and dynamically adjusts the gate signal voltage by controlling the auxiliary power supply. Since the power supply is a commercial component, a voltage adjustment circuit, referred to as the *LCL level shifter*, is incorporated into the design. Ultimately, this architecture is realized with the three-level gate driver, and the level shifter corresponds to HB_{LCL}. This circuit, directed by the LCL controller, drives the power MOSFET (S_1) into its linear region, increasing the equivalent device impedance R_{DSON} and introducing controlled power losses to effectively limit the current flow for a short period. Since the gate turn-on and off characteristics of IGBTs present nonlinearities [28], carefully operating in the linear region becomes challenging, which makes them less suitable for this research. Consequently, SiC MOSFETs are preferred for the SSCB design.

IV. PROTECTION CONTROL DESIGN

Integrating a SSCB with an LCL requires the design of a suitable controller for the gate driver. This section presents the controller that governs the breaking and the current limiting functionalities in the three-level gate driver. The simulation of both protection cases is also discussed in this section.

The primary function of the control circuit is to precisely manage the parasitic gate-source capacitance of the power MOSFETs. According to (14), the adjustable parameter is V_{GS}, which the gate driver modulates by charging and discharging this capacitance to achieve the desired control. This careful management of V_{GS} ensures accurate and reliable operation of the integrated protection system.

$$C_{gs} = \frac{Q_{gs}}{V_{GS}} \tag{14}$$

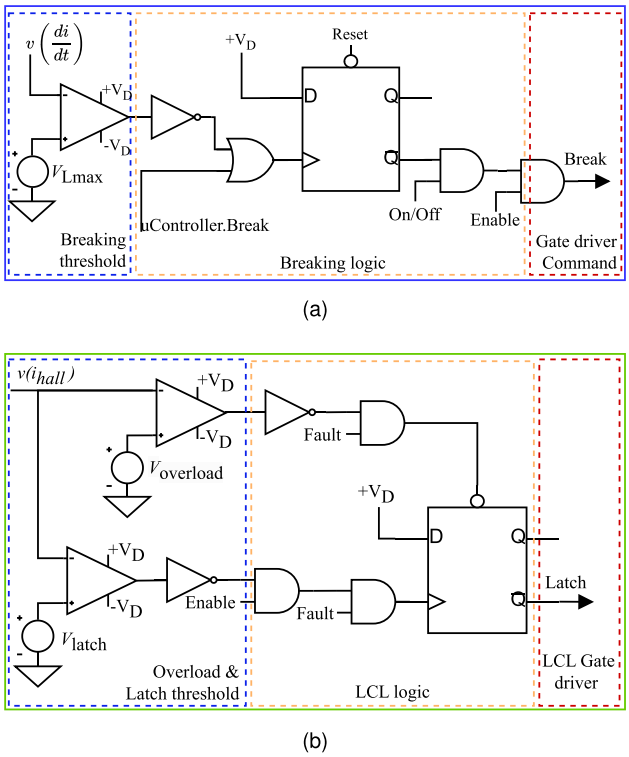


FIGURE 5. Schematic of analogue control circuits. (a) Breaking latched $\frac{di}{dt}$ control circuit. (b) Latching current limiter control circuit. *Note that "Latch" and "Break" signals are normally ON.*

The gate driver must support two distinct control modes: high-speed breaking for short circuit protection and current limiting for LCL operation. Both control modes require inverted logic signals, meaning that the on-state (logic high) indicates that breaking and/or LCL functionalities are off.

A. HIGH-SPEED BREAKING

The breaking logic sequence, illustrated in Fig. 5(a), monitors the voltage across L_d and compares it to a reference value $V_{L,max}$. This reference is established during the design phase based on load characteristics, ensuring the SSCB trips under appropriate fault conditions. As this functionality is time-sensitive, it requires critical components such as high-bandwidth comparators and logic gates to have minimal propagation delays (in the order of tens of nanoseconds).

The high-speed breaking controller's operation was tested in simulation, with the main results presented in Fig. 6. In Fig. 6(a) the gate driver voltage transitions from 10 V to 0 V. The fault current, depicted in Fig. 6(b), reaches approximately 92 A with a rise time of about 250 ns and a clearance time near 950 ns. These results suggests low stress on the semiconductor, with the surge current remaining well within its maximum current pulse rating.

Fig. 6(c) shows the voltage across the SSCB. Initially a high-speed surge is observed, stabilizing momentarily, as the driven signal reacts. The gate driver's effect becomes evident when the voltage across the SSCB increases as expected. The simulation results indicate reduced reliance on the MOV

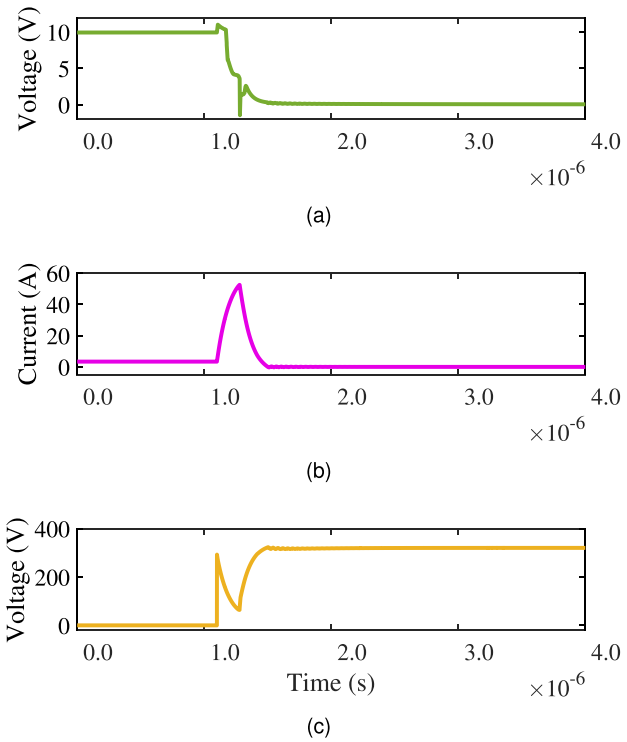


FIGURE 6. Simulation of the SSCB to validate the performance of the high-speed short circuit controller. (a) Gate-source voltage of the power switch. (b) Current through the SSCB. (c) Voltage across the SSCB.

for voltage clamping, which may enhance system reliability. However, detailed studies on MOV and its long-term performance longevity are beyond the scope of this research. These findings demonstrate the controller's effective performance and its potential for real-world application.

B. CURRENT LIMITING

The primary design consideration for the LCL is its response time, as it must suppress current surges rapidly without disrupting system dynamics. In marine applications, components adhere to standards such as IEC 62040-3:2021, which specify an overload factor of 1.2 for a duration of 100 s [43]. Furthermore, the LCL controller adopts a hiccup modulation strategy, a well-established method for protecting power converters during overload conditions by temporarily inhibiting PWM signals [44].

To achieve proper operation, the LCL design incorporates two set-point comparators with similar propagation delay, as shown in Fig. 5(b). Timing of the LCL controller is key for efficient current limiting. High-speed components are necessary to obtain a fast LCL that avoids transient overcurrents, excessive losses and load disturbances. The overload state (V_{overload}) is detected using a high-speed comparator and a high-bandwidth hall-effect current sensor, with the current measurement signal $i(t)$ conditioned as $i(t) = \text{SF}v_{(i_{\text{hall}})}$, where SF represents the scale factor for signal conditioning. The overcurrent state (V_{LCL}) triggers the LCL mechanism, providing the falling edge for the D-latch. The LCL resets when the current returns within nominal limits, as described by (15a) to (15c). Specifically, the LCL is triggered when $i(t)$ surpasses $1.2I_{\text{nom}}$. Once the current decreases below the nominal region, the LCL resets, ensuring seamless operation and effective suppression of transient overcurrents.

$$i(t)\begin{cases}\text{Nominal}, & i(t) < I_{\text{nom}} & \text{(15a)}\\ \text{Overload}, & 1.2I_{\text{nom}} > i(t) > I_{\text{nom}} & \text{(15b)}\\ \text{LCL}, & i(t) \geq 1.2I_{\text{nom}} & \text{(15c)}\end{cases}$$

The gate driver requires an adjustable power supply that becomes active during limiting phase of the LCL operation. During this phase, the source primarily acts as a sink for the gate charge (Q_{gs}) by pulling down v_{GS} to a predefined value V_{LCL}, as described in (16).

$$+V_{\text{CC}} > +V_{\text{LCL}} > V_{\text{th}} \tag{16}$$

This adjustment reduces v_{GS} from its normal $+V_{\text{CC}}$ to a level above the threshold voltage (V_{th}), enabling current limitation. Since this type of modulation counteracts the excess current in the protected system with heat dissipation in the SSCB, limiting the LCL time in accordance with the semiconductor parameters is essential. The practical implementation of the LCL requires the analysis of the dissipated energy (E_{d}) in (17), which gives the virtual junction temperature rise (ΔT_{vj}) in (18).

$$E_{\text{d}} = V_{\text{DS}} I_{\text{D}} t_{\text{LCL}} \tag{17}$$

$$\Delta T_{\text{vj}} = E_{\text{d}} \text{Z}_{\text{th(j-c)}} \tag{18}$$

where t_{LCL} is on-time of the LCL, measured from the drop until the recovery of v_{GS}, and $\text{Z}_{\text{th(j-c)}}$ is the junction-case thermal impedance of the semiconductor. The LCL controller must guarantee that T_{vj} does not exceed 80% of the reported maximum, as advised by manufacturers. However, a more conservative value should be used whenever possible. A practical estimation is possible by assuming that the current waveform due to the LCL is triangular, and that the temperature rise is equal during every LCL cycle (constant duration). The number of LCL cycles for a given ΔT_{vj} is calculated using (19).

$$\text{Cycles}_{\text{LCL}} = \frac{2\Delta T_{\text{vj}}}{I_{\text{D}} V_{\text{DS}} t_{\text{LCL}} \text{Z}_{\text{th(j-c)}}} \tag{19}$$

Since the duration of each cycle is known, the number of cycles gives a rough estimation of t_{LCL} as an absolute maximum when using nominal parameters. A safety margin of at least 10% is recommended. Calculating the total t_{LCL} is relatively straightforward by using the microcontroller break signal in Fig. 5(a). The controller can implement (20) to determine t_{LCL} and compare it with the maximum LCL time $t_{LCL,max}$.

$$t_{\text{LCL,max}} \leq \int t_{\text{LCL}}(t)\,\text{d}t \tag{20}$$

where $t_{\text{LCL}}(t)$ is a boolean signal according to (21b) and (21a).

$$t_{\text{LCL}}(t)\begin{cases}0, & \text{LCL off} & \text{(21a)}\\ 1, & \text{LCL on} & \text{(21b)}\end{cases}$$

The LCL control circuit was simulated with the SSCB, and the key results are presented in Fig. 7.

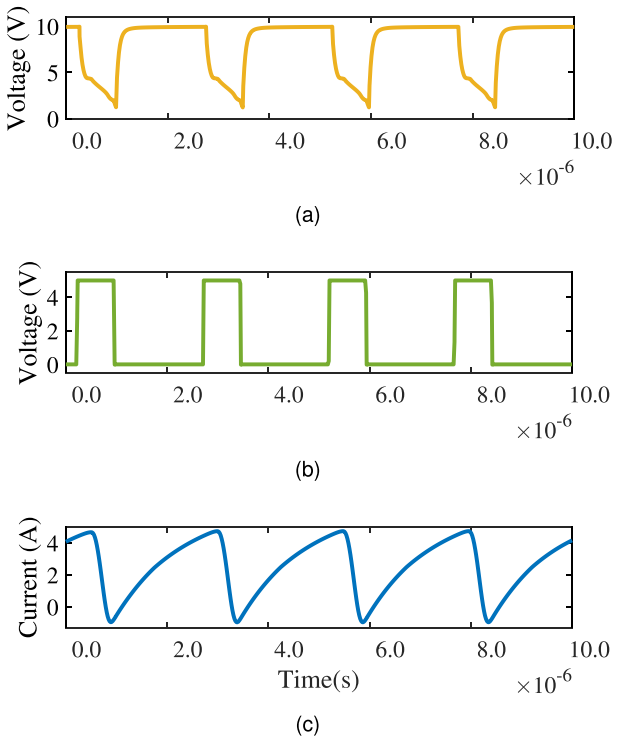


FIGURE 7. Simulation of the SSCB in overcurrent to validate the operation of the LCL. (a) Gate-source voltage of the power switch. (b) LCL logical command. (c) Current through the SSCB.

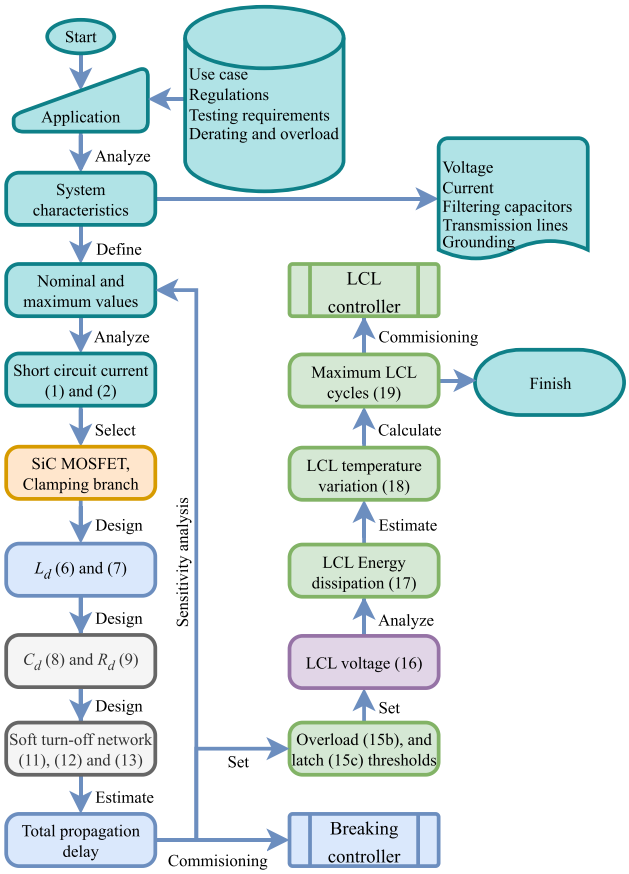


FIGURE 8. Simplified design process of a generic SSCB with LCL. *Numbers in blocks:* Reference to equations in the document.

The simulation uses a reduced source voltage of 50 V and an overcurrent setpoint of 3.3 A to align with experimental results (Section VI). During LCL, v_{GS} drops to V_{LCL}, reducing Q_{gs}, approximately following (12). Once the current returns to nominal levels, the LCL deactivates, and v_{GS} returns to its normal operating value of 10 V.

The gate driver behavior during current limiting is depicted in Fig. 7(a), with corresponding command signals in Fig. 7(b). These signals synchronize with the gate voltage v_{GS} and the SSCB current, which oscillates as the LCL activates and deactivates (Fig. 7(c)).

The current rises approximately 3.5 A, exceeding the LCL threshold, at which point the LCL forces it back, recovering once it returns to the nominal levels.

In scenarios where the overcurrent persists, the LCL triggers the SSCB to trip, preventing semiconductor overheating. Notably, current zero-crossings are observed in Fig. 7(c), caused by circuit inductance and the reduced DC voltage of 50 V during the simulation. This phenomenon, also observed in the experimental setup, can be mitigated by operating at the nominal SSCB design voltage of 350 V, which would reduce output voltage drops and improve LCL performance. Further validation of these findings, including tests at nominal voltage, is beyond the scope of this research.

V. DESIGN SUMMARY

Designing DC protection is an ever-evolving process that does not have a generalized procedure. The standard design of SSCB tends to follow diverse sets of requirements, since a converging regulation is missing and unlikely to materialize. Furthermore, LCLs are used mainly in aerospace, and there is no broadly established framework for standardizing their design across other industries. Design guidelines from aerospace regulators, such as the European Cooperation for Space Standardization (ECSS) [25], offer valuable insights. This section summarizes the design of the upgrades proposed for the SSCB with LCL. The design assumes a generic SSCB following specific regulations and objectives, used as a platform for the implementation of the enhancement functionalities.

Fig. 8 exhibit the simplified procedure, extracted from Sections II to IV, utilized as the design structure for this investigation. These guidelines can be adapted to suit several DC applications, enabling the transfer of key principles while addressing their unique challenges. The process begins with understanding the application, assumed as received information about the use case, regulations, testing requirements, and overload and derating factors. System parameters such as voltage, current, connected passive components, and grounding schemes must be clarified during the analysis, resulting in the definition of nominal and maximum values. In addition, short circuit current studies can be performed to guide the overall design and provide a reference of the effect of the designed SSCB.

TABLE 2. SSCB Design Parameters From the Proposed Design Guidelines

Parameter	Value
Overload factor	1.2
Dampening inductance L_d	0.47 µH
Dampening capacitor C_d	300 nF
Dampening resistance R_d	4.3 Ω
On resistance R_{ON}	4.64 Ω
Off resistance R_{OFF}	9.28 Ω
Breaking delay*	38 ns
Clearing time*	≈200 ns
LCL threshold	3.2 A
LCL maximum temperature rise	25 K
Energy per LCL cycle E_d	6.6 µJ
Temperature rise per LCL cycle	2.18×10^{-6} °C
Maximum LCL cycles	22957000
Maximum LCL time $t_{LCL,max}$	22.7 s
Maximum LCL time @350 V, 10 A	7.57 s
Actual LCL time	20 µs
LCL delay*	250 ns

* Measured value

TABLE 3. System and Circuit Breaker Parameters

Parameter	Value	Subsystem
Nominal voltage V_{nom}	350 V	Generator
Filter capacitance C_{out}	160 µF	Output filter
Capacitor ESR	1.325 mΩ	Output filter
Parasitic inductance* L_p	250 nH	Output filter
Nominal current I_{nom}	10 A	Generator, SSCB
On-resistance (FET) R_{DSON}	≈ 39 mΩ	SSCB
Drain-source reverse voltage	≈ 3.8 V	SSCB
Peak source current	9 A	Gate driver
Peak sink current	9 A	Gate driver
Line inductance	8.32 µH	Load
Load resistance	8.9 Ω	Load

* Estimated value

The selection of the power switch mainly takes into consideration parameters such as voltage class, nominal current, maximum drain current, short circuit withstand time, on-state resistance, power dissipation, gate voltage threshold, turn-off delay, gate charge, thermal impedance, virtual junction temperature, and the safe operating region. It is handy to employ switch selection guidelines as in [17], [45], focusing on the tripping characteristics of the circuit breaker and how it matches the safe operation region of the switch. Additional parameters used during standard power electronics design should also be considered.

The voltage-clamping branch is essential in a generic SSCB design. Opting for a MOV or an RCD snubber is an application-specific choice. The guidelines in [46] discuss the selection requirements for the MOV. [31] illustrate the trade-offs of using the RCD snubber in a bidirectional SSCB. The final choice and selection depends on the application and the expected short circuit characteristics. Ultimately, the designer should consider reliability constrains, since the voltage clamping branch can be exposed to significant stress.

The remainder of the procedure follows an iterative design, based on previously discussed parameters, in the form of a sensitivity analysis to achieve adequate performance. Some reference values should be commissioned, calibrated, or set during the process flow given that the controller governs the operation of the power stage. The outcome of the design process for this research is summarized in Table 2.

VI. EXPERIMENTAL VALIDATION

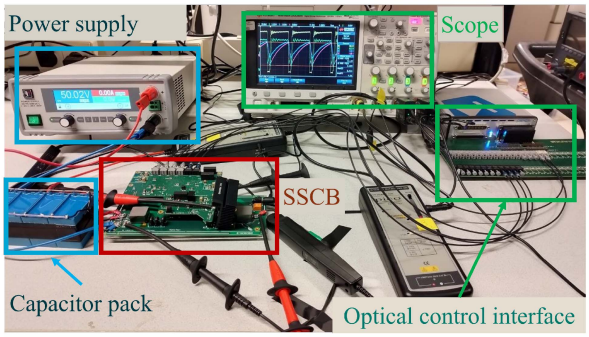
After completing simulations and determining hardware recommendations, an experimental setup was established to validate the results. This setup replicates the generic DC system, including power supplies, capacitor banks, loads, protection devices, and a short circuit forcing branch (Fig. 2). Both transient and steady-state responses were analyzed to refine the simulation model and validate key functionalities. The high-speed breaking and LCL functionalities were tested using an SSCB prototype with an integrated gate driver. The results were compared against commercial-off-the-shelf solutions to highlight improvements. Such a comparison is valid to some extent, given that the employed power SiC MOSFETs are expected to behave similarly with higher current ratings. In contrast, some DC systems on ships or heavy duty vehicles may require parallelization of power semiconductors to reach the required ratings, and further testings is necessary. However, it is noteworthy that certified LCLs outside spacecraft applications are scarce or unavailable, highlighting the added value of this work.

The key parameters of the test circuit are summarized in Table 3. Fig. 9(a) shows the implemented SSCB, which is primarily commanded via optical fiber to enhance safety and communication speed. High-speed breaking and LCL controllers were developed using discrete components, leveraging their superior timing characteristics compared to digital controllers. The experimental setup, illustrated in Fig. 9(b), includes a power supply, a low-impedance film capacitor pack for short circuit testing, and an SSCB connected to an overload branch (*not visible in the figure*). The main components and instruments used are listed in Table 4.

Care must be taken when selecting the commercial gate driver, since a high impedance output option, and a relatively low undervoltage lockout are necessary. The former prevents the MOSFET from false-gating when the SSCB has tripped, and the latter allows for a broad range of V_{LCL} without shutting down the gate driver during LCL. Although it was not necessary for this research, implementing a negative bias turn-off for the power switch can enhance false-gating immunity. This becomes unavoidable when relatively high-magnitude electromagnetic interference is present.

Due to practical limitations and simplification efforts during testing, the external power supply generated a gate voltage

(a)



(b)

FIGURE 9. Implementation of the single-feeder setup and the SSCB for testing. (a) Experimental high-speed SSCB concept design. (b) Testing setup with main components.

TABLE 4. Main Components Employed to Implement the SSCB

Component	Reference
Gate driver	
Commercial gate Driver	IXYS IXDD609SI
Schottky diode	Nexperia PMEG2010EPK
Power stage	
SiC MOSFET	Infineon IMW120R040M1H
MOV	Panasonic ERZV10D431
Capacitor	EPCOS B32776G4406K000
Sensors and control	
Hall-effect sensor	Allegro ACS37032LLZATR
High-speed rail-to-rail comparator	TI TLV3601
High-speed OR gate	TI SN74LVC1G32-EP
High-speed AND gate	TI SN74LVC1G11-Q1
High-speed Inverter gate	TI SN74LVC3GU04
High-speed D-Latch	TI SN74AHCT74DR
Measurement	
Current probe	Micsig CP1003B
Differential probe	Micsig DP700
Differential probe for LCL	Pico TA043
Scope	Keysight DSOX3024A

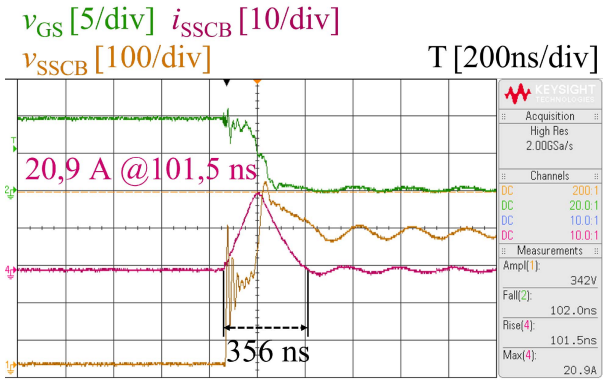


FIGURE 10. Scope snapshot of short circuit test for the proposed high-speed SSCB. *Green-top:* v_{GS}, *magenta: middle:* i_{SSCB}, *yellow-bottom:* v_{SSCB}.

lower than the device manufacturer's recommended value. However, a significant performance variation for both short circuit and LCL is not expected and the results are conclusive.

A. BREAKING MODE

The high-speed breaking functionality was validated using the circuit in Fig. 2. Two scenarios were tested: the performance case, with the high-speed controller, and the reference case, where the propagation delay of the controller is comparable to commercially off-the-shelf SSCBs. The breaking mode performance experiment was conducted by directly shorting the output port of the SSCB with the negative port of the capacitor pack. The result, shown in Fig. 10, presents v_{GS}, at the top, reacting to the short circuit after approximately 98 ns of propagation delay from the fault instant. The detection delay allows the breaker current I_{SSCB} to increase (*from zero*), reaching a peak value of about 20.9 A with a rise-time of approximately 102 ns. The total fault time is close to 356 ns, which is approximately 254 ns after the breaking time.

The experimental results in Fig. 10 surpassed the simulation predictions, showing similar response times but with peak current magnitudes reduced to approximately 60% of the simulated values. These discrepancies arise from testing circuit characteristics, where the inductance was estimated and reduced. Furthermore, Fig. 11 highlights the benefit of the proposed SSCB; its low propagation delay allows the breaker to interrupt the fault before the current rises excessively, thereby reducing stress on the semiconductor devices. For comparison, commercial SSCB products from AstrolKWx [22] and ABB [21], [47] exhibit significantly longer propagation delays. This is illustrated by a failed current blocking experiment, in which a delay of about 3 μs, comparable to those commercial products, caused destructive overcurrent in the semiconductor. In contrast, the proposed high-speed SSCB, with its narrow operation window and fast control action, achieves timely interruption without the need for large device oversizing.

In contrast, the failed experiment shows large fluctuations with delayed breaking action from electronics. The MOSFET

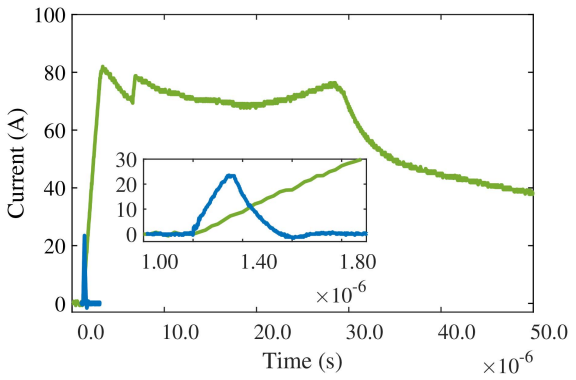


FIGURE 11. Short circuit current through the SSCB comparison for two cases of propagation delay. *Green-top:* 3 μs delay, *Blue-bottom:* 80 ns. *Inset:* Detail of the low propagation delay test, achieved with the designed gate driver.

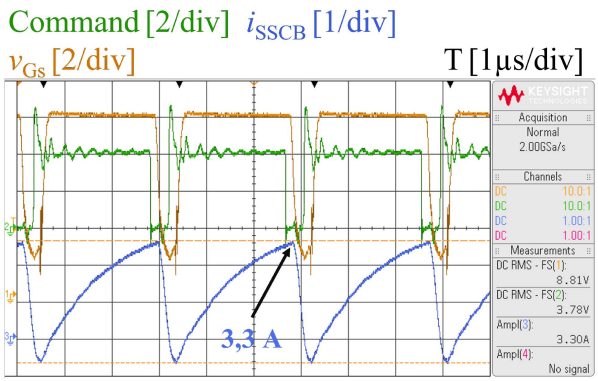


FIGURE 12. Scope snapshot of the SSCB operating as LCL with the proposed gate driver. *Yellow-top:* v_{GS}, *green-middle:* LCL command signal, *blue-bottom:* i_{SSCB}.

is likely overheating when the command occurs since it takes only a few microseconds to destroy it.

B. HICCUP MODE

To validate the LCL functionality, the circuit shown in Fig. 2 was used, with the corresponding experimental setup depicted in Fig. 9(b). The DC voltage was set to 50 V, and the LCL threshold was established at 3.3 A, consistent with the simulation parameters. From (19), the maximum LCL time for the conditions of the experiment is around 1.3 s, estimated for a junction temperature rise of 25 K. In nominal design conditions (350 V, 10 A), it would decrease to around 150 ms for the same junction temperature rise.

The experimental results, presented in Fig. 12, demonstrate the v_{GS} response of the gate driver to command signals, with a measured propagation delay of approximately 150 ns. This alignment between experimental and simulation parameters confirms the successful validation of the LCL functionality.

When the LCL threshold is reached, the SSCB reduces v_{GS} to V_{LCL}, increasing R_{DSON} and forcing the current to decrease. Once the current returns to nominal levels, the latch is released, restoring v_{GS} to its normal value. The command delay causes the current to drop further than necessary, creating oscillations in i_{SSCB} due to circuit inductance.

The results validate the LCL functionality with minimal modifications to a conventional SSCB. Despite the reduced test voltage of 50 V, the current remained within safe limits and no false tripping occurred. This was verified with the v_{GS} measurement and the command signal, as they do not drop to zero at any point. The employed independent detection mechanisms ensured that $\frac{di}{dt}$ fluctuations did not exceed the breaking threshold, while the hall-effect sensor effectively managed the LCL control. This demonstrates that the LCL design proposed in this work achieves adequate current limitation without compromising system integrity, and expanding selectivity.

C. FUTURE WORK

The technology developed in this work is versatile and applicable beyond transportion due to its relatively simple design. Although the design is for a general DC system in transportation, various applications, such as datacenters and residential buildings, have compatible protection requirements and could benefit from the proposed solution.

The SSCB with LCL in this research requires further studies to confirm its suitability for high-power DC applications. To further enhance this research, the following areas are proposed for future investigation.

- *Loss estimation:* Accurate calculation of semiconductor losses during LCL is required to minimize wear and estimate component lifespan. The design requires further study of component selection, thermal management, and current balancing. Additionally, the SSCB's efficiency must be characterized by measuring power losses under nominal conditions.
- *FPGA Implementation:* Deploying protection controllers on FPGAs could streamline hardware design, reduce costs, enable field updating, and increase flexibility without PCB modifications. Comparative benchmarking against the analog controller used in this work is essential to quantify tripping delay, false tripping, PCB relative complexity and possibly electromagnetic interference immunity.
- *Scalability testing:* The scalability of the SSCB prototype, designed for parallel MOSFET configurations, should be assessed. Testing the LCL under higher average currents is necessary to validate the suitability of the proposed SSCB with LCL for high power DC systems. In such case, self-sufficient modules comprised of a three-level gate driver and MOSFET are necessary. Furthermore, including a buck converter on the gate driver would increase the flexibility of the third voltage level, which could facilitate the balancing of power losses among MOSFETs during LCL operation.

VII. OUTLOOK AND CONCLUSION

The development of advanced protection technologies is vital for the widespread adoption of future mobile DC systems, which are critical for sustaining modern transportion. DC

protection is an enabling technology, yet current limitations hinder the adoption of DC power systems, particularly in high-power transportation systems.

This work demonstrates that existing, robust SSCB technology can be significantly improved with modifications to its control mechanisms that are relatively simple to implement. The proposed three-level gate driver architecture enables the integration of high-speed SSCBs and LCLs using a shared front-end, enhancing selectivity and reducing system complexity. The proposed SSCB demonstrated a clearing time close to 200 ns, with a peak current of 20.9 A. The LCL functionality based on the three-level gate driver was also demonstrated, limiting the current to 3.3 A for 20 μs. Experiments suggest that the proposed SSCB can reduce unnecessary tripping while containing severe short circuits, which is necessary for several applications. A comprehensive guideline to upgrade and implement a LCL in a SSCB highlights the relevance of this research for the development of DC systems in general.

This approach is particularly relevant given the high cost and perceived value of DC protection technologies currently on the market. By incorporating additional functionalities, such as LCLs, into existing platforms, the value and feasibility of these solutions grows. LCL technology, adapted from aerospace, can be customized for less demanding applications to avoid unnecessary disconnection of critical loads during key operations.

By enabling advanced protection functionalities without the stringent requirements of aerospace systems, these innovations can promote the adoption of DC systems in diverse applications. This would unlock significant potential for cleaner energy technologies based on DC systems, contributing to a more sustainable future.

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