Investigating Competing Failure Modes in Microelectronic Devices Due to Small Temperature Variations

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***Abstract*— Electronic packages with solder interconnects, such as Chip Scale Packages (CSP) and Ball Grid Arrays (BGA), are extensively utilized in various applications, including cell phones, smartwatches, and electric vehicles. The advancements in technology and the features within these applications have led to an increase in power cycles within the packages. This combined with a reduced time to market makes their reliability testing more challenging. With the increased power cycles, even the small temperature variations (ΔT) within an Integrated Circuit (IC) package contribute to the increased susceptibility of devices to failures, often triggering a complex interplay of competing failure modes. Thus, it is crucial to understand the interplay between various failure mechanisms in real-world scenarios for evaluating and overseeing the dependability and efficiency of electronic systems. This paper presents an overview of the impact of small temperature variations on component reliability. In addition, a simulation-based preliminary study is carried out on a Wafer-Level Chip Scale Package (WLCSP) by implementing a thermal load corresponding to an active power cycle. The results are analyzed to locate possible failure locations within the solder bumps based on the accumulated plastic strains for different amplitudes of thermal load (ΔT). Finally, the necessity for a new testing strategy based on variable (ΔT) is highlighted.**

Keywords — component, failure modes, temperature variations, long lifetime

I. INTRODUCTION

The ongoing trends in microelectronics show a significant shift towards miniaturization reaching micron-scale dimensions, coupled with a rise in the integration of technology and functionalities [1]. The current utilization of the smaller package i.e. Wafer Level Chip Scale Package (WLCSP) and Ball Grid Array (BGA) in modern-day electronics has turned out to be the most competent with respect to characteristics. Short interconnections, the smallest form factor, and lower cost make it impeccable for cellphones, wearable electronics, and automotive applications which require longer lifetimes[2]. According to a report provided by Deloitte claimed that more than 1000 chips used in modern Electric Vehicles (EV)[3]. An important consideration in ensuring the high quality of packaging components is the evaluation of the reliability lifespan in electronic packages.

The characteristics of these applications, along with technological developments, have increased the number of power cycles in the packages. With advancements come layers of complexity, making it increasingly challenging to comprehensively evaluate the reliability of these complex automotive systems. Power cycles do not only refer to switching on and off the package continuously, they also induce internal heat within the package. Throughout operational cycles, the die functions as a heat source, inducing non-uniform temperature distribution within the package. During operational cycles, the die generates heat, causing temperature variations (ΔT) that are unevenly distributed across the package. This leads to thermal stress, which manifests as package deformation due to a mismatch in the coefficient of thermal expansion among the package components[4]. Thermal stress can lead to various failure modes in the package and the solder joints, and considering much research in the past solder joint reliability still remains a significant challenge in WLCSP technology.

Therefore, the objective of this work is to highlight the importance of small temperature variations (ΔT) concerning a high number of power cycles, The possible competing failure modes in the solder joint due to small loading conditions, followed by the COMSOL-based thermomechanical simulation of the WLCSP and comparison of the results (viscoelastic strain) based on different (ΔT). An example of WLCSP can be seen in Figure 1[5].

Apart from that, this research will also highlight and discuss the necessity for a novel variable-based testing approach (ΔT). It has been observed that these electronics exhibit different temperature bins in the field, indicating varying ΔT values for each temperature bin. The loading is not continuous but rather a variation of loads. To comprehend extended lifetimes, it is imperative to analyze the efficacy of currently employed standardized stress-based tests defined by JEDEC, a globalized industrial standard body, such as Temperature Cycling (TC), Thermal Shock (TMSK), Power and Temperature Cycling (PTC), Power Thermal Mechanical Cycling (PTMCL), Accelerated Life Testing (ALT), Highly Accelerated Life Testing (HALT), and others. These methods might be

unable to sufficiently account for temperature changes encountered by devices in the field.

Figure 1 WLCSP9, wafer-level chip-scale package; 9 bumps

II. COMPETING FAILURES DUE TO THERMAL CYCLING

Competing failure modes (CFM) describe the state in which multiple failure modes interact with one another within a system or component, possibly impacting or speeding up the occurrence of each other. As stated in various ways, competing failure modes entail the interaction or interdependence of various failure mechanisms.

In the realm of IC packaging technology, the reliability of the solder joint is the key aspect for ensuring the longer life span of the microelectronics device. However, To grasp the concept of competing failures, engineers and researchers must acquire a comprehensive understanding of potential failure modes associated with the thermal stress within the IC package. Some of them are listed in Table 1.

Table 1 Failure modes under thermal stress

Sr.no	Failure modes	
	Failures	***Root Cause***
1	Crack Propagation	Factors like temperature range, dwell time and ramp rate on the materials cause creep deformation and lead to extended cracks in solder joints[6], [7].
2	Thermal Fatigue	CTE mismatch of different materials causes mechanical stress within solder joints leading to crack initiation[8], [9].
3	Brittle Fracture	Due to the reflow process IMC layer formed within the solder joints. That exhibits sudden fracture of the solder joint without notable plastic deformation[10], [11]
4	Whisker Formation	Solder whisker growth is promoted by thermal stress when tin is in low CTE base materials. This can lead to short circuits [12], [13].
5	Delamination	CTE mismatch, moisture ingress, and hydrothermal stress due to solder reflow cause delamination resulting in cracks in solder joints [14], [15].
6	Void Formation	Entrapment of gas or moisture in solder balls leads to premature failure due to thermal stress[16], [17].

It is essential to understand how these failure modes compete in real-world scenarios, Therefore some examples from the literature are listed to illustrate the competing failure modes within the IC packages. In the literature, CFM is also stated with different terms such as early and late fails, hard and soft failures, and surface initiation and internally nucleated failures.

Gerald et al.[18] presents the example with the fatigue statistics of the nickel alloy (Rene95), which shows the existence of two separate failure distributions on an S-N plot. One distribution is often associated with fatigue failure starting from surface sites at higher stress levels, whereas the other comprises failures nucleated from interior sources usually at lower stress levels can be seen in Figure 2 (with permission). Further supported his argument with the test result, which was performed on nickel alloy. Two failure sites were observed and can be seen in Figure 3 (with permission).

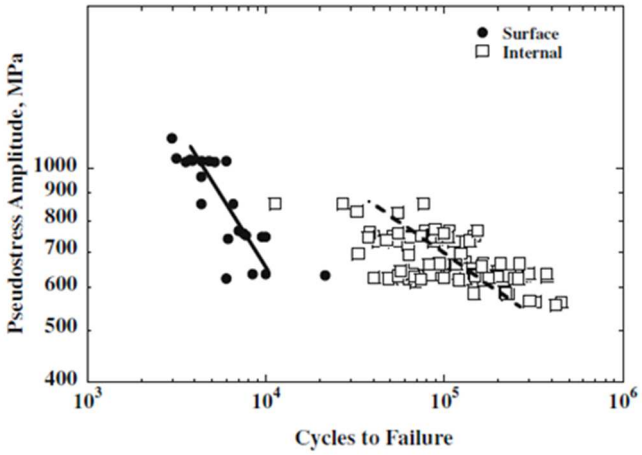

Figure 2 Fatigue data representation of nickel alloy

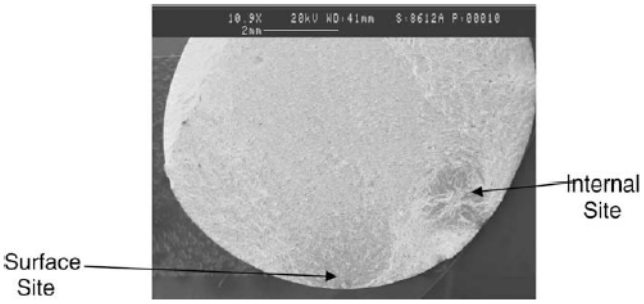

Figure 3 Fatigue fracture surface demonstrating competing surface and internal initiation sites

Xing Liu et al.[19] showed the experimental evidence of the four test series (T1 to T4) performed to analyze the effects of thermal stress on the package with different operating conditions. These loading condition based on different on and off duration of the package. Two out of four packages show the sign of the CFM. In Test 2, it is observed that the voltage collector to emitter (VCE) trend continues to show the aging of the bond wires, but chip solder fatigue becomes the dominant failure. In Test 4, it was observed that the solder beneath the bond wire was destroyed, and cracks also formed on the bond. However, if the experiment continues, wire bond lifting can be observed, potentially becoming the main cause of failure.

Van Soestbergen et al.[20] found that in QFN packages two failure modes can occur within the solder joints, as

shown in Figure 4. The primary failure mode involves a brittle fracture occurring in the intermetallic region adjacent to the solder joint and appears to be more common in early failures. Another is the crack within the solder bulk, observed for the later fails.

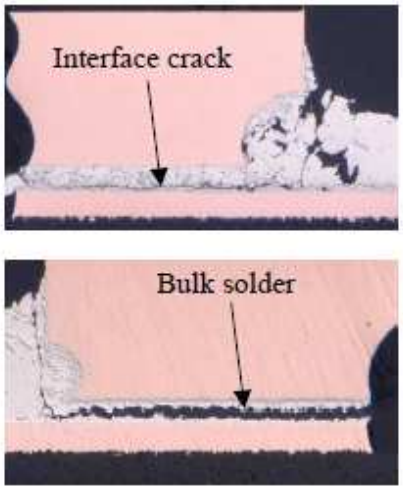

Figure 4 illustration showing a cracked intermetallic layer on top and bulk solder fatigue below

Van Soestbergen et al.[21], in other research performed simulations for WLCSP based on two different solder alloys, traditional alloy, and stiff alloy. The findings have shown that mean life for stiff alloys has improved, but earlier failures have been observed which are caused by Under-Bump Metallization peel-off (UBM). However, the latter fails were observed within the solder itself. It is also known as the competing failure mechanism, which can be seen from the lower shape of the Weibull distribution in comparison to the traditional solder and represents the competing failure modes for the stiff solder alloy (see Figure 5).

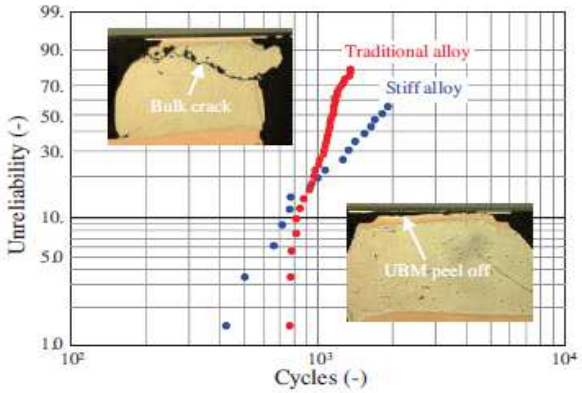

Figure 5 Weibull distribution for WLCSP for Traditional alloy and Stiff alloy

Roucou et al.[22] presents the result by using Weibull analysis can be seen in Figure 6, the graph shows that passivation cracks will occur in early failures or after a certain interval of the stress (lower cycles). However, the dominant failure comes out to be solder joint fatigue (high cycles). The graph also depicts the failure interaction point, at which the second failure mechanism becomes predominant, indicating a competing failure mechanism.

Therefore, by thoroughly analyzing and addressing these competing failure modes, we could create effective mitigation techniques to improve the reliability and performance of IC packages.

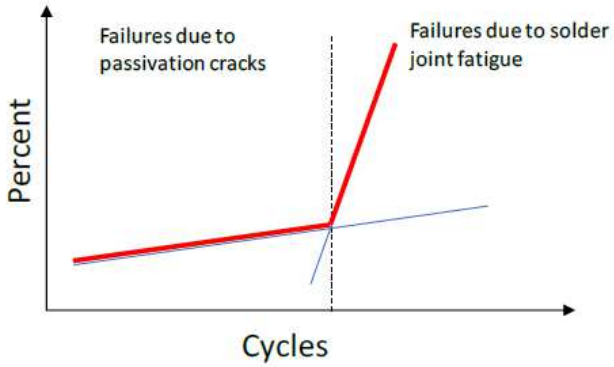

Figure 6 Competing Failure modes in WLCSP

III. Small Temprature Variations

According to the example given in section 1, regarding the advancement in microelectronics which comes with the challenge of an increased number of power cycles concerning automotive. For some devices and applications, the number of cycles can reach hundreds of thousands to millions of cycles during their useful life. These devices' applications are not limited to the automotive industry. It extends to many more applications, for example, mobile phones and the Internet of things using for instance Near-field communication (NFC), Ultra-wideband devices (UWB), etc. All of these applications require improved package reliability. To examine the reliability of these devices power cycling tests could be used to perform under the specified loading conditions. In general, these tests can be performed with high current subjected to large temperature swings from (e.g. -40 to 180°C, -40 to 125°C, etc…) and in general ΔT greater than 50°C. These accelerated tests can under- or overestimate the device's lifetime consumption, diverging significantly from actual field conditions.

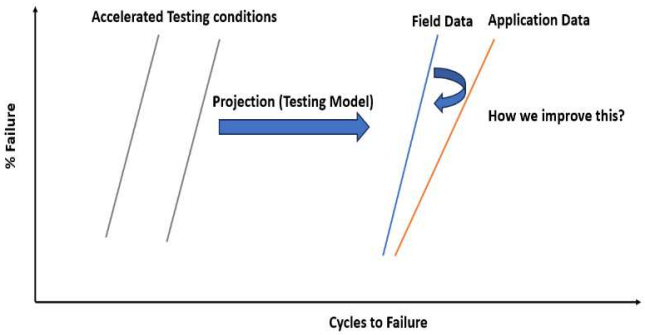

Figure 7 An example demonstrating the gap between field and testing results.

Figure 7 illustrates the tangible difference in Weibull distribution that can be observed between products that are tested in a field environment and others which is tested in an accelerated environment, with different testing conditions. This difference can be seen due to the overestimation of product lifecycle by accelerated testing,

prompting the question: What actions are necessary to narrow this gap and improve accuracy.

In such scenarios, it's essential to adjust the parameters of power cycling testing to operate within a more realistic range with respect to the applications mentioned above. For instance, the temperature variation within the package should be limited to a relatively narrow range, typically between 1 to a few tens of degrees (<50°C)[23]. At Low ΔT very high numbers of cycles are required to observe degradations which lead to very long test durations expected up to several years. Therefore there is very limited literature available concerning the reliability of the packages under low temperature swings. That's it is one of the reasons to work and highlight the importance of this new field and to find the answer to the questions listed below:

- How the test duration can be reduced.
- Does failure change or failure site shift in low-temperature swings.

For millions of expected power cycles, the test duration can be reduced by increasing the switching frequency within the range of [10Hz to 100Hz]. Francois et al. [24] developed a test bench in which testing time has been reduced by increasing the switching frequency, a series of tests have been performed at 10 and 20°C with frequencies 50 and 100 Hz. In the results, it has been observed that Vce is increased by 20mV after one billion cycles, but no physical damage has been identified. A similar approach for reducing test time has been used by Christian et al. [25], power cycling tests with 50Hz and low-temperature swing is performed. Two failure locations have been observed in these tests. When a test was performed with (ΔT) 50k the failure site appeared at the bond wire and with (ΔT) 25k failure site was noticed in the solder layer, which represents the shift of the failure site.

IV. WLCSP FEA Simulation Findings

The study focused on examining the impact of small temperature variations on the solder balls. The package comprises a 3x3 solder bump array, as depicted in Figure 1. Nine solder balls are used, each with a pitch of 0.5mm.

The size of the PCB (3mm × 3mm × 0.07mm) is taken twice concerning chip size, to reduce the effect of PCB on the solder joints. It consists of three layers top and bottom contain dielectric and the middle layer contains Copper. The solder balls connect directly to the copper layers on the die- and PCB-side.

Lead-free solder joint material model SAC355 (Sn96, Ag3.5Cu0.5) from the COMSOL library is used with a sphere radius of 0.2mm, and the upper and lower radius of the solder joints attached to the pads is 0.13mm. The thickness of the chip is 0.23mm, and it contains five different layers starting from Die, Die Passivation, Dielectric 1, RDL, and Dielectric 2. The complete FE model can be seen in Figure 8.

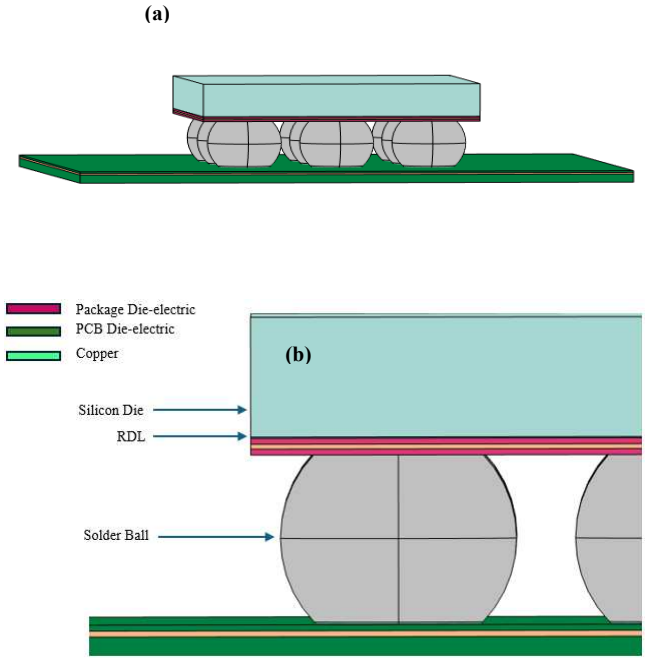

Figure 8 Figure 8 (a) FEM of WLCSP 9 with PCB, (b) Detailed structure of WLCSP with a close look of solder ball

The thermal cycle is taken as the loading condition for this package applied on the lower surface (active side) of the die, which can be seen in Figure 9. This temperature profile incorporates four stages, 1st stage is the ramp up to the positive dwell, the duration of the positive dwell is 2nd stage, 3rd stage is the ramp down to the negative dwell, and the duration of the negative dwell is stage 4th.

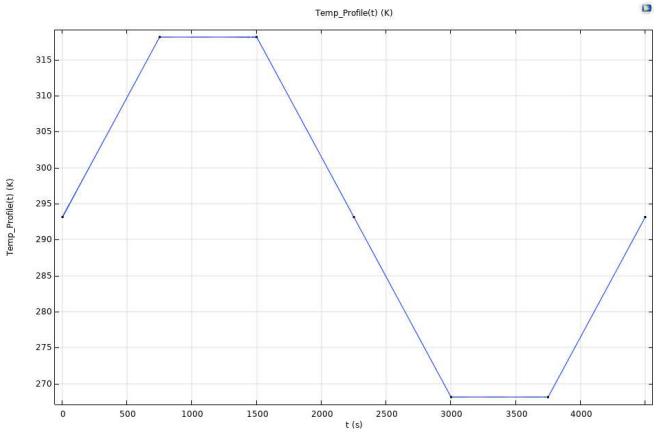

Figure 9 Thermal stress profile

Five different small temperature variations loads are applied ΔT (50 to 10 °C), in which the ramp up or ramp down is kept 2°C per minute for all cases. An elastoplastic model with hardening has been used to observe the deformation, stress and strain behavior of the materials. Equivalent plastic strain (EPS) and von Mises stress analysis method have been used to identify the location where the maximum degree of stress and strain occur. The identified location with stress concentration is a potential site for crack initiation.

The results of the simulation indicate that the highest EPS appears at the top part of the solder joint, from where

it is attached to the copper layer on the side of the silicon die. The EPS distribution on the solder joint closely corresponds with the failure mode outlined in Figure 10.

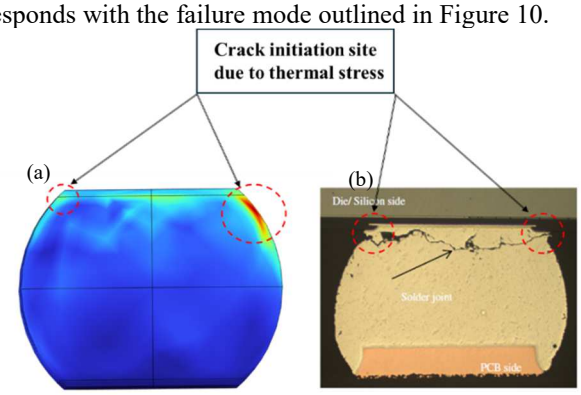

Figure 10 (a) Simulations showing equivalent plastic strain, (b) Experimental results from literature

Figure 10 b[26] represents the failure mode known as fatigue crack which is typically indued due to thermal stress. The crack site from the experimentation is similar to the maximum EPS depicted in the simulation result. The maximum EPS value with respect to five different loading conditions can be seen in Figure 11 below.

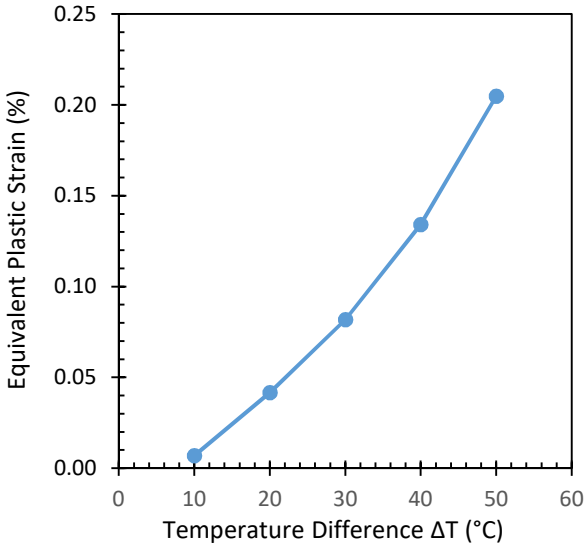

Figure 11 Accumulated equivalent plastic strain (EPS) after one temperature cycle for different ranges of temperature difference (ΔT)

Across all load conditions, these values have been taken from the same region of the solder balls.

V. Conclusion

By exploring the literature and developing the COMSOL model simulation for WLCSP under small thermal loading conditions ΔT (50 to 10 °C), the results presented indicate that: as the mismatch in the coefficient of thermal expansion (CTE) occurs the package undergoes thermal stress, the edges of the solder ball experience the maximum EPS, the point from where the crack could be initiated. It shows that the trend we got from the simulations co-relates well with results from stress-based experimental testing.

This work can be further extended to estimate the fatigue life of the IC packages and also helps to set up an experimental setup with faster test protocols, which can reduce the testing time.

VI. Future Work

If a package is tested in a single loading condition, one ΔT is applied to the package and board at a time. A new testing strategy might not be required. In small thermal stress scenarios, large cycles can be achieved by increasing the power cycling frequency. But for variable loads (see Figure 12) [27], currently used standardized stress-based tests for example, (TMCL, TMSK, PTMCL, ALT, HALT) techniques ought to be questioned because they might not cover the temperature variation that which device experienced within the field.

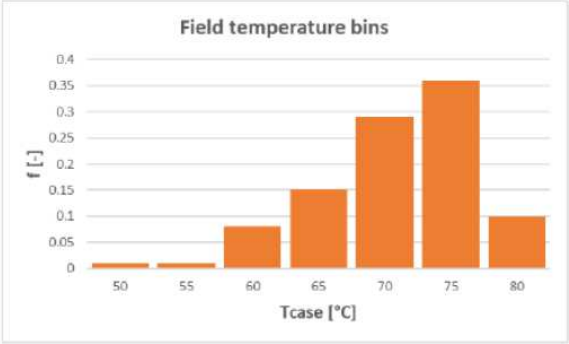

Figure 12 Variable temperature bins

Step-stress testing and variable temperature accelerated testing (VTAT) are two alternative methods for testing. Step stress testing combines traditional reliability testing with over-stress testing. These methods offer potential alternatives to traditional testing approaches. VTAT, or Variable Temperature Accelerated Testing, is an effective approach for testing products in real-world conditions. By simulating temperature variations experienced in the field, VTAT ensures comprehensive coverage of different temperature changes as can be seen from Figure 13 [27].

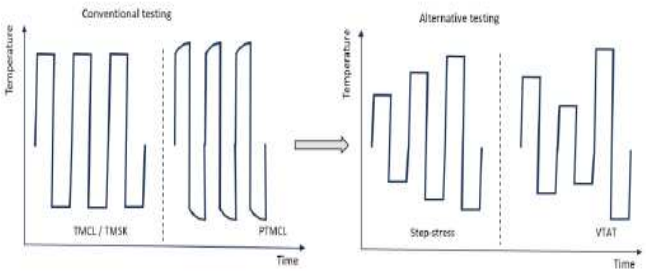

Figure 13 Current Testing strategies V/S Variable temperature strategy

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