An ASIC with Bipolar High-Voltage Transmit Switching for a Single-Cable Intra-Vascular Ultrasound Probe

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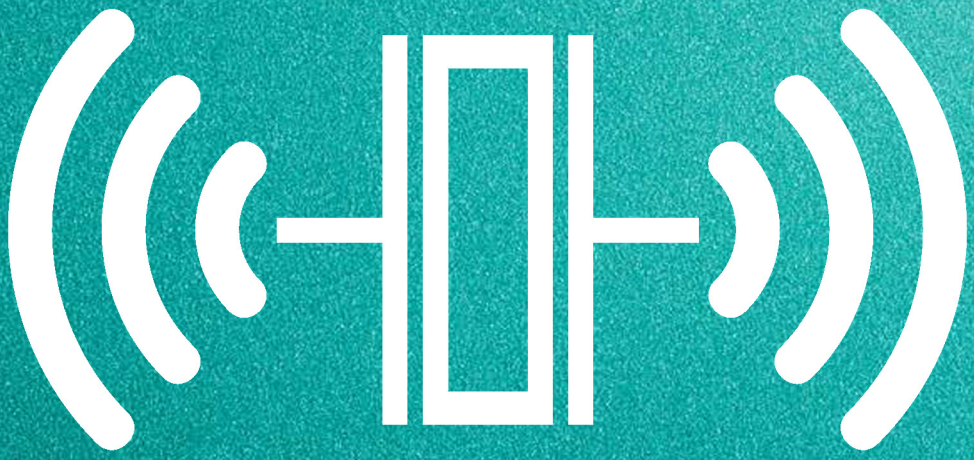

TU Delft

An ASIC with Bipolar High-Voltage Transmit Switching for a Single-Cable Intra-Vascular Ultrasound Probe

by

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TU Delft

Abstract

उद्यमेन हि सिध्यन्ति कार्याणि न मनोरथैः।
न हि सुप्तस्य सिंहस्य प्रविशन्ति मुखे मृगाः ।।

An ASIC is presented for intra-vascular ultrasound imaging. Despite being connected via a single coaxial cable, it is able to pass arbitrary high voltage bipolar signals to the transducers for acoustic imaging.

The thesis talks about the need to reduce the cable count to one and reviews the existing work in literature. It builds up on an existing single cable design and focuses on the transmit part to make it compatible to a large number of ultrasound imaging modes by allowing it to pass high frequency signals up to 20MHz and bipolar signal voltages up to $\pm 25V$.

The chip is phantom powered and thus its power supply and signals are transmitted on the same cable. The transmit switch designed for this ASIC is powered by and controlled by an on-chip low voltage supply and circuitry. The prototype ASIC has been designed in TSMC 180nm HV BCD Gen2 technology. This single cable design has 16 elements for transmit and 64 elements in the receive mode and was evaluated using simulations.

Keywords: Intra-vascular ultrasound, single-cable, bipolar, high-voltage, CMOS, transmit switch, bi-directional isolation.

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R.N.Nagarkar
Delft, August 2019

Contents

1

Introduction

In the 21^{ST} century, there has been an increase in sedentary lifestyle of people accompanied by a lack of exercising and an unhealthy diet. These factors give rise to noncommunicable diseases like heart diseases, diabetes, high cholesterol levels and obesity [1]. A combination of these may lead to build-up of plaque in the arteries, which comprises of fat and cholesterol. Plaque build-up causes stenosis, which is narrowing of the arteries restricting blood flow or even complete blockage of the arteries. Figure 1.1 shows how a healthy artery with plaque buildup could get blocked. These blockages hamper the normal functioning of arteries and result in stroke which may even lead to death [2].

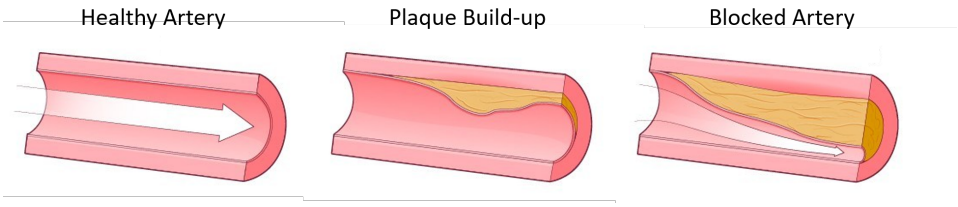


Figure 1.1: Stages of plaque build-up in the artery [3]

The availability of high-quality, low-cost and easy-to-use diagnostic tools would be beneficial in the early detection of stenosis in the arteries. A commonly used diagnostic technique is Intra-Vascular Ultrasound (IVUS) imaging.

1.1. Intra-Vascular Probes for Diagnosis of Stenosis

To determine the exact location of the blockage, intra-vascular ultrasound (IVUS) imaging can be used effectively in the arteries (example coronary arteries). The imaging helps diagnose the amount of plaque deposition at any specific location in the artery, helping the clinicians to assess the extent of stenosis or narrowing in the artery. [4]

IVUS involves the use of a miniature probe which is attached to the tip of a catheter entering the arteries and gets mechanical support for better directionality in the artery from the catheter guide wire. IVUS probes use piezoelectric transducers or capacitive micromachined ultrasonic transducers (CMUTs) for imaging [5]. Figure 1.2 shows a forward-looking IVUS probe with a CMUT array.

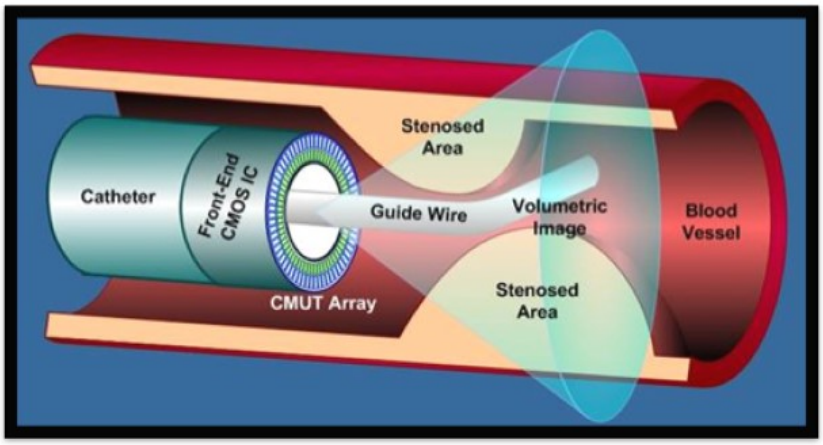


Figure 1.2: Artist impression of IVUS probe inside the artery [6]

1.1.1. Working of the IVUS Probe

The IVUS probe has piezoelectric transducers or CMUTs which are excited with high voltage electrical pulses to produce high pressure acoustic waves, during the transmission phase. The acoustic waves on interacting with the tissues, artery and plaque get reflected due to the difference in their acoustic impedances. As the echo pulses take different times to reach the transducer in the receive phase, it helps in calculating the distances of the different objects. These reflected acoustic waves are then picked up by another set of transducers in the receive phase to generate electric signals, which are then amplified on chip. These amplified signals are then sent to the system side for processing and generating the image [4].

An array of ultrasound transducers is used on the chip to generate an image of high spatial resolution. In case of a 1D array, a 2D image can be generated, whereas using a 2D array of transducers helps in generating a 3D image from the received acoustic signals. Various array shapes exist for the IVUS probes. In side-looking probes they are mostly 1D or 2D arrays, while in the front-looking IVUS, they could be tiled, circular or even spiral in shape [7].

1.2. Prior Art

In literature, various IVUS designs exist using either piezoelectric transducers (PZTs) or CMUTs. PZTs and CMUTs both can be used for transmit and receive elements for bipolar high-voltage signals. In the case of CMUTs, during the transmit phase, the element membranes vibrate due to electrostatic attraction, by sending high voltage bipolar signals. As the electrostatic forces are unipolar, DC bias voltage larger than the transmit pulse swing is needed for the proper functioning of CMUTs [8].

This is a huge disadvantage from a design perspective which aims at limiting the cable count to one as a constant biasing voltage cannot be provided, thus PZTs are used in this thesis. With a shift from 2D to 3D IVUS imaging, the transducers move from a linear array to a 2D array, increasing the total number of transducers. The increase in transducers cannot be followed by an increase in the chip size in forward-looking IVUS as it still needs to fit inside the catheter.

The conventional solutions in IVUS involve the transducer elements being individually wired to the imaging system. With an increase in the number of transducer elements, an ASIC is used for IVUS to keep the cable count at a minimum with techniques like multiplexing or on-chip beam-forming [9], [10], [11].

Numerous contributions have been made in literature to reduce cable count. The work done by Chen et al. showed that a single cable design was possible and was carried out with only the receive part [12]. Tekes et al. showed that with a smaller count of cables, 13, it was possible to make an IVUS with 64 transmit and 56 receive elements with a separate power supply for transmit and receive [13]. To have higher resolution of the image, it is essential to have a larger number of transducers. In the work presented by Tan et al., a digital probe with an even more reduced cable count of four, showed transmit and receive capabilities with 16 elements in transmit and 64 elements in receive [14].

Despite these techniques, the cable count is large and needs to be reduced to a minimum to be able to fit inside the catheter. A solution to this is to use micro-coaxial cables for smaller probes. But, they come with the disadvantage of higher capacitance relative to the transducer elements and attenuate the signal and increased costs.

Van Willigen designed a single cable chip which supports unipolar pulses of 30V on a single cable design with 64 transmit and receive elements [15],[7]. The circuit was integrated on the transducer tip and the receive signal was amplified locally. The design was taped-out in 180nm HV BCD process and was validated by imaging needle phantoms.

1.3. Objectives

Ultrasound imaging can be conducted in several ways like A-mode, B-mode, Doppler, Pulse inversion mode or Harmonic mode. The different imaging modes require different pulse shapes which last for a different time duration. Thus it is essential to have a chip which could allow the transmit signal to be arbitrary, from square unipolar pulses to sinusoidal

bipolar signals. With the number of applications increasing for small ultrasound probes, it is also important to shift to a design which supports versatility with minimum cable count.

1.3.1. Motivation for shifting to Bipolar Signals

The motivation for the ASIC to pass bipolar signals had multiple reasons. Historically, ultrasound imaging systems transmit bipolar signals as it avoids a DC bias on the transformers used in these systems and thus reduces power dissipation. Another advantage of switching to bipolar signals would be lower power dissipation on the system side. Also, bipolar pulses show better energy efficiency across the frequency spectrum. [16],[17].

Ultrasound imaging techniques like pulse inversion are widely used for contrast imaging [18]. This involves transmitting two waveforms which are phase shifted by 180°. A chip capable of transmitting bipolar signals will have the capability to employ such techniques with much ease.

Thus, a chip with arbitrary signal transmission capabilities in frequency, amplitude and shape would be of the utmost importance as it can be easily hooked up to any ultrasound pulse generator and be able to perform a variety of imaging schemes.

Table 1.1 shows an overview of the work done in literature for minimizing the cable count and the objectives of this work. The design proposed in this thesis starts with Van Willigen's [7] design as a base framework and the work focuses on the transmit part.

Table 1.1: Prior art and Objectives of this work

	[12]	[13]	[14]	[15]	This Work
Technology	0.18 μm	0.35 μm	0.18 μm	0.18 μm	0.18 μm
# Coax Cables	1	13	4	1	1
Power (RX)	13.2 mW	20 mW	10 mW	6.4 mW	6.4 mW
Bandwidth	20 MHz	40 MHz	16 MHz	24 MHz	24 MHz
RX Channels	1	56	64	64	64
TX Channels	–	64	16	64	16
TX Voltage	–	25 V	26 V	30 V	±25 V

1.3.2. Piezoelectric Transducer

Piezoelectric elements depending on their material and dimensions could have different resonant frequencies and impedances. As the amplifier proposed in [7] has a current input, the parallel capacitance of the Piezo element has a reduced influence on the signal.To model the circuit behaviour of the transducer, the Butterworth Van Dyke model was used as shown in fig. 1.3.

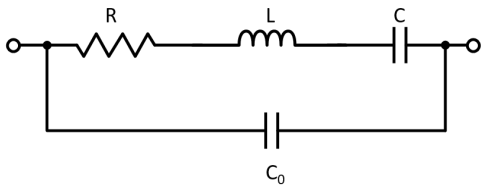


Figure 1.3: Butterworth van Dyke model [19]

Table 1.2 shows the model parameters for the PZT and its extracted parameters. The targeted transducer for this thesis is 80µm x 80µm with a resonant frequency of 14 MHz as used in [7],[20].

Table 1.2: PZT model parameters

Element Dimensions	R (kΩ)	L (μ H)	C (fF)	C_0 (fF)	F_{RES} (MHz)
80 μm x 80 μm	23.6	810	220	310	14

1.4. Existing Single-Cable Design by Van Willigen

The prototype ASIC designed had 64 transducer elements which were used in transmit as well as receive. With the help of additional circuitry, this chip could be connected to an imaging system which sends the transmit signals to the chip and then creates an image from the signals generated on chip in the receive mode.

The chip is connected by a 42 AWG single coaxial cable of length 2m. Table 1.3 shows the cable parameters. This cable was chosen as its attenuation was less than 3 dB in the frequency range of interest.

Table 1.3: Coaxial Cable Parameters [21]

Parameters	42AWG
R_{DC}(Ω /m)	7.5
C_{gnd} (pF/m)	110
L (nH/m)	275
G (nS/m)	660
Attenuation (dB/m)	0.7 (at 10 MHz)

The cable is characteristically terminated with a matching resistor on the system side to prevent reflections. Having the matching resistance on the system side is advantageous as

its power dissipation would be off-chip and does not heat up the IVUS probe. This thesis will be using the same coaxial cable setting as can be seen in fig. 1.4.

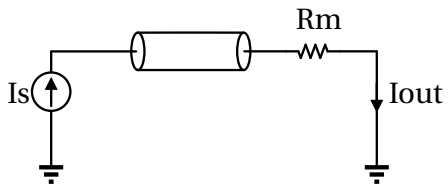


Figure 1.4: Receiver side termination of Coaxial Cable

The working of the chip is split into three main parts, a configuration phase, transmit phase (TX) and a receive phase (RX). The configuration phase involves the programming of transmit and receive switches which would select a particular transducer element which would receive the high voltage transmit pulse and receives the acoustic echoes respectively for image generation.

As the chip does not have any external signal or clock lines, the transmit and receive switches need to be configured before each TX-RX cycle. The data bits for configuration are pulse-width encoded with the clock. This encoded data is modulated over the $3V$ DC supply voltage available on the line during the configuration phase and has a value of $500mV_{PP}$. Figure 1.5 shows a block diagram of the single cable ASIC and the figure 1.6 shows the various wave-forms of voltage and current on the cable during the three stages of a TX-RX cycle.

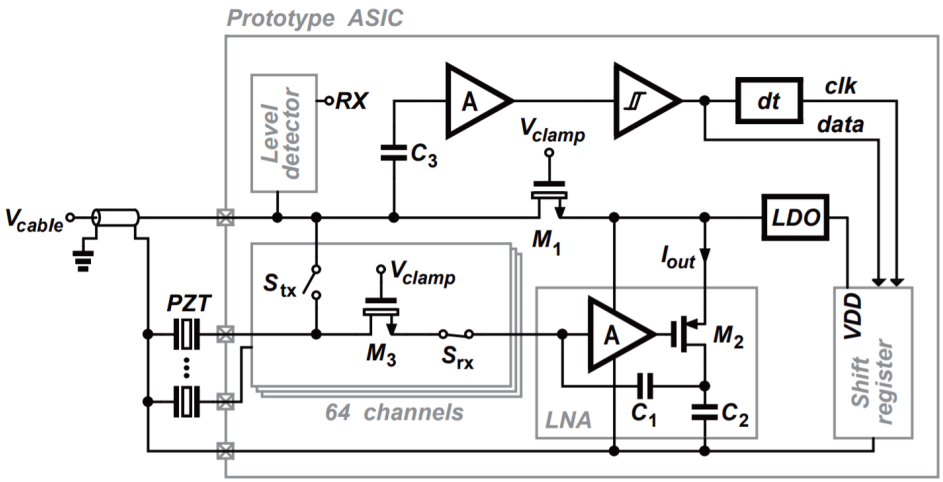


Figure 1.5: Block diagram of single cable ASIC [15]

The modulated data in the configuration phase is separated from the supply with the help of the coupling capacitor C3 as seen in fig. 1.5. As the modulated data is only a fraction of the supply voltage, it is first amplified and then converted by a Schmitt-Trigger into binary data. The reference voltage for the amplifier is half the DC supply voltage. This circuit is made insensitive to the DC level by having a short time constant of the feedback and the coupling capacitor. The schematic of the data recovery circuit can be seen in fig. 1.7.

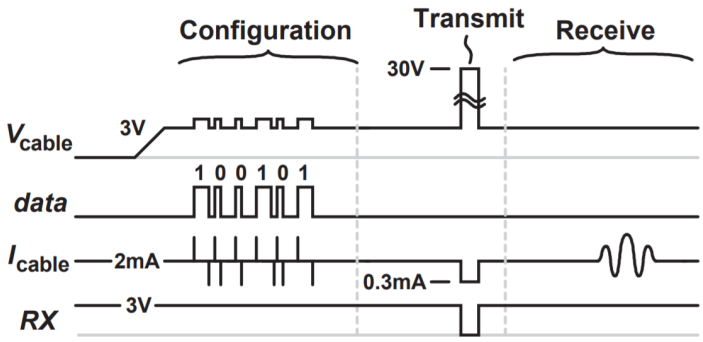


Figure 1.6: TX-RX cycle wave-forms on the cable [15]

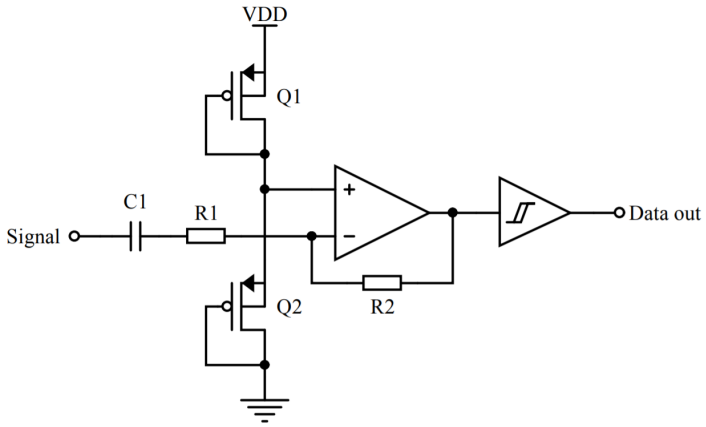


Figure 1.7: Data recovery circuit [7]

The data bits recovered are loaded into shift registers which are connected to the gain settings of a low noise amplifier (LNA) and various transmit and receive switches, which in turn are connected to a transducer element each. These recovered data bits are then used to extract a clock signal on chip with the help of the clock recovery circuit as shown in fig. 1.8. The clock signal is designed to have a rising edge after a half-period delay from the rising edge of the recovered data stream. This delay is implemented with a small capacitor which charges during the rising edge of the recovered data-stream and is emptied by a weak current source. After the configuration of the chip, high voltage transmit pulses of 30 V are sent via the cable to the selected transducers for generating acoustic signals.

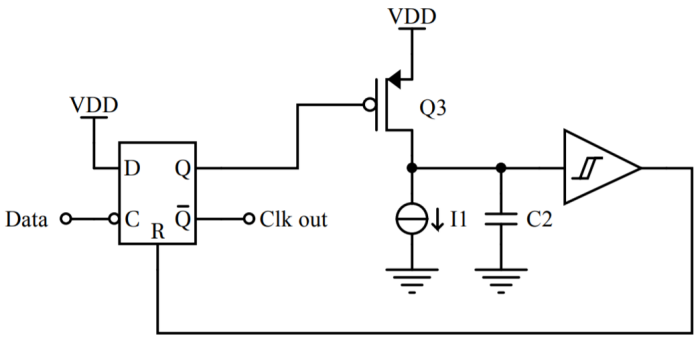


Figure 1.8: Clock recovery circuit [7]

High voltage signals passed on the cable during the transmit phase can go as high as 30 V and are supposed to be seen only by the high voltage transmit switch. The receive circuitry and other blocks are implemented using low voltage devices and thus need protection from these high voltage signals. To protect the low voltage circuitry (3V devices), a clamping voltage is generated which drives the transistors M1 and M3 (fig. 1.5), ensuring their source voltage stays below the clamping voltage. A level detector on the chip detects when the cable voltage is lower than 6V for a certain time period and then switches the chip to receive mode.

Figure 1.9 shows a circuit level implementation of the transmit switch. The capacitor C6 holds the control bit during configuration phase and is used to turn on or off M5. The high voltage pulse coming from the cable gets divided by C4 and C5 when M5 is on and causes M4 to turn on with a reasonable gate voltage and pass the signal to the transducer element. With M5 off, the parasitic capacitance of M5 is in series with C5 and ensures a low gate-source voltage on M4, thus preventing the signal to reach the transducer. The advantage of this switch structure is its compact size and it does not need power supply during the TX phase, but it can only pass unipolar high voltage signals.

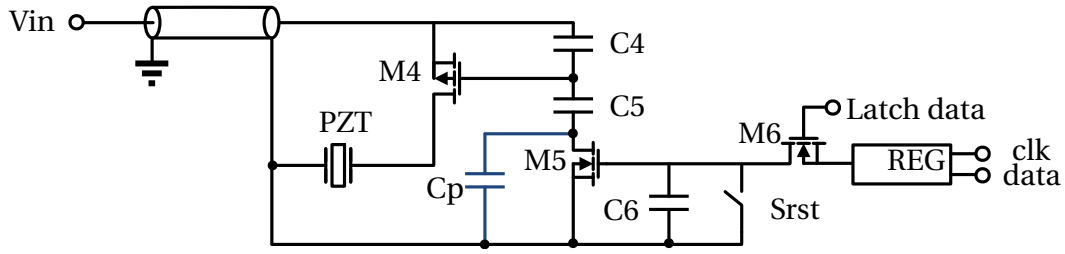


Figure 1.9: Transmit switch circuit implementation [7]

The final stage in the TX-RX cycle is the receive phase during which the 3V DC supply is again available on the cable from the system side. The chip on entering the receive mode, sends the received echo signals from the transducer selected in the configuration phase to the low noise amplifier (LNA) with programmable gain, which amplifies the small signal current and M2 in fig. 1.5 and generates the output current.

The retrieval of signal data for image processing involves the firing of one transducer in transmit and then receive of the signal from one receive transducer, thus in this case having 64x64 iterations. An off-chip trans-impedance amplifier (TIA) provides the DC supply voltage to the chip as well as converting the signal current to voltage and recover the received echo signals for image reconstruction on the system side.

1.5. Design Goals

The aim of this thesis is to design an ASIC which is connected by a single coaxial cable and is able to pass an arbitrary bipolar transmit signal with a peak amplitude of up to ±25 V for exciting the transducer and generate enough acoustic pressure for imaging.

The ASIC should be able to handle signals of different frequencies from 2 MHz to 20 MHz for ±25 V pulses. It is desirable for the probe to have an off isolation of at least 40dB for the

transmit switch.

The different waveforms on the transmit and receive channels can be seen as in fig. 1.10. It is acceptable to have a delay of 1µs between the start of transmit and receive signals because the associated loss in near field imaging is limited. The receive echo pulse would have the same frequency as that of the transmit signal. As seen in the waveform, there is an offset during the receive phase because the DC supply voltage is available again

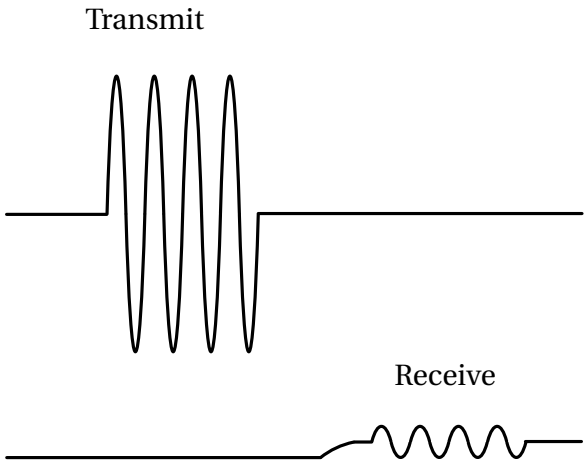


Figure 1.10: Transmit and receive Waveforms on different channels

Black et. al calculated for the maximum power dissipation by ultrasound probes to be less than 100mW inside the catheter to avoid damaging nearby tissue [22]. Also, to ensure the coaxial cable can be contained inside the catheter, the coaxial cable should be 2m in length. The ASIC will be designed in TSMC 180nm BCD Gen2 technology and is simulated with a 2m 42AWG coaxial cable.

1.6. Thesis Organization

This thesis aims to present the methodology for arriving at an ASIC with bipolar high-voltage transmit switching for a single coaxial cable intra-vascular ultrasound probe. The chapters flow sequentially starting from the concept of possible circuits to their feasibility and their optimization for an overall good circuit.

Chapter 2 discuss the various architectures possible for different blocks of the circuit and the choices made.

Chapter 3 shows the chosen circuit implementations for the transmit switch and how they were integrated to the ASIC. It also discusses the circuitry designed for protection of the low-voltage devices.

Chapter 4 shows the various simulations performed to ascertain the correct working of the transmit switch and the peripheral circuitry.

Chapter 5 concludes the thesis discussing the goals at the start of the thesis and what all was implemented. It also discusses ideas for further improvements and future work possible in this thesis.

2

Architecture

This chapter walks through the architectures of the various blocks of the ASIC. The chapter starts by discussing the scheme for powering the ASIC, configuring it and receiving data on the same cable.

In the next section, various architectures for the high voltage transmit switch are discussed which allow the transmission of the bipolar high voltage signals to the transducer when enabled for acoustic excitation and when not connected are able to provide sufficient bi-directional isolation to prevent any signals reaching the PZTs and create false images.

The substrate in ICs is generally connected to the most negative supply available. This reverse biases the NMOS source-bulk and drain-bulk regions to prevent leakage of the signal. In the single cable design, the transmit voltage pulses go as low as $-25\,\mathrm{V}$. When the transmit pulse is on the cable, no power supply exists. Thus, it needs to be ensured that the substrate is correctly biased to avoid the forward biasing of these junctions.

The following section discusses the choice of opting for separate transducer elements for transmit and receive. The low noise amplifier used for amplifying the receive phase signal from the piezoelectric transducer is discussed.

Lastly, the modes for communicating with the chip for programming switches, data transmission and receiving are discussed.

2.1. Data and Supply over One Cable

Phantom power supply is a concept where the power and readout are done on the same cable. This technique has been used in audio and RF electronics quite commonly. The power supply can be separated from the data as the two are separate in the frequency domain. The power is relatively low frequency while the data signal is transmitted at a much higher frequency. In the case of ultrasound, the signals are generally above 2 MHz, so a similar approach could be taken. Figure 2.1 shows a diagram of the configuration data being modulated on the DC supply voltage and being separated out on the ASIC.

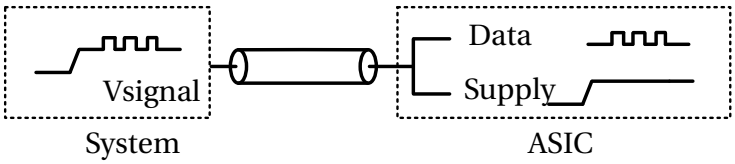


Figure 2.1: Data and supply on the same cable

Successfully shown in [7], for unipolar transmit pulses, the DC voltage can be supplied to the chip with clock encoded data for selecting the transmit and receive elements modulated over the supply in the configuration phase. With bipolar signals being transmitted over the cable, the protection of the data circuitry from the high voltage transmit pulses is necessary.

2.2. Transmit Circuitry

Ultrasound imaging involves the excitation of a piezoelectric transducer using high voltages to generate enough acoustic pressure. The high-voltages could be passed on to the transducer in two broad ways. Firstly, the chip could be connected to a high voltage power supply apart from a low voltage supply and be able to generate the high-voltage pulses on-chip. The second case involves the sending of high-voltage pulses from the system side and have a switching circuit which would be able to pass the pulses to a transducer element only if they have been switched on.

In the first category, the architectures commonly used produced the pulses on-chip using level-shifter circuits which could pass or stop the high voltage signals based on lower voltage control signals. Commonly used circuits which work on the idea of pulling the pulses to a higher supply are shown in fig. 2.2.

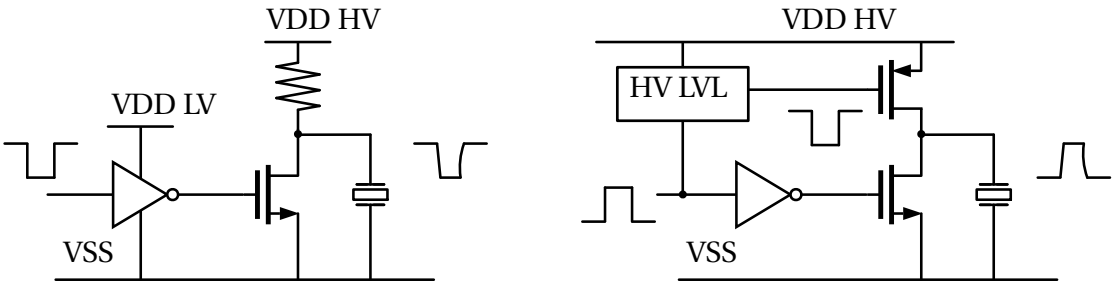


Figure 2.2: High voltage pulser generated on chip [23], [24]

Figure 2.2 (a) shows a pulser which consumes less area because of only one high voltage transistor, but it dissipates static current apart from power dissipated in exciting the transducer, making it power inefficient [23]. Thus, the resistive pull-up is an easy design with area advantage but has power limitations. Figure 2.2 (b) does not dissipate any static energy as the high voltage level-shifter can be used to switch off the PMOS when NMOS is not in action [24]. This comes at an added cost of area with many transistors needed to make the level-shifter circuits.

A disadvantage of these circuits is that they generate only unipolar pulses. They can be modified to provide bipolar pulses by having a high voltage positive and V_{SS} as a high negative voltage supply. But, implementation is impossible from the single cable design as it's not be possible to supply high and low voltages in one go.

In the second category, during the transmit phase, an excitation signal is passed on to the selected transmit transducer. A train of high voltage signal pulses is sent from the system side to the chip via the coaxial cable to the transducer. To ensure that the signal is passed only to a particular transmit transducer, a transmit switch is needed which would switch on to pass the high voltage signal and at the end of the pulse ground the element, while all the other transmit elements are shielded from the signal.

Various architectures for transmit switches were looked into which could help in passing arbitrary pulses to the transducer and help in carrying out different modes of ultrasound imaging[20],[7], [25]. In section 1.4, fig. 1.9 we saw the single cable design by Van Willigen use a simple transmit switch. The switch has an advantage of working in the absence of a power supply, which is beneficial from the single cable perspective.

A disadvantage of this switch is its incompatibility to pass bipolar signals, which would be an advantage for achieving an ultrasound probe with the capability of perform imaging with arbitrarily shaped wave-forms, which is the aim of this thesis.

In the single cable design, the transmit pulses are not accompanied by a DC supply voltage on the cable and thus the architecture used would have to work without the supply voltage and as the focus of this thesis is a bipolar signal capable ASIC, it should also be able to provide bi-directional isolation. As the implementation of a switch is possible in comparison to the high voltage pulsers from the single cable perspective, the focus was shifted to high voltage switches on the chip which would pass or block the signals.

The latching switch presented by Hara et. al is able to pass any arbitrary high voltages in the transmit phase [25]. This switch works with a low voltage supply which is provided only during the operation of the transmit and can thus limit the power dissipation. The switch can be seen in fig. 2.3

The transistors M5 and M6 can be considered as a bi-directional blocking circuit. A pulse on M5 turns on the switch while a pulse on M6 turns off the switch. M1 and M2 are the main transistors which pass the the high-voltage signal and are connected to boot-strapped capacitors which can be charged and discharged via the low voltage transistors M3 and M4.

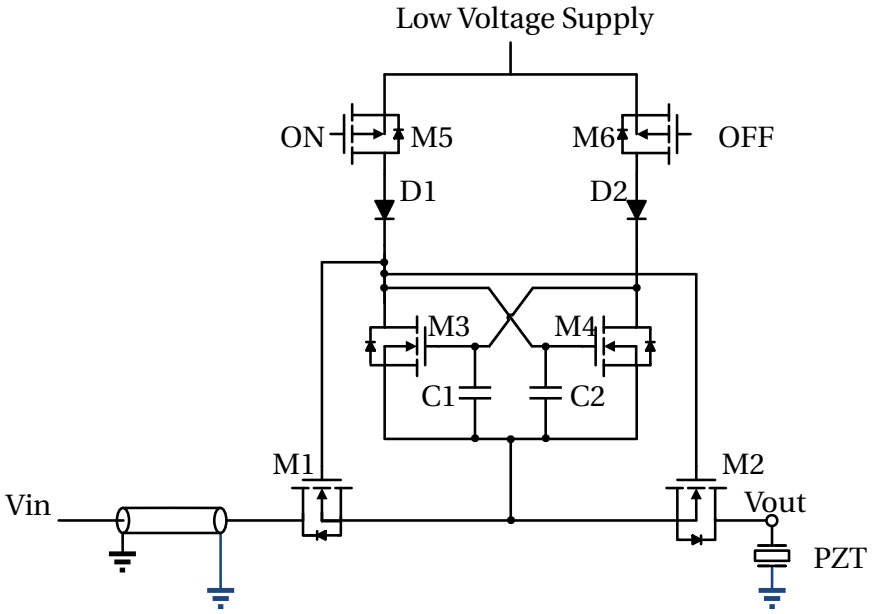


Figure 2.3: HV switch with bidirectional isolation [25]

Although this architecture is not directly compatible with a single cable design because there is no low-voltage supply provided on the cable during the transmit phase and similarly there are no extra cables which could provide the on-off signals for the switch. But, the advantage of passing arbitrary unipolar and bipolar wave-forms along with good bidirectional blocking capabilities make this switch a viable starting point for the transmit switch.

To be able to make this switch workable in the single-cable context, it needs to be provided with a low voltage power-supply and generation of on-chip control signals. A reservoir capacitor is used which supplies low-voltage supply voltage to the high-voltage transmit switch and also powers the digital blocks which provide the on-off pulses for operating the switch. The reservoir capacitor and the control signals generation for the transmit switch are discussed in more detail in the following chapter.

2.3. Substrate Biasing

In general, the substrate of the ASIC is connected to the most negative supply available. The reason for this is to prevent the forwards biasing of the source-bulk and drain-bulk junctions, which would lead to leakage of charge into the substrate and hamper the functioning of the circuit [26].

In the case of a bipolar signal capable ASIC the minimum voltage on the cable during the transmit phase and thus the transistors M1 and M2 in fig. 2.3 goes to $-25V$. Thus, the substrate needs to be kept at a potential lower than the lowest signal swing.

The solution is to use a negative peak detector circuit. A peak detector is a circuit which can be used to store the highest amplitude of the signal [27]. If we reverse the diode position

to the diode cathode facing the signal, then it would pass only the lowest amplitude of the signal. This was used to follow the signal on the cable to its lowest potential.

As there is only one cable connected to the chip, the substrate cannot be separately biased to a lower potential. Initially, the peak detector was directly connected to the cable to follow the low-peak of the transmit pulse train. But, due to the drop on the signal due to the diode and other circuit parasitics, the substrate potential would not sufficiently stay low, causing certain source/drain junctions with the substrate to get forward biased, which caused errors in the transmit signal received on the transducer element. Also, with the high-speed signal of 20MHz, the substrate would not be able to follow the signal equally fast. In the existing single cable design, the substrate was connected the ground potential as there were no signals below that being transmitted to the chip. Thus, no separate substrate charging phase was used.

The final implementation involves the addition of a separate substrate charging phase. A low voltage signal, lower than the transmit signal pulls down only the substrate, while not affecting the other circuitry on the chip.

The diode used here is the internal diode created from the N-Buried layer (NBL) and the P substrate. A cross-sectional view of the diode can be seen in fig. 2.4. The circuit was simulated with an assumed value of the substrate capacitance. The value was approximated from the drain-to-substrate capacitance of the high-voltage and low-voltage devices in simulation.

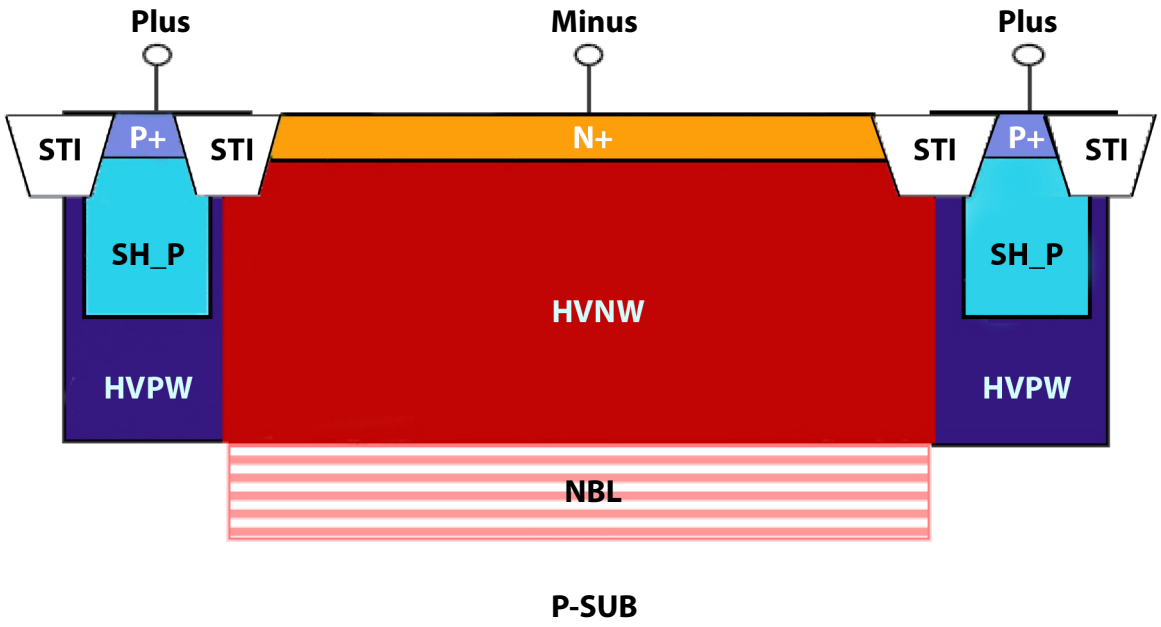


Figure 2.4: Simplified version of the NBL-PSUB Diode

As the transmit signal gets coupled with the substrate, the substrate biasing voltage was chosen to be sufficiently low, to prevent the substrate voltage in any case to rise higher than the lower peak of the transmit signals.

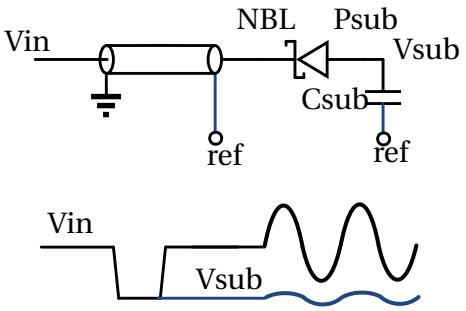


Figure 2.5: Negative peak detector with wave-forms

The negative peak detector circuit and the voltage on the substrate and the cable can be seen in fig. 2.5. Due to substrate coupling, a ripple is also created on the substrate during the transmit phase. To prevent the substrate voltage from rising above the lowest peak of the transmit signal, it is biased sufficiently lower during the substrate pre-charge phase.

2.4. Receive Circuitry

2.4.1. Separate Transmit and Receive Transducers

In Van Willigen's single cable design, the transmit elements and the receive elements are the same. Each element is connected to a transmit as well as receive switch which is enabled for the chosen elements for each transmit-receive cycle. The low-voltage receive switch is protected by a clamping circuit from the transmit switch, which uses a single NMOS transistor, and prevents the receive circuitry from facing the high voltages.

In the single cable design, from a bipolar signal perspective, this poses a problem. The same protection circuitry cannot be used as the signal swings below 0 V and would be faced by the low-voltage circuitry as well. To counter this problem, back to back switches were proposed, which would provide bi-directional isolation. The resulting circuitry in this case would be similar to the transmit switch topology chosen above and just protecting the low-voltage circuitry would consume chip area.

The final solution was to separate out the transmit and receive elements, thus eliminating the need for a clamping switch between the transmit and receive switches connected to the same element. This resulted in area reduction in the receive switch.
The receive circuitry kicks in after a delay when the transmit phase is over. As the receive transducers would be separate from the transmit transducers, they would not be connected by high voltage transistors and would only need to be protected from the high voltages. During the configuration phase, the receive element would be selected, for readout. The reflected acoustic waves excite the element and a low noise amplifier (LNA) would be used to read out the transducer.

2.4.2. LNA

This thesis uses the LNA, a current amplifier, as proposed in [7]. The ideal topology for the amplifier in the single cable design was found using Nullor, an ideal element which

has infinite gain and a zero-input voltage or current. The LNA is a current amplifier with a programmable gain and is connected to the receive element selected in the configuration phase as can be seen in fig. 2.6.

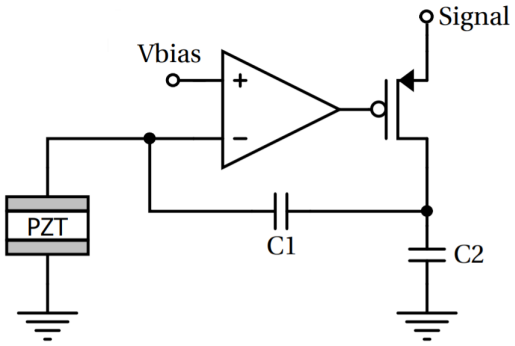


Figure 2.6: LNA block diagram [7]

The LNA has a capacitive feedback and the current gain equation is:

$$\frac{I_{out}}{I_{in}} = 1 + \frac{C_2}{C_1} \tag{2.1}$$

The capacitor C1 is programmable allowing two 6 dB gain steps, allowing gain of 34dB, 40dB and 46dB. It has an input noise level of $1\text{pA}/\sqrt{\text{Hz}}$ and a dynamic range of 74dB. The bandwidth of the amplifier is 30MHz but due to coaxial cable losses, the usable bandwidth is a little over 20MHz.

The LNA is designed to work on the DC supply of 3V during the receive phase and thus needs to be protected from the high-voltage bipolar signals on the cable during the transmit phase. The LNA and all the other low-voltage circuitry is safe due to the protection circuitry which will be discussed in the next chapter.

2.5. Communicating with the ASIC

With the chip connected to a single co-axial cable, it is impossible to select channels independently via control cables. To counter that, data is multiplexed on the supply line and the chip is pre-programmed to select the transmit and receive element for a particular transmit-receive cycle similar to [7] and the basic working was discussed in 1.4. The main changes made in the communication were the change in data bits for the transmit switch and the protection circuitry for the low voltage circuitry.

2.6. Overall ASIC structure

The block diagram in fig. 2.7 shows an overview of the system architecture. As can be seen below, the chip side has two sets of transducers, one set for receive and the other for transmit. Both set of transducers are connected by a short switch to the chip ground to isolate the elements when they are not selected. The control block defines the elements which would be selected for a particular TX-RX cycle.

The receive transducers are connected to the amplifier block, which in the receive phase amplifies the echo signals received and send it over to the system side for processing and image generation.

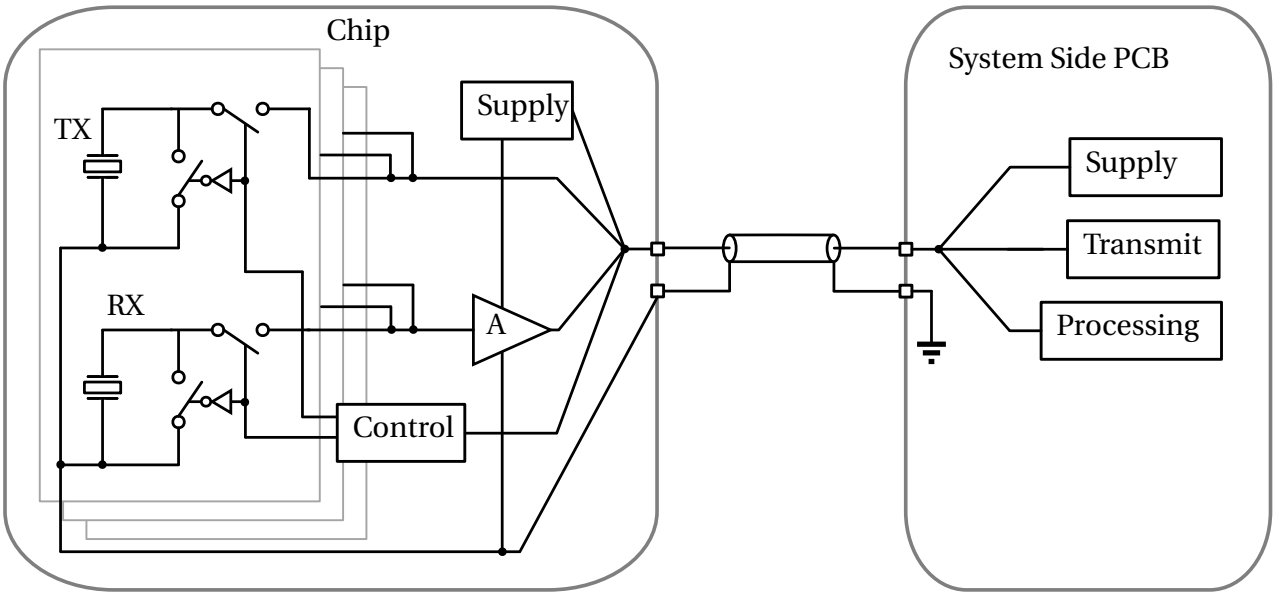


Figure 2.7: Block diagram of proposed ASIC

3

Circuit Designing

This chapter discusses primarily the transmit switch implementation. It talks about the transistors available in technology, the main switch, off-isolation considerations and the enabling and disabling of the switch. As the switch needs a supply voltage during the transmit phase, a reservoir capacitor is introduced and its implementations are discussed.

The next section talks about the protection circuitry which are important to keep the low-voltage transistors safe from the high-voltage pulses on chip. The chapter concludes with an overview of the complete ASIC.

3.1. Transmit Switch

3.1.1. Available High-Voltage Transistors in TSMC

The TSMC 180nm HV BCD technology offers various high and low voltage mosfets for designing the circuits including low voltage transistors which could be placed in high voltage n-wells. These transistors are available in 1.8V, 5V, 12V, 36V, 45V, 55V, 65V and 70V. The voltages of these transistors are defined by the difference of the $|V_d - V_{sub}|$ or the drain and substrate potentials.

Generally, in CMOS designs, NMOS switches are preferred as they have lower on-resistance due to higher mobility of carriers over PMOS switches of the same dimensions. The TSMC 180nm HV BCD technology offers GA and GB type devices in high voltages. The GA devices have their bulk and source tied to the substrate which cannot be used at higher potentials. The GB devices have an extra isolation ring which disconnects the bulk and the substrate of the transistor but at an added cost of bulky dimensions.

With the higher voltage capabilities, the area of the transistors also increases due to the isolation rings surrounding the transistor. As this work builds up on [7], the chip area remains the same. Larger number of transducers help in achieving better images, and each transducer is connected to a transmit switch making the switch sizing very crucial. Thus, it is important to choose the correct transistors for maximum area efficiency. For the target of a $\pm 25V$ amplitude signal and the substrate pre-charged to a potential $(-28V)$ lower than the lowest peak of the transmit signal, this work uses the 55V GB transistors.

3.1.2. Main Transmit Switch

The transmit switch is based on the bi-directional blocking switch as discussed in 2.2. The design methodology used for converting this switch can be seen as in fig. 3.1.

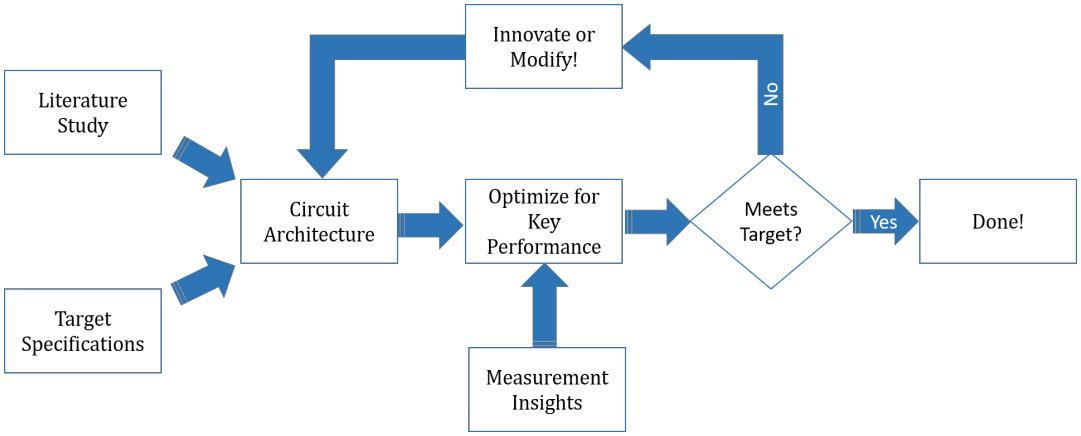


Figure 3.1: Design Methodology

After deciding the target specifications and conducting literature study, the most optimal circuit architecture was chosen to be the switch by [25]. The transmit switch designed by them was not directly usable in the single cable perspective and thus the circuit was redesigned for optimal sizing to operate with a reservoir capacitor rather than an off-chip

low-voltage supply. After a few iterations, the circuit was finally ready and met the targets.

Basic Implementation of a Bi-directional Isolation Switch

Figure 3.2 shows the basic implementation of a bi-directional isolation switch. The source terminal of the transistors M8 and M9 are tied together. The gate voltages of the main transistors are the same, thus when the gate voltage is high, the switch is on and when gate voltage is low, the transistors are off. The internal diodes of the main switch transistors can also be seen in fig. 3.2 and because of their arrangement, they are able to block bipolar signals with ease when no gate voltage exists.

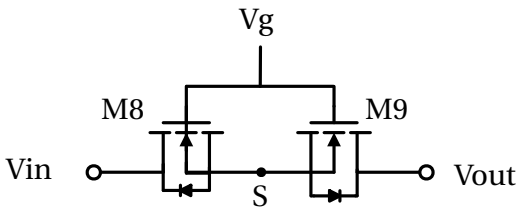


Figure 3.2: Simple bi-directional isolation switch

For a sinusoidal signal at the input, if no gate voltage is given, the signal reaching the point S is a rectified sine wave with only the negative peaks. When this faces the internal diode of the transistor M9, due to the diode arrangement, no signal passes to the output. The transistors available in the technology used are capable of passing high voltages, but they have a limitation of the maximum gate-source voltage which a transistor can operate in (5.5 V).

Implementation of the Transmit Switch

To implement the high-voltage switch, for passing arbitrary signal waveforms with a maximum amplitude of ±25 V, it is essential to maintain a gate-source voltage of less than 5.5 V. As seen in section 2.2, the base switch architecture is the design by Hara et al. [25].
As the low-voltage supply is provided by a reservoir capacitor as seen in fig. 3.3 which is charged after the configuration phase to 5V, charge distribution is the mechanism for charging the gates of M1 and M2. The charging circuit of the reservoir capacitor will be discussed in detail in 3.1.4.

The transistors M1 and M2 are the main switching transistors and implemented with 55V GB type NMOS transistors which were sized for low parasitic capacitance at the same time a low-on resistance. These devices can allow the ±25 V arbitrary transmit pulses to pass through them when they are on, from the cable to the selected piezo element, while providing bi-directional blocking due to the internal diodes of transistors M1 and M2, as understood from fig. 3.2.

Even though at first glance, the circuit looks symmetric, it is not. The gates of M1 and M2 are tied to the same node. The transistor M1 and M2 are sized the same for minimizing any signal attenuation. The gate–source voltage of the main switch transistors is kept floating by the bi-directional blocking circuitry comprising of transistors M5 and M6 while the level

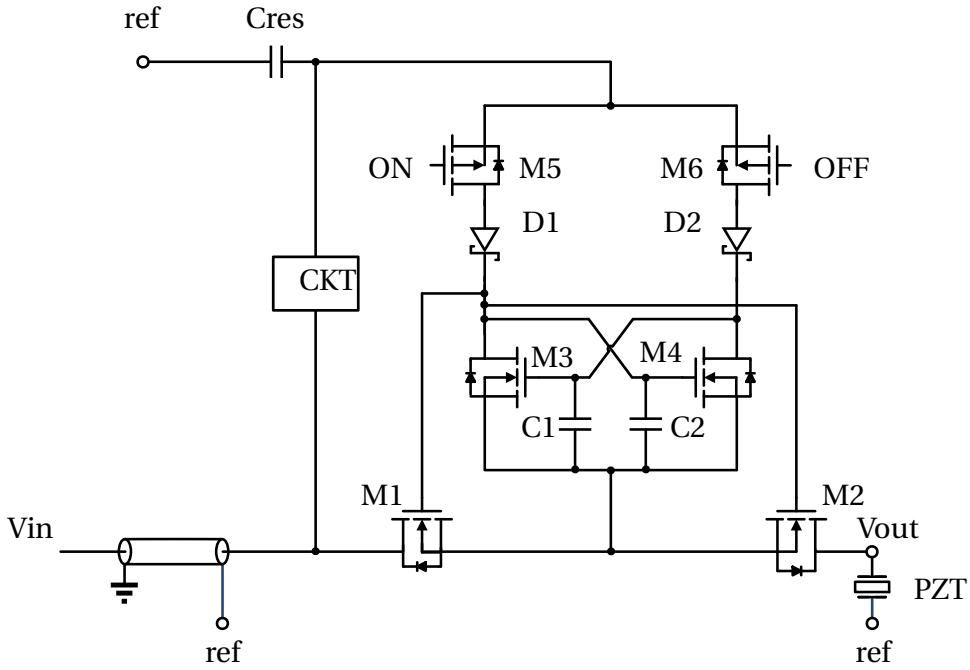


Figure 3.3: Addition of reservoir capacitor as low voltage supply

of the gate–source voltage is maintained by the latch circuit which comprises of the transistors M3 and M4.

When a low-voltage on pulse is given on M5, it turns on M4, which discharges the capacitor C1. This also provides a path for the low voltage supply to charge the gates of the main switch transistors M1 and M2 and the capacitor C2. Thus, enabling the switch to pass high voltage transmit signals.

For turning the switch off, a low-voltage off pulse is given on the transistor M6 which turns on the transistor M3, by charging capacitor C1 at it's gate and discharges the gates of M1 and M2 and the capacitor C2,thus disabling the transmit switch. The capacitors C2 and C1 are introduced to ensure stable gate – source voltages on the main switch transistors and M3 which would be able to discharge the gate voltages to turn off the switch. The capacitors C1 and C2 were implemented as MOM caps on-chip.

The transistors M5 and M6 are sized appropriately to have minimum on-resistance, at the same time ensuring low parasitic capacitances as there is no voltage source to power the switch, but a reservoir capacitor. In case the sizing is improper, the parasitic caps of the circuit could deplete the charge stored on the reservoir capacitor and critically affect the functioning of the switch.

The symmetry does not exist for transistors M3 and m4 as they drive different loads. While M4 is used to empty out the gate-source voltage of M3, for the off-state, M3 has to discharge the gate-source voltages of the transistors M1, M2 and M4. Thus, M3 was designed to be significantly larger than M4.

As the low voltage supply works on the principle of charge redistribution, the transistors M3 and M4 only see a low drain – source voltage ($V_{DS} < 5V$), even though their gate, drain and source nodes swing full with the input signal. This gave an option to use another type of transistor offered by TSMC, the low-voltage transistors in high-voltage N-wells.

The on-resistance of M3 and M4 with their respective capacitors C1 and C2 allowed for optimization in sizing for faster switching on and off of the transmit switch. But, the sizes of C1 and C2 also impact the swing of the V_{GS} on transistors M3 and M1-2 respectively which is designed to have sufficient headroom from their threshold voltages to avoid erroneous pulses hampering the switch operation.
Due to the latching circuit, the V_{GS} of the transistors M1 and M2 is less than 5V, but the gate node swings high in the transmit phase. Diodes D1 and D2 are introduced to act as another bi-directional isolation for the signal on this gate node to prevent the flow of charge into the reservoir capacitor or the low voltage supply.

Diodes in Transmit Switch

In TSMC 180nm HV BCD technology, diodes cannot be used in the forward biased condition. The only options available are diode connected NPN BJTs and Schottky Barrier Diodes. These two come with their own limitations.

The diode connected NPN BJT's in the technology do not allow a drop of more than $|12V|$. This is a big limitation in the case of a circuit which faces much higher voltage swings. An option proposed to counter that was stacking of multiple NPN BJTs to divide the voltage drop equally across them. This resulted in large parasitics affecting the charge redistribution for the low-voltage supply of the transmit switch. This option was thus not suitable.

The other option was to use the Schottky barrier diode (SBD). The only limitations with this diode in the used technology is that it has not been modelled properly for a forward voltage greater than $0.6V$. It needs to follow eq. (3.1). The equation states that the current flowing through the substrate node should be less than 1% of the current passing through the anode at $125°C$.

$$\frac{I_{sub}}{I_{anode}} \leq 1\% \tag{3.1}$$

3.1.3. Off-Isolation Improvement

The transmit switch designed was able to pass the high-voltage bipolar signals. The switch was supposed to provide high bi-directional isolation when it is in the off-state. But, due to parasitic coupling, the off-isolation was lower than the targeted off-isolation of 40dB. To improve the off-isolation of the transmit switch, new circuit implementations were tested which would prevent the signal from reaching the transducer element and generating unwanted acoustic transmissions.

Implementation 1

The first approach was to add a bi-directional isolation switch from the middle node of the transistors M1 and M2 and provide a path to the substrate in the off-state and can be seen

in fig. 3.4.

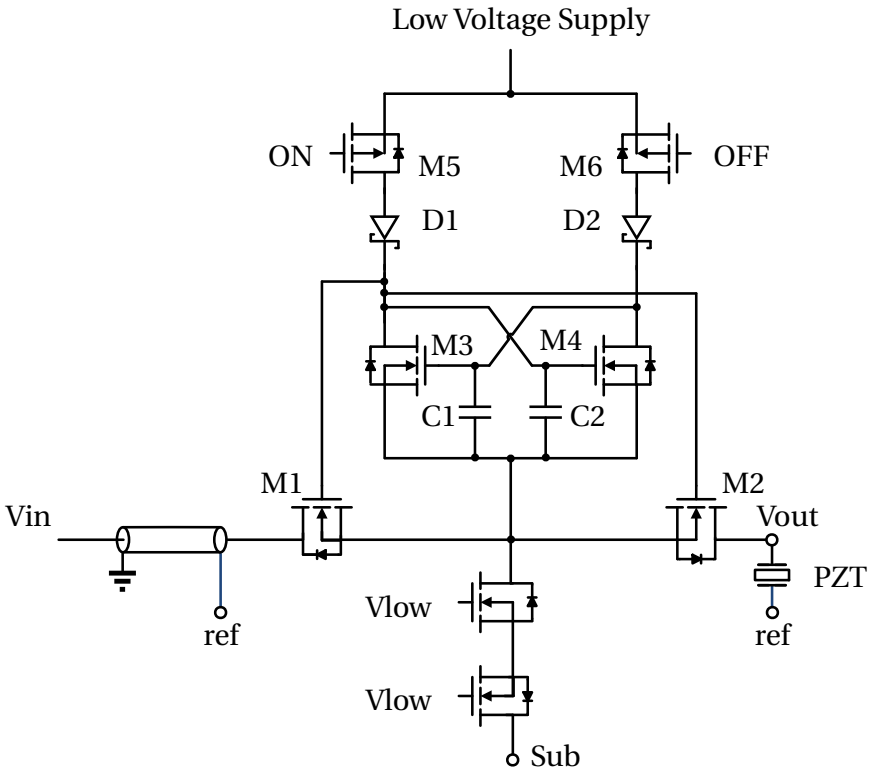


Figure 3.4: Implementation of the short switch from the mid-point

The isolation switch would turn on when the transmit switch is in the off-state. When the transmit switch is off, due to the internal diodes of the high-voltage transistor M1, the mid-point will only swing below 0V. The issue with this switch is the level-shifter circuit needed similar to the one designed in the transmit switch and needs to provide a gate voltage relative to the substrate, which is at -28V.

Implementation 2

The second approach was to use a circuit similar to the transmit switch designed above, with its input node connected to the transducer and its output connected to the chip ground. This switch is referred to as the short-circuit switch as can be seen in fig. 3.5.

The short-circuit switch can be designed with smaller C11 and C12 values compared to the main transmit switch as it does not directly face the high voltage transmit signals. Also, the short-circuit switch can function with the same on and off pulses as used in transmit switch but at the opposite transistors.

During the transmit phase, the transmit switch is on, while the the short switch is off, allowing the transducer to get excited by the train of high voltage pulses. In case a transmit element is not selected during the transmit phase, the transmit switch is off and the short-circuit switch shorts the transducer to the chip ground, thus preventing any transmit signal on the cable from reaching the transducer. The addition of a short-circuit switch improved the off-isolation capabilities of the transmit switch to 50dB at 20 MHz.

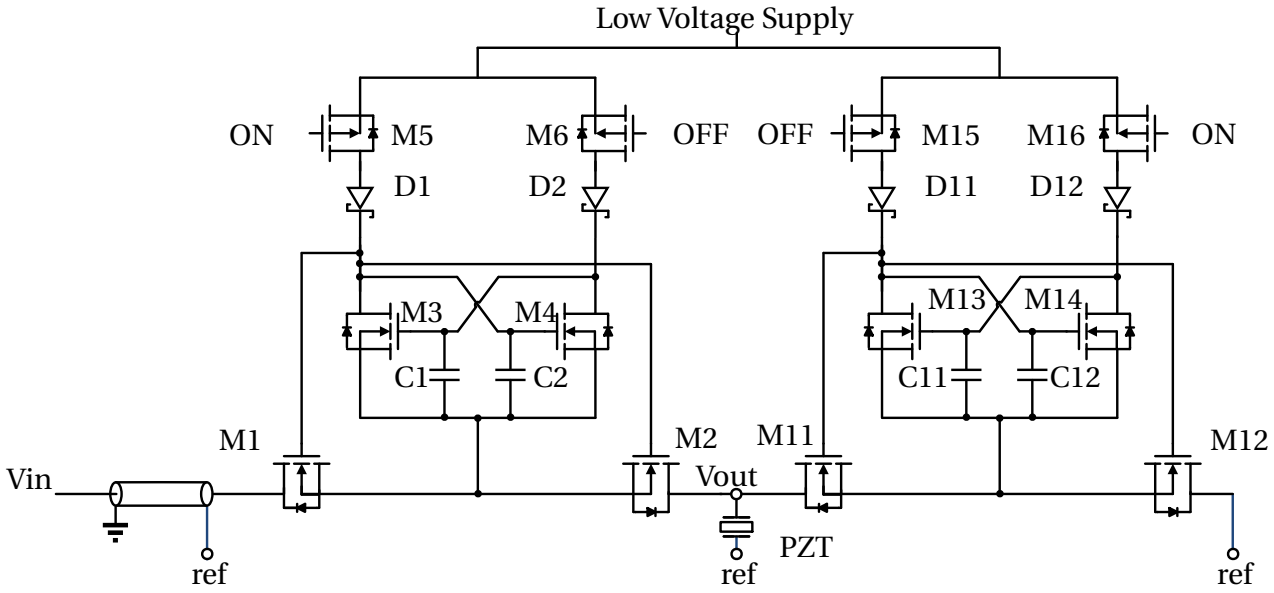


Figure 3.5: Implementation of the short-circuit switch to the transducer

3.1.4. Reservoir Capacitor

For the transmit phase to take place on the cable without an active power supply, it is essential to have a low voltage supply to power the transmit circuit. This supply is provided by the reservoir capacitor (C_{RES}), which gets charged immediately after the configuration phase. The timing diagram overview can be seen as below in fig. 3.6. A shows the start-up phase for the chip, B show the configuration phase while C shows the capacitor charging phase. During the configuration phase, the cable has $500mV$ data modulated on the 3V supply, while the reservoir capacitor is charged when the cable voltage goes to 5V.

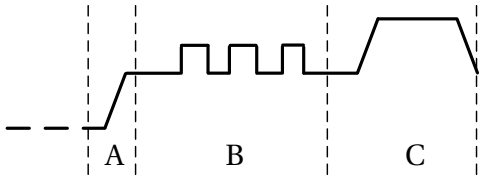


Figure 3.6: Voltage signal on the cable

The reservoir capacitor (C_{RES}) was sized relative to the capacitors C1 and C2 and took into account the transistor and SBD parasitics. When the transmit switch is given the pulse to turn on, M5 provides a path which connects C_{RES} to C1 and charge redistribution takes place between them. Apart from C1, the parasitic capacitances in this path also get charged. The charge redistribution leads to a drop in the voltage on C_{RES}, but with proper sizing, voltage across the reservoir can be sufficiently higher than the threshold of transistors M6 and M3 so that it can also provide sufficient voltage to C2 after the charge redistribution during the off state. The values of C1 and C2 of the main switch were finalized at 3.6pF and 4.8pF respectively, while the reservoir capacitor was sized at 22pF.

As the reservoir capacitor is much larger in size, it was implemented using a MIM cap. Various architectures were simulated for charging the reservoir capacitor, as it is supposed

to connect to the cable only during the phase when it is charging and then disconnect from the cable to provide the low voltage supply for the entire transmit switch.

Implementation 1

The first circuit implementation, fig. 3.7 is connected to the cable via a Schottky Barrier Diode (SBD) which prevents the capacitor from seeing the high negative pulses during the transmit phase and an NMOS which clamps the voltage to the enable signal voltage and charges the capacitor to a value lower than the enable signal by the threshold of the NMOS.

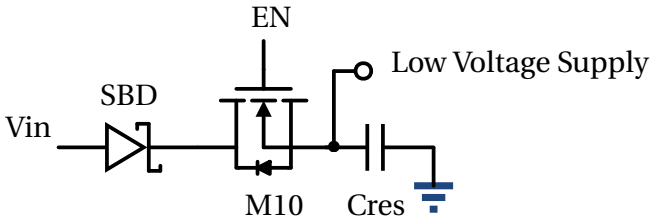


Figure 3.7: Reservoir capacitor charging circuit implementation 1

This circuit though easy to implement, requires the enable signal to be sent from the system side during the configuration phase. For the capacitor to be charged to 5V, the enable signal should be higher than 5V, which would need an amplification of that bit, even before the 5V supply is made available on the chip via a level-shifting circuit, which complicates the designing of the overall charging circuit.

Implementation 2

The second implementation, which was finally used, involves a more sophisticated circuit, shown in fig. 3.8, which could work even with a lower voltage enable bit.

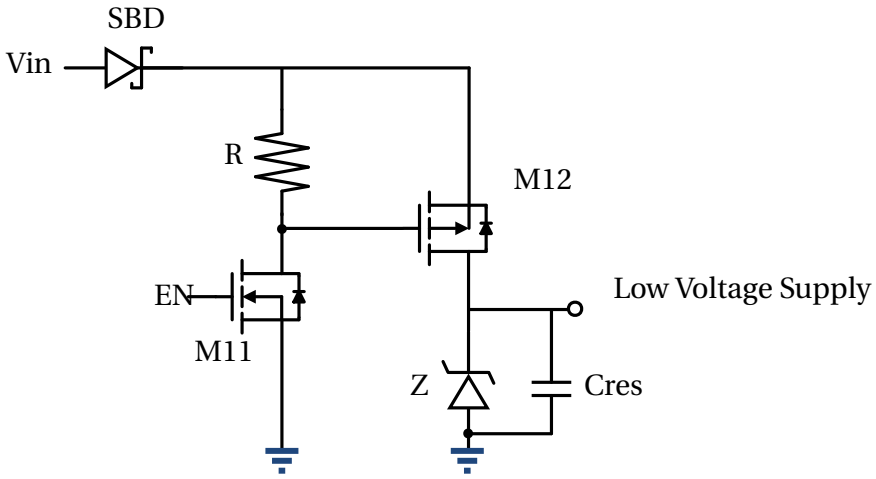


Figure 3.8: Charging circuit implementation 2

Similar to the first implementation, the circuit is connected to the cable by a SBD. The signal is then split into two branches. The first branch includes a resistance and an NMOS

M11, which is connected by the enable bit in its gate and the second branch is connected to a PMOS M12 and then the reservoir capacitor in parallel to a Zener Diode.

The charging circuit is enabled after the configuration phase. A high enable bit turns on M11 and pulls down the gate of M12, turning it on and subsequently charging the reservoir capacitor. When the enable bit goes low, M2 shuts off, creating a high impedance path looking from the drain and the voltage on the cable finds a lower impedance path to the gate and the source of M12. This cuts-off M12 and prevents the reservoir capacitor from facing any other signals on the cable.

Issues

In comparison to having an ideal supply voltage, the reservoir capacitor can only provide fixed charge. As it works on the principal of charge-redistribution, the charge depletes with every time the switch is turned on or off after sharing with C1 and C2.

The SBD diodes were introduced to act with the internal diodes of the high voltage transistors M5 and M6 fig. 3.3 to act as bi-directional isolation and prevent the signal swing reaching the reservoir capacitor. But, as the reservoir capacitor charge depletes, the internal diode of M5 and M6 gets forward biased, which leads to charge being transferred to the reservoir capacitor and a drop in the gate-source voltages.

As the transmit pulse lasts for a very short time, the drop on the gate-source voltages is minimum. The charge which is now added to the reservoir capacitor, although unwanted, helps in recycling charge and thus the reservoir capacitor is able to provide the low-voltage supply effectively.

3.1.5. Enabling and Disabling the Transmit Switch

The reservoir capacitor introduced above also provides supply to the circuitry which generates the pulses for enabling and disabling the transmit switch. During the configuration phase, an enable bit is sent out for whichever transmit transducer would be selected. This enable bit and the pulse generated on-chip pass through a logic AND gate, which feeds to the on and off terminals of the transmit switch.

Although there are multiple transmit elements, with only the reservoir capacitor providing the low-voltage supply, only a single element can be turned on in one TX-RX cycle. This limitation could be countered by having a larger reservoir capacitor, but it would reduce the number of transmit elements altogether as a larger capacitor would occupy more area on-chip.

The turning on and off of the entire transmit switch is critical to the proper working of the ASIC, thus it was needed to make sure the signals were generated at the right instances.

Implementation

The enable-disable signal implementation in fig. 3.9 is similar to the clock recovery circuit used by [7]. A small capacitor (100fF) is charged when the PMOS is on and is discharged by a weak current source. The Schmitt Trigger generates square pulses relative to its threshold

voltages which are designed for optimal pulse width of the enable and disable signal of the transmit switch. These when passed through the logic AND gate with the enabling bit, pass the on or off signal to the chosen transmit switch

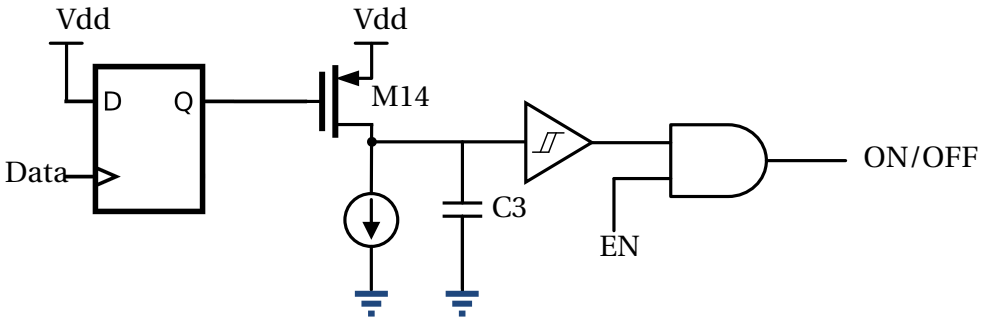


Figure 3.9: On Off pulse generation circuit

Two different pulse generators with the same input signal but operating at a time gap of a few µs are used, one for the on signal and the other for the off signal. This time gap is variable and can be programmed based on the time period of the transmit phase of a particular ultrasound imaging technique. This allows the chip to be used for various imaging modes with different transmit pulse trains. One pulse generator is used to enable the transmit switch, while the other is used to disable it.

3.1.6. Size Comparison with Van Willigen's Transmit and Receive Switch

Although the layout was not implemented for the ASIC, a first pass on the rough size for the transmit switch was calculated. All the transmit switches are connected by the same reservoir capacitor for their low-voltage supply.

Willigen implemented his ASIC with 64 transducer elements in transmit and receive. Each transmit switch has an area of roughly $7300\mu m^2$. The switch designed in this thesis supports bipolar pulses and provides a good bi-directional isolation, but it comes at the cost of area.

Also, with the receive and transmit transducers being separate in this thesis, the protection circuitry needed for the low-voltage receive circuitry can be removed, providing with an area advantage of $4000\mu m^2$ per element.

The transmit switch size for this thesis is roughly $54,000\mu m^2$ per switch and thus reduces the number of switches which could be implemented on the same size ASIC. From unitary method, for a first pass, we can conclude that for 64 receive elements, the number of transmit elements which can be used on this chip are 13.4, which means 13 transmit transducer elements connected to a bipolar signal capable high-voltage switch.

With proper layout of the chip, the number of transmit elements could be increased to 16 with 64 elements in the receive phase. These number of channels for transmit and receive are sufficient for a good resolution image as was shown in [14].

3.2. Peripheral Circuits

The section discusses the various other circuits which were designed in this thesis for its optimal working including the protection circuitry.

3.2.1. Protection Circuitry

As discussed earlier, the low-voltage circuitry on chip needs to be protected from the high-voltage bipolar signals on the cable during the transmit phase and also the substrate-charging phase. The protection circuit implemented here is a modification of the one used in [7]. To block the high-negative voltages on the cable, a Schottky Barrier Diode (SBD) is used to allow the protection circuitry to only see the positive swing on the cable. The fig. 3.10 shows a clamp designed using an NMOS voltage limiter which clamps the voltage to an acceptable low voltage which goes as high as the V_{clamp}.

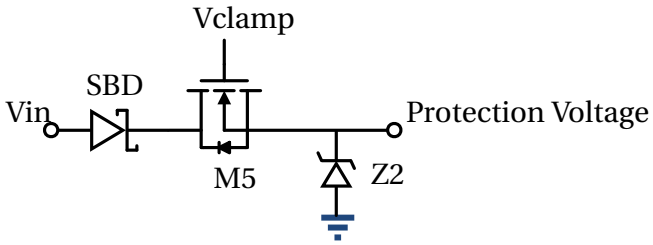


Figure 3.10: Clamping Circuit

In the case of only a single SBD, the current flowing through it is high and 3.1 was not being satisfied. A turnaround to this problem was to increase the multiplier for the SBD, which resulted in a larger area occupied by the diode in layout, but as there is only one clamping circuit, it was acceptable.

3.2.2. Clamping Voltage Generator

For the protection circuitry in the previous section, the circuit needs a V_{clamp} generator. Taking cues from the design in [7], a circuit, fig. 3.11, was designed which would block the negative voltage signals faced in the substrate charging phase and the transmit bipolar signals. This circuit also faced the same issue of 3.1 not being satisfied with a single transistor and required a higher multiplication for the SBD.

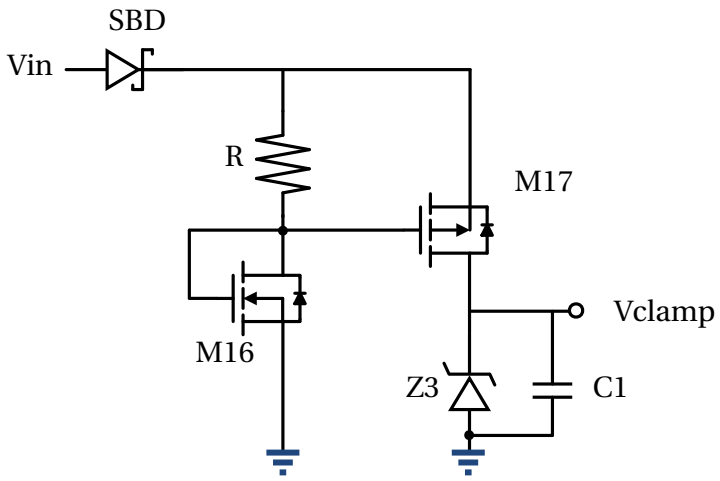


Figure 3.11: Clamping Voltage Generator Circuit

The circuit after blocking the negative voltages, creates a reference voltage for the gate of the transistor M17. This voltage rises sufficiently only when the transmit phase takes place and creates a low voltage V_{clamp}, which is stored on the capacitor C1.

3.3. Entire ASIC

The circuits which are directly used from Willigen's work and not mentioned in this thesis are as below [7]:

- Data recovery circuit
- Clock generation circuit
- Receuve Multiplexer
- LNA
- Bit Error Checking
- Receive-Mode startup
- ESD Protection

These circuits would have been impacted by the bipolar high voltage signals, but due to the protection circuitry, their low-voltage devices would work fine.

This work was tested without the receive phase. In the case of the full circuit implementation, the overall block diagram is shown in fig. 3.12.

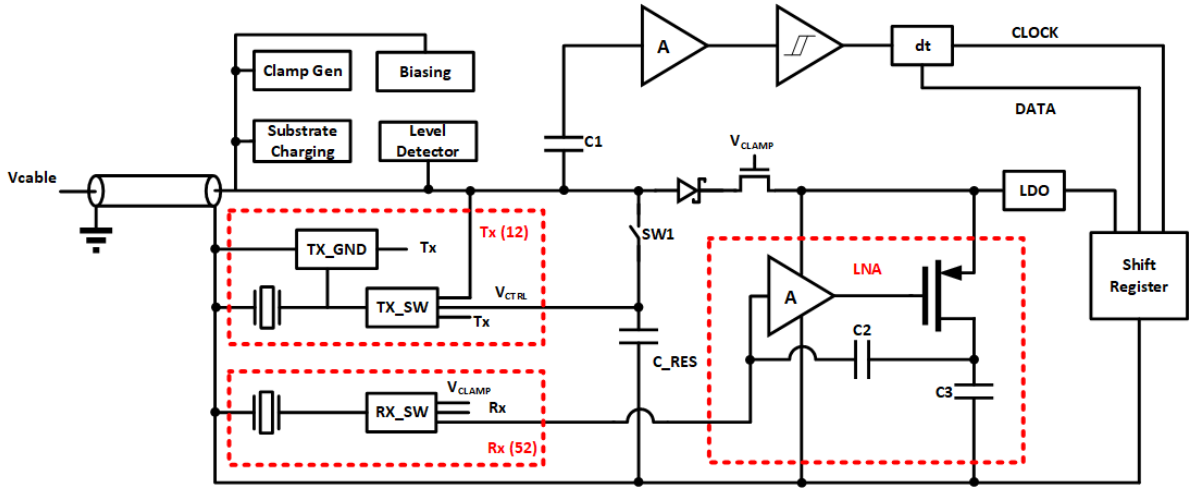


Figure 3.12: Block diagram of the entire ASIC

4

Circuit Simulation

This chapter shows the various simulations which have been performed to verify the functionality of the transmit switch. These include the control signals, the waveforms observed at the piezo element at various frequencies, the off-isolation of the switch and its AC response. Apart from this, waveforms of peripheral circuits - substrate charging and clamping circuit are also discussed.

4.1. Control Signals

The transmit switch in fig. 3.5 is enabled or disabled by sending an on and off signal pulse respectively. Figure 4.1 shows a block diagram of the complete transmit switch. The transistors M1 and M2 are basically the pass transistors and transistor M3 is referred to as the discharge transistor. On receiving an off-pulse, M3 discharges the charge at the gates of the pass transistors and thus disabling the switch from operation and the short switch connects the piezo element to the ASIC ground.

As can be seen in fig. 4.2, the cycle is started by an on signal which allows the transfer of charge to the gates of the main switch transistors M1 and M2. The high-voltage transmit pulse is passed after the switch is enabled. This is followed by the off signal which disables the switch and shorts the piezo element to the chip ground.

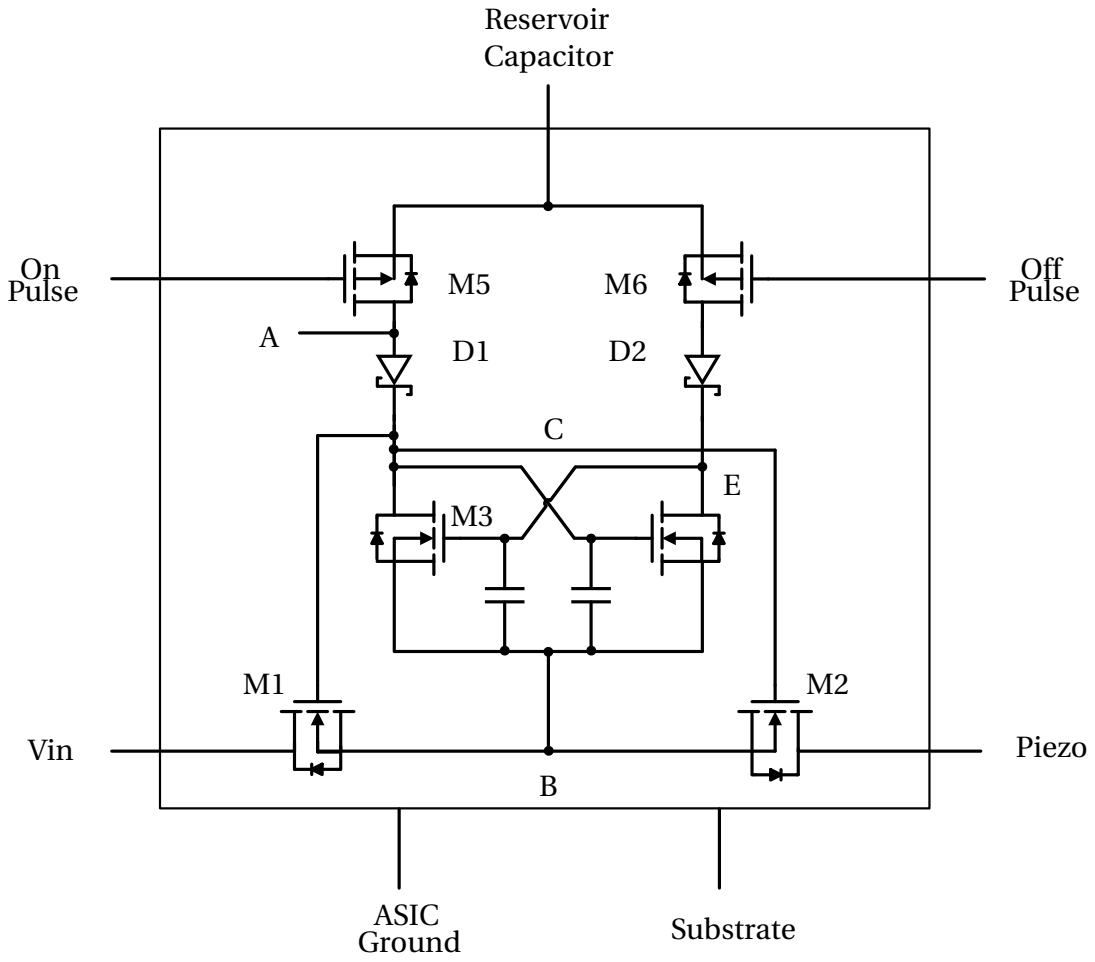


Figure 4.1: Transmit Switch Block Diagram

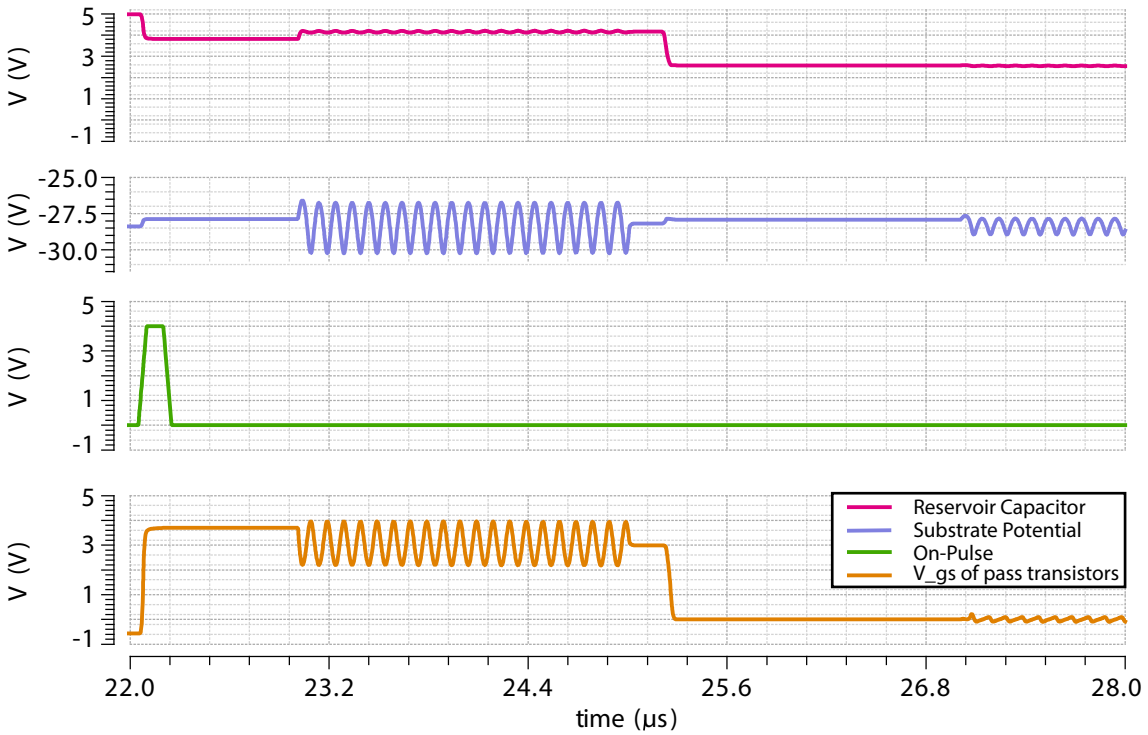
Figure 4.2 shows the various signals involved in the transmit switch operation. Sub-figure 4.2(a) shows the voltage across the reservoir capacitor, the substrate potential, on-pulse and the $|V_{GS}|$ of the pass transistors. As can be seen from the figure, charge redistribution takes place after the on-pulse is sent to the switch and the potential across the capacitor goes down.

When the pass transistors are on, the transmit signal on the cable is passed over to the piezo element. If observed carefully, the voltage across the reservoir capacitor rises during the transmit phase. This happens because the node A rises higher than the reservoir capacitor voltage and forward biases the internal diode of M5. This is essentially charge harvesting as the charge on the gates of the pass transistors came from the reservoir capacitor.

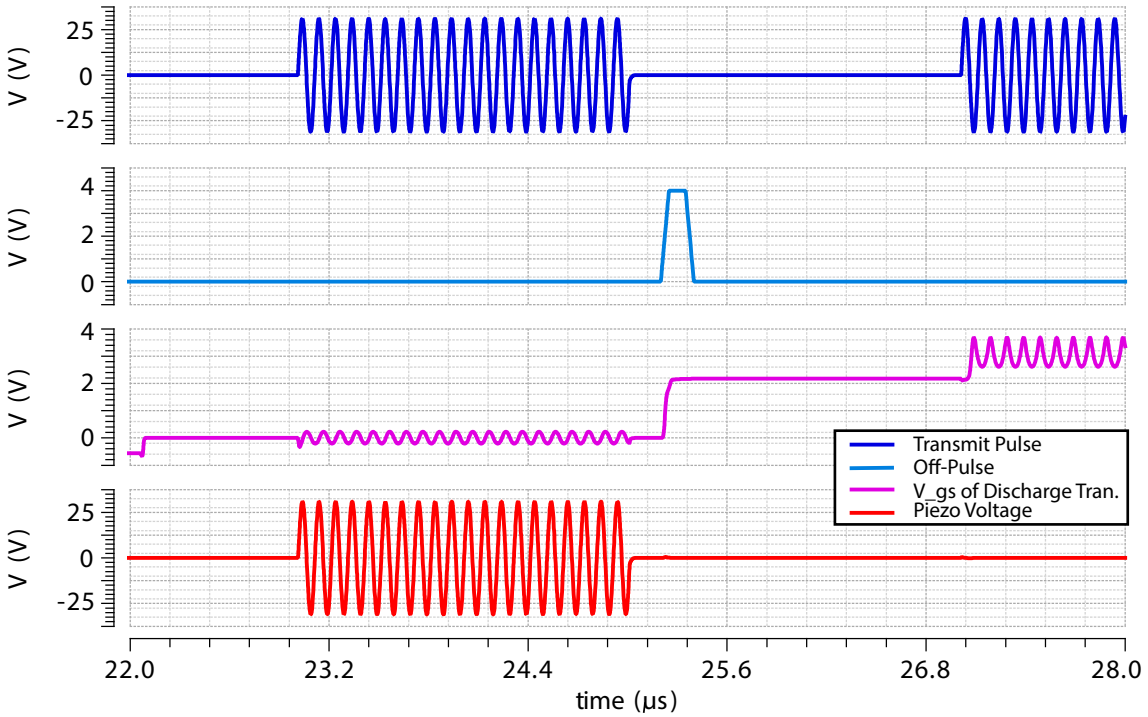
When an off-pulse is given to the transmit switch, the transistor M3, which was initially off, now gets gate charge and empties the gates of the pass-transistors. The short switch also activates then and connects the element to the ground. As can be seen in 4.2(b), when the switch is turned off, no signal is observed at the piezo element.

Also, we can see that the substrate gets coupled with the fast transmit signal and swings, but pre-charging it to a lower potential has the advantage of it not rising above the lowest peak of the transmit pulse.

The simulations shown in fig. 4.2 were carried out for a transmit pulse of amplitude $\pm 25\,\mathrm{V}$ and frequency of 10 MHz.



(a)



(b)

Figure 4.2: Transmit switch in operation

4.2. Transmit Waveforms

The switch was simulated for the ASIC without the receive part being included and performed as expected. Figures 4.3, 4.4 and 4.5 show the transmit waveforms for a sine wave input of $\pm 25V$ at 2 MHz, 10 MHz and 20 MHz respectively. At lower frequencies, the output at the piezo element follows the input signal very closely.

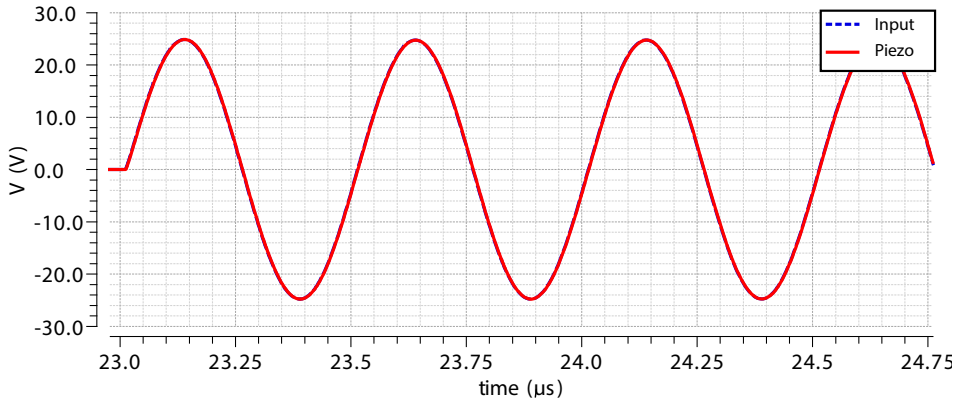


Figure 4.3: Input vs Piezo voltage at 2 MHz

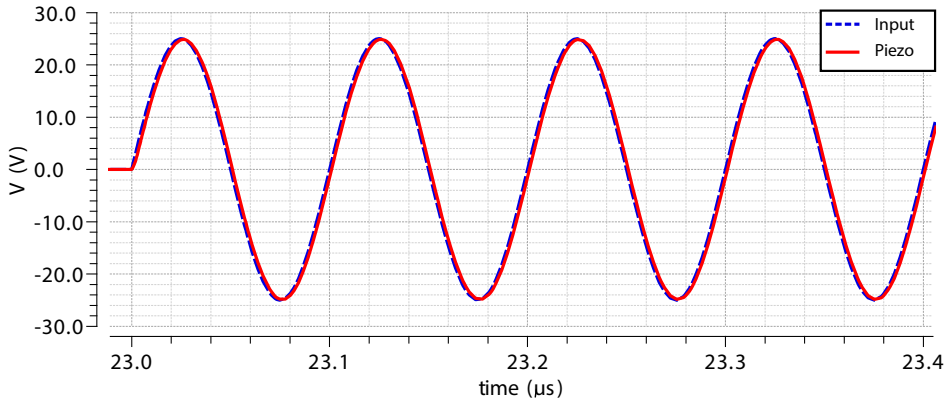


Figure 4.4: Input vs Piezo voltage at 10 MHz

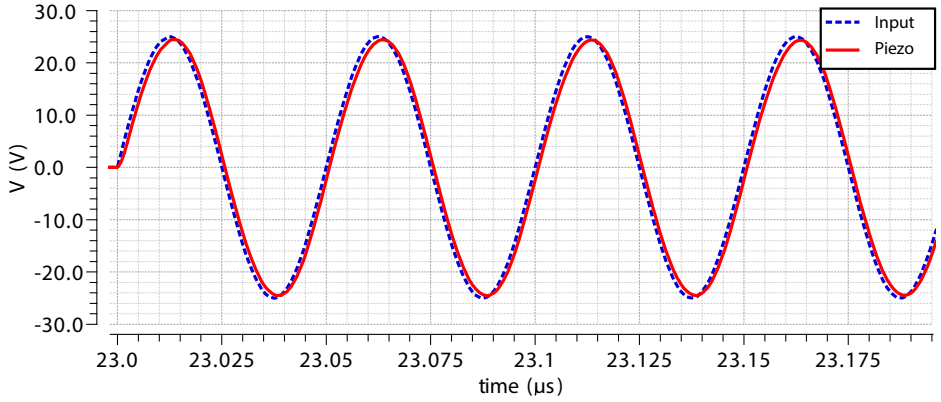


Figure 4.5: Input vs Piezo voltage at 20 MHz

4.3. Off-Isolation

When a particular transmit element is not selected, the switch is designed to provide sufficient off-isolation to prevent a non-selected piezo element from generating false images due to excitation. The figures 4.6 to 4.11 show the transient responses in absolute and logarithmic scales to show the off-isolation capabilities of the designed transmit pulse.

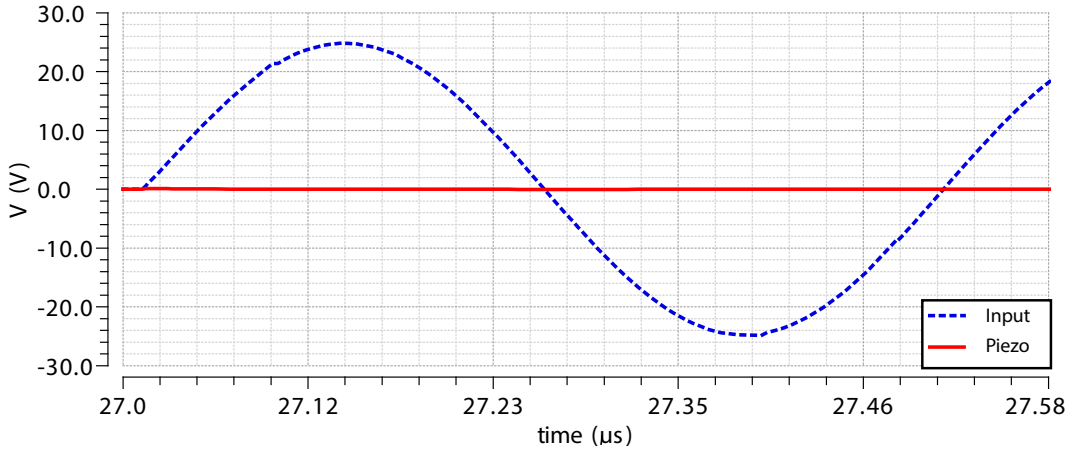


Figure 4.6: Off Isolation transient at 2 MHz

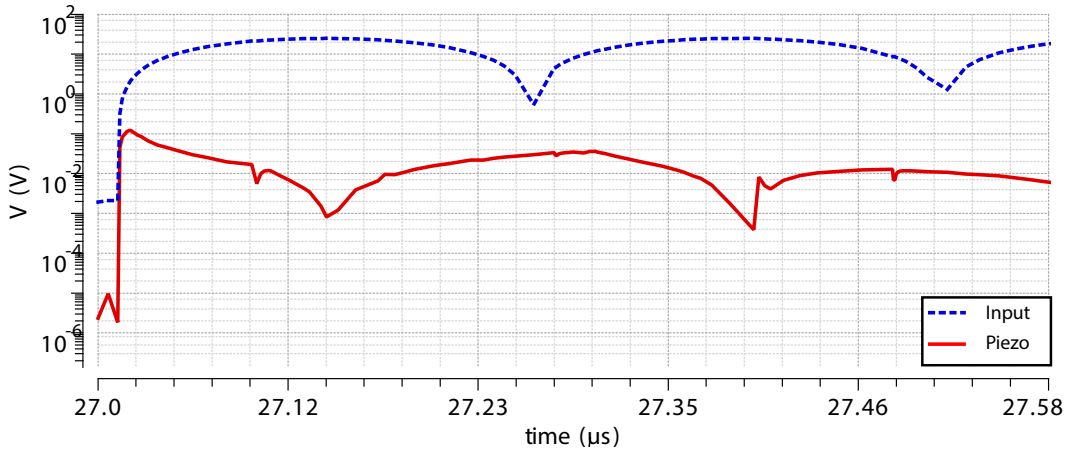


Figure 4.7: Off Isolation in log-scale at 2 MHz

The first positive edge signal in the off-state is higher in amplitude (around 400 mV) as compared to the next set of pulses (around 50 mV) as the switch settles. For the switch in off-state, when the transmit pulse is applied, the first spike is an anomaly as it charges the parasitic capacitances of the switch, and leads to a higher output on the piezo element. After this, the switch settles and the off-isolation for the pulses thereafter is much higher.

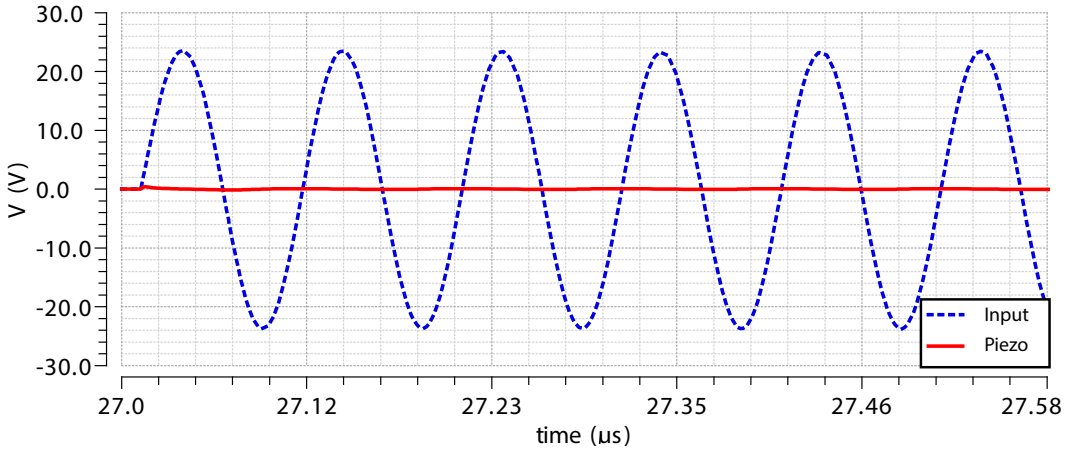


Figure 4.8: Off Isolation transient at 10 MHz

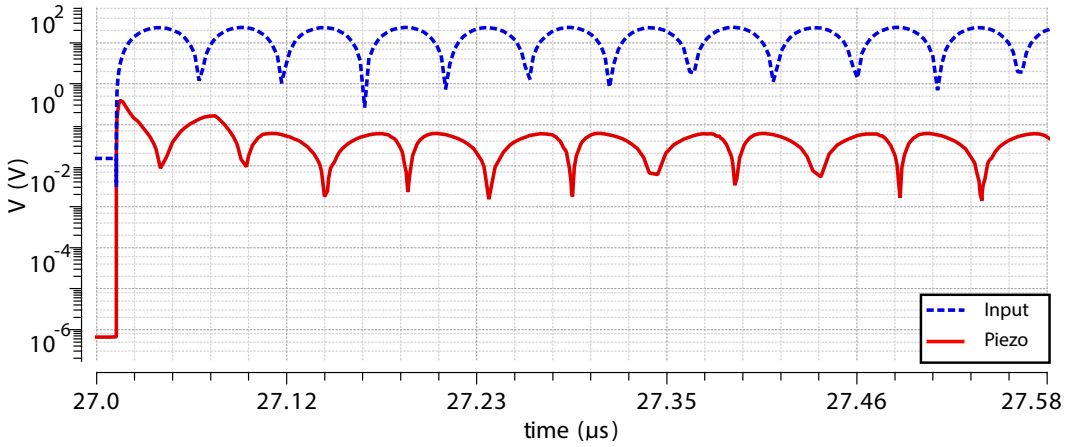


Figure 4.9: Off Isolation in log-scale at 10 MHz

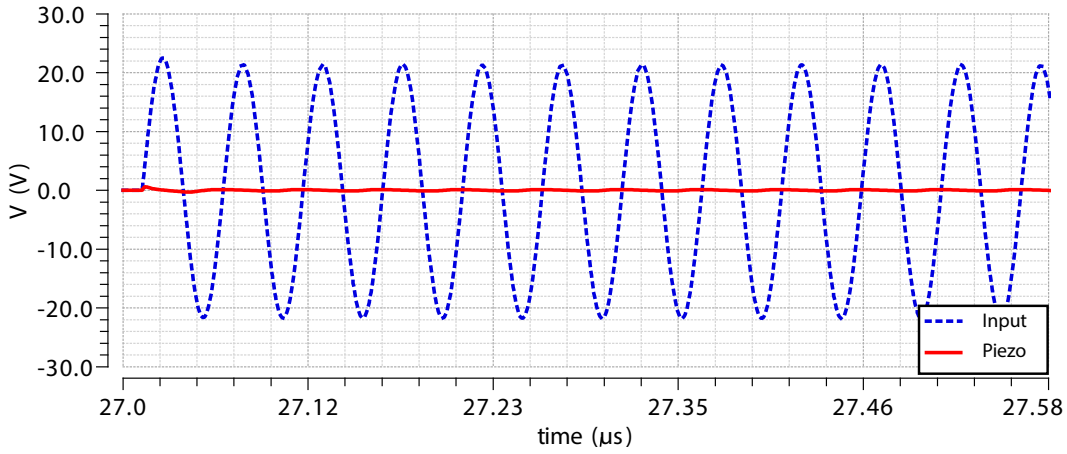


Figure 4.10: Off Isolation transient at 20 MHz

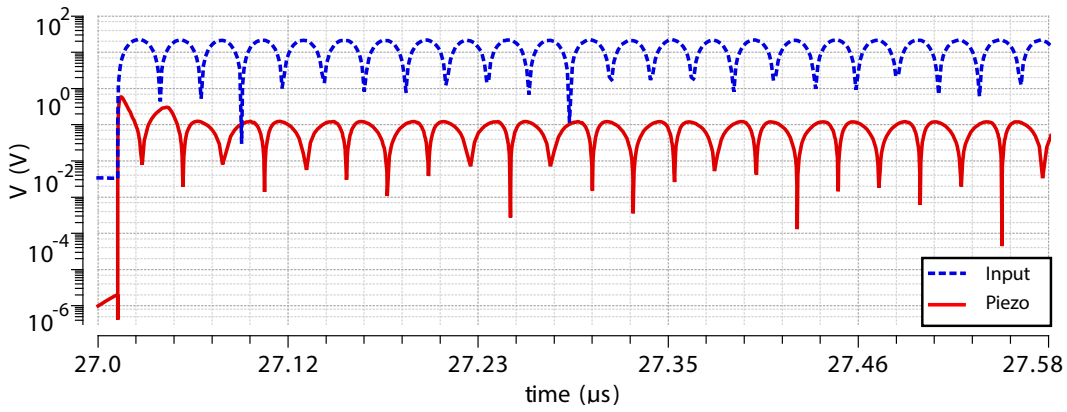


Figure 4.11: Off Isolation in log-scale at 20 MHz

Figure 4.12 shows the variation between the transmit pulse signal frequency and the off-isolation observed. Due to the attenuation caused by the co-axial cable, the signal amplitude drops with the increase in frequency. This is accompanied by a loss in the transmit switch off-isolation. Overall, in the frequency range of 2 MHz to 20 MHz, the transmit switch provides good off-isolation on settling.

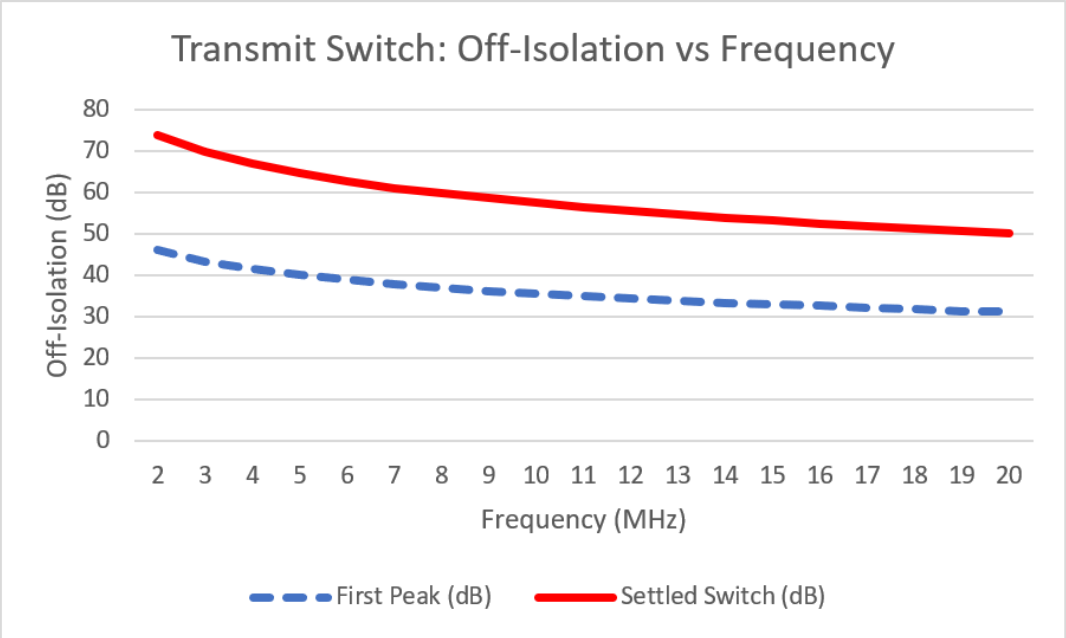


Figure 4.12: Transmit Switch: Off-Isolation vs Frequency

4.4. AC Response of transmit Switch

During intra-vascular imaging, for each TX-RX cycle, a transmit signal could range from a few pulses to around 10 pulses based on the imaging scheme applied. The switch should be designed to have a low on-resistance to allow the full signal swing for a wide range of frequencies. Lowering the on-resistance means increasing the size of the pass-transistors and thus increasing their parasitic capacitances. Proper designing for both resistance and capacitance would allow the switch to operate in a wide frequency range while maintaining signal integrity.

Figure 4.13 shows the simulation of AC response of the transmit switch output on the piezo element compared to the input signal received on-chip over a frequency range. As can be seen, the 3dB frequency of the switch is around 75 MHz, which is larger than the 3 dB bandwidth of the coaxial cable. Thus, the switch is not a limiting factor for fast transmit pulses.

The phase shift between the input and piezo voltages increases with frequency. The shift would not be very critical from a design perspective as the acoustic signals are generated by the transducer only after they receive the transmit pulse. On excitation, the received echo signals would arrive even later.

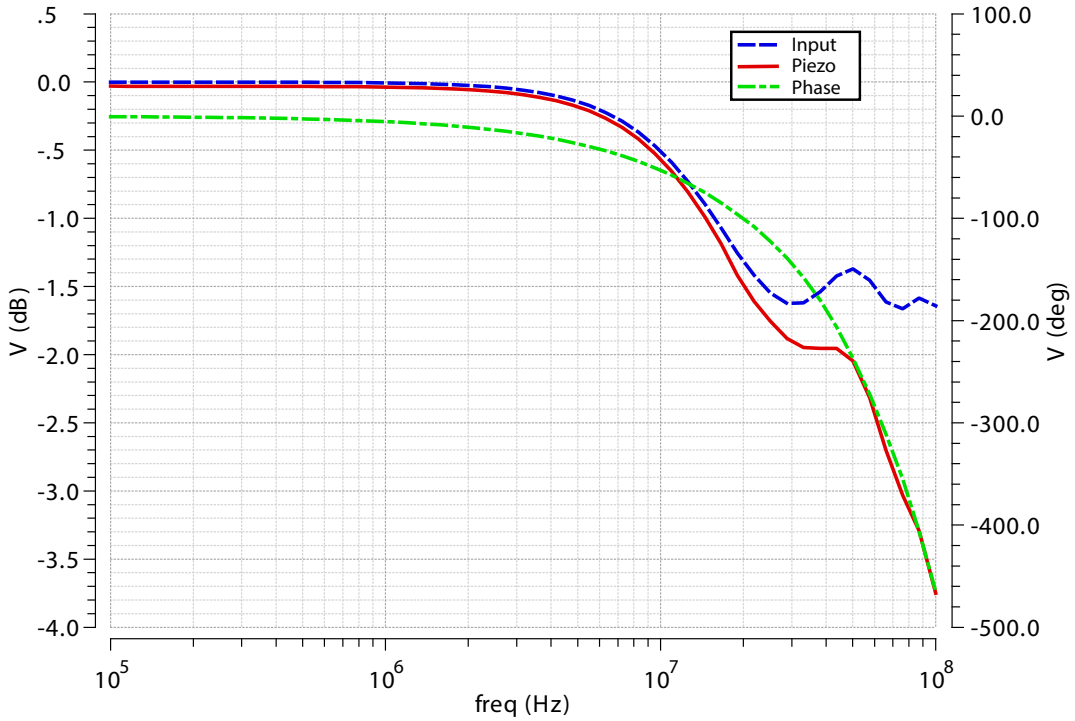


Figure 4.13: AC response of the transmit switch

4.5. Substrate Charging

Figure 4.14 shows the voltage on the cable dropping to a lower potential before the transmit phase. Coupling can be observed when the signal on the cable changes drastically, reducing the negative potential to which the substrate is biased to. Two major events seen here are the rising of cable voltage back to 0 V and the transmit phase. Despite the coupling, the circuit in fig. 2.5 ensures the substrate voltage does not rise above the lowest peak of the transmit phase.

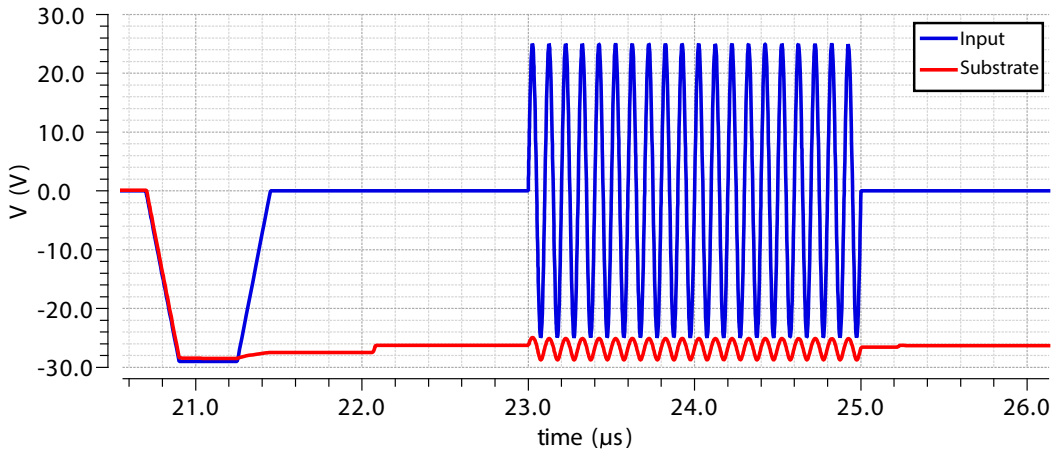


Figure 4.14: Substrate biasing vs input signal on the cable

As discussed earlier, it is essential for the substrate to be pre-charged to a lower potential before a transmit waveform to prevent the source-bulk and drain-bulk junctions of the high-voltage NMOS transistors from forward biasing.

4.6. Transmit Switch Power

The power dissipation of the transmit switch on the chip side can be discussed as two cases. Firstly, the power dissipated in turning on or off the switch. While the second is the power dissipated while the switch is in operation with a high-voltage transmit signal passing over it.

In the first case, the power is dissipated by the transistors M5 and M6 (refer fig. 4.1) which enable and disable the transmit switch. They are provided the low-voltage supply on-chip by the reservoir capacitor and dissipate 4.9 μ W each. When the transmit switch is turned on and a high-voltage transmit signal is passed over the cable, the pass-transistors M1 and M2 dissipate power. Figure 4.15 shows the input and piezo element voltages as well as the current through the pass-transistors for an input signal of ±25 V with a frequency of 10 MHz. This is the second case and 5.8 mW of power is dissipated in simulations while the switch is actively passing the high-voltage signal.

Another addition to the first case is the power dissipated by the latching transistors M3 and M4. When a switch is turned off from the on-state, M3 (discharge transistor) discharges the gates of the pass-transistors and dissipates a power of . Turning the switch from the off-state to on-state involves M4 discharging the gate of the discharge transistor M3. Here, M4 dissipates a total power of 0.71 mW.

Thus, the total power dissipated in turning on-off one transmit switch equals 1.2 mW, while the switch dissipates 5.8 mW due to the high-voltage transmit signals passing over the cable. Another way to look at the power dissipation of the switch is from the Energy perspective as none of the signals last for a long time. For example, the transmit signal could be from a few cycles to around 10 cycles and the time duration would depend on the signal frequency, thus varying the energy consumption.

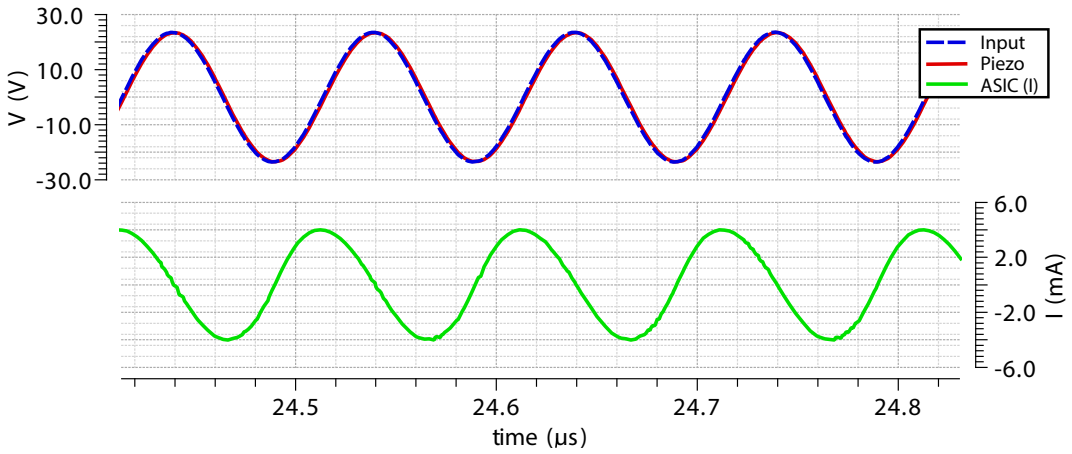


Figure 4.15: Chip side voltage and current of a single piezo element

4.7. Clamp Voltage Generation

The protection circuitry in fig. 3.10 needs a clamping voltage, which is generated by the circuit in fig. 3.11. Figure 4.16 shows generation of V_{clamp} with respect to the input signal on the cable once the transmit phase starts. V_{clamp} rises to around 5.5 V and thus prevents the receive circuitry from facing voltages higher than that.

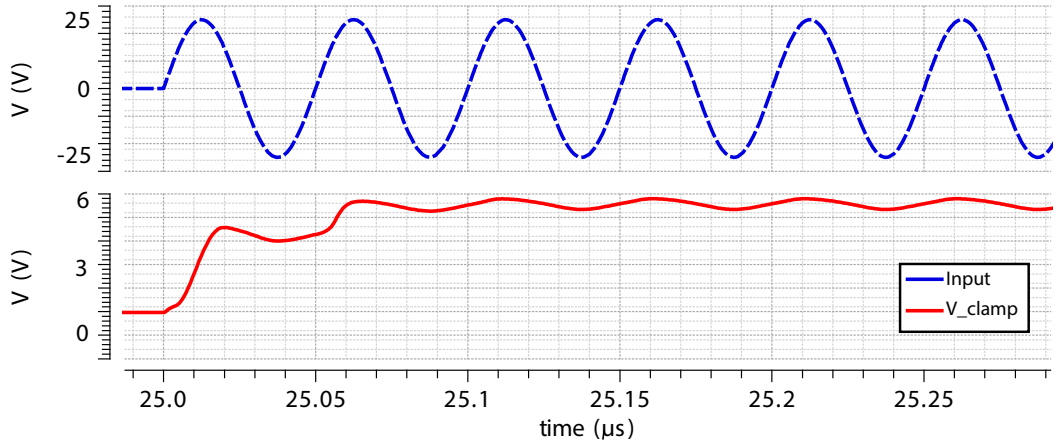


Figure 4.16: Clamping voltage waveform

5

Conclusions and Future Work

5.1. Conclusions

The aim of this thesis was to design an ASIC which is capable of transmitting high-voltage bipolar signals for single-cable intra-vascular ultrasound imaging. The circuit designed has 16 transmit and 64 receive piezoelectric transducers for generating and receiving acoustic waves.

The biggest achievement of this thesis was to make the design capable of transmitting arbitrary signals of peak value up to ±25 V with a frequency range from 2MHz to 20MHz. The lower frequency range is useful for achieving greater depth penetration at the cost of spatial resolution. The higher end of the frequency range helps in attaining a high spatial resolution but depth penetration is limited in that range. The simulations proved the switch could also be implemented in other ultrasound imaging schemes apart from intra-vascular imaging.

The transmit switch provides a high off-isolation, which would allow it to be used for various ultrasound imaging modes as well as permit the ASIC to be hooked up with any imaging system.

Although the circuit has not fully been integrated, on completion it would be the first front-end ASIC which is capable of transmitting bipolar high-voltage signal as well as providing receive functionality on a single cable to a large number of transducers. Table 5.1 shows the specs achieved by the transmit switch in the single cable design.
The key takeaways from this thesis are as follows:

- If transducers are used for both transmit and receive mode for bipolar high-voltage signals, bi-directional isolation needs to be provided between the high-voltage transmit and low-voltage receive circuitry.
- Due to the enabling and disabling transistors being on only momentarily, the power consumption while transitioning from an on to off or vice-versa state is minimal.
- The off-isolation of a transmit switch is crucial to prevent it from creating unwanted acoustic transmissions and be able to provide at least 40 dB off-isolation. In this work,

Table 5.1: Performance of the Transmit Switch

	This Work
Technology	0.18μm
# Coax Cables	1
Switching Power (TX)	1.2mW
Dynamic Power (TX)	5.8mW
Bandwidth (TX)	75 MHz
TX Channels	16
TX Voltage	±25 V
TX Switch Area	54.000 μm^2

though a higher off-isolation was achieved, it came at the cost of area, which reduced the number of transmit switches possible on the given chip.

- The 3 dB bandwidth of the switch is 75 MHz, which is much larger than the 3 dB bandwidth of the coaxial cable or the receive circuitry used in [7]. Thus, the transmit switch is not a limiting factor for the signal bandwidth.

On integration with the receive mode circuitry, the specs of the chip would be expected as in the table 5.2.

Table 5.2: Prior art and performance of this work

	[12]	[13]	[14]	[15]	This Work
Technology	0.18μm	0.35μm	0.18μm	0.18μm	0.18μm
# Coax Cables	1	13	4	1	1
Power (RX)	13.2mW	20mW	10mW	6.4mW	–
Bandwidth*	20 MHz	40 MHz	16 MHz	24 MHz	24 MHz
RX Channels	1	56	64	64	64
TX Channels	–	64	16	64	16
TX Voltage	–	25 V	26 V	30 V	±25 V

*Bandwidth with respect to receive mode

5.2. Future Work

As the main goal of this work was to work on the transmit part of the existing single cable design and making it bipolar signal compatible, there are multiple blocks which can still be improved upon to improve the overall performance.
The various tasks which could be performed in the future are as follows:

- The transmit switch is currently used for ±25V using the 55 V transistors. This can be increased by using the 70 V transistors to be able to pass around ±33V signals without changing the technology.

- Acoustic imaging can also be performed at slightly lower voltages of around ±15V which results in a peak voltage of 30 V, thus allowing the use of 36 V transistors in the

technology used, which would allow the reduction of area of a transmit switch and thus increase the number of transmit transducers, while keeping a large number of receive transducers for better image resolution.

- The use of regular diodes in forward biased conditions is not permitted in TSMC 180nm HV BCD technology. The only exceptions are diode connected NPN BJTs which allow a mere maximum of |12 V| across them and Schottky Barrier Diodes (SBD), which are not properly modelled in Cadence beyond a forward voltage of 0.6 V. This can be countered by better modelling the SBDs. The other method is to shift to a different fabrication process like X-FAB as used in [25] where high voltage diodes can be used in forward biased application.
- The depletion mode NMOS could be used instead of the enhancement mode NMOS for the reservoir capacitor charging circuit to simplify the designing.
- Complete integration of the chip with the receive circuitry, layout and tape-out for testing in real world conditions and ascertain the working.

This ASIC helps in moving a step forward to reducing the cable count to a minimum of one for intra-vascular ultrasound imaging using high-voltage arbitrary unipolar or bipolar signals.

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