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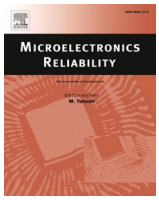

Research Paper

# Characteristics and avalanche investigation of SiC VDMOSFETs with enhanced P-Based implantation

Houcai Luo [a], Jingping Zhang [a], Huan Wu [a], Bofeng Zheng [a], Xiao Wang [a], Kai Zheng [a], Guo-Qi Zhang [b], Xianping Chen [a,*]

[a] College of Optoelectronic Engineering, Chongqing University, 400044 Chongqing, China
[b] Institute of Microsystems and Nanoelectronics, Delft University of Technology, Delft 2628 CD, Netherlands

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ABSTRACT

Two P-Based depth of SiC VDMOSFETs (group A and B) are designed and manufactured by enhanced P-Based implantation. The group A with lower P-based depth has a better static properties, while group B has a higher high frequency switching performance. Further, the avalanche reliability and failure mechanism for two groups are investigated by UIS experiment and TCAD simulation. The results show that the high temperature is generated by energy dissipation during avalanche and it drives the parasitic BJT conduction, causing $I_{ds}$ out of control and instantaneous heat concentration in a very short time. Significantly, high P-Based depth exhibits higher UIS reliability due to smaller $R_b$ and more difficult to active parasitic BJT.

## 1. Introduction

Silicon carbide metal-oxide-semiconductor field-effect transistors (SiC MOSFETs) is a promising candidate to replace silicon-based insulated gate bipolar transistors (Si IGBTs) in power electronics due to their high switching frequency, low power dissipation, high thermal conductivity, and high current density [1]. SiC MOSFETs exhibit outstanding properties due to the characteristics of SiC material wider band gap, higher thermal conductivity, and larger critical electric field strength compared to Si [2]. Due to these exceptional advantages, SiC MOSFETs have significant potential in power systems such as electric vehicles, charging stations and photovoltaic inverters [3]. Over the past years, advances in design and manufacturing technology have led to the commercialization of SiC MOSFETs in the power electronics market [4].

There are two main technology directions in SiC MOSFETs, distinguished by differences in their gate electrode structure: planar gate structure (simplified SiC VDMOSFETs) and trench gate structure (simplified SiC UMOSFETs). Compared to SiC VDMOSFETs, SiC UMOSFETs have higher power density and lower ON-resistance. However, the SiC UMOSFETs are less robust in the blocking state due to the higher electric field withstood by the trench gate oxide [5]. SiC VDMOSFETs remain the most mainstream silicon carbide power devices. Reducing the JFET region width ($L_{JFET}$) substantially decreases the gate oxide electric field in SiC VDMOSFETs [6]. However, this will also rapidly increase the specific on-resistance ($R_{on,sp}$) of the device [7]. Increasing the depth of the P-Base ($T_{P\text{-}Based}$) can also reduce the electric field strength of the gate oxide during avalanche breakdown, in comparing with decreasing the $L_{JFET}$, the $R_{on,sp}$ increases only slightly [8]. The $T_{P\text{-}Based}$ geometric parameter is critical in balancing the conduction characteristics and reliability of SiC VDMOSFETs.

Although the SiC MOSFETs have better performance than the Si IGBTs in some aspects, the reliability of the SiC MOSFETs is still a critical issue in the power system [9]. Inductive loads are widely used in uninterruptible power supply systems, electric vehicles, inverters and other fields [10]. Due to the very fast switching speed of SiC MOSFETs, it means that SiC MOSFETs need to withstand a high current change rate, that is, the di/dt is large. Large di/dt is easy to lead the device operate under avalanche conditions due to very high induced electromotive force in the circuit. During avalanche breakdown, the energy stored in the inductor will be released as heat, which will greatly increase failure risk of SiC MOSFET. Numerous studies have investigated reliability and failure mechanisms of SiC MOSFETs under conditions of avalanche, such as channel activation, parasitic BJT turn-on, and melting of surface electrodes metal [11,12]. Although there is a significant amount of research on avalanche failure, a lack of research on improving the reliability of SiC MOSFETs under avalanche conditions. Additionally, most research has only been conducted through theoretical simulations, with very few reports on practical experiments.

* Corresponding author.
*E-mail address:* xianpingchen@cqu.edu.cn (X. Chen).

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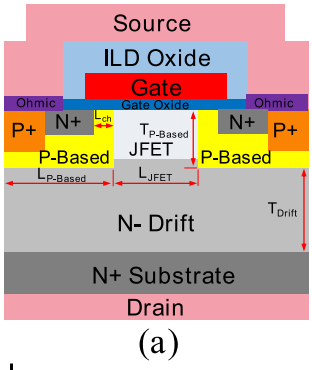
In this study, two SiC VDMOSFETs with different P-Based region depths were designed and fabricated on 6-in. FAB with enhanced P-Based implantation. The static and dynamic characteristics of SiC VDMOSFETs are investigated. Besides, the avalanche reliability and failure mechanism are compared and analyzed. This research provides guidance to engineers in developing silicon carbide devices.

## 2. Device structure and fabrication

Fig. 1 (a) shows the cell structure of the designed 1.2 kV SiC VDMOSFET. Fig. 1 (b) presents the key parameters of SiC VDMOSFETs, including geometric and doping parameters. $N_{Drift}$ represents drift region doping concentration. $T_{Drift}$ is thickness of drift region. $L_{ch}$ is channel length, generated by self-alignment technology. $T_{GOX}$ represents the thickness of gate oxygen layer. The width of the JFET region ($L_{JFET}$) is critical to $R_{on,sp}$, and its value is 1.6 μm in order to reduce the electric field and leakage current of gate oxide during blocking. The width of the P-Base region ($L_{P\text{-}Based}$) is 3.2 μm, indicating a pitch of 8.0 μm in designed SiC VDMOSFETs. The P-Based doping concentration ($N_{P\text{-}Based}$) and depth ($T_{P\text{-}Based}$) have a significant impact on device characteristics [8,13]. In this study, two different $T_{P\text{-}Based}$ are achieved by controlling ion implanting energy, divided into two groups: A and B. In order to achieve the same threshold characteristics for both designs, the dose of low energy injection is adjusted by P-Based implantation. Further, Fig. 1 (c) illustrates the key process stages involved in the fabrication of SiC VDMOSFETs. Initially, the wafer is cleaned, followed by etching of aligned marks. Ion implantation is performed in the P+ source region and P-Based region. Then, N+ source ion implantation is employed to form 0.5 μm channel by using a self-aligned process. Additionally, slight N-type implantation is executed to enhance the dopant concentration in the JFET and to adjust the threshold voltage. Following this, gate oxide is formed through thermal oxidation, and the wafer is annealed in a NO atmosphere in order to reduce $SiC/SiO_2$ defects. Polysilicon is then deposited and etched to produce the gate electrode. An isolated oxide layer is subsequently formed on the polysilicon to protect the gate structure, and then it is etched between the gate and source. Finally, the source ohmic contact is established via rapid thermal annealing. To create source and gate pads, a 4 μm thick AlSiCu layer is deposited. Nitride and polymide deposition, as passivation, are utilized to protect the chip termination, and front-side processing is finished. The SiC wafer is then thinned from 350 μm to 180 μm. Laser annealing is used to activate the ohmic contact, and backside metallization for the drain electrode is deposited, signaling the end of the fabrication process. After production, they are packed into TO 247–3.



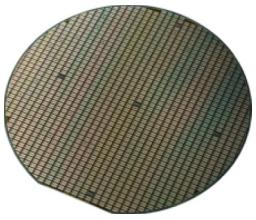

(a)

| Key Parameters | Value |
|---|---|
| $N_{Drift}$ | $8\times 10^{15}$ cm$^{-3}$ |
| $T_{Drift}$ | 11 μm |
| $L_{ch}$ | 0.5 μm |
| $T_{GOX}$ | 50 nm |
| $L_{JFET}$ | 1.6 μm |
| $L_{P\text{-}Based}$ | 3.2 μm |
| $N_{P\text{-}Based}$ (Group A) | 100 keV / 2 × $10^{12}$ cm$^{-3}$<br>200 keV / 5 × $10^{12}$ cm$^{-3}$<br>320 keV / 5 × $10^{12}$ cm$^{-3}$<br>400 keV / 5 × $10^{12}$ cm$^{-3}$ |
| $N_{P\text{-}Based}$ (Group B) | 120 keV / 3 × $10^{12}$ cm$^{-3}$<br>220 keV / 8 × $10^{12}$ cm$^{-3}$<br>500 keV / 6 × $10^{12}$ cm$^{-3}$<br>700 keV / 5 × $10^{12}$ cm$^{-3}$ |

(b)

- Align mark etching
- P+ implantation
- P-Based implantation
- N+ implantation
- JFET implantation
- Annealing
- Gate oxide growth
- Polysilicon deposition & etching
- ILD oxide deposition & etching
- Gate & source contact
- Passivation
- Backside metalization

(c)



(d)

**Fig. 1.** The SiC VDMOSFETs with (a) cell structure, (b) key geometry and doping parameters, (c) fabricating process stages, and (d) fabricated 6-in. wafer.

## 3. Device characterization

Table 1 summarizes the experimental test results for comparing the static and dynamic characteristics of group A and B. In order to further illustrate the differences static performance between group A and B, the blocking voltage (BV), threshold voltages ($V_{th}$), specific on-state resistance ($R_{on,sp}$)of group A and B in both room temperature (25 °C) and high temperatures (175 °C) are tested. At 25 °C and 175 °C, the BV capacity of group A and B are able to meet the requirements of 1200 V when $I_{ds}$ = 100 μA. The $V_{th}$ of group A and B are nearly identical due to nearly similar doping concentration in channel region. The $V_{th}$ of group A is about 3.21 V under condition of $V_{ds}$ = 10 V, $I_{ds}$ = 5 mA, and the $V_{th}$ of group B is 3.22 V at 25 °C, while they are 2.10 V and 2.12 V respectively, under condition of 175 °C. Because of larger JFET resistance in group B, there is a larger $R_{on,sp}$ in group B compared with group A. The $R_{on,sp}$ of group A is lower than that in group B at 25 °C and 175 °C. Notably, the third quadrant characteristic is investigated. Under condition of $I_{sd}$ = 5 A, the $V_{sd}$ are 2.60 V and 2.83 V, respectively, in group A and B. Due to larger $T_{P\text{-}Based}$, there is a wider area of PN junction in group B compared with group A. All the static characteristics of group A and B are shown in Fig. 2.

Further, dynamic properties for group A and B are also exhibited in Table 1. And the reverse transfer capacitance versus drain voltage ($C_{rss}$ - $V_{ds}$), output capacitance versus drain voltage ($C_{oss}$ - $V_{ds}$), input capacitance versus drain voltage ($C_{iss}$ - $V_{ds}$), drain to source capacitance versus drain voltage ($C_{ds}$ - $V_{ds}$), gate to source capacitance versus drain voltage ($C_{gs}$ - $V_{ds}$), and gate to source voltage versus gate charge ($Q_g$ - $V_{gs}$) characteristics are shown in Fig. 3. As shown in Fig. 3 (a), under condition of $V_{ds}$ = 0.1 V, the groups A and B have nearly identical $C_{rss}$ which are 907 pF and 906 pF respectively. Notably, the group B has a smaller $C_{rss}$ than A at voltage increases from 1 V to around 50 V. However, when $V_{ds}$ > 50 V, A and B have almost the same value. The $C_{rss}$ for group A and B are 6.83 pF and 4.83 pF, respectively, under condition of $V_{ds}$ = 800 V. In SiC VDMOSFET, the $C_{rss}$ is equal to $C_{gd}$, as following:

$$C_{rss} = C_{gd} \tag{1}$$

The $C_{gd}$ is approximately proportional to the overlap area between gate and drain. According to:

**Table 1**
Summary of experimental results.

| Design | Group A | | Group B | |
|---|---|---|---|---|
| Test temperature | 25 °C | 175 °C | 25 °C | 175 °C |
| BV [V] | 1544 | 1550 | 1510 | 1512 |
| *$V_{th}$ [V] | 3.21 | 2.10 | 3.22 | 2.12 |
| *$R_{on,sp}$ [mΩ·cm$^2$] | 6.48 | 12.06 | 7.69 | 13.87 |
| 3rd $V_F$ (@5 A)[V] | 2.60 | – | 2.83 | – |
| $C_{rss}$ (@ $V_{ds}$ = 800 V) [pF/cm$^2$] | 80.7 | – | 57.1 | – |
| $C_{oss}$ (@ $V_{ds}$ = 800 V) [pF/cm$^2$] | 893 | – | 917 | – |
| $C_{iss}$(@ $V_{ds}$ = 800 V) [nF/cm$^2$] | 17.7 | – | 17.1 | – |
| $Q_{gd,sp}$ [nC/cm$^2$] | 388 | – | 325 | – |
| HF-FOM ($R_{on}$ × $C_{gd}$) [mΩ·pF] | 522.9 | – | 439.1 | – |
| HF-FOM ($R_{on}$ × $Q_{gd}$) [mΩ·nC] | 2514.2 | – | 2499.3 | – |
| FOM ($C_{iss}$/$C_{rss}$) | 219.3 | – | 299.5 | – |

* Note: $V_{th}$ @ $V_{gs}$ = $V_{ds}$, $I_{ds}$ = 5 mA; $R_{on,sp}$ @ $V_{gs}$ = 20 V, $I_{ds}$ = 10 A.

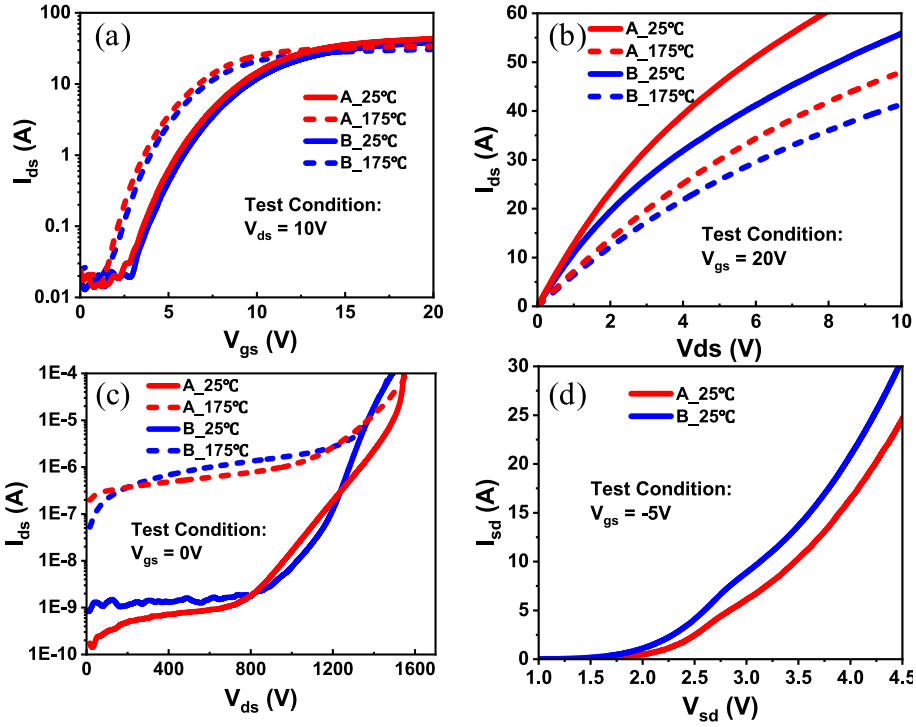



**Fig. 2.** (a) Transfer characteristics, (b) output characteristics, (c) blocking characteristics and (d) the third quadrant characteristics of group A and B.

$$A_{gd} = A_{act} \bullet \left(L_{JFET} - 2 \times L_{Dep}\right) / \left(L_{JFET} + L_{P-based}\right) \quad (2)$$

where $A_{gd}$ represents the overlap area between gate and drain, which is equal to JFET region area. $A_{act}$ is the active region area in SiC VDMOSFET chip. $L_{Dep}$ is depletion width of P-based PN junction in JFET region under applied $V_{ds}$. Group A and B have the same area of JFET region. At low $V_{ds}$ (< 1 V), the $L_{Dep}$ is not evident in JFET region. As a result, $C_{rss}$ mainly depends on the $L_{JFET}$. Further, the $L_{Dep}$ increases gradually with the increase of $V_{ds}$, resulting in a gradual decrease in $C_{gd}$. It is important to note that when $V_{ds}$ increases beyond 50 V, the JFET region is completely depleted, resulting in nearly identical $C_{gd}$ for groups A and B, meaning that the $C_{rss}$ is approximate a constant.

Fig. 3 (b) exhibits the $C_{oss}$ - $V_{ds}$ characteristics of group A and B. According to the formula:

$$C_{oss} = C_{gd} + C_{ds} \quad (3)$$

At low $V_{ds}$, groups A and B have almost the same $C_{gd}$, making $C_{ds}$ the main determinant of $C_{oss}$. The $T_{P\text{-based}}$ in group B is larger than that in group A, resulting in a larger $C_{ds}$. Fig. 3 (d) describes the characteristics of $C_{ds}$. Notably, groups A and B had almost identical $C_{oss}$ under condition of $V_{ds} > 20$ V since there are almost identical $C_{gd}$ and $C_{ds}$ in both designs.

Fig. 3 (c) displays the $C_{iss}$ - $V_{ds}$ characteristics of group A and B. According to the formula:

$$C_{iss} = C_{gd} + C_{gs} \quad (4)$$

The figure illustrates that in the range of $0\ V < V_{ds} < 1000$ V, group A has a larger $C_{iss}$ than that of group B. The study on $C_{gs}$, seeing in Fig. 3 (e), reveals that group B has a smaller $C_{gs}$ than group A at both low and high voltages. This is mainly due to group B having a deeper P-based region, resulting in a smaller P-based internal capacitance.

Fig. 3 (f) shows the characteristic of $Q_{gd}$ - $V_{gs}$. The figure shows that group B has a smaller miller plateau compared to that of group A, which are 27.5 nC and 32.8 nC, respectively.

Based on the test results, the high frequency figure-of-merit (HF-FOM) are calculated in Table I. The HF-FOM ($R_{on} \times C_{gd}$) of group A is 522.9 mΩ·pF, while that of group B is 439.1 mΩ·pF, meaning that group B has 16 % better than group A and group B has better high frequency switching performance.

## 4. UIS evaluation and reliability investigation

The circuit schematic, principle and equipment employed for the UIS test are shown in Fig. 4. The collection of instruments comprises of an oscilloscope, high-voltage power supply, signal generator, low-voltage power supply, current probe, voltage probe, and testing board. The high-voltage power supply is responsible for generating the required bus voltage for testing purposes, which in this research is set at 200 V. The signal generator supplies a drive signal to operate the DUTs in ON and OFF states, which corresponds to the inductance charging and DUT avalanche phases. The low-voltage power supply provides the voltage required for the gate driver of the DUTs. The oscilloscope displays the results of the avalanche waveform in this test. The current waveform is measured with Sybertek CPH9012 current probe, and the voltage waveform is measured with Siglent DPB5700A voltage probe. Simplified $V_{gs}$, $I_{ds}$, and $V_{ds}$ waveforms during avalanche are seen in Fig. 4 (b). When the DUT operates at the ON state, the inductor is charging and the $I_{ds}$ rising. The $I_{ds}$ can be obtained by flowing formula:

$$dI_{ds} = \frac{V_{DC}}{L} dt \quad (5)$$

When the DUT switches off and the energy stored in the inductor is released uncontrollably. A high di/dt in the inductor induces an extremely high voltage at the DUT, and the device operates on avalanche breakdown.

The energy stored in the inductor is released into thermal dissipation in DUT until the avalanche is finished. The calculated avalanche energy ($E_{av}$) is as following:

$$E_{av} = \int_0^{t_{av}} V_{BR(DSS)} \bullet I_{av}(t) dt \quad (6)$$

where $t_{av}$ represents duration of avalanche breakdown, and $I_{av}(t)$ is avalanche current varies with time.

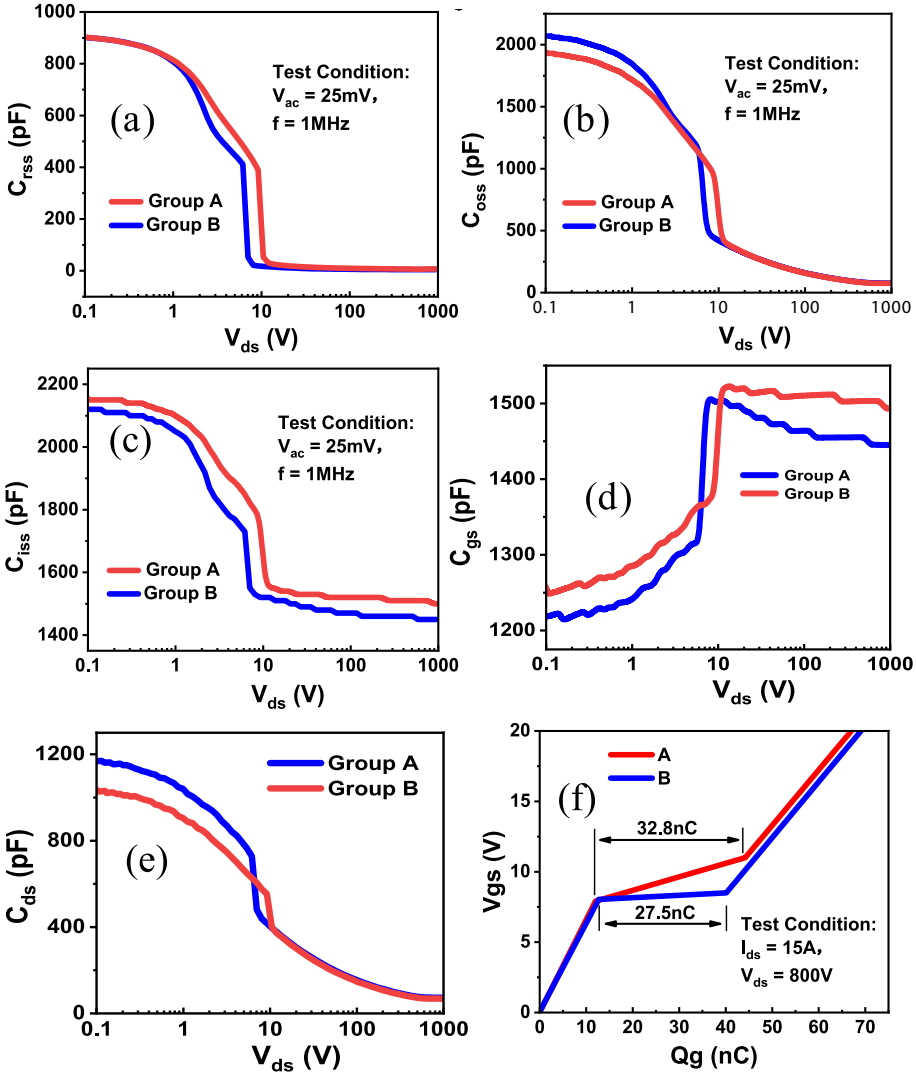



**Fig. 3.** (a) $C_{rss}$ - $V_{ds}$, (b) $C_{oss}$ - $V_{ds}$, (c) $C_{iss}$ - $V_{ds}$, and (d) $Q_g$ - $V_{gs}$ of group A and B. $C_{ds}$ - $V_{ds}$ and $C_{gs}$ - $V_{ds}$ characteristics are also shown in (e) and (f).

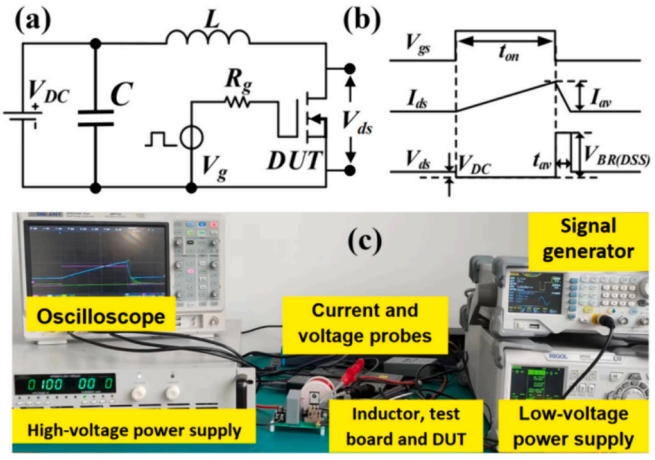



**Fig. 4.** (a) Simplified circuit diagram, (b) waveforms of $V_{gs}$, $I_{ds}$, and $V_{ds}$ and (c) UIS test platform. $V_{DC}$ = 200 V, L = 2 mH, $V_{gs}$ = −5/+20 V.

## 5. UIS results and discussion

The UIS characteristics of group A and B in both room temperature (25 °C) and high temperatures (175 °C) are tested. In order to more accurately measuring the capabilities of Group A and Group B in UIS, the experimental procedure is as follows: Firstly, take a virgin device and gradually increase the charging time by 1 μs / step until the device failure. Record the UIS waveform before and failure. Next, the maximum current ($I_{ds,max}$), maximum breakdown voltage ($V_{ds,max}$), maximum loss energy power ($P_{av,max}$), and avalanche energy ($E_{av}$) before and after avalanche failure of group A and B are extracted. All the test results are summarized in Table 2.

**Table 2**
Summary of UIS experimental results.

| Design | $T_C$ (°C) | $I_{ds,max}$ (A) | $V_{ds,max}$ (V) | $P_{av,max}$ (kW) | $E_{av}$ (mJ) | DUT Status |
|---|---|---|---|---|---|---|
| Group A | 25 | 25.1 | 1775 | 41.4 | 636 | Good |
| | | 25.3 | 1775 | 42.0 | 656 | Failure |
| Group B | 25 | 25.3 | 1741 | 41.5 | 706 | Good |
| | | 25.5 | 1741 | 41.8 | 722 | Failure |
| Group A | 175 | 28.2 | 1791 | 45.4 | 413.3 | Good |
| | | 27.2 | 1791 | 46.9 | 413.5 | Failure |
| Group B | 175 | 29.0 | 1741 | 42.7 | 470 | Good |
| | | 29.2 | 1741 | 44.3 | 473.3 | Failure |

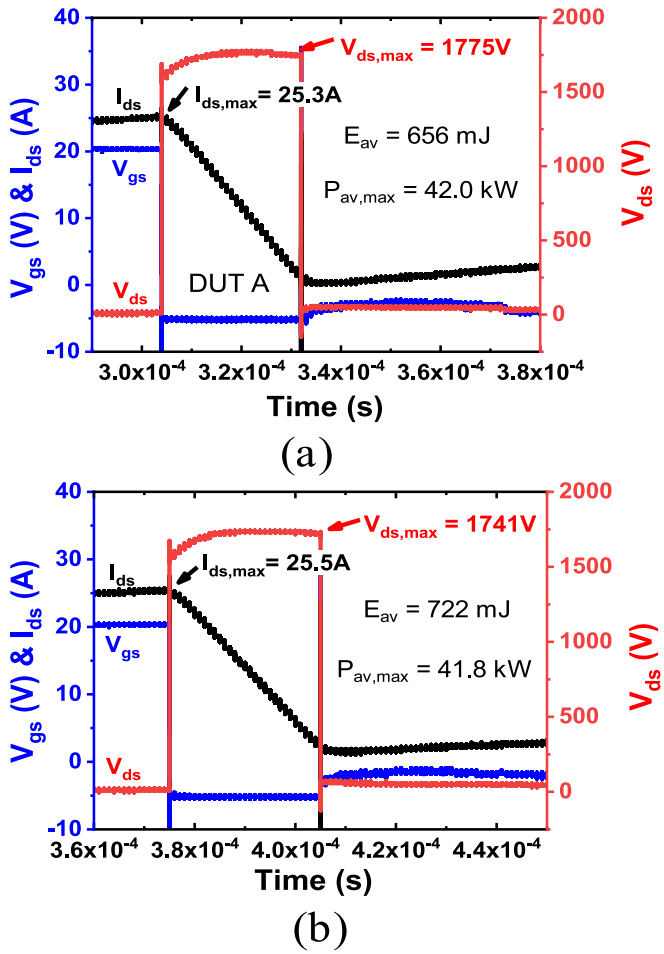



**Fig. 5.** UIS failure waveforms of group A and B in room temperature ($T_C$ = 25 °C).

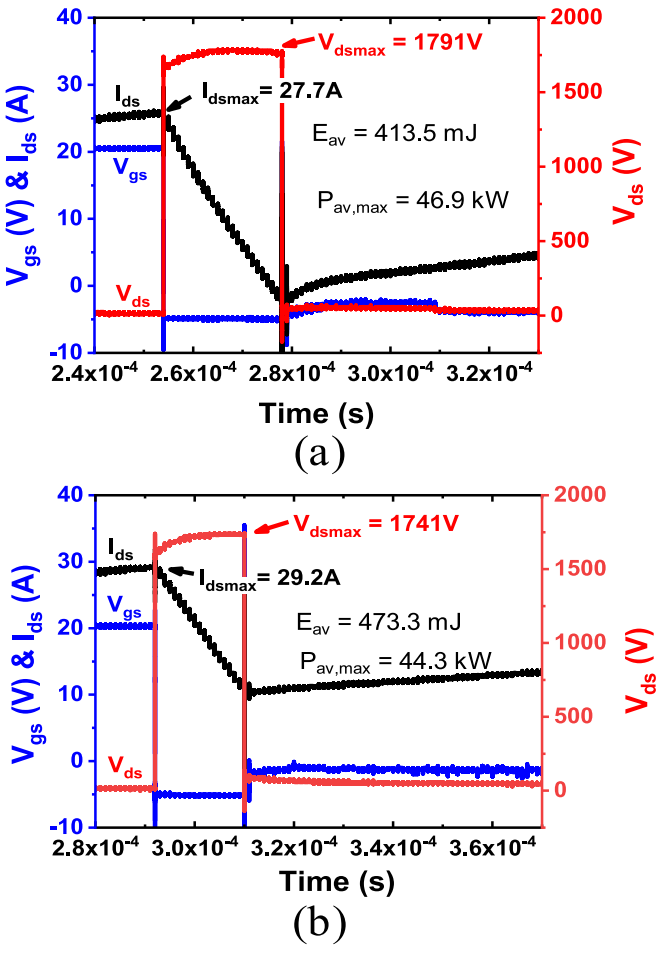



**Fig. 6.** UIS failure waveforms of group A and B in high temperature ($T_C$ = 175 °C).

In order to gain a more intuitive understanding of the failure mechanism, waveforms representing the avalanche failure process of group A and B in 25 °C are extracted and presented in Fig. 5. The pixel defect observed in the current waveform is primarily caused by the insufficient bandwidth of the oscilloscope. Fig. 5 (a) displays the waveform of group A during avalanche failure. The $I_{ds,max}$ is 25.3 A. The $V_{ds,max}$ is the same as before failure. However, the $P_{av,max}$ is 42 kW, which is 0.6 kW larger than the previous moment. The $E_{av}$ increases by 20 mJ to 656 mJ compared to the previous measurement, which is converted into heat dissipating during avalanche breakdown. Waveform characteristics of group B during avalanche failure are shown in Fig. 5 (b). At the case of avalanche failure, the $I_{ds,max}$ is 25.5 A, 0.2 A larger than the $I_{ds,max}$ contained before failure. And the $V_{ds,max}$ is 1741 V. During avalanche failure, group B has a smaller $P_{av,max}$ than group A, which is 41.8 kW. It should be noted that group B has a higher avalanche robustness than group A, as evidenced by its $E_{av}$ at avalanche failure of 722 mJ, which is 66 mJ higher.

Fig. 6 displays the UIS failed waveforms of group A and B in high case temperatures (Tc = 175 °C). The $E_{av}$ of group A before and after failure are 413.3 mJ and 413.5 mJ, respectively, while the $P_{av,max}$ are 45.4 kW and 46.9 kW, respectively. The values of both are very close, indicating that the device is on the verge of failure. The $E_{av}$ before and after group B failure are 470 mJ and 473.3 mJ, respectively. The $P_{av,max}$ are 42.7 kW and 44.3 kW, respectively. The results show that the avalanche ability of group A and group B decreases at 175 °C, mainly due to the increase of on-resistance. In the avalanche state, the parasitic BJT turns on earlier than that at 25 °C, and the current is easier to reach a runaway state, resulting in failure.

In order to investigating failure mechanism, group A and B are analyzed by Scanning Acoustic Microscope (SAM) and optical microscope (OM). Fig. 7 (a) and (b) display scanning results by SAM. The red areas in the images represent the layered regions. Clearly, the layered region in group A is located at the edge of chip, while group B is located at the chip corner, indicating different failed point positions. It is well known that the group A and B underwent significant thermal dissipation during avalanche. Such a large amount of heat is generated at the failed position, and the local temperature would exceed the burning temperature of molding compound, resulting in carbonization. Further, group A and B after avalanche failure are decapsulated and observed, and the OM pictures are shown in Fig. 7 (c) and (d), respectively. Besides, the OM photographs are zoom up for a clearer analysis of the failure points. As seen in Fig. 7 (c), there is a noticeable carbonization traces at burnt out position of group A, and the failure location is consistent with the SAM result. Significantly, there is a clear indication of metal melting at the failure position. This suggests that the instantaneous heat generated during avalanche not only carbonized the molding compound, but also melted the source metal. The OM photograph of group B in Fig. 7 (d) illustrates that the failure position is situated in the upper corner of the chip, which is consistent with the result of SAM. Clear traces of carbonized molding compound and metal melting are also observed by zoom up. Additionally, a significant crack is observed at burnt out region. It is confirmed that group B experiences a greater degree of temperature shock during avalanches than group A, as evidenced by the fact that group B has a larger $E_{av}$.

In order to further analyze the reliability and failure mechanism of SiC VDMOSFETs with different P-based depths, the half-cell structure of

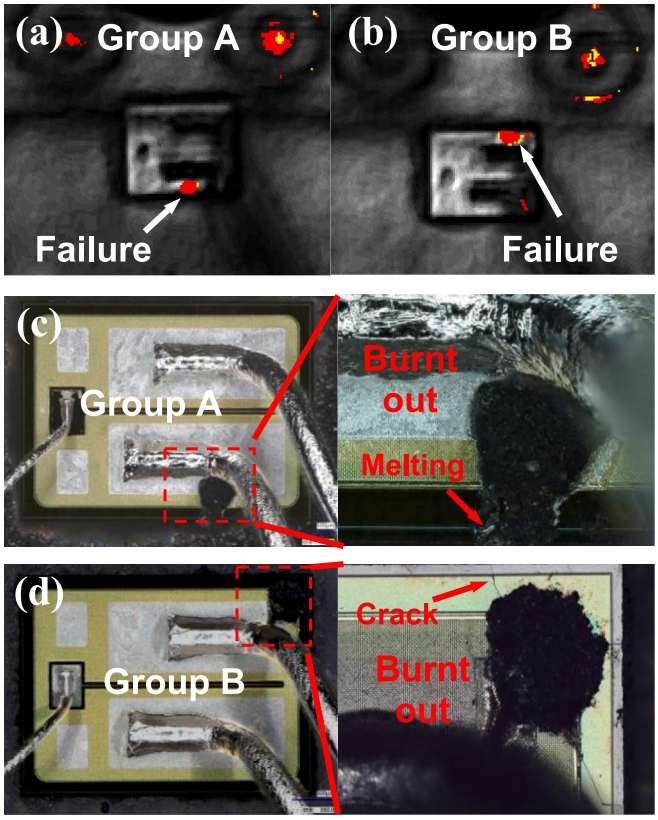



**Fig. 7.** (a) and (b) are C-SAM of group A and B, (c) and (d) are optical microscope images and zoom in for failed device in $T_C = 25$ °C.

SiC VDMOSFET were constructed using Sentaurus TCAD. The simulated geometric parameters and doping concentration are consistent with experimental parameters. Electrothermal simulations are performed to estimate the temperature of SiC VDMOSFETs. The physical models including self-heating, incomplete dopant ionization, interface mobility degradation, doping and temperature-dependent mobility, and anisotropic high-field mobility saturation are considered. The anisotropy is fully accounted for in mobility, impact ionization coefficients, permittivity, and thermal conductivity [14,15]. The critical parameters including thermal conductivity $k$ and heat capacity $c_v$ of 4H-SiC are significant in electrothermal simulation. In this paper, the $c_{v,4H\text{-}SiC}$ from [14] is used. The error between simulated fit and the measured $c_v$ data is <10 % in the whole range from 300 to 2700 K. The thermal conductivity of 4H-SiC $k_{c,4H\text{-}SiC}$ is also referred from [14]. The temperature dependence of the mass density for 4H-SiC, as well as for gate oxide and top metal, is very small and, hence, neglected in the TCAD electrothermal simulations. According to the reference [14], the simulated results are consistent with experimental measurement, indicating that the simulation results presented in the paper are reliable. Further, the simulated circuit is the same as that in previous UIS test, seeing in Fig. 4 (a). Fig. 8 (a) displays the waveforms and characteristics of SiC VDMOSFETs extracted from TCAD simulation during avalanche, including $V_{gs}$, $I_{ds}$, $V_{ds}$, and maximum internal temperature ($T_{max}$). During avalanche breakdown, the moments of t1 and t2 are extracted, which represent the avalanche breakdown start and end, in order to analyze internal physical parameters of SiC VDMOSFETs. The following step involves discussing the change of internal parameters of SiC VDMOSFETs during three periods divided by t1 and t2. Besides, the circuit schematics of SiC VDMOSFETs and avalanche current paths during avalanche breakdown are described, as shown in Fig. 8 (b). Fig. 8 (c) illustrates the current density distribution inside group A at t1, t1 ~ t2, and t2. Clearly, the breakdown point of group A at t1 is located at the P-based corner, and the current mainly flows from the drain to the source through the breakdown position. Between t1 and t2, the breakdown current exists at both the breakdown position and the channel. It is important to note that the $V_{gs}$ is currently at 0 V, indicating that the channel is closed. Consequently, the parasitic BJT of group A is turned on, resulting in uncontrolled current. Current distribution at t2 moment indicates the parasitic BJT is fully turned on, meaning current out of control completely. Likewise, this phenomenon is also observed in group B, which is not depicted in the picture. Furthermore, the internal temperature distributions of group A are extracted at t1, t1 ~ t2, and t2 during avalanche breakdown, seeing in Fig. 8 (d). Clearly, the highest temperature is mainly concentrated at JFET region. The temperature rises dramatically in a very short time during avalanche breakdown. The maximum temperature of group A is 508 K at t1. However, the temperature reaches 1725 K at t2 and the duration from t1 to t2 only takes 17 μs. The highest temperature in group A has exceeded the melting point of aluminum metal (935 K), meaning failure of device. The group B and group A have similar temperature distribution trends, as shown in Fig. 8 (e). The maximum temperature of group B is 655 K at t1. Notably, at time t2, the maximum temperature of group B reaches 1858 K, which is 133 K higher than that of group A. The result indicates that the group B is also failed at t2. In order to investigate the failure mechanism of device, current paths during avalanche breakdown in SiC VDMOSFET are described, as shown in Fig. 8 (b). The group B has a larger P-based region than group A, meaning a smaller $R_b$ in group B. The parasitic BJT in silicon carbide is activated when the voltage at both ends of $R_b$ exceeds 2.7 V, which is the potential barrier of the PN junction. The group B requires higher avalanche energy to increase high temperatures and active the parasitic BJT during UIS, no matter in room temperature (25 °C) or high temperature (175 °C). Once the BJT is turned on, the current is uncontrollable in SiC VDMOSFETs, and the internal temperature would rise to an extremely high temperature in an instant, exceeding the limitation of material, contained modeling compound, metal alloy, and so on, and causing device damage. In addition, the instantaneous temperature shock will also lead to metal melting and material cracking, which are confirmed in Fig. 7 (c) and (d). Therefore, group B has a high avalanche capacity and higher UIS reliability than group A.

## 6. Conclusion

In this paper, two $T_{P\text{-}Based}$ of SiC VDMOSFETs are designed and manufactured, which are named group A and B, corresponded to low and high energy implantation, respectively. The static and dynamic properties of group A and B are measured and compared. The group A has a better static properties, while group B has a higher high frequency switching performance. Further, the avalanche reliability and failure mechanism for two groups are investigated by UIS experiment and TCAD simulation. Group B has a higher capacity for avalanche energy. Additionally, the avalanche damage in Group B is more severe. The reason is that high instantaneous temperature is generated by energy dissipation during avalanche and it drives the parasitic BJT conduction, causing Ids out of control. High $T_{P\text{-}Based}$ exhibits higher UIS reliability in group B since from smaller $R_b$ and more difficult to active parasitic BJT.

## CRediT authorship contribution statement

All authors contributed to the study conception and design. Material preparation, data collection and analysis were performed by Houcai Luo, JingpingZhang and Huan Wu. The first draft of the manuscript was written by Houcai Luo and all authors commented on previous versions of the manuscript. All authors read and approved the final manuscript.

## Declaration of competing interest

The authors declare that they have no known competing financial

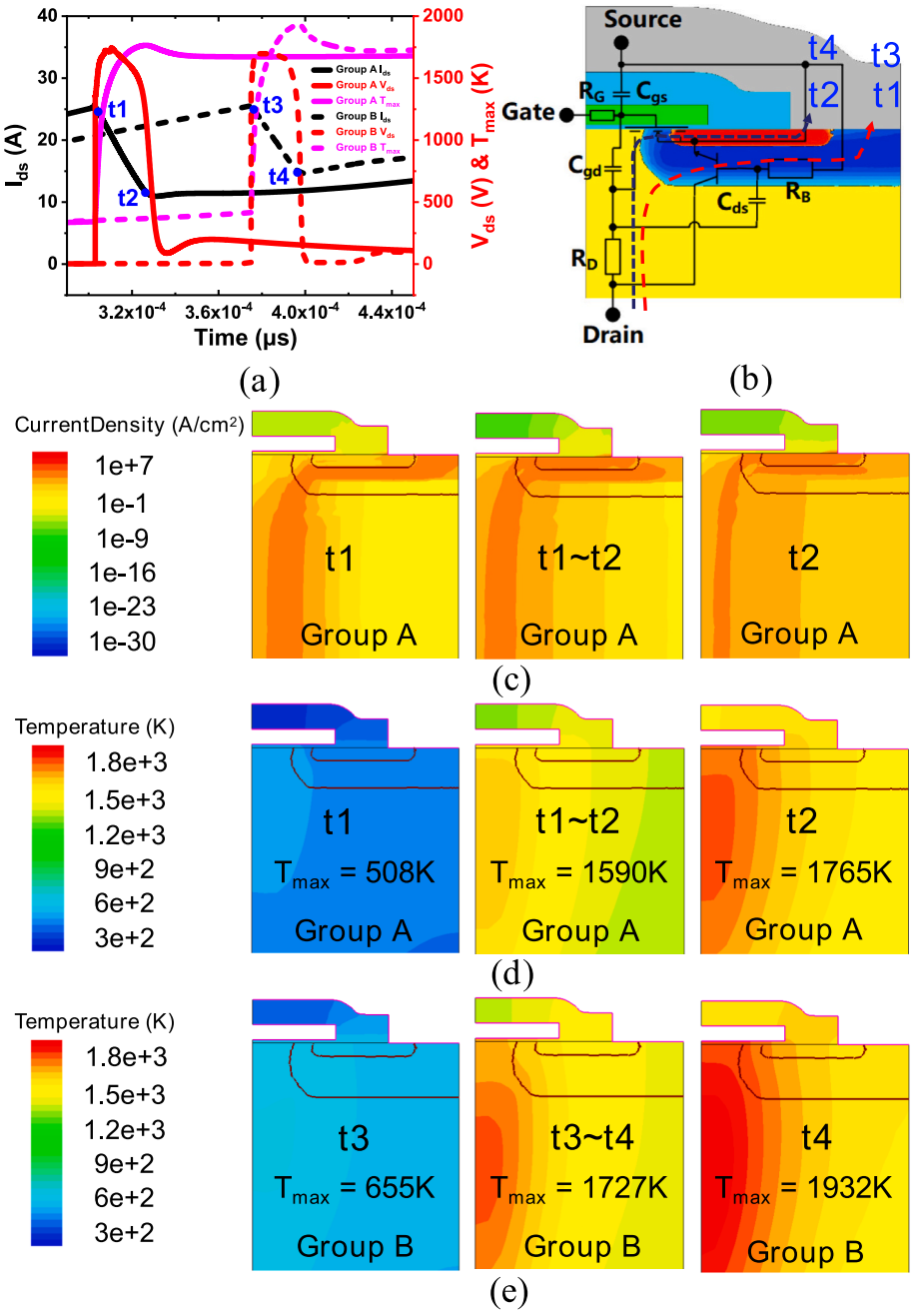



**Fig. 8.** (a) Simulated waveform of avalanche failure. (b) Circuit schematics of SiC VDMOSFETs and current paths during avalanche breakdown. (c) Current density within group A, (d) temperature distribution at time point t1, t1 ~ t2, and t2 in group A, and (e) in group B.

interests or personal relationships that could have appeared to influence the work reported in this paper.

## Data availability

No data was used for the research described in the article.

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