Reinforcement bipolar read: addressing read disturb in RRAM

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by

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What a long, strange trip it's been... while things may not have gone the way I wanted them to, which may have its reverberations for some time, I am glad to have eventually seen it through.
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Douwe Brinkhorst
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Abstract

Memory advances have not kept up with computing demands. Emerging device technology Resistive RAM (RRAM) addresses this by enabling computation-in-memory. However, RRAM suffers from read disturb, limiting viability. While earlier work has had some success in reducing read disturb by switching the read current direction (a bipolar read scheme), the RRAM device eventually degraded. In this work, a reinforcing bipolar read scheme is introduced, which aims to prevent read disturb by reinforcing both HRS and LRS, away from the undefined state. From device-level simulation, this reinforcing behaviour is predicted for V = 0.5, 0.4 and 0.3 V with a fixed switching ratio between time under positive and negative read voltage polarity r_{switch} = 2.5, 2.5 and 2.75, respectively. At V = 0.2 V and V = 0.1 V, it is predicted that no reinforcement scheme exists. The bipolar read scheme found for V = 0.5 V was evaluated in circuit simulation with a sense amplifier. however the HRS and LRS reinforcing behaviour found at device-level could not be replicated. From unipolar read results at circuit level, it was determined no switching ratio exists that reinforces both the HRS and LRS state boundaries as chosen here at $R_{HRS,min}$ = 12.8$k\Omega$ and $R_{LRS,max}$ = 4.4$k\Omega$ for V = 0.5 V. However, a 5.1x reduction in resistance drift compared to conventional unipolar read was still obtained.

1 Introduction

1.1. Motivation

The demand for computing is still expanding, in particular in artificial intelligence, where Large Language Models have seen much success in the last few years . To meet this demand in an economic and sustainable way, advances in computing are needed, but these have been become increasingly difficult to achieve this century. Several walls describe these issues[7]:

- The leakage wall of static power approaching or exceeding dynamic power in advanced Complementary Metal-Oxide Semiconductor (CMOS) transistor technology .
- The reliability wall of increasing error rate and reduced lifespan as CMOS is scaled down.
- The cost wall of nearly flat cost-per-transistor as CMOS is scaled down.
- The instruction-level parallelism wall of limited growth of performance per processor core.
- The power wall of heat dissipation limits being reached and slow performance-per-Watt improvements since the end of Dennard scaling around 2005.
- The memory wall of conventional memory not keeping up with increases in CMOS logic speed.

Let us look further into the memory wall.

Of the conventional memory technologies, DRAM is much slower than CMOS logic and needs to be refreshed periodically, making it volatile and consuming static power. NAND flash as a storage-class memory is nonvolatile, but suffers from high write voltages and low write endurance. Emerging memory technologies seek to address these issues. Among these are resistive random-access memory (RRAM or ReRAM), ferroelectric random-access memory (FeRAM), phase change random-access Memory (PCRAM), spin-transfer-torque magnetic random-access memory (STT-MRAM) [7][8]. Several properties make RRAM of interest: high density, great scalability, low write power, faster write and high resistance ratio [1][9][10].

Of particular interest is the use of RRAM devices for computation-in-memory (CIM), where computation can be performed in the memory array, avoiding the high energy cost of data transportation. This can be done by exploiting the fact that the data is stored as a resistance R or a conductance G = 1 /R. When the memory is read, output current I is a function of input voltage V and stored conductance G, so some (logic) function $V, G \Rightarrow I$ can be implemented. This is particularly useful for performing vector-matrix multiplication (VMM), a key part of neural network inference [7][8][11].

However, RRAM does suffer from read disturb, where read operations cause resistance drift in the device, accumulating into a change of logical state [12] [4][13][14][15]. A reduction in read disturb is desired.

1.2. State of the art

A way of addressing read disturb which shows promise is bipolar read. As changing the read polarity of the RRAM device changes the sign of resistance drift, reading the RRAM device with a mix of positive and negative read voltages results in lower net drift, delaying read disturb by 6x-14.85x [6][16]. This relies on a uniform read

pattern, such as vector-matrix multiplication on the RRAM array.
These existing solutions do however have their limitations. Shim *et al.* [6] employ a bipolar read scheme which seeks to keep device resistance in equilibrium. However this scheme can only stabilize LRS, leaving HRS vulnerable to read disturb. Yan *et al.* [16] instead reinforce the device state, but this requires a bipolar read scheme that has poor area scaling and fails to reinforce the device when the neural network output is incorrect. It also relies on a specific neural network implementation that may limit wider use.

1.3. Contributions

- Device-level simulation that predict RRAM device characteristics allow for a reinforcement bipolar read scheme. This scheme involves switching the read current direction, with the ratio between the positive and negative read polarities chosen such that both the high-resistance state and low-resistance state are reinforced (i.e. resistance increases/decreases in HRS/LRS, respectively), away from the undefined state in-between. This concept is illustrated in figure 1.1.
- Requirements for a stabilizing bipolar read scheme, that keeps both HRS and LRS out of the undefined state and deep states, are formulated.
- A test circuit for RRAM write and read where the read voltage polarity can be switched, enabling a bipolar read scheme.
- An circuit-level evaluation of RRAM write, read and the proposed reinforcement bipolar read scheme.

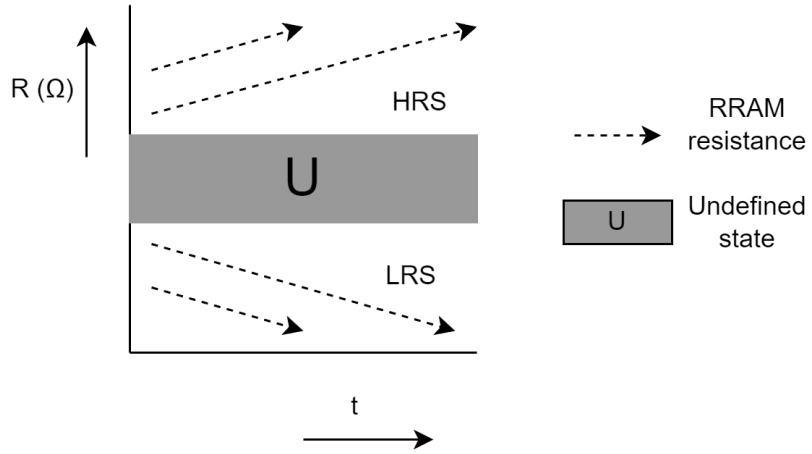


Figure 1.1: Conceptual drawing of the reinforcing effect of a reinforcement bipolar read scheme.

1.4. Organisation

The thesis is organised as follows. Chapter 2 provides background on RRAM, read disturb, the RRAM device model and RRAM arrays. Chapter 3 discusses the related works on RRAM bipolar read. Chapter 4 discusses the proposed bipolar read scheme. Chapter 5 discusses the proposed circuit design. Chapter 6 provides the evaluation setup, simulation results of circuit write, read and bipolar read. These results are then discussed. Finally, chapter 7 concludes this thesis and discusses future work.

2
Background

This chapter provides the background information that is required for the understanding of this thesis. First, an overview of the RRAM device is given in section 2.1, followed by a description of the RRAM array in section 2.2. Section 2.3 describes the VCM RRAM type in more detail. Thereafter, sections 2.4 and 2.5 discusses the read disturb phenomenon and logical RRAM states, respectively. Section 2.6 goes on to briefly discuss CIM and how it relates to read disturb. Finally, section 2.7 describes the RRAM device model that was used in this thesis.

2.1. Resistive Random Access Memory (RRAM) overview

Resistive Random Access Memory is a class of emerging nonvolatile memory with the unifying property that its resistance can be changed through an electrical signal. The RRAM device has a low resistance state (LRS) and a high resistance state (HRS). By applying V_{SET} for sufficient time the device transitions from the HRS to the LRS, while applying V_{RESET} similarly causes a transition from LRS to HRS [9]. A voltage V_{READ}, lower in absolute terms that either of the write voltages, can be used to read the resistance state of the device.
A major distinction within RRAM devices is between the unipolar and bipolar device.

2.1.1. Bipolar RRAM

The bipolar device is characterized by V_{SET} and V_{RESET} having opposite polarities (see figure 2.1). This means the polarity of V_{READ} has to be the same as either V_{SET} or V_{RESET}, which leaves the device susceptible to read disturbance of the HRS or LRS, respectively [1].

2.1.2. Unipolar RRAM

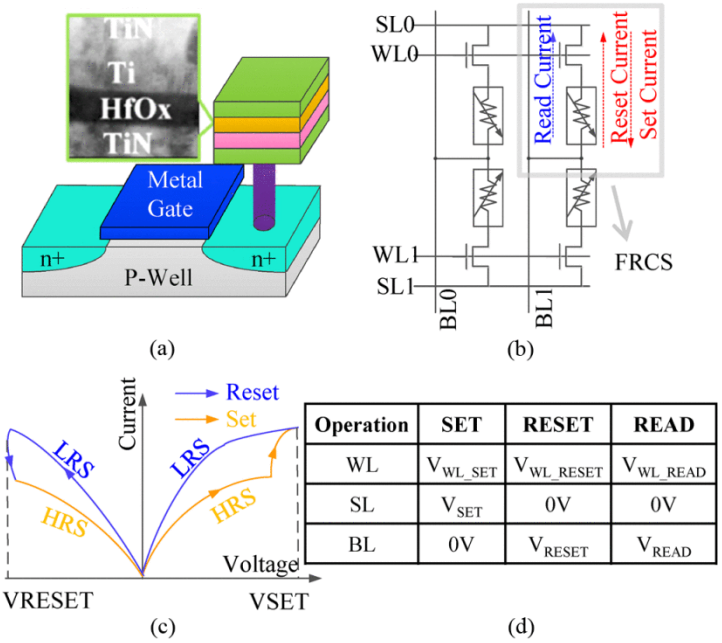
In the unipolar device, on the other hand, V_{SET} and V_{RESET} have the same polarity, with SET requiring a higher voltage and current [1]. A major advantage of the unipolar device is that V_{READ} can have the opposite polarity to both V_{SET} and V_{RESET}, making it immune to read disturb [1].

2.1.3. Bipolar RRAM advantages & RRAM types

Bipolar RRAM devices have been shown to achieve much lower write voltage ($V_{write} < 2V$) and write current ($I_{write} < 10$ than the unipolar RRAM device (($V_{write} \approx 3V$ and $I_{write} > 50$) [1]. Devices based on the valence change mechanism (VCM), among which HfO2-based cells, are bipolar [17]. Other devices that have been described as RRAM are phase change memories (PCM) and thermochecmical memories (TCM) [18]. In this work, the VCM device is focused on.

2.2. RRAM array

Common RRAM array types are crossbar and 1T1R, where 1T1R array is has cells composed of a select transistor and RRAM device, while the crossbar array has cells composed of just the RRAM device, sometimes paired with a nonlinear device to reduce sneak paths.
Let us explore the design and operation of a typical 1T1R bipolar RRAM array (see also figure 2.1) [1]. The wordline (WL) is connected to the select transistor gates. By powering a wordline, the connected array row



Operation	SET	RESET	READ
WL	V_{WL_SET}	V_{WL_RESET}	V_{WL_READ}
SL	V_{SET}	0V	0V
BL	0V	V_{RESET}	V_{READ}

(d)

Figure 2.1: a) Cell structure, b) array, c) *I-V*curves, d) operational voltages for a typical bipolar 1T1R cell. [1, figure 4]

is opened for read or write. The sourceline (SL) is connected to the select transistor, while the bitline (BL) is connected to the RRAM device.

2.2.1. (Forward) read operation

The read operation is performed by grounding the source line (SL) and powering the bitline (BL) to V_{read}. This is a forward read configuration [1]. By connecting the NMOS select transistor to ground, the body effect is avoided. However this choice leaves the LRS susceptible to read disturb.

2.2.2. Write operation

The RRAM device is connected such that when writing the cell, SET (RESET) is performed by powering the source line (bit line line) to V_{SET} (V_{RESET}) while the bit line (source line) is grounded [1]. By aligning the voltage polarities of both the read and RESET operations, both avoid the body effect. It is preferable to suffer the body effect during SET than during RESET, as the SET operation requires a lower voltage [3]. Typically, V_{SET} (V_{RESET}) are defined to be a positive (negative) voltage.

2.2.3. Reverse read operation

The RRAM device can also be read by powering the SL while grounding the BL. This is called reverse read, which is typically avoided due to the body effect in the select transistor. However in the goals of this thesis both forward and reverse read will be used in an attempt to reduce read disturb. The body effect is the increase in threshold voltage when the NMOS transistor source voltage is higher than the bulk voltage (which is typically zero).
In this thesis, the voltage polarities for the read and write operation are referred to as positive (negative) when the SL (BL) is powered and the BL (SL) is grounded. This means the typical forward read is has a negative voltage polarity and may also be referred to as negative read. The reverse read operation has a positive voltage polarity and may be referred to as positive read.

2.3. Valence change mechanism (VCM) RRAM

The valence change mechanism RRAM relies on the movement of oxygen vacancies in the device. This is shown in figure 2.2.
A positive voltage causes a conductive filament to form (set operation), bringing the device to a low resistance state (LRS)[19]. Continued application of a positive voltage increases the width of the conductive filament, further decreasing resistance [5].

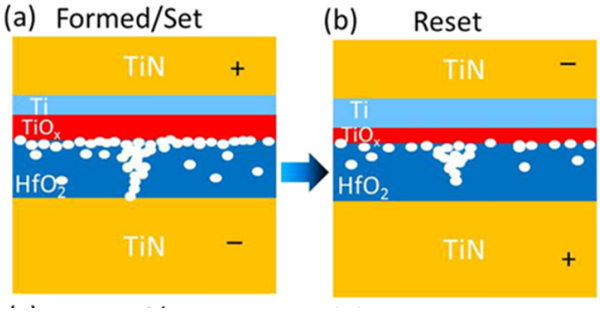


Figure 2.2: Conductive filament diagram [2, fig. 4]

A negative voltage ruptures this conductive filament (reset operation), putting the device into a high resistance state (HRS)[19]. The resistance of this state depends on whether a partial filament still exists which increases conductivity [5].
The rate of this formation/rupturing exponentially increases with the internal voltage across the Schottky barrier [3] [5]. This enables writing the device at high speed with a 1-2 V voltage while a small read voltage will cause very little change in device resistance. Unfortunately this resistance drift can still accumulate over time, which will be discussed in section 2.4.

The resistance of RRAM after write is variable, as shown in figure 2.3.

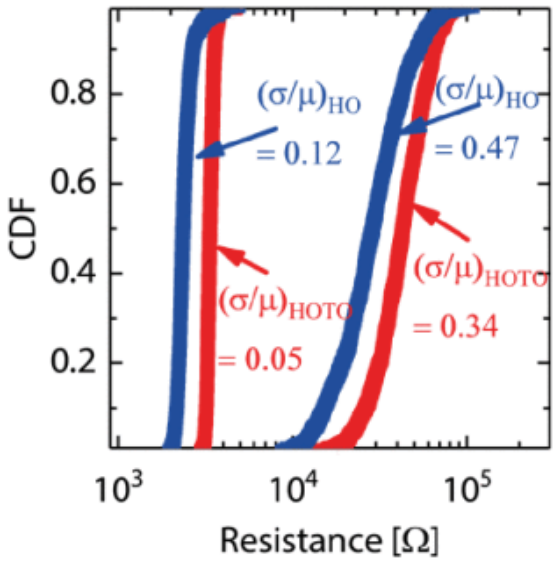


Figure 2.3: Variability of HfO_2/TiO_x resistance after pulsed-write [3, fig. 3b]

2.4. Read disturb

As was brought up in section 2.3, while small read voltages have an exponentially smaller effect than write voltages, they still cause some resistance drift. Over many reads, this resistance drift can accumulate into read disturb, where the logical value of the device has changed.
Measurements of read disturb in RRAM measurements were performed by Lee et al. [4]. These are shown for the LRS in figure 2.4. It can be seen that the current decreases under a small negative stress voltage, indicating an increase in device resistance. Observed stress times to see read disturb vary greatly, as read disturb after 0.1 seconds has also been observed for V = 0.5 V [5].

Figure 2.5 shows a simulation how neural network accuracy degrades due to read disturb. It can be seen read disturb exponentially increases with voltage, as was mentioned in section 2.3.

Resistance decrease in the LRS state is limited in speed and depth by series resistance becoming dominant

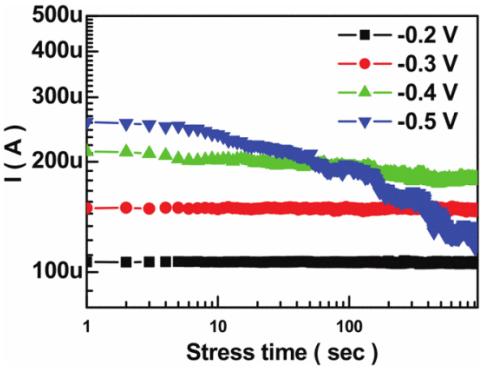


Figure 2.4: TiN/Ti/HfO2/TiN RRAM in LRS is disturbed under negative stress voltage. [4, figure 5]

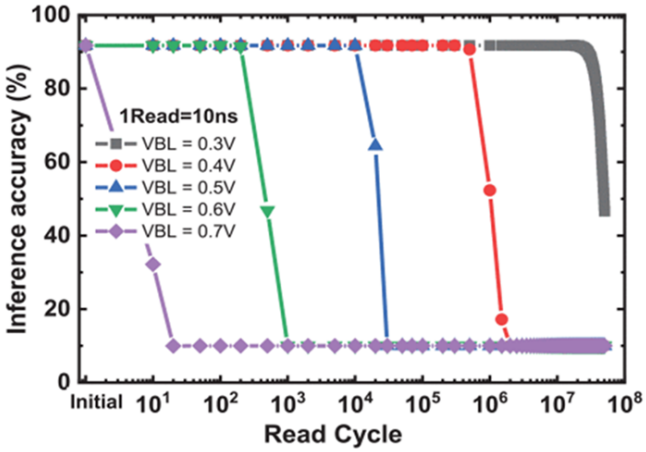


Figure 2.5: Simulated inference accuracy degrades due to read disturb. [5, figure 10]

for lower V_{read} [15] . A strong correlation between higher SET currents and faster read disturb was observed in tungsten oxide RRAM [14].

2.5. RRAM states

To properly address read disturb, it should be considered what logical states exists for RRAM that the device should remain in.
Several fault mode RRAM states have been noted in literature on RRAM testing [20][21]. Figure 2.6 shows the RRAM states as referred to in this thesis. The undefined state exists between LRS and HRS. Extremely high (low) resistances are known as the deep HRS (LRS) state, respectively (elsewhere described as H (L), respectively). HRS and LRS can also be referred to as logical 0 and logical 1, respectively, directly referring to binary data storage. What resistance bands the RRAM device must remain in depends on the application. Input voltages can be analog or digital, multilevel cells exist where LRS is split into multiple logical values [5], output current is frequently analog [8][22][23][24][25][26][11].

2.6. Computation-in-memory

In this section, computation-in-memory (CIM) is briefly discussed. The focus is on how CIM relates to read disturb.

2.6.1. Vector-matrix-multiplication

A typical use case for RRAM is vector-matrix-multiplication (VMM). This computation is widely used in neural network inference. The weight matrix of the neural network is stored in the RRAM array. The input vector is provided to the word lines, opening some of the rows. Let us discuss two variants of VMM:

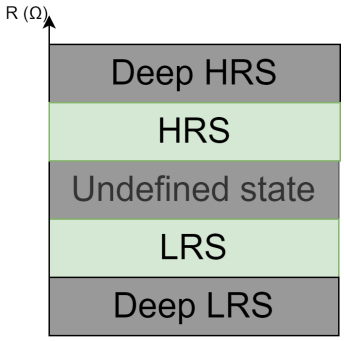


Figure 2.6: Overview of RRAM states as referred to in this thesis.

- Binary VMM [7]: the bitline is pre-charged. If any cell in the column is logical 1 and it received a logical 1 input, the pre-charged voltage will drain through this cell, bringing it low enough for the voltage sense amplifier to output logical 1. Otherwise the output is logical 0.
- Weighted sum VMM [6]: After providing a voltage on the bitline, each cell that receives an input will produce some current. These currents will drain into the current sense amplifier at the bottom of the column, becoming an analog summation. If this passes a threshold, the sense amplifier output becomes logical 1, corresponding to activation of a neuron.

2.6.2. VMM in relation to read disturb

VMM in RRAM is typically a write-once-read-many application. After the weights are programmed, it is preferred to not write again, as this takes a comparatively high amount of energy and requires additional circuitry. Also, write endurance of RRAM is limited.
This high number of reads leaves VMM in RRAM vulnerable to read disturb. However, in VMM the array access is quite uniform, so a bipolar read scheme (where a mix of forward and reverse read operations are used), which may reduce read disturb, can also be applied to each cell in a uniform manner.

2.7. RRAM device model

Hardtdegen et al. propose a compact model for a HfO_2/TiO_x (HOTO) bipolar redox-based resistive random-access memory (RRAM) device [3]. This device model was chosen for compatibility with other research within the group. They claim HfO_2 as a switching material enables a high switching speed and a stable endurance. The model is shown to match the measured device fairly well in figure 2.7.

Here follows an overview of the model. Select model equations are given, which are of particular interest to this work.
The electrical components of the model are shown in figure 2.8. The device state is determined by the oxygen vacancy concentration N_{disc} in HfO_2 near the Pt interface, this area is called the disc. These vacancies modulate the height of the Schottky barrier, which is a major component of effective device resistance.
Through the HfO_2 layer there is a conductive filament of oxygen vacancies (a reduced oxide), comprised of the disc and plug. The plug oxygen vacancy concentration N_{plug} is assumed constant. l_{plug}, l_{disc} and l_{cell} are the plug length, disc length and HfO_2 layer length, respectively.
In the filament, band conduction is assumed. As the oxygen vacancy concentration varies by orders of magnitude, it is assumed to dominate conductivity. Resistances of the plug and disc can then be calculated as:

$$R_{\text{plug}} = \frac{l_{\text{plug}}}{e\, z_{\text{V0}}\, N_{\text{plug}}\, \mu_n\, A} \tag{2.1}$$

$$R_{\text{disc}} = \frac{l_{\text{disc}}}{e\, z_{\text{V0}}\, N_{\text{disc}}\, \mu_n A} \tag{2.2}$$

where A is the filament cross-section area with $A = \pi r_{\text{fil}}^2$ with r_{fil} being the filament radius. In addition, e is the elementary charge, z_{V0} is the oxygen vacancy charge number, and μ_n is the electron mobility. The equations for the forward and reverse Schottky current can be found in [3]. Of note is that $I_{\text{Schottky}} \propto exp(V_{\text{Schottky}})$

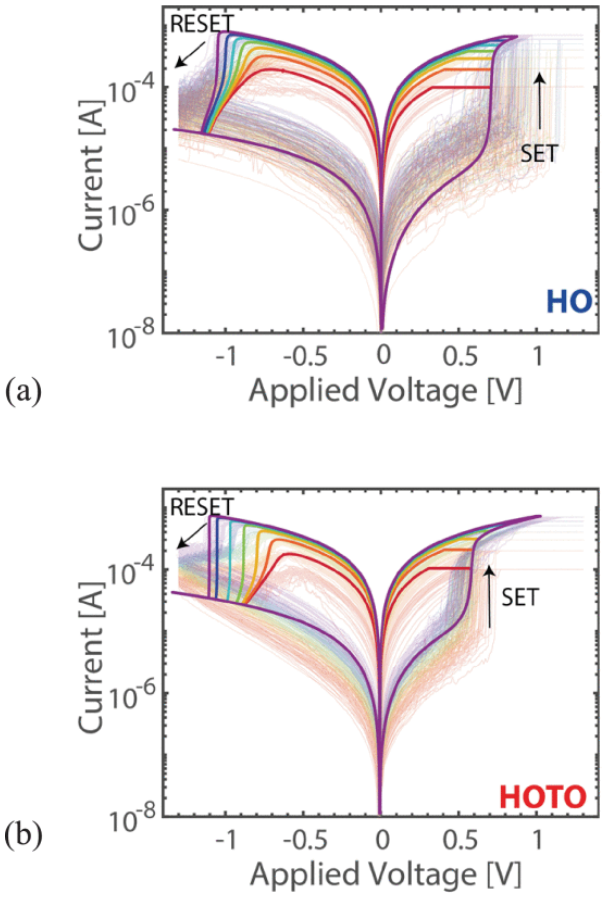


Figure 2.7: Comparison of modeled I-V curves to the measured I-V curves. [3, figure 6].

The change in oxygen vacancy concentration in the disc is given by:

$$\frac{dN_{\text{disc}}}{dt} = \frac{I_{\text{ion}}}{z_{\text{V0}}\, e\, A\, l_{\text{disc}}} \tag{2.3}$$

and is caused by an ionic current (oxygen vacancies moving), $I_{\text{ion}} \propto sinh(E)$, where E is the electric field. When V > 0, the voltage across the disc is responsible for moving ions into the disc:

$$E = V_{\text{disc}} / l_{\text{disc}} (V > 0) \tag{2.4}$$

While for V < 0, the voltage across the HfO_2/Pt region is more appropriate for calculating the field:

$$E = (V_{\text{Schottky}} + V_{\text{disc}} + V_{\text{plug}}) / l_{\text{disc}} (V > 0) \tag{2.5}$$

Disc concentration is capped at $N_{\text{disc,min}}$ and $N_{\text{disc,max}}$. The local temperature is calculated as:

$$T = (V_{\text{Schottky}} + V_{\text{disc}} + V_{\text{plug}}) \cdot I \cdot R_{\text{th,eff}} + T_0 \tag{2.6}$$

where $R_{\text{th,eff}}$ is the effective thermal resistance and T_0 the ambient temperature.

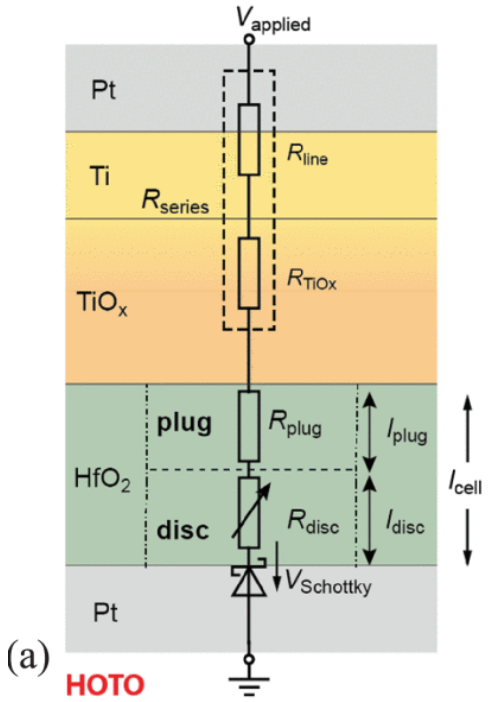


Figure 2.8: Equivalent circuit diagram of the electrical model of the Pt/HfO_2/TiO_x/Ti/Pt (HOTO) device.[3]

3

Related works

There are two existing solutions that have obtained a reduction in read disturb by switching the read current direction. These are discussed in sections 3.1.1 and 3.1.2, after which this is summarised and the research gap is identified in section 3.2.

3.1. Bipolar read

3.1.1. Bipolar read scheme

Shim *et al.* [6] propose a bipolar read scheme for vector-matrix multiply (VMM) neural network with 4-state (2-bit) storage and analog readout. Figure 3.1 shows how alternatively reading with a positive or negative read voltage an be used to keep the device within some small resistance range.

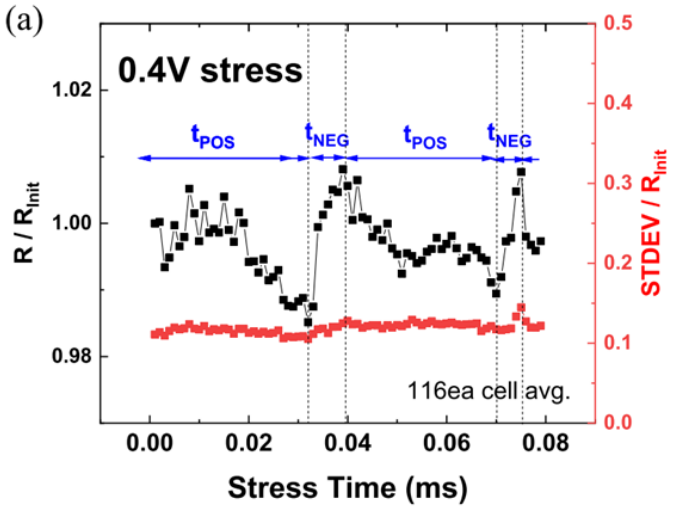


Figure 3.1: Measurement of cell that is kept within 1% of initial resistance by switching the read voltage polarity, as well as standard deviation of 116 cells. [6].

They implement this bipolar read scheme by adding a multiplexer near the sense amplifiers that acts to switch the bitline and sourceline voltage, as shown in figure 3.2.
This does mean that the select transistor is sometimes connected directly to ground, sometimes to V_{dd}. However, this transistor is usually connected to ground to avoid the body effect [1]. In this design, the body effect would occur in one of the sensing directions, creating an asymmetry in sensing.

Simulation of a VMM neural network was performed with this bipolar read scheme. The switching behaviour, that is, when to switch the read current direction, is determined by measuring $t_{pos}(t_{neg})$, the time until a positive (negative) read polarity incurs a 1% resistance change. From this, the switching ratio r_{switch} =

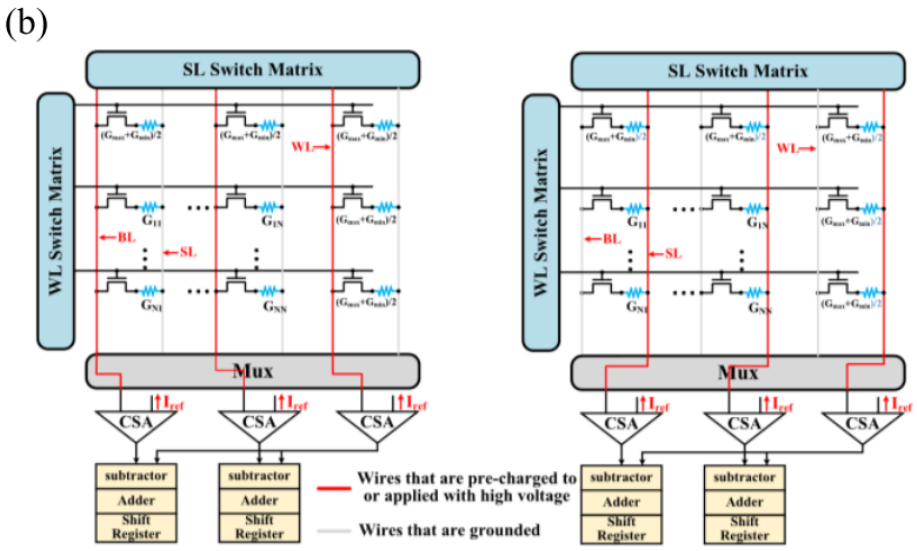


Figure 3.2: Peripheral circuitry showing how bitline and sourceline voltage are switched. [6].

$t_{pos} : t_{neg}$ is calculated. Figure 3.3 shows these for states 2, 3, and 4 (all part of the low-resistance state in this multi-level cell). As state 2 is disturbed the fastest, it is used to determine the switching ratio $r_{\text{switch}} = 3.8 : 1$. This is implemented as $t_{pos} = 5.4$ ms and $t_{neg} = 1.4$ ms. Using this static switching ratio and switching period, a 6x reduction in read disturb is obtained.

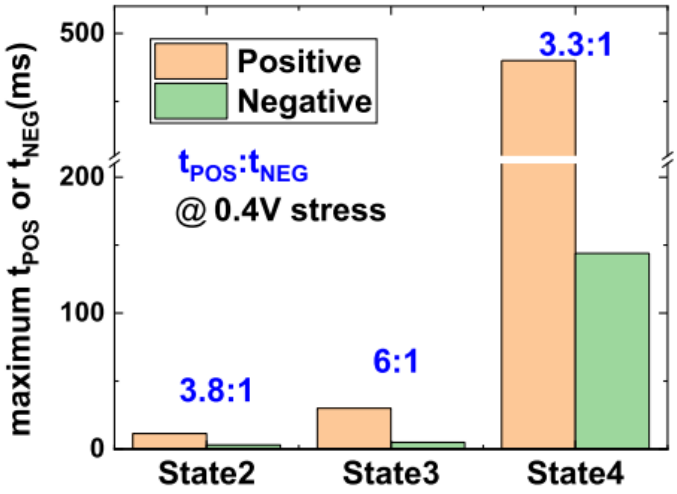


Figure 3.3: Measured time a positive or negative read voltage can be used before 1% resistance deviation is reached, as well as switching ratio $t_{pos} : t_{neg}$. [6].

There are some limiting factors to this approach:

- The switching scheme aims to keep the device in equilibrium, but due to device-to-device variation, some net resistance drift will remain.
- The equilibrium that is sought may be unstable. As the rate of resistance drift depends on the resistance, deviation from the initial resistance could bring it out of the optimal operating range, further increasing resistance drift per cycle.
- Disturb of the HRS state is not considered. It is expected HRS would require a different switching ratio to be brought to equilibrium.

- Due to resistance drift being a function of resistance, a higher switching frequency will lead to less resistance drift within a cycle, which could also improve performance. In addition, this may let a smaller counter be used, saving area.

Addressing these may be key to achieving a further reduction read disturb.

3.1.2. Closed-loop neural network

Yan *et al.* [16] propose a bipolar read scheme in a spiking neural network based on RRAM. They propose choosing the read current direction dynamically based on the output, such that the RRAM device resistance is reinforced towards providing the same output in the future. That is, the column with the maximum output is subsequently sensed as to increase the weights, while all other columns are oppositely sensed to decrease the weights. Hence, a closed loop neural network. A 14.85x reduction in read disturb is achieved in exchange for 1.16% power overhead.
These limiting factors were identified:

- For multilayer neural networks, a larger feedback controller is needed to determine the read direction. Area overhead increases from 2.34% for single-layer to 7.89% for a two-layer design. As the read direction must be calculated from the layer itself and all subsequent layers, the area required to perform this for n layers scales quadratically (as $0.5n(n+1)$, to be precise), making the area overhead quickly untenable as the number of layers increases.
- As noted in the paper, if the network output is incorrect, the next read direction will be suboptimal. This causes some decay of the device state, which eventually leads to read disturb.
- The solution is tailored to an analog neural network, it is unclear if it could also be used for other neural networks.

This paper also mentions ECC as not helpful in this analog use case. ECC could help reduce error in binary/multilevel RRAM – a concern is that read disturb may be correlated between cells, which may cause ECC to fail due to multiple simultaneous errors.

3.2. Summary & research gap

The state-of-the-art in bipolar read has been discussed. Existing solutions achieve a 6x-14.85x reduction in read disturb.
Attempts have been made to keep the device in equilibrium in LRS with a static switching scheme, however this could be an unstable equilibrium. Also, read disturb in HRS was not addressed.
It has also been attempted to reinforce the device state with a dynamic switching scheme, but this solution makes use of internal neural network topology which makes it application-specific. On top of this, the area overhead of determining this dynamic switching makes this solution scales poorly with neural network depth.
Existing research lacks a broader search of the design space of bipolar read schemes.
In this work, a method is shown for determining the sign of net resistance drift for arbitrary switching ratios and resistances. From this, it is predicted whether the device can be reinforced or stabilized with a static switching ratio, promising a more robust way of addressing read disturb.

4

Proposed bipolar read scheme

This chapter concerns the design of the bipolar read scheme, i.e. when the circuit is switched from a positive read current direction to a negative read current direction and vice versa. The effect of the bipolar read scheme is quantified with the switching ratio, which is the ratio between the time the positive and negative read voltage used.
Section 4.1 specifies the objective, reinforcing the device state. Section 4.2 specifies the requirements for reinforcing the device state. Section 4.3 defines the switching ratio, equilibrum ratio and reformulates requirements. Section 4.4 gives two examples of equilibrium ratio graphs and explains how the previously explained theory can be used to show RRAM state can (not) be reinforced. Section 4.5 shows what resistance range was assumed for the undefined state, which will be used later on. Section 4.6 gives the setup for the device-level simulations, where resistance drift under both positive and negative voltage is determined, from which the equilibrium ratio can be calculated. Section 4.7 then shows the equilibrium ratio graphs that result from these simulations and shows where the RRAM state can (not) be reinforced. Section 4.8 briefly discusses the stabilization of the device state, which is a more stringent case than reinforcement. Section 4.9 discusses limitations of these device-level simulations. Section 4.10 then concludes the chapter.

4.1. Objective

As was seen in chapter 2, multiple existing works manage to reduce read disturb in resistive RAM by switching the read current direction, however a further reduction in read disturb is still desired. Existing solutions consider the effects of read disturb at neural network-level, where 70% [16] or 80% [6] recall/inference accuracy is the threshold. In this work, the effect of read disturb is considered at device-level. We define read disturb as the event where the device enters the undefined state between the low-resistance state and high-resistance state.
To this end, the objective is set to **keep the device out of the undefined state by reinforcing HRS and LRS simultaneously**. The undefined state exists between the high-resistance state and low-resistance state. When the device enters this state, read disturb has occurred, which must be prevented. The approach here is to find a bipolar read scheme that has a positive resistance drift in (part of) the high resistance state and a negative resistance drift in (part of) the low resistance state. In this case, resistance drift is away from the undefined state, which is referred to as reinforcing read. It will be investigated if reinforcing read can be achieved with some bipolar read scheme, which would be a reinforcement bipolar read scheme.
After this reinforcement scheme has been investigated, stabilization (keeping the device in a resistance band) will be discussed in section 4.8.

4.2. Requirements for reinforcement bipolar read

To prevent read disturb, the device must be prevented from entering the undefined state. Any device initialized to HRS or LRS will not enter the undefined state if the following requirements are met:

- There exists some resistance interval LRS' or $1'$ extending downwards from $R_{LRS,max}$ where $\frac{\Delta R}{\Delta t} < 0$.
- There exists some resistance interval HRS' or $0'$ extending upwards from $R_{HRS,min}$ where $\frac{\Delta R}{\Delta t} > 0$.

- The resistance intervals HRS' and LRS' are sufficiently large as to prevent them being crossed due to transient effects.

Here $R_{LRS,max}$ ($R_{HRS,min}$) is the maximum (minimum) resistance of the LRS (HRS) state, where it meets the undefined state. Figure 4.1 shows these intervals. Note that $\frac{\Delta R}{\Delta t}$ and dR/dt are used interchangeably in this thesis to mean resistance drift in time.

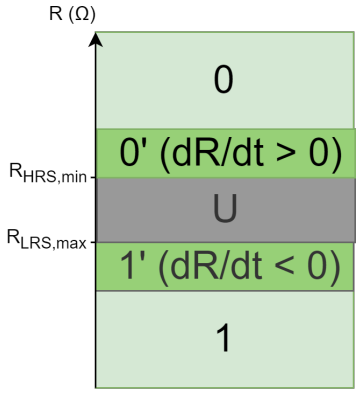


Figure 4.1: Visualization of the 1' and 0' regions that must exist to meet the requirements

If these requirements hold, any device at risk of leaving the LRS (HRS) state will encounter a region where resistance drift is negative (positive), reinforcing it into its original state. Requirement 3 is to protect against transient effects that would have the resistance change rapidly, overpowering the reinforcing effect and crossing into the undefined state.
Note that no requirement is placed on the magnitude of the net resistance drift. However a larger magnitude will make it less likely unaccounted factors would be able to flip the sign of the resistance drift.

4.3. Switching ratio & equilibrium ratio

To start, some definitions must be made.
Let us define the switching ratio as in equation 4.1. Bipolar read entails periodically switching the read voltage polarity.

$$r_{switch} = t_{pos}/t_{neg} \tag{4.1}$$

where t_{pos} (t_{neg}) is the duration for which the positive (negative) read voltage polarity or read current direction is used. t_{pos} and t_{neg} can be an integer multiple of the read period t_{read} (switching the read current direction during the read operation is not considered). This imposes some limits on the values r_{switch} can take. The switching ratio is used in literature but had not yet been defined [6].
Let us also define the switching period in equation 4.2:

$$T_{switch} = t_{pos} + t_{neg} \tag{4.2}$$

Net resistance drift during a switching period is given in equation 4.3:

$$\text{For } V > 0, \ \frac{\Delta R(R,V)}{\Delta t}_{\text{net}} = \frac{\Delta R(R,V)}{\Delta t} * t_{pos} + \frac{\Delta R(R,-V)}{\Delta t} * t_{neg} \tag{4.3}$$

where $\frac{\Delta R(R,V)}{\Delta t}$ ($\frac{\Delta R(R,-V)}{\Delta t}$) are the rate of resistance drift under a positive (negative) voltage for a given resistance and voltage amplitude, respectively. The assumption here is that net resistance drift under bipolar read is a linear function of behaviour under unipolar read. I.e. transient effects from switching the voltage polarity are ignored.
With this, the effect of a bipolar read scheme can be assessed.
For the next part, the following properties of RRAM are exploited:

$$\text{For } V > 0, \ \frac{\Delta R(R,V)}{\Delta t} < 0 \tag{4.4}$$

$$\text{For } V<0,\ \frac{\Delta R(R,V)}{\Delta t}>0 \tag{4.5}$$

Let us start from a naive approach: t_{pos} and t_{neg} chosen such that $R_{net}(R,V)=0$, or a switching ratio chosen such that the resistance drift during the positive and negative read current period cancel out. Then equation 4.3 can be rewritten as:

$$\frac{\Delta R(R,V)}{\Delta t} * t_{pos} = -\frac{\Delta R(R,-V)}{\Delta t} * t_{neg} \tag{4.6}$$

This can be rewritten to equation 4.7:

$$\text{For } V>0,\ r_{eq}(R,V) = t_{pos}/\,t_{neg} = -\frac{\frac{\Delta R(R,-V)}{\Delta t}}{\frac{\Delta R(R,V)}{\Delta t}} \tag{4.7}$$

Where r_{eq} is the equilibrium ratio. When the read current direction is switched at this ratio, the positive and negative resistance drift cancel out, creating an equilibrium. The switching frequency f_{switch} must be sufficiently high as to keep the resistance change small enough that the rate of resistance drift does not change significantly. However switching the read current direction at the equilibrium ratio is not generally sufficient to stabilize the device. This is because it could very well be an unstable equilibrium, in which case residual resistance drift due to perturbation or device variation would not be corrected. In addition, since $\frac{\Delta R(R)}{\Delta t}$ and thus r_{eq} depend on the device resistance, a large change in resistance may lead to a difference between r_{switch} and r_{eq}, increasing net resistance drift even further.
Instead, the equilibrium ratio may be used to meet the requirements set in section 4.2. To this end, let us consider the relationship between the switching ratio and equilibrium ratio as given in equation 4.8:

$$\text{for} f_{switch}\to\infty,\ \frac{\Delta R(R,r_{switch})}{\Delta t}_{net}\begin{cases}<0, & r_{switch}>r_{eq}(R)\\ =0, & r_{switch}=r_{eq}(R)\\ >0, & r_{switch}<r_{eq}(R)\end{cases} \tag{4.8}$$

where $\frac{\Delta R(R,r_{switch})}{\Delta t}_{net}$ is the net resistance drift for a given switching ratio at the given resistance. For a switching ratio greater (smaller) than the equilibrium ratio, a negative (positive) net resistance drift will occur. With this the requirements can be rewritten as:

- There exists some resistance interval LRS' or $1'$ extending downwards from $R_{LRS,max}$ where $r_{switch} > r_{eq}$.
- There exists some resistance interval HRS' or $0'$ extending upwards from $R_{HRS,min}$ where $r_{switch} < r_{eq}$.
- The resistance intervals HRS' and LRS' are sufficiently large as to prevent them being crossed due to transient effects.

For a static switching ratio to simultaneously satisfy requirements 1 and 2 it follows that r_{eq} must be larger in HRS' than in LRS'.

4.4. Equilibrium ratio graph

The equilibrium ratio can be plotted versus the resistance. This equilibrium ratio graph can then be used to analyse net resistance drift for a given switching ratio. In this section, two equilibrium ratio graphs are given to show how these requirements are (not) met in some simplified cases.

Figure 4.2 shows the case where r_{eq} is monotonically increasing and thus r_{eq} is always larger in HRS than anywhere in LRS. It is shown that everywhere left (right) of r_{eq}, $dR/dt > 0$ (< 0), as was shown in equation 4.8. For any choice of r_{switch}, the resistance where $r_{eq} = r_{switch}$ will be a diverging point: for any larger (smaller) resistance than this value, $dR/dt > 0$ (< 0). In this case, by choosing r_{switch} such that $r_{eq} = r_{switch}$ falls in the undefined state, the device is reinforced away from the undefined state in both LRS and HRS. Referring back to the requirements: requirements 1 and 2 are met: $dR/dt > 0$ (< 0) in HRS (LRS), reinforcing these states, preventing read disturb. In fact, the intervals HRS' (LRS') cover all of HRS (LRS). Moreover, in this case no restrictions need are made on the location of the undefined state. For any choice, $r_{eq}(HRS') > r_{eq}(LRS')$.

Conversely, figure 4.3 shows the case where r_{eq} is monotonically decreasing. Thus, r_{eq} is always smaller in HRS than anywhere in LRS. In this case, it still holds that everywhere left (right) of r_{eq}, $dR/dt > 0$ (< 0). However in this case, any switching ratio will create a convergent (asymptotically stable) point at the resistance where $r_{switch} = r_{eq}$, since for any larger (smaller) resistance than this value, $dR/dt > 0$ (< 0). Unfortunately this that no matter whether this is placed in HRS or LRS, the other state will now still suffer resistance drift towards the other state. No static switching ratio can simultaneously restore both LRS and HRS. This applies no matter the location of the undefined state, since r_{eq} is larger everywhere in LRS than anywhere in HRS.

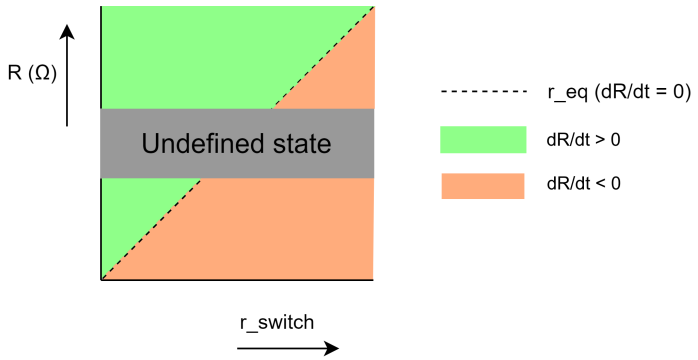


Figure 4.2: Equilibrium ratio graph where r_{eq} monotonically increases with resistance

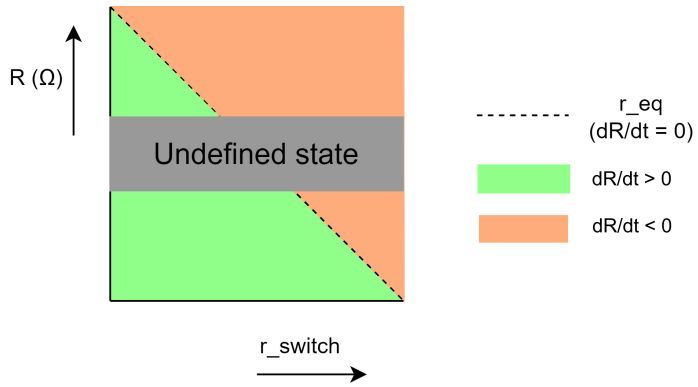


Figure 4.3: Equilibrium ratio graph where r_{eq} monotonically decreases with resistance

4.5. Defining the undefined state

So far, the boundaries of the undefined state ($R_{HRS,min}$ & $R_{LRS,max}$) have not been given a value. Assigning any single value to these will be a simplification, as both writing and reading are variable processes. However the requirements assume their existence, so this must be addressed in some way.
The undefined state has been previously defined as the region between 40% and 60% of the maximum resistance [27]. Here instead the undefined state is defined from write variability. This is based on the assumption that it is convenient for HRS and LRS to cover most of the written values. Figure 2.3 in chapter 2 shows the measured write variability in RRAM states LRS and HRS for the device that the model is based on [3].
From this figure it is estimated $\mu_{SET} = 4$ kΩ, $\mu_{RESET} = 40$ kΩ. $\sigma/\mu_{SET} = 0.05$ and $\sigma/\mu_{RESET} = 0.34$ are given. Here μ_{SET} (μ_{RESET}) are the mean SET (RESET) resistances and σ_{SET} (σ_{RESET}) are the SET (RESET) resistance standard deviation.
Here the choice is made that $R_{HRS,min} = R_{RESET,\mu-2\sigma} = 12.8k\Omega$ & $R_{LRS,max} = R_{SET,\mu+2\sigma} = 4.4k\Omega$. where $R_{SET,\mu+2\sigma}$ ($R_{RESET,\mu-2\sigma}$) is the resistance two standard deviations above (below) the mean SET (RESET) resistances after write. With this choice a large percentage of write resistances will be permitted, as far as bipolar read is considered. $R_{RESET,\mu-3\sigma}$ and $R_{SET,\mu+3\sigma}$ were not chosen due to SET and RESET regions overlapping if that is permitted.

What has not been considered is that a write-verify could tighten the resistance distribution after write further, which would lead to a different choice for HRS and LRS boundaries.

4.6. Device-level simulation setup

From simulation of the RRAM device under both positive and negative stress voltages we can calculate the equilibrium switching ratio for a range of resistances. Simulations were performed in Spice with Spectre version 14.1.0.032 32bit. A TSMC 40nm transistor model was used. The Resistive RAM (RRAM) model used is the JART VCM v1 compact model [3]
A RRAM device starting at R = 78 kΩ (R = 1.9 kΩ) was simulated under a constant stress voltage of + (-)0.5 V until R = 1.9 kΩ (R = 120 kΩ) was reached. This was done at device-level as circuit-level simulation was prohibitively slow to see such large resistance change. The temperature started at T_0 = 293 K but was allowed to vary. From simulation, current I through the RRAM device was obtained under.
The following processing was performed on these simulation results:

- Calculate device resistance $R(t) = V/I(t)$ for both positive and negative voltage case.
- Calculate $\frac{\Delta R(t)}{\Delta t} = \frac{R(t+\Delta)-R(t)}{\Delta t}$ for every time step Δt and both positive and negative voltage case.
- Determine the resistance range for which resistance data exists for both the negative and positive voltage case.
- Calculate $\frac{\Delta R(R)}{\Delta t}$ for both the positive and negative voltage cases in this overlapping resistance range. This is done by interpolating the negative voltage case to find $\frac{\Delta R}{\Delta t}$ at those resistances that occurred in the positive voltage case.
- Calculate the equilibrium ratio r_{eq} as given in equation 4.7.

With the above steps r_{eq} was obtained from R = 1.9 kΩ to R = 78 kΩ. This procedure was repeated for V = +(-) {0.4, 0.3, 0.2, 0.1} V.
In the results, initially it was seen that at V = 0.4 V & V = 0.5 V, the equilibrium ratio varied strongly across very small resistance changes. In some case the equilibrium ratio even went negative. After investigation, it was found that this was caused by oscillations in the temperature and current at timestep scale. Due to calculating the resistance from the current, any change in read current is attributed entirely to a change in device resistance. This caused the current to not monotonically increase (decrease) as expected, ultimately showing up as the sign of the equilibrium switching ratio flipping. Since this effect was not due to a change in device resistance it should be excluded. For V = 0.4 V & V = 0.5 V, where this occurred, this was corrected by sorting the obtained equilibrium ratio into bins of 50Ω, of which the mean is taken.

4.7. Device-level simulation results & discussion

4.7.1. V = 0.5 V

Figure 4.4 shows the simulated equilibrium switching ratio versus the resistance for V = 0.5 V and T_0 = 293 K. Also shown is the sign of net resistance drift as expected from equation 4.8, for any shown combination of switching ratio and resistance.
It can be seen that for r_{switch} = 2.5, resistance drift is positive (negative) in HRS (LRS), reinforcing the device state. So any device in HRS or LRS is expected to be reinforced, preventing it from entering the undefined state (here assumed to be $R_{SET,+2\sigma} < R < R_{RESET,-2\sigma}$).
To look at this more formally, let us look back on the requirements. It can be seen that r_{eq} is always larger in HRS than anywhere in LRS, satisfying requirements 1 & 2. HRS' and LRS' exist, extending upward (downward) from $R_{HRS,min}$($R_{LRS,max}$). No minimum resistance interval is specified in requirement 3, but 100Ω is assumed to be sufficient, which is greatly exceeded here. Thus both HRS and LRS can be reinforced by choosing some r_{switch} between $r_{eq}(R_{LRS,max}) \approx 1.7$ and $r_{eq}(R_{HRS,min}) \approx 3.3$.
r_{switch} = 2.5 is chosen as a compromise between these two factors:

- A larger margin between r_{switch} and r_{eq} allows for a larger variation in r_{eq} between devices while maintaining the same sign of resistance drift and reinforcing behaviour (although device variation was not included in simulations).

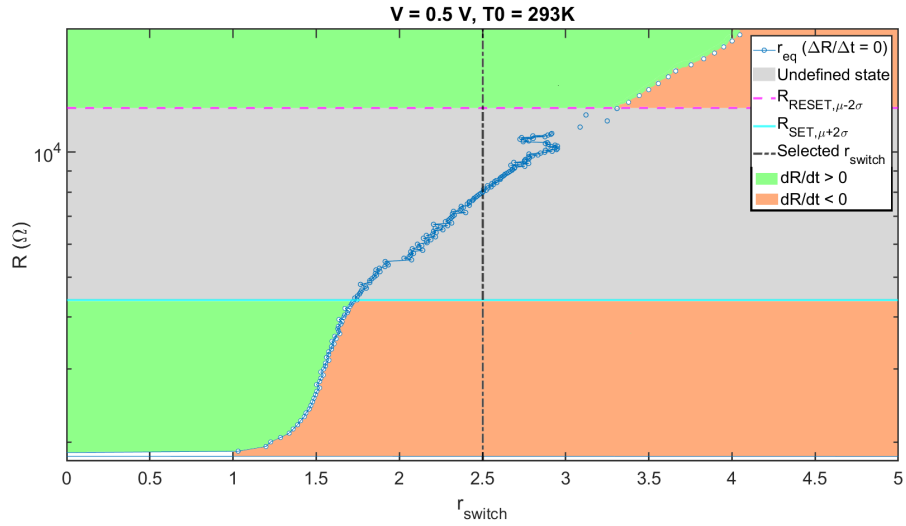


Figure 4.4: Device-level simulation results for V = 0.5 V and T_0 = 293 K

- The switching ratio has some impact on the implementation. I.e. an integer switching ratio can likely be implemented in a simpler way than a simple fraction. A lower numerator (& denominator) is likely simpler to implement than a higher one.

r_{switch} = 2.5 was chosen to give an approximate equal distance between r_{switch} and r_{eq} at both the upper and lower undefined state boundaries, without excessive increase in numerator & denominator. If implementing this is a concern, r_{switch} = 2 or r_{switch} = 3 are also viable, with perhaps weaker state reinforcing and thus lower robustness.

4.7.2. V = 0.4 and V = 0.3 V

For V = 0.3 V and V = 0.4 V, it can be seen in figures 4.6 and 4.5 that for r_{switch} = 2.5 and r_{switch} = 2.75 resistance drift is mostly increasing (decreasing) in HRS (LRS), which reinforces the device state for V = 0.4 V and V = 0.3 V, respectively.
Formally, on some interval HRS' (LRS') exists extending upward (downward) from $R_{HRS,min}$ ($R_{LRS,max}$) where r_{eq} is always larger on HRS' than anywhere on LRS', satisfying the requirements.

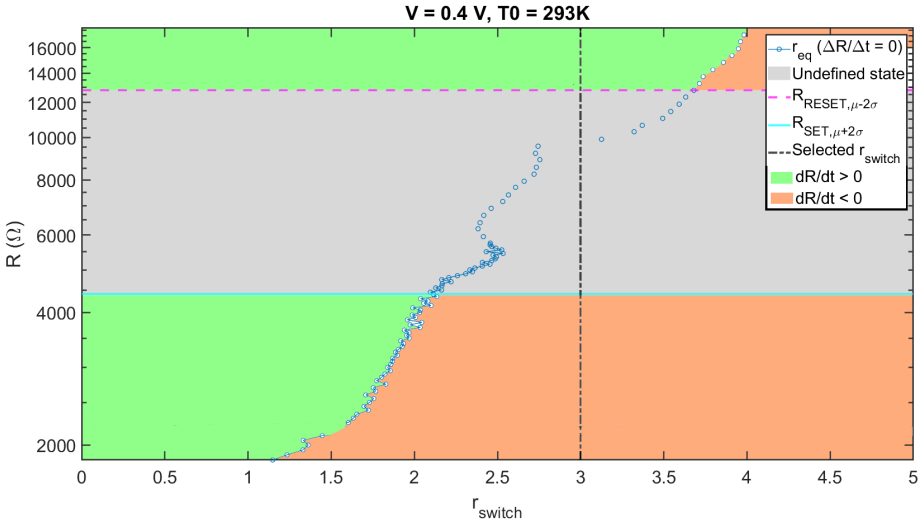


Figure 4.5: Device-level simulation results for V = 0.4 V and T_0 = 293K

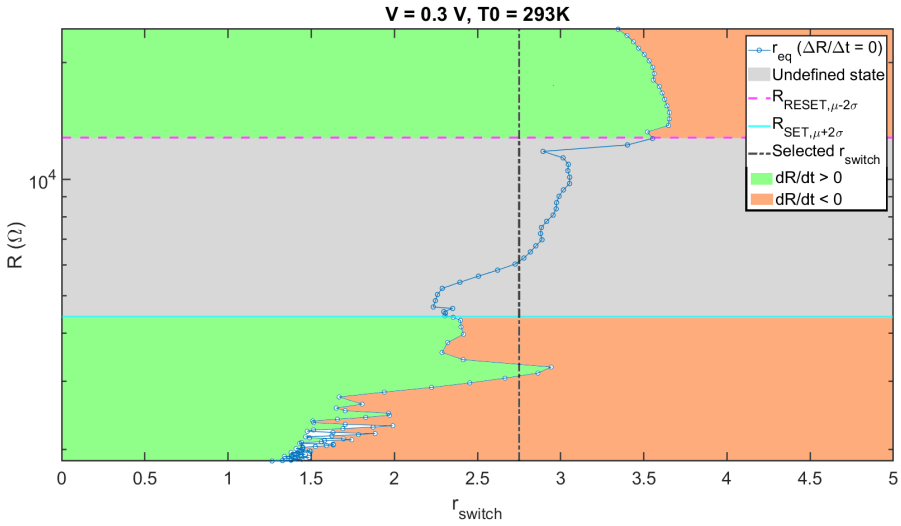


Figure 4.6: Device-level simulation results for V = 0.3 V and $T_0 = 293K$

4.7.3. V = 0.2 V

For V = 0.2 V, figure 4.7 shows us that if $r_{switch} = 2.75$ is selected, resistance drift is negative in HRS, which will decay to the boundary with the undefined state. However, at HRS boundary ($R_{RESET,-2\sigma}$), $r_{switch} \approx r_{eq}$, there is an equilibrium. Given the negative slope of the equilibrium ratio at this point, this is expected to be a stable equilibrium. However it may still be a problem to have the HRS state degrade to the HRS boundary with the undefined state. A reinforcing effect is seen at lower boundary $R_{SET,+2\sigma}$. If instead $r_{switch} = 2.5$ is chosen, the HRS equilibrium will be at a higher resistance, however then the LRS will have positive resistance drift bringing the device to the LRS boundary with the undefined state. Formally, while it holds that $r_{eq}(R_{LRS,max}) < r_{eq}(R_{HRS,min})$, the HRS' interval is very small, as r_{eq} increases beyond $R = R_{HRS,min}$. The device will eventually decay to either the HRS or LRS boundary, depending on the choice of resistance. As this leaves very little sensing margin, reinforcement is deemed not possible.

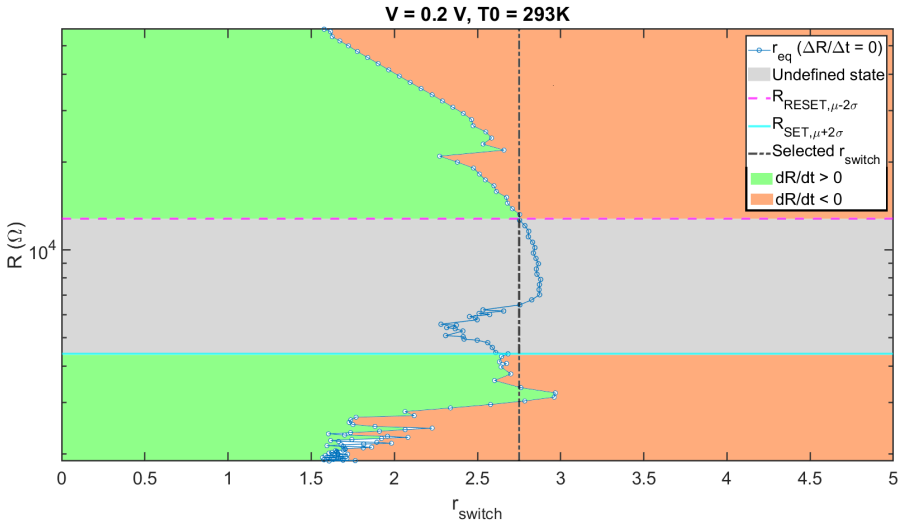


Figure 4.7: Device-level simulation results for V = 0.2 V and $T_0 = 293K$

4.7.4. V = 0.1 V

For V = 0.1 V, figure 4.8 shows that $r_{eq}(R_{LRS,max}) > r_{eq}(R_{HRS,min})$, thus the requirements are not met. No switching ratio can simultaneously reinforce both LRS and HRS at the chosen resistance boundaries. $r_{switch} = 2.25$ is chosen, resulting reinforcing behaviour at the LRS boundary, while there is a convergent point at the

HRS boundary. While this is a stable equilibrium, this means from any HRS resistance decay to the HRS boundary is expected, which leaves very little sensing margin. Reinforcement is deemed not possible.

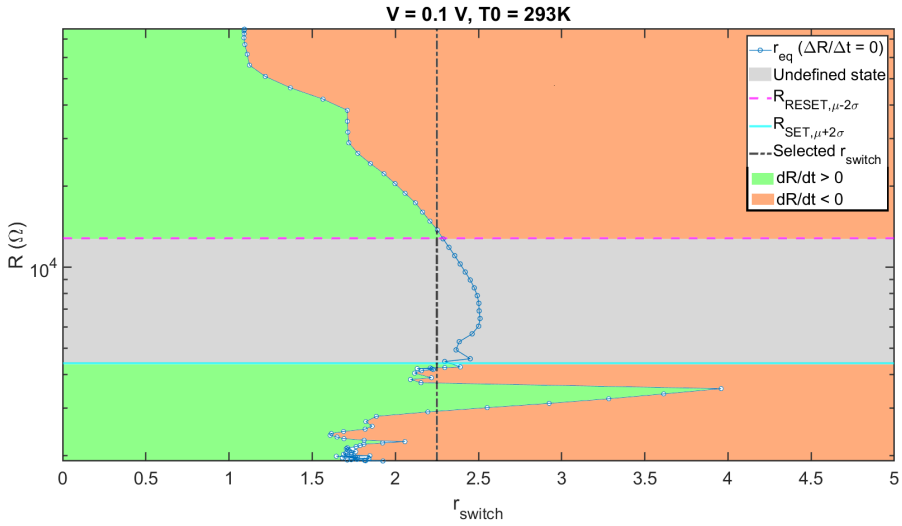


Figure 4.8: Device-level simulation results for V = 0.1 V and $T_0 = 293K$

4.7.5. Overview table

An overview of the device-level results is given in table 4.1. Net $\Delta R/\Delta t$ is shown as ↑ increasing, ↓ decreasing or - inconclusive and colored where applicable to indicate a reinforcing effect. Resistance values correspond to undefined state boundaries $R_{LRS,max} = 4.4\ k\Omega$ & $R_{HRS,min} = 12.8\ k\Omega$.

$V(V)$	0.5		0.4		0.3		0.2		0.1	
$R(k\Omega)$	4.4	12.8	4.4	12.8	4.4	12.8	4.4	12.8	4.4	12.8
r_{eq}	1.7	3.3	2.1	3.7	2.3	3.5	2.6-2.7	2.75	2.3	2.3
Selected r_{switch}	2.5 (5:2)		2.5 (5:2)		2.75 (11:4)		2.75 (11:4)		2.25 (9:4)	
Net $\Delta R/\Delta t$	↓	↑	↓	↑	↓	↑	↓	-	-	-
Reinforcement of HRS & LRS	✓		✓		✓					

Table 4.1: Overview of device-level simulation results.

Putting aside the undefined state as chosen here, some other interesting conclusions can be drawn. At V = 0.5 V, the graph closely resembles the ideal behaviour ($r_{eq}(R_2) > r_{eq}(R_1)$ if $R_2 > R_1$) as given in figure 4.2. For most other choices of undefined state, the device can still be reinforced away from it given the right choice of r_{switch}. As the voltages decrease, more non-idealities appear until finally at V = 0.1 V the graph more closely resembles the anti-ideal case for reinforcement.

4.7.6. Temperature variation

Figure 4.9 compares the equilibrium ratio at $T_0 = 293K$ and $T_0 = 353K$ for V = 0.3 V. The original $r_{switch} = 2.75$ does not meet the requirements for this elevated temperature anymore, as $r_{switch} \approx r_{eq}$ at $R_{HRS,min}$. It can be seen that if we take $r_{switch} = 2.5$, the conditions can still be met.

4.8. Stabilization

Let us also briefly consider the stabilization of the RRAM device to some resistance band. Figure 4.10 illustrates what kind of resistance drift behaviour would be needed to stabilize both HRS and LRS. As before in figure 4.2, the device state is reinforced away from the undefined state. However in this case there are nega-

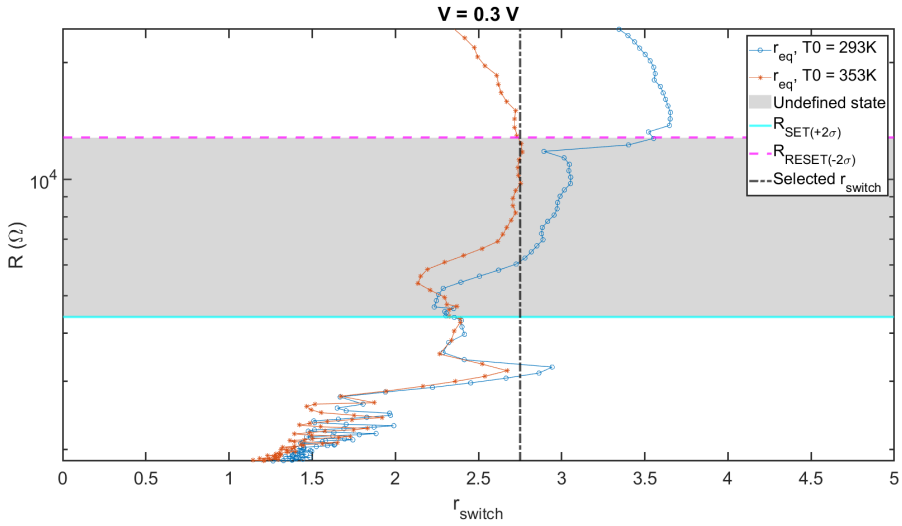


Figure 4.9: Device-level simulation results for V = 0.3 V at varying temperatures

tively sloped crossover point in HRS and LRS, which are asymptotically stable. HRS and LRS resistance would converge on these points, respectively. Due to this, the deep HRS and LRS states are avoided. Put another way:

- dR/dt < 0 in HRS near deep HRS, keeping the device away from this state.
- dR/dt > 0 in HRS near the undefined state, keeping the device away from this state.
- dR/dt < 0 in LRS near the undefined state, keeping the device away from this state.
- dR/dt > 0 in LRS near deep LRS, keeping the device away from this state.

The deep states have been described as a fault mode [20][21]. Comparing this ideal figure to those obtained from simulation, none exhibit the desired characteristic for stabilization of the HRS and LRS away from the undefined state and both deep states. The V = 0.2 V graph in figure 4.7 somewhat resembles it, but it was concluded before that neither $r_{switch} = 2.5$ or $r_{switch} = 2.75$ would keep the device sufficiently away from the undefined state.

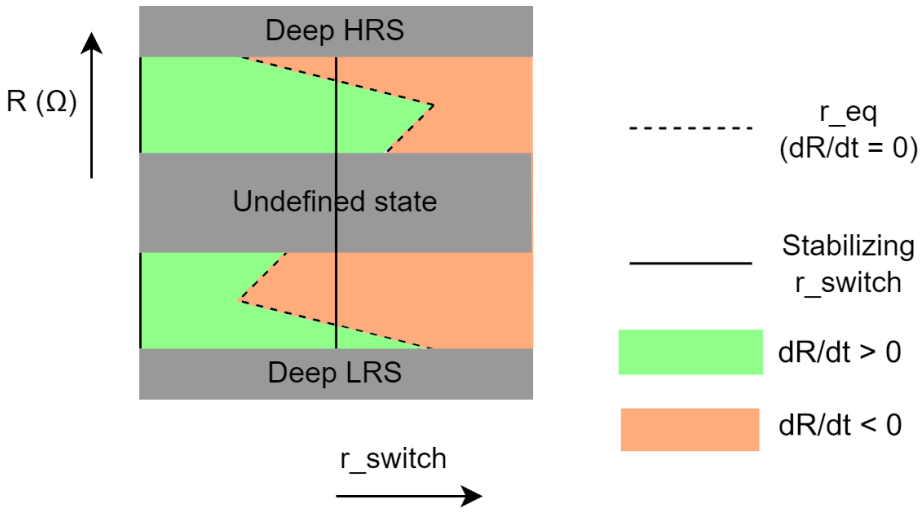


Figure 4.10: Concept of equilibrium ratio graph that would stabilize the device to some point in HRS and LRS

4.9. Discussion & limitations

It was assumed there are no transient effects from switching the read voltage polarity, however these still may exist. One case has been identified: in the device model itself the voltages and currents determine the temperature of the next time step (see equation 2.6). This creates a discrepancy between net resistance drift as predicted here from positive and negative polarity read simulation, compared to net resistance drift from directly simulating bipolar read.
These simulations were performed at device-level and were used to predict device behaviour and select a switching ratio for circuit-level evaluation. Circuit-level simulation results are provided in chapter 6.

4.10. Summary

Requirements were specified for the RRAM resistance drift behaviour for which both LRS and HRS can be reinforced with a static voltage polarity switching ratio. Device level simulation was performed to determine this net resistance drift. From this the equilibrium ratio graphs were calculated. From these predictions are made for the ability to reinforce or stabilize RRAM.
Device-level simulations predict that for V = 0.5, 0.4 and 0.3 V, a static switching ratio exists for which both LRS and HRS are reinforced, with r_{switch} = 2.5, 2.5 and 2.75, respectively. For V = 0.2 V and V = 0.1 V, reinforcement does not seem possible. Stabilization of the device to and HRS and LRS resistance band was also considered, but these device-level results predict no such scheme exists.

5

Proposed circuit design

Bipolar read is investigated with a small-scale test circuit. Section5.1 gives an overview, block diagram and circuit diagram of this circuit. Section 5.2 explains how the direction switching is implemented. Section 5.3 and section 5.4 explain the write and read operations, respectively.

5.1. Overview

Figure 5.1 shows the test circuit, with just one Resistive RAM cell. The direction switching circuit located at the top and bottom allows for changing the current direction through the cell through control signal D, as seen in figure 5.2. This effectively switches the source line (SL) and bit line (BL).

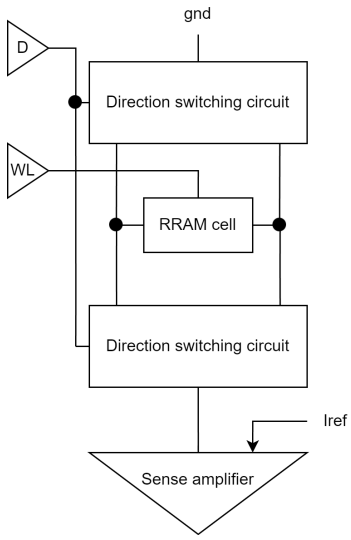


Figure 5.1: Block diagram of circuit with 1T1R cell, direction switching circuitry and sense amplifier

The reference circuit is shown in Figure 5.3. This uses a resistor as reference. The direction switching circuit and a select transistor are included to make the reference case more similar to the measured case.

Figure 5.4 shows the circuit diagram. The different parts and functions of this circuit will be described in subsequent sections.

5.2. Direction switching

At the top and bottom of the array column (here just one cell), the direction switching transistors are located. When D = 1, the positive current path is opened by turning on transistors MN9 & MN11 (and equivalently

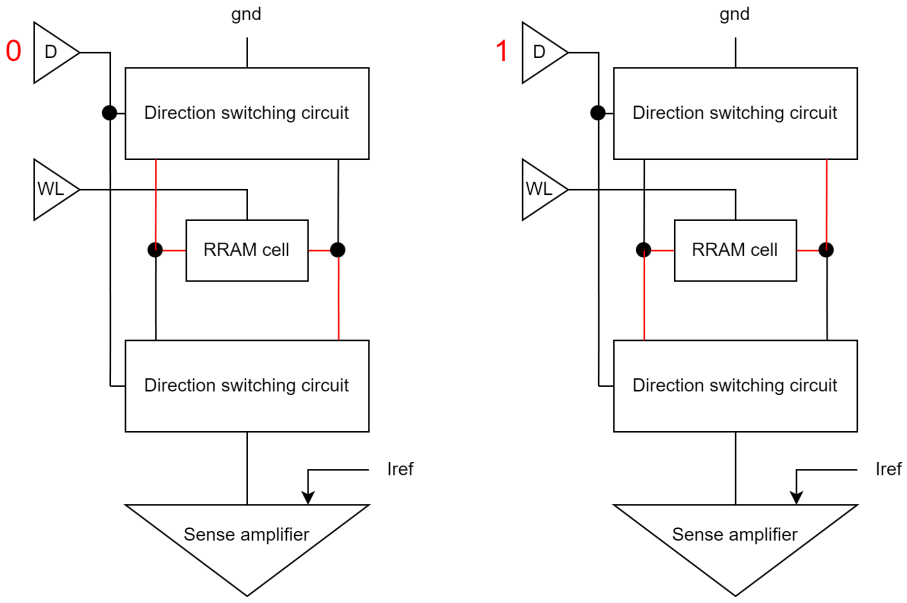


Figure 5.2: Block diagram of circuit with the alternate current paths shown in red.

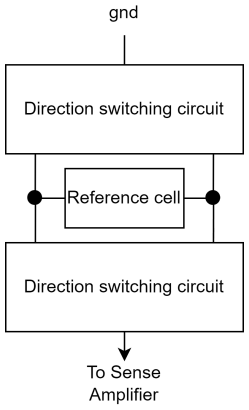


Figure 5.3: Reference circuit.

MN8 & MN10). When D = 0, the negative current path is opened by turning on transistors MN4 & MN13 (and equivalently MN5 & MN12).

5.3. Write operation

By enabling `wr_col`, and powering the wordline, RRAM1 can be written. When signal D is 1 (0), the device can be SET (RESET) by turning on `wr_col`. Note that due to the bipolar nature of write, the select transistor will incur the body effect during one of these. The RRAM device is connected such that the body effect occurs on the SET operation, so this is avoided on the slower RESET [28].

5.3.1. Transistor sizing

Transistor widths are given in Table 5.1.

For transistors in the write path, the required equivalent transistor width is determined using the test circuit shown in Figure 5.5. Using this it is determined W_{eq} = 450 nm is sufficient for a sub-15 μs reset. The 4 transistors in the write path are thus sized for an equivalent width of 450 nm. $1/W_{eq} = 1/W_{MN14} + 1/W_{MN9} + 1/W_{MN7} + 1/W_{MN11} = 1/5400 + 1/5400 + 1/600 + 1/5400 = 1/450$ satisfies this, with MN4,MN5 and MN8 through MN13 also 5400 nm wide to account for other write paths or symmetry.

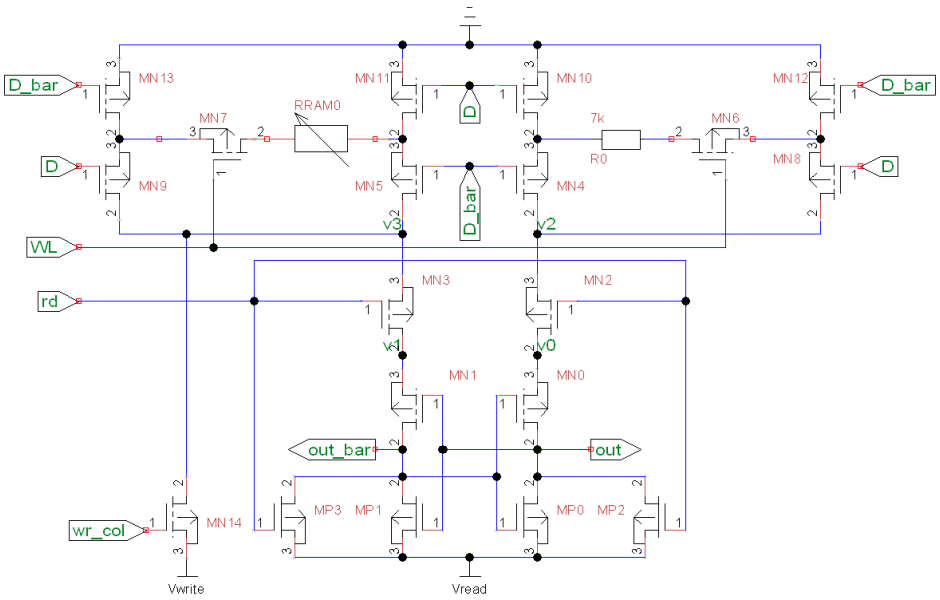


Figure 5.4: Diagram of proposed circuit, showing the RRAM cell, reference current generator, direction switching circuit and pre-charge sense amplifier

Transistor name	Type	Width (nm)	Length (nm)
MP0-MP3	PMOS	120	40
MN0-MN1	NMOS	240	40
MN2-MN3	NMOS	120	40
MN4-MN5	NMOS	5400	40
MN6-MN7	NMOS	600	40
MN8-MN14	NMOS	5400	40

Table 5.1: Transistor widths

Note that the width of select transistors MN6 & MN7 is kept small at the expense of others since when scaling up to an array there is a select transistor in every cell, while the direction switching circuit would be replicated once per column at most.

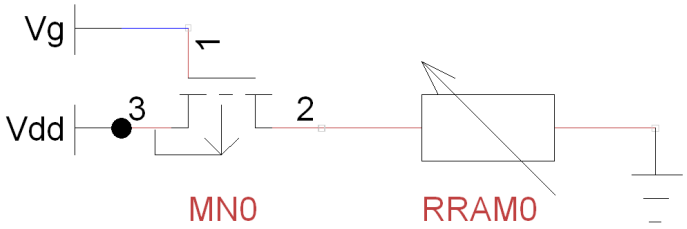


Figure 5.5: Test circuit for determining transistor width

5.4. Read operation

When signal `D` is logical 1 (logical 0), a positive or reverse read (negative or forward read) can be performed. The read operation itself is performed with a pre-charge sense amplifier [29]. While `rd` is logical 0, the following occurs:

1. Transistors MP2 and MP3 precharge nodes `out` and `out_bar`
2. This turns off MP1 and MP3 and turns on MN0 and MN1

3. Nodes v0 and v1 are precharged

Then, the read operation is started by enabling `rd`, beginning the following sequence:

1. MP2 and MP3 are turned off, stopping precharge
2. The charge on v0 and `out` (v1, and `out_bar`) starts draining into the RRAM cell/column (the reference circuit)
3. If the RRAM device is in in high resistance state, the charge on `out_bar` drains slower than the charge on `out`.
4. `out` voltage is the first to fall to the threshold voltage of MN1 & MP1. MN1 is turned off to stop the charge draining, while MP1 turns on to raise `out_bar` voltage again to logical 1.
5. `out` voltage drains further towards logical 0, aided by increasing `out_bar` voltage switching MN0 fully on and MP3 fully off.
6. `out` is logical 0, which corresponds to the high-resistance state. The read operation is successful.

Where the RRAM device to be in the low-resistance state, `out_bar` would instead fall to the threshold voltage first. Then `out` goes to logical 1, which corresponds to this LRS state.

5.4.1. Decision threshold

By placing the decision threshold in the region where the distributions have little to no overlap, the two states can be best distinguished. In chapter 4 the undefined state was taken to be between $R_{SET,\mu+2\sigma} = 4.4k\Omega$ and $R_{RESET,\mu-2\sigma} = 12.8k\Omega$. Again, from figure 2.3 in chapter 2 it is estimated that $\mu_{SET} = 4$ kΩ, $\mu_{RESET} = 40$ kΩ. $\sigma/\mu_{SET} = 0.05$ and $\sigma/\mu_{RESET} = 0.34$ are given. Here μ_{SET} (μ_{RESET}) are the mean SET (RESET) resistances and σ_{SET} (σ_{RESET}) are the SET (RESET) resistance standard deviation.
This could be taken further to have the decision threshold where HRS and LRS are equally probable, which would be at $R_{SET,\mu+2.61\sigma} = R_{RESET,\mu-2.61\sigma} = 4.52$. However this leaves an extremely small sensing margin between mean LRS resistance and the decision threshold, so $R_t = 7k\Omega$ is taken instead, which is implemented by using a reference resistor $R_{ref} = 7k\Omega$.

5.5. Summary

The test circuit consists of one RRAM cell, a reference, direction switching circuitry and a pre-charge sense amplifier. Write operations (SET & RESET) and bipolar read operations (reverse & forward) can be performed in this circuit.

6

Results

This chapter contains the results of this thesis. In section 6.1, the general setup is covered. Section 6.2 covers setup and results of writing the RRAM device. Section 6.3 covers setup and results of reading the RRAM device in both read current directions. Sections 6.4 and 6.5 covers setup and results, respectively, of read disturb and the effectiveness of the bipolar read scheme. Section 6.6 discusses these results and section 6.6.1 their limitations.

6.1. Setup

Simulations were performed with the circuit shown in figure 5.4. Models & initial parameters are given in Table 6.1. Table 6.2 shows the signals used in read & write.

6.2. RRAM write operation

This section covers the results of simulating write (SET and RESET) the RRAM device.
The write functionality of the circuit was simulated. Write voltage V_{write} = 1.1V and supply voltage V_{DD} = 1.6V were used, to allow NMOS to perform pull-up ($V_G = V_{DD} > V_{write} + V_t$). Write is started by enabling column 1 write control signal `wr_col1` from t = 3 ns with $t_{rise} = 100ps$.
Two scenarios were simulated: 0w1 (1w0) (SET (RESET) operation on RRAM device in HRS (LRS) state, respectively).

Simulator	Spice language in Spectre (version 14.1.0.032 32bit)
CMOS transistor model	TSMC 40 nm low V_t 1.1 V
Resistive RAM model	JART VCM v1 compact model [3]
T_0	293K
Initial HRS resistance (write & unipolar read)	78 kΩ (via $N_{disc,init} = 4 * 10^{24}$)
Initial LRS resistance (write & unipolar read)	1.9 kΩ (via $N_{disc,init} = 1 * 10^{27}$)
Initial HRS boundary resistance (bipolar read)	12.8 kΩ
Initial LRS boundary resistance (bipolar read)	4.4 kΩ
Further processing	Matlab R2022b or R2024a

Table 6.1: Overview of simulation models and parameters

	V_{write}	V_{read}	Wr_{col}	D	$\bar{D}$	WL
SET	V_{dd}	GND	1.6 V	1.6 V	GND	1.6 V
RESET	V_{dd}	GND	1.6 V	GND	1.6 V	1.6 V
Positive read	GND	0.5 V	GND	V_{dd}	GND	V_{dd}
Negative read	GND	0.5 V	GND	GND	V_{dd}	V_{dd}

Table 6.2: Read and write signals and voltages. $V_{dd} = 1.1V$.

Figures 6.1 and 6.2 show the output of these simulations. Write current and RRAM resistance are shown. It can be seen that the device is successfully written with $t_{SET} \approx 0.1\mu s$ and $t_{RESET} \approx 16\mu s$. These speeds are comparable with literature, where modal $t_{SET} \approx 0.1\mu s$ and $t_{RESET} \approx 10\mu s$ were shown [1].

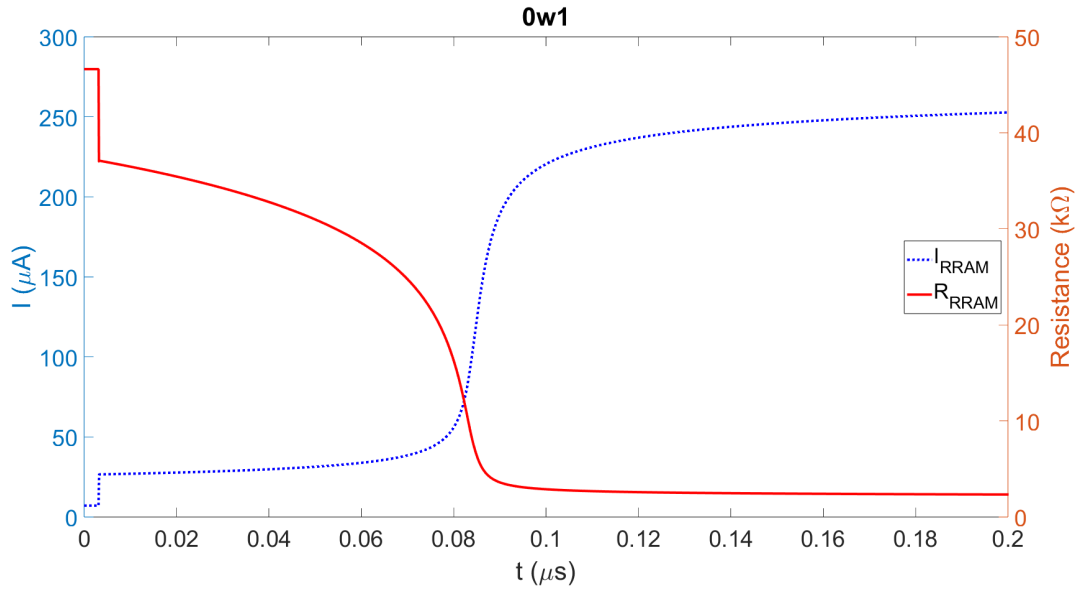


Figure 6.1: Simulation of RRAM 0w1 (SET while OFF)

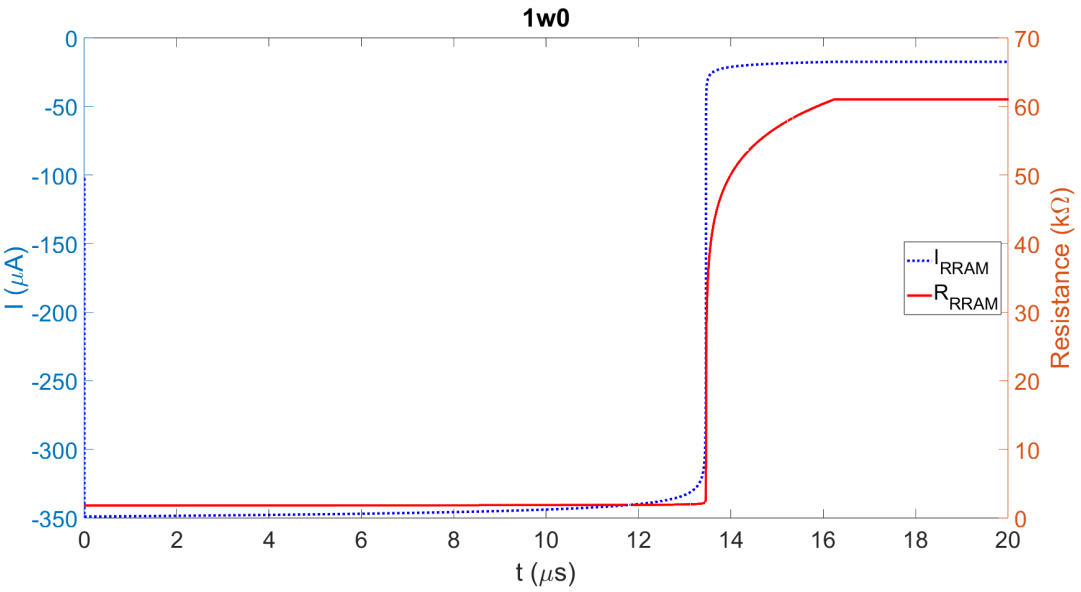


Figure 6.2: Simulation of RRAM 1w0 (RESET while ON)

6.3. RRAM read operation

This section covers the simulation setup and results of reading the RRAM device with both a positive and negative read current.

The read functionality of the circuit was simulated. Read voltage $V_{read} = 0.5V$ and supply voltage $V_{DD} = 1.1V$ were used, expect read control signal `rd`, which uses V_{read} as its supply. Two read operations were performed. Between these operations, the read current direction was switched using the direction switching circuit. At $t = 5.1ns$, the read current direction is switched by disabling (enabling) control signal `D` ($\overline{D}$) with fall time (rise time) $t_{rise} = t_{fall} = 0.1ns$ and $t_{max} = 3ns$.
Figures 6.3 and 6.4 show that for the device in ON (OFF) state, output signal `out` is 1 (0) as expected for both sensing operations. It is desired for either read current direction to be symmetric, but it can be seen that for both 1r1 and 0r0 the second read operation corresponding to `D` = 0 reaches its final value faster. This is expected to be due to the body effect of the select transistor slowing down the reverse read case, which is `D` = 1 or the positive read current/read voltage polarity.

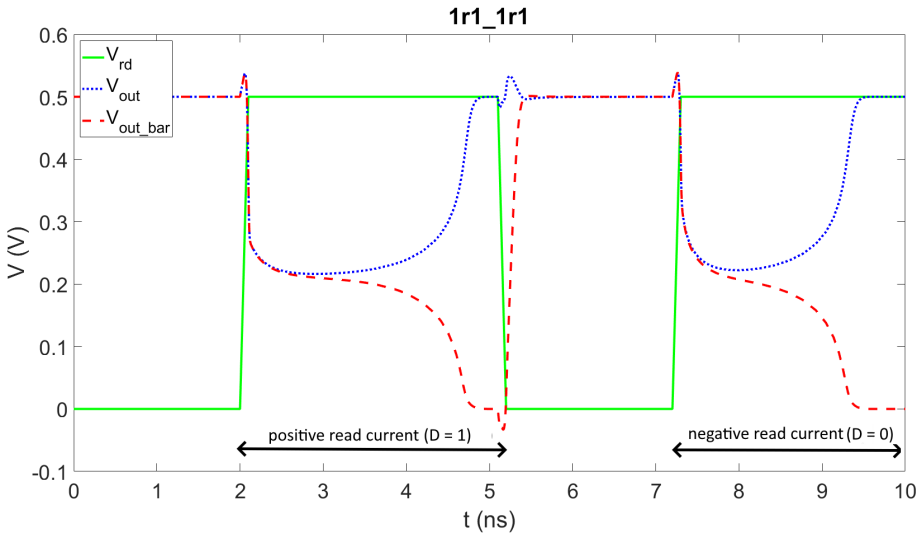


Figure 6.3: Bipolar read of ON state

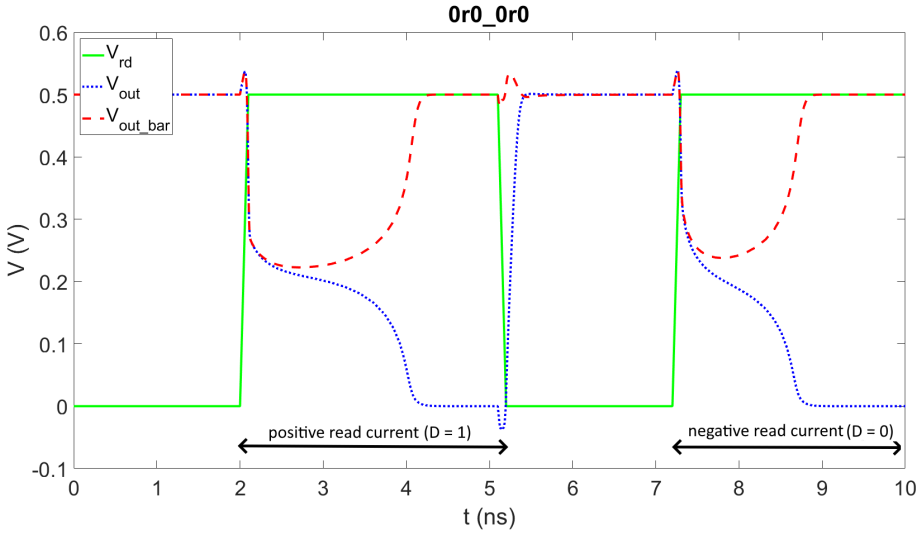


Figure 6.4: Bipolar read of OFF state

6.4. Read disturb setup

To estimate the read disturb behaviour of the circuit, the RRAM resistance drift under periodic read was simulated for both LRS and HRS. Read voltage $V_{read} = 1.3V$ and supply voltage $V_{DD} = 1.1V$ were used. The read voltage was chosen such that the effective read voltage across the 1T1R cell $\Delta V_{read,eff} \approx 0.5V$. This effective read voltage was chosen for two reasons. First, a larger read voltage will require less simulation time for the same resistance drift. Secondly, V = 0.5 V was predicted to be the best candidate for reinforcement bipolar read in the device-level analysis. The read control signal `rd` was enabled periodically with $t_{rise} = 10ps$, $t_{max} = 3ns$, $t_{fall} = 10ps$ and read period $T_{read} = 5ns$. Stop time $t_{final} = 20\mu s$ for a total of 4000 read cycles.
To simulate bipolar read, a switching ratio of $r_{switch} = 5:2$ was used, as was found in chapter 4 for $V_{read} = 0.5V$. A *m:n* switching ratio is implemented by reading with the positive voltage polarity for $t_{pos} = m * T_{read}$, followed by reading with the negative voltage polarity for $t_{neg} = n * T_{read}$. This was compared to the base unipolar cases of always reading with the positive (negative) read voltage polarity, corresponding to reverse (forward) read (see section 2.2).
These simulation were carried out for both HRS and LRS. RRAM resistances were initialized to the boundary with the undefined state ($R_{HRS,min} = 12.8k\Omega$ and $R_{LRS,max} = 4.4k\Omega$, see section 4.5).
The circuit was altered by replacing the reference resistance with another RRAM device. With two RRAM devices now available, one was initialized to HRS while the other was initialized to LRS. This optimization allowed for obtaining HRS and LRS results simultaneously.

6.5. Read disturb results

Figures 6.5 and 6.6 show the resistance drift at the boundary of the HRS and LRS state, respectively. Tables 6.3 and 6.4 list derived results for HRS and LRS, respectively. These are the cumulative drift, average drift per cycle and drift reduction relative to positive and negative read.

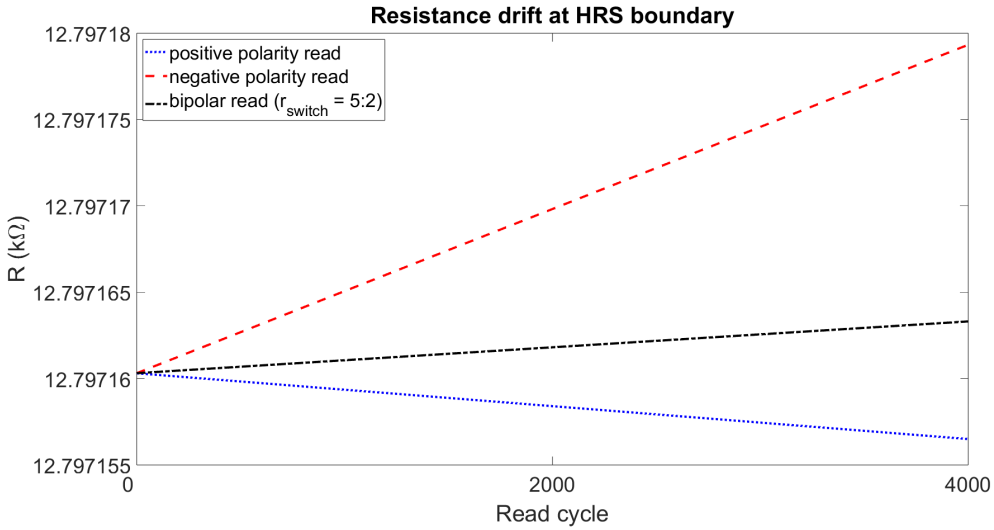


Figure 6.5: Resistance drift at HRS boundary for bipolar read compared to both baseline unipolar read cases

Read scheme	Positive polarity	Negative polarity	Bipolar read ($r_{switch} = 5:2$)
Cumulative ΔR ($m\Omega$)	-3.81	19.0	3.01
$\Delta R/\Delta t$ (mΩ/cycle)	-0.952	4.76	0.751
Drift reduction w.r.t. positive polarity			-1.3
Drift reduction w.r.t. negative polarity			6.3

Table 6.3: Derived metrics from resistance drift simulation at HRS boundary, comparing positive polarity read, negative polarity read and bipolar read

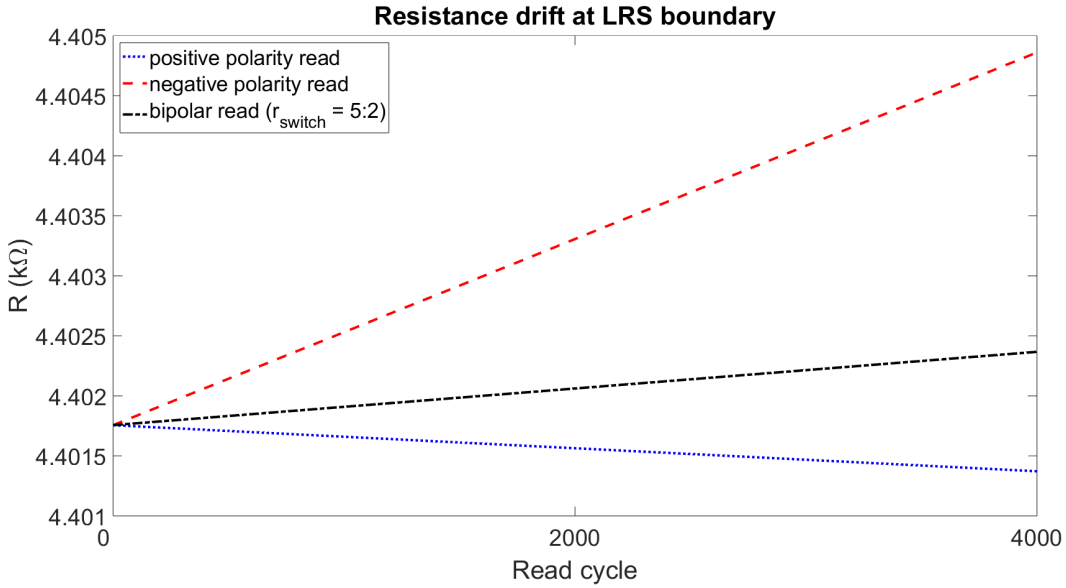


Figure 6.6: Resistance drift at LRS boundary for bipolar read compared to the baseline unipolar read cases

Read scheme	Positive polarity	Negative polarity	Bipolar read ($r_{switch} = 5:2$)
Cumulative ΔR (Ω)	-384	3105	612
$\Delta R/\Delta t$ (mΩ/cycle)	-95.9	776	153
Drift reduction w.r.t. positive polarity			-0.63
Drift reduction w.r.t. negative polarity			5.1

Table 6.4: Derived metrics from resistance drift simulation at LRS boundary, comparing positive polarity read, negative polarity read and bipolar read

6.6. Discussion

RRAM write and unipolar read have been discussed in their respective sections. This section will discuss the bipolar read results in-depth.

To interpret the bipolar read results, recall that when in LRS (HRS), a resistance decrease (increase) is reinforcing (destructive). Figure 6.5 shows that for $r_{switch} = 5:2$, resistance drift is reinforcing at the HRS boundary. Figure 6.6 shows that at the LRS boundary, destructive resistance drift can be observed, while the device-level analysis predicted reinforcing behaviour. A 5.1x reduction in destructive resistance drift is obtained in this case compared to unipolar negative/forward read, which is the conventional unipolar read polarity.

Recall that $r_{switch} = 5:2$ was found in chapter 4, where it was predicted that at both the LRS and HRS boundary with the undefined state, the resistance drift would be reinforcing. The prediction made at device-level are thus not representative of circuit-level behaviour. The expected main culprit is that the select transistor of the cell was not included in at device-level while it is present at circuit-level. This transistor suffers from the body effect with a positive read voltage, which will manifest as a voltage drop across the transistor. This in turn causes a lower voltage across the RRAM device in the positive read voltage case and a lower resistance drift. The immediate effect of this is a net resistance drift towards the HRS state from the LRS state boundary, which brings the device into the undefined state.

In light of this, it was considered if a different switching ratio might still reinforce both HRS and LRS as desired. This is the case if:

$$\frac{\Delta R_{net}}{\Delta t}_{\text{HRS}} = r_{switch} * \frac{\Delta R_{pos,HRS}}{\Delta t} + \Delta R_{neg,HRS} > 0 \tag{6.1}$$

and

$$\frac{\Delta R_{net}}{\Delta t}_{\text{LRS}} = r_{switch} * \frac{\Delta R_{pos,LRS}}{\Delta t} + \Delta R_{neg,LRS} < 0 \tag{6.2}$$

Taking these $\Delta R/\Delta t$ values from tables 6.3 and 6.4 , it can be calculated that equation 6.1 holds for $r_{\text{switch}} < 5$, while equation 6.2 holds for $r_{\text{switch}} > 8.1$. This can not be simultaneously satisfied, so no switching ratio can

reinforce both HRS and LRS at the boundary with the undefined state as chosen here.

6.6.1. Limitations

A reinforcement bipolar read scheme can only keep the RRAM undefined state. Reinforcing the HRS/LRS state may eventually put the device into a deep state, however [20][21]. For designs that rely on keeping the device in some resistance band, this may not be suitable. In addition, reinforcement is only sufficient if the RRAM cell stores a binary value - if multiple states are stored in HRS or LRS, stabilization within the resistance range of that state is required instead.
These results show only a small ΔR, due to simulation time constraints. The 5.1x reduction in resistance drift does not necessarily correspond to a 5.1x reduction read disturb.
The device model used is a compact model, with some concessions made to make it suitable for circuit simulations.
The replacement of the reference resistance with a RRAM device of opposite state in bipolar read simulations (done to reduce simulation time) has changed the duration and shape of the read operation.
Device and temperature variation, read noise and diffusion have not been taken into account. Device variation has been added to the Jart VCM model in [30]. Read noise and diffusion may also affect the read disturb behaviour, models for those have been described in [31] and [32] , respectively.

7

Conclusion

It was investigated if a bipolar read scheme exists that can simultaneously reinforce the HRS and LRS states in RRAM. That is, a positive resistance drift in HRS and negative resistance drift in LRS. This with the goal of preventing read disturb, where accumulated resistance drift from repeated read operations put the device into the undefined state.
RRAM resistance drift behaviour was characterised in a device-level simulation, from which net resistance drift for a given ratio between positive and negative read voltage polarities is calculated. These simulations predict that at V = 0.5, 0.4 and 0.3 V, a static switching ratio is able to reinforce both HRS and LRS, that is, increase HRS resistance and decrease LRS resistance, with r_{switch} = 2.5, 2.5 and 2.75, respectively. This is possible by exploiting the fact that resistance drift depends on both resistance and read voltage polarity, allowing for HRS and LRS to incur resistance drift of opposite signs. For V = 0.2 V and V = 0.1 V, device-level simulations predict that HRS and LRS can not both be reinforced simultaneously with a single static switching ratio. Stabilization of RRAM to some resistance band was also investigated, keeping the device out of deep HRS, deep LRS and undefined state, is predicted to not be possible with a static switching ratio.
The reinforcement bipolar read scheme was evaluated for V = 0.5 V on a test circuit with a single RRAM cell, direction switching circuit and sense amplifier. Results showed that only the HRS is reinforced for the found switching ratio, while the LRS is not, at $R_{HRS,min}$ = 12.8$k\Omega$ and $R_{LRS,max}$ = 4.4$k\Omega$. The device-level prediction does not hold at circuit level. It is expected this discrepancy mainly comes from the body effect of the select transistor, which occurs for the positive read voltage. From circuit-level unipolar read results it was determined that no switching ratio exists that can reinforce both HRS and LRS state boundaries as chosen here. However, a 5.1x reduction in net resistance drift compared to the typical (negative) unipolar read was still obtained.

7.1. Future work

Net resistance drift and the existence of a reinforcement bipolar read scheme or stabilizing bipolar read scheme should be investigated at circuit-level for a wider resistance range. This could be done for arbitrary switching ratios by estimating net resistance drift under bipolar read from the resistance drift in unipolar read, as in this work. Alternatively, some selection of switching ratios can be directly simulated. Simulation time can be kept feasible by determining the net resistance drift only at select resistances and interpolating this.
While the device-level behaviour was not well predictive of circuit-level behaviour where a select transistor is present, it might be a better predictor for crossbar arrays, where the select transistor is not present.
A direct challenge to the usefulness reinforcing the device state, is the existence of deep state faults. The reinforcement scheme by nature causes resistance drift towards the deep states. If RRAM device characteristics permit, a stabilizing bipolar read scheme might still exist, which can keep the device in an LRS and HRS band, away from undefined and deep states. Otherwise, applications should be sought where deep states are permissible.
Beyond this, a different voltage could be used for the positive and negative read operation, opening new ways to shape net resistance drift.

By taking into account device variation, temperature variation, read noise, diffusion and array effects, a step closer to applicability can be taken. For device variation, Monte Carlo simulations can be used. Measurements should also be considered.
To combat the effect of temperature variation, it may be possible to dynamically adjust the switching scheme to the temperature.
It might also be of interest to see if bipolar read can be used to rectify electromigration or compensate for changes in the device state at rest, as retention is limited.

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A

Other results

This appendix contains results that did not merit inclusion in the main text. Note that the equilibrium ratio is referred to by its old name, the critical ratio, in some figures.

A.1. Minimum error bipolar read scheme & results

After the results showed the HRS and LRS were not simultaneously reinforced, an alternative bipolar read scheme was devised. The goal here was to further reduce resistance drift. As the obtained 5x reduction did not improve on what was already achieved, it was deemed not worth including in the main text.

A.1.1. Design of minimum error-based direction switching

A read current direction switching ratio can also be found by treating resistance drift as an error to be minimized, as shown in equation A.1. Minimizing this function gives us the switching ratio. Resistance drift numbers were obtained from the unidirectional read disturb results found in chapter 6. This gives us $r_{switch} = 7:1$.

$$E = \left| \frac{r_{switch} * \Delta R_{set,LRS} + \Delta R_{reset,LRS}}{\Delta R_{set,LRS}} \right| + \left| \frac{r_{switch} * \Delta R_{set,HRS} + \Delta R_{reset,HRS}}{\Delta R_{set,HRS}} \right| \tag{A.1}$$

A.1.2. Minimum error-based results

Let us consider $r_{switch} = 7:1$, obtained using the minimum error function. Visual inspection of figures A.1 and A.2 shows imperceptible resistance drift. Tables A.1 and A.2 show disturbing drift is reduced 5.3x and 61x reduction in compared to unidirectional sensing in HRS and LRS, respectively. It should be noted that this switching ratio was chosen for minimum error at these initial resistances. It is unclear if this can be generalized to other resistance states.

Read scheme	Positive polarity	Negative polarity	Bipolar read ($r_{switch} = 7:1$)
Cumulative $\Delta R(m\Omega)$	-3.81	19.0	-0.723
$\Delta R/\Delta t$ (mΩ/cycle)	-0.952	4.76	-0.181
Drift reduction w.r.t. positive polarity			5.3
Drift reduction w.r.t. negative polarity			-26

Table A.1: Derived metrics from resistance drift simulation at HRS boundary

A.1.3. Discussion

Due to constraints in simulation run time, only a small amount of resistance drift could be simulated. It was assumed that the obtained reduction in resistance drift could be extrapolated to an equivalent reduction in read disturb, however this neglects the resistance drift changing with resistance, so this does not hold. These

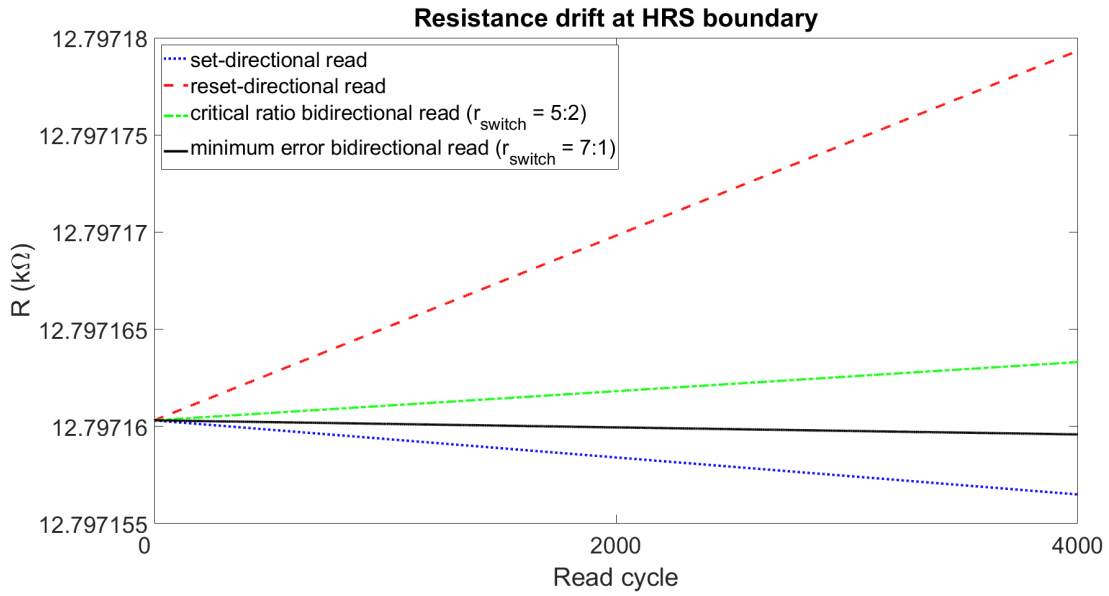

Figure A.1: Resistance drift at HRS boundary for both bidirectional read methods and the baseline unidirectional reads

Read scheme	Positive polarity	Negative polarity	Bipolar read ($r_{switch} = 7:1$)
Cumulative $\Delta R(\Omega)$	-384	3105	51.1
$\Delta R/\Delta t$ (mΩ/cycle)	-95.9	776	12.8
Drift reduction w.r.t. positive polarity			-7.5
Drift reduction w.r.t. negative polarity			61

Table A.2: Derived metrics from resistance drift simulation at LRS boundary

results can thus not be taken as a reduction in read disturb.
It might be possible to estimate the read disturb reduction by finding the resistance drift at select resistance values and interpolating the read disturb curve from this. However it was decided against this, since there was no indication of an improvement to the state of the art in read disturb reduction. The reason for this are several. First, the reduction in resistance drift in the HRS state already falls short of the state of the art. In addition, the minimum error method was optimized for minimum error at this precise resistance value, so is expected to perform worse at other values. Finally, there was no indication of read disturb reduction inherent to the design: the improvement was expected to come from improving the direction switching pattern.

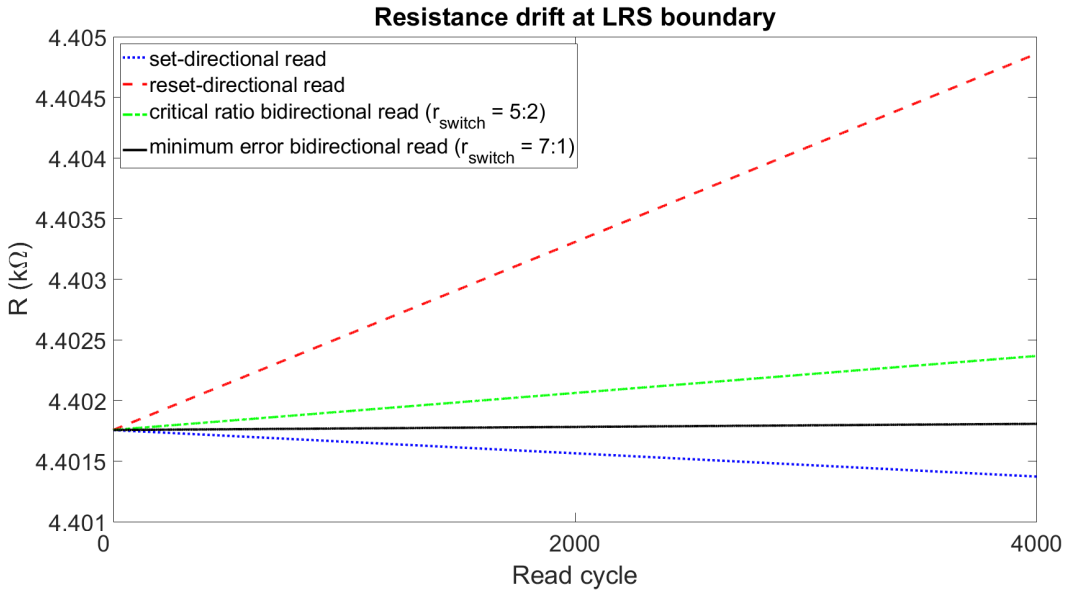

Figure A.2: Resistance drift at LRS boundary for both bidirectional read methods and the baseline unidirectional reads