Wideband Digital Intensive Doherty Concepts

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Challenge the future

WIDEBAND DIGITAL INTENSIVE DOHERTY CONCEPTS

by

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ABSTRACT

Many applications require wide bandwidth transmitters, but unfortunately, they usually have way less than 50% average drain efficiency for their modulated signals. This low efficiency is a significant drawback in all wireless applications, both for battery power devices and base stations. The Doherty radio frequency (RF) power amplifier architecture is widely used to enhance the average efficiency for modulated signals in base stations. Its popularity is due to its relatively cheap and simple hardware and its suitability to handle high-power wideband modulated signals. However, even Doherty amplifiers often have less than 50% average efficiency and are restricted in their RF bandwidth.

This thesis reviews recent research on the Doherty power amplifier (DPA) topology and discusses possible power and bandwidth efficiency improvements. In the second part of the thesis, another topology is introduced, which also provides Doherty-like behavior. That topology is called a Pseudo Doherty Load Modulated Balanced Amplifier (PD-LMBA). The performance of PD-LMBA is compared with “conventional” DPAs. Circuit design examples of DPA and PD-LMBA are given. The thesis concludes with a PD-LMBA prototype design, which appears to be very promising in its wideband performance. Also, its compatibility with future digital transmitters (DTX) concepts is discussed.

Keywords: RF power amplifier, Doherty, Pseudo Doherty Load Modulated Balanced Amplifier, PD-LMBA, wideband, transmitter, DTX.

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ABBREVIATIONS

ACPR	Adjacent Channel Power Ratio. It is the ratio of adjacent signal power to the reference signal power.
ADC	Analog to Digital Converter
AM	Amplitude Modulation
BA	Balanced Amplifier
BLC	Branch Line Coupler (one kind of -3 dB hybrids)
CA	Control Amplifier
CDMA	Code Division Multiple Access
CL	Coupled Lines (one kind of -3 dB hybrids)
CSP	Control Signal Power. Control signal is used in LMBA amplifiers.
DAC	Digital to Analog Converter
DC	Direct Current
DPA	Doherty Power Amplifier
DPD	Digital Predistortion
DTX	Digital Transmitter
FM	Frequency Modulation
IM3	3rd order Intermodulation Distortion
LDMOS	Laterally-Diffused Metal-Oxide Semiconductor
LMBA	Load Modulated Balanced Amplifier
LNA	Low Noise Amplifier
LO	Local Oscillator
OFDM	Orthogonal Frequency Division Multiplexing
OMN	Output Matching Network
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak to Average Power Ratio
PBO	Output Power Back-Off efficiency
PCL-DPA	Doherty Power Amplifier with Parallel Connected Load
PCL-IDPA	Inverted Doherty Power Amplifier with Parallel Connected Load
PDPA	Pseudo Doherty Power Amplifier. This is an amplifier which has Doherty PA like behavior but works in a different way.
PD-LMBA	Pseudo Doherty Load Modulated Balanced Amplifier. This is one of PDPA architectures. It is based on LMBA.

RF	Radio Frequency
RFC	Radio Frequency Choke. This is an inductor which acts as an open circuit for RF frequencies while as a short for DC. It is used to feed DC to a circuit.
SCL-DPA	Doherty Power Amplifier with Series Connected Load
SCL-IDPA	Inverted Doherty Power Amplifier with Series Connected Load

1

INTRODUCTION

Since its invention, wireless communication has steadily become essential to our daily life. Every day, we use laptops, mobile phones, or tablets to connect to the Internet wirelessly, for navigation, and to communicate with people who are far away. Various environment and health monitoring systems also use wireless connections for transmitting telemetry data to their hosts. For example, satellites send CO_2 and temperature measurement data to a ground station for analysis, vital for global warming research.

1.1. BACKGROUND INFORMATION

Devices, who use wireless communication, contain transmitters, receivers, or both. For example, a TV set acts as a TV signal receiver while a TV tower operates as a transmitter. Since a TV set does not need to send anything back to a TV station, it does not have any transmitter. For example, a laptop or other device, which supports Wi-Fi has a chip that contains a transceiver. A transceiver, in general, is a subsystem having both a transmitter and a receiver, which are designed for handling the same type of signals. The structure diagram of a generic RF transceiver is shown in Figure 1.1.

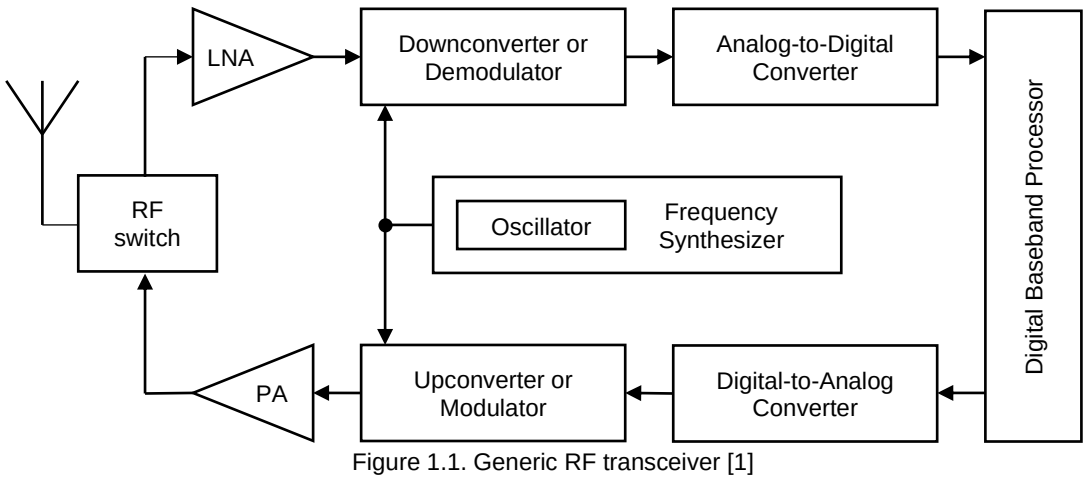


Figure 1.1. Generic RF transceiver [1]

In a time-domain-division (TDD) system, in reception, the RF switch connects the antenna to the Low Noise Amplifier (LNA). Then the amplifier amplifies the very weak input signal, which is then fed to the downconverter. A frequency synthesizer with the local oscillator generates a tone. Depending on the receiver architecture, this tone has equal or similar frequency to the frequency of the wanted RF signal. The downconverter contains a mixer that combines the signal from the LNA with the signal from the frequency synthesizer. The output from the mixer can be demodulated baseband signal or intermediate frequency (IF). If its output is located at IF, this intermediate signal is demodulated after some additional amplification. Finally, the baseband signal is converted to the digital domain by the Analog-to-Digital Converter (ADC) and sent to the processor.

In transmission mode, the RF switch connects the antenna to the Power Amplifier (PA). In this case, the processor sends baseband data to the Digital-to-Analog Converter (DAC), which converts it to an analog baseband signal. Then it goes to a modulator/upconverter. It contains a mixer that upconverts the baseband signal using the LO signal from the frequency synthesizer. The mixer output is an RF signal modulated by the baseband data. This RF signal is fed to the PA. Since an energy-efficient amplifier is typically not very linear, the transmitter often contains a pre-distortion block (DPD) to compensate for the signal distortions at the output of the PA (i.e., to compensate for non-linearities of the amplifier). Note that the use of that DPD, which is typically implemented in the baseband signal processing unit, is practical only in high power applications, such as base stations, because for low power applications (such as Wi-Fi) the DPD costs more energy than just having a linear PA. The amplified signal goes to the antenna and creates electromagnetic waves.

This work focuses on wideband efficiency enhancement topologies to implement the high-power amplifier/transmitter (e.g., P_{out} > 50 W). There are two main techniques for this efficiency enhancement: supply modulation (a.k.a. envelope tracking) and load modulation [2]. The latter technique relates to Doherty and pseudo-Doherty power amplifiers, which are investigated in this project.

It turned out that the performance of Doherty architecture can still be improved significantly [3, 4]. Most Doherty amplifiers rely on Class AB and Class C as main and peak amplifiers, respectively [5, 6, 7, 4], but other combinations are being tested as well, for example, using Class B [8, 9], Class D [5], Class E [6] amplifiers, or by trying different layouts for their power combiner [10]. Several non-Doherty architectures which have a Doherty amplifier-like operation have been invented, and they seem to have potential because they can have wider bandwidth than conventional topologies [11, 12, 2].

1.2. History of Doherty Power Amplifier

At the beginning of 20th century, radio transmitters used Class AB RF power amplifiers [13] and amplitude modulation. These amplifiers reach high efficiency only at their peak power, which is lower than 78.5% (Class B efficiency). Due to the applied AM modulation, the average power is much smaller than the peak power, especially for signals with a high peak-to-peak average power ratio (PAPR). As a result, these transmitters typically provide only around 33% average efficiency.

The Great Depression started in 1929, and many people, including radio operators, had minimal money [13]. They wanted to spend less on their operating cost, and one way to do that was to decrease their electrical energy consumption. Back then, the most energy-efficient, known RF power amplifier was operating in Class C. The Class AB amplifiers used to broadcast AM modulated signals could not be replaced by Class C amplifiers because AM requires good linearity while Class C is very non-linear (heavily distorts signal) [13]. Thus, there was a demand for research on more efficient power amplifiers that can handle AM signals. In 1936 William H. Doherty came up with an amplifier that can increase the average efficiency to 60-65% [14]. His solution consisted of a combination of Class AB and Class C amplifiers. Today, there are many different variations of it. The first 50 kW Doherty power amplifier (DPA) was implemented in a radio broadcast transmitter in 1938. It was based on vacuum tubes. Its introduction increased the average efficiency from 33% to 60% [15].

Later FM transmitters started to dominate. An FM signal has a constant envelope (i.e., it has a PAPR of 0 dB). Therefore, its transmitter can continuously operate at peak power, yielding a high average

efficiency. With this popularity of FM signals, the interest in the Doherty amplifier topology disappeared.

1.3. Motivation

Modern digital communication systems use broadcast signals with a “complex modulation,” i.e., they use both amplitude and phase modulation simultaneously. They usually use modulation schemes with sub-carriers (such as OFDM) which, like vintage AM, also have high PAPR. These signals spend most of their time at lower output power levels; however, they sometimes produce signal peaks that require 6, 8, or even up to 12 dB of power amplifier headroom in reserve [13]. Furthermore, while in the early days of AM radio 20 kHz bandwidth was enough, now, due to many inventions, there is a need to transfer very high bitrate digital data, for example, to exchange big (multimedia) files quickly, stream high-resolution video in real-time. Some complex embedded systems also need high-speed data transfer, including the latest generation of smart cars. Very high bitrate means that PAs, who have high bandwidth, are required. Examples of mentioned modern digital communication technologies include Wi-Fi, 4G, 5G, DVB-T. 4G has 7-8 dB PAPR, 5G and WLAN IEEE 802.11ax has >9.5 dB [2].

Many years have passed since the invention of wireless communication and DPA, but wideband RF transmitters’ efficiencies are still relatively low. Thus, intensive research is going on which aim is to improve transmitters’ drain efficiency and bandwidth [13]. One of the ways to enhance the power and efficiency bandwidth could be using an amplifier with Doherty architecture, which utilizes the load modulation technique in combination with pre-distortion. This is why interest in DPA reappeared.

1.4. Thesis Goals

The research goals of this thesis are as follows:

1. According to recent research [16], DPA with series-connected load (SCL) might be more wideband than the one with parallel-connected load (PCL). This thesis work should provide an objective comparison.
2. Improve the Doherty operation bandwidth by modifying/improving existing DPA topologies.
3. A new topology, called Pseudo Doherty Load Modulated Amplifier (PD-LMBA) has been mentioned in several recent papers [12, 2, 17]. It is claimed that this PD-LMBA does not have a fundamental bandwidth limitation since it does not utilize an impedance inverter as is used in conventional Doherty topologies. This thesis should investigate this new architecture and verify if this is the case, even when using output stage devices with a realistic output capacitance.
4. Investigate the highest bandwidth achievable with DPA/LMBA topologies when absorbing the transistor output capacitances (C_{DS}) within the power combiner. In this work, we will assume LDMOS technology to perform this study.
5. Evaluate the compatibility of the investigated DPA/PD-LMBA topologies with future DTX techniques.

1.5. Thesis Organization

This thesis is organized as below.

Chapter 2 presents conventional amplifier classes. The most important for this thesis are Class B and Class B/J. They are discussed in detail. Their design procedure is described, and design examples are given with their simulated results.

Chapter 3 introduces conventional Doherty amplifiers. Doherty topologies with series and parallel connected load (SCL-DPA and PCL-DPA), including inverted DPA topologies, are described. Two papers are reviewed, and their proposed solutions are simulated with a comparison of their performance. A design example is also given. Various methods to increase power and efficiency bandwidth are presented.

Chapter 4 introduces a topology, which operates differently than traditional Doherty amplifiers but gives similar performance results. It is the so-called Pseudo Doherty topology which is based on load modulated balanced amplifier (PD-LMBA).

Chapter 5 shortly discusses the physical design of the PD-LMBA. The focus is on its feasibility since no finalized layout is given in this report. First, different implementations of harmonic termination have been discussed, and the most suitable one has been selected. Suggestions on how to design the 3 dB hybrid needed for the PD-LMBA realization have also been provided.

2

CONVENTIONAL AMPLIFIER CLASSES

Amplifiers are the main building blocks of RF and Analog circuit design. Power amplifiers can be divided into classes, which can be separated into two groups: the classical controlled conduction angle amplifiers (Class A, AB, B, and C) and so-called “switching” amplifiers (Class D, E, and F) and inverse classes. An amplifier class is selected based on the linearity and efficiency requirements of the aimed application. Some amplifier classes are more optimized for linearity (important for high fidelity signals, e.g., analog AM or digital modulation schemes like CDMA and OFDM). Other considerations hold for efficiency. Typically there is a tradeoff between linearity and efficiency [18]. Classes D, E, and F are considered outside the scope of this thesis, so they will not be discussed in this work. However, classes A, AB, B, C, and J will be described. Classes B and B/J will be discussed in more detail, and related design examples will be given.

2.1. CLASSES A, AB, B, AND C

A generic circuit diagram of an amplifier that can work in any of these classes is represented in Figure 2.1. A transistor here acts as a current source. An RF choke (RFC) acts like a short for DC (DC feed) but is open for high frequencies. The voltage waveforms across the drain and source (V_{DS}) and the drain current overlap significantly. Thus, a significant portion of DC power is dissipated (wasted) in the transistor as heat instead of being delivered to the load as useful RF power. Despite this fact, these kinds of amplifiers are straightforward to design can be very simple and reliable. They are the oldest types of amplifiers in the history of electronics engineering, so they are time-tested and still very widely used in recent designs [18].

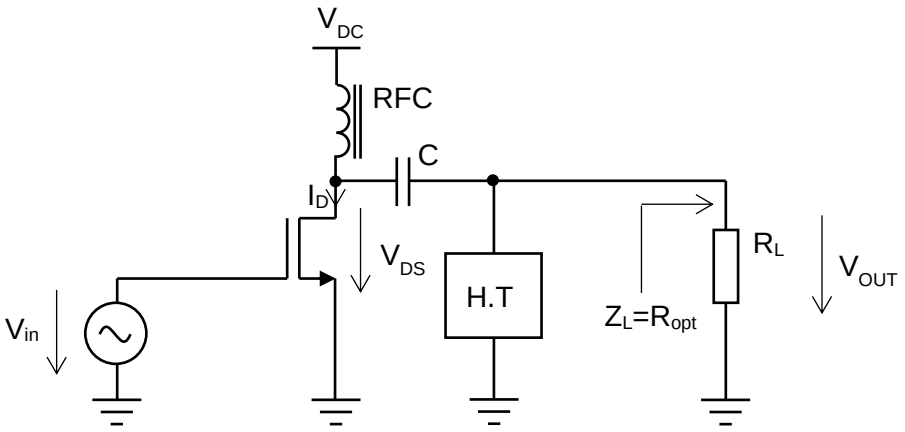


Figure 2.1. A generic schematic of a single-ended amplifier that can work as Class A, AB, B or C. H.T. means harmonic termination. RFC is a RF Choke, C is a capacitor for DC blocking.

For Class A operation, the operating point should be set to the middle of transistor output characteristics where maximum drain current should be chosen using equation (2.17) as described later in this chapter. For Class AB the operating point should be below the middle of the output characteristic, but still, a quiescent current will flow, while in the case of Class B and C amplifiers, the quiescent current is basically zero. No quiescent current means that the amplifiers do not consume power when their input signal is zero, which is a significant advantage. The operating points for different classes are shown for the transistor input and output characteristics in Figure 2.2. From the plot on the right (input characteristics) the difference between classes B and C can be noted. Namely, depending on the threshold voltage of the active device, the voltage between gate and source (V_{GS}) is typically zero for Class B, while for Class C, a negative bias is often used. As a result, in Class B operation, the transistor will be open only during the positive period of the input signal (in practice a bit less due to the transistor threshold voltage), while in Class C operation, it will be open only close to the peak of the positive period of the input signal. The negative swing will switch the transistor off in both cases. Furthermore, in practical circuits, the negative input swing coincides with the peak voltage in the drain output. That is a potential problem because this can result in semiconductor reverse breakdown if it is not well designed [19].

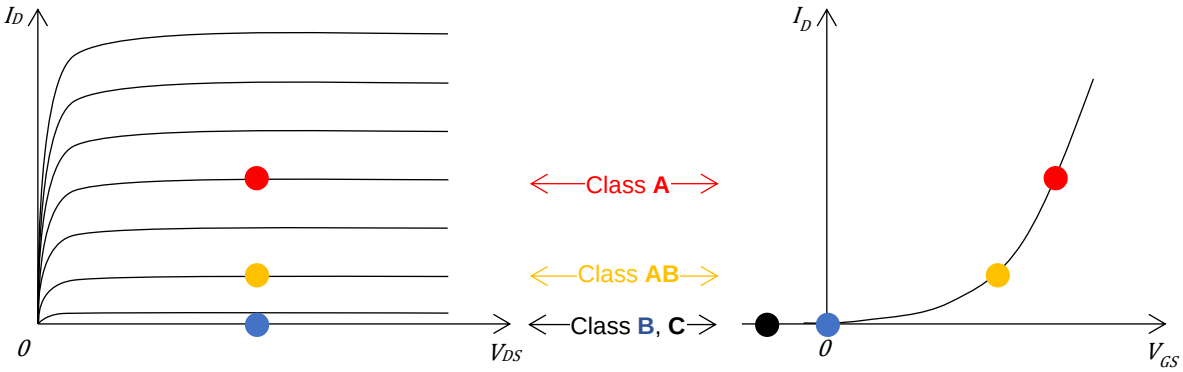


Figure 2.2. Relationship between amplifier class and transistor operating point [15]

The part where the transistor is conducting can also be expressed quantitatively by a *conduction angle*, α. Let's assume that the input signal is a cosine waveform; see the top plot (the voltage waveform) of Figure 2.3. Assume that this is the signal passed to the input of the amplifier. Then by applying Fourier analysis, the design equations can be derived as follow.

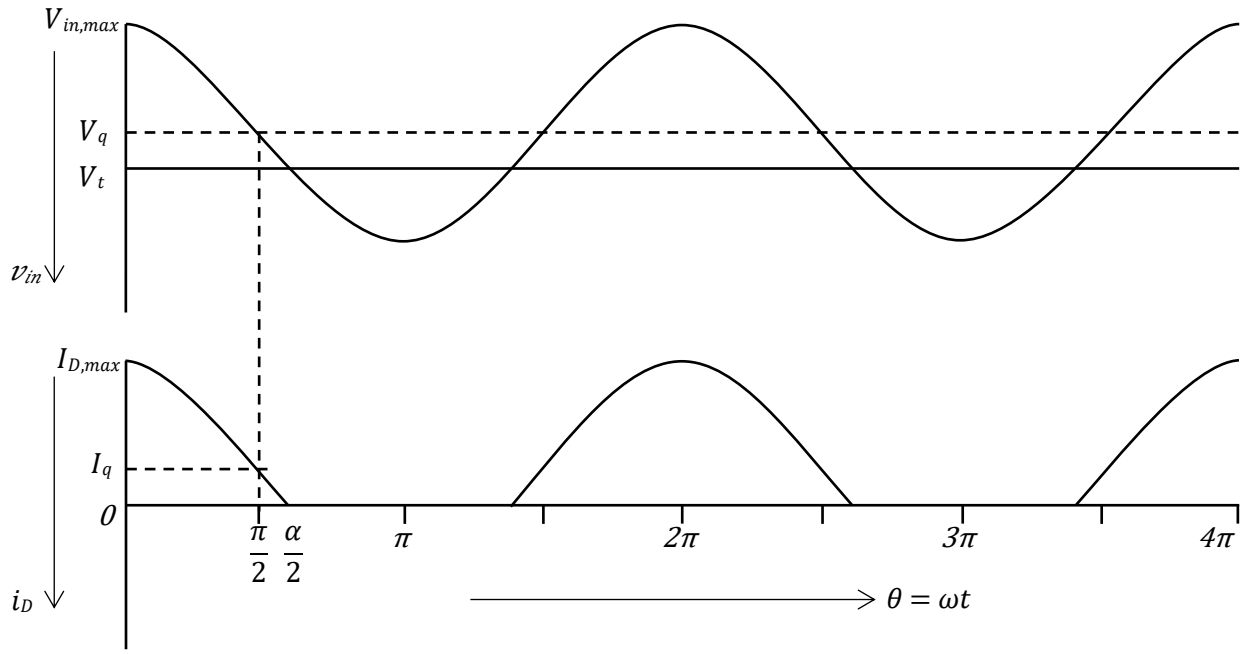


Figure 2.3. Input voltage and drain current waveforms of Class AB amplifier [19]

Drain current waveform (bottom plot of Figure 2.3) can be expressed as [19]:

$$i_D(\theta) = \begin{cases} I_q + I_{pk} \cdot \cos\theta & , \ -\alpha/2 < \theta < \alpha/2 \\ 0 & , \ -\pi < \theta < -\alpha/2 \\ 0 & , \ \alpha/2 < \theta < \pi \end{cases} \tag{2.1}$$

where I_q is the quotient current, θ is the phase, and I_{pk} is the amplitude of drain current. It can be observed from Figure 2.3 that:

$$\cos(\alpha/2) = -\frac{I_q}{I_{pk}}; \tag{2.2}$$

$$I_{pk} = I_{D,max} - I_q \tag{2.3}$$

Then equations (2.2) and (2.3) can be applied to (2.1), and after some manipulations, we can obtain:

$$i_D\,(\theta) = \frac{I_{D,max}}{1 - \cos(\alpha/2)} \cdot (\cos\theta - \cos(\alpha/2)).$$

Fourier decomposition can be applied to find the: DC current, fundamental, and all harmonic currents. The Fourier series is given by:

$$i_D(\theta) = I_{DC} + \sum_{n=1}^{\infty} I_n \cos(n\theta)$$

DC component:

$$I_{DC} = \frac{1}{2\pi} \cdot \int_{-\alpha/2}^{\alpha/2} \frac{I_{D,max}}{1 - \cos(\alpha/2)} \cdot (\cos\theta - \cos(\alpha/2))\ d\theta$$

$$I_{DC} = \frac{I_{D,max}}{2\pi} \cdot \frac{2\sin(\alpha/2) - \alpha\cos(\alpha/2)}{1 - \cos(\alpha/2)} \tag{2.4}$$

The magnitude of n[th] harmonic is:

$$I_n = \frac{1}{2\pi} \cdot \int_{-\alpha/2}^{\alpha/2} \frac{I_{D,max}}{1-\cos(\alpha/2)} \cdot (\cos\theta - \cos(\alpha/2)) \cdot \cos(n\theta)\ d\theta \tag{2.5}$$

The magnitude of the fundamental of the drain current is ($n = 1$):

$$I_{fund} = \frac{I_{D,max}}{2\pi} \cdot \frac{\alpha - \sin\alpha}{1-\cos(\alpha/2)} \tag{2.6}$$

When an amplifier works in Class A, the quiescent point is far from the bottom, and the conduction angle is 2π. Thus the drain current should never be clipped in regular operation. As a result, ideally, harmonics do not exist even if a harmonic termination (see H.T. block in Figure 2.1) is not present. However, in reality, harmonics still exist due to not ideal transistor characteristics, but they are very small. When an amplifier works in a different class than Class A (Class AB, B, C), the conduction angle is smaller than 2π (Figure 2.3) and, due to a clipped bottom of drain current waveform, harmonics are present. These harmonics could be found using (2.5).

Furthermore, this equation can be used to verify that the Class A amplifier does not have harmonics. All harmonics must be terminated (shorted to ground) for classes AB, B, and C to have a linear output. So, shorts to the ground (or very low impedance) for the higher harmonics (note that this applies only to the classes AB, B, and C) and open (infinite or very high impedance) for the fundamental frequency. Typically the input signal is sinusoidal, i.e., without harmonics.

The most straightforward practical harmonic termination implementations could be a parallel LC tank circuit or a λ/4 transmission line. The latter realization would only terminate even harmonics, so it is primarily applicable for Class B amplifiers. However, such implementations are too narrowband for the most recent wireless applications. A wideband alternative could be a Class B/J amplifier. It operates somewhat as a Class B amplifier but with complex fundamental and harmonic terminations that fulfill some specific conditions. The theory and design of such an amplifier are described in section 2.4.

Assume that maximum voltage swing will be reached when the peak input level corresponding to the peak drain current I_{max}. The drain voltage will be a sine waveform since all harmonics are shorted. Assuming no clipping takes place, the maximum output voltage swing is set by the load impedance (R_L in Figure 2.1). Then RF fundamental output power is:

$$P_1 = \mathrm{Re}\left\{\frac{V_{DC}}{\sqrt{2}} \cdot \frac{I_{fund}^*}{\sqrt{2}}\right\} = \mathrm{Re}\left\{\frac{1}{2} \cdot V_{fund} \cdot I_{fund}^*\right\} \tag{2.7}$$

here I_{fund}^* is a complex conjugate of I_{fund} resulting from (2.6). In this example, the load is entirely ohmic, so the current does not have an imaginary component. The voltage and the current are in phase. Thus, in this case $I_{fund}^* = I_{fund}$. However, if the load has a reactive component, there is be a phase difference between voltage and current waveforms, so the use of a complex conjugate termination would be necessary. This latter fact is mentioned for completeness. V_{fund} is the voltage of the fundamental tone. Both V_{fund} and I_{fund}^* are measured on the load. DC supply power can be expressed by

$$P_{DC} = V_{DC} \cdot I_{DC} \tag{2.8}$$

where I_{DC} is given by (2.4). Then the *drain efficiency*:

$$\eta = \frac{P_1}{P_{DC}} \tag{2.9}$$

However, this efficiency does not consider drive power requirements which are usually relatively high for RF power amplifiers. Due to this reason, another definition is also used. It is called Power Added Efficiency (PAE):

$$PAE = \frac{P_{fund} - P_{in}}{P_{DC}} \tag{2.10}$$

Where P_{in} is RF drive power. PAE equation suggests that some output power originates from the input power. But this is not true for modern amplifiers. Thus, PAE is a figure-of-merit, which does not represent what is going on in the circuit. Alternatively, RF drive power can be taken into consideration by calculating an efficiency using the following equation:

$$Total\ Efficiency = \frac{P_{fund}}{P_{DC} + P_{in}}. \tag{2.11}$$

When the quiescent current is lower, the efficiency is higher, but linearity typically decreases. However, proper harmonic termination and device optimization can reduce harmonic distortion, and this may improve linearity.

Equations (2.6) and (2.9) have been plotted, and the result is shown in Figure 2.4. As in equations, it was assumed that there is a maximum linear current I_{max}. When there is a perfect harmonic short and that there is no knee region. The maximum voltage swing between drain and source and at the output is twice the supply voltage i.e.,$2V_{DC}$. This factor two is due to the symmetry and use of even harmonic shorts. Since a sinusoidal RF waveform is symmetrical about its mean level, it has to rise to a peak voltage of twice the DC supply to remain higher than zero on the downward part of the cycle [19]. For these conditions, optimum load impedance would be [19]:

$$R_{opt} = \frac{V_{DC}}{I_{fund}} \tag{2.12}$$

Alternatively, the optimum load impedance expression can be derived from (2.7) by using Ohm's law for I^*_{fund}. Let's assume that all values are real. Then impedance seen by the amplifier should be:

$$R_{opt} = \frac{V^2_{fund}}{2P_{fund}}. \tag{2.13}$$

The impedance seen by the amplifier should be equal to that optimum load impedance to reach the highest efficiency at its maximum drive level.

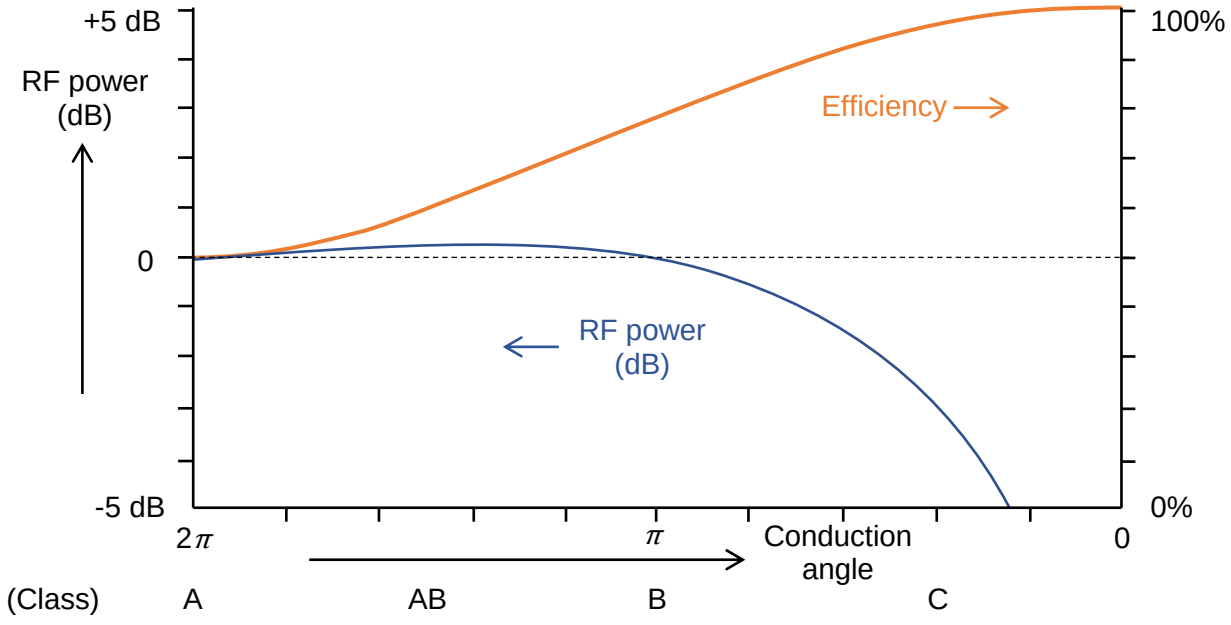


Figure 2.4. RF power (relative to Class A) and efficiency as a function of conduction angle; optimum load and harmonic short assumed [19].

From Figure 2.4 we can see that efficiency is lowest for Class A and highest for Class C. However, although 100% drain efficiency in Class C is theoretically possible, there is no power delivered to the load in this extreme case. Consequently, a tradeoff between power and efficiency has to be made.

Equations (2.4) and (2.6) - (2.9) can be applied to each class separately. After analyzing Figure 2.4 the following conclusions could be made, which are summarized in Table 2.1. Class AB is a tradeoff between Class A and Class B.

Table 2.1. Comparison of conventional amplifier classes [19, 15]

Class	Gate bias point	Quiescent current	Conduction angle (α)	Efficiency	Gain[1]	Linearity
A	0.5	0.5	$\alpha = 2\pi$	< 50%	High	Good
AB	0-0.5	0-0.5	$\pi < \alpha < 2\pi$	< 78.5%	High	Moderate
B	0	0	$\alpha = \pi$	< 78.5%	Medium/High	Moderate
C	<0	0	$0 < \alpha < \pi$	< 100%	Low	Poor

2.2. Bandwidth Limitation

Ideal amplifiers do not have bandwidth limitations; however, in practice, bandwidth is limited. One of the bandwidth limiting factors are parasitic capacitances. For the bandwidth, the most critical transistor parasitic capacitance is between drain and source, and it is presented as C_{DS}.

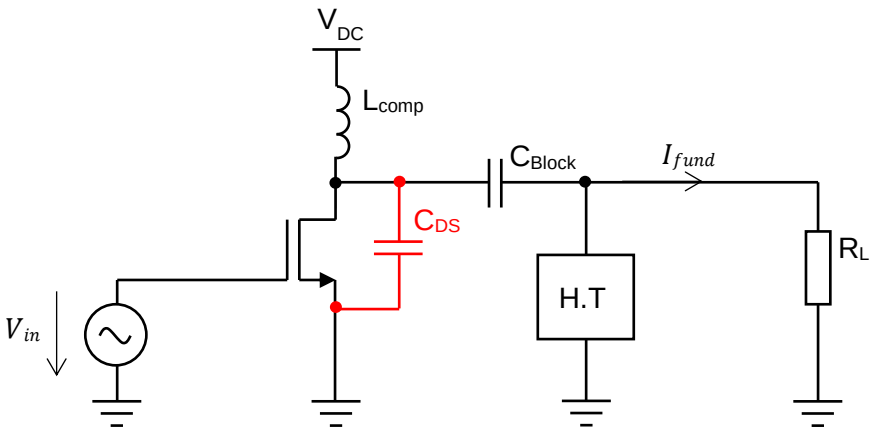


Figure 2.5. Basic amplifier with transistor parasitics C_{DS}.

C_{DS} has to be compensated in the design frequency; otherwise, the amplifier will not work. This can be done using an inductor which would offer a precise opposite reactance to the C_{DS} reactance. It is known that the reactance of a capacitor is

$$X_C = -\frac{1}{2\pi f C} \tag{2.14}$$

And the reactance of an inductor is

$$X_L = 2\pi f L \tag{2.15}$$

thus, the inductance needed to achieve the wanted condition ($X_C = X_L$) can be calculated using the equation (2.16),

$$L_{comp} = \frac{1}{4\pi^2 f^2 C_{DS}} \tag{2.16}$$

[1] Gain strongly depends on device characteristics and operating frequency.

This inductor could be connected in parallel to C_{DS} via DC blocking capacitor. However, since V_{DC} and ground are the same from the input signal point of view, it is more practical to replace DC pass inductor (a.k.a. RF Choke or RFC, see Figure 2.1) with the compensation inductor (L_{comp}, see Figure 2.5). Then L_{comp} serves two purposes: parasitic capacitance compensation and DC feed. Unfortunately, L_{comp} and C_{DS} make a parallel tank circuit, which limits the bandwidth of the amplifier. If the tank circuit has high-quality factor Q, this limitation is significant, and this is a common problem in wideband amplifier design.

In general, tank quality can be reduced using a resistor. For example, it can be connected in series to the inductor, the capacitor, or parallel. In this design case, it obviously cannot be connected in series with $C_{DS,}$ but if high inductance (RFC) inductor would be connected instead of L_{comp} and L_{comp} is moved after the blocking capacitor, it can be connected to the ground via the resistor. However, then L_{comp} will not do such a good job as C_{DS} compensation because of that resistor. As a result, drain efficiency and power will be lower even at the center frequency, so this way is impractical. Note that the amplifier's load resistance is parallel to the tank circuit, limiting the tank quality factor. Thus, a more practical way to increase bandwidth is to reduce optimum load impedance because that also reduces the tank quality factor. As seen from (2.13), the optimum load impedance can be reduced by lowering the power supply voltage. Alternatively, Class B/J topology can be used as described in section 2.4.

2.3. Design Example of Class B amplifier

Let's assume that we need to design an amplifier with the following specifications:

- Supply voltage (V_{DC}): 28 V;
- Maximum output power (P_{max}): 18.75 W;
- Efficiency (η): 78%;
- Center frequency (f_c): 3.5 GHz

Also, let's assume for the LDMOS technology considered:

- Maximum current per 1mm LDMOS transistor ($I_{D,max/mm}$): 0.15 A/mm;
- Transistor parasitic capacitance between drain and source ($C_{DS/mm}$): 0.313 pF/mm;
- Breakdown voltage is 64 V;
- Assume, for simplicity, that the transistor's threshold voltage (V_t) is 0 V.

For this design, assume that the input voltage swing (V_{in}) is normalized to 1 V. In practice, LDMOS technology needs a higher V_{in}.

Class B is a good candidate for these specifications because it can reach the required efficiency. First, choose a generic topology, which is shown in Figure 2.1. Equations used in this example can be derived from equations mentioned in the previous section. Although we aim for a Class B amplifier, let's still use generic equations suitable for classes A, AB, C, and J. If the reader decides to redesign for other classes, α can be changed and calculations performed again.

Fundamental current:

$$I_{fund} = \frac{2P_{max}}{V_{fund}} = \frac{2 \cdot 18.75}{28} \approx 1.34\ A;$$

Optimal load impedance.

$$R_{opt} = \frac{V_{fund}^2}{2P_{max}} = \frac{28^2}{2 \cdot 18.75} \approx 20.9\ \Omega;$$

Maximum drain current:

$$I_{D,max} = \frac{I_{fund} \cdot 2\pi[1 - \cos(\alpha/2)]}{\alpha - \sin\alpha}; \quad (2.17)$$

Choose Class B for 78% efficiency. Then $\alpha = \pi$ and (2.17) becomes

$$I_{D,max} = 2I_{fund} \approx 2.68\ A; \quad (2.18)$$

Required supply current:

$$I_{DC} = \frac{I_{D,max}}{2\pi} \cdot \frac{2 \cdot \sin(\alpha/2) - \alpha \cdot \cos(\alpha/2)}{1 - \cos(\alpha/2)} \approx 0.853\ A; \quad (2.19)$$

Power consumption:

$$P_{DC} = V_{DD} \cdot I_{DC} = 28 \cdot 0.853 \approx 23.9\ W;$$

The transconductance of a transistor can be found using the following equation:

$$g_m = \frac{\partial I_D}{\partial V_{GS}}\Big|_{V_{DS} = \ const.} = \frac{I_{D,max}}{V_{GS,max}} \approx 2.68\ S; \quad (2.20)$$

where I_D is the drain current and V_{GS} is the voltage between the gate and the source, V_{DS} is the voltage between the drain and the source and $V_{GS,max}$ is $V_{in,max}$.

Required offset voltage (for Class B it is 0, but for other classes, it would not be 0, let's use general equation):

$$V_{offset} = \frac{V_{in,max} \cdot \alpha}{\pi} - V_{in,max} = 0\ V;$$

Equations (2.17) and (2.19) can be significantly simplified for Class B if one would fill-in $\alpha = \pi$. However, the given example does not have this simplification applied in case to show how more general equations can be used. If someone would decide to, for example, change Class B to Class AB while retaining all other specifications, they would only need to change α from π to a chosen value which would be in between π and 2π.

From technology specifications, we know that a 1 mm LDMOS transistor can provide 0.15 A. Thus, transistor sizes:

$$W_g = I_{D,max}/I_{D,max/mm} = 2.68/0.15 \approx 17.9\ mm; \quad (2.21)$$

where W_g is a transistor gate width. Now we can find parasitic capacitance:

$$C_{DS} = W_g \cdot C_{DS/mm} = 17.9 \cdot 0.313 \approx 5.6\ pF. \quad (2.22)$$

These parasitic capacitances have to be compensated. The same inductor (L_{comp}) is used for this compensation and for DC feed. The following equation can be used to find its value:

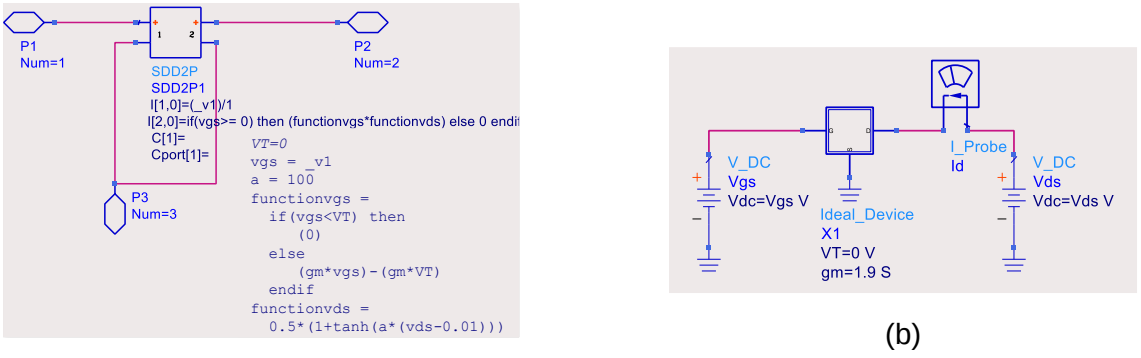
$$L_{comp} = \frac{1}{4\pi^2 f_c^2 C_{DS}} = \frac{1}{4\pi^2 \cdot (3.5 \cdot 10^9)^2 \cdot 5.6 \cdot 10^{-12}} \approx \mathbf{369\ pH}.$$

Calculated component values are summarized in Table 2.2.

Table 2.2. Calculation results.

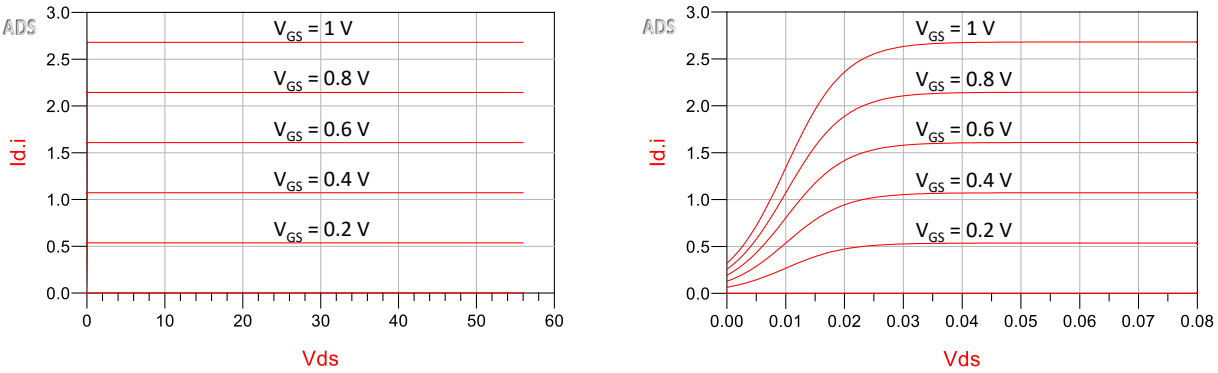
g_m, S	R_{opt}, Ω	L_{comp}, pH	C_{DS}, pF	V_{DC}, V
2.68	20.9	369	5.6	28

After these calculations, the circuit was entered into “Keysight ADS” software (see Figure 2.9). The ideal transistor is modeled by a component called “Ideal_Device”[2]. The model is implemented using “SDD2P1” as presented in Figure 2.6a. Test circuit (Figure 2.6b) has been used to obtain output characteristics shown in Figure 2.7. Figure 2.7a shows the characteristics for the whole region of interest, and Figure 2.7b shows it only for very small V_{DS} values. Despite there appears a region in the output characteristics (Figure 2.7b) which somewhat resembles a “linear” FET region of a transistor. For this ideal device it is actually is not supposed to be there. That region is implemented (by $\tanh()$ function) to have a smooth transfer function that helps numerical simulation convergence.



(a) (b)

Figure 2.6. “Ideal Device”: (a) Model, (b) Test circuit for output characteristics.



(a) (b)

Figure 2.7. Output characteristics of the “Ideal Device”: (a) Complete region of interest, (b) V_{DS} scale zoomed-in.

Ideal harmonic termination in “Keysight ADS” software has been implemented using “Z1P_Eqn” component. It is shown in Figure 2.8a and its frequency response in Figure 2.8b. It can be seen that this implementation also provides high impedance for DC component, but that is not necessary for Figure 2.1 because DC blocking capacitor is added before that harmonic termination (H.T.) component.

A harmonic balance simulation has been performed. Then efficiency and power versus input voltage plots were generated (Figure 2.10). It can be seen that 78.5% is reached as it should. However, output power still didn’t reach exactly 18.75W because despite this ideal transistor model should not have a linear region, there is still a small region that resembles it, although the region is tiny. We didn’t consider this region during our calculations because that would make it more complicated for only a minimal benefit.

[2] *Ideal_Device* can be used to model not only ideal transistors but also other structures which have transistor like behavior, such as a simplified model of transistor arrays which are used in DTX.

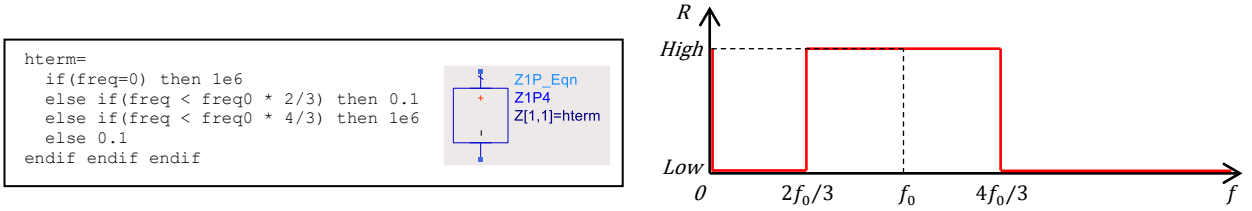


Figure 2.8. Ideal harmonic termination[3]: (a) example implementation in ”Keysight ADS”, (b) its frequency response.

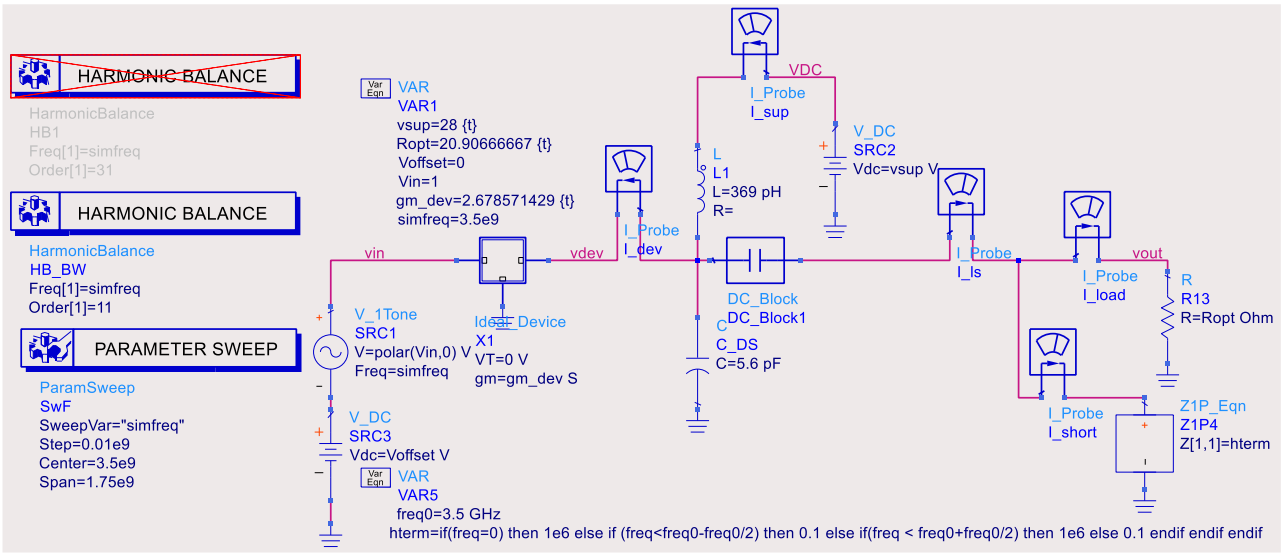
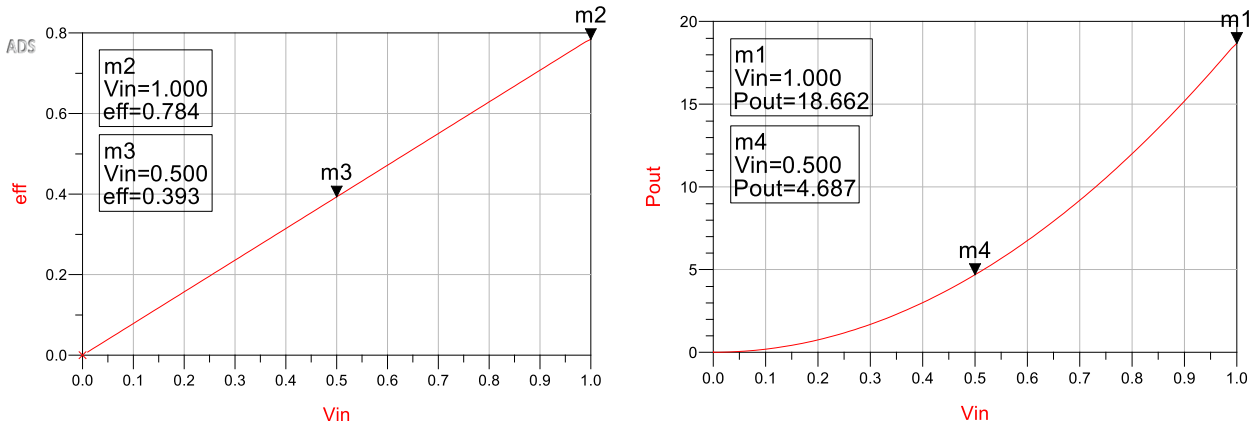


Figure 2.9. Designed Class B power amplifier prepared for harmonic balance simulation in “Keysight ADS” software



(a) (b)

Figure 2.10. Simulation results vs. input voltage (V_{in}): (a) efficiency, (b) power.

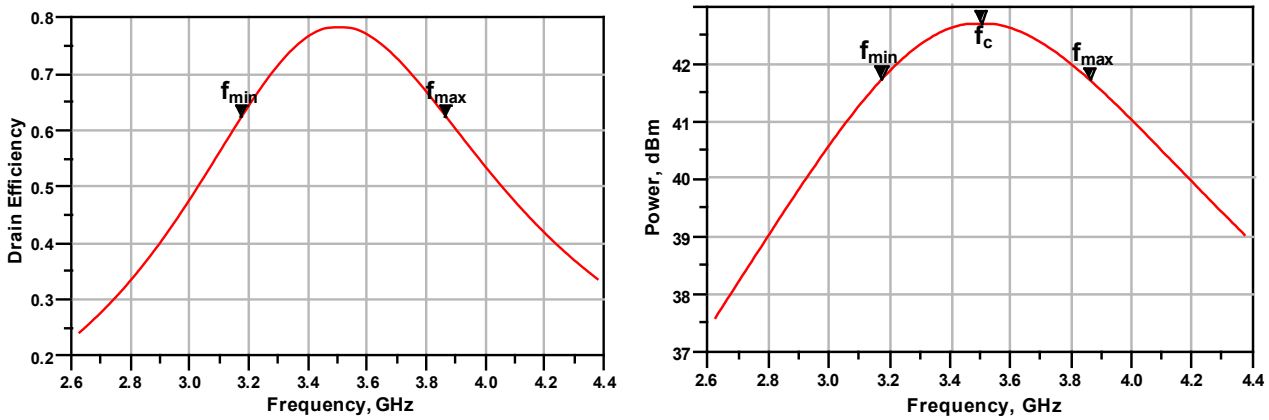
It is worth noting here that even if drain efficiency at maximum input voltage is 78.6%, it is still only 39.3% at 0.5 V. This can be seen from Figure 2.10a or can be calculated using equation (2.23) which can be delivered from (2.7) and (2.8) [14]:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{\pi}{4} \cdot \frac{V_{in}}{V_{in,max}} \tag{2.23}$$

[3] Note that the range from $f_0 - f_0/2$ to $f_0 + f_0/2$ has been used during all simulations instead of the range from $2f_0/3$ to $4f_0/3$. This results in a difference between IM3 when tone spacing is above 0.8 GHz.

where V_{in} is input signal voltage, $V_{in,max}$ is the maximum input signal voltage. This is a big problem when such RF power amplifiers are used for signals with high PAPR. These signals usually provide significantly smaller input voltages to the transistor, so most of the time, such an amplifier would work with a much smaller efficiency than 78.6%. As it has been already mentioned in the previous chapter, this issue is addressed by Doherty power amplifier architecture, which uses load modulation for efficiency enhancement and is described in the next chapter. Another widely used efficiency enhancement technique is supply modulation (also known as envelope tracking); however, it has more limited video/modulation bandwidth, and its implementation is more complicated than the implementation of load modulation.

Figure 2.11 shows efficiency and power versus frequency plots acquired from simulation results. According to Figure 2.11b, the 1 dB bandwidth is 690 MHz. If the parasitic capacitance were not present, bandwidth would be, in theory, only limited by the harmonic terminations.



(a) (b)

Figure 2.11. Simulated bandwidth: (a) efficiency, (b) power.

2.4. Continuous-Mode Operation. Class B/J Amplifier.

If broadband amplification is needed, a *continuous-mode* power amplifier operation could be used. This concept increases the bandwidth of the traditional amplifier. By applying the concept to a Class B amplifier, Class B/J topology can be derived. It is shown in Figure 2.12. Then design procedure would consist of a modified Class B PA design using a Class B/J output matching network (OMN) design. OMN design can be very challenging because it is difficult to simultaneously make an OMN that satisfies the PA load impedance requirements in the fundamental and harmonics frequency bands [20]. This section describes a design procedure of Class B/J OMN, gives an example. Then harmonic balance simulation results of Class B and Class B/J are compared.

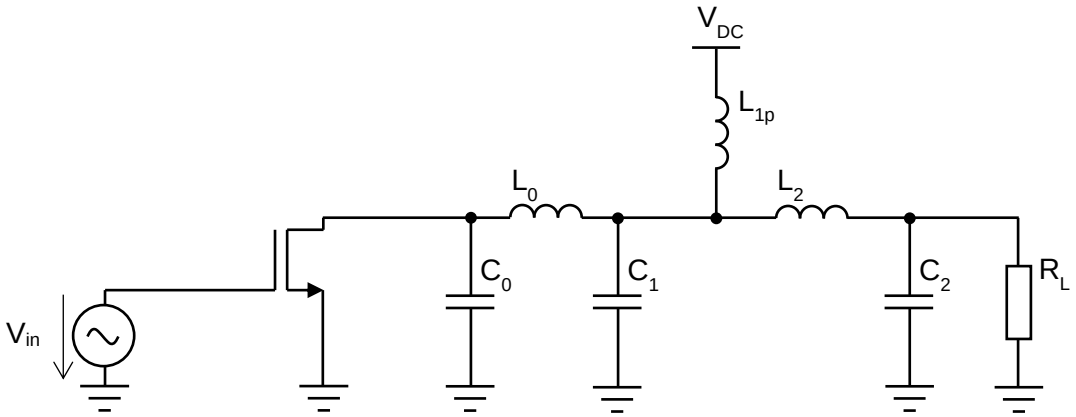


Figure 2.12. Class B/J amplifier

To work in *continuous mode*, a PA should have the same product and overlap between the voltage and current waveforms (at the intrinsic drain node) over its entire operating bandwidth regardless of the amplifier class. The *Class B/J mode* represents the case where the amplifier maintains the same voltage and current overlap and product as in conventional Class B, over a wide frequency range [20]. This can be achieved by assuming that the drain voltage $V_{DS}(\theta)$ and the current $I_D(\theta)$ have the following evaluation:

$$V_{DS}(\theta) = V_{DC} - (V_{DC} - V_t)\left[\cos\theta - \sin\theta + \frac{q\sin(2\theta)}{2}\right] \tag{2.24}$$

$$I_D(\theta) = \frac{I_{max}}{\pi} + \frac{I_{max}}{2}\cdot\cos\theta + \frac{2I_{max}}{3\pi}\cdot\cos(2\theta) \tag{2.25}$$

where V_{DC} and V_t are the supply and the transistor threshold (knee) voltages, respectively. θ is the angular phase at the fundamental frequency f_0 and it is equal to $2\pi f_0 t$. The coefficient q is a real factor in the range of [-1, 1], and I_{max} is the maximum drain current. Note that higher-order harmonics are neglected in these equations [20].

Impedances of required fundamental and second harmonic load termination (at intrinsic drain node) can be obtained from the ratio between (2.24) and (2.25). These impedances at f_0 and $2f_0$ are expressed by (2.26) and (2.27) respectively.

$$Z_{f0} = R_{opt} + jX_{opt} \text{ with } X_{opt} = qR_{opt} \tag{2.26}$$

$$Z_{2f0} = -j\cdot\frac{3\pi}{8}\cdot qR_{opt} \tag{2.27}$$

where R_{opt} is the optimal load for conventional Class B PA. Thus, the equation (2.26) shows that q is the quality factor of the fundamental impedance Z_{f0} (not to be confused with the quality factor of a tank circuit!). For a broadband amplifier, the change in f_0 from f_{min} to f_{max} should correspond to the change in q between -1 and 1. Note: the fundamental and the second harmonic impedances trajectories should have opposite directions. They are presented in Figure 2.13, as seen at the transistor's drain.

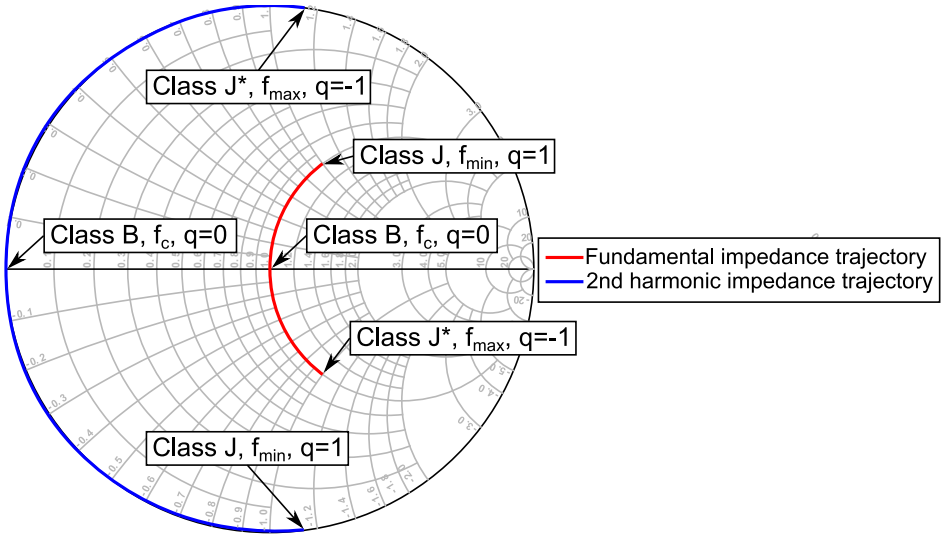


Figure 2.13. Theoretical fundamental and second harmonic impedance trajectory of continuous Class B/J amplifier (normalized to optimum load impedance)

2.4.1. Output Matching Network Architecture

The OMN is shown in Figure 2.14. As shown in Figure 2.13, it has to ensure that the Class B/J amplifier at the center frequency f_c works as a Class B amplifier while it has to work as Class J or J*

at the off-center frequency (a.k.a. Class J^{-1}) amplifier. Thus, it should have R_{opt} impedance for the center frequency (f_c) and as low impedance as possible (short) for its 2nd harmonic ($2f_c$) at its input. Capacitors C_0, C_1, and inductors L_0, $L_{1'}$ are necessary for the 2nd harmonic short, and while working together with L_2 and C_2 they provide it. However, C_0, C_1, and L_0, $L_{1'}$ changes optimum impedance for the fundamental from R_{opt} to Z_{inter} as well and that is unwanted. Thus, Z_{inter} has to be matched to the load impedance R_L which should be equal to[4] R_{opt}. However, Z_{inter} matching has to be done very carefully because the L_2 C_2 network must act as an inductor or capacitor with a specific value (not equal to L_2 and C_2) for the 2nd harmonic as described later in this section, and at the same time, it has to match Z_{inter} to R_L for the fundamental. 2nd harmonic impedance trajectory from f_{min} to f_{max} is determined by capacitors C_0, C_1 and inductors L_0, $L_{1'}$. L_2 and C_2 allow setting the impedance trajectory in the fundamental band from f_{min} to f_{max} while having a relatively low impact on the impedance trajectory in the 2nd harmonic frequency band [20]. $L_{1''}$ is used only during the design procedure, and it is not present in the final design, so this introductory description ignored it. It will be described later.

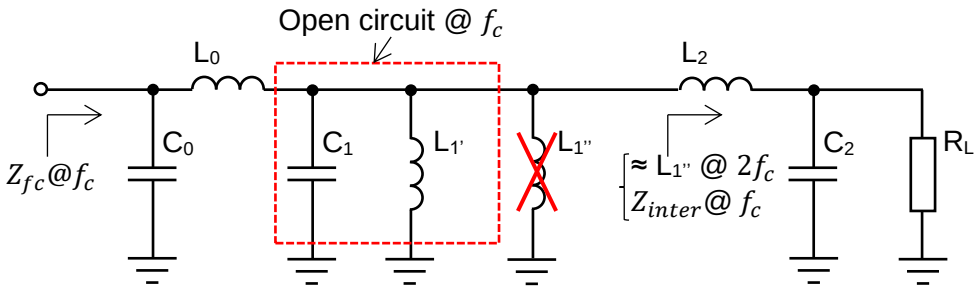


Figure 2.14. Class B/J Output Matching Network (OMN)

The design of OMN starts by building up the matching network part that traces the 2nd harmonic frequency trajectory. The part consists of C_0, C_1, L_0, $L_{1'}$ and $L_{1''}$, which must be connected for now instead of L_2 and C_2.

At $2f_c$, the parallel resonator $C_1L_{1'}L_{1''}$ should present an equivalent capacitor $C_{eq@2f_c}$, which in turn, will resonate in series with inductor L_0. The series resonance between L_0 and $C_{eq@2f_c}$ will short-circuit the capacitor C_0 at $2f_c$. These conditions lead to the following relationship [20]:

$$2\omega_c C_{eq@2f_c} = -\frac{1}{2\omega_c L_1} + 2\omega_c C_1; \tag{2.28}$$

$$2\omega_c L_0 - \frac{1}{2\omega_c C_{eq@2f_c}} = 0. \tag{2.29}$$

At $2f_{max}$ the parallel resonator C_1 $L_{1'}$ $L_{1''}$ should present an equivalent impedance $Z_{C_1L_1'L_1''@2f_{max}}$ as shown on the right side of Figure 2.15. Together with series-connected L_0 it makes a network which acts then as an equivalent inductor $L_{eq@2f_{max}}$. This equivalent inductor will dominate the capacitor C_0 and presents the required impedance, which has to be purely inductive when the frequency is above the center frequency f_c. This can be seen from Figure 2.13. Equations (2.30) and (2.31) describe the relationship between C_1, L_0, $L_{1'}$, $L_{1''}$, $L_{eq@2f_{max}}$ and the purely inductive input impedance $Z_{@2f_{max}}$.

$$2\omega_{max} L_{eq@2f_{max}} = \frac{1}{\frac{1}{2\omega_{max}L} - 2\omega_{max}C_1} + 2\omega_{max}L_0; \tag{2.30}$$

$$2\omega_{max} C_0 - \frac{1}{2\omega_{max} L_{eq@2f_{max}}} = -j \cdot \frac{1}{Z_{2f_{max}}}. \tag{2.31}$$

Where L is the total inductance of $L_{1'}$ and $L_{1''}$ and it can be expressed as follows:

[4] Since L_2 with C_2 simply form a matching network, it may be used to match Z_{inter} to other impedance.

$$L = \frac{L_1' L_1''}{L_1' + L_1''}. \tag{2.32}$$

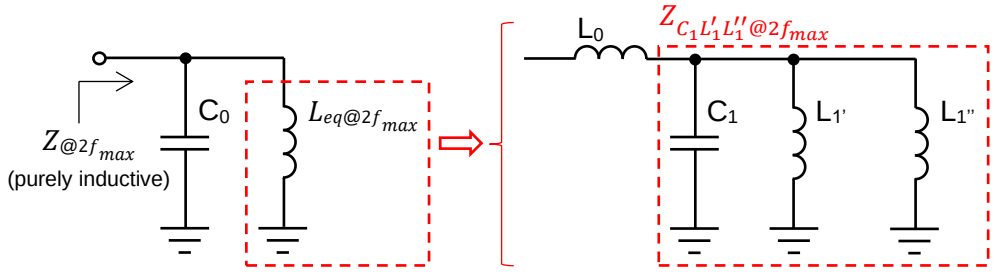


Figure 2.15. Equivalent circuit of the OMN at $2f_{max}$. $L_{1"}$ is the effective inductance of the network which consists of L_2, C_2 and R_L.

At $2f_{min}$ the parallel resonator C_1 $L_{1'}$ $L_{1"}$ should present an equivalent impedance $Z_{C_1L_1'L_1''@2f_{min}}$ as shown on the right side of Figure 2.16. Together with series-connected L_0 it makes a network which acts then as an equivalent capacitor $C_{eq@2f_{min}}$. This equivalent capacitor will be added to the capacitor C_0 and presents the required impedance which has to be purely capacitive when the frequency is below the center frequency f_c. This can be seen in Figure 2.13. Equations (2.33) and (2.34) describe the relationship between C_1, L_0, $L_{1'}$, $L_{1"}$, $C_{eq@2f_{min}}$ and the purely capacitive input impedance $Z_{@2f_{min}}$ [20].

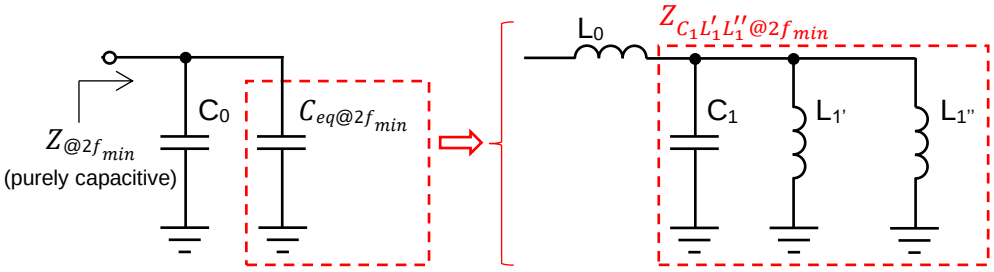


Figure 2.16. Equivalent circuit of the OMN at $2f_{max}$. $L_{1"}$ is the effective inductance of the network which consists of L_2, C_2 and R_L.

$$-\frac{1}{2\omega_{min}C_{eq@2f_{min}}} = \frac{1}{-\frac{1}{2\omega_{min}L} + 2\omega_{min}C_1} + 2\omega_{min}L_0; \tag{2.33}$$

$$2\omega_{min}C_0 + 2\omega_{min}C_{eq@2f_{min}} = -j \cdot \frac{1}{Z_{2f_{min}}}. \tag{2.34}$$

The equations from (2.28) to (2.34) make a non-linear system that can be solved numerically to calculate the values of the components. The inputs of the system are the impedances $Z_{2f_c} = 0$, $Z_{2f_{max}} = jX$, and $Z_{2f_{min}} = -jX$ where X is a constant value fixed by the choice of q and R_{opt}, since $X = qR_{opt}$ [20]. As it has been already told, for broadband operation $|q|$ should be equal to 1. Moreover, we already know from (2.27) that $X_{opt@2f_0} = \frac{3\pi}{8} \cdot qR_{opt}$. Therefore, for the highest bandwidth X should be set to the following value:

$$X = \frac{3\pi}{8} \cdot R_{opt}. \tag{2.35}$$

When C_0, L_0, C_1, $L_{1'}$ and $L_{1"}$ values have been chosen, $L_{1"}$ should be removed from the circuit, and a network which consists of L_2, C_2, R_L should be connected as it has been shown in Figure 2.14. The inserted network should act as $L_{1"}$ for $2f_c$ and provide impedance matching from Z_{inter} to R_L (which

can be equal to R_{opt}) at f_c. In case to derive the expression of Z_{inter}, the circuit from Figure 2.14 can be simplified to the one shown in Figure 2.17. The Z_{inter} can be calculated using (2.36).

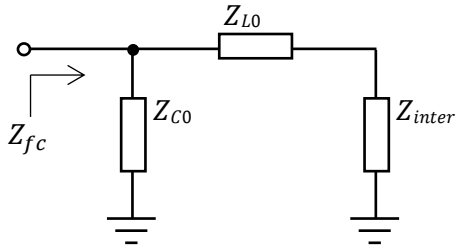


Figure 2.17. Class B/J Output Matching Network (OMN)

$$Z_{inter} = \frac{Z_{fc}(Z_{C0} + Z_{L0}) - Z_{C0}Z_{L0}}{Z_{C0} - Z_{fc}}. \tag{2.36}$$

Where Z_{C0} and Z_{L0} are impedances of C_0 and L_0 at fc, respectively, they can be found using (2.37) and (2.38):

$$Z_{C0} = -j/\omega_c C_0\,; \tag{2.37}$$

$$Z_{L0} = j\omega_c L_0. \tag{2.38}$$

Then values of C_2 and L_2 can be calculated the same way as for any other matching network:

$$C_2 = \sqrt{\frac{R_L - Re\{Z_{inter}\}}{R_L^2\omega_c^2 \cdot Re\{Z_{inter}\}}}; \tag{2.39}$$

$$L_2 = \frac{Im\{Z_{inter}\} \cdot (1 + R_L^2 C_2^2 \omega_c^2) + R_L^2 C_2 \omega_c}{\omega_c + R_L^2 C_2^2 \omega_c^3}. \tag{2.40}$$

Note that the network, which consists of L_2, C_2, and R_L can only approximately be equal to $L_{1'}$ at $2f_c$. This makes the design procedure difficult. The error depends on the R_L and how well L has been divided into $L_{1'}$ and $L_{1''}$ for the specific design case. There are no equations for this, so the best values can be found only experimentally. Sometimes wanted results may not be achieved. Careful modification of the topology may help to improve results for the specific design case.

2.4.2. Design Example

Let's choose $f_{min} = 3\ GHz$, $f_c = 3.5\ GHz$, $f_{max} = 4\ GHz$. These values correspond to:

$$\omega_{min} = 18.9 \cdot 10^9\ rad/s\,;$$

$$\omega_c = 22 \cdot 10^9\ rad/s\,;$$

$$\omega_{max} = 25.1 \cdot 10^9\ rad/s.$$

Before OMN design, Class B design procedure should be followed in case to calculate R_{opt}. It has already been introduced in section 2.3.

Let's take R_L equal to R_{opt}. Note that by applying introduced equations, it can also be matched to different impedance. Thus, in general, R_L does not need to be equal to R_{opt}. First, let's express $L_{eq@2f_{max}}$ and $C_{eq@2f_{min}}$ from equations (2.28) and (2.29), respectively. Here capacitance C_0 (see Figure 2.14) can be transistor parasitics. L_0 can be bound wire inductance [20]. Let's assume that L_0 is 0.1 nH. Thus, then it will be 5.63 pF. Since we want to make it very wideband, choose $|q| = 1$. Then, according (2.35):

$$Z_{2f_{min}} = -j \cdot \frac{3\pi}{8} \cdot R_{opt} = -j \cdot \frac{3\pi}{8} \cdot 20.9 = -j24.6\ \Omega;$$

$$Z_{2f_{max}} = j \cdot \frac{3\pi}{8} \cdot R_{opt} = j24.6\ \Omega.$$

Equations for equivalent inductance and capacitance can be derived from (2.34) and (2.31), respectively. After we fill-in values to these derived equations, we get:

$$C_{eq@2f_{min}} = -\frac{2\omega_{min}C_0 + j/Z_{2f_{min}}}{2\omega_{min}} = -4.55 \cdot 10^{-12}.$$

Unfortunately, this is a negative value so it is not valid. After decreasing q to 0.16, $C_{eq@2f_{min}}$ becomes 1.12 pF. Then the equivalent inductance:

$$L_{eq@2f_{max}} = \frac{1}{2\omega_{max}\left(2\omega_{max}C_0 + j/Z_{2f_{max}}\right)} = 37.1\ pH.$$

Place of $L_{eq@2f_{max}}$ and $C_{eq@2f_{min}}$ in the equivalent circuit has been shown on the left-hand side of Figure 2.15 and Figure 2.16. The following equation system can be created from (2.30) and (2.33):

$$\begin{cases} 2\omega_{max}L_{eq@2f_{max}} = \dfrac{1}{\dfrac{1}{2\omega_{max}L_1} - 2\omega_{max}C_1} + 2\omega_{max}L_0 \\ -\dfrac{1}{2\omega_{min}C_{eq@2f_{min}}} = \dfrac{1}{-\dfrac{1}{2\omega_{min}L_1} + 2\omega_{min}C_1} + 2\omega_{min}L_0 \end{cases}$$

After filling in our values and solving for L_1 and C_1 it was found that L_1 is **42.5 pH** and C_1 is **15.6 pF**. Then the equivalent capacitance for $2f_c$ can be found using (2.28)

$$C_{eq@2f_c} = \frac{1}{4\omega_c^2 L_0} = 5.17\ pF$$

and inductances of L_1, $L_{1'}$ and $L_{1''}$ using (2.29), (2.16) and (2.32), respectively:

$$L_1 = \frac{1}{4\omega_c^2(C_1 - C_{eq@2f_c})} = \mathbf{49.5\ pH};$$

$$L_{1'} = \frac{1}{C_1\omega_c^2} = \mathbf{132\ pH};$$

$$L_{1''} = \frac{L_1 L_{1'}}{L_{1'} - L_1} = 79.1\ pH.$$

Now let's fill-in calculated values into Figure 2.14 and use $L_{1''}$ instead of the network, which consists of L_2, C_2, and R_L. The circuit has been simulated, and the results are shown in Figure 2.16. To get the impedance plot on the Smith chart, the reflection coefficient $|\Gamma|$ can be calculated using (2.41), and plotted.

$$\Gamma = \frac{Z - R_{opt}}{Z + R_{opt}} \tag{2.41}$$

It can be seen that the 2nd harmonic of the center frequency is shorted to ground correctly. However, there are two unwanted resonances.

Now L_2, C_2 values will be calculated, and $L_{1''}$ will be replaced with the network which consists of L_2, C_2, and R_L. First, equations (2.36) - (2.38) have to be used with $Z_{fc} = R_{opt}$ in case to find the intermediate impedance Z_{inter}:

$$Z_{C0} = -\frac{j}{\omega_c C_0} = -j8.08\ \Omega;$$

$$Z_{L0} = j\omega_c L_0 = j2.2\ \Omega;$$

$$Z_{inter} = \frac{Z_{fc}(Z_{C0}+Z_{L0})-Z_{C0}Z_{L0}}{Z_{C0}-Z_{fc}} = 2.72 + j4.83\ \Omega.$$

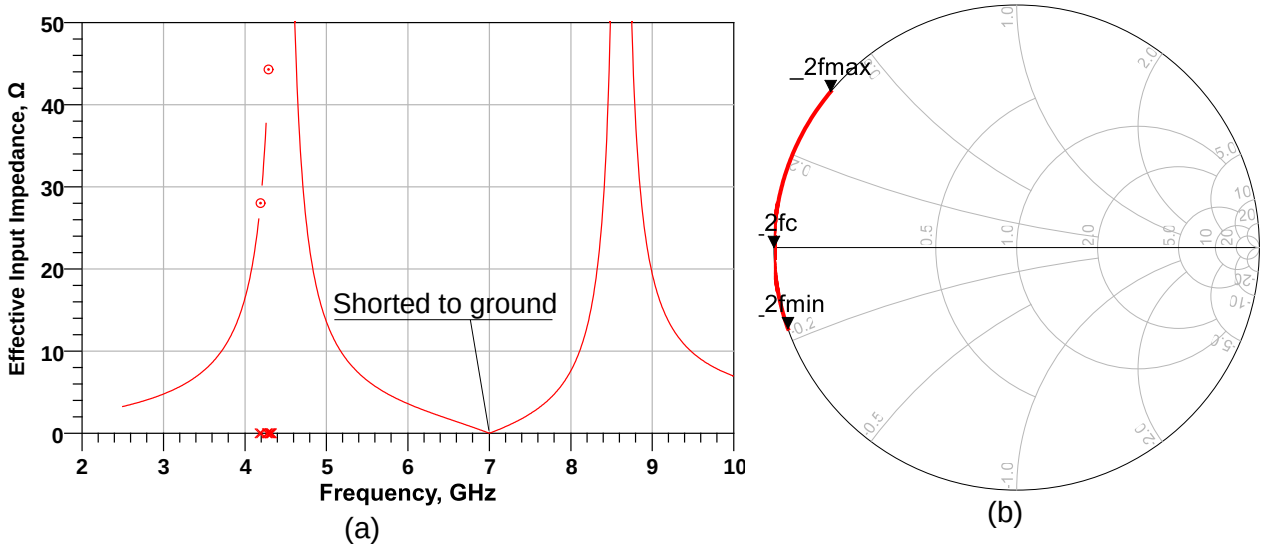


Figure 2.18. Intermediate simulation results of Class B/J circuit. C2, L2, RL are not present and inductor L1" is used instead of them: (a) effective input impedance, (b) impedance versus frequency from 2.5 GHz to 10 GHz

Then from (2.39) and (2.40) we can find out that L_2 is **540 pH** and C_2 is **5.63 pF**. Now $L_{1"}$ has been replaced with L_2, C_2, R_L, and the simulation has been repeated. Results are presented in Figure 2.19. It can be seen that now the input at the center frequency is loaded with the correct impedance (20.9 Ω). On the other hand, the frequency of unwanted resonance shifted to lower frequencies. The short to ground shifted from 7 GHz (2nd harmonic) to 5.7 GHz, and resonance from 4.5 GHz shifted to 3.6 GHz, contributing to bandwidth limitation. 1 dB power bandwidth now is only 250 MHz. So, it is significantly lower than for the usual Class B amplifier (690 MHz). This is highly unwanted. The impedance plot on the Smith chart, as shown in Figure 2.19b is too different from the ideal one introduced in Figure 2.13. Then optimization tool has been used in "Keysight ADS" and values have been adjusted. Final values are shown in

Table 2.3 and corresponding simulation results are presented in Figure 2.20 and Figure 2.21. Thus, bandwidth increased to 1360 MHz, so it became almost twice higher than for Class B. However, bandwidth is asymmetrical, and efficiency drops abruptly on high frequencies. Thus, these results are still not satisfying.

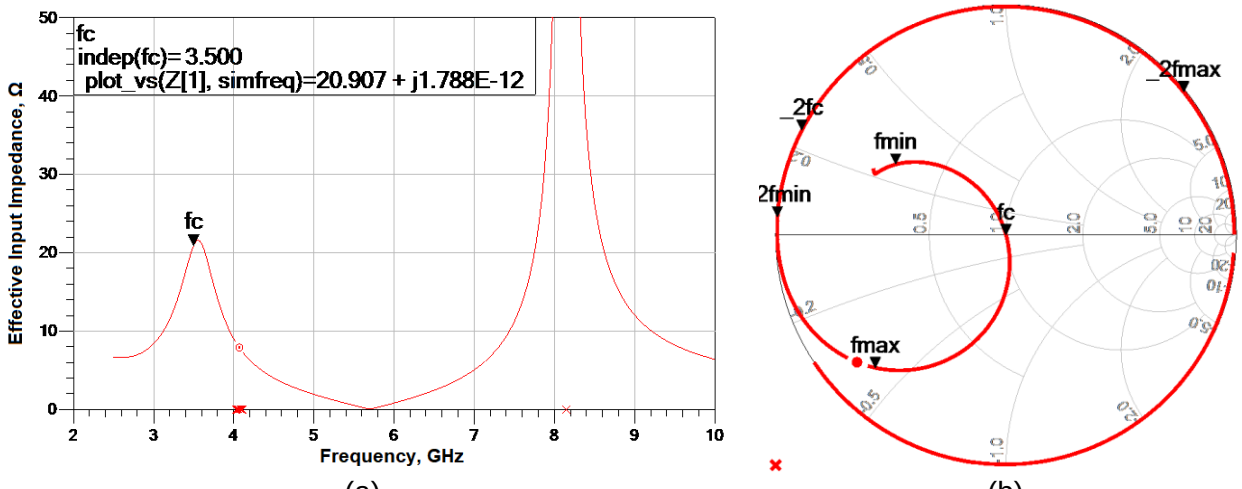
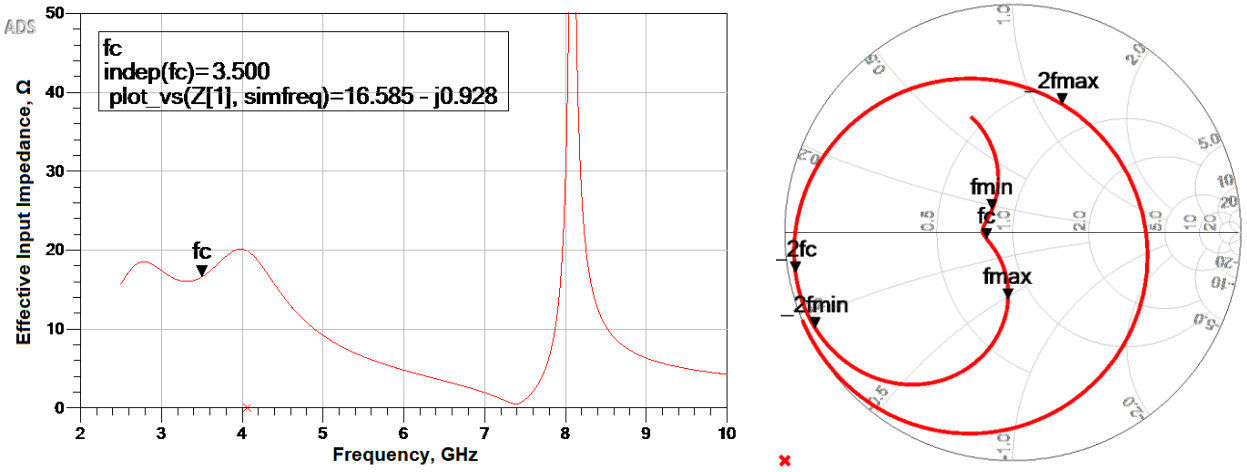


Figure 2.19. Intermediate simulation results of Class B/J circuit: (a) effective input impedance, (b) impedance versus frequency from 2.5 GHz to 10 GHz

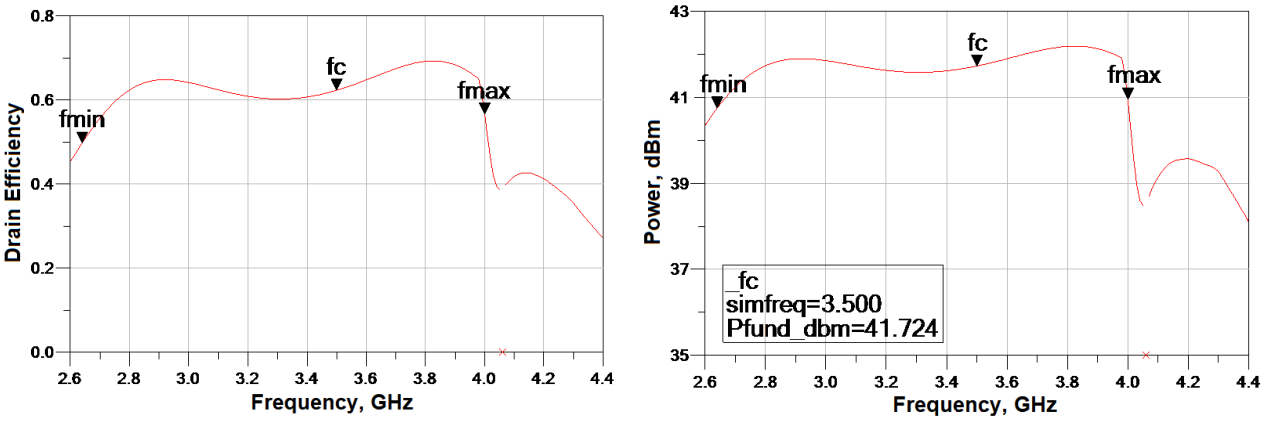
Table 2.3. Values for the Class B/J OMN.

C_0, pF	L_0, pH	C_1, pF	$L_{1'}$, pH	L_2, pH	C_2, pF	R_L, Ω
5.63	192	6.55	172	434	3.86	20.9



(a) (b)

Figure 2.20. Simulation results of Class B/J circuit after optimization & fine tuning: (a) effective input impedance, (b) impedance versus frequency from 2.5 GHz to 10 GHz.



(a) (b)

Figure 2.21. Simulation results of Class B/J circuit after optimization & fine tuning: (a) efficiency, (b) power (in dBm) versus frequency

The next step to improve the results was a modification of the OMN topology. Modified Class B/J topology has been shown in Figure 2.22. Here L_{comp} compensates parasitics C_p as in conventional Class B amplifier. L_{comp} and C_p make a parallel tank circuit that has infinite impedance for the center frequency. A series tank circuit consists of L_1 and C_1. It provides short only for the main frequency. This circuit still has higher bandwidth than the conventional Class B amplifier because the amplifier switches between classes B, J, and J*. The bandwidth depends on the quality factor of both tank circuits. Since parasitics are fixed, the quality of $L_{comp}C_p$ tank cannot be changed by adjusting only L_{comp}. However, it can be changed for L_1C_1 tank, and there is an optimal value for the highest bandwidth. The resonant frequency of both tank circuits has to be equal to the center frequency (f_c) of the amplifier. Final values after fine-tuning have been presented in Table 2.4. The circuit as entered into "Keysight ADS" schematics editor is shown in Figure 2.24 and Figure 2.25. As Figure 2.24 shows, despite 1 dB bandwidth decreased from 1360 MHz to 1280 MHz, now there is no such abrupt drop in efficiency at high frequencies. However, now 2nd harmonic termination is not present, so it has quite a high impedance, as shown in Figure 2.25. Attempts to add 2nd harmonic termination as an additional tank circuit didn't give better results.

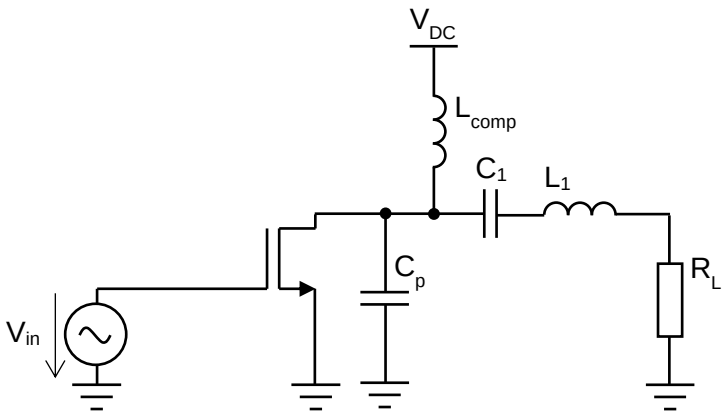


Figure 2.22. Alternative Class B/J topology.

Table 2.4. Values for the modified Class B/J OMN.

C_p, pF	L_{comp}, pH	C_1, pH	L_1, pH	R_L, Ω
5.63	368	1.38	1500	20.9

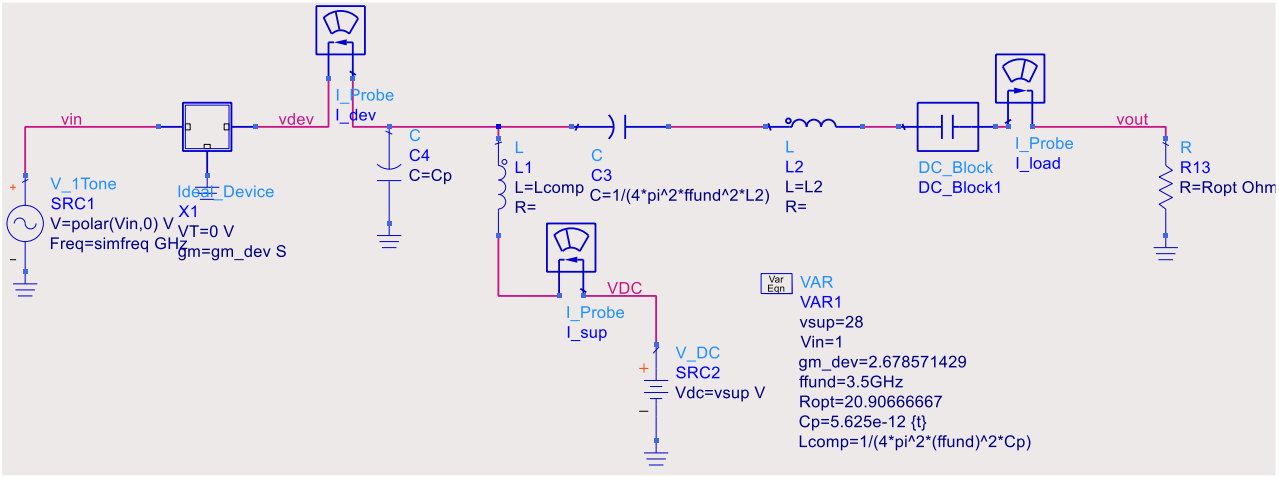
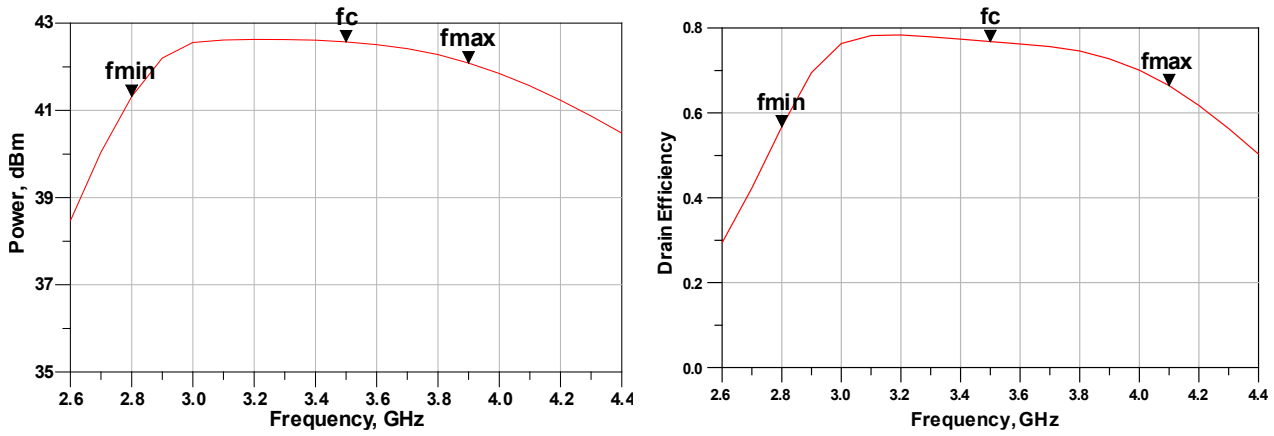


Figure 2.23. Final Class B/J circuit in “Keysight ADS” schematics editor.



(a) (b)

Figure 2.24. Final Class B/J circuit: (a) effective input impedance, (b) impedance versus frequency from 2.5 GHz to 10 GHz.

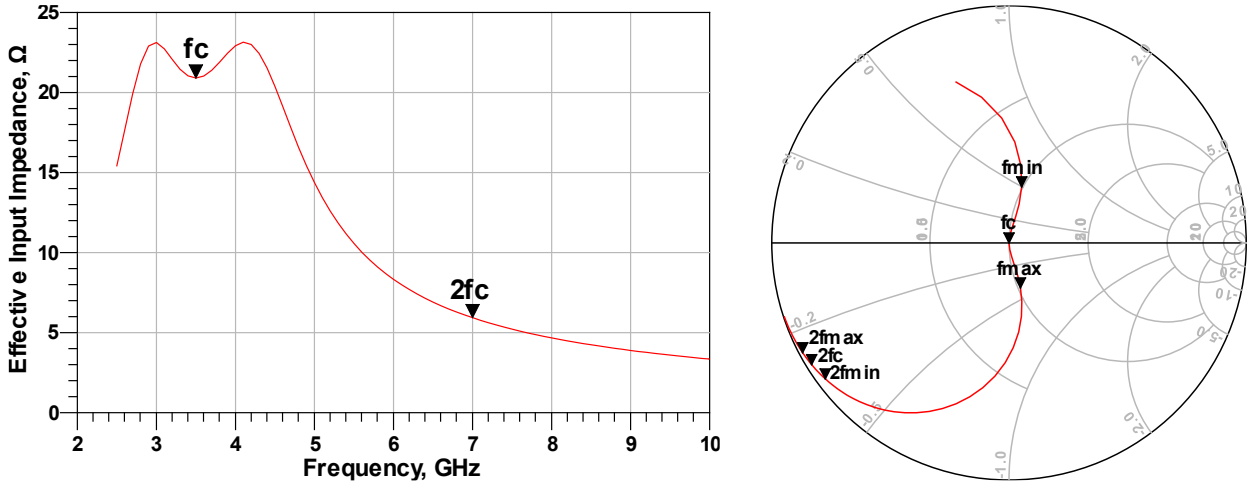


Figure 2.25. Simulation results of alternative Class B/J circuit after optimization & fine tuning: (a) effective input impedance, (b) impedance versus frequency from 2.5 GHz to 10 GHz.

2.5. Amplifier Classes in Digital Transmitters

Conventional analog-intensive transmitters suffer from poor integration and complicated design procedure while having severe linearity/efficiency trade-offs. Most digital transmitters (DTX) currently use conventional high-speed digital CMOS technologies, which are not suited for base station applications in output power and efficiency. These technologies are unfit to generate the required RF output power levels due to their low supply voltage. As a solution, the hybrid digital/analog approach has been invented. It is presented in Figure 2.26a. It can provide a peak output power of up to a few watts; however, it relies on an analog current-mode interface with the common-gate GaN PA output stage, yielding scaling limitations for higher frequencies and powers (e.g., above 10 W) [21].

To enable fully digital transmitter operation at higher output power levels, while avoiding high driver power consumption, a low voltage digital controller with high-speed to activate a segmented (V_T-shifted LDMOS) output stage (Figure 2.26b) could be used. Such a concept can achieve high (system) efficiencies, replacing the power-hungry analog-intensive transmitters [21].

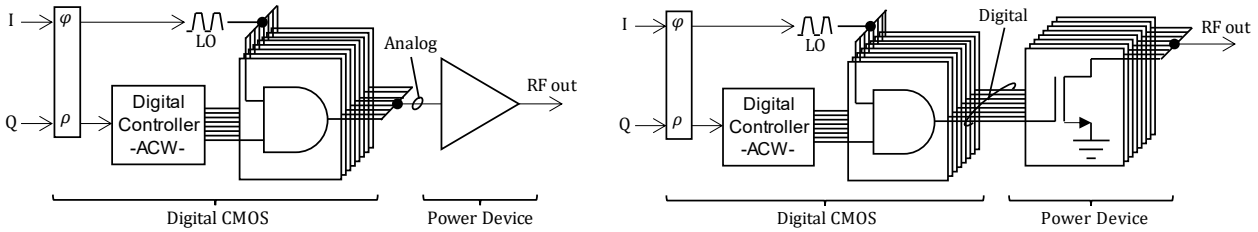


Figure 2.26. Concepts of DTXes when the input signal to the PA is (a) analog and when it is (b) digital [21]. Parasitics are not shown.

Analog power amplifiers are driven by a single continuous amplitude modulated RF signal. Amplitude modulation is implemented by varying the amplitude of the drive voltage. When DTX architecture, which is shown in Figure 2.26b is used, each segment (transistor) in the segmented device (transistor array) can be either “fully-on” or “fully-off”. As a result, a discretized current waveform can be generated at its (combined) output. This waveform is set by amplitude codeword (ACW), which is bitwise mixed with a square-wave (phase-modulated) local oscillator (LO) clock [21]. The number of active segments determines the amplitude. When these transistors are hard-driven and their combined R_{on} is significantly lower than the effective load impedance at the device plane, the output stage toggles between the off-state and linear (triode) region [22]. This is an important advantage versus analog amplifiers since quiescent currents can be avoided. In addition, the use of a more energy-efficient switch-mode of operation of the output stage devices is facilitated. The drains of

these devices are connected, so these devices can be interpreted as a single big device (transistor) whose activated gate width is proportional to the applied ACW. As a result, conventional amplifier topologies can be used with these segmented devices. High output power can be achieved if a high-breakdown voltage technology is used for the segmented devices [21].

One more advantage is that in DTX the effective gate width scaling is used (in contrast to scaling the input voltage in analog transmitters). In this way, disadvantages of conventional classes, such as gain expansion, especially noticeable in Class C amplifiers, can be avoided while still having Class C-like efficiency [22].

This project focuses on the power amplifier, so the rest of DTX can be significantly simplified. The simplification makes debugging more manageable, and simulations consume less time. Thus, in our simulations, segmented transistors are replaced with one big transistor, and a sinusoidal drive signal with normalized amplitude to 1 V is connected directly to the gate. Note that one could refine this later by selecting a square wave with a controlled duty cycle to enhance the transmitter efficiency. However, since this adds an extra degree of freedom (the duty-cycle) that affects the optimum loading conditions in the design, we have chosen to omit this refinement in favor of a clearer comparison with analog class-B oriented circuits.

2.6. Conclusion

Classes A, AB, B, and C are defined by their conduction angle. Class A amplifiers ideally do not introduce harmonics, they can have the best linearity even without harmonics termination, but their efficiency can reach only 50%. Meanwhile, Class C amplifiers have the worst linearity but can have the best efficiency. Class B amplifiers have higher efficiency (78%), but worse IM3 than Class A. Class AB is like a trade-off between classes A and B. It has a lower efficiency, but better IM3 than Class B. Class AB and Class B amplifiers can be used for non-sinusoidal signals with relatively (to Class C) low distortion if the push-pull configuration is used. Classes A and AB consume current even when the input signal is not present, while classes B and C do not.

Real transistors have parasitics. This work assumes that parasitics consist only of capacitance between the drain and the source. This capacitance has to be compensated. That can be done by using an inductor. However, in such a way, a tank circuit will be created. It can significantly limit the bandwidth, which depends on the quality factor of the LC tank. The load impedance is connected parallel to the tank circuit, which also influences the quality factor. When the quality factor is lower, bandwidth is higher. There is an output matching strategy that forces the amplifier to operate in Class B only at the center frequency. When such a matching network is designed correctly, the amplifier will work as Class J when the frequency is above the center frequency and as Class J^{-1} when it is below the center frequency.

3

DOHERTY AMPLIFIERS

Traditional amplifier classes provide maximum efficiency only at their full output power level. However, modern wireless signals feature high peak-to-average power ratios (PAPR). These digital communication signals use complex phase and amplitude modulation, i.e., in combination with orthogonal frequency division multiplexing (OFDM) techniques. Since drain efficiency is proportional to the output voltage swing, when a traditional amplifier class is used for such a high PAPR signal, the average efficiency will be much lower than the peak efficiency of this amplifier. However, Doherty amplifiers can provide high average efficiency also for signals that have a large PAPR.

The key topics in modern Doherty power amplifier research are efficiency and bandwidth. These are essential features since high-speed communication signals can be very wideband. Furthermore, it is attractive to have one PA, that can handle as many wireless channels as possible.

3.1. PRINCIPLE OF OPERATION

Conventional Doherty power amplifiers consist of two branch amplifiers that can be connected in parallel or series to the load, yielding two basic topologies, namely the “parallel connected load Doherty PA (PCL-DPA)” or the “series connected load Doherty PA (SCL-DPA)”. The most common is the PCL-DPA since a shunt connection appears to be more advantageous for most practical purposes because the load circuit is grounded, while in a SCL-DPA, the load is neither grounded nor balanced to the ground [14].

3.1.1. DOHERTY PA WITH PARALLEL CONNECTED LOAD (PCL-DPA)

A Doherty PA with parallel-connected load (PCL-DPA) is presented in Figure 3.1. One amplifier is called the main (a.k.a. carrier), the other is the peak (a.k.a. auxiliary). The main is always active, while the peak amplifier is activated only when the input signal rises above a certain threshold, see Figure 3.2. The original Doherty topology uses Class B amplifier as the main and Class C as the peak amplifier because this yields the simplest implementation. As explained in chapter 2, the conduction angle for a Class B amplifier is equal to π, while for Class C it is less than π. Thus, in Class

B the ideal active device is open during the whole positive swing[5]. In the design of Class C amplifier, one should choose the conduction angle below π. For Doherty peak amplifier design this angle should be chosen such a way that when the input swing rises above the decided threshold level (for example, take a look at the red horizontal line in Figure 3.2), the transistor in the peak amplifier starts to conduct. Then if one would connect main and peak amplifier inputs and apply a signal source, the main amplifier would be constantly active, and the peak amplifier will be activated only when the chosen threshold level is reached. Then outputs of these amplifiers have to be combined and delivered to the load R_L. When the peak amplifier activates, it causes an increase in the effective load impedance. Since the main amplifier has to experience a decrease of impedance, instead of an increase, an impedance inverter[6] is connected to the output of the main amplifier. However, it does not only invert impedance but also shifts phase by 90°. This shift is somewhat unwanted since signals from both amplifiers should reach the load in-phase. To align them back in phase at the load, a *phase aligner,* which also shifts by 90°, is connected to the input of the peak amplifier.

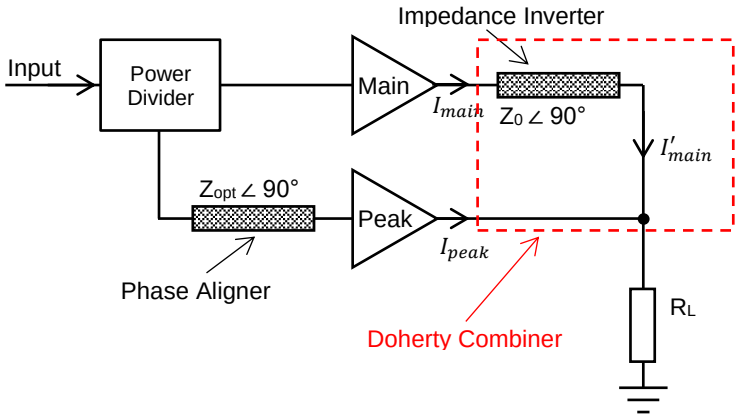


Figure 3.1. Block diagram of conventional parallel connected load Doherty power amplifier (PCL DPA).

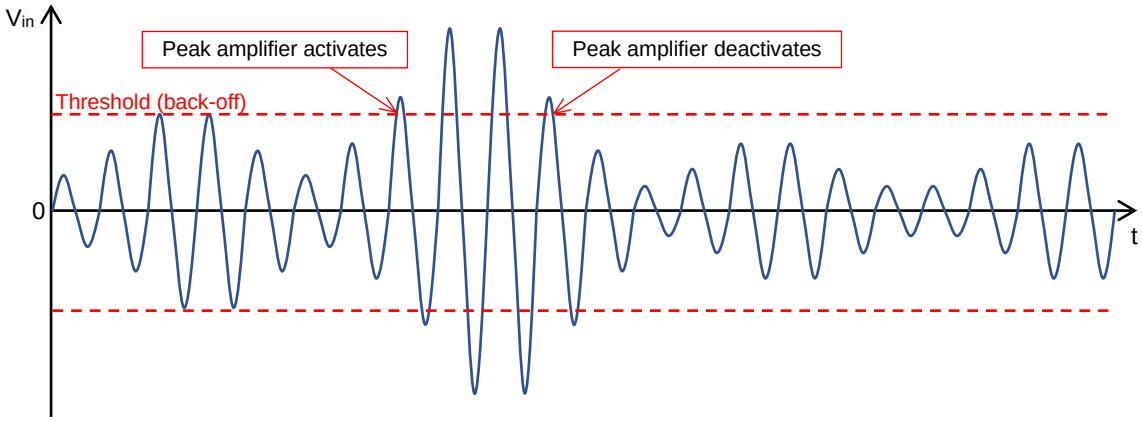


Figure 3.2. How the input signal activates peak amplifier.

The main amplifier should be designed to saturate at a certain threshold (back-off) level (Figure 3.2); in the case of symmetrical DPA design, the load impedance should be 2x higher than the load impedance of the whole Doherty amplifier R_L. The impedance inverter needs to transform the load to an impedance $R_L = R_{opt}/2$ when the peak amplifier is inactive. Consequently, the main amplifier sees an impedance $4R_L$ or $2R_{opt}$. Then as input signal magnitude increases from zero to back-off point, the main amplifier current I_{main} increases linearly while the peak amplifier stays inactive and does not deliver any current to the load ($I_{peak} = 0$). When the main amplifier saturates, the peak amplifier kicks in because the peak amplifier transistor starts to conduct when the main amplifier saturates. This

[5] In practice, transistors have threshold voltage so they have to be biased at threshold voltage in case to have conduction angle equal to π.
[6] Its operation is described in section 3.4.

operation is illustrated by Figure 3.3 plots (a) and (b). The input voltage at which the peak amplifier turns on ($V_{PBO} = 0.5 \cdot V_{in,max}$)[7] specifies the *output power back-off (PBO) point*. When input voltage rises above that point, the current provided by the peak amplifier I_{peak} starts to increase linearly. Then due to the current flowing from the peak amplifier, the effective load impedance R_L will increase. At the main amplifier output, this increase in effective impedance is seen, due to the impedance inverter, as decrease. This is represented in Figure 3.3c. The decreased load impedance forces the main amplifier to provide more current and RF power because the voltage at its output (V_{main}) stays constant. So, the currents from each amplifier (I_{main} and I_{peak}) continue to rise linearly (Figure 3.3a). Furthermore, voltage saturation is achieved for the main over an extensive range, so its efficiency remains high. This is crucial in this topology: maximum efficiency is reached at the threshold for the main, and it stays high as the input signal increases further. This is shown in Figure 3.4a. That threshold is called output power back-off level (PBO). At maximum input signal, both amplifiers are voltage saturated. The total output power is equal to the sum of powers delivered by each amplifier. Figure 3.4b compares drain efficiency of Doherty topology with the efficiency of the conventional Class B PA and denote Doherty PA advantage.

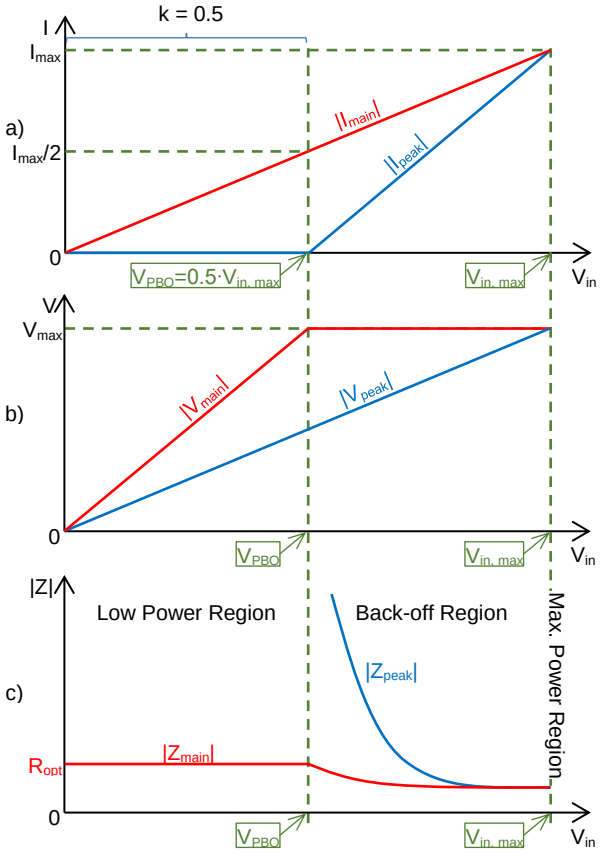


Figure 3.3. Doherty amplifier operation. a) drain currents, b) voltages at output of each amplifier, c) effective impedances. V_{OBO} is input voltage at a back-off. All values are magnitudes.

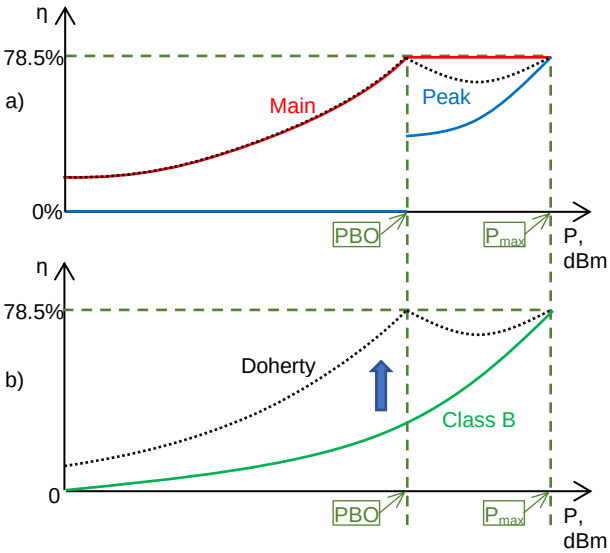


Figure 3.4. Amplifier efficiency versus input power [15]. a) Efficiencies of the main and the peak amplifiers separately and total efficiency of the whole Doherty PA; b) Comparison of Doherty and conventional Class B PA efficiencies.

Frequently in literature, the main and the peak amplifiers are replaced with current sources for analysis purposes. Then the circuit from Figure 3.1 turns to Figure 3.5a. Here current sources generate sine waves that have 90° phase difference. Current source values can only be adjusted according to Doherty PA operation profile; for example, see Figure 3.3a. Figure 3.5a shows currents, voltages, and impedances so it can be used to derive equations that characterize the change in the impedance experienced by the main amplifier due to the influence of the peak amplifier:

$$Z'_{main} = \frac{V_{peak}}{I'_{main}} = \frac{R_{opt}}{2} \cdot \left(\frac{I'_{main} + I_{peak}}{I'_{main}} \right) \qquad (3.1)$$

where R_{opt} is the optimum load impedance of the main (and the peak) amplifier when the Doherty PA works at maximum power. Then the impedance before the impedance inverter (seen by the main amplifier or, in other words, by the main current source) can be found by applying the following equation:

[7] Note that the multiplier 0.5 is only valid for so called *symmetrical* DPA. Symmetry will be explained in section 3.3.

$$Z_{main} = \frac{R_{opt}^2}{Z'_{main}} = \frac{2R_{opt}}{\left(1 + \frac{I_{peak}}{I'_{main}}\right)} = \frac{R_{opt}^2}{R_L} \cdot \frac{I'_{main}}{I'_{main} + I_{peak}} \tag{3.2}$$

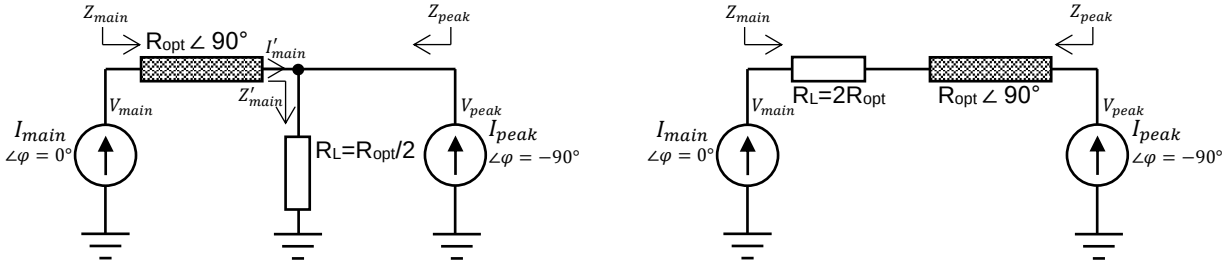
and the impedance seen by the peak amplifier:

$$Z_{peak} = R_L \left(1 + \frac{I'_{main}}{I_{peak}}\right). \tag{3.3}$$

Note that I'_{main} is constant above back-off because the impedance inverter turns constant V_{main} to constant I'_{main}.

3.1.2. Doherty PA With Series Connected Load (SCL-DPA)

A Doherty PA with a series-connected load is presented in Figure 3.5b. When the input signal is lower than PBO, only the current from the main-current source flows. The peak current source is disabled as in Figure 3.3a. The current source has infinite impedance. The impedance inverter changes this impedance to 0 Ω (short to ground). As a result, like in PCL-DPA the main amplifier (current source) is loaded with $2R_{opt}$. When the input signal rises above PBO, the terminating impedance of the impedance inverter is reduced, and since the input signal on the peak amplifier causes its output current to be opposite in phase to its potential, the terminating impedance provided by the peak amplifier is a negative shunt resistance [14]; that is the peak amplifier delivers power to the circuit. As the contribution of the peak amplifier increases, lowering the negative terminating resistance of the network, the input impedance of the network, which was initially zero, increases. This input impedance is a negative series resistance that reduces the impedance presented to the main amplifier from its initial value of 2R ohms. At the modulation peak, the peak amplifier contributes half of the total power (if the Doherty amplifier is symmetrical). Then the load impedance to the main amplifier is R ohms, and the main amplifier can supply twice the power than at PBO but still has maximum efficiency (Figure 3.4a) [14]. Consequently, the SCL-DPA operation plots look the same as for a PCL-DPA, i.e., Figure 3.3 and Figure 3.4.



a) b)

Figure 3.5. Simplified conventional symmetrical parallel (a) and series (b) connected load Doherty power amplifier topologies.

3.2. Comparison of PCL and SCL Doherty Topologies

High power PCL-DPA needs a low load impedance that is usually equal to half of the transistor's optimum impedance (R_{opt}). It can even be only a few ohms for high power (a few hundreds of watts) amplifiers, while typical RF loads have 50 Ω impedance[8]. Deviating from that 50 Ω value typically leads to a significant reduction in the realizable bandwidth. When the amplifier's output impedance is so low, output matching can be challenging. The complexity and size of the required output matching network can become impractical [16]. This results in more significant matching errors thus more reflections. The SCL-DPA needs a 4 times higher load impedance than PCL-DPA for the same output power, as it can be seen from Figure 3.5. Thus, it is likely that a real-life implementation of SCL-

[8] Commonly loads are antennas or other amplifier stages. 50 Ω is very common value because this is compromise between best power handling capacity (when 30 Ω) and lowest attenuation (when 77 Ω).

DPA can have a higher bandwidth than PCL-DPA. SCL-DPA topologies are very popular in integrated circuits (ICs). This is primarily because of the inherently differential nature of most ICs; SCL-DPA can utilize the inherent virtual ground of differential circuitry, which is typically needed to reduce losses due to poor ground contact in the standard RF CMOS process [16].

However, SCL-DPA also has significant disadvantages. Namely, in SCL-DPA the load is neither grounded nor balanced to the ground, while in PCL-DPA, it is grounded [14]. Classical SCL-DPA is unsuitable for high-frequency operation because transistor parasitics cause a significant phase shift at the package plane. Thus, the assumption that the current source of the main amplifier is connected directly to the load at high frequencies is invalid [16]. A new output combiner topology has to be introduced to solve this problem like it is done in [16].

Furthermore, conventional PCL-DPA and SCL-DPA do not allow for a change in load impedance R_L without changing voltage or current profile. This was improved later by inserting 2 additional quarter wavelength transmission lines [16]. The resulting topologies are called inverted Doherty PAs, and they will be discussed in section 3.6.2.

3.3. Asymmetrical Doherty Power Amplifiers

Note that all presented operation plots (Figure 3.3) apply only to *symmetrical* Doherty power amplifiers, i.e., where the main and peak amplifiers contribute equally when the applied input voltage is maximum. For example, in 50 W symmetrical Doherty PA at the maximum input voltage, the main and the peak amplifier both contribute 25 W. Originally, Doherty PAs were symmetrical [14].

In *asymmetrical* Doherty PA, contributions of the main and the peak amplifiers to output power are not equal even when the input signal is equal to the maximum supported. Examples of asymmetrical DPA operation plots are shown in Figure 3.6. Since different kinds of signals have different PAPR, such Doherty PAs are also widely used. The (a)symmetry is characterized by the *high-efficiency output power back-off level* parameter (k) which can be defined as (Figure 3.6a),

$$k = \frac{V_{PBO}}{V_{in,max}} \tag{3.4}$$

where V_{PBO} is the input voltage at the power back-off, $V_{in,max}$ is the maximum input voltage. Note that I_{main} increases linearly with the input. Meanwhile, the related output power increases quadratically. Thus, the power back-off factor (k) can also be expressed as:

$$k = \sqrt{\frac{P_{PBO}}{P_{max}}} \tag{3.5}$$

where P_{max} is the maximum output power, P_{PBO} is the output power at back-off. k is usually is expressed in decibels (k_{dB}). The relationship between k and k_{dB} is,

$$k = 10^{-k,dB/20}. \tag{3.6}$$

Remember that the peak amplifier is off at high-efficiency power back-off; thus, only the main is active and works at its full power. As a result, then the output power provided by the DPA is equal to power provided by the main amplifier and is equal to P_{PBO}. (3.5) and (3.6) can be used to derive equation (3.7), which is very convenient during the design procedure because the back-off level is usually given in decibels, and this value of power at back-off (P_{PBO}) is important to further design steps.

$$P_{out@back} = P_{main@back} = P_{PBO} = 10^{-k,dB/10} \cdot P_{max} \tag{3.7}$$

Typical power back-off level (k_{dB}) values are 6 dB, 9 dB, 10 dB, 12 dB. k_{dB} for a symmetrical Doherty PA is 6 dB, which corresponds to 0.5 in linear scale. For asymmetrical arbitrary case $k \neq 0.5$. The power provided by each amplifier can be expressed by (2.7). As Figure 3.6a shows, when the input voltage is maximum, the drain current is highest, and it is equal to $I_{main@max}$ while at back-off drain current is equal to $k \cdot I_{main@max}$. Thus,

$$P_{main@max} = \frac{P_{main@back}}{10^{-k,dB/20}}. \tag{3.8}$$

Since each amplifier contributes by some amount of power when the input signal is at its highest value, the power delivered by the peak amplifier at the maximum input signal is

$$P_{peak@max} = P_{max} - P_{main@max}. \tag{3.9}$$

The load impedance of the main amplifier at the back-off and the maximum power can be found using (2.13). At back-off $I_{peak} = 0$ thus (3.2) becomes

$$Z_{main@back} = \frac{R_{opt}^2}{R_L} \tag{3.10}$$

and at maximum power $I_{peak} = I_{peak@max}$ and $I_{main} = I_{main@max}$ so then (3.2) becomes

$$Z_{main@max} = \frac{R_{opt}^2}{R_L} \cdot \frac{I'_{main@max}}{I'_{main@max} + I_{peak@max}}. \tag{3.11}$$

Note that R_{opt} in Figure 3.5c is the optimum load impedance of the *main* amplifier at the *maximum* output power.

It can be seen from Figure 3.5a that the current after the impedance inverter can be expressed as

$$I'_{main} = \frac{V_o}{R_L} - I_{peak} \tag{3.12}$$

where V_o is voltage swing at the load. At the maximum power $V_o = V_{sup}$ and $I_{peak} = I_{peak@max}$. Then the following equation system can be written from (2.13), (3.5) and (3.10)-(3.12):

$$\begin{cases} \dfrac{V_{sup}^2}{2k^2 P_{max}} = \dfrac{R_{opt}^2}{R_L} \\ \dfrac{V_{sup}^2}{2P_{max}} = \dfrac{R_{opt}^2}{V_{sup}} \cdot \left(\dfrac{V_{sup}}{R_L} - I_{peak@max} \right) \end{cases} \tag{3.13}$$

Then from this system of equations, the design equations for the calculation of R_{opt} and R_L can be obtained:

$$R_{opt} = V_{sup}/I_{main@max}\,; \tag{3.14}$$

$$R_L = kR_{opt}. \tag{3.15}$$

In this work, we focus on symmetrical amplifiers because they are more intuitive than asymmetrical.

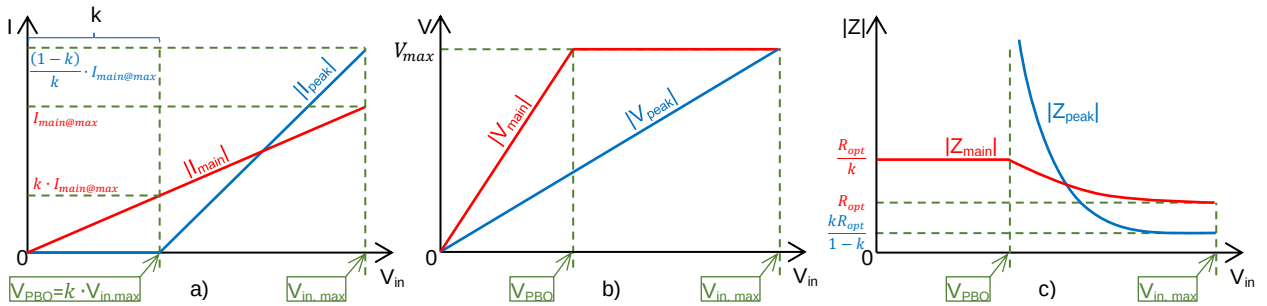


Figure 3.6. Asymmetrical ($k \neq 0.5$) Doherty amplifier operation. a) drain currents, b) voltages at output of each amplifier, c) effective impedances. V_{OBO} is input voltage at a back-off. All values are magnitudes.

3.4. Impedance Inverter

Before jumping into the design procedure, we should discuss how an impedance inverter works and how it can be designed. Usually, it is a quarter wavelength (λ/4 or 90° electrical length) transmission line, also known as λ/4 transformer or its lumped equivalent.

3.4.1. Transmission Lines

A transmission line, in general, is a conductor designed to conduct electromagnetic waves. It is a specific type of waveguide. A transmission line can be made on-chip, on PCB as a track, or a cable. Transmission line theory is relevant when the signal wavelength is in the same order or shorter than the length of the transmission line. A transmission line can be represented as an infinite number of infinitesimally small sections of a lumped network that are connected in a cascade. Such a section is shown in Figure 3.7. Here R represents the distributed resistance of the conductor (expressed in ohms per unit length), L is the distributed inductance of the conductor. The inductance results from the magnetic field around the tracks or wires, measured in henries per unit length. C is the distributed capacitance between the conductors (in farads per unit length). G is the distributed conductance of the wire insulator or the substrate. L, C, G, and R can be frequency-dependent. For an ideal lossless transmission line R and G is 0. An ideal transmission line is defined by its characteristic impedance, (electrical) length, and related reference frequency. For implementing a transmission line as a PCB trace, with a given impedance and electrical length, the physical line width and length must be found based on the substrate parameters. These calculations require complex EM calculations, so design tools are often used, such as “LineCalc” from “Keysight ADS.” However, existing equations and even design tools are limited and cannot be used in all cases. In such cases, the heuristic design approach is the fastest way to go.

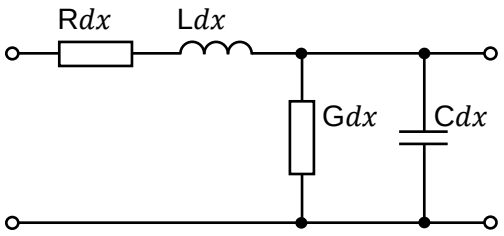


Figure 3.7. Schematic representation of the elementary component of a transmission line.

The transmission line characteristic impedance Z_0 is the ratio of the amplitude of a single voltage wave to its current wave. Because most transmission lines also have a reflected wave, the characteristic impedance is generally not the impedance that is measured on the line. The impedance at given length l from the load Z_L (see Figure 3.8) can be expressed as:

$$Z_{in}(l) = \frac{V(l)}{I(l)} = Z_0 \cdot \frac{Z_L + Z_0 \tanh(\gamma l)}{Z_0 + Z_L \tan(\gamma l)} \qquad (3.16)$$

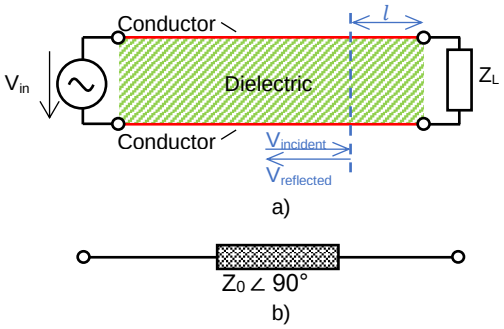


Figure 3.8. Transmission line (a) and its schematic representation (b).

where γ is the propagation constant (it is a measure of the change undergone by the amplitude and phase of the wave as it propagates in a given direction). In this chapter we will deal only with ideal transmission lines. For this ideal case, it is always:

$$\gamma = j\beta \qquad (3.18)$$

where β is a wavenumber:

$$\beta = \frac{2\pi}{\lambda} \qquad (3.17)$$

Where λ is the wavelength. From the equations (3.16), (3.18), and (3.17) we can get (3.19), which is very widely used in calculations:

$$Z_{in}(l) = Z_0 \cdot \frac{Z_L + jZ_0 \tan(\beta l)}{Z_0 + jZ_L \tan(\beta l)} \qquad (3.19)$$

where βl is the electrical length. We will use (3.19) to derive an equation for the impedance transformer (a.k.a. λ/4 transformer; it has 90° electrical length). The relationship between electrical length and transmission line length:

$$\beta l = \frac{2\pi}{\lambda} \cdot \frac{\lambda}{4} = \frac{\pi}{2} = 90°. \tag{3.20}$$

If we will fill-in $\beta l = 90°$ or $l = \lambda/4$ and calculate the limit (because $\tan(90°) = \infty$):

$$Z_{in} = \lim_{\beta l \to \pi/2} \left(Z_0 \cdot \frac{Z_L + jZ_0 \tan(\beta l)}{Z_0 + jZ_L \tan(\beta l)} \right) = Z_0 \cdot \frac{jZ_0}{jZ_L} = \boldsymbol{\frac{Z_0^2}{Z_L}}.$$

So:

$$Z_{in} = \frac{Z_0^2}{Z_L}. \tag{3.21}$$

Equation (3.21) shows how impedance inverter works. For example, if Z_L is ∞, Z_{in} is 0 ohm.

3.4.2. Lumped Equivalent

As mentioned in the previous section, a transmission line can be represented as an infinite number of infinitesimally small sections of a lumped network connected in a cascade. One such section is shown in Figure 3.7. If this number of sections would be finite, the lumped circuit could still approximate the transmission line but less precisely. However, lumped equivalents of transmission lines are frequently used in practice because they have certain advantages. The most important benefit is that they can be very small, even at low design frequencies where transmission lines may have enormous dimensions due to the wavelength involved. Another advantage is that parasitic capacitances of other components (e.g., transistors) can be absorbed in the network to implement the shunt capacitors in their lumped equivalent. Then these reused parasitic capacitances would not limit the bandwidth. This technique is applied many times in this research. In some projects, parasitic inductances could be used as inductors, but that was not done in this work. Sometimes even a single section is enough to have a reasonably good lumped equivalent. Figure 3.9a shows a single section π equivalent (called so because the circuit resembles letter π). Note the difference between Figure 3.7 and Figure 3.9a: a capacitor has to be added to the left side to make the network symmetrical. Theoretically, π equivalent should be exactly equivalent of a transmission line only at a center frequency.

However, the approximation is still valid for the bandwidth at its neighborhood region. Better approximation over wider bandwidth is obtained if more sections are used, e.g., Figure 3.9b. Equivalents that represent the letter T also exist, and they are called respectively. Since DC can flow from input to output (Figure 3.9), these equivalent networks are called *low-pass*. *High-pass* lumped equivalents also exist. They can be obtained by interchanging inductors and capacitors. *High-pass π equivalent* and T equivalents are not used in this project.

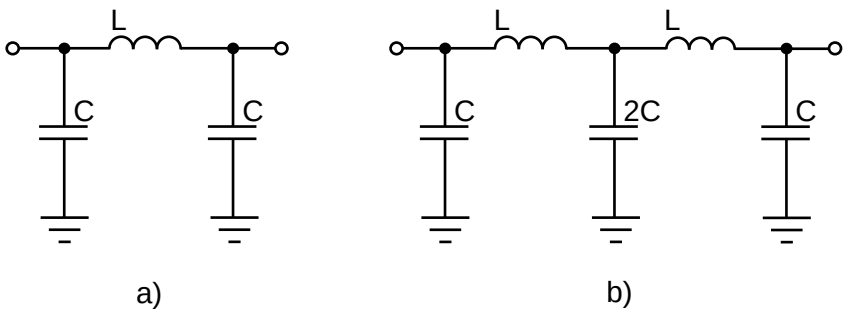


Figure 3.9. Low pass π lumped equivalents of transmission lines.
a) poor equivalent, b) better equivalent

Series inductor values for circuits in Figure 3.9 can be calculated using [23]

$$L_S = \frac{Z_0}{2\pi f_0} \cdot \sin\theta \tag{3.22}$$

where Z_0 is the characteristic impedance, f_0 is the design frequency, θ is the electrical length in radians. Shunt capacitor values can be calculated using (3.23) [23].

$$C_P = \frac{1 - \cos\theta}{2\pi f_0 Z_0 \sin\theta} \tag{3.23}$$

An impedance inverter (λ/4 transformer) has 90° electrical length. If we substitute this electrical length in (3.22) and (3.23) we get equations (3.24) and (3.25), which can be used to calculate values of lumped elements for a lumped version of the impedance inverter, which would look like Figure 3.9a.

$$L_S = \frac{Z_0}{2\pi f_0} \tag{3.24}$$

$$C_P = \frac{1}{2\pi f_0 Z_0} \tag{3.25}$$

If more equivalent lumped network sections are needed to approximate a piece of transmission line (e.g., 90°), more than one section can be used, e.g., 2 (like Figure 3.9b), in which the sections now need to have $90°/2 = 45°$ electrical length. Values can be found by applying (3.22) and (3.23).

3.5. Design Procedure

This section describes the design procedure of conventional Doherty power amplifiers with parallel and series-connected loads. Although this work focuses on symmetrical Doherty amplifiers, equations that can also be used for asymmetrical amplifiers were used during the design procedure. Also shown are possible push-pull and differential implementations of these topologies. After introducing the design procedures, the simulation results are presented and compared.

Let's assume that the amplifier with the following specifications has to be designed:

- Supply voltage (V_{sup}): 28 V;
- Class B device operation;
- Output power back-off (PBO): 6 dB;
- Maximum output power (P_{max}): 50 W or 47 dBm;
- Center frequency (f_c): 3.5 GHz;
- 1 dB power and efficiency bandwidth: 1 GHz;
- 3rd intermodulation product (IM3): ≤ 60 dBc.

For the LDMOS technology, we assume:

- Maximum current per 1 mm LDMOS transistor (I_{DSmax}): 0.15 A/mm;
- Transistor parasitic capacitance between drain and source (C_{DSmm}): 0.313 pF/mm;
- The breakdown voltage is 64 V.

For this design, we assume that the input voltage swing (V_{in}) is normalized to 1 V. In practice, LDMOS technology needs higher V_{in}.

Unless specified otherwise, these specifications are used for the rest of this project (here and in the following chapters).

3.5.1. With Parallel Connected Load

This subsection introduces some of the possible implementations of Doherty PA with the parallel-connected load. The main and/or the peak amplifier can be implemented as a single transistor, like in Figure 3.33. If Class B operation is needed, then each amplifier can also use push-pull configuration. Such configuration can have better linearity. Figure 3.33 shows the circuit when the main amplifier is push-pull and the peak amplifier is a conventional single transistor in Class B.

3.5.1.1. Basic

The most straightforward basic parallel connected load Doherty PA implementation is shown in Figure 3.10.

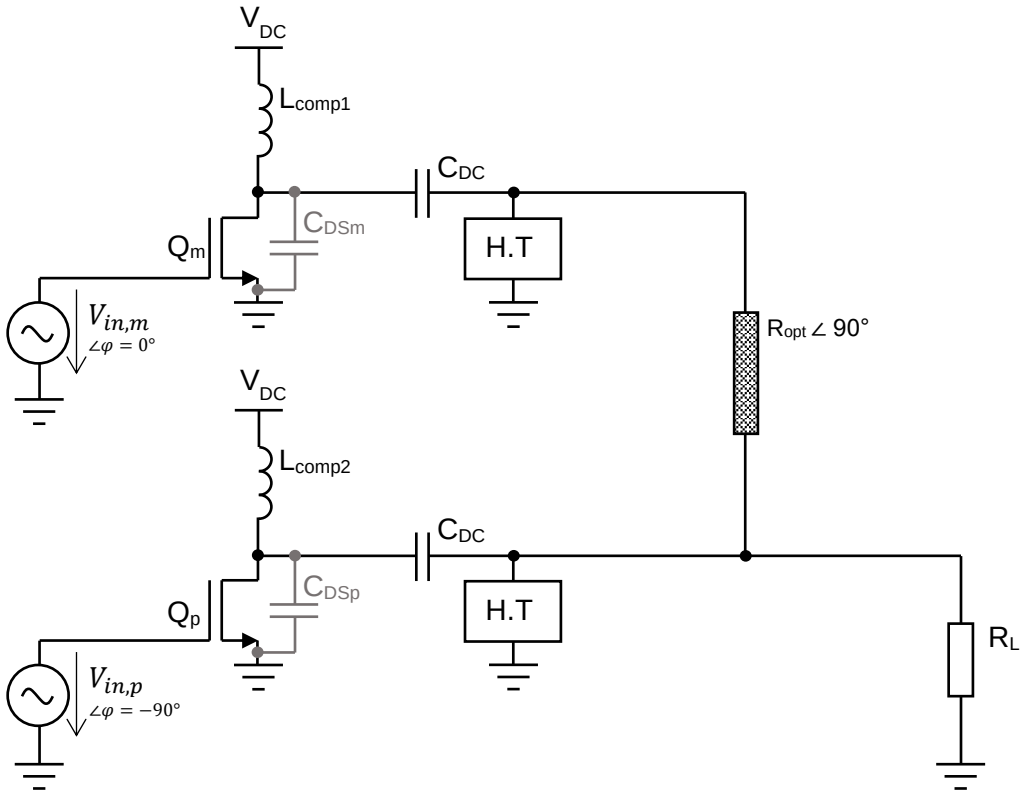


Figure 3.10. Single-ended parallel connected load Doherty PA (PCL-DPA) circuit diagram.

Using provided specifications and filling in equations (2.13), (2.18), (2.20), (3.7)-(3.11), (3.14), and (3.15), the values presented in Table 3.1 can be obtained. The design procedure is as follows (note that indices $@back$ and $@max$ means values at back-off and at the maximum power respectively):

1. Calculate high-efficiency output power back-off level: $k = 10^{-k,dB/20} = 10^{-6/20} = 0.5$.
2. Powers for the main and peak amplifier:
   $P_{main@back} = P_{max}k^2 = 50 \cdot 0.5^2 = 12.6\,W$;
   $P_{main@max} = P_{main@back}/k = 12.6/0.5 = 25\,W$;
   $P_{peak@max} = P_{max} - P_{main@max} = 50 - 25 = 25\,W$.
3. Drain current of the main and peak amplifier:
   $I_{main@max} = 2P_{main@max}/V_{sup} = 2 \cdot 25/28 = 1.79\,A$;
   $I_{peak@max} = 2P_{peak@max}/V_{sup} = 2 \cdot 25/28 = 1.79\,A$.
4. Transconductances:
   $g_{m,main} = \frac{2I_{main@max}}{V_{in}} = \frac{2 \cdot 1.79}{1} = \mathbf{3.57\,S}$;
   $g_{m,peak} = \frac{2I_{peak@max}}{V_{in}} = \frac{2 \cdot 1.79}{1} = \mathbf{3.57\,S}$.
5. Load impedance:
   $R_{opt} = V_{sup}/I_{main@max} = \frac{28}{1.79} = \mathbf{15.6\,\Omega}$;
   $R_L = kR_{opt} = 0.5 \cdot 15.6 = \mathbf{7.84\,\Omega}$.
6. Parasitic capacitance & its compensation (values are the same for each branch due to symmetry):
   $W_g = 2I_{main\&peak@max}/I_{D,max/mm} = 2 \cdot 1.79/0.15 = 23.9\,mm$;
   $C_{DS,main\&peak} = W_g \cdot C_{DS/mm} = 23.9 \cdot 0.313 = 7.5\,pF$;

$$L_{comp} = \frac{1}{4\pi^2 f_c^2 C_{DS}} = \frac{1}{4\pi^2 \cdot \left(3.5 \cdot 10^9\right)^2 \cdot 7.5 \cdot 10^{-12}} = \mathbf{276\ pH}.$$

Note that more precise values have been used during the calculations, so there might be minor deviations in the numbers provided.

Table 3.1. Component values for PCL-DPA.

$g_{m,\,main}$, S	$g_{m,\,peak}$, S	R_{opt}, Ω	R_L, Ω	$C_{DS,\,main}$, pF	$C_{DS,\,peak}$, pF	$L_{comp,\,main}$, pH	$L_{comp,\,peak}$, pH
3.57	3.57	15.6	7.84	7.5	7.5	276	276

The circuit from Figure 3.10 has been entered into “Keysight ADS” schematics editor (see Figure 3.11) and 31st order harmonic balance simulation has been performed.

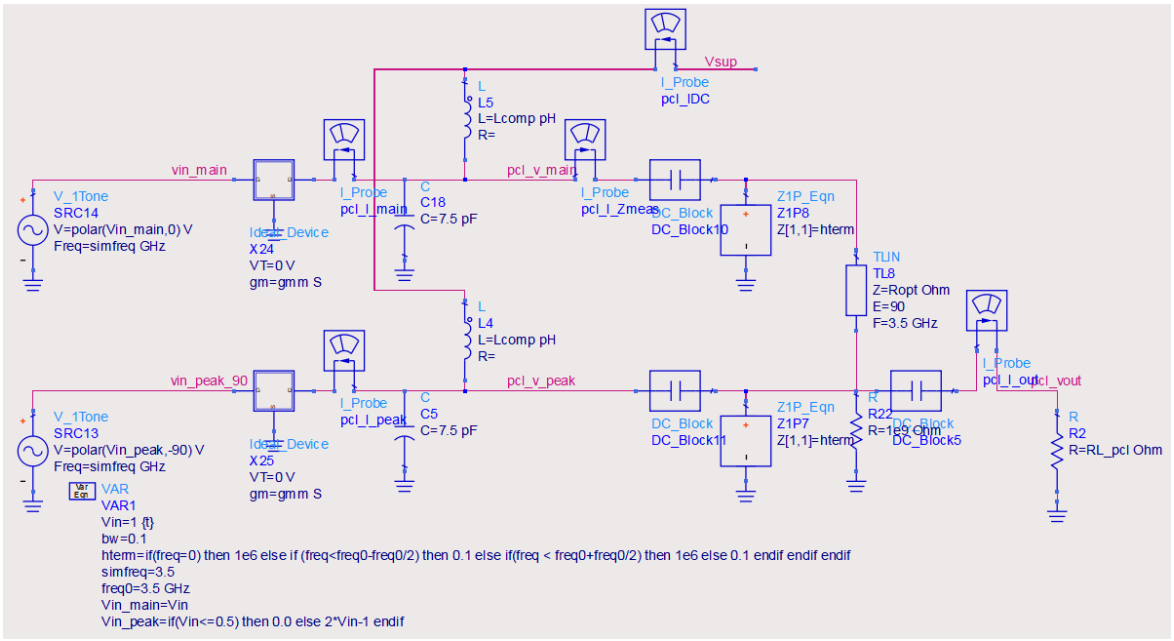


Figure 3.11. PCL-DPA circuit in “Keysight ADS” schematics editor. Prepared for simulations.

According to the harmonic balance simulation results, the designed PCL Doherty PA works properly because its plots (Figure 3.14) show the correct Doherty operation, i.e., it matches the theory described in subsection 3.1.1, Figure 3.3, and Figure 3.4. Load-lines in Figure 3.18 and Figure 3.19 corresponds load-line of the usual Class B power amplifier. Thus, both amplifiers work in Class B as expected. Judging by Figure 3.24 AM to AM and phase distortion is insignificant. AM to AM distortion (AM) is calculated by

$$AM = \left|\frac{V_{out}}{V_{in}}\right| \tag{3.26}$$

and phase distortion (PD) by

$$PD = \arg\left(\frac{V_{out}}{V_{in}}\right) \tag{3.27}$$

where V_{in} and V_{out} are input and output voltages to the whole Doherty PA.

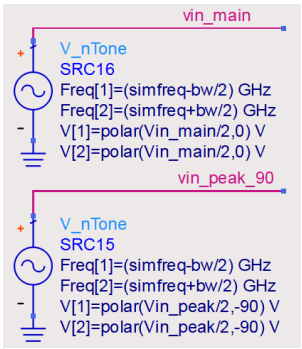


Figure 3.12. Input signal sources for 2-tone test.

According to specifications, this amplifier has to be very wideband. In other words, it should be suitable for signals which take considerable bandwidth. It should not distort these signals to an unacceptable level but only amplify them. When the input signal is high (near to maximum), the amplifier starts to compress and signal distortion increases. A 2-tone test is suitable for checking such distortion. For this test, two tones are passed to the input of the main and the peak amplifier. Figure 3.12 shows how input signal sources were set for this test. These two tones simulate a wideband signal. As seen from the figure, each tone has to be 2 times smaller than the total input signal. Spacing between them, in reality, corresponds to a wideband signal bandwidth. Intermodulation distortion occurs when such an input signal is high enough for the amplifier to go into compression. Nonlinearities in the rest of a circuit also contribute. As a result, at the output many additional tones will be present, as it is shown in Figure 3.13. The highest unwanted tones result from 2nd (see gray color) and 3rd (shown in red) intermodulation products. However, 2nd order products are not very important because they are far away from the signal. However, 3rd order products (IM3) are near the fundamental tones and on top of them (see red arrows in Figure 3.13). The IM3 products, which are on top of the fundamental tones, are very small and can often be neglected (except in higher-order modulation schemes), while the ones around them are very important and can contribute significantly to overall ACPR distortion. IM3 can be calculated in decibels with respect to carrier using (3.28). Where P_{fund} is the total output power of the fundamental 2 tones and P_{IM3} is total power of IM3 products which are on the left and on the right side of the fundamental tones.

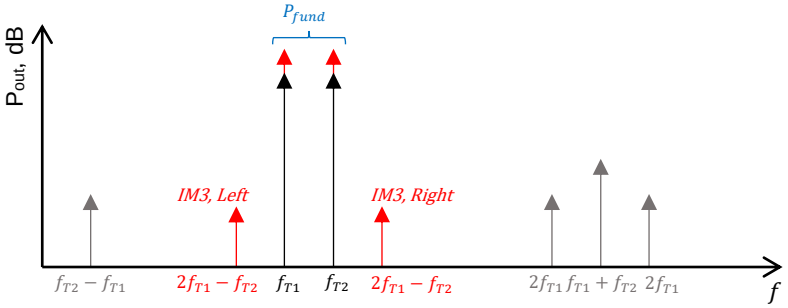


Figure 3.13. 2-tone test in frequency domain. Illustration for IM3 calculation.

$$IM3_{dBc} = 10\log_{10}\left(P_{IM3}/P_{fund}\right) \tag{3.28}$$

The resulting 3rd intermodulation product (IM3) is also very small, according to Figure 3.25, indicating good linearity. The harmonic balance simulation order for each signal source was set to 11 because this gives quite precise results, and the related simulation does not take long.

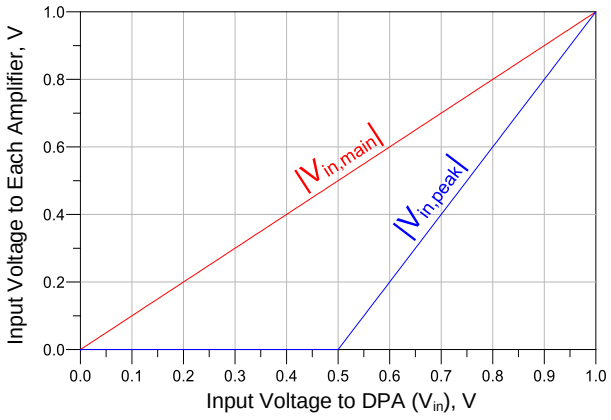


Figure 3.14. Input voltage levels for the main (red curve) and the peak (blue curve) amplifiers versus input voltage to the whole PCL-DPA. 1-tone test.

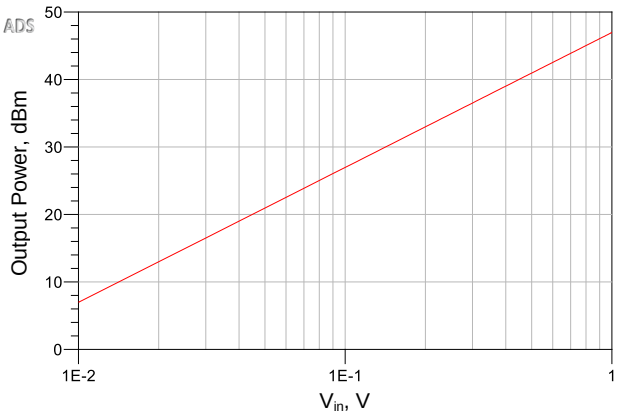


Figure 3.15. Output power versus input voltage for PCL-DPA. 1-tone test.

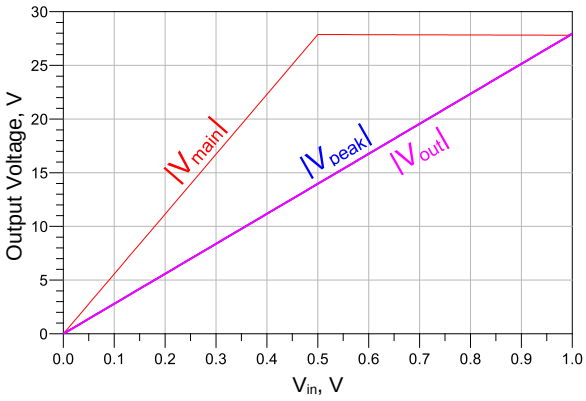


Figure 3.16. The output voltage of the main (red curve), of the peak (blue curve) amplifiers, and voltage on the load (magenta curve) versus input voltage for PCL-DPA. 1-tone test.

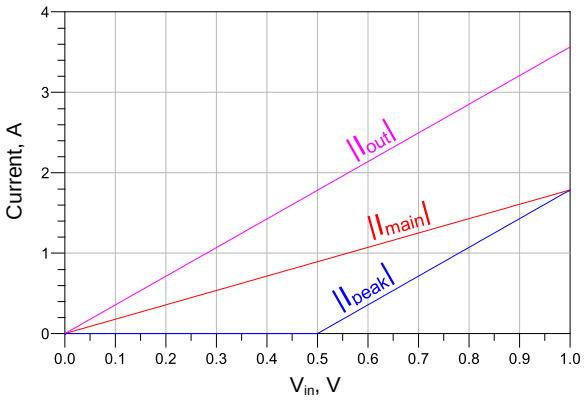


Figure 3.17. Output currents of the fundamental tone. Red curve is for the main amplifier, blue curve is for the peak amplifier, and the magenta curve is for the whole PCL-DPA. 1-tone test.

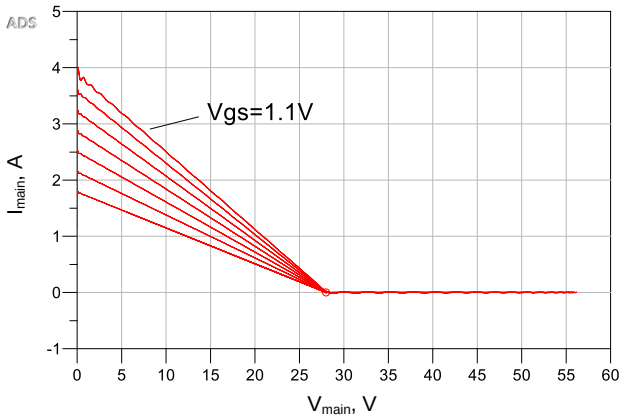


Figure 3.18. Load-line of the main amplifier's transistor. 1-tone test.

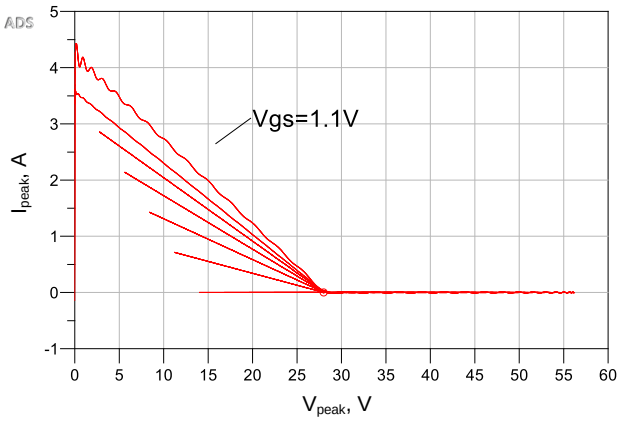


Figure 3.19. Load-line of the peak amplifier's transistor. 1-tone test.

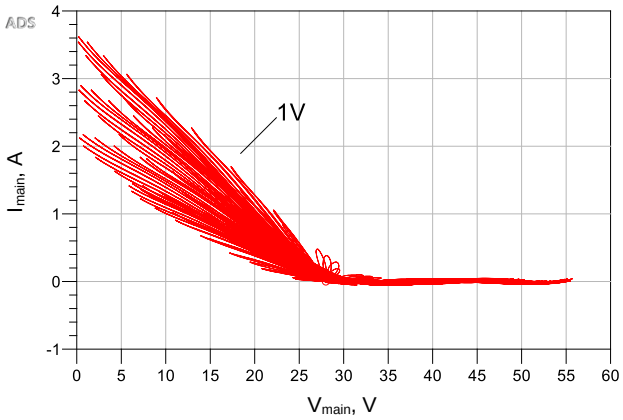


Figure 3.20. Load-line of the main amplifier's transistor. 2-tone test.

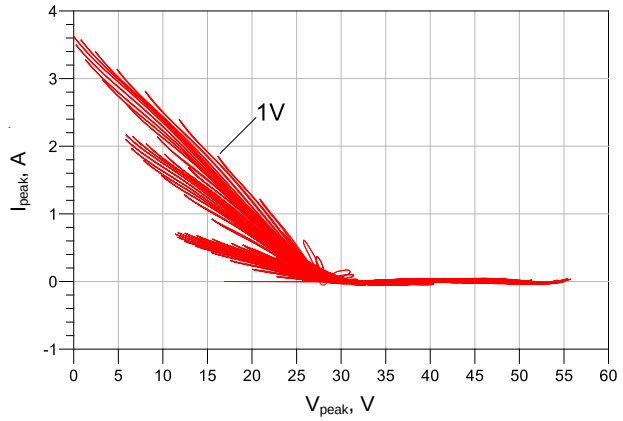


Figure 3.21. Load-line of the peak amplifier's transistor. 2-tone test.

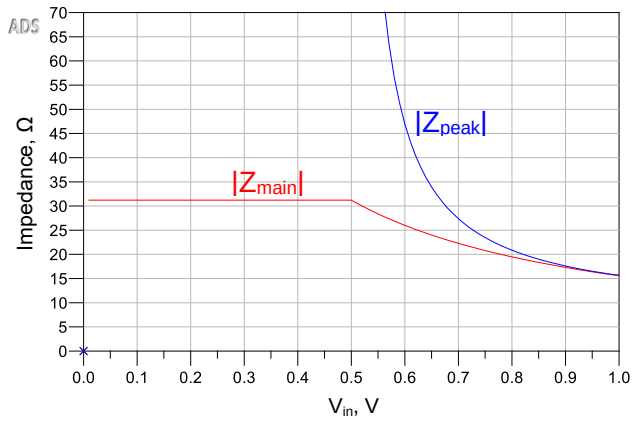


Figure 3.22. Effective load impedance for the main (red curve) and for the peak (blue curve) amplifiers.

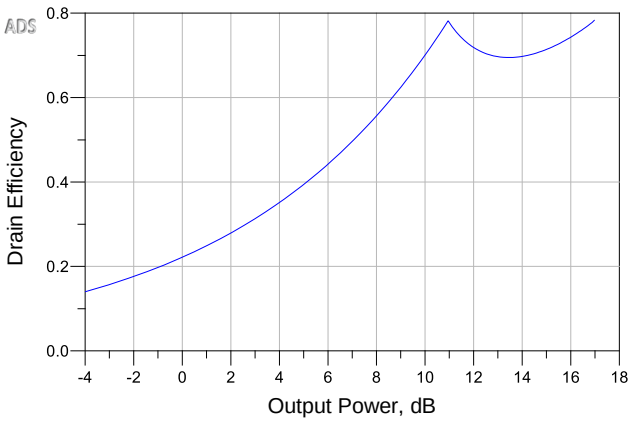


Figure 3.23. Drain efficiency versus output power.

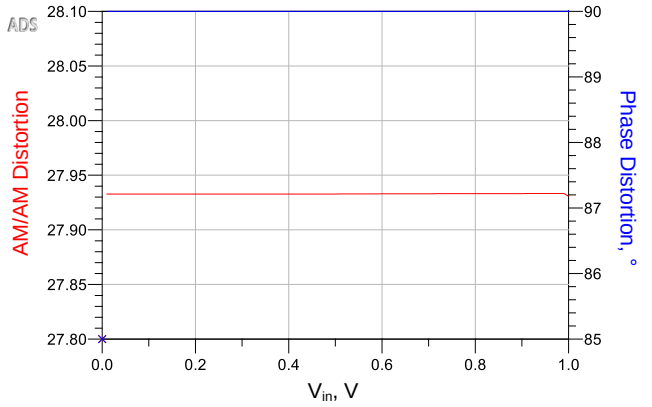


Figure 3.24. AM to AM (red) and phase (blue) distortion. A transmission line has been used as an impedance inverter.

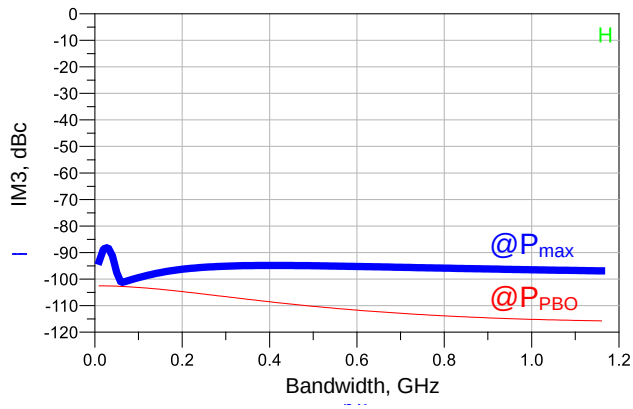


Figure 3.25. IM3 in dBc (decibels with respect to carrier) versus bandwidth (tone spacing). The red curve is at back-off, and blue is at maximum power. A transmission line has been used as an impedance inverter.

From the bandwidth plots (see red curves in Figure 3.27 to Figure 3.30), we see that 1 dB bandwidth is only 360 MHz at the back-off and 530 MHz at the maximum power. This is way too low to satisfy specifications. This bandwidth is limited by transistor output capacitances, which, together with compensation inductors, result in LC tank circuits. On top of this, there are bandwidth restrictions imposed by the impedance inverter. However, as mentioned, the impedance inverting transmission line can be replaced with its lumped equivalent. If the equivalent from Figure 3.9a is used, we end up with two shunt capacitors. After replacing these capacitors by reusing the parasitic capacitors C_{DSm} and C_{DSp}. Thus, the additional capacitors can be avoided. Only a smaller part of the output capacitance needs to be compensated by the inductor. Figure 3.26 illustrates how this is done. Here is assumed that the parasitic capacitances are bigger than the capacitor values required by the lumped equivalent. It could also be possible that these capacitors are smaller than the needed lumped shunt capacitors of the lumped equivalent network. In that case, inductive compensation will not be necessary, and additional capacitors will have to be added. Then the bandwidth will be limited only by the impedance inverter because the parasitic transistor capacitances will be completely reused.

The inductor and required shunt capacitance values for the lumped equivalent can be calculated using (3.24) and (3.25) respectively:

$$L_S = \frac{Z_{opt}}{2\pi f_c} = \frac{15.6}{2\pi \cdot 3.5 \cdot 10^9} = \mathbf{711\ pH};$$

$$C_P = \frac{1}{2\pi f_c Z_{opt}} = \frac{1}{2\pi \cdot 3.5 \cdot 10^9 \cdot 15.6} = \mathbf{2.91\ pF}.$$

Thus, the parasitic capacitances (7.5 pF for each transistor) are much higher than the lumped equivalent required. The method shown in Figure 3.26 can compensate a part of the parasitic capacitances and reuse the remaining part for the lumped equivalent. Then the inductor's value:

$$L_{comp} = \frac{1}{4\pi^2 f_c^2 (C_{DS} - C)} = \frac{1}{4\pi^2 \cdot 3.5 \cdot 10^9 \cdot (7.5 - 2.91) \cdot 10^{-12}} = \mathbf{450\ pH}.$$

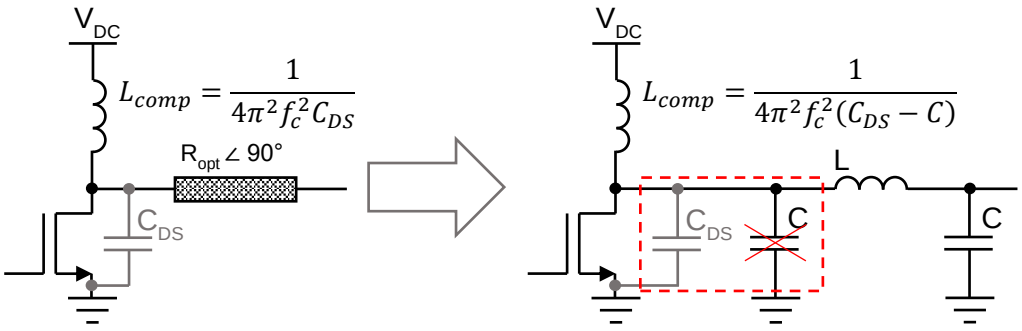


Figure 3.26. Parasitic capacitance absorption after replacing the transmission line with its lumped equivalent

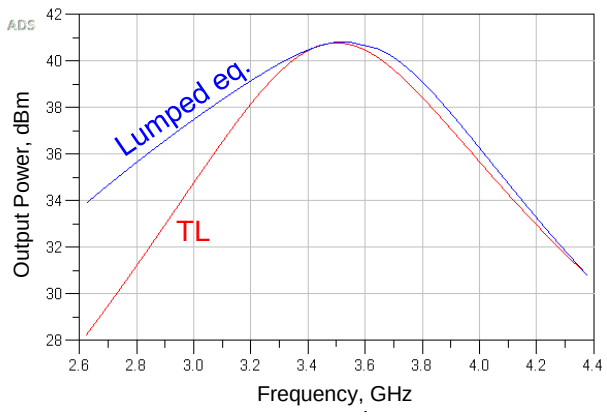


Figure 3.27. Power bandwidth at back-off when the impedance inverter is a transmission line (see the red curve) and when its lumped equivalent is used (see blue curve).

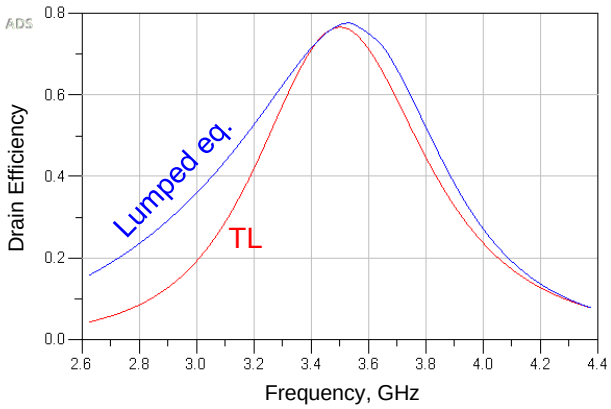


Figure 3.28. Efficiency bandwidth at back-off when the impedance inverter is a transmission line (see the red curve) and when it is the lumped equivalent (see blue curve).

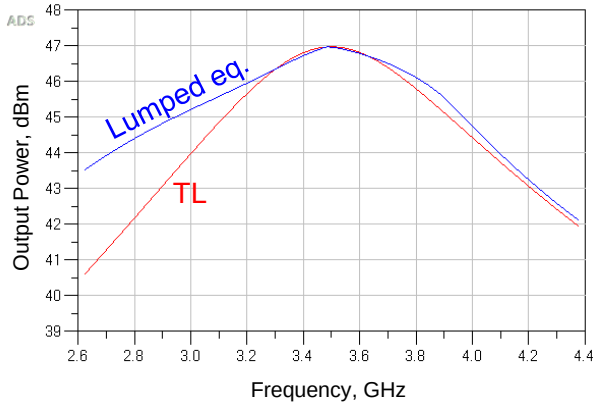


Figure 3.29. Power bandwidth at P_{max}, when the impedance inverter is a transmission line (see the red curve) and when its lumped equivalent is used (see blue curve).

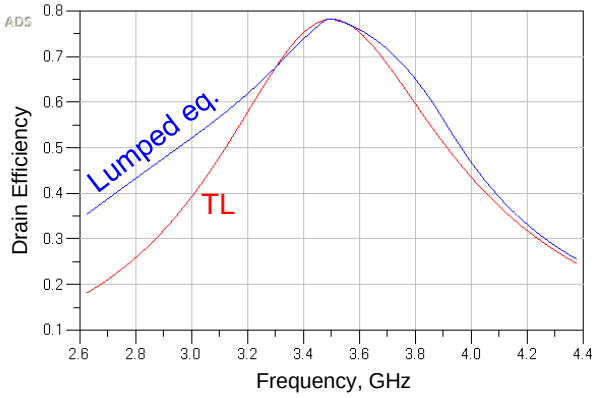


Figure 3.30. Efficiency bandwidth at P_{max}, when the impedance inverter is a transmission line (see the red curve) and when its lumped equivalent is used (see blue curve).

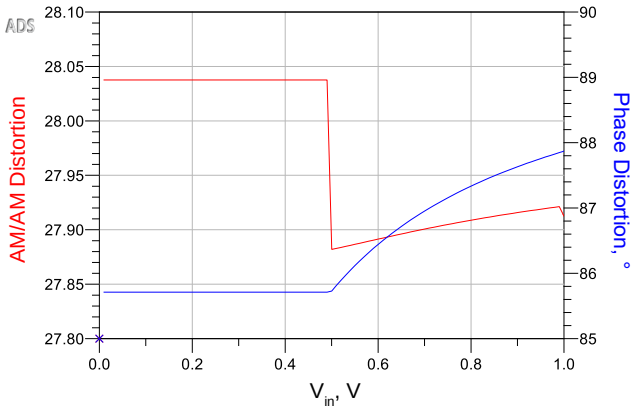


Figure 3.31. AM to AM (red) and phase (blue) distortion. The lumped equivalent of the impedance inverter has been used for this simulation. These results relate to the single-ended and push-pull PCL-DPA.

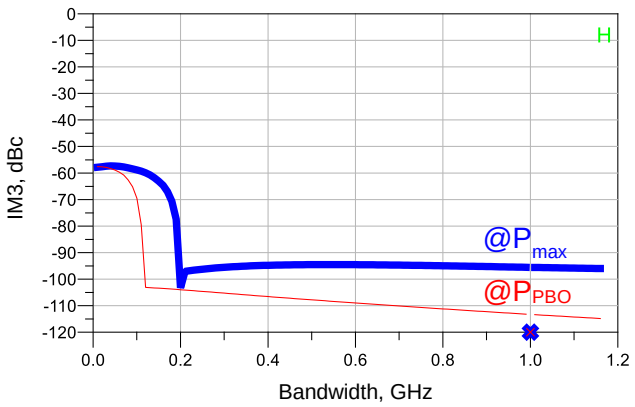


Figure 3.32. IM3 in dBc (decibels with respect to fundamental tones) versus bandwidth (tone spacing) in GHz. Red curve is at power back-off, and blue is at maximum power. The lumped equivalent impedance inverter has been used in this simulation. PCL-DPA.

The circuit, which is shown in Figure 3.11 has been modified as follows. The transmission line TL8 has been replaced by the 711 pH inductor then L_4 and L_5 values have been changed to 450 pH. After this change, the harmonic balance simulation was performed once more. The bandwidth plots of Figure 3.27 to Figure 3.30 show that the bandwidth at the back-off increased from 360 MHz to 440 MHz, and at the maximum power, from 530 MHz to 610 MHz. However, as Figure 3.32 shows, linearity became worse but remained very satisfying. This happened because the lumped equivalent has an asymmetrical frequency response with respect to the center frequency, while the transmission line has a purely symmetrical response.

3.5.1.2. Push-Pull

Only the single-ended (simplest) topology has been used for Class B amplifiers so far. The other topology which is widely used for Class B amplifiers is called *Push-Pull*. It has at least 2 transistors instead of one. In the most straightforward Class B configuration, the single transistor converts the input signal to current only during positive input signal swing. The additional transistor in push-pull topology converts the input signal also during the negative input signal swing. At that moment, the other transistor is off. As a result, the output signal waveform is even more similar to the input signal, thus push-pull topology can provide better linearity than a single-ended version. Furthermore, it can have a differential output.

The main and the peak amplifiers can be made Push-Pull. However, the linearity of the peak amplifier is a lot less important than of the main because the peak amplifier is active only when the input signal is above the back-off point and its non-linearities gave significant influence only when it works near or at the maximum power, while the main amplifier saturates at the back-off. Input signal level should be slightly below the back-off point most of the time if the system where Doherty PA is used works appropriately. Thus, we have replaced only the main amplifier with Push-Pull and left the peak amplifier as it was. See Figure 3.33 for the updated version of PCL-DPA circuit from Figure 3.10. Each transistor in the push-pull circuit has to be twice as small as in a single transistor case. This is because the input voltage is still 1 V to each transistor, but both transistors now control the output simultaneously. Thus, each one should have half the transconductance (g_m) and so also half the parasitic capacitances. It can be seen from equation (2.16) that when parasitic capacitance is twice smaller, the compensation inductor (L_{comp}) value has to be twofold higher, as it is shown in the updated circuit.

This (Figure 3.33) circuit has precisely the same bandwidth as the usual PCL-DPA. However, its IM3 is even significantly better at the power backoff point, e.g., compare Figure 3.34 with Figure 3.25. At the back-off, it is lower than -340 dBc, and at the maximum power, it is lower than -95 dBc. Now, let's replace the impedance inverting transmission line with its lumped equivalent, as done with PCL-DPA in the previous section. Values of the lumped equivalent are exactly the same as before. However, while choosing compensation inductor values, it is important to keep in mind that effective

capacitance after the transformer is different if the transformer ratio is different from 1. However, in this case, the transformer ratios are 1:1:1. Thus L_{comp1} value is the same as in the previous section. After performing the simulation, it has been noticed that the bandwidth and efficiency plots overlap with the plots of the conventional PCL-DPA with a lumped equivalent, see from Figure 3.27 to Figure 3.30 (blue and red curves). IM3 is slightly better than for the previous circuit with the lumped equivalent; compare Figure 3.35 with Figure 3.32. Amplitude and phase distortion plots with transmission line and the lumped equivalent overlap with the plots shown in Figure 3.24 and Figure 3.25.

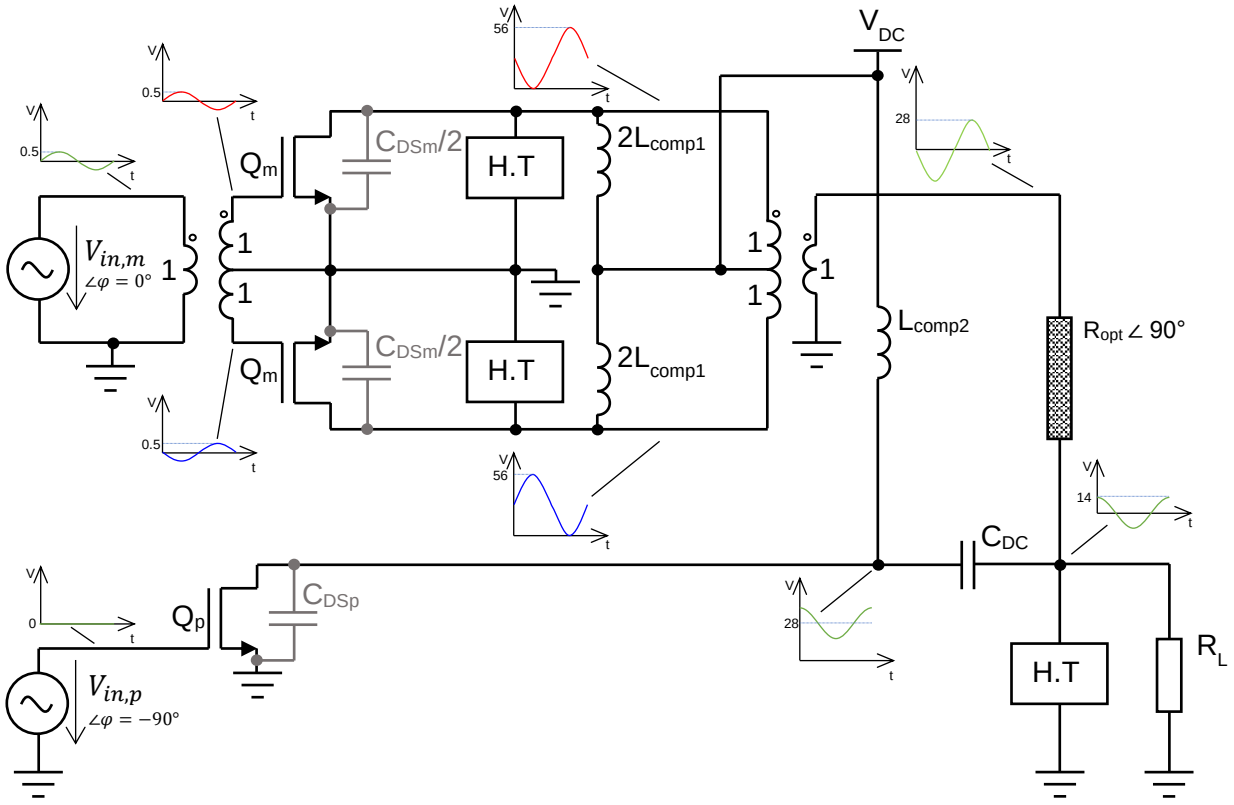


Figure 3.33. Push-pull variant of parallel-connected load Doherty PA (PCL-DPA). Circuit diagram. Signal is shown at the back-off. Green – the single-ended signal, red and blue – the differential signal.

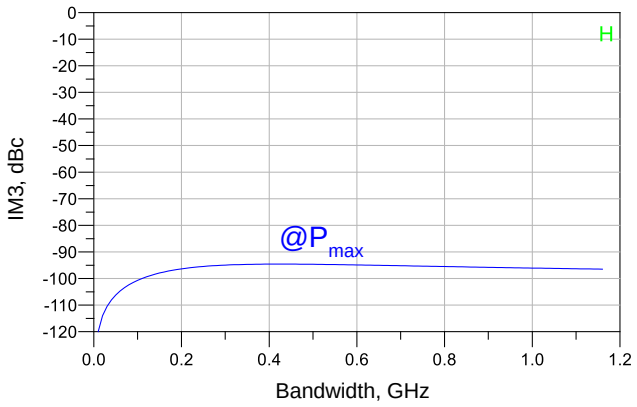


Figure 3.34. IM3 versus bandwidth (tone spacing) in GHz at maximum power. It is below -340 dBc at backoff, so outside the plot. The simulation results relate to the push-pull variant of PCL-DPA.

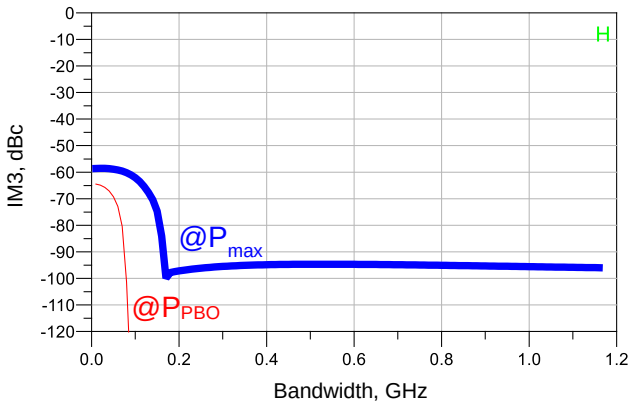


Figure 3.35. IM3 versus bandwidth (tone spacing) in GHz. Red curve is at back-off, and blue is at full power. The lumped equivalent circuit has been used as an impedance inverter. The simulation results relate to the push-pull variant of PCL-DPA.

It can be concluded that the push-pull version increases linearity but does not show any improvement for the bandwidth. However, even a non-push-pull version has pretty good linearity when ideal components are used. On the other hand, the Push-Pull version may have a significant advantage on linearity if realistic components are used, but this situation has not been tested.

3.5.2. With Series Connected Load

This subsection introduces some of the possible implementations of Doherty PA with series-connected load (SCL-DPA). The main and/or the peak amplifier can be made using a single transistor, like in Figure 3.36. If Class B operation is needed, each amplifier can also use a push-pull configuration like in PCL-DPA. Figure 3.46 shows the circuit when the main amplifier is push-pull, and the peak amplifier is a single transistor Class B line-up. Furthermore, SCL-DPA can be fully differential, see Figure 3.49.

3.5.2.1. Single Ended

The values calculated in section 3.5.1.1 can be reused. The only difference in values is that while in PCL-DPA R_L is kR_{opt}, in SCL-DPA it is R_{opt}/k. The circuit from Figure 3.36 has been entered into "Keysight ADS" schematics editor, and 31st order harmonic balance simulation has been performed. Obtained plots also show the correct Doherty PA operation. Since the plots are exactly the same as for PCL-DPA (see Figure 3.14, Figure 3.15, and figures from 3.17 to 3.23), they are omitted here. An exception is made for the output voltage, compare Figure 3.16 with Figure 3.45.

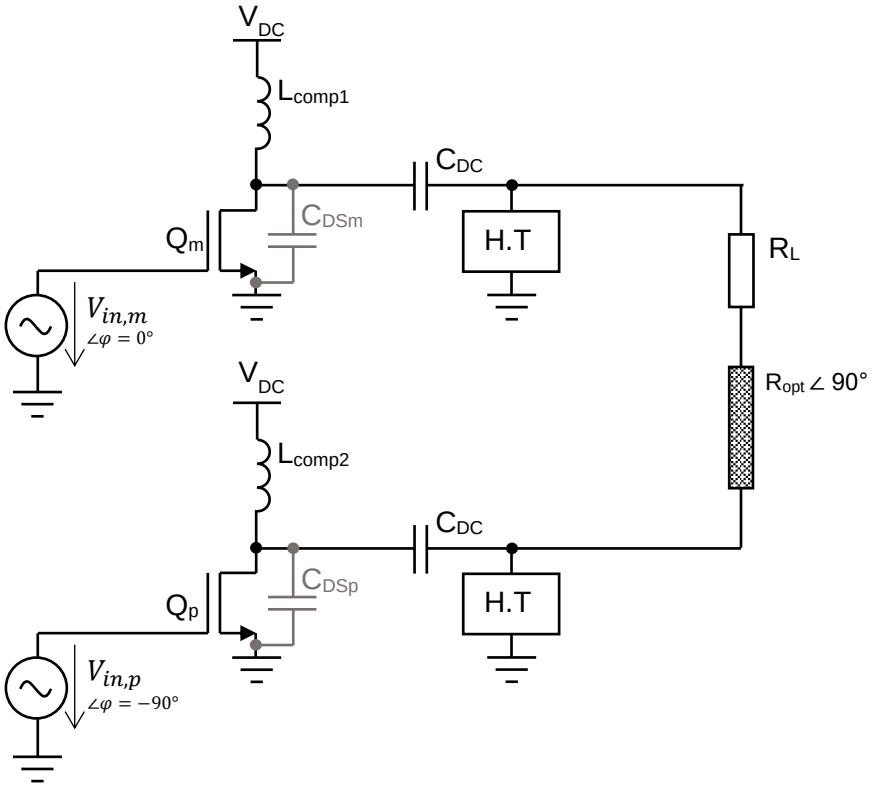


Figure 3.36. Single-ended series connected load Doherty PA (SCL-DPA) circuit diagram.

From the bandwidth plots (see red curves from Figure 3.39 to Figure 3.42), we can see that 1 dB power bandwidth is 560 MHz at the back-off and 1130 MHz at the maximum power when the transmission line is used as an impedance inverter. After replacing the transmission line with its lumped equivalent, bandwidth decreased. Furthermore, it became asymmetrical due to asymmetry in the frequency response of the equivalent network. Thus 1 dB power bandwidth at back-off became 510 MHz and at the maximum power only 630 MHz.

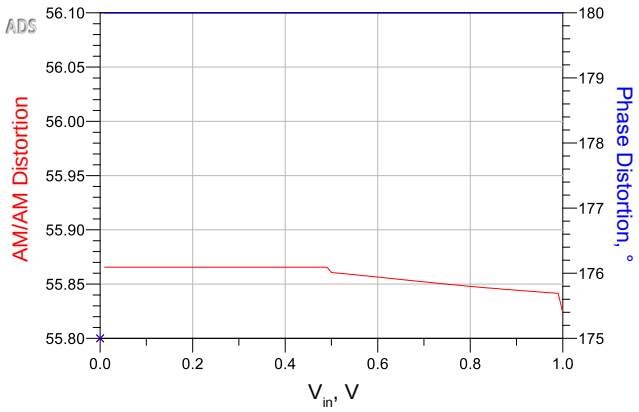


Figure 3.37. AM to AM (red) and phase (blue) distortion. The transmission line has been used as an impedance inverter. This simulation result relates to the most straightforward push-pull SCL-DPA case.

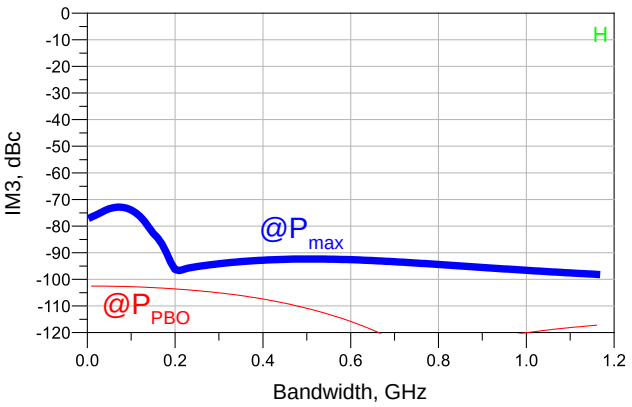


Figure 3.38. IM3 in dBc (decibels with respect to carrier) versus bandwidth (tone spacing). Red curve is at back-off, and blue is at maximum power. The transmission line has been used as an impedance inverter. SCL-DPA.

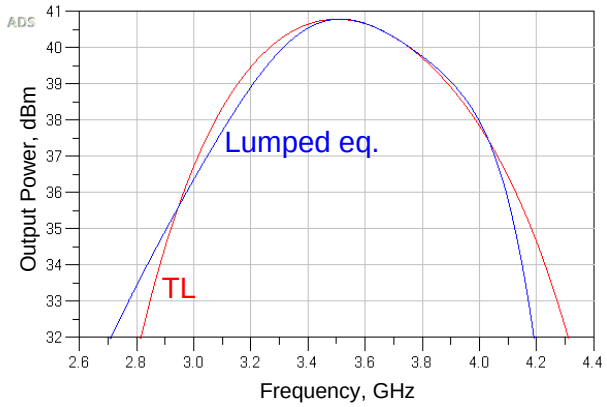


Figure 3.39. Power bandwidth at back-off when the impedance inverter is a transmission line (see the red curve) and when its lumped equivalent is used (see blue curve).

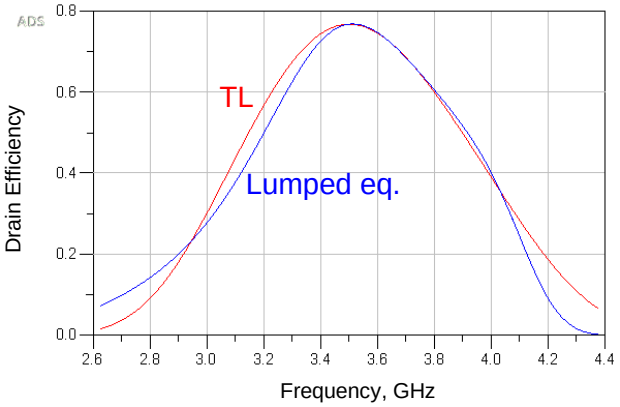


Figure 3.40. Efficiency bandwidth at back-off when the impedance inverter is a transmission line (see the red curve) and when its lumped equivalent is used (see blue curve).

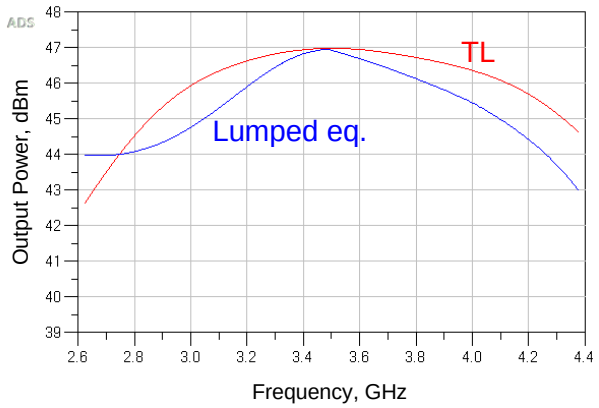


Figure 3.41. Power bandwidth at P_{max} when the impedance inverter is a transmission line (see the red curve) and when its lumped equivalent (see blue curve) is used. Results relate to the SCL-DPA.

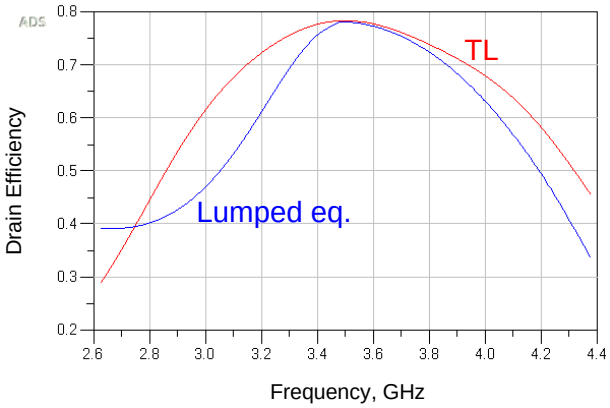


Figure 3.42. Efficiency bandwidth at P_{max} when the impedance inverter is a transmission line (see the red curve) and when its lumped equivalent (see blue curve) is used. Results relate to the SCL-DPA.

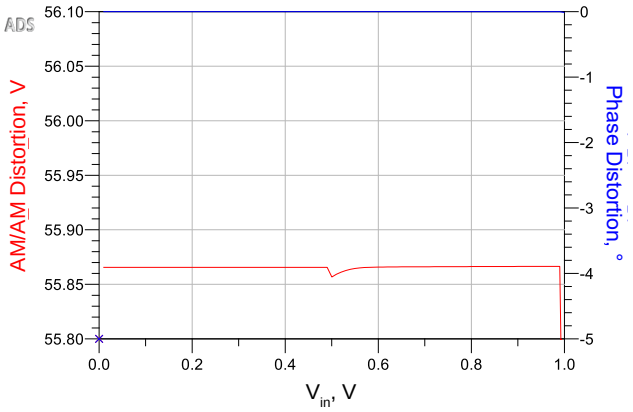


Figure 3.43. AM to AM (red) and AM-PM (blue) distortion results for both the lumped equivalent and transmission line-based impedance inverter case. These results apply to the simplest SCL-DPA topology.

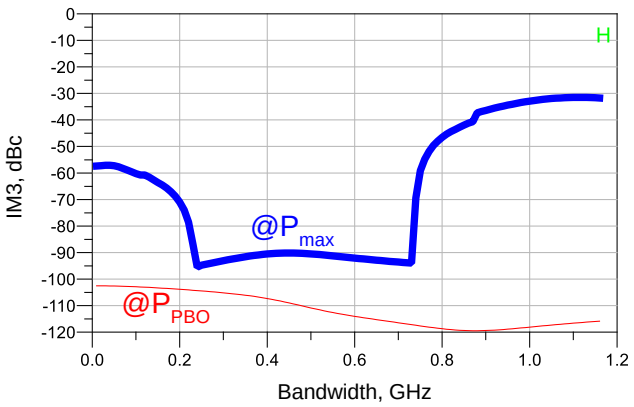


Figure 3.44. IM3 in dBc versus bandwidth (tone spacing). The red curve is at back-off, and blue is at maximum power. The lumped equivalent circuit has been used as an impedance inverter. SCL-DPA.

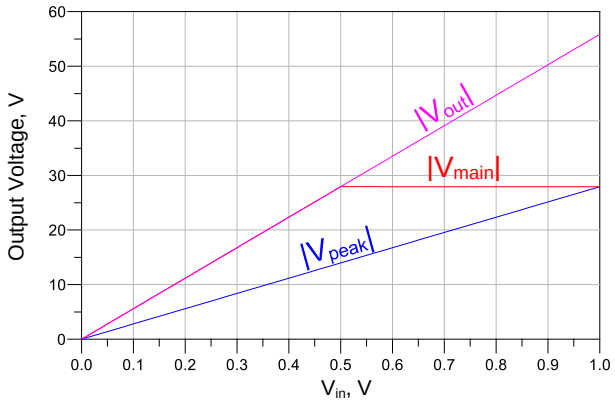


Figure 3.45. The output voltage of the main (red curve), of the peak (blue curve) amplifiers and voltage on the load (magenta curve) versus input voltage for SCL-DPA. 1-tone test

3.5.2.2. Push-Pull

The Push-Pull version of SCL-DPA is shown in Figure 3.46. One of its advantages is that the load references the ground differently than in the conventional SCL-DPA. After harmonic balance simulation, it turned out that bandwidth and efficiency plots overlap with the plots from the previous section (from Figure 3.39 to Figure 3.42). Amplitude and phase distortion plots of the push-pull versions overlap with the plots obtained for the previous case (Figure 3.43), except that there is no dip at V_{in} = 0.5 V in the AM/AM plot (see the red curve). The IM3 at the back-off is better than in the previous case, but at the maximum power, it is the same (compare Figure 3.38 with Figure 3.47). This also applies to the case with the lumped equivalent; compare Figure 3.44 with Figure 3.48.

A peak amplifier can also be made push-pull; however, that has not been attempted in this work. Doing so would give some important advantages. First, the required load impedance R_L would increase two times. Higher load impedance makes matching to actual load in a real circuit easier, yielding more straightforward matching with smaller errors resulting in higher bandwidth. Secondly, the baluns could provide a unique ability to separate the second-harmonic termination from the fundamental impedance [16]. This could also give some other minor advantages. For example, undesired load modulation at the second-harmonic frequencies can be avoided [16]. However, the disadvantage is that the load would be again connected between the main and the peak amplifiers, similarly to the conventional (single-ended) SCL-DPA.

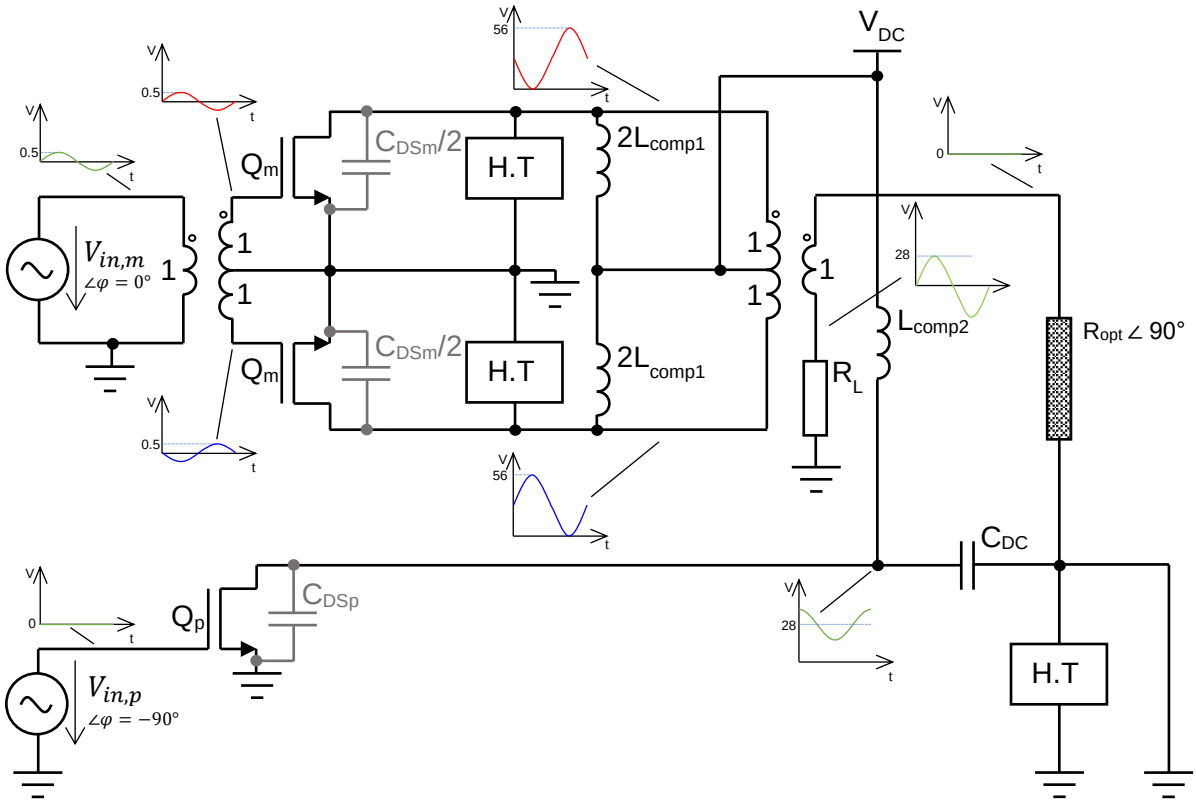


Figure 3.46. Push-pull variant of series-connected load Doherty PA (SCL-DPA). Circuit diagram.
The signal is shown at the back-off. Green – the single-ended signal, red and blue – the differential signal.

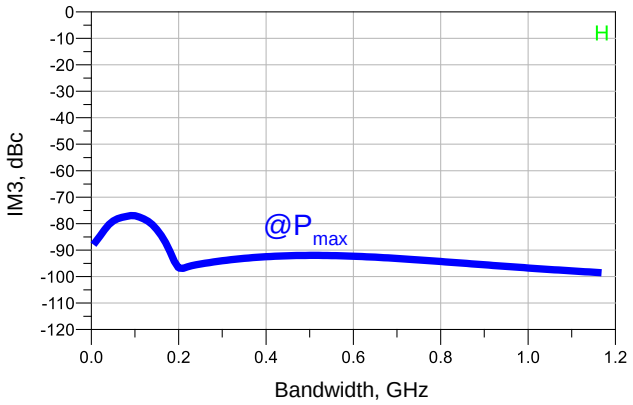


Figure 3.47. IM3 versus bandwidth (tone spacing) at maximum power. It is below -340 dBc at backoff, so outside the plot. The transmission line has been used as the impedance inverter.

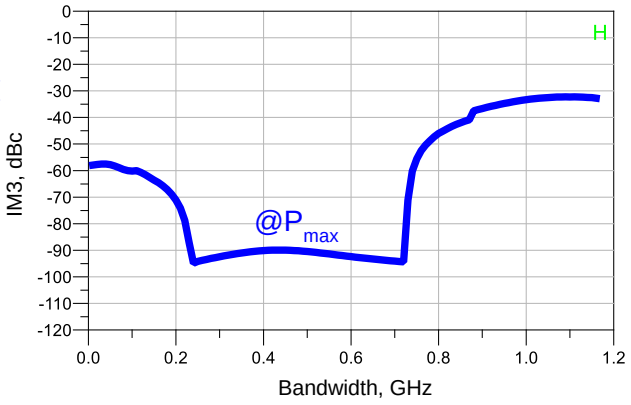


Figure 3.48. IM3 versus bandwidth (tone spacing) at maximum power. It is below -120 dBc at backoff, so outside the plot. The lumped equivalent has been used as an impedance inverter.

3.5.2.3. Differential

A fully differential version of SCL-DPA is also possible, and it is presented in Figure 3.49. In this case, both the main and the peak amplifier are in a push-pull configuration. Each transistor is twice smaller than in Figure 3.36. As a result, each transistor's transconductance (g_m) and parasitic capacitance are half, and the compensation inductors need to have twice as high inductance. Since the circuit is differential, two equal impedance inverters are required. Each of them needs to have twice higher characteristic impedance, and each half (top and bottom) needs to see a twice higher load than conventional single-ended SCL-DPA (Figure 3.5b). Thus, each half (top and bottom) of the circuit provides half of the total output power.

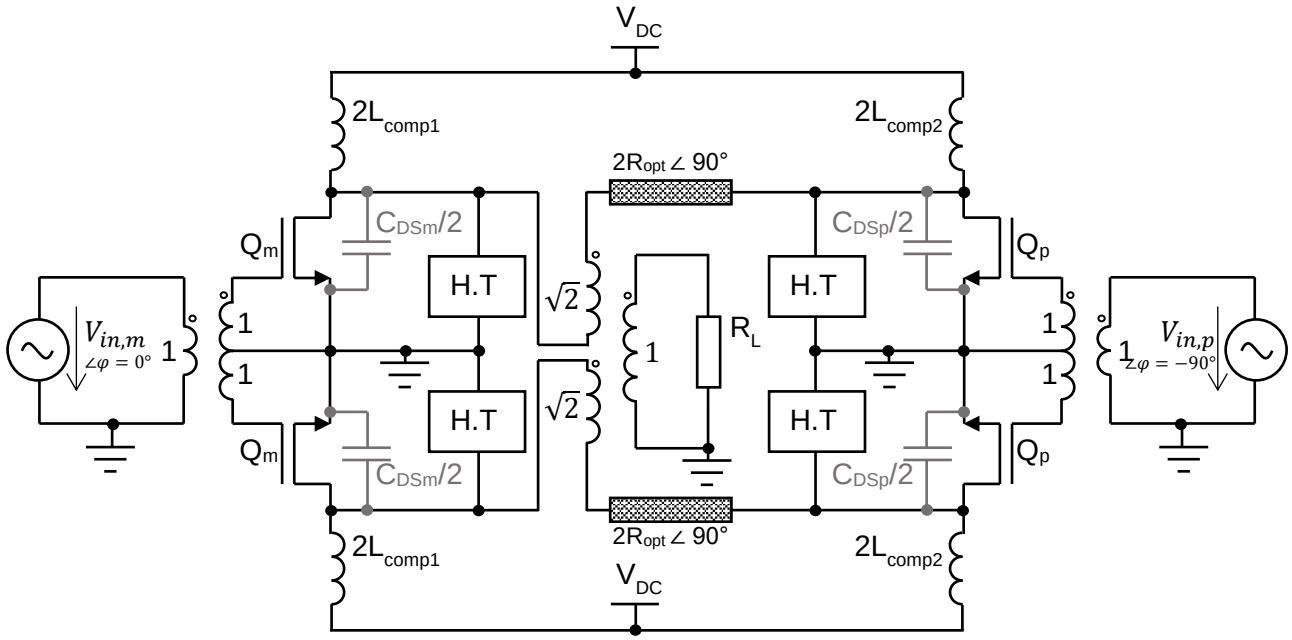


Figure 3.49. Differential version of series-connected load Doherty PA (SCL-DPA). Circuit diagram.

Unlike in all previous circuits, the load is connected via a transformer. Its turn ratios are $\sqrt{2}$: 1 between each primary and the secondary winding.

$$\frac{n_1}{n_2} = \frac{V_1}{V_2} = \sqrt{\frac{R_1}{R_2}} \tag{3.29}$$

Where R_1 and R_2 are impedances at the primary and secondary sides of a transformer, V_1 and V_2 are voltages on the corresponding windings, n_1 and n_2 are the number of turns on the primary and secondary sides. See **Error! Reference source not found.** for reference. Here R_1 should be 2 times higher than R_2. Thus from (3.29) that $n_1/n_2 = \sqrt{2}$. Let's choose $n_2 = 1$. Then $n_1 = \sqrt{2}$. This transformer can also be used for matching any load impedance value, for example, to 50 Ω.

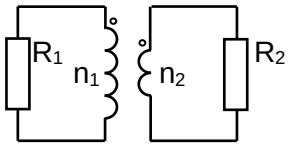


Figure 3.50. A transformer.

The transmission lines still can be replaced with lumped equivalents; however, in this case, only capacitances $C_{DSp}/2$ can be (partially) absorbed because the transformer is connected on the left-hand side of the impedance inverting transmission line, see Figure 3.49.

After harmonic balance simulation, it turned out that bandwidth and efficiency plots overlap with the plots from the single-ended SCL-DPA (see from Figure 3.39 to Figure 3.42). Amplitude and phase distortion plots of the differential versions are shown in Figure 3.53 (transmission line based) and Figure 3.54 (lumped-equivalent based), respectively, and look fine (shows no significant distortion). The differential SCL-DPA with lumped impedance inverter has a very similar IM3 but a lot worse bandwidth than with transmission line-based impedance inverter. IM3 plots for the differential SCL-DPA are represented in Figure 3.51 and in Figure 3.52. IM3 is very good (below 200 dBc) at the back-off, like in push-pull version. IM3 is the best at the maximum power (the best of all tested topologies). IM3 has abrupt change (increase) after 0.8 GHz because when bandwidth increases at some points, IM3 products overlap with signal harmonics.

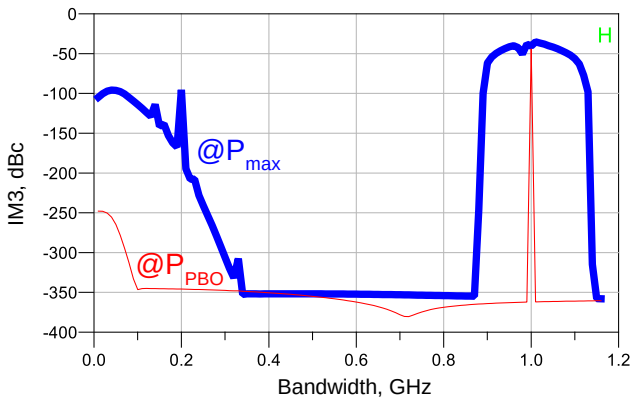


Figure 3.51. IM3 versus bandwidth (tone spacing) in GHz at maximum power. It is below -340 dBc at backoff, so outside the plot. A transmission line has been used as the impedance inverter. Differential SCL-DPA.

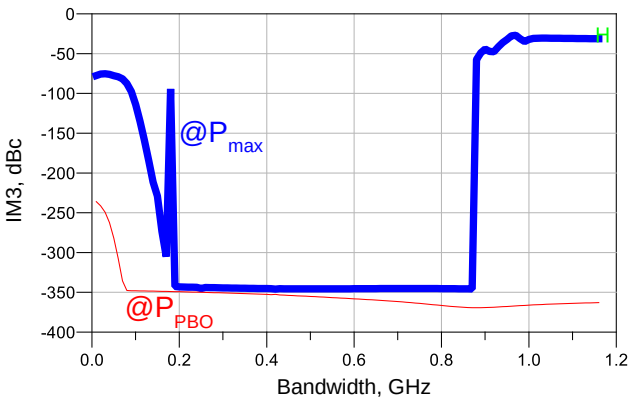


Figure 3.52. IM3 versus bandwidth (tone spacing) in GHz at maximum power. The red curve is at back-off, and blue is at full power. The lumped equivalent has been used as an impedance inverter.

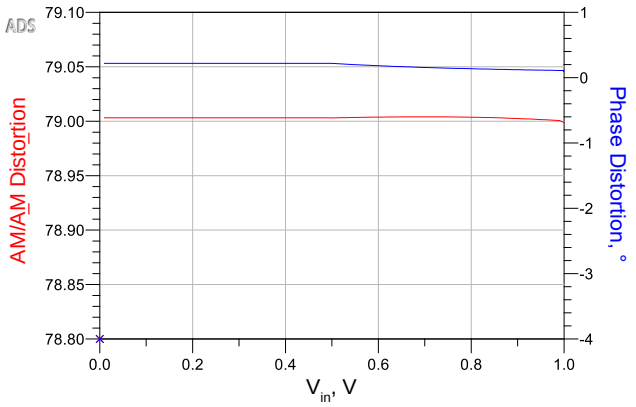


Figure 3.53. Amplitude (red) and phase (blue) distortion. A transmission line has been used as the impedance inverter. Differential SCL-DPA.

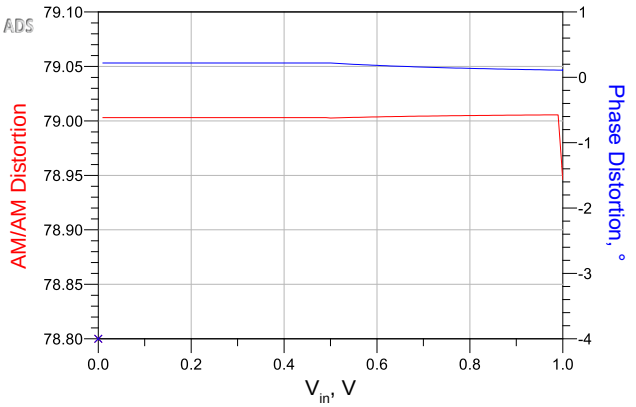


Figure 3.54. Amplitude (red) and phase (blue) distortion. The lumped equivalent has been used as an impedance inverter. Differential SCL-DPA.

3.5.3. Comparison of Simulation Results

The most important simulation results (bandwidth at the back-off and the maximum power) are summarized in Table 3.2. In the table, *TL* and *lumped* in brackets tell whether the impedance inverter is a transmission line (TL) or its lumped equivalent. η_{min} is minimum efficiency at the 1 dB bandwidth and η_{cent} is efficiency at the center frequency. Differential SCL-DPA topology with impedance inverting transmission lines has the best linearity (lowest distortion and the best IM3). The PCL-DPA cannot be made differential. In all cases making the main amplifier push-pull improved IM3. According to the results, all PCL-DPA topologies with the lumped transmission line equivalent and all SCL-DPA topologies with transmission line-based impedance inverters are worth attention. However, these SCL-DPA topologies have better bandwidth than the best PCL-DPA. This may be explained due to the different kind of resonance in PCL-DPA (see next paragraph for more details).

Finally, simulation of a single-ended PCL-DPA (Figure 3.10) and a single-ended SCL-DPA (Figure 3.36) without any parasitic capacitances has been performed, and output power versus frequency was plotted. The plots were used to measure the 1 dB bandwidth. Results are presented in the last two rows of Table 3.2. These are the fundamental bandwidth limitations of these topologies because in the end the impedance inverter always limits bandwidth. PCL and SCL DPA topologies without parasitics have almost equal bandwidths, while at the backoff, SCL-DPA has a lot higher bandwidth than PCL-DPA. This difference in bandwidth exists due to the different resonances that occur in the impedance inverter when peak amplifiers are off. A series resonance occurs in the Doherty amplifier with a series-connected load, while in the PCL-DPA a parallel resonance arises. In a symmetrical

case, this parallel resonance has a higher quality factor than series resonance. This is why at back-off PCL-DPA has a lot smaller power bandwidth while both topologies are very similar at full power.

Table 3.2. Summarized simulation results.

	BW@P_{OBO}, MHz	η_{min}	η_{cent}	BW@P_{max}, MHz	η_{min}	η_{cent}
PCL (TL)	360	0.61	0.768	530	0.62	0.783
Push-Pull PCL (TL)						
PCL (lumped)	**440**			**610**		
Push-Pull PCL (lumped)						
SCL (TL)	**560**			**1130**		
Push-Pull SCL (TL)						
Differential SCL (TL)						
SCL (lumped)	510			630		
Push-Pull SCL (lumped)						
Differential SCL (lumped)	500			690		
PCL (without parasitics)	1330	0.62	0.78	1750	0.62	0.783
SCL (without parasitics)	≫1750	≪0.77	0.78	1710		

3.6. Improvements

A lot of research has been done over the years after the invention of the original Doherty power amplifier topologies with series and parallel connected load (PCL and SCL-DPA), and it is still going on. Many variations of the architecture were proposed. This section reviews two recent articles ([16] and [24]). Then applies proposed design equations to the example specifications which were introduced in the previous section.

3.6.1. Improved Output Combiner Topology for Series Connected Load Doherty PA

A. Jundi *et al.* in their article [16], review earlier research and conclude that SCL-DPA topology is more promising for bandwidth improvement because it needs higher optimum load impedance than PCL-DPA. However, classical SCL-DPA is unsuitable for high-frequency operation because transistor parasitics cause a significant phase shift at the package plane. Thus, the assumption that the current source of the main amplifier is connected directly to the load at high frequencies is invalid [16]. This has to be addressed during the design. A. Jundi *et al.* derived a generalized formulation of the output combiner where the load is not connected directly and could be used for arbitrary load impedance selection while retaining good bandwidth. The combiner is shown in Figure 3.55a. It is known that a general formulation for the main and auxiliary networks can be obtained as a function of the load impedance R_L.

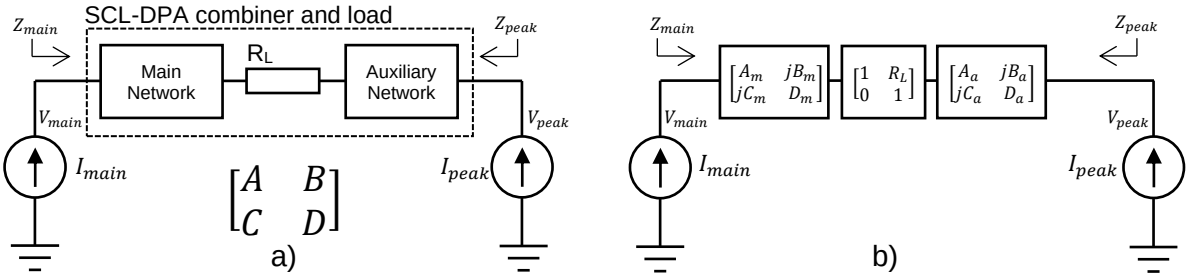


Figure 3.55. Generic representation of the SCL-DPA output combiner as a single two-port network.

The combiner is a 2-port network, so ABCD parameters can easily describe it. Then the relationship between the voltages and currents can be expressed as [16]

$$\begin{bmatrix} V_{main} \\ I_{main} \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_{peak} \\ -I_{peak} \end{bmatrix}. \tag{3.30}$$

After evaluation of (3.30) these relations can be obtained:

$$V_{main}^{B} = AV_{peak}^{B} - BI_{peak}^{B} \tag{3.31}$$

$$I_{main}^{B} = CV_{peak}^{B} - DI_{peak}^{B} \tag{3.32}$$

$$V_{main}^{S} = AV_{peak}^{S} - BI_{peak}^{S} \tag{3.33}$$

$$I_{main}^{S} = CV_{peak}^{S} - DI_{peak}^{S} \tag{3.34}$$

Where superscripts B and S represent back-off and saturation conditions, respectively. The current, voltage and load modulation profiles must be defined before solving equations (3.31) – (3.34). An infinite number of these profiles exist. They are defined by biasing conditions, transistor size (i.e., maximum current), back-off level, phase relationship between the main and peak transistors, etc. Here, as well as in the article [16], the drain voltages are assumed to be the same (symmetrical[9]) and the load modulation for both the main and peak transistors is from real to real for all power levels.

Consequently, the profiles are set for every choice of back-off level (k). They have been introduced already, see Figure 3.6. From these profiles the following relationships can be derived (assuming the load impedance R_L is real) [16]:

$$\frac{V_{main}^{B}}{I_{main}^{B}} = \frac{R_{opt}}{k} \tag{3.35}$$

$$\frac{V_{main}^{S}}{I_{main}^{S}} = R_{opt} \tag{3.36}$$

$$I_{peak}^{B} = 0 \tag{3.37}$$

$$\frac{I_{main}^{S}}{I_{peak}^{S}} = \frac{k}{1-k} \cdot e^{-j\theta} \tag{3.38}$$

$$\frac{V_{main}^{B}}{V_{peak}^{B}} = \frac{1}{k} \cdot e^{-j\theta} \tag{3.39}$$

where R_{opt} is the optimum load impedance of the main transistor at peak power, θ is the phase of the peak amplifier current I_{peak} relative to the main amplifier current I_{main}. Using these boundary conditions, the generalized ABCD matrix is [16, 25]

$$ABCD = \begin{bmatrix} \frac{e^{-j\theta}}{k} & \frac{R_{opt}}{e^{j\theta}} \\ \frac{e^{-j\theta}}{R_{opt}} & 0 \end{bmatrix}. \tag{3.40}$$

It is known that θ can only take a discrete set of values for the network to be realizable using passive elements [16]. Value $\theta = 90°$ will be used. Analysis of the combiner can be done for any other set of profiles. Then boundary conditions will change, and that will lead to a different set of solutions. The ABCD matrix is valid for any back-off level (k). The combiner can be divided into three parts, see Figure 3.55a. Each of them can be expressed as ABCD matrixes, as shown in Figure 3.55b. The main and auxiliary networks are assumed to be reciprocal and lossless. Therefore, diagonal elements of all three matrixes are real, while off-diagonal values are purely imaginary. By multiplying all three ABCD matrixes symbolically, the ABCD matrix of the whole combiner can be obtained. This allows to create an equation and find values of each matrix from Figure 3.55b. The matrixes of the main and the auxiliary networks are given by (3.41) and (3.42), respectively [16].

[9] Do not confuse with symmetrical amplifiers (amplifiers for which $k = 0.5$).

$$\begin{bmatrix} A_m & jB_m \\ jC_m & D_m \end{bmatrix} = \begin{bmatrix} -\sqrt{\frac{R_{opt}}{kR_L}} & jB_m \\ 0 & -\sqrt{\frac{kR_L}{R_{opt}}} \end{bmatrix} \tag{3.41}$$

$$\begin{bmatrix} A_a & jB_a \\ jC_a & D_a \end{bmatrix} = \begin{bmatrix} -\frac{B_m}{R_{opt}} & j\sqrt{kR_LR_{opt}} \\ \frac{j}{\sqrt{kR_LR_{opt}}} & 0 \end{bmatrix} \tag{3.42}$$

There B_m and R_L are free values, so that when B_m is set, a unique set of networks can be obtained for an arbitrary value of R_L. The resulting ABCD matrices can be synthesized to an infinite set of networks but only at the center frequency. They may not be equivalent at other frequencies. During derivation of the main and auxiliary network ABCD matrices, two important assumptions were made [16]:

- Impedance modulation for both main and peak amplifiers is real to real. This assumption was made to set boundary conditions. It may not be valid for the entire operating bandwidth, but at least they are valid at the center frequency. The frequency response of the output combiner can be analyzed after selecting its specific topology.
- The topology of the output combiner is unknown in general. The only known fact is that the load is between the main and auxiliary networks, as shown in Figure 3.55a. This assumption was made to get a general solution that does not require a predefined topology.

Ideal combiner topology is not yet known. However, the resulting solution gives a possibility for the designer to explore multiple topologies.

Comparison of possible networks when B_m is set to 0 and higher than 0 are shown in Figure 3.56. For simplicity, let's set B_m to 0. Then ABCD matrices of the main (3.41) and the auxiliary (3.42) networks turn to (3.45) and (3.46), respectively. Locations of these networks as matrices are shown in Figure 3.56a.

$$\begin{bmatrix} A_m & 0 \\ 0 & D_m \end{bmatrix} = \begin{bmatrix} -\sqrt{\frac{R_{opt}}{kR_L}} & 0 \\ 0 & -\sqrt{\frac{kR_L}{R_{opt}}} \end{bmatrix} \tag{3.43}$$

$$\begin{bmatrix} 0 & jB_a \\ jC_a & 0 \end{bmatrix} = \begin{bmatrix} 0 & j\sqrt{kR_LR_{opt}} \\ \frac{j}{\sqrt{kR_LR_{opt}}} & 0 \end{bmatrix}. \tag{3.44}$$

Non-zero values of B_m may be useful when taking into consideration the influence of reactive elements used for transistor parasitics absorption. It is important to note that these reactive elements may result in the asymmetric frequency response of the combiner. That would lead to narrowed bandwidth [16].

It is known that ABCD parameter matrix of a lossless transmission line is

$$ABCD = \begin{bmatrix} \cos(\beta l) & jZ_0 \sin(\beta l) \\ jY_0 \sin(\beta l) & \cos(\beta l) \end{bmatrix}. \tag{3.45}$$

For a quarter wavelength ($\beta l = 90°$) transmission line (3.45) evaluates to

$$ABCD = \begin{bmatrix} 0 & jZ_0 \\ jY_0 & 0 \end{bmatrix}. \tag{3.46}$$

Where Z_0 and Y_0 are characteristic impedance and characteristic admittance ($Y_0 = 1/Z_0$) of the transmission line, respectively.

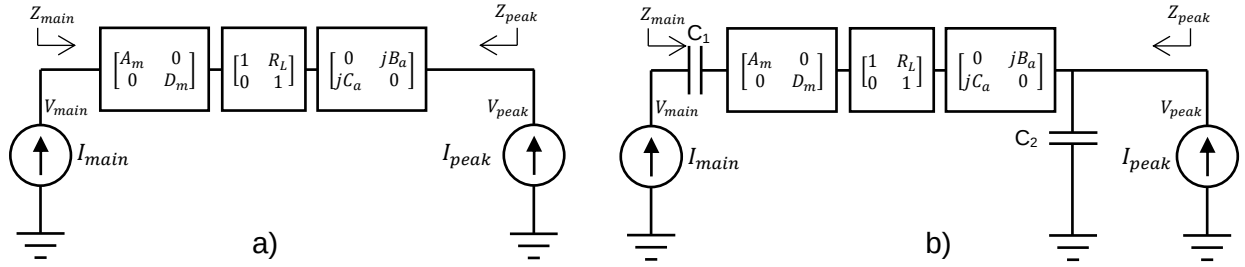


Figure 3.56. Output combiner network for (a) case of $B_m = 0$ and (b) case of $B_m > 0$.

After comparing the auxiliary network matrix, which is shown in (3.44) with (3.46) it can be concluded that the network can be synthesized to a quarter wavelength transmission line that has a characteristic impedance

$$Z_a = \sqrt{kR_{opt}R_L}. \tag{3.47}$$

Now let's connect two quarter wavelength transmission lines with different characteristic impedances Z_{m1} and Z_{m2} in series. Then their ABCD matrices (3.50) have to be multiplied to obtain the total ABCD matrix:

$$\begin{bmatrix} 0 & jZ_{m1} \\ j/Z_{m1} & 0 \end{bmatrix}\begin{bmatrix} 0 & jZ_{m2} \\ j/Z_{m2} & 0 \end{bmatrix} = \begin{bmatrix} -Z_{m1}/Z_{m2} & 0 \\ 0 & -Z_{m2}/Z_{m1} \end{bmatrix}. \tag{3.48}$$

After comparison of the result of (3.48) with (3.43), it can be seen that the main network can be synthesized to these two transmission lines, which have the following characteristic impedances:

$$Z_{m1} = \frac{R_{opt}}{k} \tag{3.49}$$

$$Z_{m2} = \sqrt{\frac{R_{opt}R_L}{k}} \tag{3.50}$$

The resulting topology is shown in Figure 3.58. Note that here the main amplifier receives the delayed input signal while the peak amplifier receives the undelayed input signal [16]. This is opposite to conventional DPA.Doherty. DPA topologies that work this way are called *inverted Doherty PA (IDPA)* [26, 27]. This inversion is needed due to additional transmission lines and has advantages which will be introduced in the next section.

Note that ABCD parameters can also be used to analyze a combiner used in the conventional SCL-DPA (see Figure 3.5b). There the main network is just a wire. It is known that ABCD matrix of a wire is

$$\begin{bmatrix} A_m & 0 \\ 0 & D_m \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \tag{3.51}$$

and for the auxiliary network it is

$$\begin{bmatrix} 0 & jB_a \\ jC_a & 0 \end{bmatrix} = \begin{bmatrix} 0 & jR_{opt} \\ j/R_{opt} & 0 \end{bmatrix}. \tag{3.52}$$

In conclusion, this theory could be constructive during future research to find more suitable combiner topologies for SCL-(I)DPA. Generic combiner topology using ABCD matrices can also be derived for PCL-(I)DPA.

Now, let's apply (3.47), (3.49), and (3.50) to find values for the example specifications, which were given in 3.5. For the topology which is given in Figure 3.58:

$$Z_a = \sqrt{kR_{opt}R_L} = \sqrt{0.5 \cdot 15.6 \cdot 31.2} = \mathbf{15.6\ \Omega};$$

$$Z_{m1} = \frac{R_{opt}}{k} = \frac{15.6}{0.5} = \mathbf{31.3\ \Omega};$$

$$Z_{m2} = \sqrt{\frac{R_{opt}R_L}{k}} = \sqrt{\frac{15.6 \cdot 31.2}{0.5}} = \mathbf{31.3\ \Omega}.$$

Then for the topology which is given in Figure 3.57:

$$Z_{mp} = Z_a = \mathbf{15.6\ \Omega};$$

$$Z_{a1p} = Z_{m1} = \mathbf{31.3\ \Omega};$$

$$Z_{a2p} = Z_{m2} = \mathbf{31.3\ \Omega}.$$

Simulations with these values have been performed, and results confirmed correct DPA operation. However, after comparing the power and efficiency bandwidth with results of other circuits, it turned out that the circuits which used equations (3.47), (3.49), and (3.50) were outperformed by other investigated Doherty PA circuits, including conventional SCL-DPA and variants of PCL-IDPA topology which has been proposed by Qureshi *et al*. [24]. On the other hand, only harmonic balance simulations were performed with ideal components that do not have current leakage at the center frequency and other parasitics. Moreover, matching errors were not considered (the matching network was not used at all during the simulations), while the article [16] states that the reason why SCL-(I)DPA can have a higher bandwidth is that it is easier to implement a matching network for it. Matching networks which can be implemented easier usually introduce smaller matching errors. It is easier to make matching networks for SCL topologies because they require higher load impedance than PCL topologies. For example, symmetrical (i.e., with 6 dB power back-off) SCL-DPA requires 4x higher impedance than PCL-DPA. When the required power back-off is even higher than that, SCL-DPA requires more than 4x higher impedance than PCL-DPA. If both the main and the peak amplifiers are made push-pull, then the required load impedance is even higher, e.g., for a symmetrical amplifier, it is 8x higher than for conventional PCL-DPA [16]. Thus, it is very likely that SCL-(I)DPA topologies will outperform a lot more PCL-(I)DPA topologies in electromagnetic simulations or in real life.

3.6.2. Inverted Doherty Power Amplifier Topologies

As it was mentioned in 3.2, conventional DPA topologies do not allow for a change in load impedance R_L without a change in voltage or current profile. This limitation was eliminated later by inserting two additional quarter wavelength transmission lines [16]. That gave researchers an additional degree of freedom which allows defining a much wider spectrum of solutions. That allowed to significantly improve the operational bandwidth of PCL-DPA and introduced the possibility to arbitrary control some other parameters, such as the load impedance R_L [16], and to prevent leakage to the peak amplifier when it is not active [26, 27]. This, can also be applied to SCL-DPA. The resulting topologies are shown in Figure 3.57 and Figure 3.58. Here, the main amplifier receives the delayed input signal while the peak amplifier receives the undelayed input signal [16, 26, 27]. Since this is opposite to conventional DPA, such topologies are called *inverted Doherty PA (IDPA)*. This inputs exchange (inversion) is required because additional transmission lines introduce phase shift, which must be compensated. Additional transmission lines also give a chance to absorb the parasitic transistor capacitance by replacing it with its lumped equivalent.

When the input voltage is below back-off, the peak amplifier is inactive (see Figure 3.57). Z_{a2p} can be used as an impedance inverter. Then the additional quarter wavelength transmission line (Z_{a1p})

minimizes the power leakage from the main amplifier. Lower leakage results in better linearity, efficiency, and power bandwidth [24, 26, 27]. When the load is connected in series with the amplifiers, Z_{m2} should work as an impedance inverter while Z_a minimizes the leakage (see Figure 3.58).

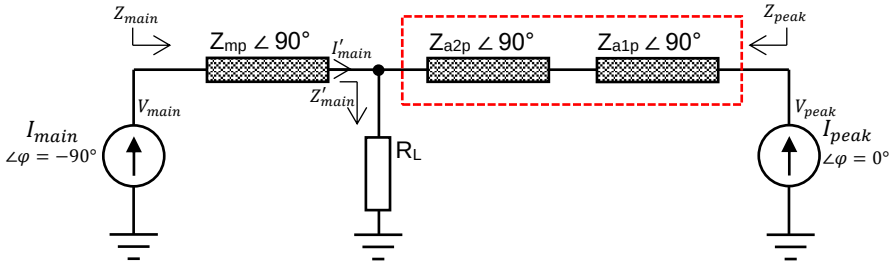


Figure 3.57. Inverted Parallel Connected Load Doherty PA (PCL-IDPA)

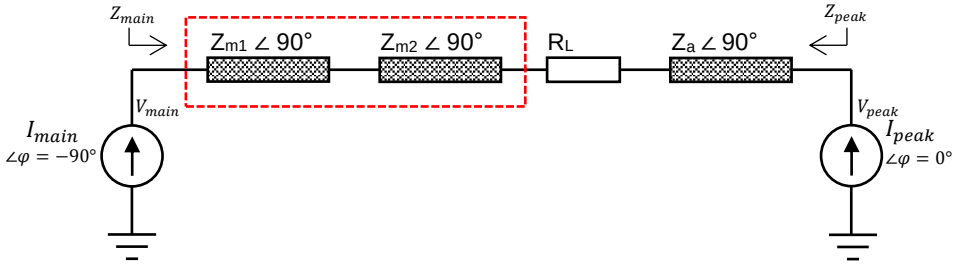


Figure 3.58. Inverted Series Connected Load Doherty PA (SCL-IDPA)

It was also proposed in [16] to replace the 90° transmission line Z_a with 270° one which would have the same characteristic impedance Z_a, see Figure 3.59. This is suboptimal, but it is a simple solution that would satisfy the auxiliary network's ABCD matrix when solved for $\theta = 90°$. Moreover, that allows for significantly wider degree of freedom in the auxiliary network to allow for better parasitic absorption over a wider band. This has not been tested during this project.

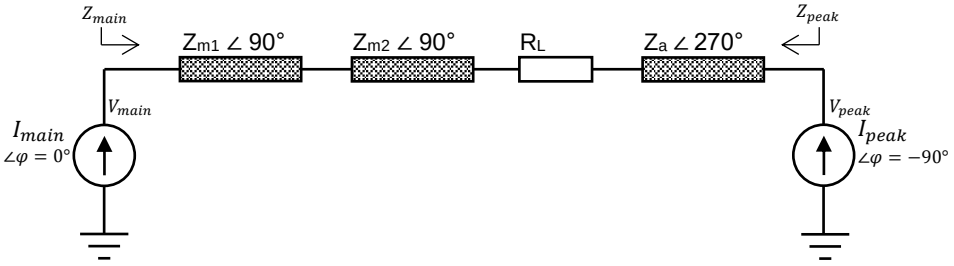


Figure 3.59. Not inverted Series Connected Load Doherty PA (SCL-DPA) with arbitrary real load impedance RL and extended auxiliary network.

Different design equations for PCL-IDPA were suggested by Raheem Quershi *et al.* [24]. They proposed a low-cost design approach for high-power PCL-IDPA, which can be implemented on a single-layer PCB. Their suggested circuit with design equations for a symmetrical PCL-IDPA is shown in Figure 3.60. C_{dM} and C_{dP} are transistor parasitics. L_M and L_P are used for their compensation. Impedances seen by the main and the peak amplifiers at full power are Z_{MF} and Z_{PF} and at back-off Z_{MB} and $Z_{PB,}$ respectively. The characteristic impedance of transmission lines for the main and the peak amplifiers are Z_M and $Z_{P,}$ respectively. Because of IDPA configuration, the quarter wavelength transmission line is placed in the path of the peak amplifier with characteristics impedance of Z_A. They introduced parameters σ_m and σ_p which can be used to optimize combining node impedance Z_{LE} and the characteristic impedance of transmission lines in case to get the best power and efficiency bandwidth [24].

It is known that for a general DPA:

$$\frac{Z_{main}}{Z_{peak}} = \frac{1-k}{k}. \tag{3.53}$$

By applying (3.53) to equations from Figure 3.60 they found out that a single parameter σ can be used instead σ_m and σ_p, then $\sigma_p = \frac{k}{1-k} \cdot \sigma$ and $\sigma_m = \sigma$. According their simulation results and conclusion $\sigma = 1/\sqrt{k}$ seem to be a good compromise for the output power and the efficiency behavior at back-off and at maximum power. They used the same supply voltage for the main and for the peak amplifier [24]. The same thing has been done during this project, so $\rho = 1$. Thus, equations which are shown in Figure 3.60 can be simplified to:

$$Z_M = \frac{R_{opt}}{\sqrt{k}} \tag{3.54}$$

$$Z_P = \frac{\sqrt{k}}{1-k} \cdot R_{opt} \tag{3.55}$$

$$Z_A = \frac{R_{opt}}{1-k} \tag{3.56}$$

$$Z_{LE} = R_{opt} \tag{3.57}$$

$$Z_{TE} = \sqrt{R_L R_{opt}} \tag{3.58}$$

Now let's apply (3.54) – (3.58) to find values, for example, specifications which were given in 3.5:

$$Z_M = R_{opt}/\sqrt{k} = 15.6/\sqrt{0.5} = \mathbf{22.1\ \Omega};$$

$$Z_P = \frac{\sqrt{k}}{1-k} \cdot R_{opt} = \frac{\sqrt{0.5}}{1-0.5} \cdot 15.6 = \mathbf{22.1\ \Omega};$$

$$Z_A = \frac{15.6}{1-0.5} = \mathbf{31.3\ \Omega};$$

$$Z_{LE} = R_{opt} = \mathbf{15.6\ \Omega};$$

$$Z_{TE} = \sqrt{R_L R_{opt}} = \sqrt{7.84 \cdot 15.6} = \mathbf{11.1\ \Omega}.$$

Note that Z_{TE} is used only for matching. It has been skipped in simulations. Since it should be used to match R_{opt} to R_L, instead of using that ZTE transmission line load which impedance is equal to R_{opt} has been used. Harmonic balance simulation of this PCL-IDPA topology has been compared with conventional PCL-DPA. At back-off, PCL-DPA has 360 MHz power bandwidth while PCL-IDPA has 530 MHz. Thus, 170 MHz higher. However, PCL-IDPA has similar power bandwidth to conventional SCL-DPA (but a bit worse). After an attempt to apply PCL-IDPA equations to SCL-DPA, its power and efficiency bandwidth becomes similar to PCL-DPA. Thus, although PCL-DPA equations can be used to find values for SCL-DPA, this does not work for inverted topologies. Further research is needed to improve existing equations for SCL-IDPA and find out why PCL-IDPA equations cannot be used for SCL-IDPA. Equations for PCL-IDPA are derived to decrease that leakage. For full comparison, refer to Table 3.3, compare row № 1 with the "PCL" row. On the other hand, as mentioned in the previous section, SCL-IDPA can still be useful because it gives designers and researchers additional freedom to define a much wider spectrum of solutions [16].

Like in conventional Doherty PA topologies, lumped equivalents of the transmission lines can be used to absorb part of the transistor parasitic capacitances. Single section lumped equivalent has been chosen because it can absorb more capacitance. Values for such low pass π lumped equivalent (Figure 3.9a) of the transmission line can be calculated using (3.24) and (3.25). Let's find capacitor and inductor values for the equivalent of the λ/4 transmission line, which has with characteristic impedance Z_M:

$$L_{SM} = \frac{Z_M}{2\pi f_0} = \frac{22.1}{2\pi \cdot 3.5 \cdot 10^9} = \mathbf{1.01\ nH};$$

$$C_{PM} = \frac{1}{2\pi \cdot 3.5 \cdot 10^9 \cdot 22.1} = \mathbf{2.04\ pF}.$$

Then the equation shown on the right side of Figure 3.26 can be applied to find inductance of the parasitic capacitance compensation inductor:

$$L_M = \frac{1}{4\pi^2 f_c^2 (C_{DS} - C)} = \frac{1}{4\pi^2 \cdot (3.5 \cdot 10^9)^2 \cdot (7.5 - 2.04) \cdot 10^{-12}} = \mathbf{379\ pH}.$$

The same equations can be applied to replace the transmission line Z_P with its lumped equivalent. This has been tried. However, PCL-IDPA with both Z_M and Z_P transmission lines replaced with lumped equivalents had worse linearity, not smooth, asymmetrical frequency response. Its power and efficiency bandwidth has been outperformed by many other variations (including PCL-IDPA with only lumped main) at back-off and maximum power, but it has the best bandwidth when operating just before compression (see row №5 of Table 3.3).

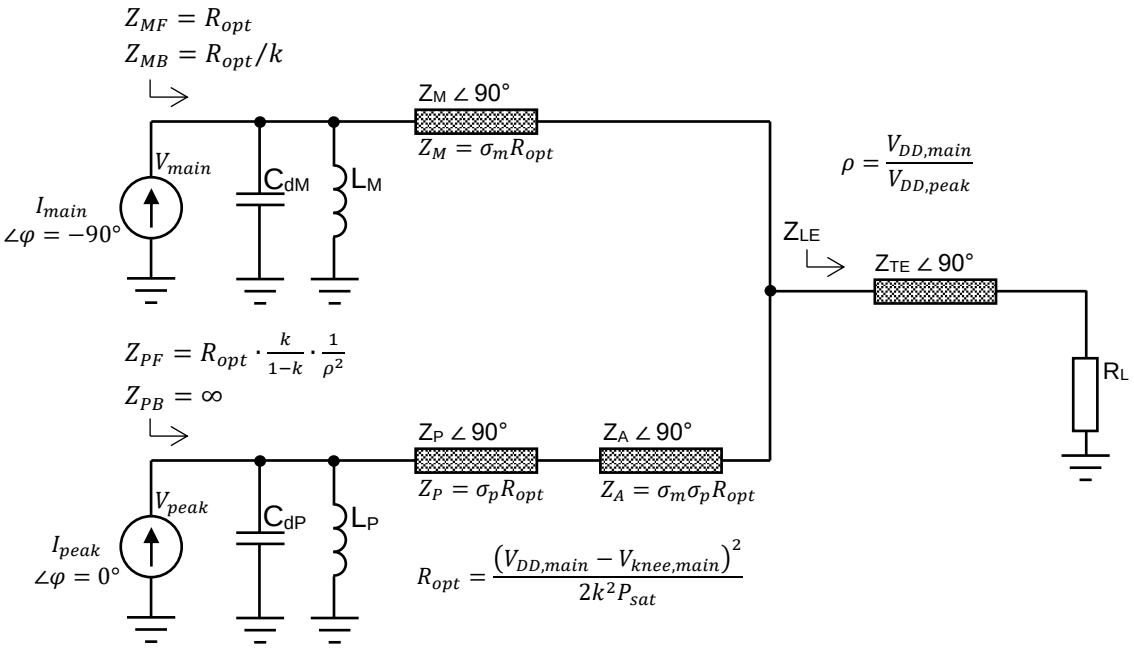


Figure 3.60. A simple circuit diagram for Inverted Doherty PA [24].

3.6.3. Attempt To Use Shorter Transmission Line With Additional Capacitors

Part of transmission line can sometimes be replaced with capacitors. This technique is commonly used in IC design in case to make transmission lines shorter, see Figure 3.61.

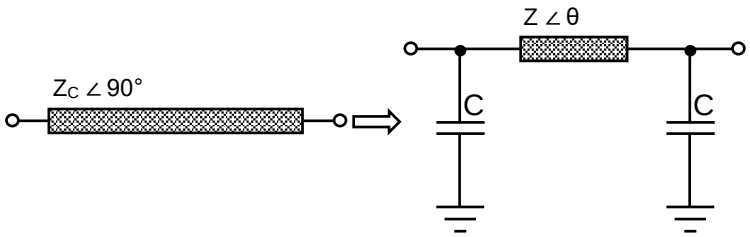


Figure 3.61. How part of transmission line can be replaced with capacitors.

ABCD parameters of transmission line:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 0 & jZ_C \\ j/Z_C & 0 \end{bmatrix}; \tag{3.59}$$

Then ABCD parameters of the equivalent are as follow:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ j\omega C & 1 \end{bmatrix} \begin{bmatrix} 0 & jZ_C \\ j/Z_C & 0 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C & 1 \end{bmatrix}; \tag{3.60}$$

where

$$Z = \frac{Z_C}{\sin\theta}; \tag{3.61}$$

$$\omega C = \frac{\cos\theta}{Z_C}. \tag{3.62}$$

If we will fill-in Z_C, value of parasitic capacitance, (3.59), (3.61) and (3.62) into (3.60) and then solve it, we could get characteristic impedance and electrical length of the shorter TL.

However, this idea didn't give any good results so far but should be investigated further.

3.6.4. Comparison of Simulation Results

Over 45 variations of Doherty PA have been simulated. Their power and efficiency bandwidths were compared at three states: at back-off, just before compression, and at maximum power. Six best topologies have been chosen.

3.6.4.1. Initial Results

The choice of the best topologies has been made as follows. First of all, over 20 topologies that have the broadest minimum 1 dB bandwidth at these states have been chosen. The selected range was from 530 MHz to 630 MHz (highest value). It turned out that these values, in most cases, occur at back-off. Then values before compression and at the maximum power were compared. Finally, the six best variants of topologies were chosen: original SCL-DPA [14] (Figure 3.63), push-pull SCL-DPA (Figure 3.64), differential SCL-DPA (Figure 3.65), PCL-IDPA by [24] with transmission lines (Figure 3.66), with lumped equivalent connected to the main amplifier (Figure 3.67) and with lumped equivalents connected to both amplifiers (Figure 3.68). Simulation results are presented in figures from Figure 3.69 to Figure 3.75. They are summarized in Table 3.3. Numbers in the plots correspond to № of topology in the table. PCL and SCL-IDPA are the narrowest ones, and they are added to the table for reference. Phase distortion at the center frequency is highest for differential SCL-DPA, but it is smaller than by 0.25°. The largest AM/AM distortion is when lumped equivalents are used, and it is by 0.5 V. Otherwise, it is by less than 1 mV. When the input frequency is higher than center frequency by 100 MHz, i.e., 3.6 GHz, AM/AM distortion is by almost 3 V when lumped equivalents are used and in other cases by less than 1 V, see Figure 3.73. Remember that the supply voltage for both amplifiers is 28 V and the maximum input voltage is 1 V. Impedances seen by both transistor drains are shown in Figure 3.75. Figure 3.62 shows how this measurement has been done.

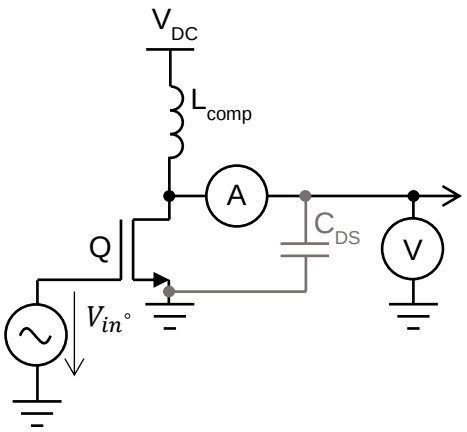


Figure 3.62. Measurement of impedance seen by transistor drain.

It turned out that the replacement of transmission lines with lumped equivalents in case to absorb parasitics didn't give significant power and efficiency bandwidth improvement versus other topologies. Moreover, their power and efficiency plots are less smooth and asymmetrical, IM3 is a lot worse. However, this technique may be very useful with transistors with bigger parasitic capacitances or higher frequency designs. On the other hand, PCL-IDPA with a lumped equivalent connected only to the main amplifier has the highest bandwidth before compression (V_{in} = 0.8 V) of all checked over 45 topologies. The point where compression starts can be found by plotting I_D versus V_{DS} for each transistor for various V_{GS} voltages. However, since transistors are ideal, the compression point is very near V_{in} = 1 V (maximum input voltage).

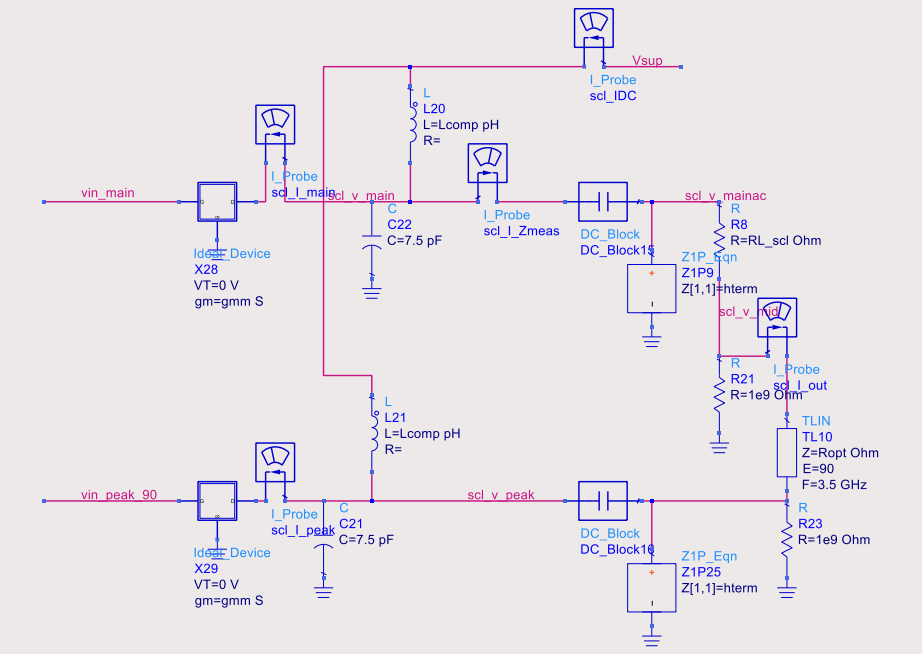


Figure 3.63. Conventional SCL-DPA [14]. The design procedure has been described in section 3.5.2.1.

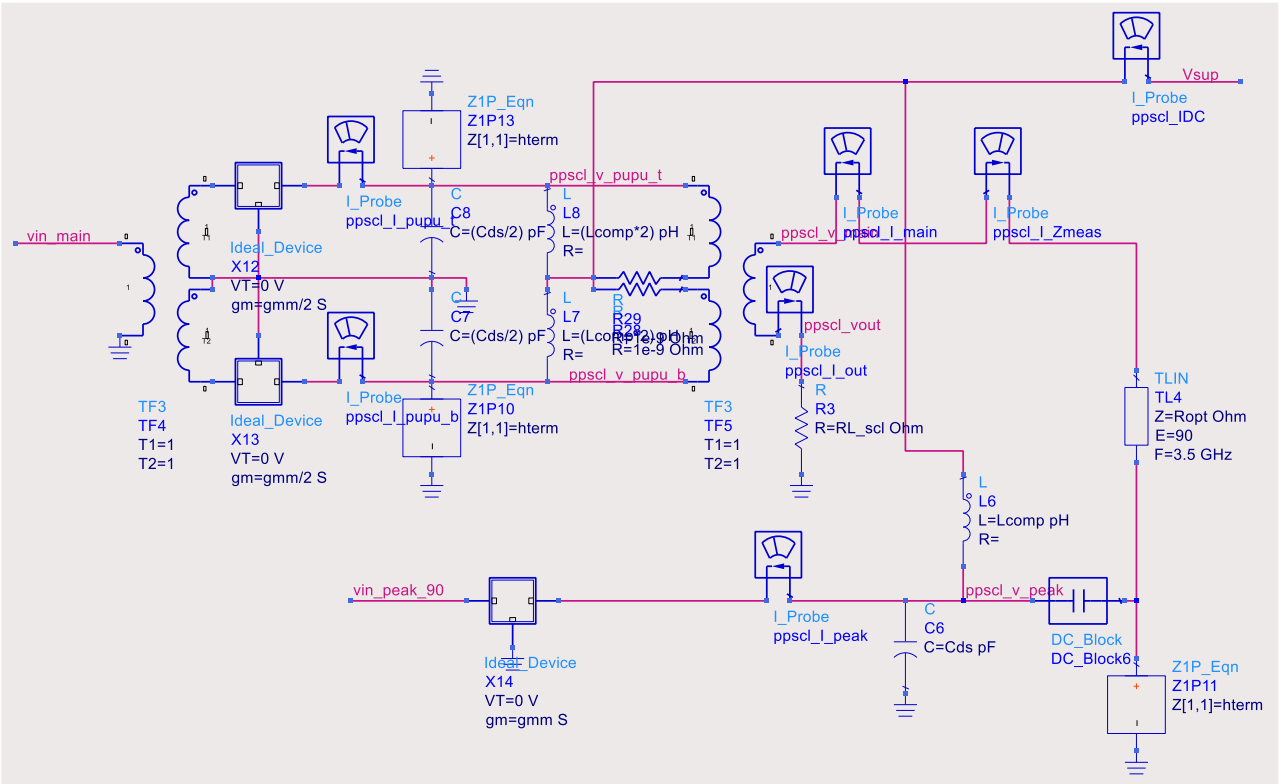


Figure 3.64. Push-pull SCL-DPA. The design procedure has been described in section 3.5.2.2.

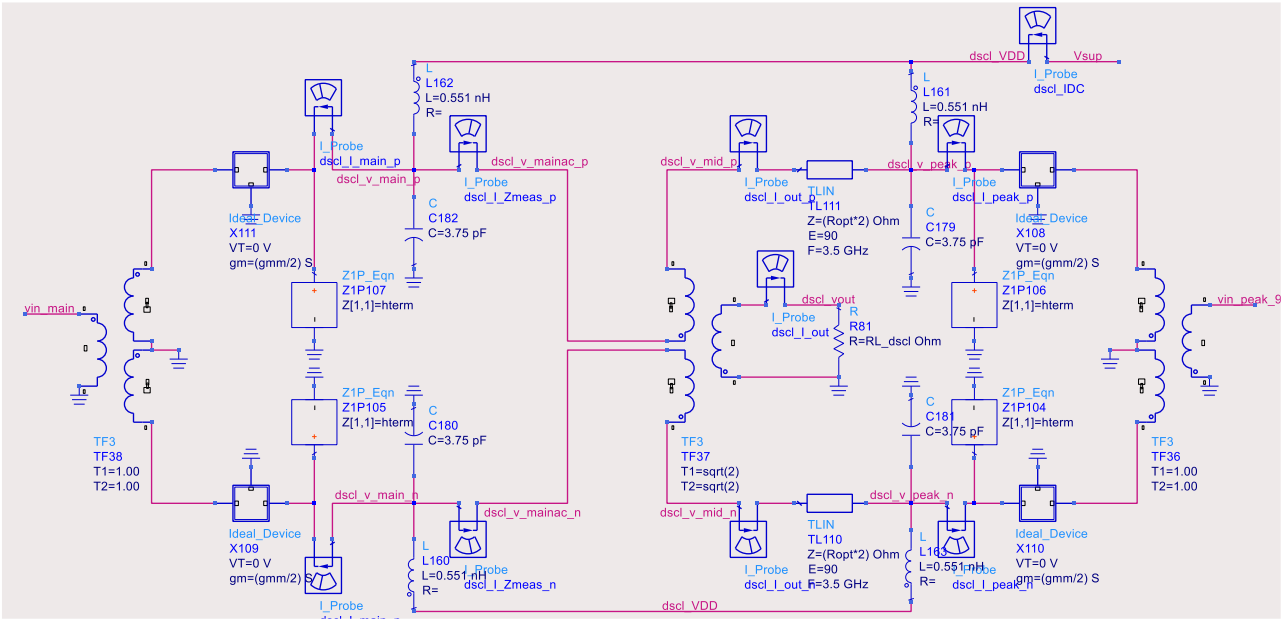


Figure 3.65. Differential SCL-DPA. The design procedure has been described in section 3.5.2.3.

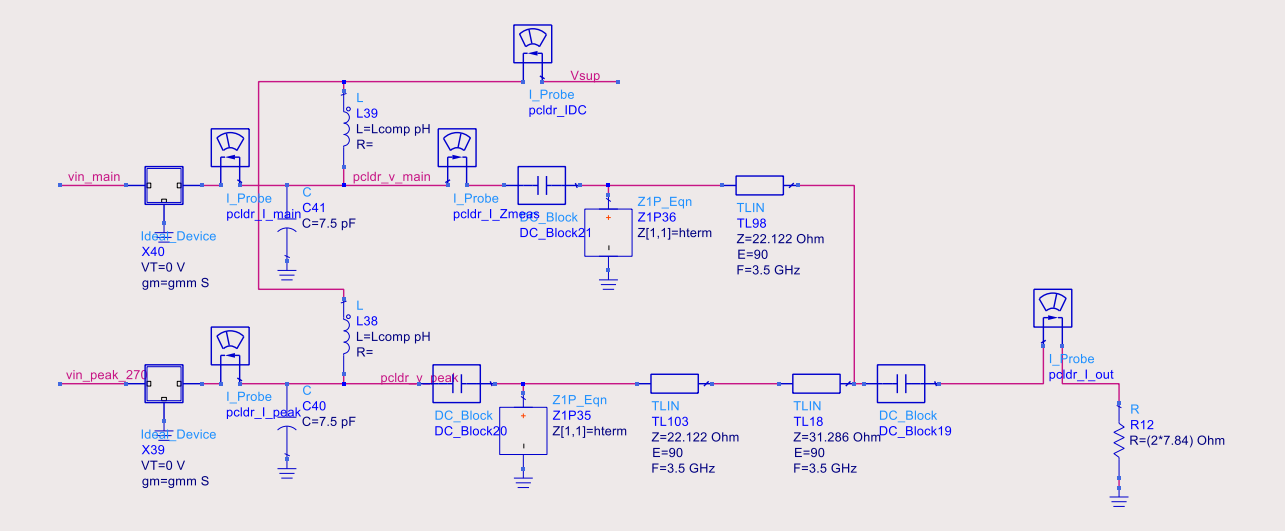


Figure 3.66. PCL-IDPA. Combiner values have been calculated according to [24], see section 3.6.2. The rest of the design procedure matches conventional PCL Doherty PA, see section 3.1.1.

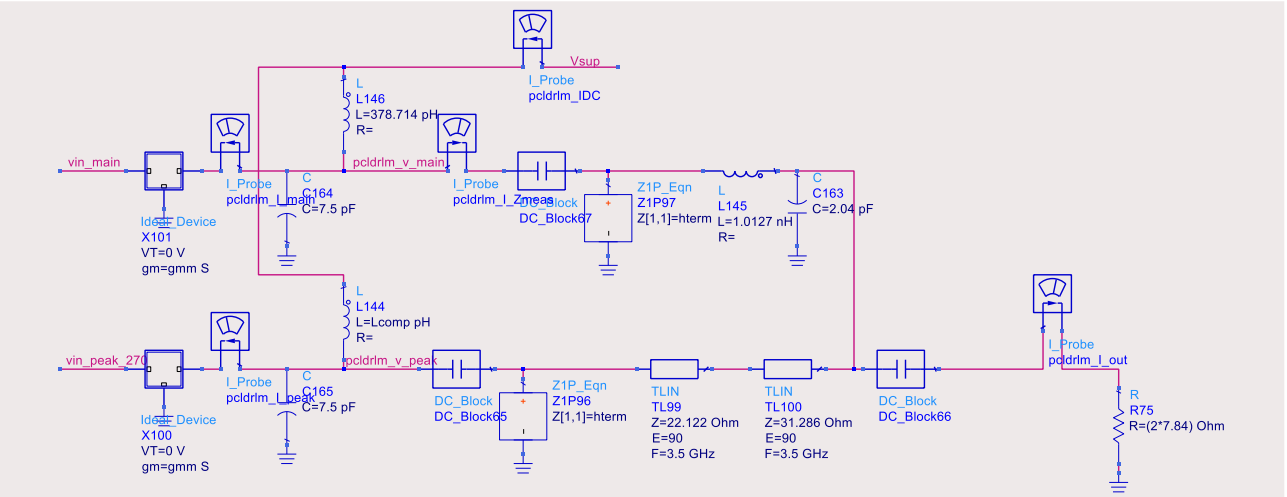


Figure 3.67. PCL-IDPA with the lumped equivalent of the transmission line, which is connected to the main amplifier. Combiner values have been calculated according to [24], see section 3.6.2. The rest of the design procedure matches conventional PCL Doherty PA, see section 3.1.1.

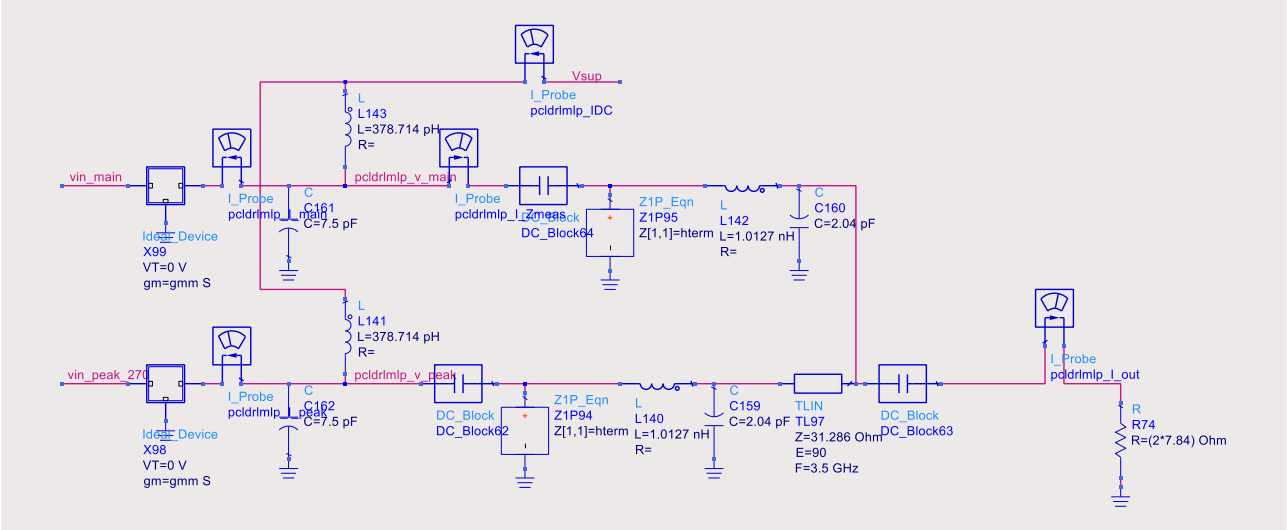


Figure 3.68. PCL-IDPA with the lumped equivalent of the transmission lines, which are connected to both amplifiers. Combiner values have been calculated according to [24], see section 3.6.2. The rest of the design procedure matches conventional PCL Doherty PA, see 3.1.1.

Table 3.3. Performance of the selected topologies. Bandwidth is 1 dB, in MHz.

№	Topology	Back-off (V_{in}=0.49V)			Before Compression (V_{in}=0.8V)			Max Power (Vin=1V)		
		BW	**η_{min}**	**η_{center}**	**BW**	**η_{min}**	**η_{center}**	**BW**	**η_{min}**	**η_{center}**
1.	Inv. PCL [24]	530	0.607	0.766	800	0.565	0.715	990	0.658	0.783
2.	SCL, Push-pull SCL, Differential SCL	560	0.607	0.768	750	0.566	0.716	1130	0.619	
3.	Inv. PCL [24] with lump. eq. to main	610	0.628	0.783	880	0.619	0.716	820	0.73	
4.	Inv. PCL [24] with lump. eq. to main and peak.	530	0.62		**1020**	0.591	0.718	960	0.689	
5.	PCL	360	0.61	0.77	440	0.566	0.715	530	0.62	0.783
6.	Inv. SCL, equations [24]	340				0.571		620		

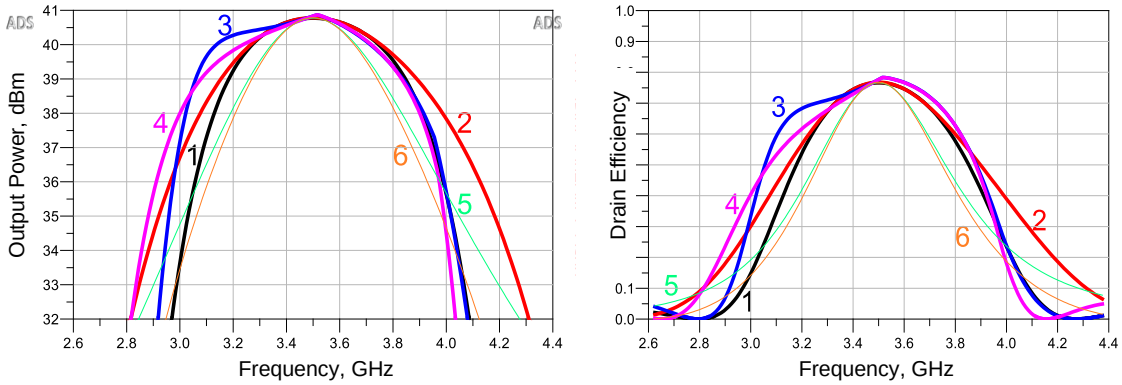


Figure 3.69. Power in dBm (left) and drain efficiency (right) versus frequency at back-off (V_{in}=0.49 V). Numbers correspond to № of topology from Table 3.3.

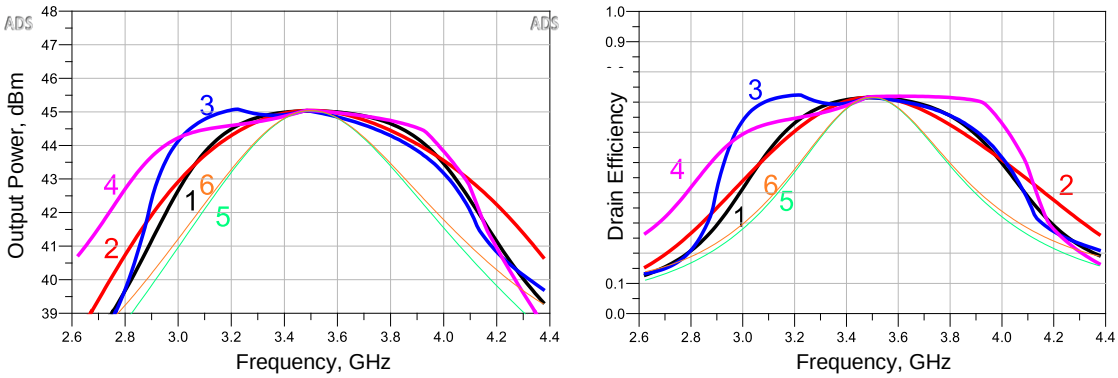


Figure 3.70. Power in dBm (left) and drain efficiency (right) versus frequency just before compression (V_{in}=0.8 V). Numbers correspond to № of topology from Table 3.3.

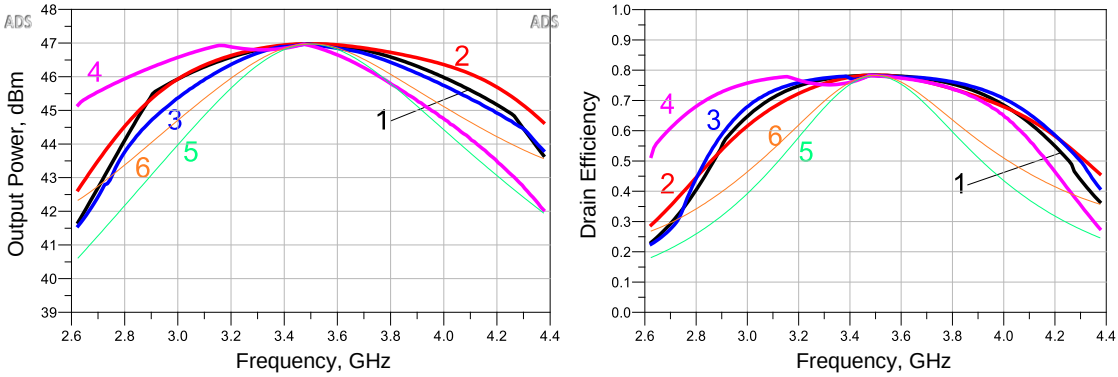


Figure 3.71. Power in dBm (left) and drain efficiency (right) versus frequency at maximum power (V_{in}=1 V). Numbers correspond to № of topology from Table 3.3.

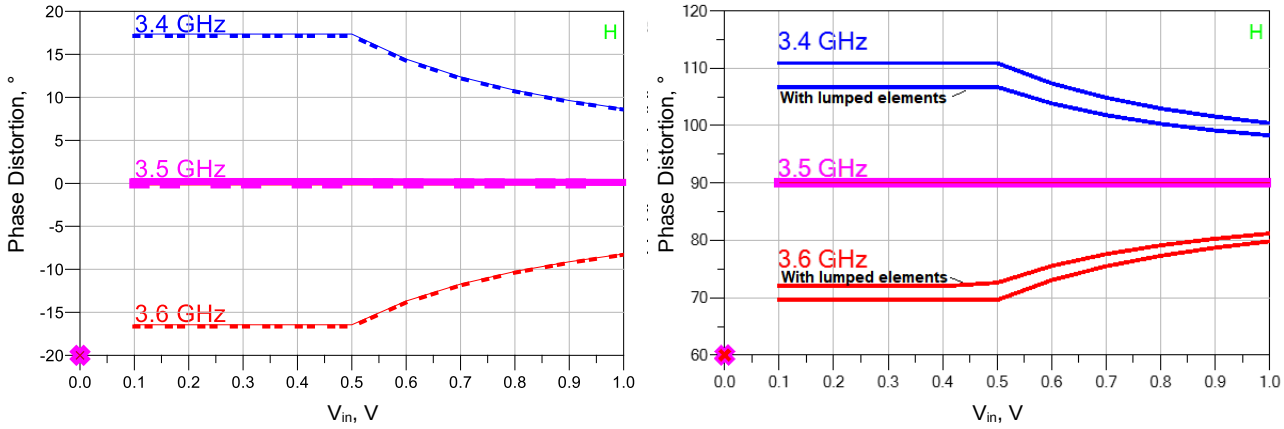


Figure 3.72. Phase distortion. The left plot is for SCL-DPA (overlaps: conventional, push-pull, and differential – group № **2**). The right plot is for PCL-IDPA (with transmission lines and lumped elements – groups № **1, 3** and **4**). Only results of selected topologies are included (Table 3.3).

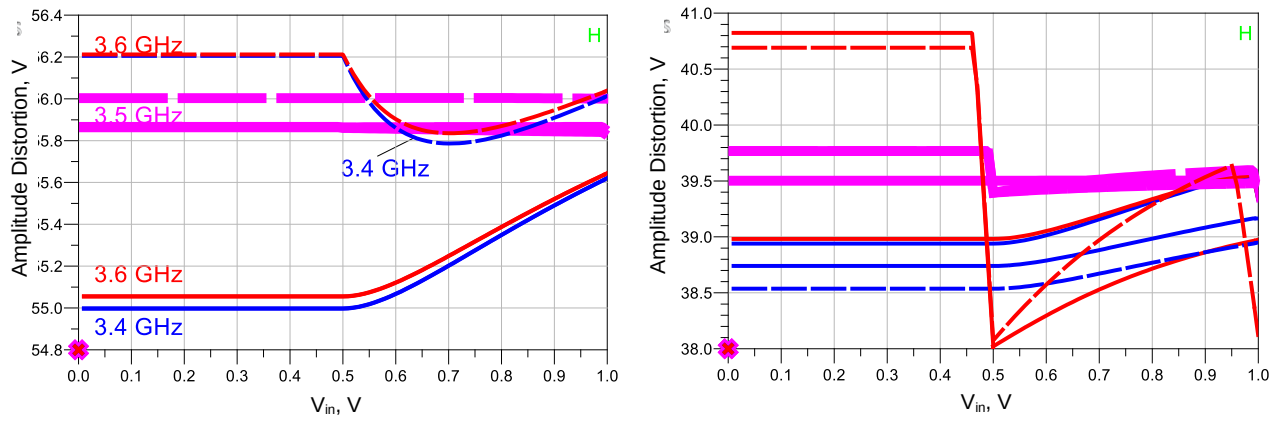


Figure 3.73. Amplitude Distortion. The left plot is for SCL-DPA: conventional (solid line), push-pull (dotted line), and differential (dashed line). The right plot is for PCL-IDPA: with transmission lines (solid line), as shown in Figure 3.67 (dotted line), as shown in Figure 3.68 (dashed line). Only results of selected topologies are included (Table 3.3).

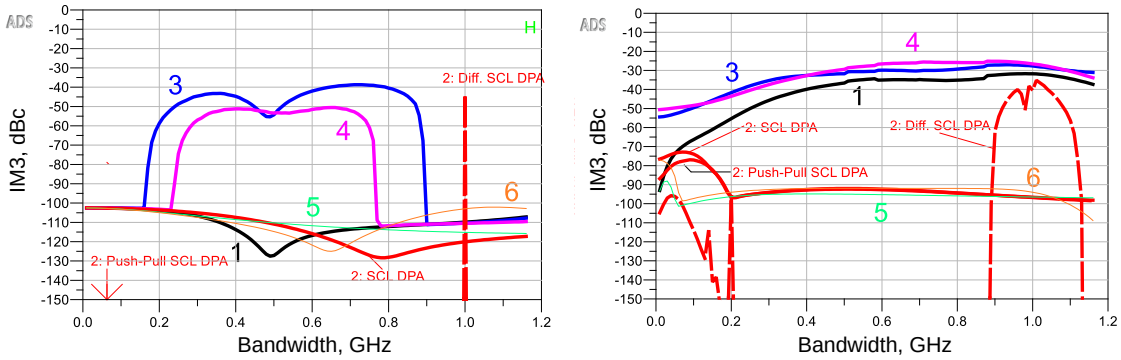


Figure 3.74. IM3 in dBc versus bandwidth at back-off (left) and at maximum power (right). Numbers correspond to № of topology from Table 3.3. Push-pull (at back-off) and differential and version of SCL-DPA goes below -340 dBc. Level bellow -150 dBc is considered irrelevant so it was not included in the plots.

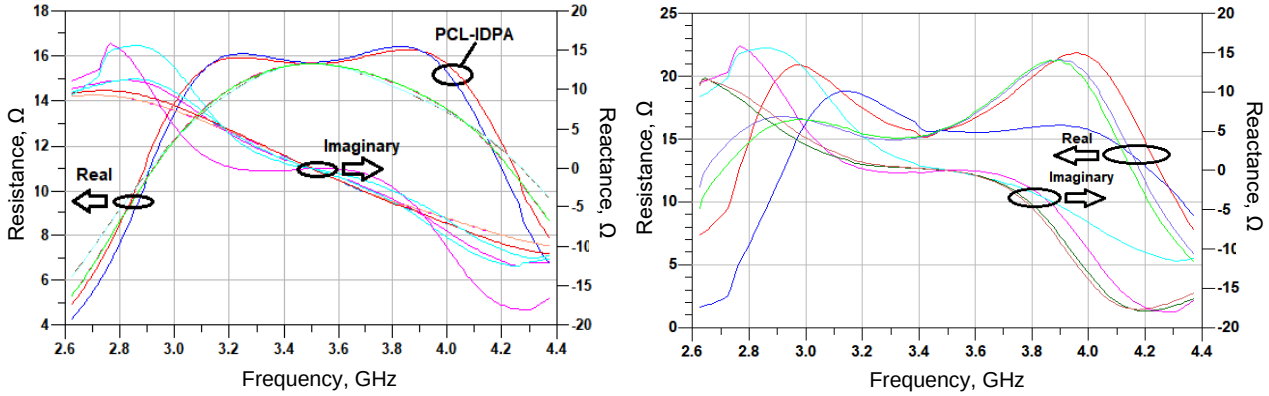


Figure 3.75. The impedance seen at drains of the main transistors and the peak amplifiers versus frequency for all selected topologies (Table 3.4 excluding **5** and **6**) looks very similar. Plots are at maximum power. Left – without lumped equivalents, right – with.

3.6.4.2. Delay Compensation

Transmission lines (and their lumped equivalents) are designed for the center frequency. When the frequency is lower, a transmission line's effective electrical length will be lower than the design value and vice versa. The electrical length depends on frequency linearly. Moreover, the parasitic compensation network makes tank circuits, where the capacitance or inductance dominates if it does not work at its resonant (center) frequency. This results in unwanted imaginary load components seen by non-center frequency components at the drain of the transistor, which also introduces unwanted phase shifts. Thus, it is possible that if the input signal phase is adjusted to the opposite direction

linearly according to frequency, the imaginary part of impedance may be compensated for a certain frequency range. This may result in a bandwidth increase. However, the authors of [16] found out that keeping phase shift between the inputs to the transistors constant during the entire bandwidth results in less impedance dispersion than when a linear phase shift is done according to frequency. This conclusion has been checked during this project. First of all, additional variables X and Y were introduced. The X variable was used with non-inverted DPA (Figure 3.76) and Y with inverted DPA. Figure 3.77 shows how this setup looks like in "Keysight ADS" software. During simulations, it has been noticed that if the phase shift is adjusted only by a minimal amount, it is possible to increase bandwidth at maximum power by around 100 MHz. Experimentally it has been found that optimum values are X = -15 and Y=9.5. This phase shift may be implemented in the digital domain. Phase and AM/AM distortion did not change because these values are very small. IM3 results didn't change significantly for PCL-IDPA topologies, but it deteriorated for SCL-DPA topologies. After comparison of Figure 3.74 (right) with Figure 3.81 it can be seen that while IM3 was below 70 dBc for smaller than 900 MHz bandwidth, now they have similar IM3 results as PCL-IDPA. Impedances seen by transistor drains versus frequency improved, see Figure 3.82. Power and efficiency bandwidth results after improvement are shown in figures from Figure 3.78 to Figure 3.80. Numbers in the plots correspond to № of topology in Table 2.1. Improved bandwidths after the change are shown in green color, and degraded ones are shown in red. Thus, bandwidth at maximum power increased by around 100 MHz for all these topologies; however, at V_{in} = 0.8 V, it degraded by about 100 MHz for inverted DPA topologies but increased by 150 MHz for the conventional SCL (single-ended, differential, and push-pull implementations). Results haven't changed at back-off because here, the peak amplifier is inactive.

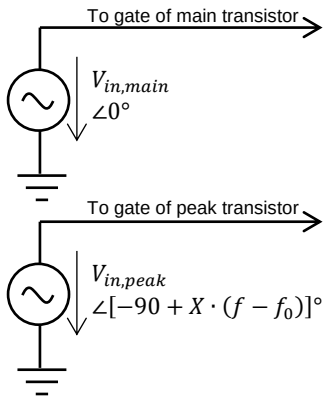


Figure 3.76. Delay compensation. f is input signal frequency, f_0 is design frequency.

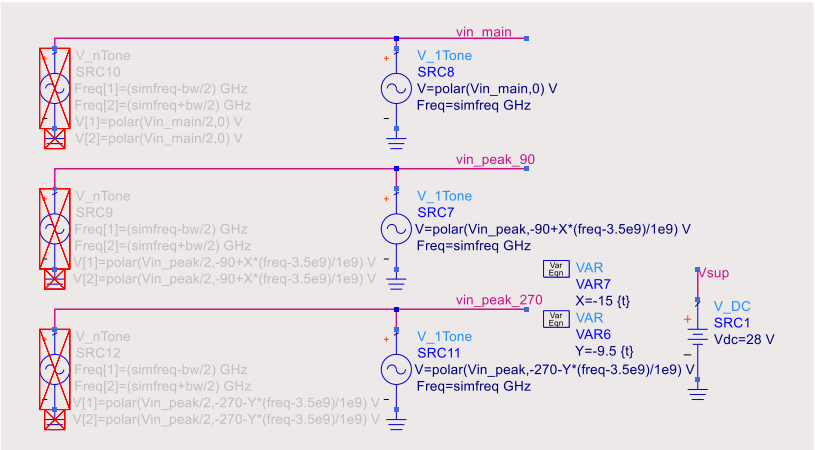


Figure 3.77. Input voltage sources with linear phase shift versus frequency.

Table 3.4. Performance of the best topologies. Bandwidth is 1 dB, in MHz. After improvement.

№	Topology	Back-off (V_{in}=0.49V)			Near Compression (V_{in}=0.8V)			Max Power (Vin=1V)		
		BW	η_{min}	η_{center}	BW	η_{min}	η_{center}	BW	η_{min}	η_{center}
1.	Inv. PCL [24]	530	0.607	0.766	730	0.564	0.715	1100	0.624	0.783
2.	SCL, Push-pull SCL, Differential SCL	560	0.607	0.768	900	0.569	0.716	1240	0.621	
3.	Inv. PCL [24] with lump. eq. to main	610	0.628	0.783	840	0.605	0.716	920	0.709	
4.	Inv. PCL [24] with lump. eq. to main and peak.	530	0.62		940	0.566	0.718	1080	0.614	

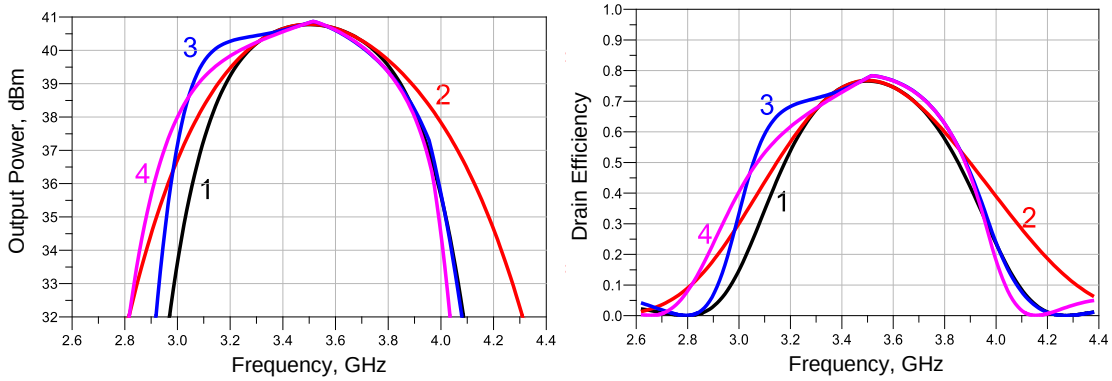


Figure 3.78. Power in dBm (left) and drain efficiency (right) versus frequency at back-off (V_{in}=0.49 V). Numbers correspond to №of topology from Table 3.4. After improvement.

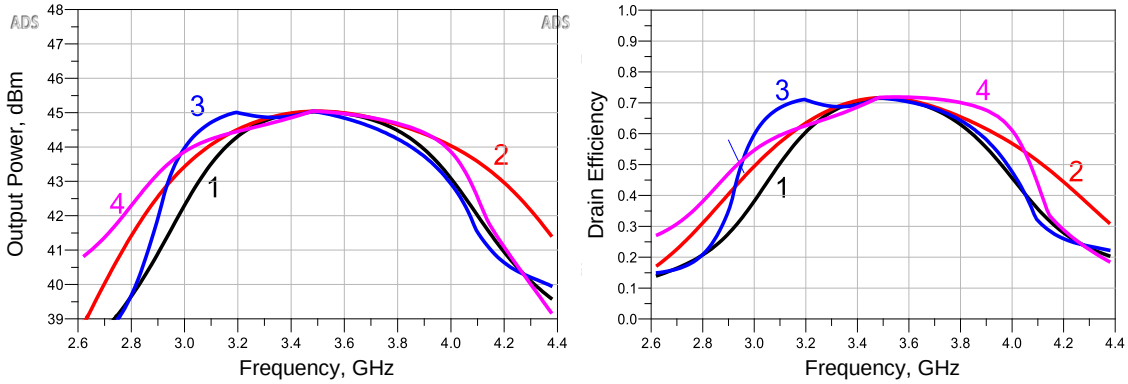


Figure 3.79. Power in dBm (left) and drain efficiency (right) versus frequency just before compression (V_{in}=0.8 V). Numbers correspond to №of topology from Table 3.4. After improvement.

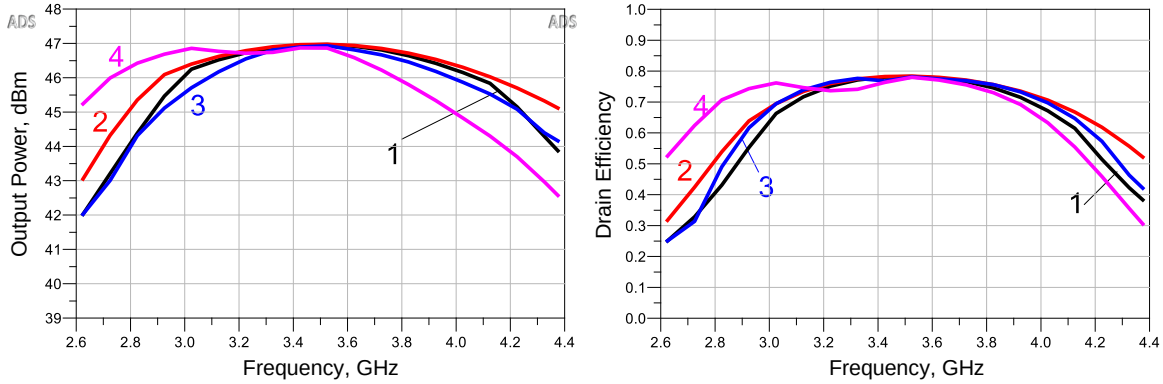


Figure 3.80. Power in dBm (left) and drain efficiency (right) versus frequency at maximum power (V_{in} = 1 V). Numbers correspond to №of topology from Table 3.4. After improvement.

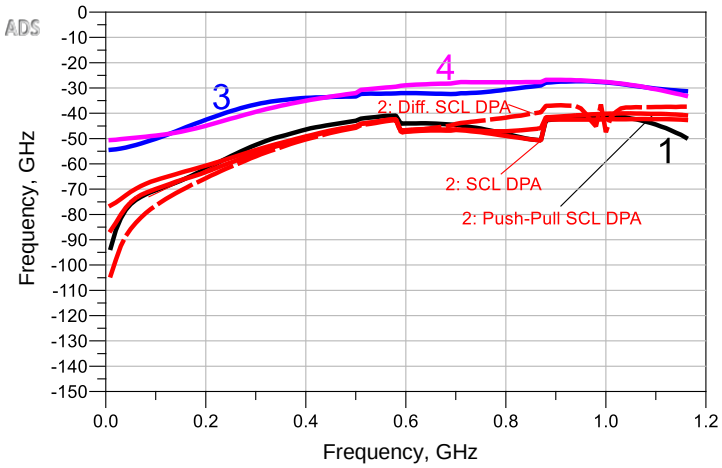


Figure 3.81. IM3 in dBc versus bandwidth at maximum power. Numbers correspond to № of topology from Table 3.4. Red – push-pull SCL-DPA, gray – SCL-DPA, cyan – differential SCL-DPA.

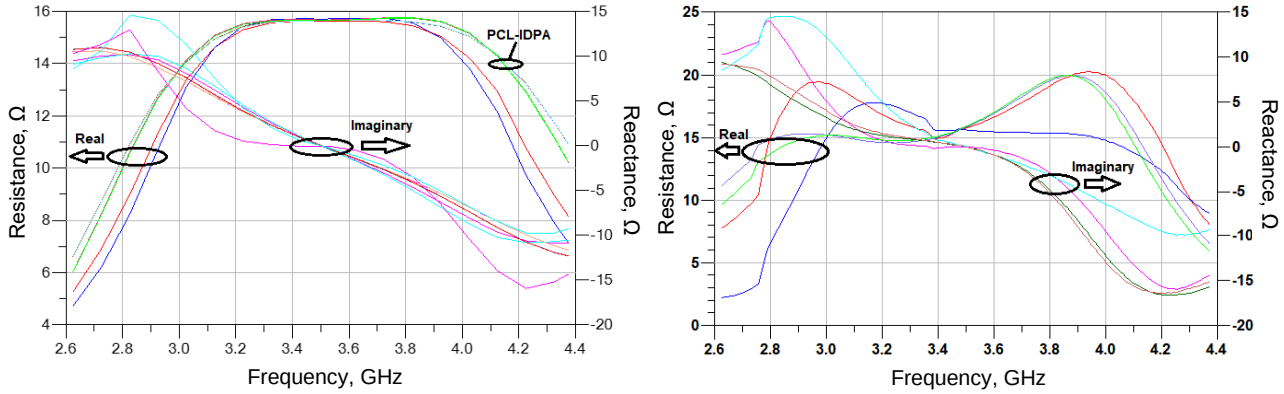


Figure 3.82. The impedance seen at drains of the transistors of the main and the peak amplifiers versus frequency for all selected (Table 3.4) topologies looks very similar. Plots are at maximum power. Left – without lumped equivalents, right – with. After improvement.

3.7. Possible Use in Digital Transmitters

The power divider and the phase aligner can be removed. Each transistor can be replaced with a transistor array (segmented device) where drains of the transistors (segments) are connected. Then all gates can be connected to a digital circuit which can be made using conventional high-speed CMOS technology. Then signal splitting, phase alignment, and the peak amplifier activation threshold can be implemented in the digital domain. Such setup could benefit from the advantages that segmented devices offer (when working in the right configuration), including better linearity, higher efficiency, and simpler high-power design, as introduced in section 2.5. Moreover, this configuration allows easy adjustment (calibration) of the phase difference between the main and the peak amplifier. It also allows changing the threshold when the peak amplifier is activated. Furthermore, this makes implementation of delay compensation relatively simple because it can be done in the digital domain. The delay compensation may give some small benefits, as we have found out in section 3.6.4.2. A possible implementation of PCL-IDPA with lumped equivalents of transmission lines connected to the main and the peak amplifiers is shown in Figure 3.83 (parasitic capacitances have not been shown).

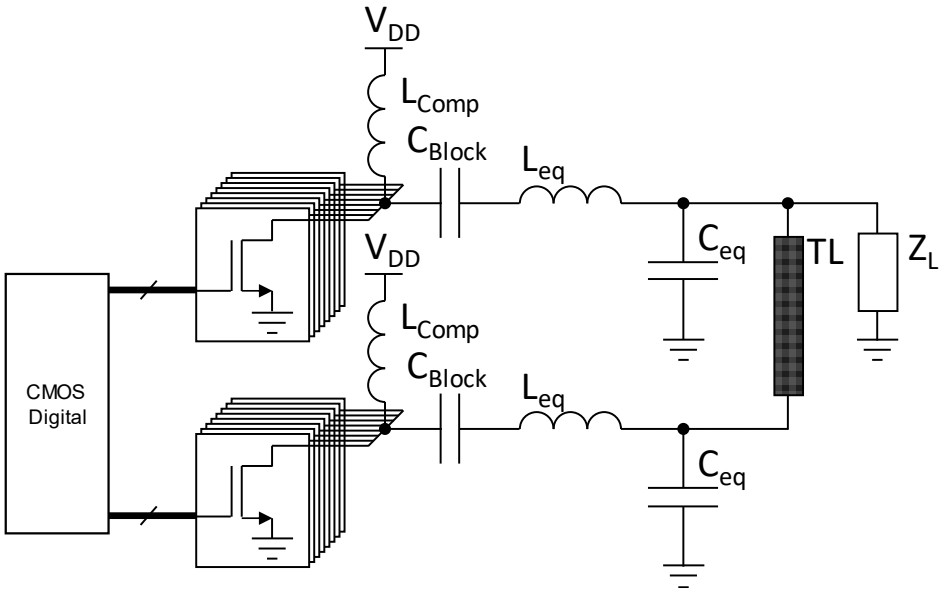


Figure 3.83. A potential implementation of PCL-IDPA in DTX.

3.8. Other Variations of Doherty PA

Some variations of Doherty PA topology use more than two branch amplifiers (more than one peak amplifier), for example, 3 or 4, and are called 3- or 4-way Doherty PA, respectively. A 4-way Doherty

PA has three peak amplifiers, and it is still under research and is not yet in commercial use. It seems impractical to use more amplifiers than that. More peak amplifiers give the opportunity to have multiple output power back-off points. That allows making the amplifier more efficient [28, 29]. In general, they are called *multi-way Doherty PAs*. There are also so-called *distributed Doherty PAs* [2]. The main, the peak, or both amplifiers consist of several lower power amplifiers, which have their outputs combined using power combiners [30, 31]. They are out of the scope of this work, so they will not be discussed further.

3.9. Conclusion

The operation of classical and inverted 2-way Doherty amplifiers has been explained, and design examples have been shown. Possible bandwidth and efficiency improvement techniques have been presented and applied. Over 45 variations of 2-way conventional and inverted Doherty PA have been checked by using harmonic balance simulation, and the 6 best ones have been selected for a more detailed investigation. The highest bandwidth at back-off (610 MHz) has been achieved by PCL-IDPA (designed according to [24]) with the lumped equivalent of the transmission line connected to the main amplifier. The other results are shown in Table 3.3. Next, a delay compensation technique has been applied, and bandwidth at maximum power increased by around 100 MHz, but for PCL-IDPA, it decreased near compression by approximately 100 MHz. Moreover, IM3 of SCL-DPA topologies degraded. Parasitic capacitance absorption with lumped equivalents of transmission lines helped increase power bandwidth at back-off from 530 MHz to 610 MHz; however, IM3 versus bandwidth became worse.

According to harmonic balance simulation results, PCL-IDPA is significantly more wideband than PCL-DPA while having similar power and efficiency bandwidth as SCL-DPA (see Table 3.3). However, only very ideal elements were used except those transistors had parasitic capacitances between drain and source. Thus, simulations did not consider possible matching errors, while the main advantage of SCL topologies versus PCL is that it is easier to design a matching network for it than for PCL with the same specifications. As a result, SCL-DPA can have smaller matching errors than PCL-DPA. This is because SCL-DPA requires a higher load impedance than PCL-DPA. The matching error typically leads to a reduction of realizable bandwidth. Thus**, it is likely that in electromagnetic simulation and practical implementation SCL-DPA will have higher bandwidth than PCL-IDPA and PCL-DPA.**

Furthermore, bandwidth specification would vary less between manufactured units than in PCL-DPA case (assuming the same component tolerances used). Finally, it is also important to note that if SCL-DPA were made completely push-pull, its load impedance would be even higher. For example, symmetrical SCL-DPA needs 4x higher load impedance than the same PCL-DPA. Moreover, if it is made entirely push-pull, it will need 8x higher load impedance than PCL-DPA [16]. This trick cannot be applied to PCL-DPA to increase its load impedance. Complete push-pull implementation has **not** been tested during this project.

Although conventional Doherty power amplifiers are analog, each transistor can, in principle, be replaced with multiple transistors having their drains connected. Then gate of each transistor could be connected to a digital circuit. That would allow fully digital implementation, which may allow better drain efficiency and linearity [22]. This could be a topic for future research.

4

Pseudo Doherty Amplifiers

Traditional parallel and series-connected Doherty power amplifier topologies need an impedance inverter for their operation. This impedance inverter always limits the achievable bandwidth due to its phase dispersion versus frequency. The previous chapter proved this by performing simulations of the topologies omitting circuit parasitics, other than the transistors' output capacitances. These results had been presented in the last two rows of Table 3.2, see page 50.

Recently, alternative topologies which do not need this inverter but still provide a Doherty amplifier-like operation have been researched [2, 11]. Sometimes they are referred to as Pseudo Doherty (PD) amplifiers. Such a topology is described in this chapter, and its schematic is presented in Figure 4.1. Its architecture is based on a Load Modulated Balanced Amplifier (LMBA) using a 90° -3 dB coupler. Ideally, the topology has unlimited bandwidth; however, it is still limited by the bandwidth of the coupler and transistor parasitics in practice. However, couplers can be a lot more wideband than impedance inverters. Furthermore, some transmission lines in the couplers can be replaced by lumped equivalents, and then (a part of) the transistor parasitic output capacitance can be absorbed in the coupler.

4.1. Principle of Operation

The LMBA is a 90° hybrid-based amplifier with two amplifiers connected to the ports with a 90° offset. See the red circled section of Figure 4.1. Consequently, the signal phase between these amplifiers has to differ also by 90° to add constructively at the hybrid RF output port. In the original LMBA implementation, a single-ended input signal is converted, using an additional 90° hybrid to provide these 90° offset amplifier input signals. The isolated port can be terminated by an isolation resistor or take in the output signal of another amplifier with a controlled RF input signal [32]. This latter configuration allows dynamic optimization of the RF output power/efficiency of the LMBA and frequency performance by externally adjusting the amplitude and phase of this controlled signal. The

amplified control amplifier (CA) signal can modulate the impedance seen by the balanced amplifiers in its phase and magnitude.

The impedance modulation contributes to the Doherty-like operation of the LMBA. Namely, the control signal power adds to the RF output power, while the CA is not affected by the BA operation since it is connected to the isolated port of the hybrid (provided that the BAs use the proper 90° phase offset).

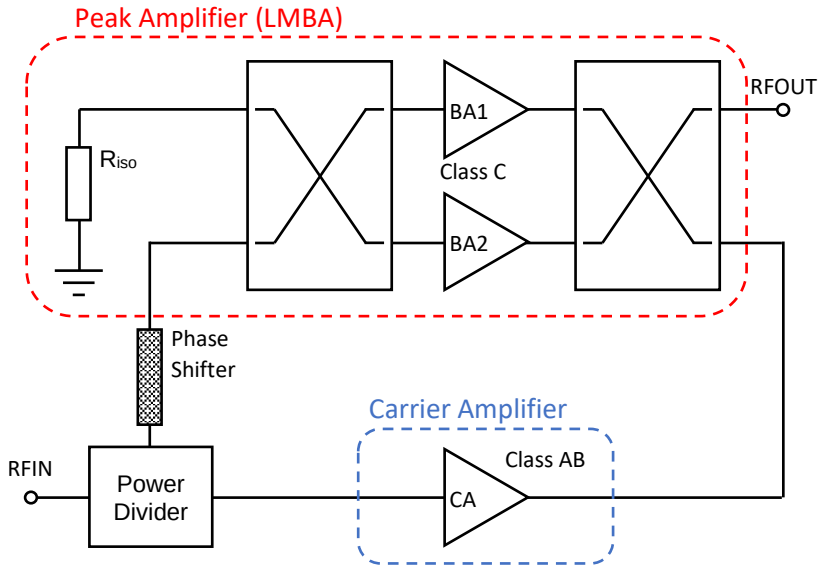


Figure 4.1. Original Pseudo Doherty Load Modulated Balanced Amplifier (PD-LMBA) [2]

If the balanced amplifiers (BA) are used as the peak, and the control amplifier (CA) as the main amplifier, a Pseudo Doherty LMBA (PD-LMBA) can be created. In an analog implementation, the CA can work in Class AB, and the BA or peak amplifier in Class C, with the “Doherty” threshold voltage chosen according to the power back-off specification. It is also important to note that the optimized back-off efficiency can be achieved with only one static setting of phase offset at any given frequency. Such a wideband phase shifting can be easily implemented using a transmission line, see Figure 4.1 [2].

The power divider, the phase shifter, and the input hybrid can be replaced by a configuration where phase-shifting and signal power conditioning are done in the digital domain (e.g., by a CMOS controller). Such a configuration would allow adjusting these parameters in the software domain after the design is completed. This latter arrangement can be implemented as a DTX (digital transmitter) with digital signals controlling the LDMOS/GaN power transistors segments with connected drains (see Figure 4.2). These segmented transistors can replace the BA and CA amplifiers. In addition, it should be noted that an analog implementation (Figure 4.1) suffers from a significant flaw, namely when the PD-LMBA works above back-off, the main amplifier gets oversaturated, yielding lower efficiency and increased distortion at high powers (Figure 4.3). The figure also shows that the best solution is to limit the input voltage to the main amplifier when the input is above back-off to avoid oversaturation. Such a precise limiting is challenging to implement at RF frequencies in the analog domain, but it can be done straightforwardly in the digital domain. Class B is also included in Figure 4.3. This shows what would happen if we would not limit the input signal to the CA. Note that there we assume that transistors do not have threshold voltage. In an analog implementation, the use of Class B for the main PA is avoided because of the distortion that occurs when the main gets oversaturated, as shown by plot (a). Another reason is that pure Class B in an analog implementation would yield a too low gain and a non-linear response for small signals due to the threshold voltage of practical devices. Class AB is used instead. As we can see from Figure 4.3, it also has a slightly closer to ideal behavior.

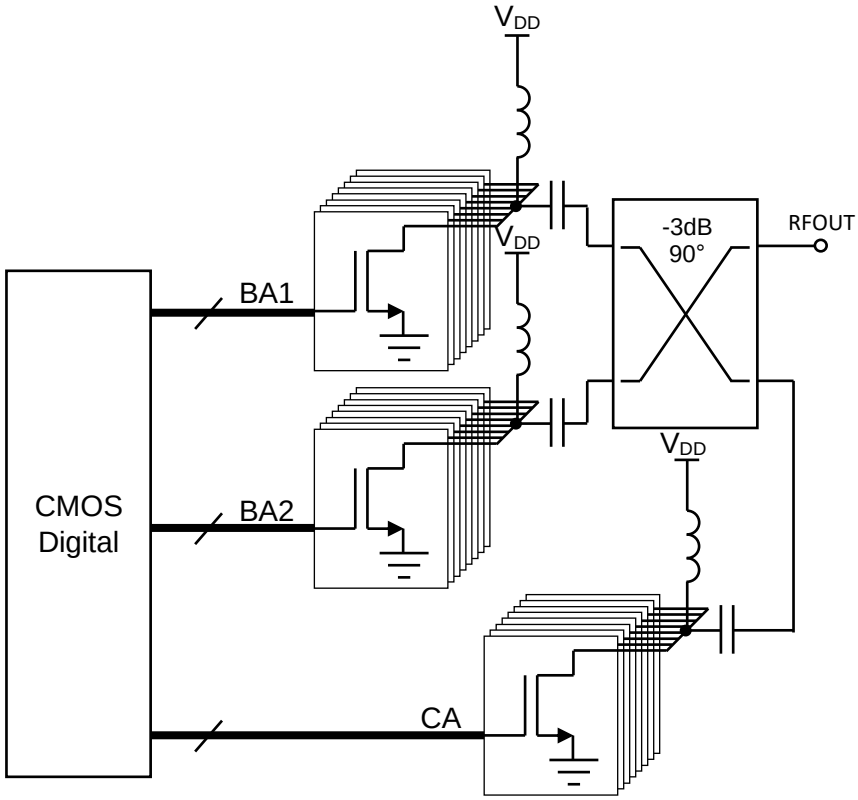


Figure 4.2. Possible digital implementation of PD-LMBA. Transistors can be LDMOS or GaN.

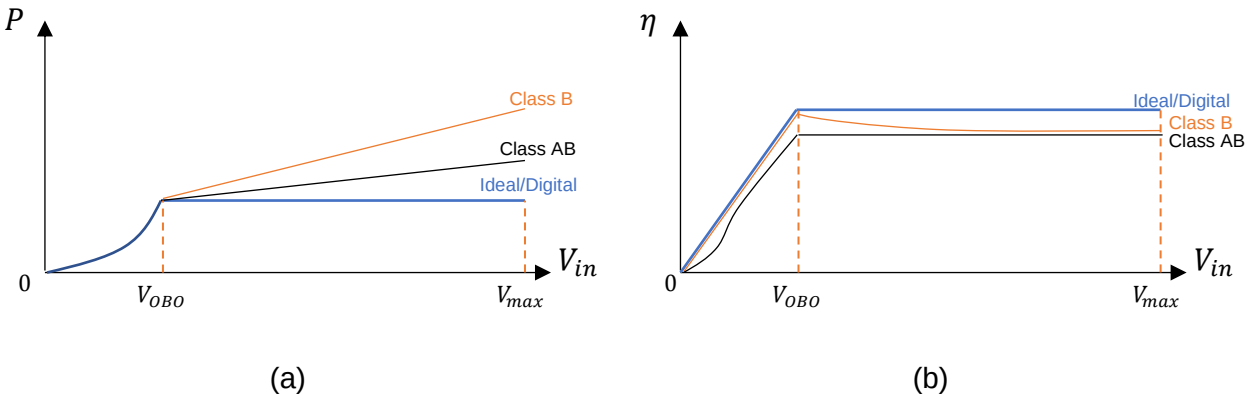


Figure 4.3. Power (a) and efficiency (b) plots of PD-LMBA when BA is not connected.

4.1.1. Review of LMBA

The LMBA is derived from the conventional balanced amplifier (BA) architecture. A BA also has two amplifiers whose inputs and outputs are split and combined using quadrature hybrids outputs. The only difference between the LMBA and BA is that the isolated port of the hybrid in an LMBA is no longer terminated with an isolation resistor (impedance equal to the hybrid's port characteristic impedance), but driven by a control(ed) amplifier [2]. Thus, an LMBA features two identical amplifiers (BA1 and BA2) and a control amplifier. These amplifiers are represented as current sources in the generalized ideal schematics, see Figure 4.4a. The easiest way to analyze the LMBA operation of the circuit is by using the Z-parameter matrix for an ideal 3 dB hybrid. Both branch line coupler and coupled lines can be used to implement the quadrature hybrid. For our analysis, we will assume the use of coupled lines (CL). Their Z-parameters are given as [32]:

$$Z_{CL} = Z_0 \cdot \begin{bmatrix} 0 & 0 & -j & -j\sqrt{2} \\ 0 & 0 & -j\sqrt{2} & -j \\ -j & -j\sqrt{2} & 0 & 0 \\ -j\sqrt{2} & -j & 0 & 0 \end{bmatrix}. \tag{4.1}$$

Then the following matrix equation can be written:

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = Z_0 \cdot \begin{bmatrix} 0 & 0 & -j & -j\sqrt{2} \\ 0 & 0 & -j\sqrt{2} & -j \\ -j & -j\sqrt{2} & 0 & 0 \\ -j\sqrt{2} & -j & 0 & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix}. \tag{4.2}$$

Note that for the Z matrix, the port currents I_n are defined to flow into the black-box and the port-voltages V_n are measured with respect to the common ground. The behavior of LMBA can be considered the result of the three excitation sources driving the quadrature hybrid. Then according to Figure 4.4b the currents in the matrix equation (4.2) are defined as follows. $I_2 = -I_B$ and $I_4 = -jI_B$ are the input currents from BA1 and BA2 respectively. $I_1 = -I_{out}$ is the output current. $I_3 = I_{con} = -jI_C\, e^{j\varphi}$ denotes the current from the control signal source, I_{con}. φ is phase of the control signal in respect to I_B. Since the output port (1) is terminated with a load, the voltage on the load is,

$$V_1 = Z_0 \cdot I_1 = -Z_0 \cdot I_{out}$$

Similarly,

$$\begin{aligned} V_2 &= Z_{BA2} \cdot I_2 = -Z_{BA2} \cdot I_B; \\ V_4 &= Z_{BA1} \cdot I_4 = -Z_{BA1} \cdot jI_B; \\ V_3 &= Z_C \cdot I_3 = -jZ_C I_C e^{j\varphi}. \end{aligned} \tag{4.3}$$

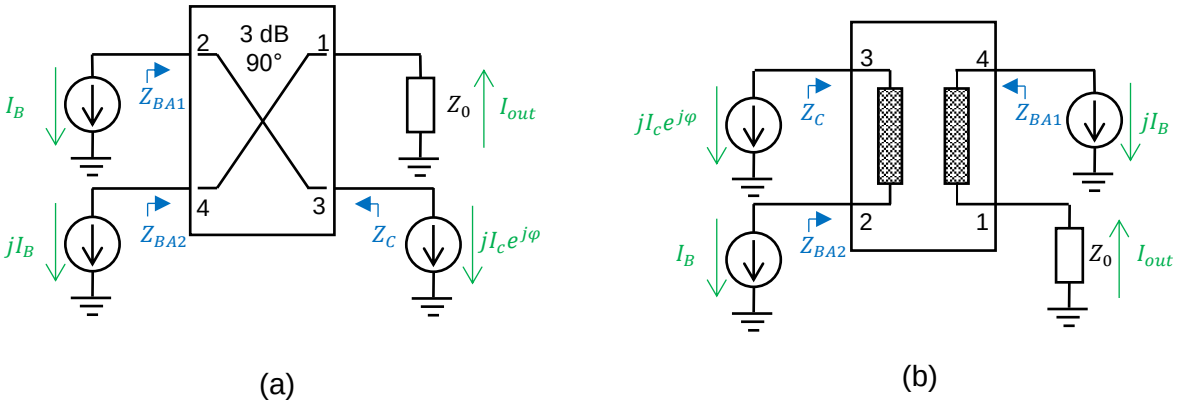


Figure 4.4. Ideal schematics of the output combining network for analyzing the proposed PD-LMBA architecture. (a) is with generalized hybrid, (b) is case when coupled lines are used as a hybrid.

Thus, after filling in these variables to (4.2), the following equation can be obtained:

$$\begin{bmatrix} -Z_0 I_{out} \\ -Z_{BA2} I_B \\ -jZ_C I_C e^{j\varphi} \\ -jZ_{BA1} I_B \end{bmatrix} = Z_0 \cdot \begin{bmatrix} 0 & 0 & -j & -j\sqrt{2} \\ 0 & 0 & -j\sqrt{2} & -j \\ -j & -j\sqrt{2} & 0 & 0 \\ -j\sqrt{2} & -j & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{out} \\ -I_B \\ -jI_C e^{j\varphi} \\ -jI_B \end{bmatrix}. \tag{4.4}$$

Since a 3 dB quadrature coupler is symmetrical, the injected control signal is split equally into two halves, appearing at the drain of the PA of each branch. Then after solving (4.4), we get

$$I_{out} = \sqrt{2} I_B + I_C e^{j\varphi}; \tag{4.5}$$

$$Z_C = Z_0; \tag{4.6}$$

$$Z_{BA} = Z_{BA1} = Z_{BA2} = Z_0\left(1 + \sqrt{2}\cdot\frac{I_C e^{j\varphi}}{I_B}\right). \tag{4.7}$$

Equation (4.7) concludes that the control signal interacts with the output signals generated by the two branch power amplifiers. This interaction leads to load-modulation behavior represented by the red part of the equation [2]. According to equation (4.6) the load impedance seen by the CA is always equal to the characteristic impedance of the hybrid port.

Equations for the output power can be derived from (2.7). There $I^*_{fund} = -I^*_{out}$ and $V_{fund} = -Z_0 I_{out}$. Then

$$P_{out} = \mathrm{Re}\left\{\frac{1}{2}\cdot I_{out}\cdot I^*_{out}\cdot Z_0\right\}. \tag{4.8}$$

If we apply Euler's formula to (4.5):

$$I_{out} = \sqrt{2}I_B + I_C(\cos\varphi + j\sin\varphi). \tag{4.9}$$

It is known that a complex number multiplied by its complex conjugate is equal to its squared modulus, i.e. $I_{out}\cdot I^*_{out} = |I_{out}|^2$. Thus, if we will apply this rule to (4.8) and fill-in (4.9) then we will get:

$$P_{out} = \frac{1}{2}\cdot Z_0\cdot\left|\sqrt{2}I_B + I_C\cos\varphi + jI_C\sin\varphi\right|^2 = Z_0\left(I_B^2 + \sqrt{2}I_B I_C\cos\varphi + \frac{1}{2}\cdot I_C^2\right). \tag{4.10}$$

According (4.10), the output power is highest when $\cos\varphi$ value is highest. Thus, when $\varphi = 0°$. However, this only applies to the ideal case. In practice parasitics, a non-ideal coupler design can change this optimum φ value to different but still constant value. When $\varphi = 0°$ then (4.10) turns to

$$P_{out} = Z_0\left(I_B^2 + \sqrt{2}I_B I_C + \frac{1}{2}\cdot I_C^2\right). \tag{4.11}$$

The control signal power can be expressed analogically to (4.8). Thus,

$$P_{con} = \frac{1}{2}\cdot|I_{con}|^2\cdot Z_0. \tag{4.12}$$

Fill-in $I_3 = I_{con} = -jI_C\, e^{j\varphi}$ to (4.12), and then the following equation can be obtained:

$$P_{con} = \frac{1}{2}\cdot\left|-jI_C e^{j\varphi}\right|^2\cdot Z_0 = \frac{1}{2}\cdot I_C^2\cdot Z_0. \tag{4.13}$$

Power provided by each BA:

$$P_{BA} = \frac{1}{2}\cdot|I_B|^2\cdot\mathrm{Re}\{Z_{BA}\}. \tag{4.14}$$

After filling-in (4.7) to (4.14):

$$P_{BA} = \frac{1}{2}\cdot|I_B|^2\cdot Z_0\mathrm{Re}\left\{1 + \sqrt{2}\cdot\frac{I_C e^{j\varphi}}{I_B}\right\} = Z_0\left(I_B^2 + \sqrt{2}I_B I_C\cos\varphi\right). \tag{4.15}$$

Now if we compare equations (4.10), (4.13) and (4.15), we can see that (4.10) can be rewritten as

$$P_{out} = 2P_{BA} + P_{con}. \tag{4.16}$$

The obtained equation (4.16) is crucial when designing PD-PMBA. Transistors for analog implementation can be sized according to the current scaling ratio $I_{C,max}/I_{B,max}$ which can be derived from (2.7)

$$\frac{I_{C,max}}{I_{B,max}} = \frac{V_{BDC} \cdot P_{C,max}}{V_{CDC} \cdot P_{B,max}} \tag{4.17}$$

where $I_{C,max}$ and $I_{B,max}$ are the currents of the fundamental tone, $P_{C,max}$ and $P_{B,max}$ are powers of the fundamental tone, V_{CDC} and V_{BDC} the supply voltages used for CA and BA, respectively.

While the original LMBA needs dual inputs, the single input (or RF-input) has been proposed and demonstrated [2]. In [2] the LMBA with the RF-input uses a control amplifier (CA) instead of an independent control signal (CSP). Furthermore, the CA and BA share the same RF input. Namely, the RF-input power is split to the CA and BA at a given ratio through a dedicated power divider. The CA provides its signal power to the isolation port of the output coupler, see Figure 4.1. The load impedance of the BAs depends on the power (i.e., current) and the phase of the control signal generated by the CA.

4.1.2. Pseudo-Doherty LMBA Mode

PD-LMBA operation can be split into the following three operating regions [2]:

- ***Low-Power Region*** ($P_{out} < P_{max}/PBO$): When the PA is operating at a low power level below than the predefined back-off power (PBO), the BA is completely turned off, i.e., $I_B = 0$, as represented in Figure 4.5a plot, see the part when $V_{in} < V_{PBO}$. Therefore, in this region the output power is only generated by the control amplifier (CA). Thus, the control amplifier (CA) in the PD-LMBA has a similar purpose to the main amplifier in Doherty topologies. From (4.7), we can see that the impedances of BAs (LP means Low-Power):

  $$Z_{BA1,LP} = Z_{BA2,LP} = \infty. \tag{4.18}$$

  From (4.6):

  $$Z_{C,LP} = Z_0. \tag{4.19}$$

  In this region, the total LMBA efficiency is equal to the efficiency of CA, which increases towards maximum as the CA voltage swing saturates at the target PBO power.
- ***Back-Off Region*** ($P_{max}/PBO \leq P_{out} < P_{max}$): When the power rises to the target PBO level, the CA should reach its voltage and current saturation, this $I_C = I_{C,max}$. As the power further increases, the BA is turned on and I_B starts to increase from 0 toward $I_{B,max}$, as it is presented in Figure 4.5a. Since the load seen by the CA never changes as it has been proven by (4.6), the saturation of CA is maintained, while I_C remains its maximum value of $I_{C,max}$ [2]. Note that this is different behavior than in traditional Doherty PAs. Thus, in this back-off region, the load-modulation behavior of BA1 and BA2, as well as CA impedance, is given by the following equations, which are derived from (4.6) and (4.7), respectively:

  $$Z_{BA1,BO} = Z_{BA2,BO} = Z_0 \left(1 + \sqrt{2} \cdot \frac{I_{C,max} e^{j\varphi}}{I_B}\right); \tag{4.20}$$

  $$Z_{C,BO} = Z_0. \tag{4.21}$$

  In this region, the CA remains saturated with the highest efficiency, while BA's efficiency can also be significantly boosted through load modulation. As a result, enhanced back-off efficiency of the overall LMBA can be achieved [2].
- ***Saturation "Region"*** ($P_{out} = P_{max}$): As the power increases to the saturation of BA, the CA and BA are both saturated. Then the saturation load impedances of both BAs and CA can also be derived from (4.6) and (4.7), respectively, and they are as follows [2]:

  $$Z_{BA1,SAT} = Z_{BA2,SAT} = Z_0 \left(1 + \sqrt{2} \cdot \frac{I_{C,max} e^{j\varphi}}{I_{B,max}}\right); \tag{4.22}$$

  $$Z_{C,SAT} = Z_0. \tag{4.23}$$

The ratio of $I_{C,max}/I_{B,max}$ is dependent on the PBO range, and this ratio is smaller for higher PBO values. At its saturation, all the LMBA PAs achieve their maximum efficiency [2].

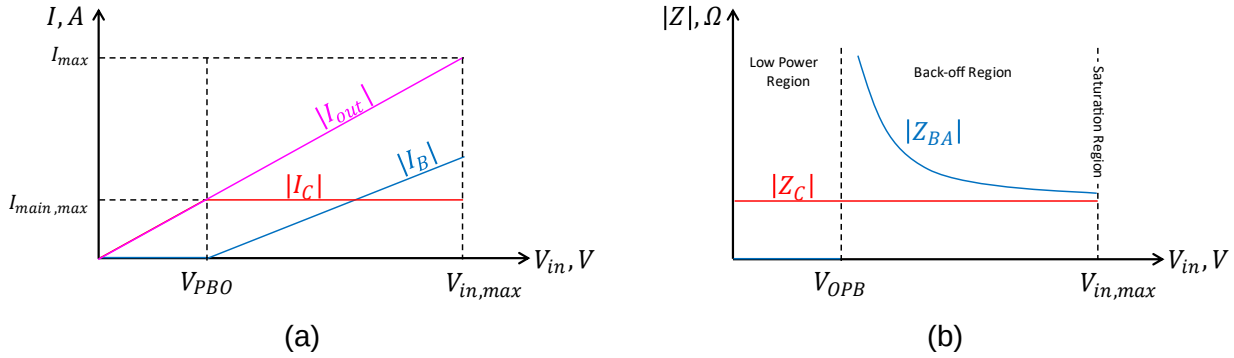


Figure 4.5. PD-LMBA operation. (a) – drains and output currents versus the input voltage, (b) – effective impedance seen by CA and BAs versus the input voltage.

Note that the impedance seen by CA is Z_0 (Figure 4.5) across all these three regions, while in DPA, this impedance decreases when power is above back-off (Figure 3.3c). This is why PD-LMBA does not need an impedance inverter that fundamentally limits the bandwidth of DPA topologies. However, in an actual implementation, some load modulation of Z_C still occurs due to [12]:

- design/implemenation imperfections,
- the powers of BA1 and BA2 are not exactly equal because of the non-ideality in their driving conditions.

Overall, the operations of the BA and CA in PD-LMBA are to a great extent independent since the load impedance of the CA remains Z_0, and the BA's load modulation occurs mainly because due to variation of its own current, see the $I_{C,max}/I_B$ component of (4.20).

4.1.3. Amplitude Control

To achieve the maximum output power back-off efficiency (OPB), the CA must saturate, and the BAs must be turned on at the back-off point. The CA (and BA) should not oversaturate; otherwise, significant distortion will occur. These conditions can be achieved by setting the power dividing ratio between BA and CA, correctly choosing threshold voltage for the BA (which acts as the peak amplifier), and limiting the input voltage for CA to its saturation voltage when the input signal rises above back-off. Input voltage limiting can be implemented in digital domain, while it is relatively complex in the analog domain.

4.1.4. Phase Control

The *optimum phase* angle depends mainly on the electrical length of the coupler and the amplifiers involved. In the idealized example with coupled lines and driving current sources, this phase angle is 0° yielding an ohmic load trajectory in Figure 4.6 (assuming Class B operation), see (2.13). This condition yields the maximum back-off efficiency of the PD-LMBA. Furthermore, it can be noted that high efficiency can be achieved over the entire power back-off range using a constant CSP phase [2]. However, it will work out that on top of the phase itself also the optimum group delay is important when dealing with wideband modulated signals, as we will address in section 4.3.5.

To summarize, the most important advantage of PD-LMBA is that it does not need an impedance inverter which limits the bandwidth in DPA topologies. Its other advantages over other known load-modulation techniques are:

- The CA is loaded with a constant impedance which ideally is not affected by the BA. This considerably simplifies the complexity of broadband design without the need to control the load trajectory over a wide frequency range [2].
- Optimal load modulation behavior for the entire bandwidth can be achieved only by setting a static phase offset between BA and CA. Using this approach, the circuit and system complexity can be reduced [2].

- A matching network between the hybrid's ports and amplifiers can be avoided if the CA uses a lower supply voltage or if an asymmetrical hybrid would be used.

Disadvantages:

- When impedance matching is avoided, and high power is desired, required coupler port impedances may become low (e.g., 6.94 Ω for 50 W and 28 V supply voltage). The odd impedance of the coupled lines would have to be even lower (2.87 Ω if a single section is used). It may be difficult to design such a hybrid. Moreover, the optimum load impedance is equal to the coupler port impedance. Such low value complicates matching to the actual load.
- Couplers introduce additional power losses. These losses depend on phase and amplitude errors, and non-idealities of the coupler(s). In contrast, in conventional DPA an impedance inverter together with a joint node (Figure 3.1) acts as a power combiner which is significantly easier to design. However, its losses also depend on the phase error. Phase error can be avoided when phase shift is done in the digital domain because then it can be easily fine tunned after manufacturing.

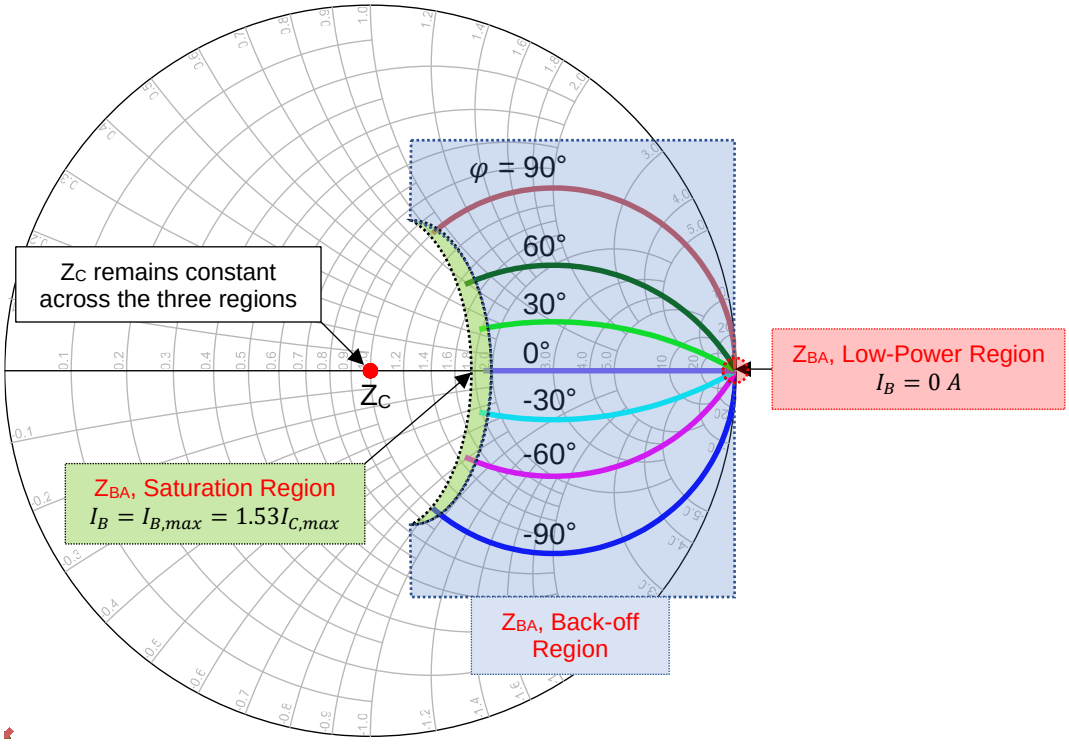


Figure 4.6. Dynamic CA and BA load impedances using the ideal generalized model for 10 dB PBO [2].

4.2. Derivation of Design Equations

This work provides design examples. In the simplest one the coupler is symmetrical, and (extra) matching networks are present between the coupler and the (balanced) amplifiers (BA). In the second design example, no intermediate matching networks are present, and the asymmetrical coupler in combination with the CA amplifier provide directly the desired impedance level to the BA amplifiers. This configuration represents the current state of the art and is first demonstrated in [12]. Asymmetrical off-the-shelf hybrid (IPP-2281IT) which has 25 Ω and 50 Ω port impedances has been chosen and such a way matching networks between the hybrid and the amplifiers have been avoided. In the final design example, a symmetrical coupler and adjusted supply voltages between the CA and BA amplifiers are used to meet their PD-LMBA matching requirements. All these design examples will be presented in section 4.3, but first, we will derive a few other equations which will make the design procedure more straightforward. That is the aim of this section.

4.2.1. With Symmetrical Coupler & Matching Networks

When a 3 dB symmetrical quadrature coupler is used, and all amplifiers use the same supply voltage, the effective load impedance seen at the ports by the BA needs to be known. This information is required to determine the ratios of the BA's output matching networks. First, let's take (4.7) and assume that the amplifier works at maximum power and $\varphi = 0°$ (the optimum phase as shown in Figure 4.6). Then fill-in $I_{B@max}$ which can be expressed using (4.14), furthermore the impedances (and currents) have to be real and then we end-up with the following equation:

$$Z_{BA@max} = Z_0 + \sqrt{2}Z_0 \cdot \frac{I_{C@max}\sqrt{Z_{BA@max}}}{\sqrt{2P_{B@max}}}. \tag{4.24}$$

After solving (4.24) for $Z_{BA@max}$:

$$Z_{BA@max} = \frac{1}{4} \cdot \left(\frac{Z_0 I_{C@max}}{\sqrt{P_{B@max}}} + \sqrt{\frac{Z_0^2 I_{C@max}^2}{P_{B@max}} + 4Z_0} \right)^2. \tag{4.25}$$

The derived equation (4.25) is very useful during the design procedure. When we know the effective impedance seen by BAs ($Z_{BA@max}$) and optimum load impedance of each amplifier ($R_{C,opt}$ and $R_{B,opt}$), we can design impedance matching networks. $R_{B,opt}$ should be matched to $Z_{BA@max}$ and $R_{C,opt}$ to Z_0 (coupler port characteristic impedance). $P_{B@max}$ and $P_{C@max}$ can be found using (4.13) with (4.16). Optimum impedances and $I_{C@max}$ can be calculated by following a conventional amplifier design procedure which has been described in section 2.3. Design examples of such PD-LMBA will be presented in section 4.3.1.

4.2.2. With Asymmetrical Coupler & Without Matching

When an asymmetrical quadrature coupler is used to skip the need for intermediate matching between the transistors and the quadrature coupler, we need to determine the coupler's Z-parameter matrix. This matrix can be used in circuit simulations, e.g., it can be entered in "Z4P_Eqn" block of "Keysight ADS" software, and for the synthesis of the coupler. Unfortunately, asymmetrical couplers are rarely presented in the literature, so their Z-parameters are typically unknown. However, their Z-parameters can be derived from a pair of symmetrical coupled lines because the wanted behavior in the PD-LMBA circuit is known, so a system of equations can be constructed.

The Z-parameter matrix for two symmetrical coupled lines (CL) is shown in (4.1). The circuit with CL for analysis is shown in Figure 4.4b. It can be noticed that $Z_{13} = Z_{31} = Z_1$ and $Z_{24} = Z_{42} = Z_2$. Where Z_1 is the characteristic impedance of ports 1 and 4, where Z_2 is the characteristic impedance of ports 2 and 3. Though it is not yet obvious how Z-parameters which are on the diagonal of the matrix are expressed using Z_1 and Z_2. It is known that they are all equal because the coupler still has symmetry between its ports 1, 3, and 2, 4. Let's assign for the moment the value $-jX$ to all of them, as shown in (4.43).

$$Z_{CL} = \begin{bmatrix} 0 & 0 & -jZ_1 & -jX \\ 0 & 0 & -jX & -jZ_2 \\ -jZ_1 & -jX & 0 & 0 \\ -jX & -jZ_2 & 0 & 0 \end{bmatrix}. \tag{4.26}$$

Now we can write an equation similar to (4.2) and follow the same steps as in section 4.1.1. The voltages $V1$ to $V4$ will be different from that section and will be as follows:

$$V_1 = -jZ_1\left(-jI_C e^{j\varphi}\right) + (-jX) \cdot (-jI_B) = -Z_0 I_C e^{j\varphi} - XI_B;$$

then:

$$I_1 = -\frac{V_1}{Z_1} = I_C e^{j\varphi} + \frac{XI_B}{Z_1};$$

and the voltage at port 2 (V_2):

$$V_2 = -XI_C e^{j\varphi} - Z_2 I_B = -I_B \left(X \cdot \frac{I_C e^{j\varphi}}{I_B} + Z_2 \right); \tag{4.27}$$

the multiplier in brackets represents Z_{BA}. If we compare it with (4.7), we can see when the coupler is symmetrical ($Z_1 = Z_2 = Z_0$), when $X = Z_0\sqrt{2}$. Where Z_0 is characteristic impedance of each symmetrical coupler port. The voltage at port 4 (V_4) is:

$$V_4 = -jXI_1 + jZ_2 I_B = -jI_B \left(X \cdot \frac{I_C e^{j\varphi}}{I_B} + \frac{X^2}{Z_1} - Z_2 \right). \tag{4.28}$$

If we compare this last equation with (4.3), we can notice that the multiplier $\left(X \cdot \frac{I_C e^{j\varphi}}{I_B} + \frac{X^2}{Z_1} - Z_2 \right)$ in (4.27) is also Z_{BA}, like in (4.27). Regarding the theory of PD-LMBA operation, which has been described in section 4.1, the coupler port impedances seen by each balanced amplifier must be equal (Z_{BA1}=Z_{BA2}=Z_{BA}). Thus, we can write an equation using components which are shown in red in equations (4.27) and (4.28):

$$\frac{X^2}{Z_1} - Z_2 = Z_2.$$

After solving the equation above, we get:

$$X = \sqrt{2Z_2 Z_1}. \tag{4.29}$$

Thus, Z_{BA} can be expressed as (assuming $\varphi = 0°$):

$$Z_{BA} = \sqrt{2Z_1 Z_2} \cdot \frac{I_C}{I_B} + Z_2. \tag{4.30}$$

The following equation can be obtained by assuming that the amplifier works at maximum power, then solving (4.30) and then replacing Z_1 with $R_{CA,}$ and Z_{BA} with $R_{BA,pt}$ because Z_1 and Z_{BA} should be equal to optimum load impedances of CA and BA respectively:

$$Z_2 = \frac{1}{4} \cdot \left(\sqrt{\frac{2R_{C,opt} I_{C@max}^2}{I_{B@max}^2} + 4R_{B,opt}} - \sqrt{2R_{C,opt}} \cdot \frac{I_{C@max}}{I_{B@max}} \right)^2. \tag{4.31}$$

The final (4.31) equation will prove to be very useful during the design procedure.

Note that equations that have been introduced in section 4.1 can be obtained from equations presented in this subsection if one would fill-in Z_0 to Z_1 and Z_2. This is because solutions for the case when the coupler is entirely symmetrical is a subset of solutions for the asymmetrical coupler, which have been introduced in this subsection.

4.2.3. With Symmetrical Coupler & Lower Supply Voltage for Control Amplifier

The problem with the first variant (see subsection 4.2.1) is that intermediate matching networks are required. Matching networks can limit bandwidth and introduce losses. The disadvantage of the second variant (see subsection 4.2.2) is that asymmetrical couplers are challenging to design. None of these problems exist in the following variant. Here the supply voltage for the main amplifier is lowered in favor of reaching the proper matching conditions. Then a symmetrical coupler can be used, and an intermediate matching network is not necessary. As a result, higher bandwidth may be possible. We need to derive an equation for the supply voltage that is required for the main amplifier. First, we take (4.7) and assume that the amplifier works at maximum power, also that $\varphi = 0°$ because this is optimal phase, see Figure 4.6. Then we fill-in I_C from (2.7) and the optimum CA load impedance ($R_{C,}$) as Z_0 from (2.13). Assume that all values are real because this is needed for correct operation. By following these steps, the following equation can be obtained:

$$Z_{BA@max} = \frac{V_{sup,CA}^2}{2P_{C@max}} \cdot \left(1 + \sqrt{2} \cdot \frac{2P_{C@max}}{I_{B@max} V_{sup,CA}}\right). \tag{4.32}$$

Now solve (4.32) for $V_{sup,}$. Then replace Z_0 with $R_{opt,}$ and the following equation has been obtained:

$$V_{C,sup} = P_{C@max}\sqrt{2}\left(\sqrt{\frac{1}{I_{B@max}^2} + \frac{R_{B,opt}}{P_{C@max}}} - \frac{1}{I_{B@max}}\right) \tag{4.33}$$

This final (4.42) equation is very useful in the design procedure of this variant.

4.3. Design Examples

The three different flavors of PD-LMBA design with ideal couplers are provided in this section. It also shows how to compensate for phase dispersion caused by the electrical delay, typically introduced by the hybrid and parasitics. The first example is the simplest one. Here an off-the-shelf symmetrical hybrid is used, which has a 50 Ω port impedance. In this case, the optimum load impedance of each amplifier is unequal to the effective impedances offered by the coupler ports. Thus, intermediate impedance matching between the PAs and the coupler is required. This matching can be done by using a lumped or λ/4 transformer.

The second design example is very similar to the first one, except that the optimum impedances are chosen to match the hybrid port impedances (alternatively, a custom hybrid can be designed to match the optimum impedances of all amplifiers). In this case, intermediate impedance matching between the PAs and coupler is no longer required. This approach represents the current state of the art where an asymmetrical hybrid has been used in such a way that each effective port impedance is equal to the corresponding amplifier optimum load impedance so matching networks are avoided between the coupler and the amplifiers [12]. The final example shows how impedance matching requirements can be directly satisfied using a symmetrical hybrid. Example design specifications have been given already in section 3.5.

4.3.1. Using Symmetrical Off-The-Shelf Hybrid

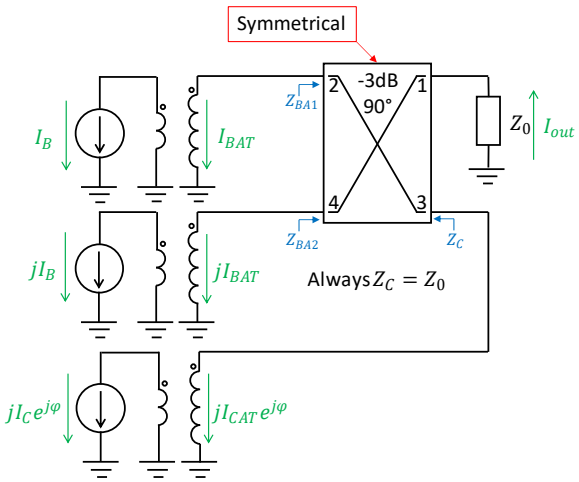


Figure 4.7. PD-LMBA with a symmetrical coupler and transformers for impedance matching

For the most obvious design procedure, let's assume that we have off-the-shelf symmetrical coupled lines with 50 Ω port impedances and that the power supply voltage V_{sup} for each amplifier is the same and equal to 28 V. This topology is shown in Figure 4.7. Here each amplifier's optimum load impedance needs to be matched to the coupler port impedances. In this example, that is done by using ideal transformers. Thus, design steps are as follows (values which have to be used in the circuit are shown in red):

1. Powers of the control and each balanced amplifier, using (3.7), (4.16):
   $P_{C@max} = 10^{-k,dB/10} \cdot P_{out@max} = 10^{-6/10} \cdot 50 \approx 12.6\,W$;

$P_{B@max} = (P_{out@max} - P_{C@max})/2 = (50 - 12.6)/2 \approx 18.7\ W$.

2. Currents which have to be provided by the amplifiers (before transformers), using (2.7):
   $I_{B@max} = \frac{2P_{B@max}}{V_{sup}} = \frac{2 \cdot 18.7}{28} \approx \mathbf{1.34\ A}$;
   $I_{C@max} = \frac{2P_{C@max}}{V_{sup}} = \frac{2 \cdot 12.6}{28} \approx \mathbf{0.897\ A}$;
3. Optimal load impedances of the control and balanced amplifiers, using (2.13):
   $R_{C,opt} = \frac{V_{sup}^2}{2P_{C@max}} = \frac{28^2}{2 \cdot 12.6} \approx 31.2\ \Omega$;
   $R_{B,opt} = \frac{V_{sup}^2}{2P_{B@max}} = \frac{28^2}{2 \cdot 18.7} \approx 20.9\ \Omega$.
4. Transformer turn ratio for the control amplifier:
   $T_C = \sqrt{R_{C,opt}/Z_0} = \sqrt{31.2/50} \approx \mathbf{0.79}$.
   Note that practical lumped transformers have a lot worse performance than ideal representation. Thus, in practice, it is better to implement them as multi-section λ/4 transformers that can offer a higher bandwidth with an increasing number of sections.
5. Current after transformer which is connected to CA:
   $I_{CAT@max} = I_{C@max} \cdot T_C = 0.9 \cdot 0.79 \approx 0.711\ A$;
6. The effective impedance at the inputs of the hybrid (assume that we chose, for example, 50 Ω off the shelf hybrid), using (4.25):
   $Z_{BA@max} = \frac{1}{4} \cdot \left(\frac{Z_0 I_{CAT@max}}{\sqrt{P_{B@max}}} + \sqrt{\frac{Z_0^2 I_{CAT@max}^2}{P_{B@max}} + 4Z_0} \right)^2$;
   $Z_{BA@max} = \frac{1}{4} \cdot \left(\frac{50 \cdot 0.711}{\sqrt{18.7}} + \sqrt{\frac{50^2 \cdot 0.711^2}{18.7} + 4 \cdot 50} \right)^2 \approx 151\ \Omega$.
7. Transformer turn ratio for balanced amplifiers:
   $T_B = \sqrt{R_{B,opt}/Z_{BA@max}} = \sqrt{20.9/151} \approx \mathbf{0.373}$.
8. Output power back-off voltage, using (3.4) and (3.6):
   $V_{PBO} = V_{in@max} \cdot 10^{-k,dB/20} = 1 \cdot 10^{-6/20} \approx \mathbf{0.5\ V}$.
   Thus, the BA should be enabled when input voltage reaches 0.5 V.

It is essential to realize that the effective port impedances seen by the peak amplifiers are not equal to the hybrid design port impedances.

This example is the simplest case, but it has significant disadvantages. First of all, the impedance transformers would take additional area and contribute to distortion and bandwidth limitation. Furthermore, in this case, only a tiny amount of transistor parasitics can be absorbed. Thus, improved design methods are needed to avoid the need for intermediate impedance matching networks.

4.3.2. Using Asymmetrical Custom Hybrid

This variant is very similar to the previous one except that the optimum PA impedances are selected to match the effective hybrid port impedances. Alternatively, a custom hybrid can be designed. Effective characteristic impedances of its ports have to be equal to optimum impedances of all amplifiers. Since the CA and BA have different optimum load impedances, such hybrid would be asymmetrical. Then the intermediate impedance matching networks are not required. See Figure 4.8. This approach represents the current state of the art [12]. A design described in [12] uses off-the-shelf coupler IPP-2281IT, which has two ports with 25 Ω and two with 50 Ω impedances. Amplifiers are designed so that their optimal load impedances would be equal to the hybrid effective port impedances.

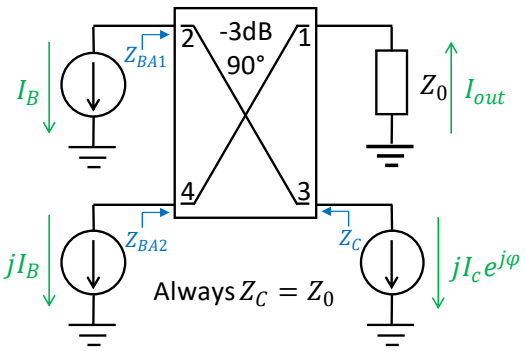


Figure 4.8. PD-LMBA without matching network. The coupler can be symmetrical or asymmetrical (see text).

The design procedure of such an example is very similar to the previous case except that there is no impedance transformation:

Steps 1-3 are precisely the same as in the previous case.

4. The impedance of the hybrid ports 1 and 3 should be equal to the optimal load impedance of the main amplifier to avoid a transformer, i.e.:
$$Z_0 = Z_1 = Z_3 = R_{C,opt}.$$
5. Z_0 characteristic impedance is **not** equal to actual port impedance, which is calculated as follow, using (4.31):
$$Z_2 = Z_4 = \frac{1}{4}\cdot\left(\sqrt{\frac{2R_{C,opt}I_{C@max}^2}{I_{B@max}^2} + 4R_{B,opt}} - \sqrt{2R_{C,opt}}\cdot\frac{I_{C@max}}{I_{B@max}}\right)^2;$$
$$Z_2 = Z_4 = \frac{1}{4}\cdot\left(\sqrt{\frac{2\cdot 31.2\cdot 0.897^2}{1.34^2} + 4\cdot 20.9} - \sqrt{2\cdot 31.2}\cdot\frac{0.897}{1.34}\right)^2 \approx \mathbf{6.93\ \Omega}.$$
Thus, a custom hybrid has to be designed. Its ports 1, 3 should have **31.2 Ω,** and its ports 2, 4 should have **6.93 Ω** design impedance.
6. This step is identical to the last step of the previous case.

The problem is that it is challenging to design an asymmetrical hybrid. There is no straightforward design procedure described in the literature.

4.3.3. Using Custom Symmetrical Hybrid

In this work, it has been noticed that if the supply voltage of the control amplifier (CA) is decreased, at some level again, a symmetrical hybrid can be used while the use of intermediate impedance matching networks can still be avoided (Figure 4.8). This design procedure is very similar to the previous case. However, in this case, the supply voltage for the main amplifier needs to be calculated while keeping his power contribution the same. The design sequence is as follows:

1. This step is the same as in the first example (4.3.1).
2. Currents which have to be provided by the balanced amplifiers (BAs), using (2.7):
$I_{B@max} = \frac{2P_{B@max}}{V_{sup}} = \frac{2\cdot 18.7}{28} \approx \mathbf{1.34\ A}$;
3. Optimal load impedance of each BA, using (2.13):
$R_{B,opt} = \frac{V_{sup}^2}{2P_{B@max}} = \frac{28^2}{2\cdot 18.7} \approx 20.9\ \Omega.$
4. Supply voltage for the control amplifier (**28 V** power supply voltage is used for the BAs):
$$V_{C,sup} = P_{C@max}\sqrt{2}\left(\sqrt{\frac{1}{I_{B@max}^2} + \frac{R_{B,opt}}{P_{C@max}}} - \frac{1}{I_{B@max}}\right) = 12.6\cdot\sqrt{2}\left(\sqrt{\frac{1}{1.34^2} + \frac{20.9}{12.6}} - \frac{1}{1.34}\right) = \mathbf{13.2\ V}.$$
5. Current which has to be provided by the control amplifier (CA):
$I_{C@max} = \frac{2P_{C@max}}{V_{sup}} = \frac{2\cdot 12.6}{13.2} \approx \mathbf{1.9\ A}$;
6. Hybrid's each port characteristic impedance (it is equal to the optimal load impedance of the CA, so again using (2.13)):
$Z_0 = R_{C,opt} = \frac{V_{sup}^2}{2P_{C@max}} = \frac{13.2^2}{2\cdot 12.6} \approx \mathbf{6.94\ \Omega}$;

Since this method is not yet reported in the literature, is relatively easy to design, and seems promising, we will focus on this approach. Thus, transconductances of transistors can be calculated using (2.18) and (2.20). Class B operation has been selected:

$$g_{m,CA} = \frac{2I_{C@max}}{V_{in@max}} = \frac{2\cdot 1.9}{1} = \mathbf{3.8\ S};$$

$$g_{m,BA} = \frac{2I_{B@max}}{V_{in@max}} = \frac{2\cdot 1.34}{1} = \mathbf{2.68\ S}.$$

After replacing current sources in this PD-LMBA circuit (see Figure 4.8) with transistors, we get the schematics shown in Figure 4.9. Output parasitic capacitances can be calculated using (2.21) and (2.22). When LDMOS LM8 technology is used, values for the BA have been calculated in the design example 2.3, and for the CA they can be calculated as follows:

$$W_g = I_{max}/I_{D,max/mm} = 3.8/0.15 \approx 25.3\ mm;$$

$$C_{DS} = W_g \cdot C_{DS/mm} = 25.3 \cdot 0.313 \approx \mathbf{7.92\ pF}.$$

This value is quite big, so it can limit the bandwidth significantly. It is known that while LDMOS LM8 can achieve 1.05 W/mm[10] at 28 V, LDMOS GEN9 can achieve 1.5 W/mm at 28 V. These values can be scaled to 0.495 W/mm and 0.707 W/mm for 13.2 V, respectively, according (2.7). Thus, if LM8 is replaced with GEN9, C_{DS} decreases to:

$$C_{DS,GEN9} = C_{DS} \cdot \frac{0.707}{0.495} \approx \mathbf{5.6\ pF}.$$

However, calculations before doing simulations were performed with lower precision, so 5.333 pF has been used instead of 5.6 pF.

Implementation in GaN25 technology has also been considered. According to the datasheet [33], this transistor can have 0.615 pF/mm drain parasitic capacitance near its linear region. Despite that this value is higher than for LDMOS LM8, which has 0.297 pF/mm, the output capacitance of GaN is quite non-linear, and it changes more than a factor of two over its operating range. Moreover, a 4 times higher current density can be used. Thus, it is safe to assume that effective parasitic capacitances can be approximately four times smaller when GaN technology is used than LDMOS. The power supply voltage is 50 V for GaN. So, the parasitic output capacitances have been set to 0.9375 pF and 1.40625 pF for the CA and BAs, respectively.

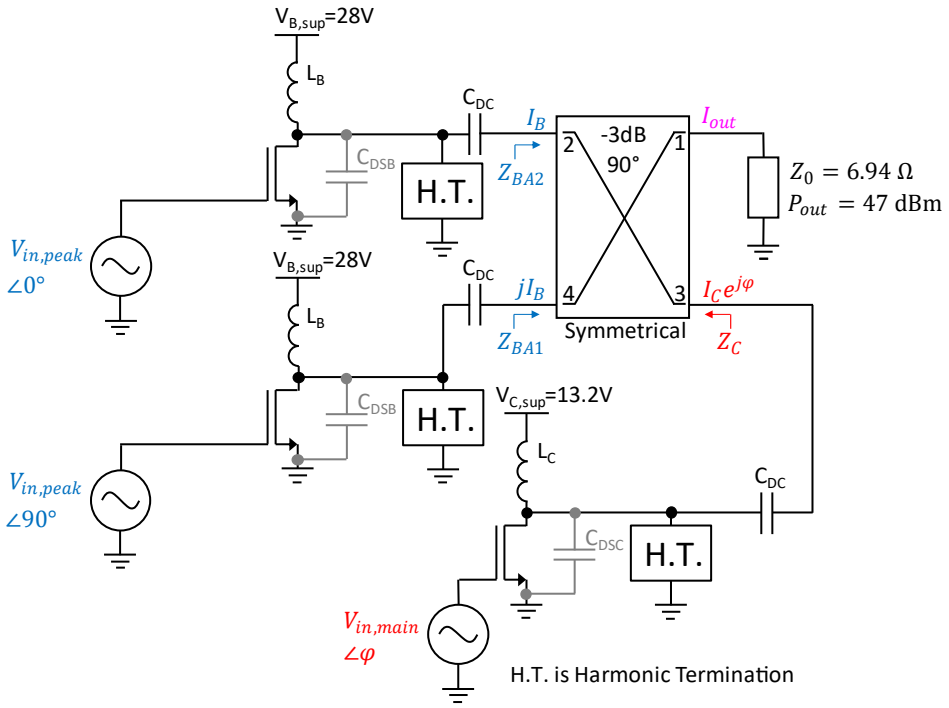


Figure 4.9. PD-LMBA with symmetrical coupler and lowered power supply voltage for CA.

4.3.4. Ideal Hybrid Implementation

This section describes how single-section and multi-section coupled lines, and branch-line couplers can be constructed using ideal transmission lines. Attempts to replace the outer sections with lumped equivalents for parasitics absorption have been made. S-parameter SPICE simulations have been performed, and couplers were compared. As calculated in the previous section, the required characteristic impedance Z_0 of a hybrid port is 6.94 Ω.

[10] Power per unit gate width can be calculated from I_{DS} per unit gate width at chosen V_{DS} using (2.7) and (2.17).

4.3.4.1. Coupled Lines

When two transmission lines are unshielded and near each other, power can couple from one transmission line to the other due to the interaction of electromagnetic fields. Such transmission lines are called *coupled transmission lines*. They usually consist of three conductors in close proximity, though more conductors can be used. They are assumed to operate in transverse electromagnetic (TEM) mode despite such assumption is not very accurate. TEM means that electric and magnetic field vectors are perpendicular (i.e., transverse) to the radiation's propagation direction. Coupled transmission lines can support two distinct propagating modes (odd and even), and this feature can be used to implement many directional couplers, hybrids, and filters [34]. Coupled lines can be composed out of a single section or multi-sections. More sections allow obtaining higher bandwidth, making the physical implementation larger and likely lossier. Each section can be characterized by its odd and even characteristics impedances (Z_o and Z_e respectively), electrical length, and frequency.

A single section coupled lines are presented in Figure 4.10a. Their characteristic impedances can be calculated using the following equations:

$$Z_{o1} = Z_0 \sqrt{\frac{1-c}{1+c}}; \tag{4.34}$$

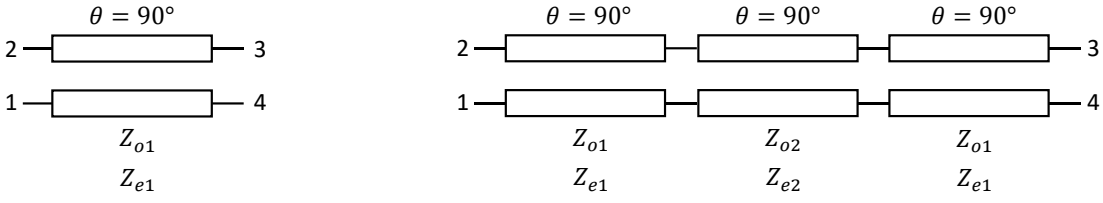
$$Z_{e1} = Z_0 \sqrt{\frac{1+c}{1-c}} \tag{4.35}$$

where Z_0 is each port characteristic impedance, c is coupling coefficient which has to be calculated from loss which is usually specified in decibels. It can be calculated using the equation below:

$$c = 10^{-loss\_dB/20}. \tag{4.36}$$

We first consider couplers with no additional losses for this work, so half of the input power (i.e., -3 dB) is delivered to each output port. Thus, c should be 0.708. It has been mentioned already that the required characteristic impedance Z_0 of each port is 6.94 Ω. Therefore, by applying (4.34) and (4.35) it has been calculated that Z_{o1} = 2.87 Ω and Z_{e1} = 16.8 Ω.

There are no equations for multi-section coupled lines design. Explanation of multi-section transmission lines operation together with universal design equations has been provided in *Microwave Engineering* by D. Pozar [34]. However, it turned out that while provided equations are useful for theoretical analysis, they are not accurate enough for practical calculations. Nevertheless, design tables with normalized impedance values are provided for three and five-section coupled lines in *RF and Microwave Coupled-Line Circuits* by R. Mongia *et al.* [35]. Values have been given for various bandwidth ripple coefficients δ. Since ripples are unwanted in this design, smallest δ has been chosen ($\delta = 0.05$). Then for five-section coupled lines (Figure 4.10c), normalized even-mode characteristic impedances Z_{1e}, Z_{2e} and Z_{3e} are 1.05972, 1.32624, and 3.81243, respectively [35]. Then the even and odd mode characteristic impedance can be obtained by multiplying and dividing required port impedance (6.94 Ω) by these normalized values, respectively. The same way values can be obtained for three-section coupled lines (Figure 4.10b).



(a) (b)

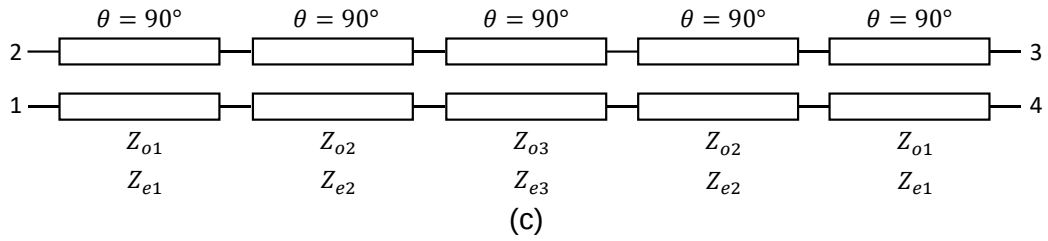


Figure 4.10. Coupled lines. (a) is single section, (b) is three-section, (c) is five-section.

Like conventional transmission lines, coupled lines also can have lumped equivalents [23]. Thus, part of (or complete) outer sections of coupled lines can be replaced with lumped equivalents, see Figure 4.11. Equations from (4.37) to (4.40) can be derived from (3.22) and (3.23). They can be used to find values of lumped components:

$$C_P = \frac{1-\cos\varphi_L}{2\pi f_0 Z_e \sin\varphi_L} \tag{4.37}$$

$$L_S = \frac{Z_e + Z_o}{4\pi f_0} \cdot \sin\varphi_L \tag{4.38}$$

$$C_C = \frac{1-\cos\varphi_L}{4\pi f_0 \sin\varphi_L} \cdot \left(\frac{1}{Z_o} - \frac{1}{Z_e}\right) \tag{4.39}$$

$$M = \frac{Z_e - Z_o}{4\pi f_0} \cdot \sin\varphi_L \tag{4.40}$$

where L_S are inductances and M are mutual inductance of coupled inductors. How much length should be replaced with lumped equivalents can be specified by electrical lengths φ_L and φ_R as shown in Figure 4.13. Transistors are connected to the ports with the port capacitors shown in red so that the parasitic transistor capacitances could be part of them. A lower part of the transistor parasitic output capacitance can be absorbed when only a part of coupled transmission lines is replaced with the lumped equivalents. However, such lumped equivalent approximates transmission lines well only at the center frequency, and it has asymmetrical frequency response, so there is a tradeoff. Optimal φ_L and φ_R values can be found during simulations of complete PD-LMBA. They usually are between 20° and 60°.

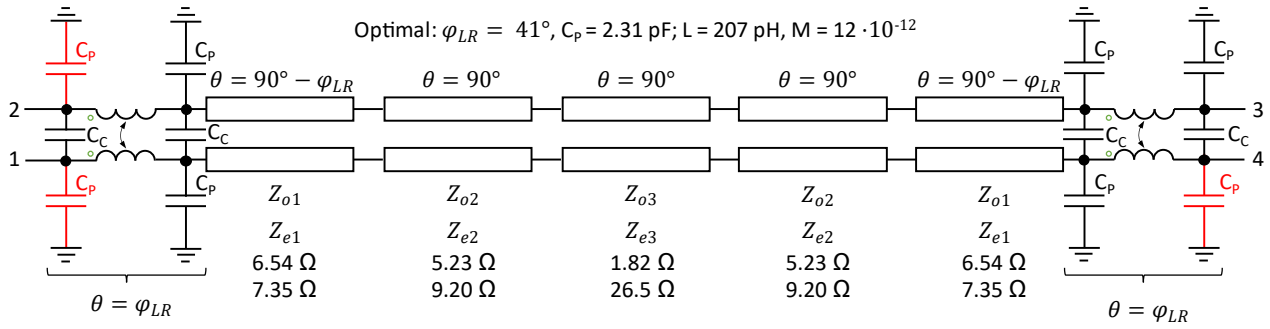


Figure 4.11. Five-section coupled lines with lumped equivalents for parasitics absorption. Values are for 6.94 Ω.

4.3.4.2. Branch Line Coupler

A single section branch line coupler (BLC) together with equations is shown in Figure 4.12a. A signal enters the top left corner of the coupler (port 1). Then if all ports are matched, it is split into two quadrature signals on the right (ports 2 and 3). They have equal magnitudes (-3 dB), but their phases are different by 90°. Port 4 is completely isolated from the input port at the center frequency. Thus, no power is coupled to port 4. The lower output port (port 3) has the most negative transmission phase (delay) since that port is farthest from the input. S-parameter matrix of branch line couplers is shown in (4.41) [36, 34].

$$[S] = -\frac{1}{\sqrt{2}}\begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix} \tag{4.41}$$

A two-section BLC is shown in Figure 4.12b. It works similarly to a single section BLC; however, its bandwidth is higher. Characteristic impedances of its transmission lines can be calculated using equations (4.43), (4.43), and (4.44) [36]. It has been calculated that for two-section BLC Z_1 = 6.94 Ω, Z_2 = 16.8 Ω, and Z_3 = 9.81 Ω. The outer transmission lines can be replaced with their lumped equivalents, see Figure 4.13. Then the outer capacitors of the lumped equivalents could be used to absorb these parasitics capacitors and are shown in red color. Transmission line replacement to the lumped equivalents can be done by applying equations (3.22) and (3.23). Like in CL case, how much length should be replaced with lumped equivalents can be specified by electrical lengths φ_L and φ_R, as shown in Figure 4.13. Optimal values can be found during simulations of complete PD-LMBA. Usually, both these values are around 45°. This could be used to absorb at least part of parasitic transistor capacitances, which should contribute to the capacitance of capacitors shown in red.

Five sections branch line coupler has also been checked, but it had poor port isolation, and there is a lack of literature on how to design it right.

$$Z_1 = Z_0 \tag{4.42}$$

$$Z_2 = \left(1+\sqrt{2}\right)Z_0 \tag{4.43}$$

$$Z_3 = \sqrt{2}Z_0 \tag{4.44}$$

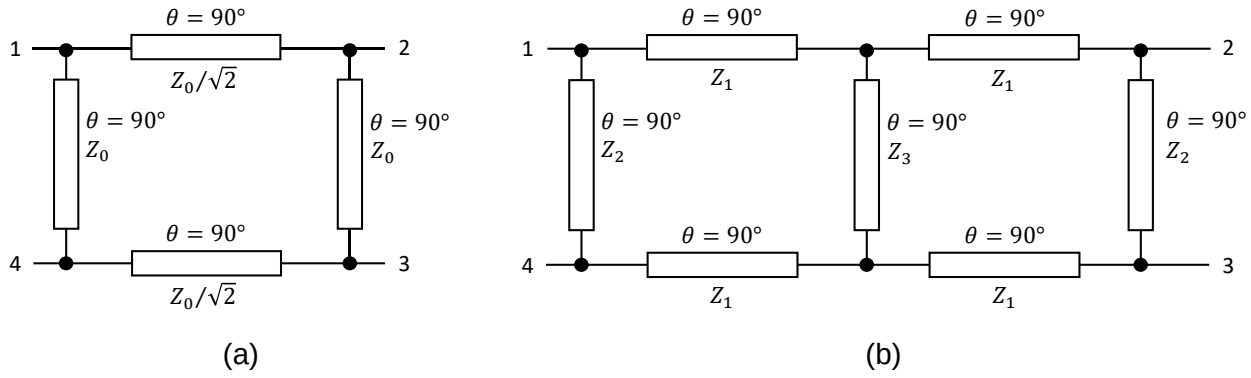


Figure 4.12. Branch line couplers. (a) is a single section, (b) is two-section.

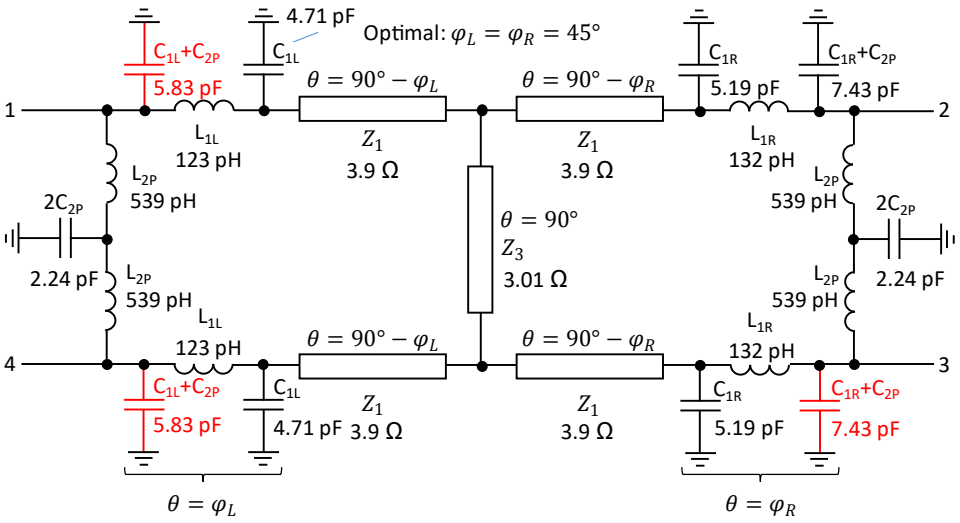


Figure 4.13. Two-section branch line coupler with lumped equivalents for parasitics absorption. Values are for 6.94 Ω.

The good thing about the branch line coupler is that its lumped parts need bigger capacitors than coupled lines. Thus, a more significant amount of parasitic transistor capacitance can be reused, so less need to be compensated. However, in general, branch line couplers are less wideband than coupled lines.

4.3.5. Delay Compensation

Transmission lines, hybrids, parasitics, and other non-idealities introduce frequency-dependent delays, which must be compensated for to get the highest efficiency and power bandwidth. Optimal phase offset function $\phi(f)$ can be introduced for that compensation. Fortunately, this function is almost linearly proportional to frequency in a negative slope [12]. Thus, it can be written as

$$\phi(f) = -Y(f - f_0) \tag{4.45}$$

where f_0 is the center frequency, f is the frequency of the tone of interest. Variable Y has been introduced so that the slope can be adjusted. Figure 4.15 shows how it can be used in the PD-LMBA circuit. It is expected that this delay can be compensated in the digital domain. Such digital delay compensation intellectual property is claimed by TU Delft, most likely also applicable to other wideband DPAs. In the analog domain (4.19), it can be implemented using a wideband phase shifter which actually is just a transmission line. It should be connected between the output of the power divider and LMBA, see Figure 4.1.

Variable Y for digital implementation or electrical length of the phase shifter transmission line for analog implementation should be set by following these steps:

1. Set simulation frequency higher or lower than the design frequency, for example, by ±100 MHz;
2. Plot phase distortion. It should look similar to Figure 4.14a;
3. Adjust variable Y (or phase shifter electrical length) until phase distortion becomes (almost) constant for all V_{in} values like in Figure 4.14b.

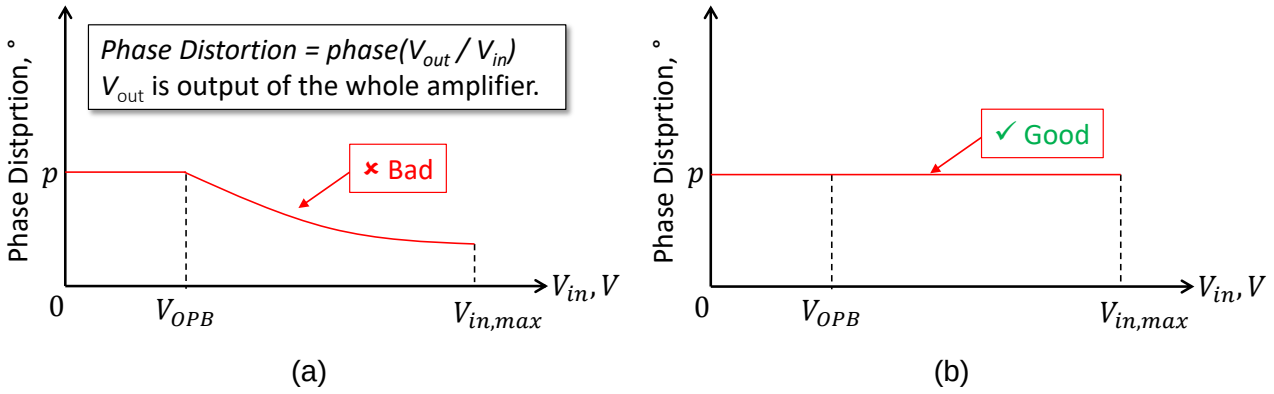


Figure 4.14. Phase distortion for off-center frequency. (a) when delay compensation is not present or incorrect, (b) when it is configured correctly.

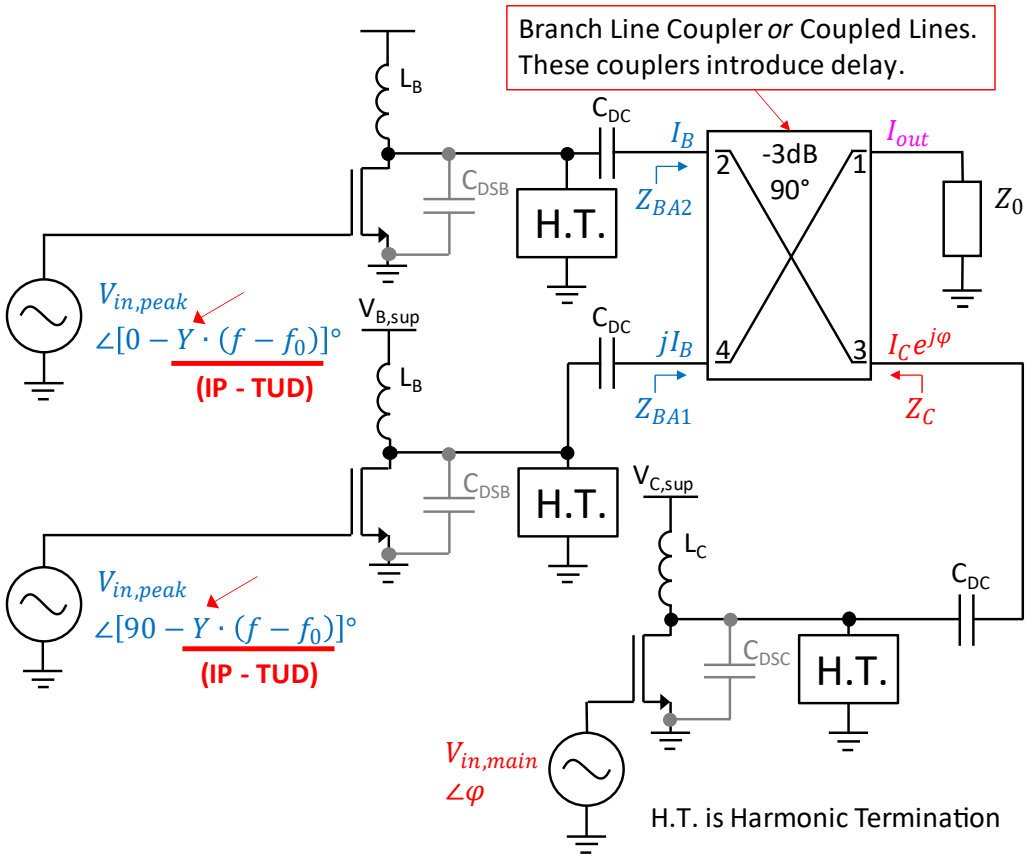


Figure 4.15. Delay compensation in the PD-LMBA circuit.

4.4. Development of Universal Simulation Test Bench

It is helpful to have a simulation workbench in which one can change the specifications, and all required values are calculated automatically. Such a workbench gives a quick starting point for those who are not yet familiar with the operation of this topology. First of all, a completely ideal circuit from Figure 4.4a has been entered into “Keysight ADS” schematics editor, see Figure 4.16. Then equations have been entered. These equations have been discussed already. Note that both equations (4.31) and (4.33) have been inserted as well. Equation (4.31) is essential when an asymmetrical hybrid is used, and (4.33) is necessary when a symmetrical hybrid is used. Thus, this test bench can be used to research both cases. The circuit from Figure 4.16 can be used when the variant with the symmetrical coupler and lower supply voltage for the CA must be investigated (the circuit has been described in section 4.3.3). The following variables can be adjusted in case to change specifications:

- supply voltage of the peak amplifier (`Pout_max`);
- maximum power in watts (`Vsup_peak`);
- output power back-off (`OPB`).

The testing workbench can calculate the following:

- the currents of the main and peak amplifiers;
- output current;
- impedances seen by the control (main) and balanced (the peak) amplifiers.

If one wants to investigate the behavior with the asymmetrical coupler (which has been described in section 4.3.2), they have to delete an equation for `Vsup_main` and set it to the same voltage as for the BA, i.e., `Vsup_peak`. Then `Z1hybrid` is calculated automatically. “Z4P_Eqn” component acts as a hybrid. Z-parameters of coupled lines have been entered; however, for the branch-line coupler,

only signs of some parameters are different, and that results in different optimum phase φ (`phi`, has to be specified in degrees). Thus, there should be no need to change these parameters.

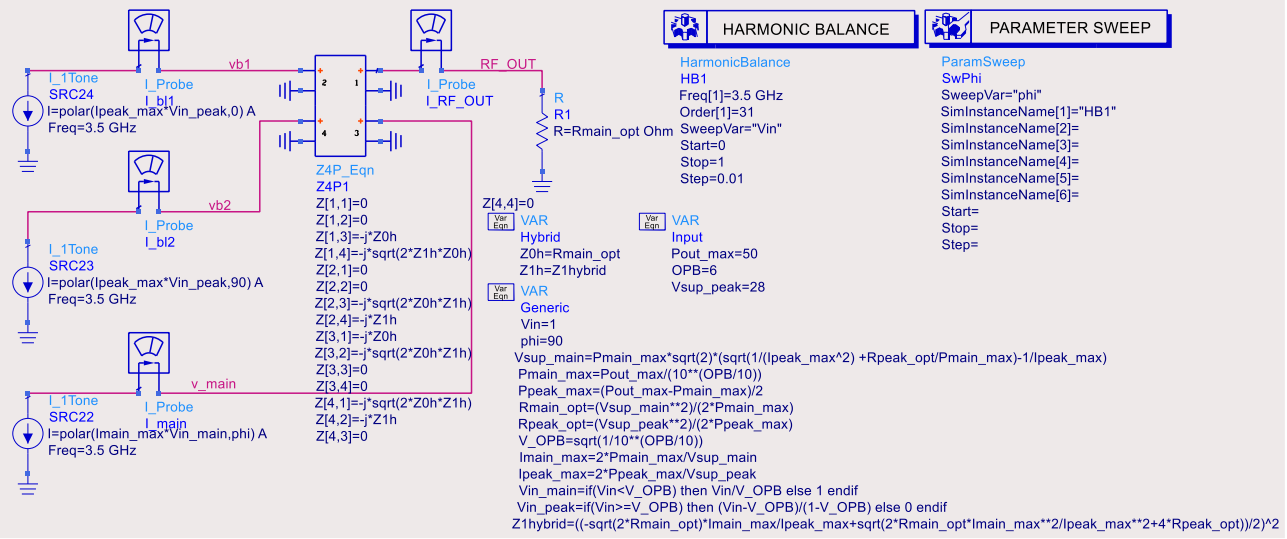


Figure 4.16. Universal simulation test workbench for the most ideal PD LMBA.

The completely ideal workbench is handy when one needs to familiarize with the topology. However, it is not very useful for research because it could not be used for the investigation of the influence of the parasitics and the coupler. Thus, a few other workbenches have been developed. One for 2-section branch-line coupler, another coupled lines: for a single section and 5-section. Performance of the circuit when the single section and 3-section coupled lines are used has similar performance, so 3-section coupled lines have not been investigated further. Single section branch line coupler has a too narrow bandwidth, so that case has also not been studied more.

A complete test bench for PD LMBA with 5-section coupled lines is shown in Figure 4.17. Since individual components of the circuit are not very clearly visible in Figure 4.17, it has been separated into subcircuits shown from Figure 4.18 to Figure 4.21. Figure 4.18 shows equations that are used in the test bench. Most of these expressions match equations that have been shown already in Figure 4.16. In addition, this testbench contains the expressions for calculations of all transistor transconductances (g_m), capacitances that can be absorbed (variables `Cparm_useful` and `Cparp_useful`) and which cannot be absorbed (variables `Cparm_useless` and `Cparp_useless`), values of compensation inductors L_m and L_p. Specifications should be entered into VAR block, which is called “Input.” Like for the ideal PD LMBA test bench, there can only be entered: maximum input voltage, power supply voltage, the maximum output power in watts, and power back-off level (PBO). The test benches, like in Figure 4.17 use a symmetrical hybrid and do not have a matching network. Thus, they are only suitable for analysis of the PD LMBA with symmetrical coupler and decreased voltage for the control amplifier (CA) explained in section 4.3.3 and the schematic diagram shown in Figure 4.9. This is fine as the project focuses on that variant because it has not been researched but seems promising. The VAR block which is called “Parasitics_pF” can be used to enter output parasitic capacitances in picofarads, `Cparm` is for CA and `Cparp` is for BA1 and BA2. Variable `Y` can be used to adjust delay compensation. This has to be done experimentally by following the technique which has been described in section 4.3.5. Variable `phi_L` corresponds to φ_L in Figure 4.11. It is described in section 4.3.4.1. It is convenient to use “Tunning” tool for adjusting `Y` and `phi_L`.

Figure 4.19 shows input signal sources. In practice, there can be connected outputs of DTX (see Figure 4.2) which generates signals with the right driving profile and phases digitally or a single output of analog transmitter via power divider, phase shifter, another coupler, and offset for BAs (e.g., by using BAs in Class C) as it is done in Figure 4.1. Since this work focuses on the output signal, keeping the rest of the circuit as simple and as ideal as possible is essential. This allows to focus on the problem (because the influence of part which is not under research is avoided) and to have quicker simulations. The sources are prepared for single-tone simulations. However, if 2-tone

simulations are needed, e.g., for checking IM3, all three active sources must be disabled, and the other three (2-tone) sources must be enabled.

Figure 4.20 presents the control (CA) and balanced (BA1 and BA2) amplifiers. Remember that the CA works similarly to the main amplifier in conventional DPA topologies while BA1 with BA2 act like the peak amplifier. Note that each parasitic capacitance is separated into two parts: useless and useful. Useful means that it can be reused, i.e., absorbed by the coupler, while the useless part has to be compensated and still contributes to the bandwidth limitation.

Figure 4.21 shows a 5-section coupler that is connected to this test bench. It corresponds to the circuit from Figure 4.11. It has been described in section 4.3.4.1. Inductors in lumped equivalents have to be coupled. Coupling is done with Mutual Inductance components (Mutual1 and Mutual2). Alternatively, a single section coupled lines (Figure 4.22) or 2-section branch line coupler (Figure 4.23) can be used. It has been explained in section 4.3.4.2 (see Figure 4.13), and Figure 4.23 shows it in the schematics editor prepared for simulations.

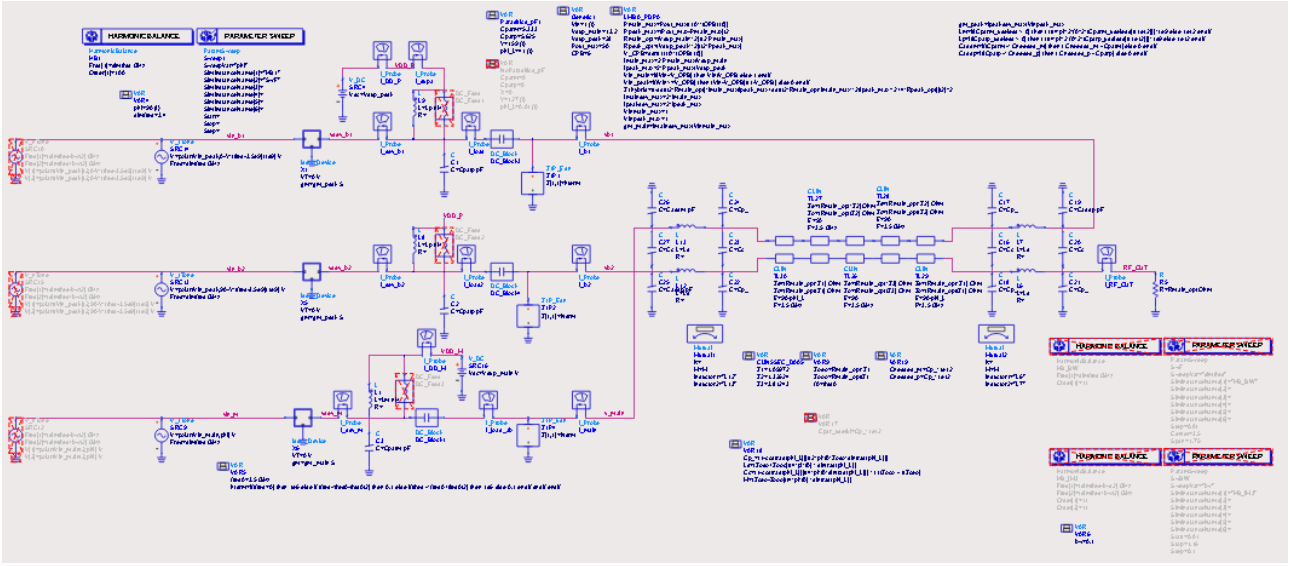


Figure 4.17. Universal test workbench for PD LMBA with 5-section coupled lines.

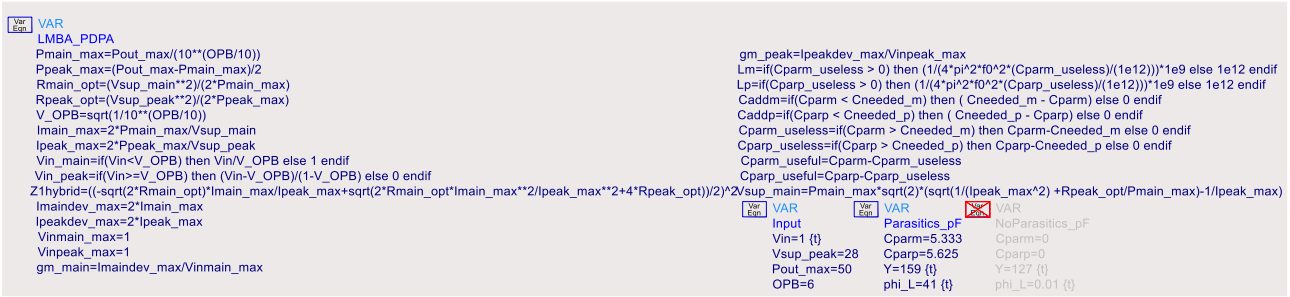


Figure 4.18. Variables and equations of PD LMBA test workbench with 5-section coupled lines.

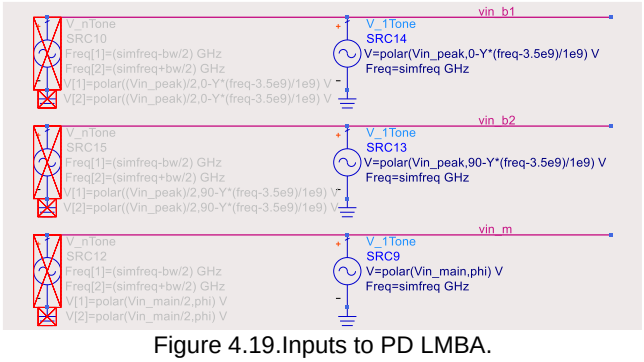


Figure 4.19.Inputs to PD LMBA.

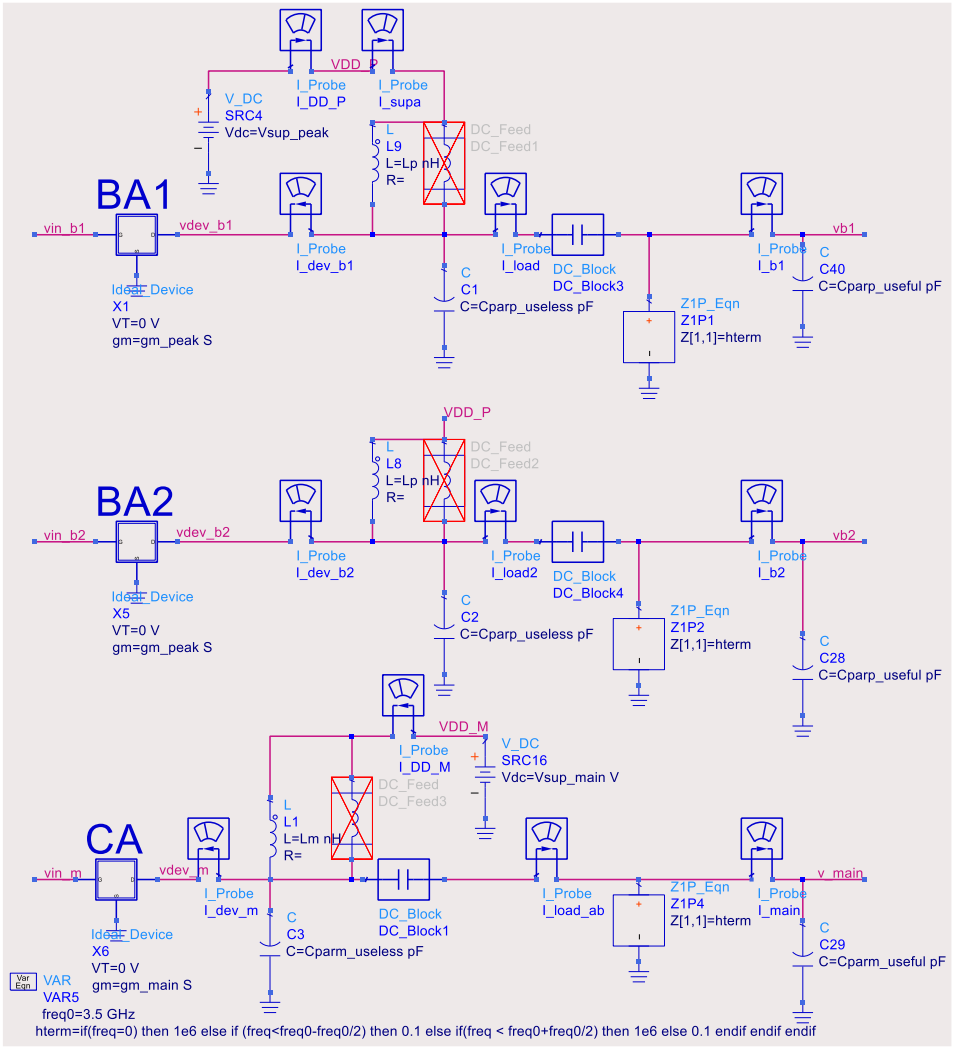


Figure 4.20. Balanced (BA1 and BA2) and control amplifiers of PD LMBA.

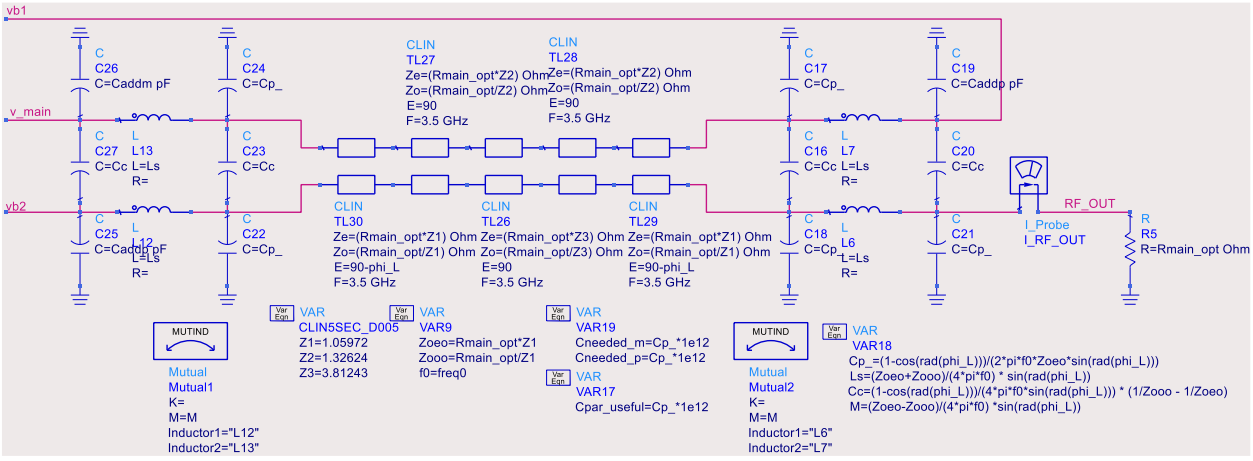


Figure 4.21. 5-section coupled lines inside PD LMBA test workbench

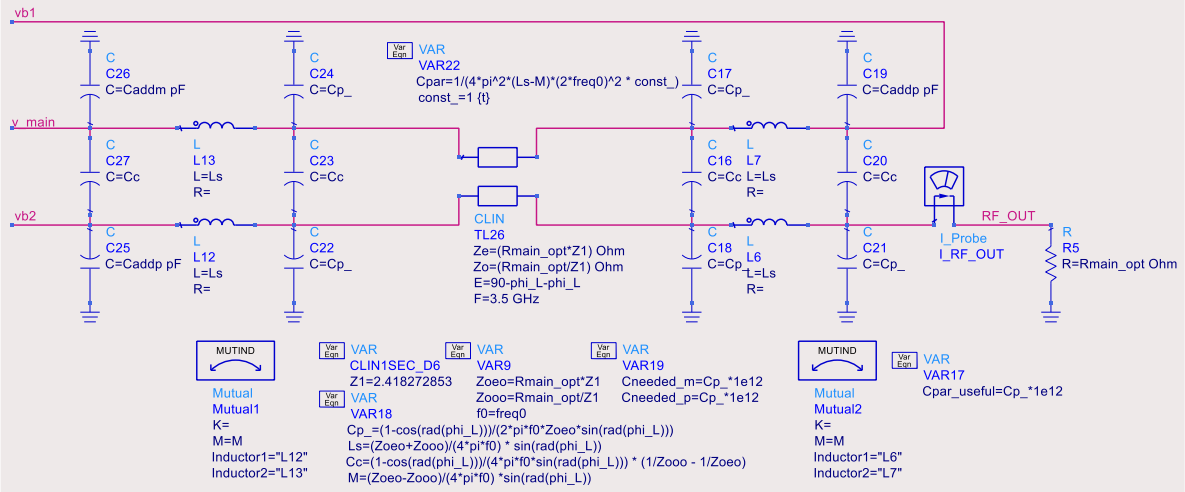


Figure 4.22. 1-section coupled lines inside PD LMBA test workbench

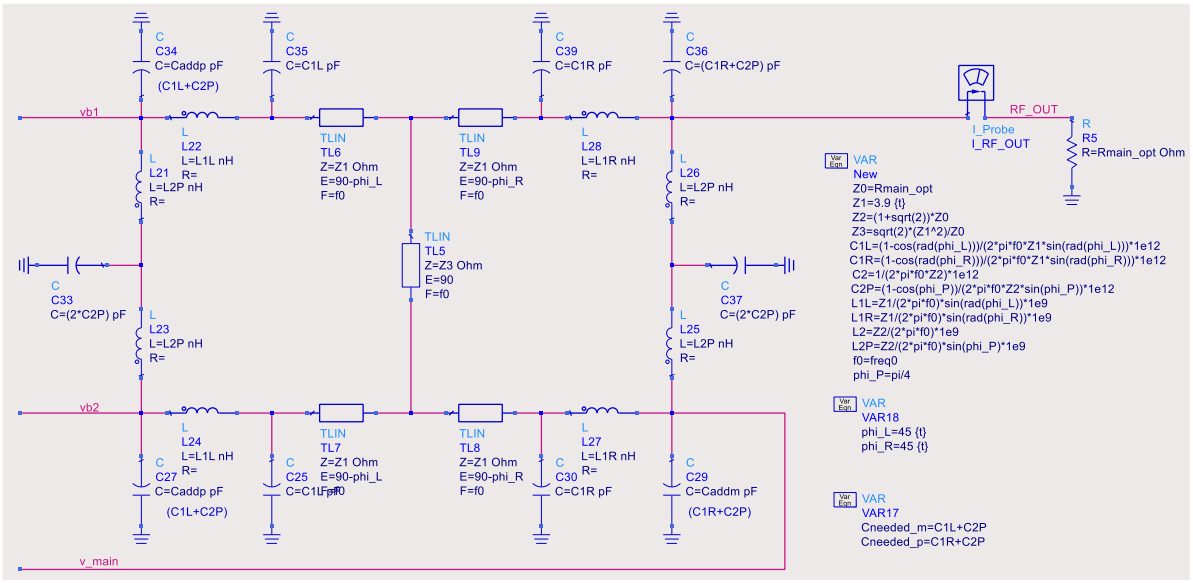


Figure 4.23. 2-section branch line coupler which can be connected to PD LMBA test workbench

4.5. Simulation Results

The specifications that have been introduced in section 3.5 have been selected, and SPICE harmonic balance simulations have been done for implementation in LDMOS and GaN technologies. When DPA topologies were analyzed in the previous chapter, it was assumed that the main and the peak transistor has 1 W/mm power density, while here for the LDMOS case, it is assumed that the transistor of the CA has 1.5 W/mm power density (when V_{DS} is 28 V) which results in lower parasitic capacitance. GaN has a lot higher power density. Thus, to have a fair comparison with DPA, additional simulation has been performed, assuming 1 W/mm power density in all transistors. Figure 4.24a shows dynamic CA and BA load impedances versus the input voltage (V_{in}).

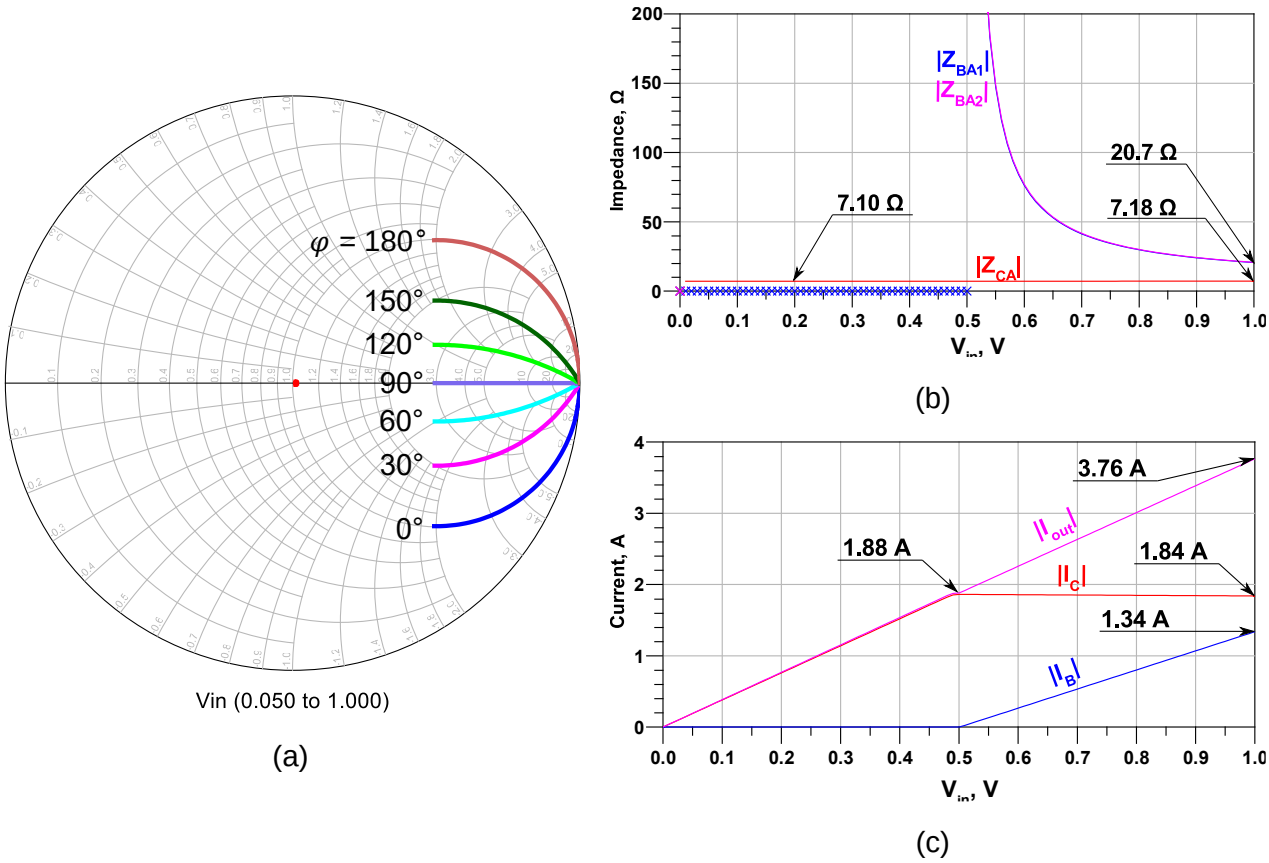


Figure 4.24. Simulation results: (a) Dynamic CA and BA load impedances versus V_{in} and φ, (b) Dynamic CA and BA effective load impedances versus V_{in} when $\varphi = 90°$, (c) currents versus V_{in}.

Table 4.1. Experimentally determined values and absorbed parasitics for different configurations.

Configuration	**Experimentally found**			**Not Absorbed/Total C_{DS}, pF**	
	Y	φ_L, °	φ_R, °	**CA**	**BA**
LDMOS, 1-section CL	74	0		5.33/5.33	5.63/5.63
LDMOS, 5-section CL	159	41		3.02/5.33	3.31/5.63
LDMOS, 2-section BLC	99.6	44	48	0/5.33	0/5.63
GaN, 5-section CL	141	41		0.214/0.938	0.683/1.41
GaN, 2-section BLC	102	20		0.001/0.938	0.469/1.41
LDMOS, CL (for comparison with DPA)	172	41		5.61/7.92	3.31/5.63

First, simulation at the center frequency has been performed while changing the phase to the CA (φ) and the input voltage (V_{in}). This allowed finding the optimum phase. The simulation results are shown in Figure 4.24. It can be seen that the optimum phase is 90° while in Figure 4.6 it is 0°. The coupler causes this, also note that each amplifier also inverts the phase (in other words, it shifts it by 180°). Another difference is higher impedance at maximum V_{in}. Figure 4.24b shows effective impedances seen by the amplifiers. $|Z_{CA}|$ should be completely constant and equal to 6.94 Ω (as calculated in section 4.3.3), but it is higher, and still has a slight dependence on V_{in}. This is because the coupler normalized even and odd impedances have limited precision. Since all plots shown in Figure 4.24 match the theory that has been described at the beginning of this chapter and the drain efficiency plot at the center frequency exactly matches the one for Doherty PA (see Figure 3.23), we can conclude that PD LMBA works correctly. Next, initial bandwidth simulation has been performed for each variation and optimum Y, and φ_R values have been found experimentally and they are shown in Table 4.1. The table also shows how much parasitic capacitance cannot be absorbed. Finally, the rest of

the simulations were performed, and plots shown in figures from Figure 4.31 to Figure 4.57 have been generated.

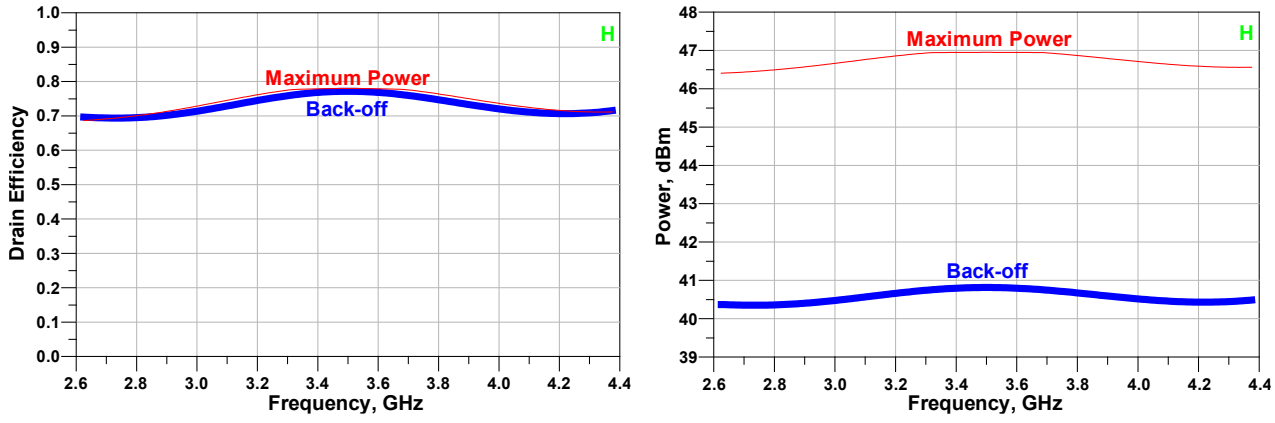
4.5.1. In LDMOS Technology

It has been assumed that the BA transistors have 1 W/mm power density while the CA transistor has 1.5 W/mm (when V_{DS} is 28 V). 5.333 pF and 5.625 pF parasitic capacitances have been chosen for the CA and BAs, respectively. Then simulations have been performed with 5-section coupled lines and alternatively with a 2-section branch-line coupler.

4.5.1.1. With 1-section Coupled Lines

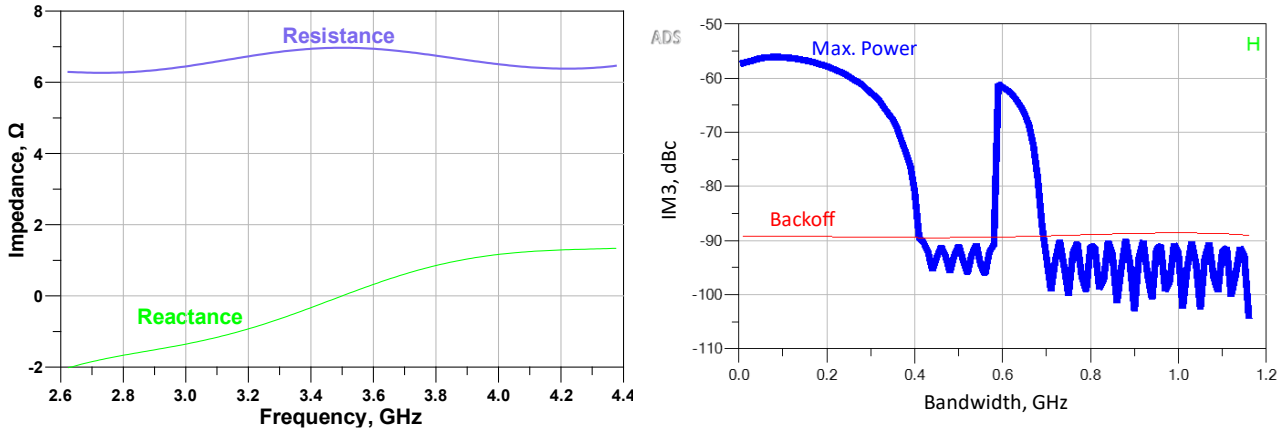
1 dB power bandwidth is over 1.8 GHz at maximum power and at a back-off, as presented in Figure 4.25b. This is a lot higher than the best one of Doherty PAs, which are shown in Figure 3.69a and Figure 3.71a. When the amplifier works at back-off, the impedance seen by the CA does not vary significantly over the frequency range, and the reactive part is small enough, see Figure 4.26a. BAs are disabled and see infinite impedance. The impedance seen by the CA at maximum power (Figure 4.27a) is basically the same as at back-off (Figure 4.26a). However, the impedance seen by the BAs is finite (Figure 4.27b). Imaginary parts are almost zero, and real parts are almost constant in the whole frequency range as they should. AM/AM and phase distortion can be very small. See the plots which are presented in Figure 4.28, Figure 4.29, and Figure 4.30. Results are 100 MHz below the center frequency, at the center frequency (3.5 GHz), and 100 MHz above the center frequency. Y = 74 is the optimum value that has been found by simulations. Y values equal to 20 and 120 are shown to illustrate the expected influence on distortion if this value is set incorrectly. Note that at the center frequency, all curves overlap because here Y does not have any impact, as it can be noticed from equation (4.45). 2-tone test has also been performed, and it generated an IM3 plot introduced in Figure 4.26b.

Although PD-LMBA with a single section coupled lines has shown excellent simulation results, it cannot be used to demonstrate parasitics absorption technique because the negative influence of replacing any part of the coupled lines with lumped equivalents is more significant than bandwidth increase caused by parasitics absorption. The same applies to 3-section CL. However, 5-section CL could be used to demonstrate the parasitic absorption technique. Moreover, that causes an increase of -0.5 dB power bandwidth, see Figure 4.31a.



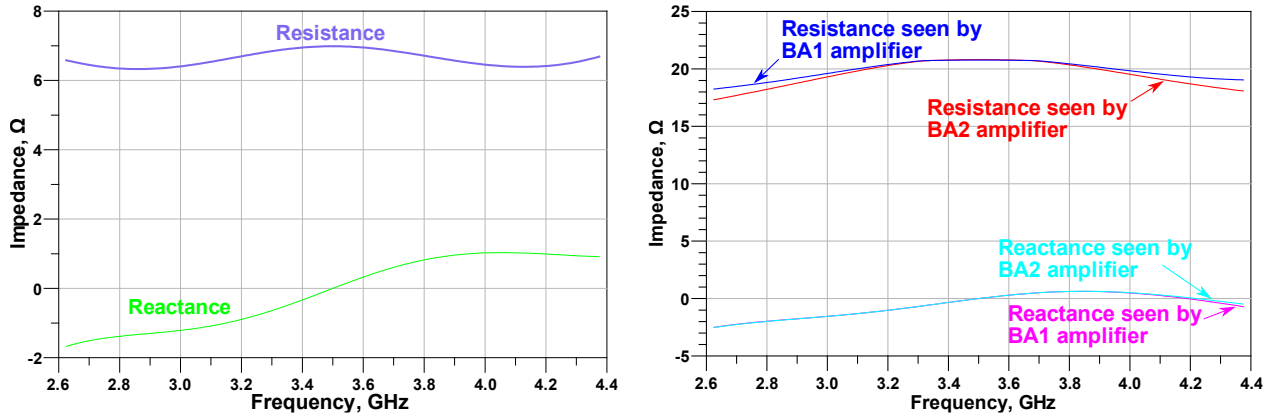
(a) (b)

Figure 4.25. (a) Drain efficiency and (b) power bandwidth when LDMOS tech. and 1-section coupled lines are used.



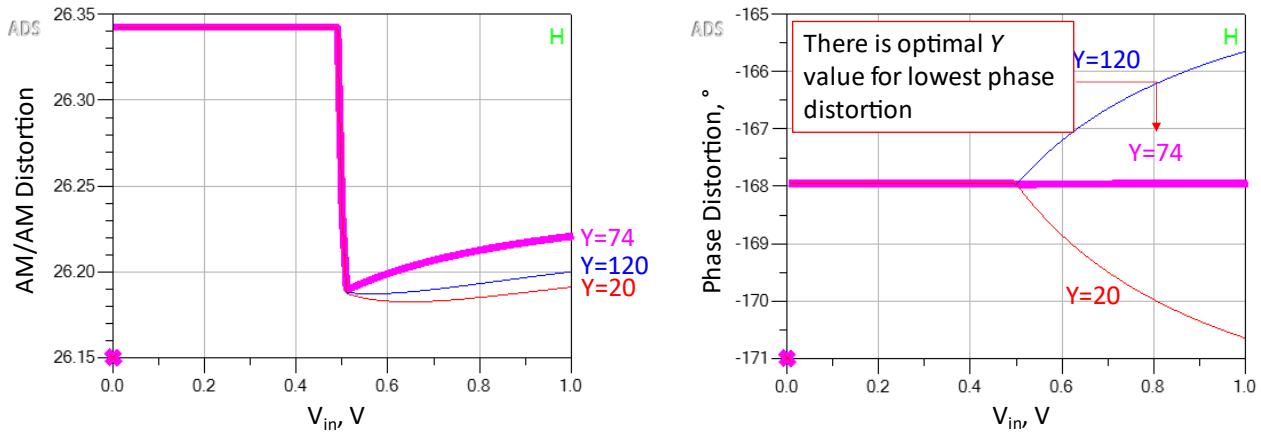
(a) (b)

Figure 4.26. Simulation results when LDMOS tech. and 1-section CL are used: (a) impedance at the back-off ($V_{in} = 0.49\ V$) seen by the CA, (b) IM3.



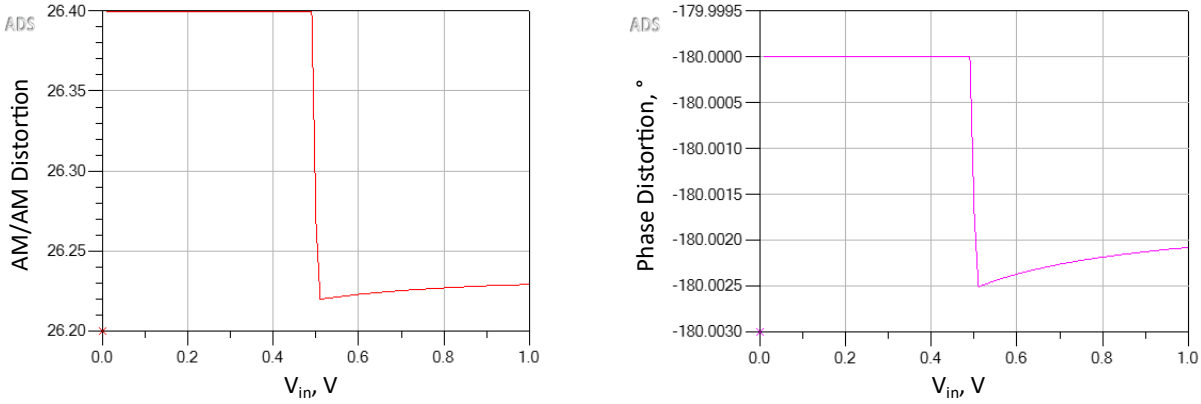
(a) (b)

Figure 4.27. Impedances at max. power ($V_{in} = 1\ V$) when LDMOS tech. and 1-section coupled lines are used. Impedances seen by: (a) the CA, (b) the BA.



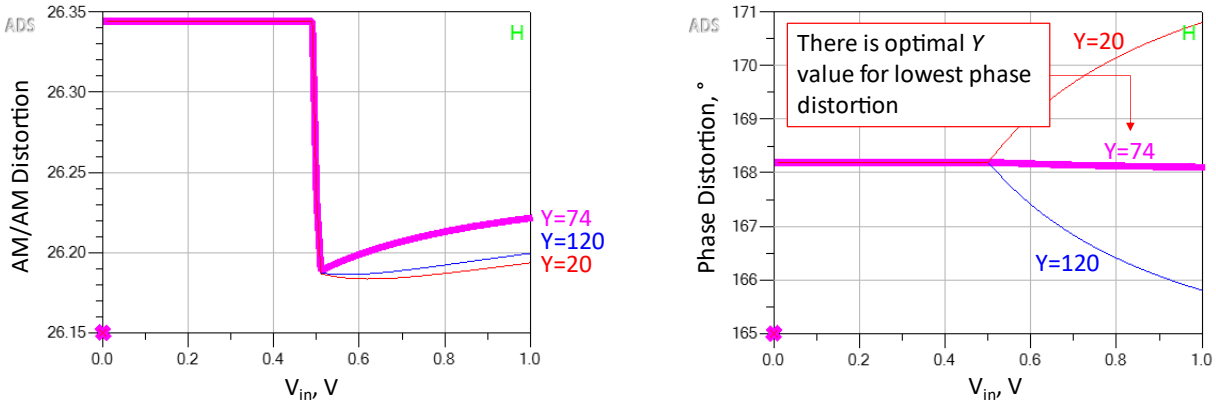
(a) (b)

Figure 4.28. Simulation results when LDMOS technology and 1-section coupled lines are used and the input signal frequency (3.4 GHz) is below the center frequency (3.5 GHz): (a) AM/AM distortion, (b) phase distortion.



(a) (b)

Figure 4.29. Simulation results when LDMOS technology and 1-section coupled lines are used, and the input signal frequency is equal to the center frequency (3.5 GHz): (a) AM/AM distortion, (b) phase distortion.

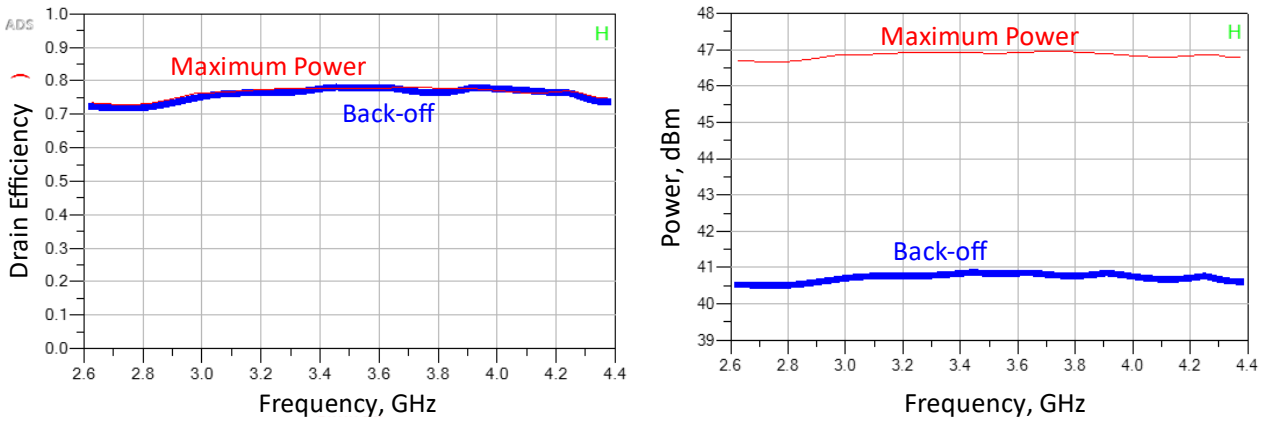


(a) (b)

Figure 4.30. Simulation results when LDMOS technology and 1-section coupled lines are used and the input signal frequency (3.6 GHz) is above the center frequency (3.5 GHz): (a) AM/AM distortion, (b) phase distortion.

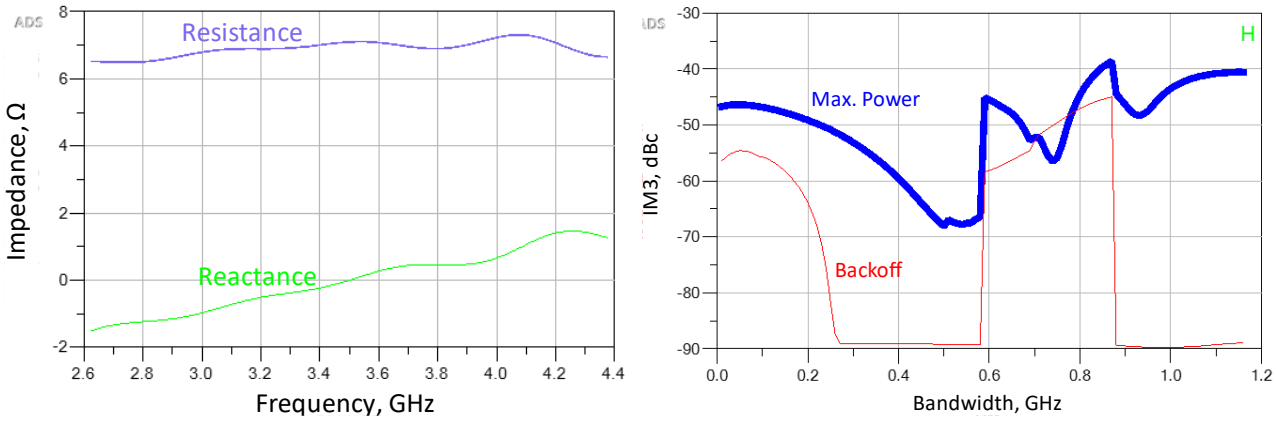
4.5.1.2. With 5-section Coupled Lines

Now, 1-section coupled lines have been replaced with 5-section coupled lines, and the same simulations were performed once more. The results are shown from Figure 4.31 to Figure 4.36 and can be compared with the plots from the previous section. The 1 dB power bandwidth is still over 1.8 GHz at maximum power and at a back-off, as presented in Figure 4.31b. This is similar to 1-section coupled lines. However, -0.5 dB power bandwidth increased (compare Figure 4.31b with Figure 4.25b). Differently than a 1-section coupled line, 5-section can be used to demonstrate parasitic absorption technique.



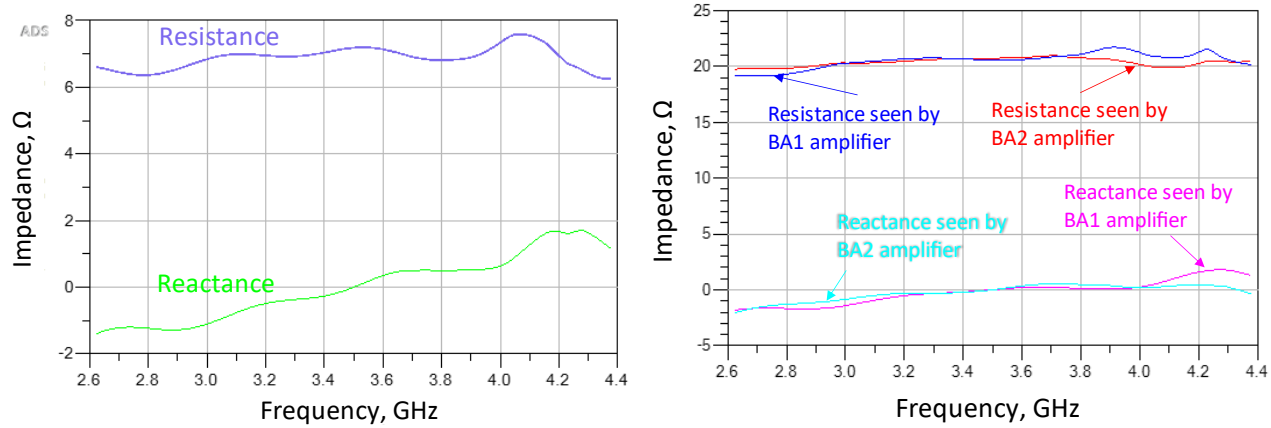
(a) (b)

Figure 4.31. (a) Drain efficiency and (b) power bandwidth when LDMOS tech. and 5-section coupled lines are used.



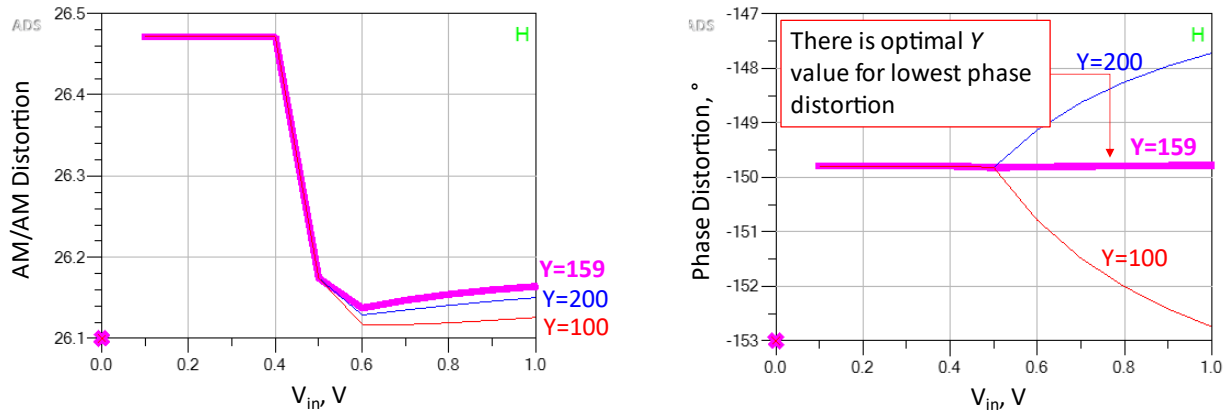
(a) (b)

Figure 4.32. Impedance at back-off ($V_{in} = 0.49\ V$) seen by: (a) the CA when LDMOS tech. and 5-section coupled lines are used, (b) the BA for all tested cases.



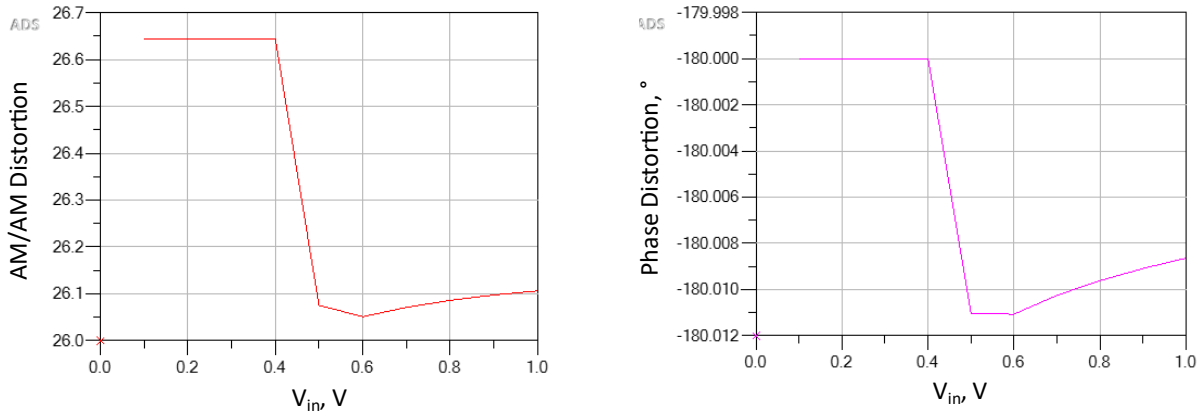
(a) (b)

Figure 4.33. Impedances at max. power ($V_{in} = 1\ V$) when LDMOS tech. and 5-section coupled lines are used. Impedances seen by: (a) the CA, (b) the BA.



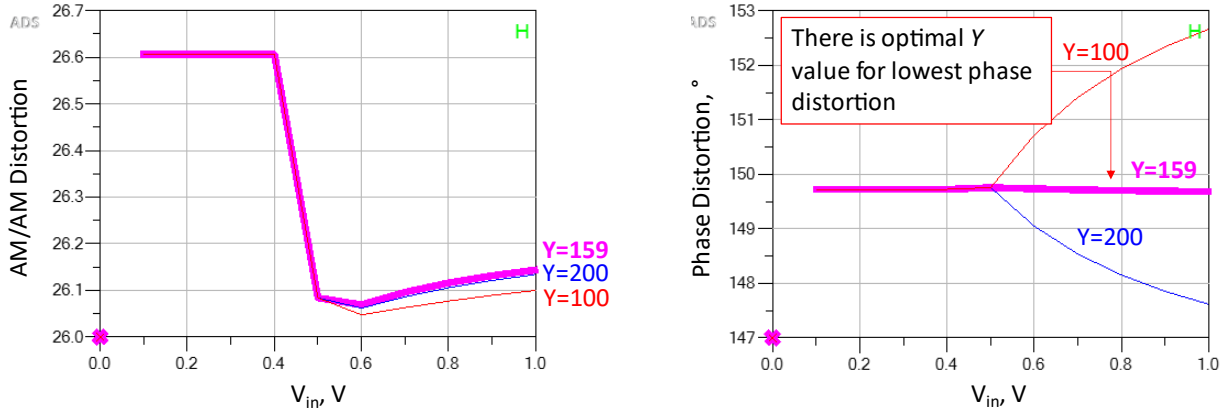
(a) (b)

Figure 4.34. Simulation results when LDMOS technology and 5-section coupled lines are used and the input signal frequency (3.4 GHz) is below the center frequency (3.5 GHz): (a) AM/AM distortion, (b) phase distortion.



(a) (b)

Figure 4.35. Simulation results when LDMOS technology and 5-section coupled lines are used and the input signal frequency is equal to the center frequency (3.5 GHz): (a) AM/AM distortion, (b) phase distortion.



(a) (b)

Figure 4.36. Simulation results when LDMOS technology and 5-section coupled lines are used and the input signal frequency (3.6 GHz) is above the center frequency (3.5 GHz): (a) AM/AM distortion, (b) phase distortion.

4.5.1.3. With 2-section Branch Line Coupler

Now 5-section coupled lines have been replaced with a 2-section branch-line coupler, and the same simulations were performed once more. The results are shown from Figure 4.37 to Figure 4.42 and can be compared with the plots from the previous section. Now 1 dB power bandwidth is over 1.5 GHz at maximum power and 1.3 GHz at a back-off, as presented in Figure 4.37b. This is worse than with coupled lines, where 1 dB bandwidth was over 1.8 GHz even at the back-off.

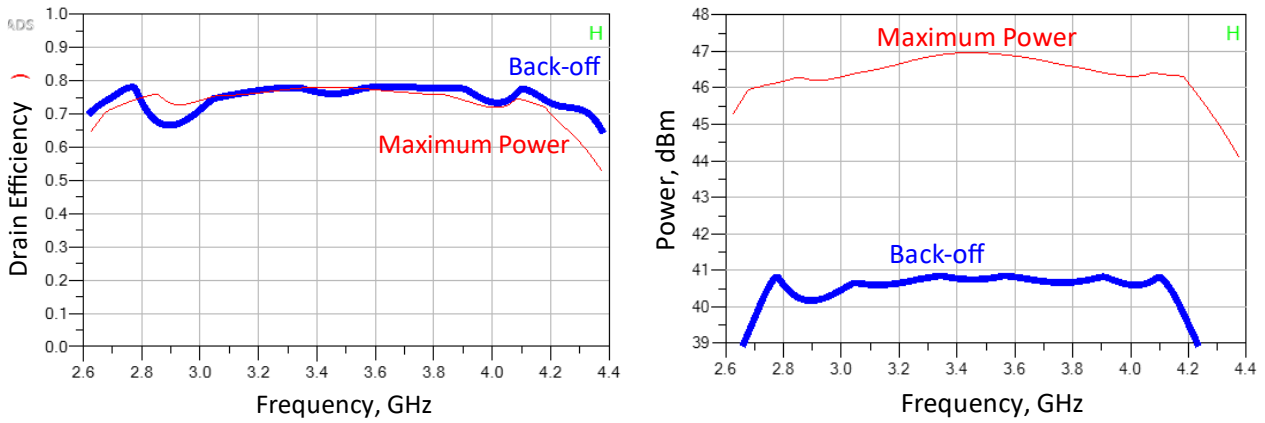


Figure 4.37. (a) Drain efficiency and (b) power bandwidth when LDMOS tech. and 2-section BLC is used.

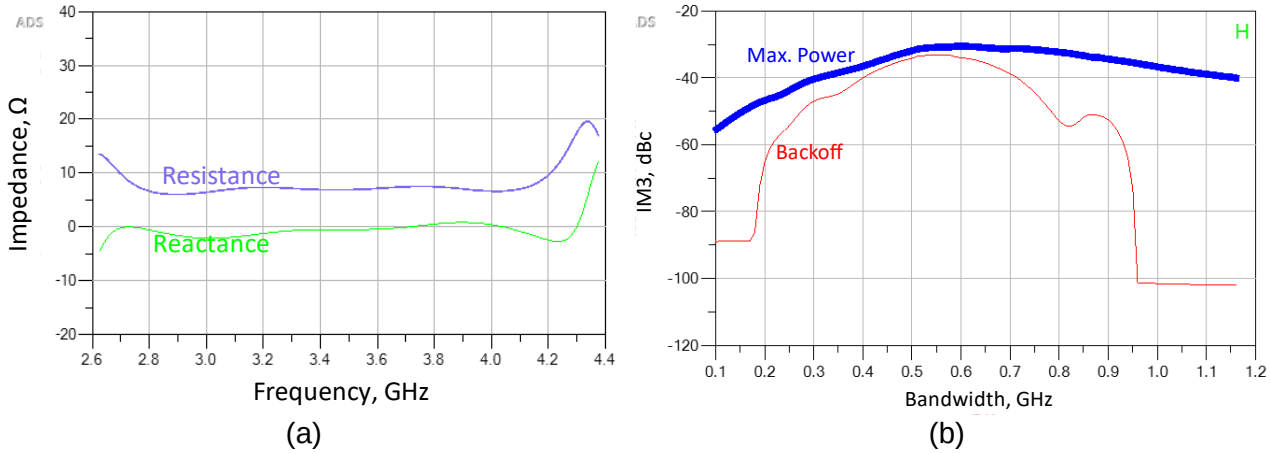


Figure 4.38. Simulation results when LDMOS tech. and 2-section BLC is used: (a) impedance at the back-off ($V_{in} = 0.49\ V$) seen by the CA, (b) IM3.

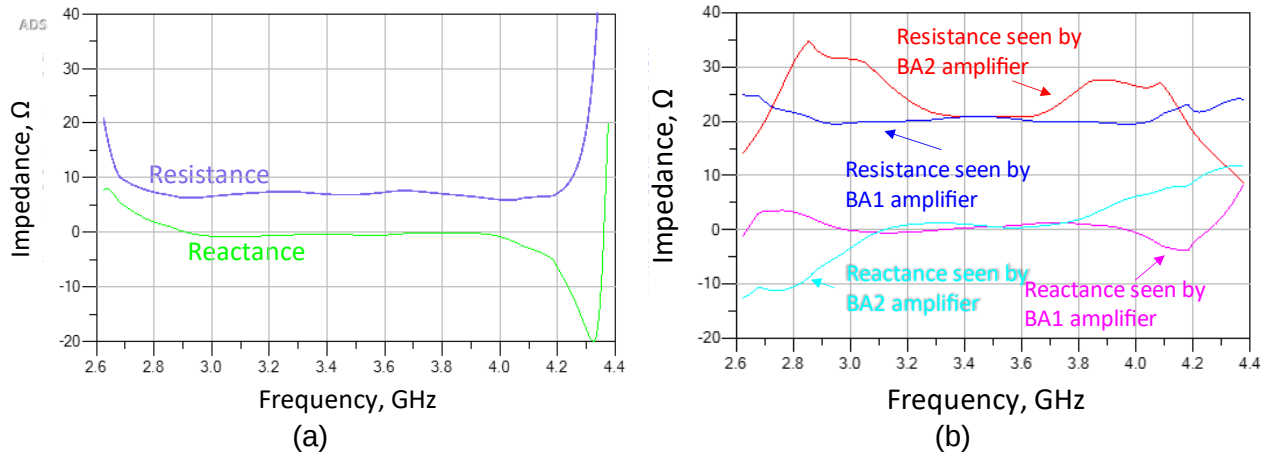


Figure 4.39. Impedances at max. power ($V_{in} = 1\ V$) when LDMOS tech. and 2-section BLC is used. Impedances seen by: (a) the CA, (b) the BA.

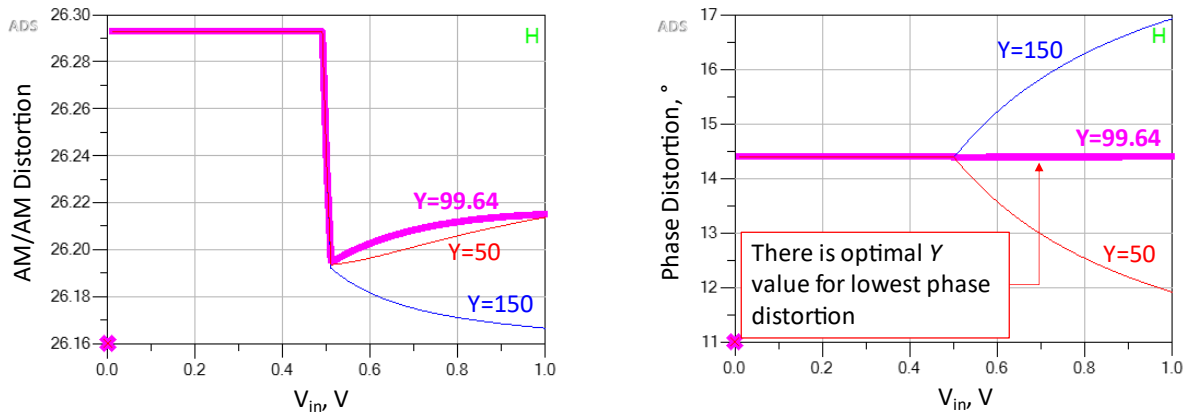


Figure 4.40. Simulation results when LDMOS technology and 2-section BLC are used, and the input signal frequency (3.4 GHz) is below the center frequency (3.5 GHz): (a) AM/AM distortion, (b) phase distortion.

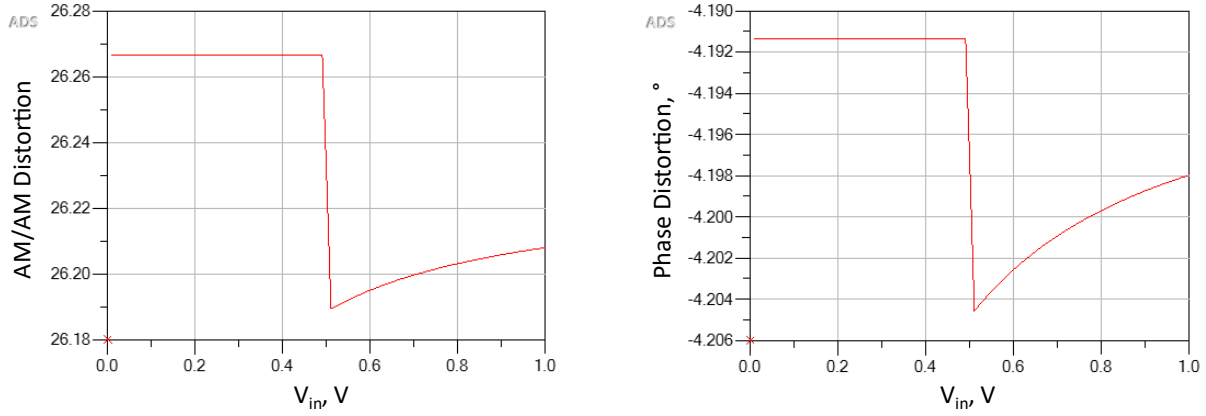


Figure 4.41. Simulation results when LDMOS technology and 2-section BLC is used and the input signal frequency is equal to the center frequency (3.5 GHz): (a) AM/AM distortion, (b) phase distortion.

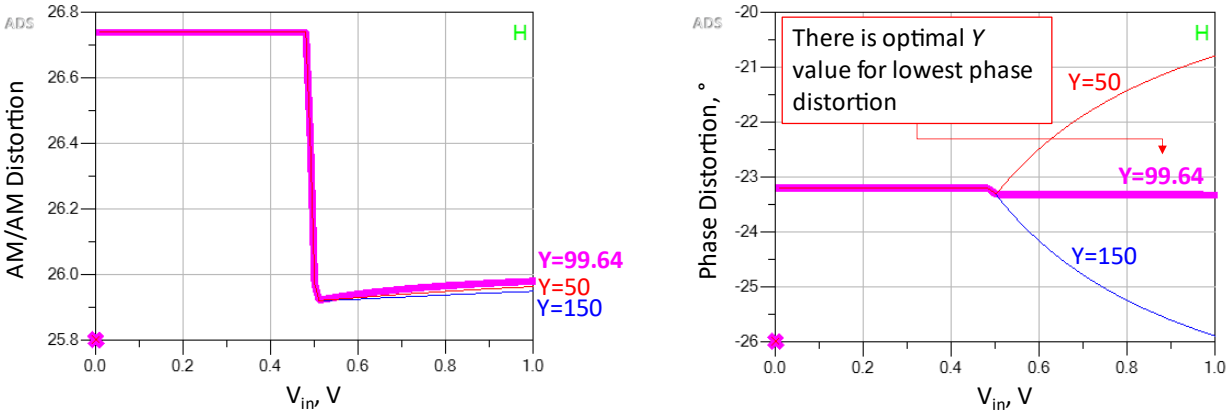


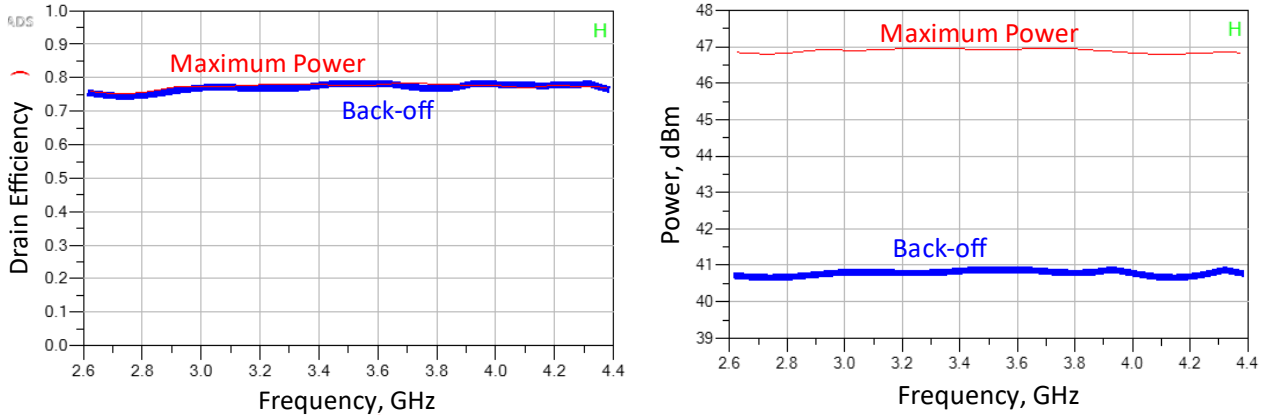
Figure 4.42. Simulation results when LDMOS technology and 2-section BLC is used and the input signal frequency (3.6 GHz) is above the center frequency (3.5 GHz): (a) AM/AM distortion, (b) phase distortion.

4.5.2. In GaN Technology

It has been assumed that GaN technology has 4 times smaller capacitances than LDMOS. Thus, 1.33325 pF and 1.40625 pF parasitic capacitances should be chosen for the CA and BAs, respectively. However, because of a mistake, 0.9375 pF capacitance has been used instead of 1.33325 pF. Such value is also realistic, so simulations have not been repeated. Then simulations have been performed with 5-section coupled lines and alternatively with a 2-section branch line coupler once more.

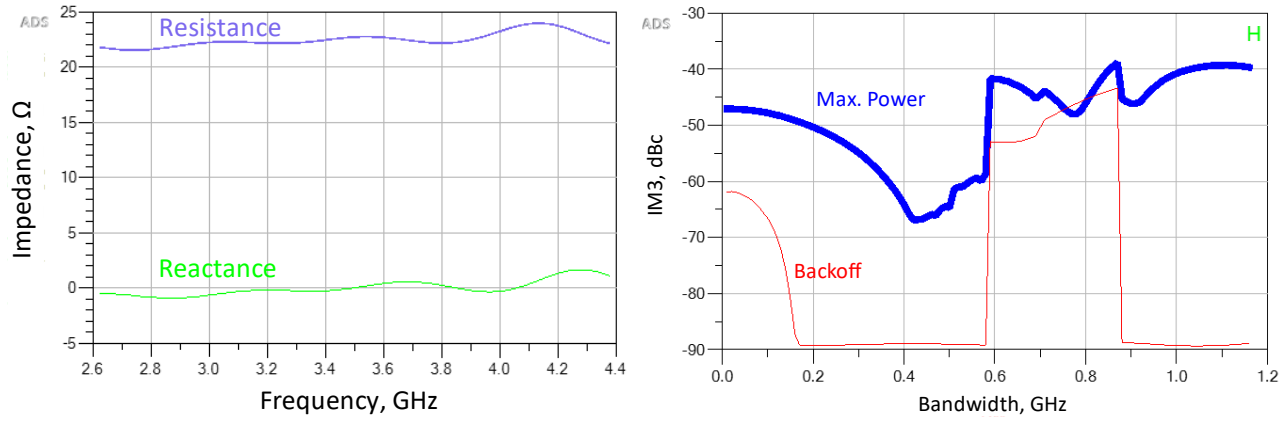
4.5.2.1. With 5-section Coupled Lines

The results are shown from Figure 4.43 to Figure 4.48 and can be compared with the plots for LDMOS cases. As in the LDMOS case with 5-section CL, 1 dB power bandwidth is over 1.8 GHz at maximum power and at the back-off, as presented in Figure 4.43b.



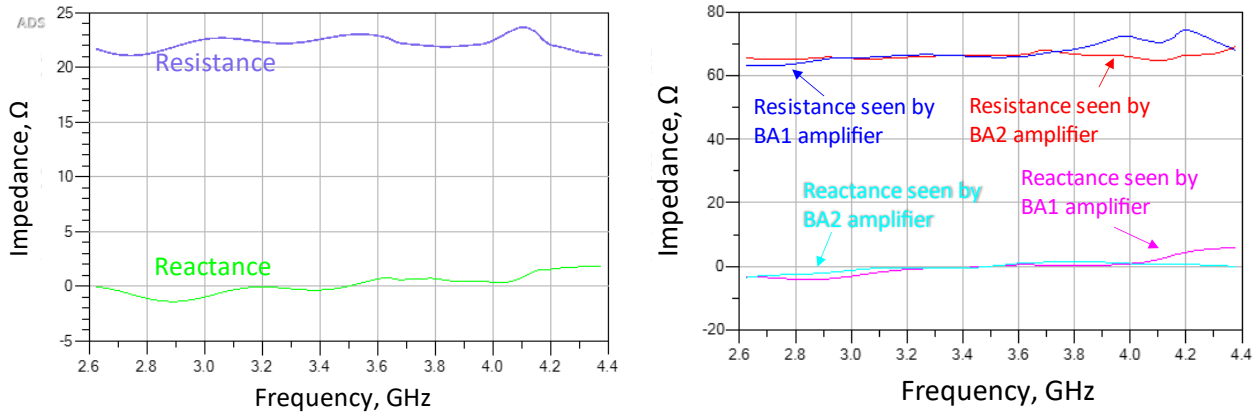
(a) (b)

Figure 4.43. (a) Drain efficiency and (b) power bandwidth when GaN tech. and 5-section CL are used.



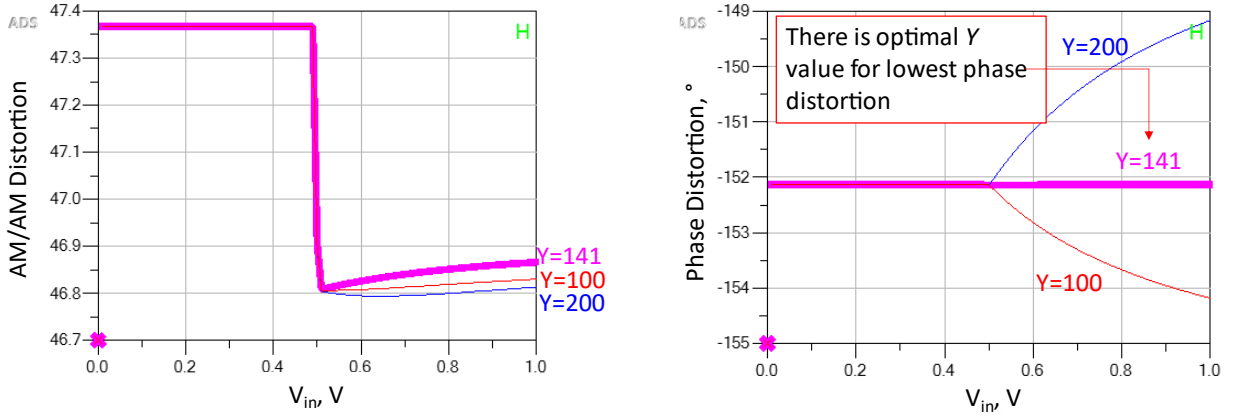
(a) (b)

Figure 4.44. Simulation results when GaN tech. and 5-section CL are used: (a) impedance at the back-off ($V_{in} = 0.49\ V$) seen by the CA, (b) IM3.



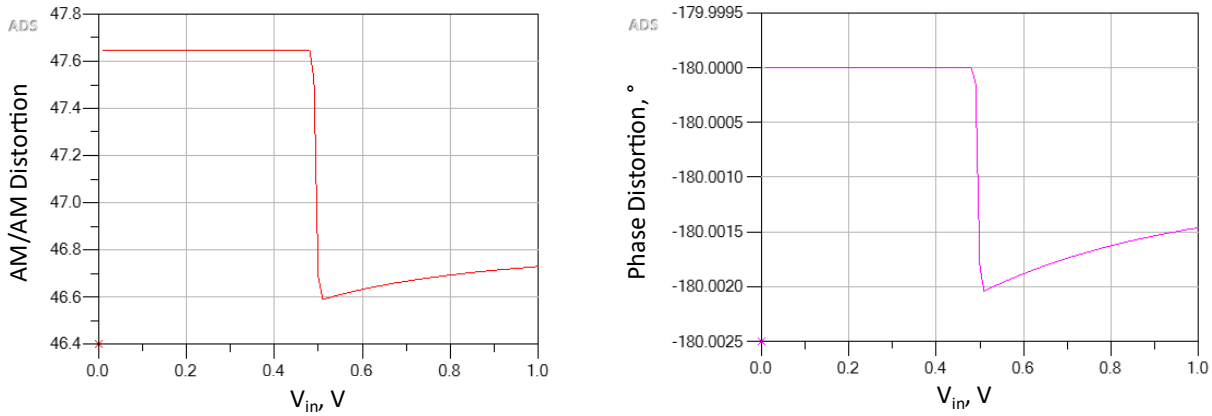
(a) (b)

Figure 4.45. Impedances at max. power ($V_{in} = 1\ V$) when GaN tech. and 5-section CL are used. Impedances seen by: (a) the CA, (b) the BA.



(a) (b)

Figure 4.46. Simulation results when LDMOS technology and 5-section CL are used, and the input signal frequency (3.4 GHz) is below the center frequency (3.5 GHz): (a) AM/AM distortion, (b) phase distortion.



(a) (b)

Figure 4.47. Simulation results when GaN technology and 5-section CL are used, and the input signal frequency is equal to the center frequency (3.5 GHz): (a) AM/AM distortion, (b) phase distortion.

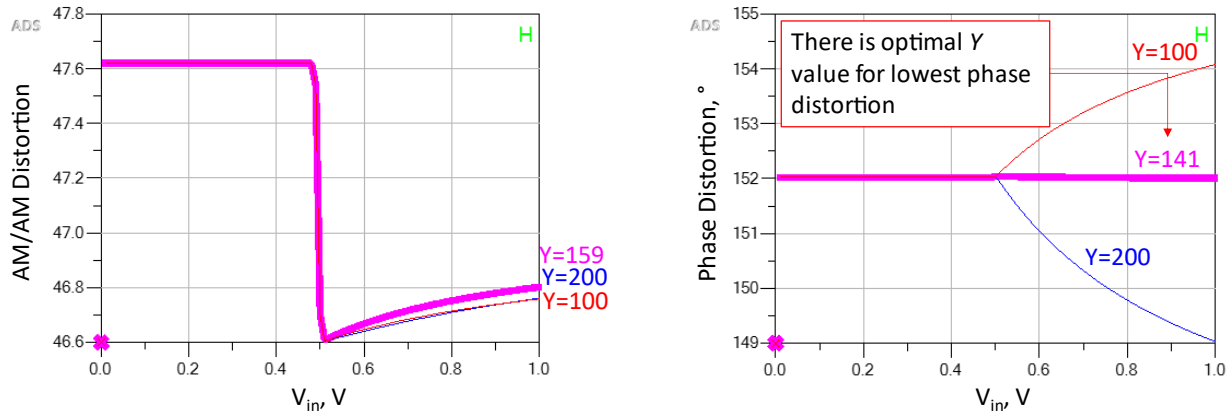


Figure 4.48. Simulation results when GaN technology and 5-section CL are used, and the input signal frequency (3.6 GHz) is above the center frequency (3.5 GHz): (a) AM/AM distortion, (b) phase distortion.

4.5.2.2. With 2-section Branch Line Coupler

In the following, the 5-section coupled lines have been replaced with 2-section branch-line coupler, and the same simulations were performed once more. The results are shown from Figure 4.49 to Figure 4.54 and can be compared with the plots of the previous simulation results. Now 1 dB power bandwidth is over 1.5 GHz at maximum power and 1.4 GHz at a back-off as presented in Figure 4.49b. This is worse than with 5-section coupled lines and similar to LDMOS with BLC.

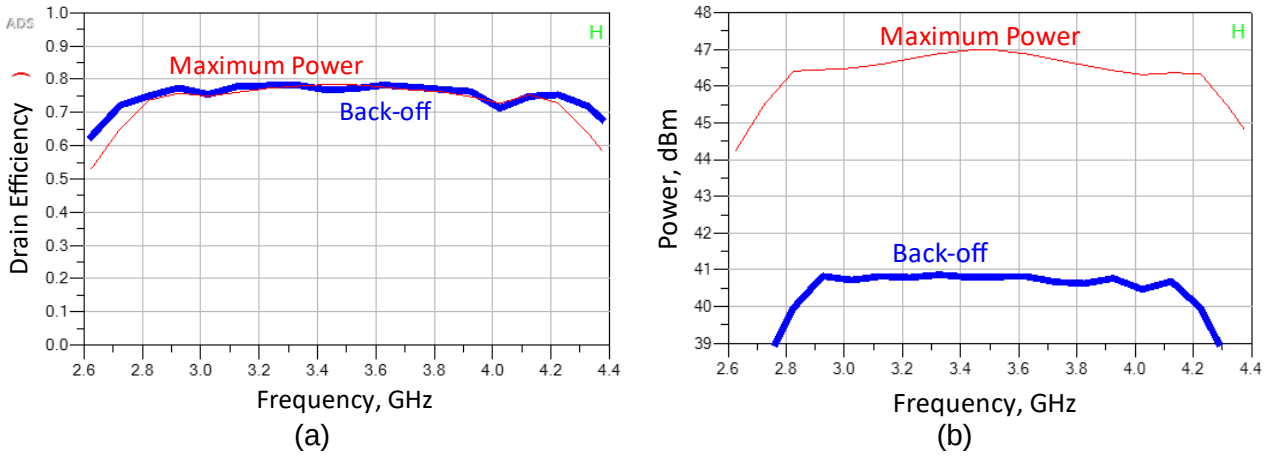


Figure 4.49. (a) Drain efficiency and (b) power bandwidth when GaN tech. and 2-section BLC is used.

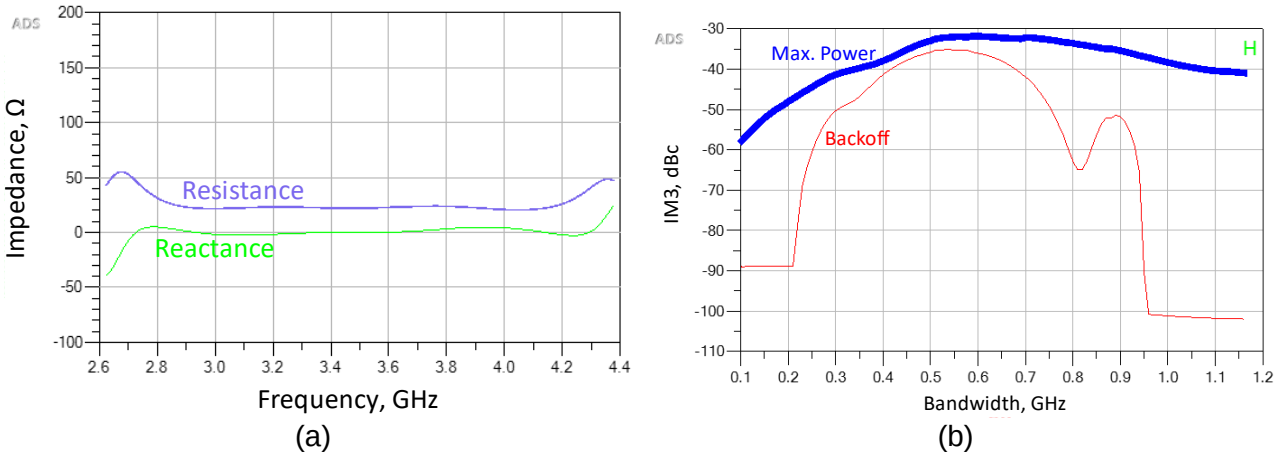
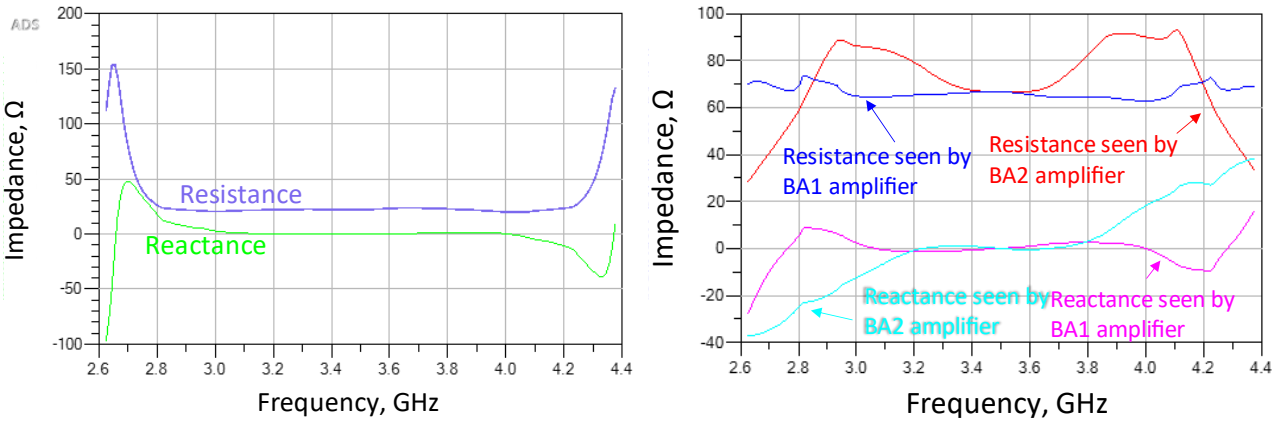
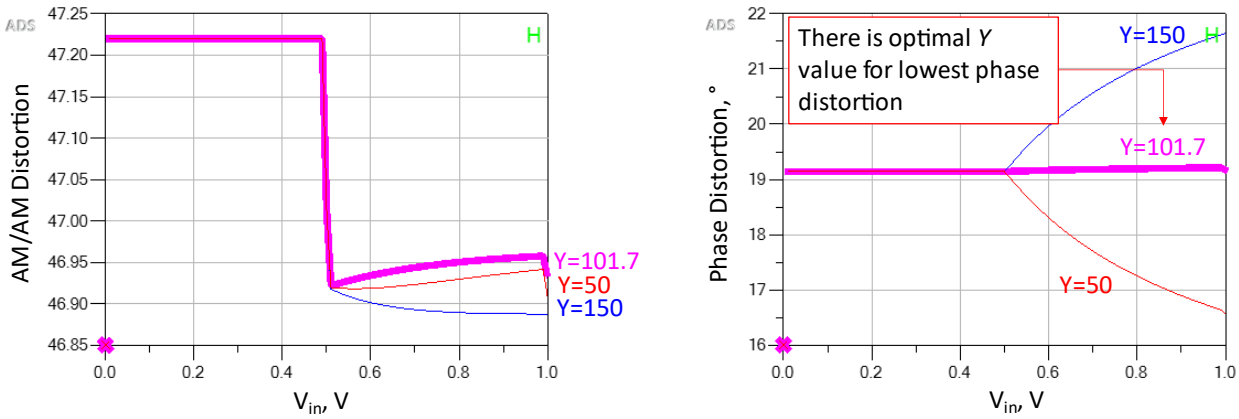


Figure 4.50. Simulation results when GaN tech. and 2-section BLC is used: (a) impedance at the back-off ($V_{in} = 0.49\ V$) seen by the CA, (b) IM3.



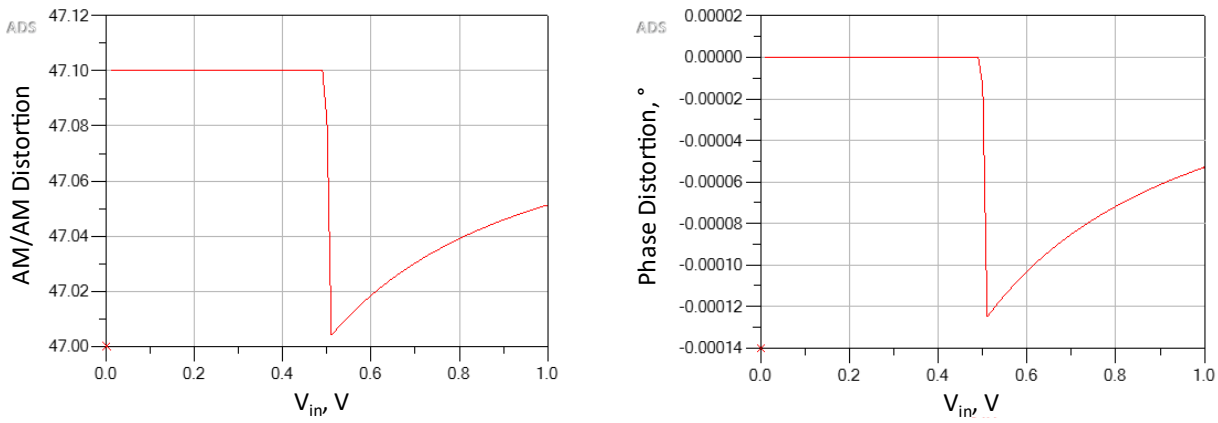
(a) (b)

Figure 4.51. Impedances at max. power ($V_{in} = 1\ V$) when GaN tech. and 2-section BLC is used. Impedances seen by: (a) the CA, (b) the BA..



(a) (b)

Figure 4.52. Simulation results when GaN technology and 2-section BLC are used, and the input signal frequency (3.4 GHz) is below the center frequency (3.5 GHz): (a) AM/AM distortion, (b) phase distortion.



(a) (b)

Figure 4.53. Simulation results when GaN technology and 2-section BLC are used, and the input signal frequency is equal to the center frequency (3.5 GHz): (a) AM/AM distortion, (b) phase distortion.

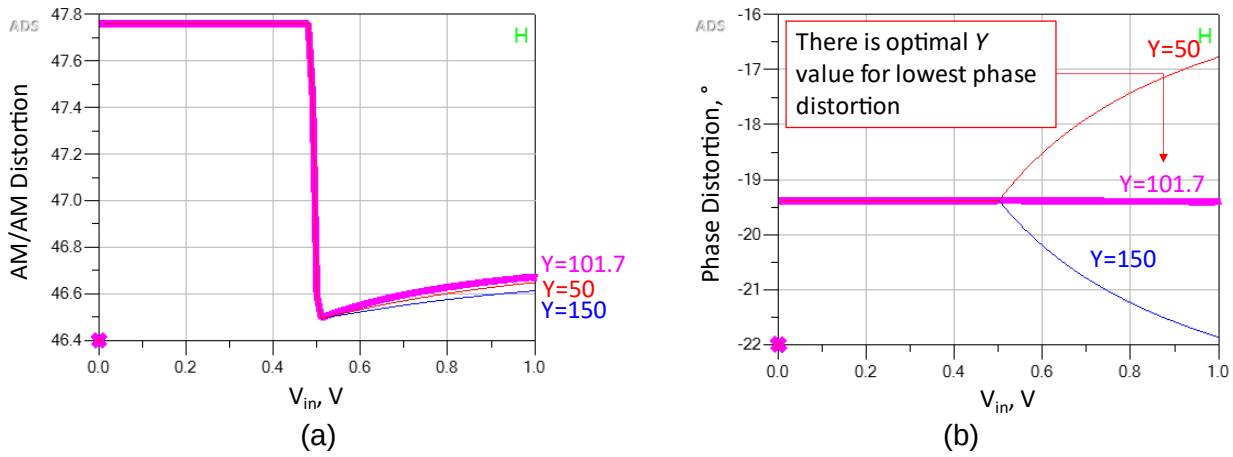


Figure 4.54. Simulation results when GaN technology and 2-section BLC are used, and the input signal frequency (3.6 GHz) is above the center frequency (3.5 GHz): (a) AM/AM distortion, (b) phase distortion.

4.5.3. For Comparison with Conventional Doherty Power Amplifiers

Various Doherty PA topologies have been simulated in the previous chapter while assuming LDMOS technology and 1 W/mm power density at 28 V. However when simulating PD LMBA, it was assumed that the control amplifier's transistor has 1.5 W/mm power density (at 28 V) while other transistors have the same 1 W/mm. Due to this difference, a fair comparison between DPA and PD LMBA topologies cannot be made using the results from sections 4.5.1 and 4.5.2. Thus, additional simulations have been performed where all transistors have 1 W/mm power density at 28 V and 5-section CL. Then parasitic capacitance of the CA's transistor is 7.92 pF and for each BA's transistor is 5.63 pF. Calculations of these values have been provided in section 4.3.3. Results are shown in Figure 4.55 and Figure 4.56. 1 dB power bandwidth at maximum power is over 1.8 GHz, while it is around 1.7 GHz at the back-off. If we compare these results with the summary of the Doherty power amplifier (DPA) simulation results shown in Table 3.3, we could see that this PD LMBA topology can achieve significantly higher bandwidth than DPA even at back-off. The main reason for bandwidth increase at the back-off is that need for an impedance inverter is omitted and that a low impedance load is used for the CA in PD-LMBA. This is made possible by using approximately only half the supply voltage (13.2 V) as is used for the main amplifier in a (conventional) DPA, or the other discussed variants of PD-LMBA (28 V). The lower impedance results in a lower quality tank circuit made of the parasitic capacitance and compensation inductor. A lower quality tank circuit allows getting higher bandwidth. In case to check this, two 12.6 W conventional Class B amplifiers were simulated. One used 28 V power supply while another used 13.2 V. It has been assumed that the current density is 0.15 A/mm (or 1 W/mm at 28 V), and technology is LDMOS. Then parasitic capacitances are 3.75 pF and 7.92 pF, respectively. Despite more than twice the higher capacitance, it has higher bandwidth, as shown in Figure 4.57. The green curve shows how parasitics absorption in the 5-section coupled lines hybrid further increases the bandwidth. However, the implementation of a coupler that has a lower port characteristic impedance is more complicated.

If we would compare Figure 4.56 with Figure 3.74, we could notice that PD-LMBA with a single section transmission line-based coupler has better IM3 at the maximum power than PCL-IDPA with lumped equivalents. When tone spacing is small in PD-LMBA, IM3 is worse (-46 dBc versus -50 dBc and lower for DPA). When the tone-spacing increases, IM3 becomes better. This is opposite to PCL-IDPA. There are fluctuations in IM3 for tone spacing higher than 0.6 GHz because 3rd order intermodulation products which are located around the fundamental tones interact with intermodulation products which are located around the 2nd harmonic. This does not affect DPA so significantly. As we will see in chapter 5, coupler layout can be challenging, and also it can turn out that the lumped implementation of the hybrid is more feasible than transmission line based. Therefore, it is possible that PD-LMBA will have worse IM3 than the inverted PCL DPA topologies. IM3 of compared SCL-DPA is insignificant. Only its differential version can have considerable IM3 (above -60 dBc) when tone spacing is higher than 0.9 GHz.

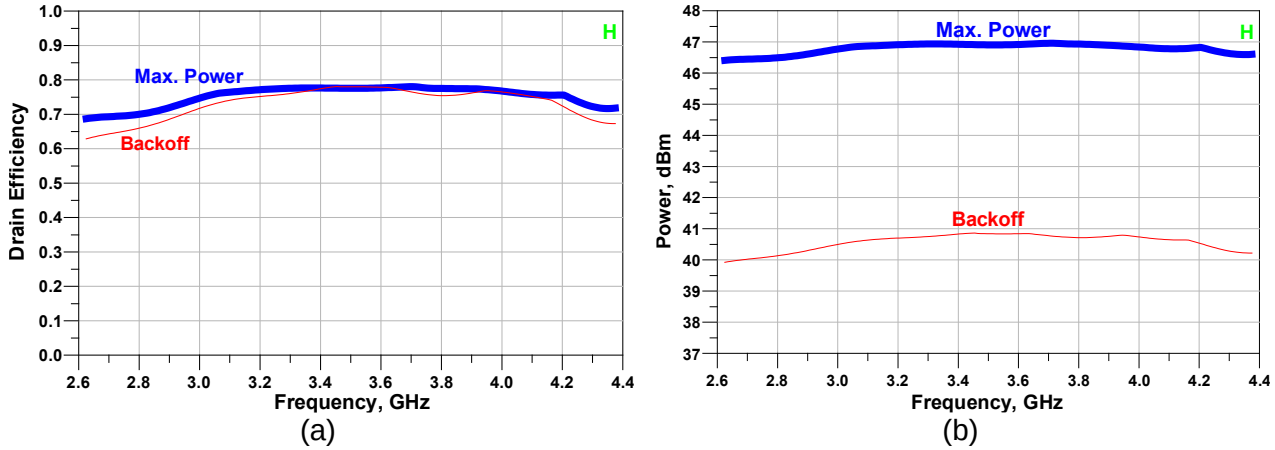


Figure 4.55. (a) Drain efficiency and (b) power bandwidth when LDMOS tech. and 5-section CL are used. All transistors have equal power densities.

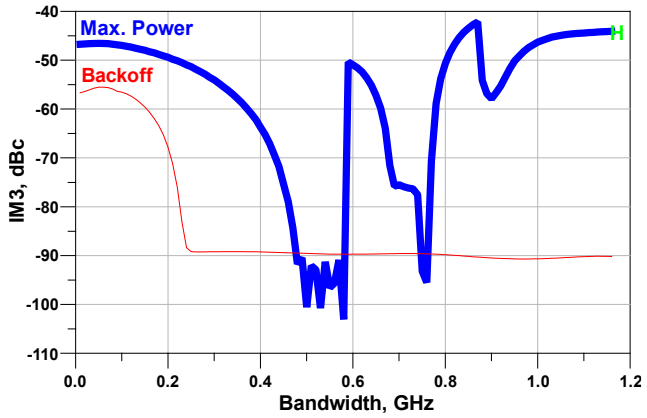


Figure 4.56. IM3 when LDMOS tech. is used, and all transistors have the same power density.

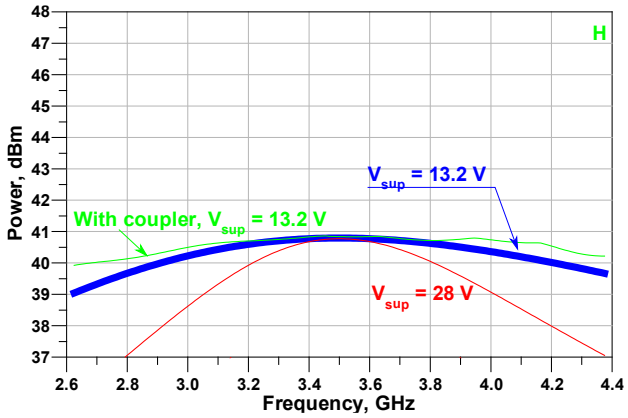


Figure 4.57. Power bandwidth of a 12.6 W Class B amplifier at maximum power (input voltage is 1 V).

4.6. Conclusion

The operation of the PD-LMBA has been explained. Design equations have been derived, design examples and schematics of universal test bench have been provided. Unlike conventional Doherty amplifier topologies, the PD-LMBA theoretically can have unlimited bandwidth; however, it is still limited by parasitics and the hybrid bandwidth in practice. The suitability of single and multi-section coupled lines (CL) and branch-line couplers (BLC) has been researched. The PD-LMBA with 5-section CL and 2-section BLC provided the highest power bandwidth, so they were investigated in more detail, and simulation results have been provided, compared with DPA, and then summarized in Table 4.2.

It has been concluded that even PD-LMBA with a single section CL has higher 1 dB power bandwidth than with a 2-section BLC despite BLC that could absorb the capacitive parasitics completely for LDMOS while CL version could not (see Table 4.1). A 3-section CL has no significant benefit versus a single section, while a 5-section CL can be extremely wideband. There is a lack of information in the literature on designing a BLC with more than two sections. The PD-LMBA with 5-section CL has the best power bandwidth in all tested cases (LDMOS and GaN). BLC has better IM3 when the 2-tone spacing is smaller than CL while CL offers better IM3 for higher tone spacings. GaN topologies have just slightly better power bandwidth than LDMOS counterparts. Consequently, LDMOS can still be very competitive.

By doing simulations studies, it has been concluded that the best results could be obtained with the BLC (in terms of efficiency and 1 dB power bandwidth, IM3) when a half ($\varphi_L = \varphi_R = 45°$) of outer

transmission lines are replaced with their lumped equivalents. Moreover, in that case, the parasitics of the CA (5.33 pF) and of BA (5.63 pF) output stages can be absorbed entirely (see Figure 4.13, for the circuits can component values). The best results for LDMOS with a 5-section CL can be achieved when almost half (φ_L = 41°) of outer transmission lines (TLs) are replaced with their lumped equivalents. Optimum φ_L can be quite different for different specifications and parasitics, and is normally it is between 20° and 60° (e.g., for GaN with 5-section CL it is 20°). It has to be determined by trial & error way. See Figure 4.11 for the circuit and component values.

In our design examples, the CA of PD-LMBA needs 6.94 Ω load impedance. This is a relatively low value. Moreover, for higher power amplifiers, it would be even lower. It is challenging to design a coupler that has so low port characteristic impedance. It is possible to use a hybrid with a higher port characteristic impedance and match the amplifiers to the hybrid. However, it is tough to do matching between very low load impedance and relatively high, e.g., 50 Ω. Matching networks may be complicated and introduce significant matching errors, resulting in reduced efficiency and power bandwidth. Classical PCL-DPA requires 7.84 Ω, which is still low, but SCL-DPA needs a value four times higher than that, i.e., 31.4 Ω. If SCL-DPA were made entirely push-pull, it would require even a two times higher value in terms of load impedance, i.e., 62.7 Ω. On the other hand, it would not have a reference to ground. Alternatively, one could try to develop hybrids with different port impedances for the CA, RFout, and BA ports. Although a straightforward design procedure for such a hybrid is not yet available, this latter option might provide the ultimate solution. So, this remains a fruitful area for further investigations.

Table 4.2. Comparison of PD-LMBA variants.

Topology	**Back-off (V_{in} = 0.49 V)**			**Max Power (V_{in} = 1 V)**		
	BW	**η_{min}**	**η_{center}**	**BW**	**η_{min}**	**η_{center}**
LDMOS, 5-sec. CL	>1800	0.718	0.78	>1800	0.729	0.775
LDMOS, 2-sec. BLC	1480	0.665	0.765	1530	0.685	0.778
LDMOS, 1-sec CL	>1800	0.694	0.772	>1800	0.686	0.78
GaN, 5-sec. CL	>1800	0.745	0.783	>1800	0.752	0.777
GaN, 2-sec. BLC	1420	0.71	0.768	1500	0.684	0.784
For comp. with DPA	1800	0.629	0.78	>1800	0.687	0.775
IPCL-DPA with lumped eq. to main amp. (highest DPA overall bandwidth result)	610	0.628	0.783	920	0.709	0.783

5

IMPLEMENTATION AND LAYOUT CONSIDERATIONS

When SPICE simulation results look satisfying, the next step is IC or/and PCB layout design and electromagnetic simulations. PD-LMBA topology is new, and our observation which allows us to use a symmetrical hybrid without a matching network (see section 4.3.3) has to be tested in practice. Thus, this chapter discusses how the layout could be made. Note that the focus is on its feasibility since no finalized layout is given.

5.1. HARMONIC TERMINATION

Until now, only ideal harmonic termination (HT) has been used. It can be implemented in many ways. Our initial idea was to use 5-section coupled lines (CL) and skip the HT at all. Unfortunately, its performance becomes unsatisfying without the HT. Then we replaced Class B amplifiers with Class B/J, which can be very wideband and include HT in its output matching network. This has been described in more detail in section 2.4. However, it turned out that Class B/J output matching network cannot provide a sufficient 2nd harmonic short when the optimum load impedance is so low.

Moreover, we have noticed that implementing a 5-section CL is complicated because some sections have extremely low odd impedances (only a few ohms), it also may be large, and its transmission lines may be too lossy. Since the PD-LMBA can also have very high bandwidth only with a single section CL, we decided to use only that one. It turned out that when using only a single section CL, the circuit can have quite satisfying performance even with completely skipped HT.

5.1.1. TEST CASES

When we have noticed that PD-LMBA with a single section CL and without harmonic termination can give good enough performance, we still decided to check several other simple ways to terminate harmonics. In total, the following cases were tested before going to the final conclusion:

1. Ideal harmonic short (Figure 4.9);

2. No harmonic termination (Figure 5.1a);
3. LC short (Figure 5.1b);
4. Ideal harmonic open (Figure 5.1c);
5. LC open (Figure 5.1d).

"H.O." component in the circuit means harmonic open. It has low impedance at frequencies below 4.67 GHz and very high above, see Figure 5.2. Cases 1-3 were tested when the coupled lines were true transmission lines. All cases were tested when the coupled lines were replaced with two lumped segments (each one has 45° electrical length, 2×45°) and when replaced with four lumped segments (then each segment has 22.5° electrical length, 4×22.5°). When lumped equivalents were used, parasitics absorption was done.

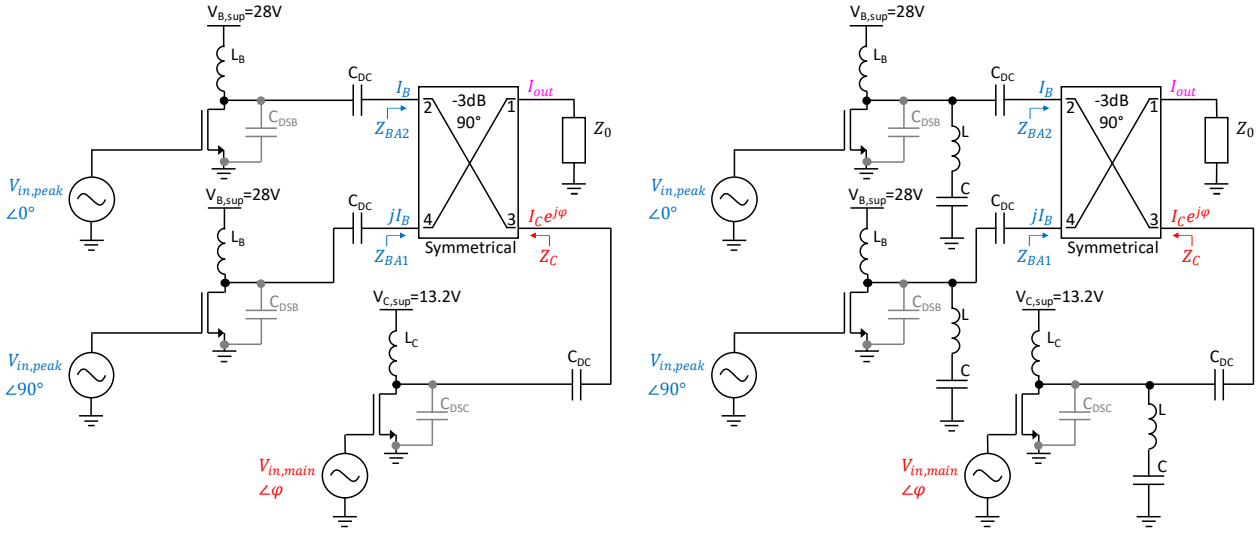


Figure 5.1. Test cases for harmonic termination

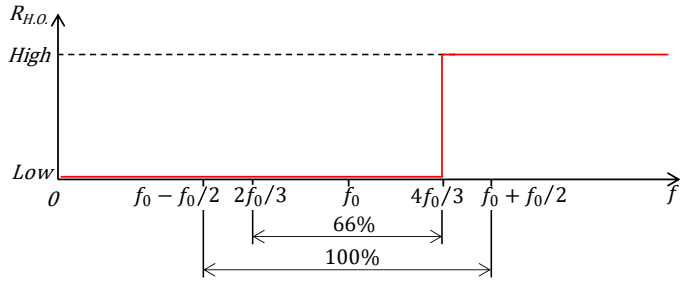


Figure 5.2. Frequency response of "ideal harmonic open" component.

5.1.2. Comparison of Simulation Results

When simulations have been performed, it turned out that the highest and smoothest bandwidth is obtained when harmonics are not terminated (Figure 5.1a) and lumped equivalents are not used at all, despite that parasitic capacitance cannot be absorbed in this case. When lumped equivalent replacements are used, bandwidth plots created at the power back-off and the maximum power level are shown in Figure 5.3 and Figure 5.4, respectively. Thus, it seems that the most practical choice is to skip harmonic termination and do not absorb parasitic capacitances. Note that the parasitic capacitance and compensation inductor are seen as a parallel tank circuit by the AC signal. The tank circuit acts as an open circuit for the center frequency and has low impedance for harmonics. Thus, even if the harmonics termination is not implemented, the tank circuit still provides a sort of weak harmonic termination. In case to check harmonics inhibition, the reflection coefficient from each coupler input port for the fundamental and second harmonic has been plotted on the Smith chart at back-off and the maximum power. The results are shown in Figure 5.5 and Figure 5.6, respectively. It can be seen from these figures that the fundamental tone does not have significant reflections while the 2nd harmonic is not well terminated, so it influences bandwidth, efficiency, and IM3 distortion. Nevertheless, this variant still provides relatively good performance.

The variant where the lumped equivalent with 4 segments (4×22.5°) is used and parasitics are absorbed also have decent performance when harmonic termination is not implemented. This can be seen if we would compare simulation results which are shown in figures 5.3 to 5.16. Thus, it can be an excellent alternative to the previously discussed variant because it is likely that the physical implementation of the lumped equivalent of the hybrid will be more feasible than the transmission lines-based one.

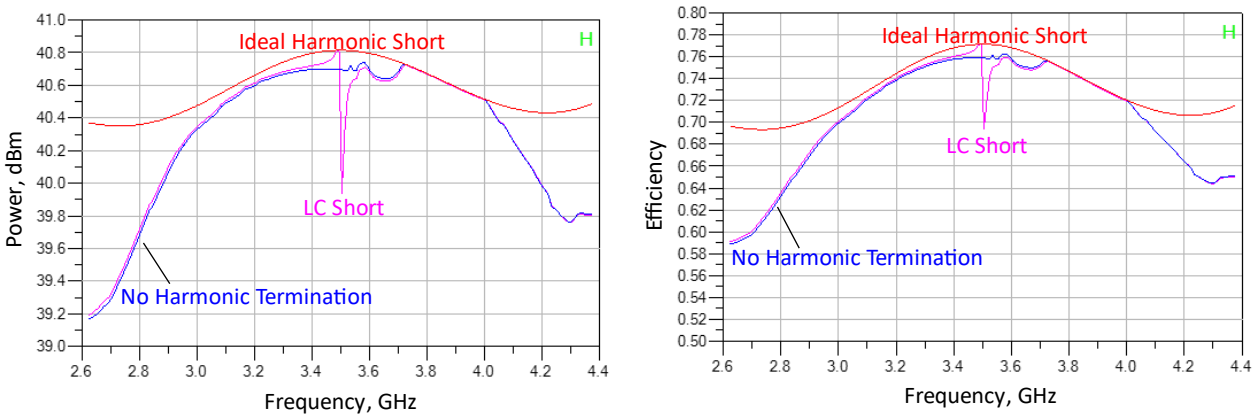


Figure 5.3. Power (a) and efficiency (b) bandwidth at back-off (V_{in} = 0.49 V) for different harmonic termination cases when transmission lines are used.

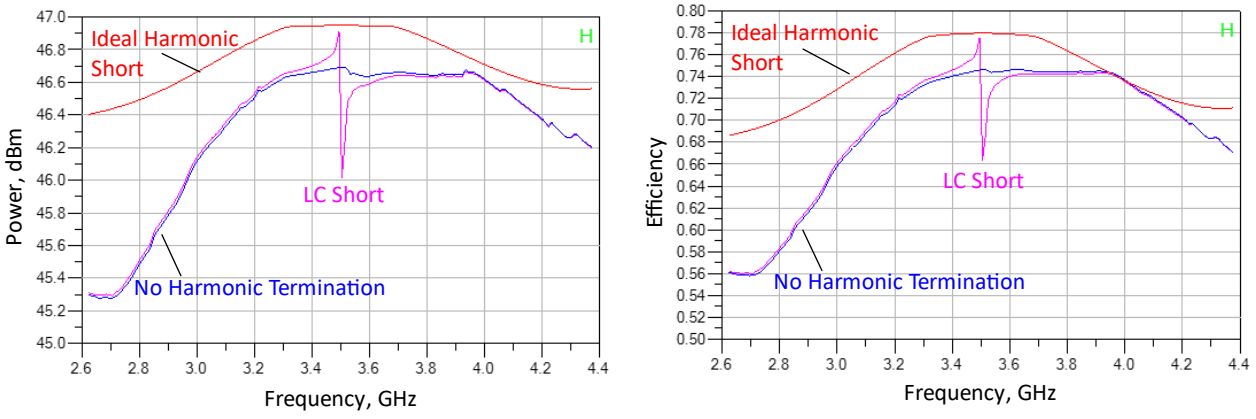


Figure 5.4. Power (a) and efficiency (b) bandwidth at maximum power (V_{in} = 1 V) for different harmonic termination cases when transmission lines are used.

The variant where the lumped equivalent with 2 segments (2×45°) is used has the worst results. Therefore not complete simulation results are included for this case. They are present only in figures 5.11 – 5.16. 0.539 pF can be absorbed when lumped equivalent is 4×22.5°, or 1.123 pF can be absorbed when the lumped equivalent is 2×45°.

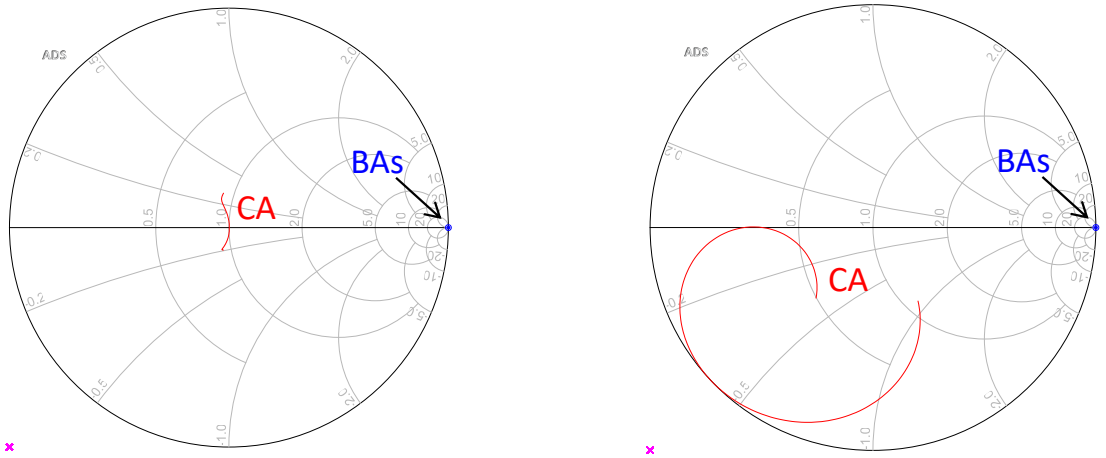


Figure 5.5. Reflection coefficient from each coupler input port for the fundamental tone (a) and its second harmonic (b) at back-off (V_{in} = 0.49 V) when transmission lines are used. Frequency range is from 2.625 GHz to 4.375 GHz.

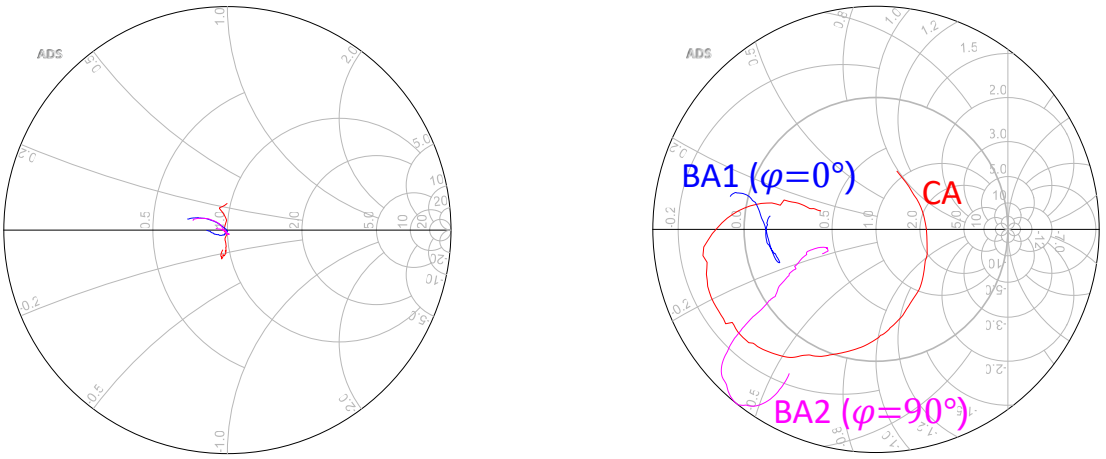


Figure 5.6. Reflection coefficient from each coupler input port for the fundamental tone (a) and second harmonic (b) at the maximum power (V_{in} = 1 V) when transmission lines are used. The frequency range is from 2.625 GHz to 4.375 GHz.

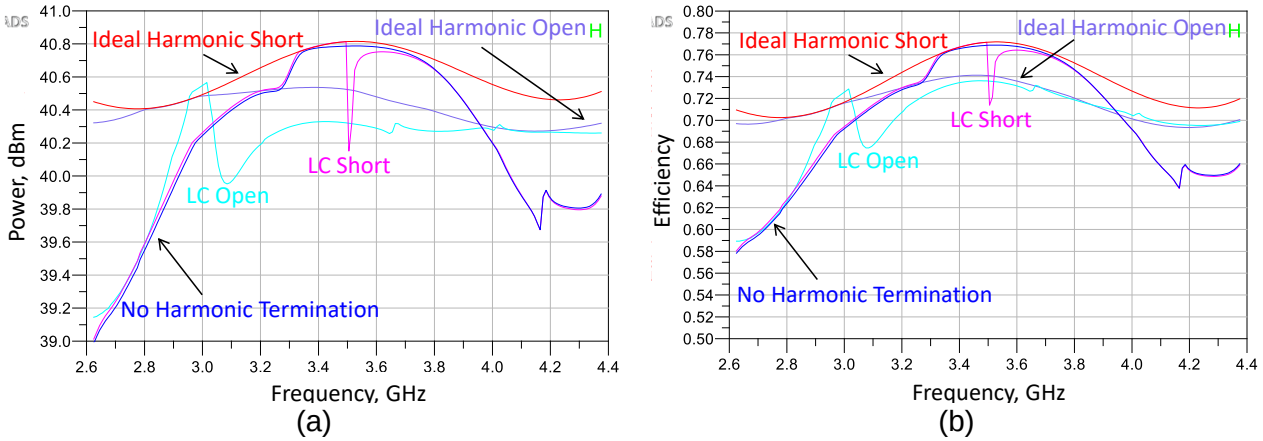
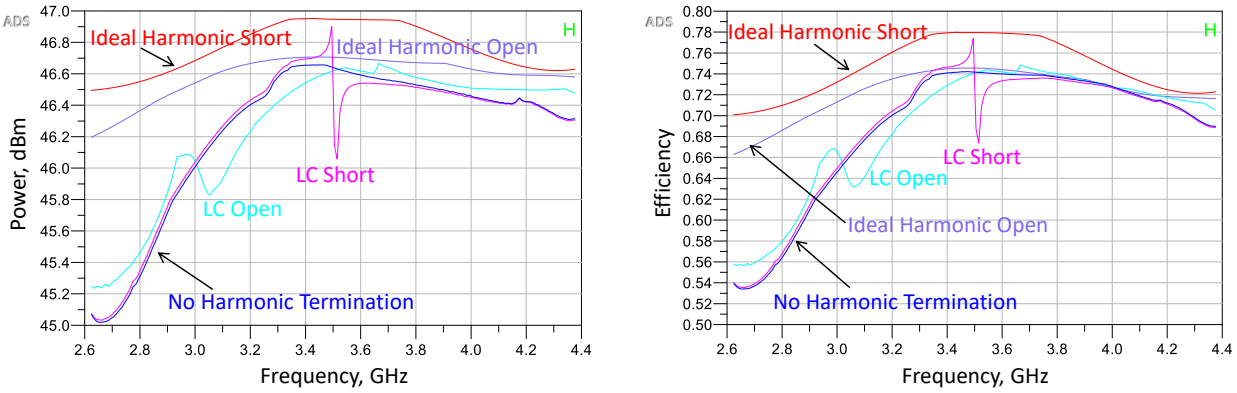
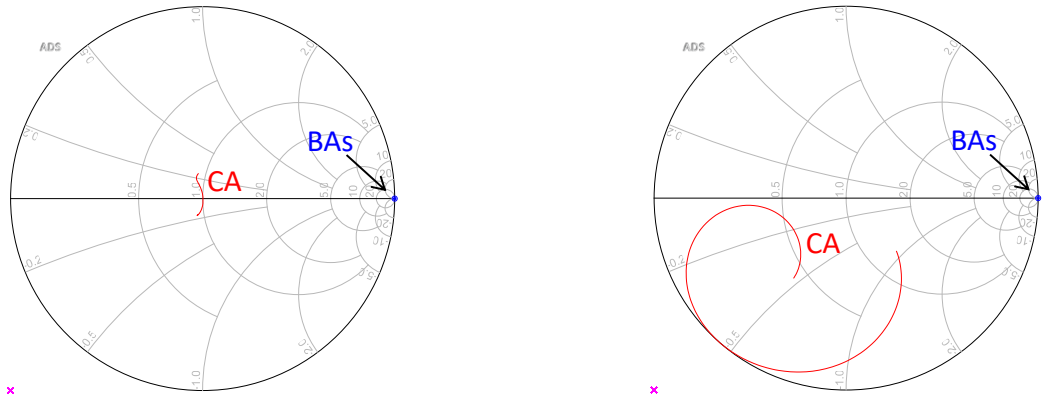


Figure 5.7. Power (a) and efficiency (b) bandwidth at back-off (V_{in} = 0.49 V) for all harmonic termination test cases when 4×22.5° lumped equivalents of transmission lines are used.



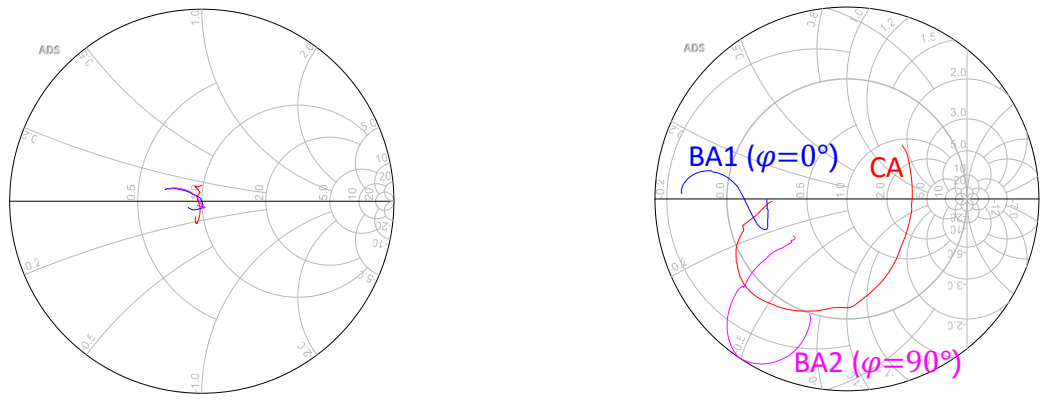
(a) (b)

Figure 5.8. Power (a) and efficiency (b) bandwidth at maximum power (V_{in} = 1 V) for all harmonic termination test cases when 4×22.5° lumped equivalents of transmission lines are used.



(a) (b)

Figure 5.9. Reflection coefficient from each coupler input port for the fundamental tone (a) and its second harmonic (b) at back-off (V_{in} = 0.49 V) when 4×22.5° lumped equivalents of transmission lines are used. The frequency range is from 2.625 GHz to 4.375 GHz.



(a) (b)

Figure 5.10. Reflection coefficient from each coupler input port for the fundamental tone (a) and its second harmonic (b) at maximum power (V_{in} = 1 V) when 4×22.5° lumped equivalents of transmission lines are used. The frequency range is from 2.625 GHz to 4.375 GHz.

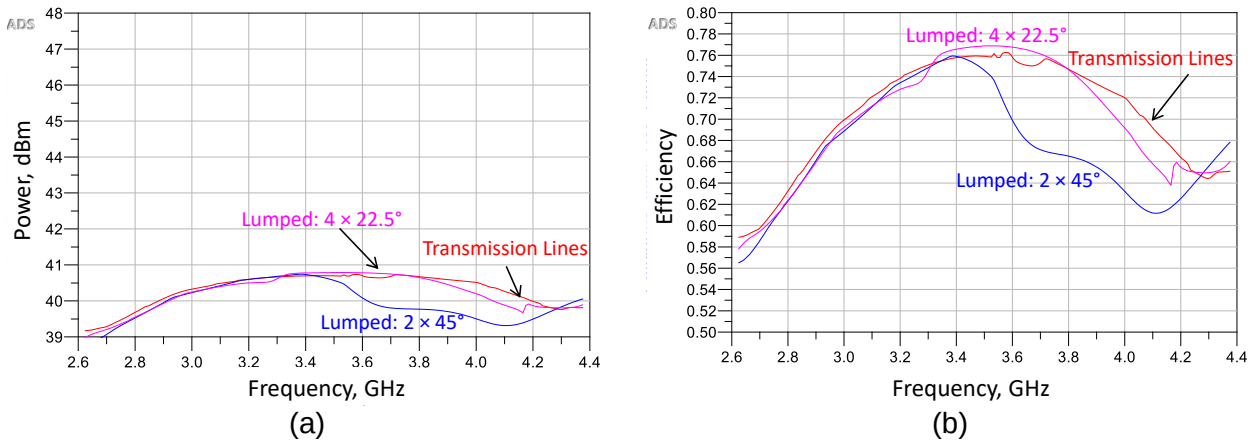


Figure 5.11. Power (a) and efficiency (b) bandwidth at back-off (V_{in} = 0.49 V) when harmonic termination is not present. Comparison of performance when transmission lines and their lumped equivalents are used.

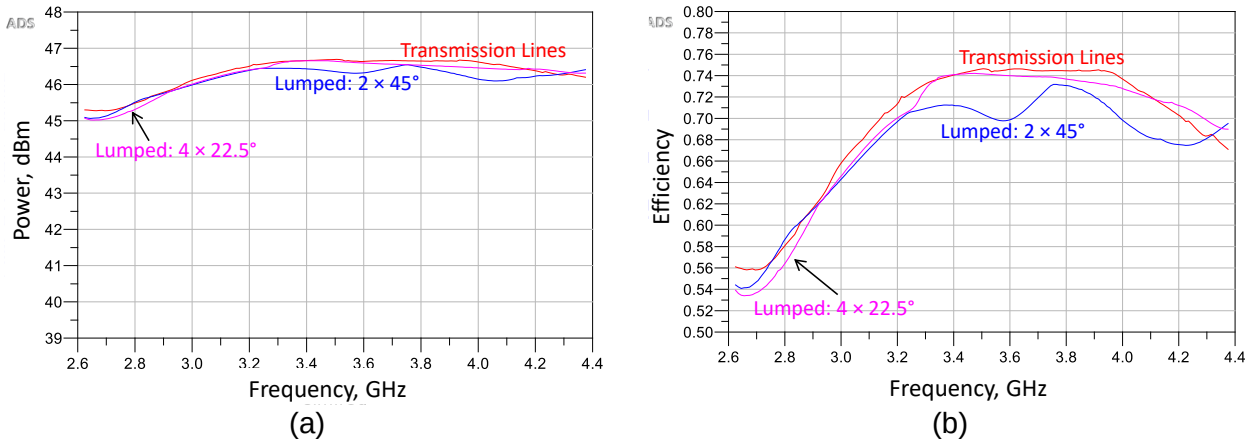


Figure 5.12. Power (a) and efficiency (b) bandwidth at maximum power (V_{in} = 1 V) when harmonic termination is not present.

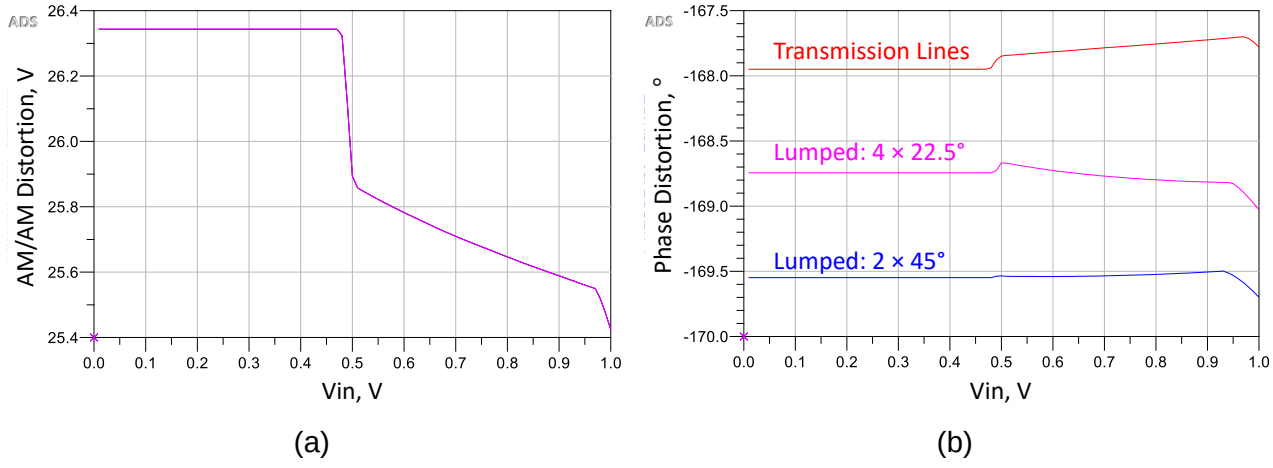
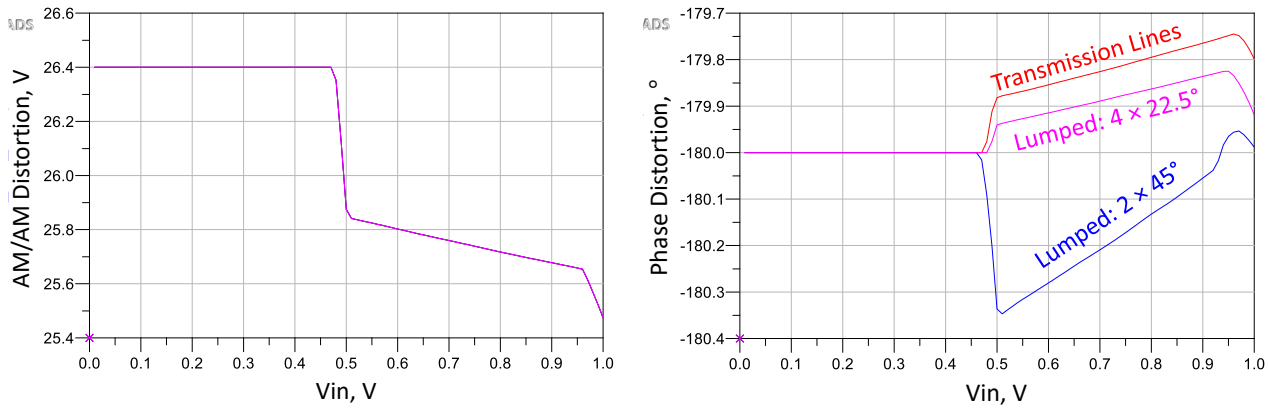
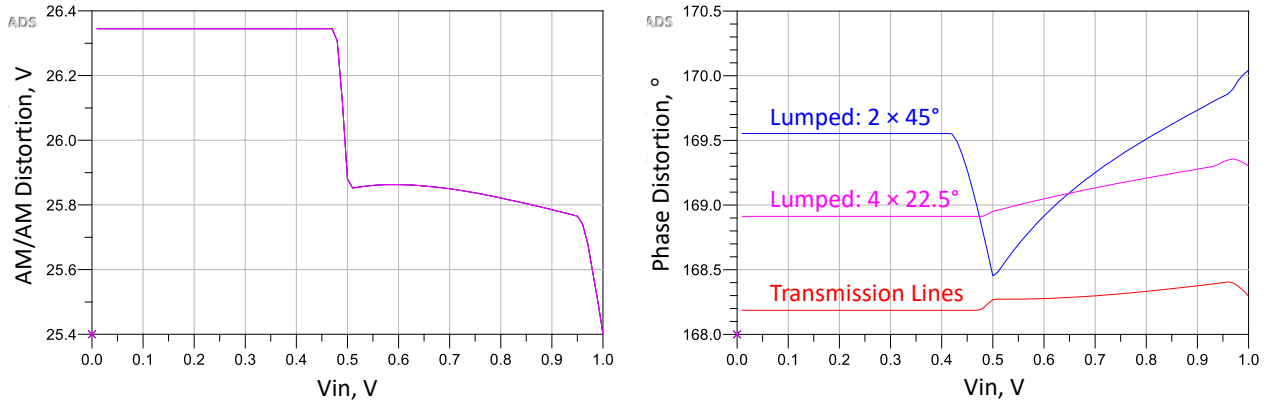


Figure 5.13. AM/AM (a) and phase (b) distortion when harmonic termination is not used. Input signal frequency (3.4 GHz) is below the center frequency (3.5 GHz). Comparison of performance when transmission lines and their lumped equivalents are used. Note that AM/AM results overlap.



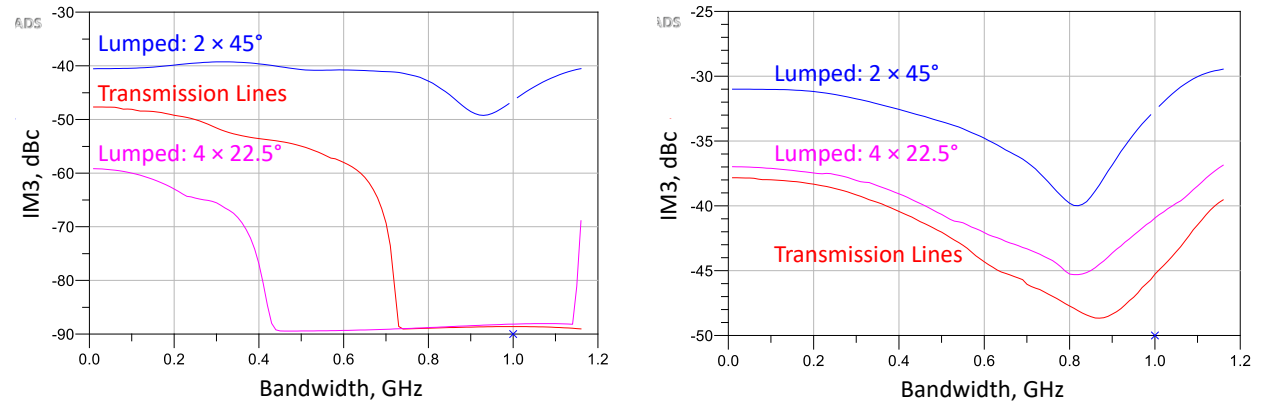
(a) (b)

Figure 5.14. AM/AM (a) and phase (b) distortion when harmonic termination is not used. Input signal frequency is equal to the center frequency (3.5 GHz). Comparison of performance when transmission lines and their lumped equivalents are used. Note that AM/AM results overlap.



(a) (b)

Figure 5.15. AM/AM (a) and phase (b) distortion when harmonic termination is not used. Input signal frequency (3.6 GHz) is above the center frequency (3.5 GHz). Comparison of performance when transmission lines and their lumped equivalents are used. Note that AM/AM results overlap.



(a) (b)

Figure 5.16. IM3 distortion at the center frequency (3.5 GHz) when harmonic termination is not used. Comparison of performance when transmission lines and their lumped equivalents are used.

5.2. Coupled Lines Hybrid

Now we know that it is best to skip the implementation of harmonic termination. The next step is to create the coupler layout and perform electromagnetic simulations. As described in the previous section, according to the harmonic balance simulation results, the single section coupled lines hybrid which uses transmission lines or their lumped equivalent with four segments (4×22.5°), can have good performance. Thus, these two variants are good candidates for the layout. While doing the layout, it can be noticed that one candidate is more feasible than the other one. The focus is on the layout feasibility since no finalized layout is given.

It is preferred to have the complete power amplifier on a single chip and avoid the requirement of external components. Thus, if possible, the hybrid should be made on that chip. The structure of the preferred LDMOS substrate is already known. It has been entered into “Keysight ADS” substrate editor. The structure definition is shown in Figure 5.17.

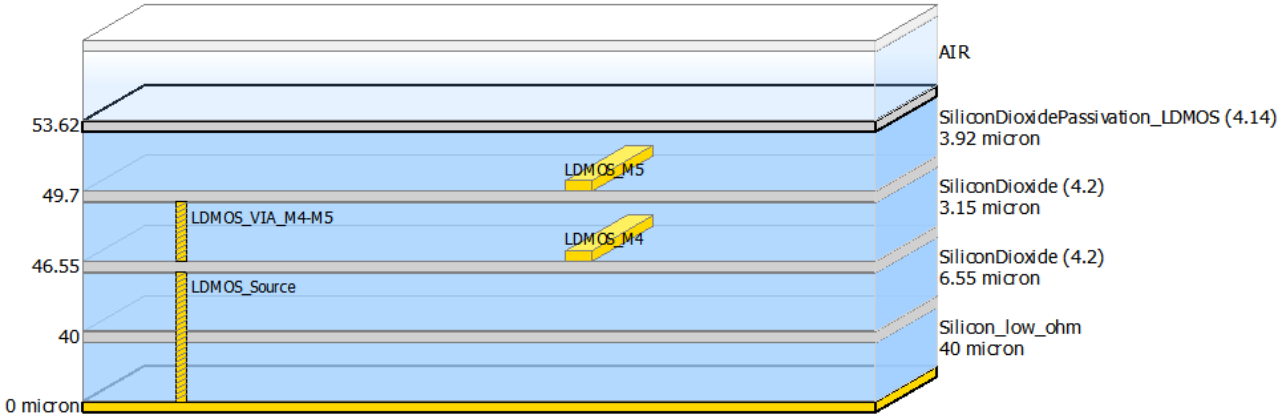
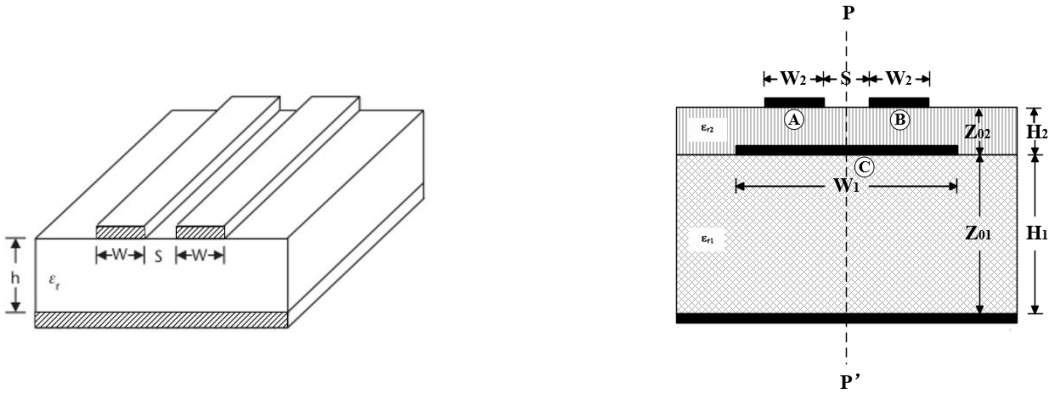


Figure 5.17. Structure of preferred LDMOS substrate.

5.2.1. Transmission Line Based Version

As it has been calculated in section 4.3.4.1, the required coupled lines have Z_{odd} = 2.87 Ω and Z_{even} = 16.8 Ω. The odd characteristic impedance is very low. This makes the design procedure challenging.

The simplest and most common implementation of coupled lines is shown in Figure 5.18a. Its design equations are implemented in the “LineCalc” tool, a part of the “Keysight ADS” software suite. Moreover, after we define substrate and perform geometry calculations using “LineCalc” tool, the layout can be generated automatically. However, it turned out that in our case, “LineCalc” cannot be used for the calculations because the substrate parameters are out of bounds which are supported by implemented design equations. Therefore, we created a parametrized layout instead. Width (W), length (L), and spacing (S) have been chosen as independent variables. Electromagnetic simulations have been performed to calculate S-parameters and Z-parameters. S-parameters can be used to compare the simulated structure with ideal coupled lines. Z-parameters can be used to calculate Z_{odd} and Z_{even} impedances. In such a way, we could check how the adjustment of each variable affects the behavior of the structure. After many attempts to tune the values manually and using an optimization tool, we decided to try re-entrant edge-coupled microstrip lines as presented in Figure 5.18b. S. B. Cohn first described them [37]. They give additional degrees of freedom which may help to reach low odd impedances with the desired behavior. However, this didn’t give any good results yet but needs further investigation. An alternative could be the use of multiple conventional edge-coupled microstrip lines in parallel. Then lines with higher Z_{odd} could be used, but this would also result in a complicated layout which would take a lot of space. This case has not been tested at all. Another alternative could be implemented using lumped equivalents.



(a) (b)

Figure 5.18. Edge-coupled microstrip lines: (a) conventional, (b) re-entrant [38].

5.2.2. Lumped Equivalent Based Version

As already mentioned, the coupled lines hybrid can be replaced with its lumped equivalent. A single section 90° hybrid can be implemented by its lumped equivalent. However, a single segment lumped equivalent does not have adequate bandwidth performance (simulation results not included). Even when two segments are used, the bandwidth performance is not very good, according to the results presented in figures 5.11 – 5.16. However, the four-segment equivalent offers sufficient bandwidth performance according to figures 5.3 to 5.16. When two segments are used, each one should have 45° electrical length because the total electrical length has to be 90° (2×45°). Similarly, four segments can be used when each segment has 22.5° electrical length (4×22.5°), as shown in Figure 5.19. Although 4×22.5° lumped equivalent shown significantly better performance than other tested lumped equivalents, it is also possible that 4×22.5° will be too lossy or too big, and then a smaller number of segments may be preferable. The layout of each segment can look like in Figure 5.20b. Then they might be implemented on the chip, as shown in Figure 5.21.

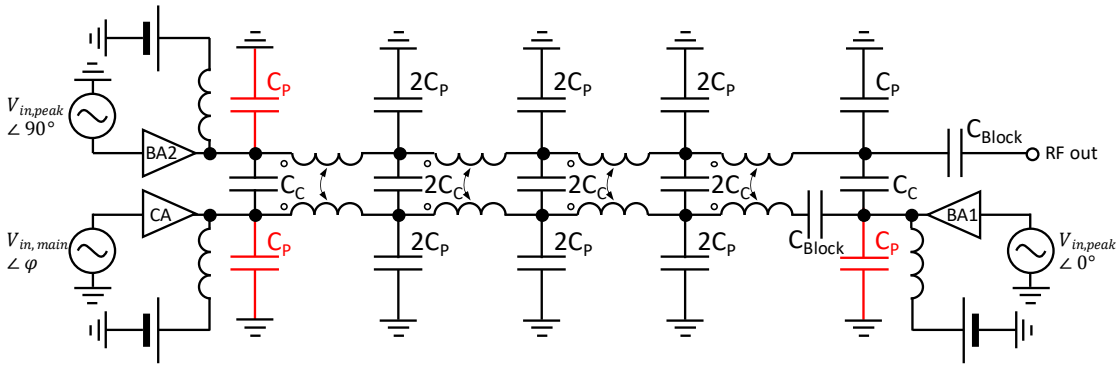
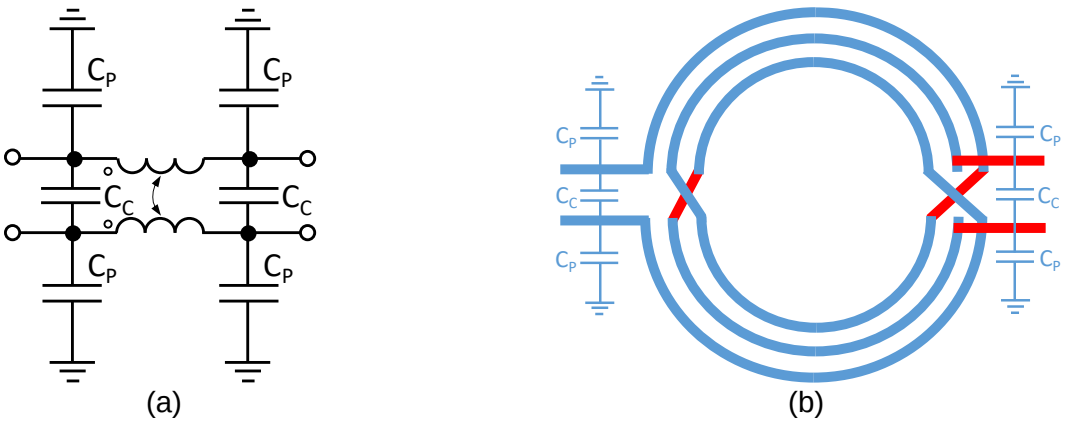


Figure 5.19. PD-LMBA with 4×22.5° lumped equivalent of coupled lines hybrid. Transistor C_{DS} parasitics can be a part of capacitances which are shown in red.



(a) (b)

Figure 5.20. The lumped equivalent of coupled lines hybrid's segment with electrical length 90°/N, where N is the number of segments (with N in the range 1-4): (a) circuit diagram, (b) its proposed layout draft sketch.

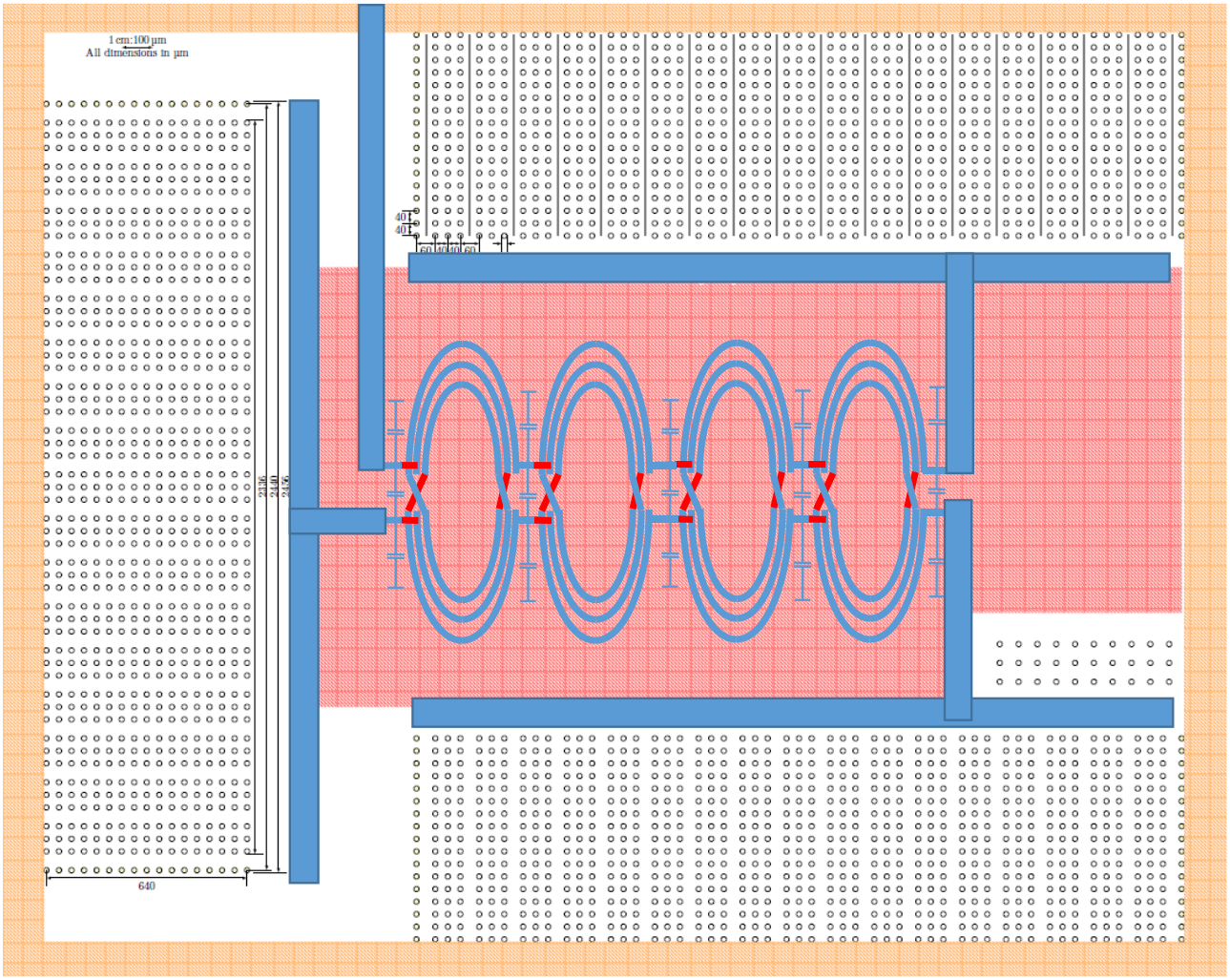


Figure 5.21. Flip-Chip, draft sketch.

5.3. Conclusion

It has been found out that the most optimal solution is to skip harmonic termination and to use a single-section coupled lines hybrid or its lumped equivalent, which consists of 4 lumped segments. Each one should have 22.5° electrical length. It is challenging to implement the coupled transmission line-based hybrid because Z_{odd} is very low. Conventional edge-coupled microstrip lines (Figure 5.18a) are not directly suited for implementation on the preferred LDMOS substrate. However, their re-entrant version (Figure 5.18b) gives an additional degree of freedom, so there is more chance that values for the desired operation exist. Alternatively, a lumped version of the hybrid can be used. However, its design is also challenging. There is a lack of tools for automated coupled inductors design. Existing automated transformer design tools are not very suitable for such cases. Thus, even in this case, the design could be done in a trial-and-error way. Moreover, transformer geometry is more complicated, making the design tricky, and simulations would be significantly slower. Attempts to design and test layouts for these variants should be made before concluding which variant is the most suitable.

CONCLUSION

In this project, we have researched and compared various Doherty PA topologies in terms of their; linearity, 1 dB power bandwidth, and efficiency over the bandwidth. It has been assumed that only parasitic capacitance between drain and source of each transistor is present. We targeted as application mMIMO operating at 3.5 GHz center frequency and 50 W peak output power.

First, a simulation study has been performed for over 45 variations of the Doherty PA. These include conventional as well as inverted topologies with PCL and SCL. Both single-ended as well push-pull/differential topologies have been studied. The inverted Doherty PA achieved the highest bandwidth at power back-off (610 MHz) when designed according [24]. Using a lumped equivalent circuit approximation of the transmission line connected to the main amplifier allows for absorption of its parasitic capacitance. Without using the absorption technique, the bandwidth was reduced to 530 MHz. On the other hand, using lumped equivalent networks for the impedance inverter made the IM3 versus bandwidth (tone spacing) worse for all topologies.

1 dB power bandwidth of the mentioned PCL-IDPA at maximum power is 820 MHz (see Table 3.3). According to these results, the PCL-IDPA has a significantly larger bandwidth than a conventional PCL-DPA, while having a similar power bandwidth as SCL-DPA. It is important to note that no output matching networks have been used in these simulations to reach the external 50 ohm level. Instead, the optimum load impedance has been connected directly. Thus, these simulations did not consider possible deviations in the applied matching in practical situations. The SCL topology is assumed to be more forgiving than the PCL for identical specifications due to its higher load impedance. Note that a deviation in the matching conditions typically leads to a reduction of realizable bandwidth.

Thus, it is likely that practical implementations of the SCL-DPA will reach a higher bandwidth than PCL-IDPA and PCL-DPA. Moreover, if SCL-DPA is made completely push-pull, its load impedance would be even higher. For example, a symmetrical SCL-DPA needs a 4x higher load impedance than the same PCL-DPA. If it is made entirely push-pull, it will feature 8x higher load impedance than the PCL-DPA [16]. This trick cannot be easily applied to PCL-DPA to increase its load impedance.

Next is a novel architecture with a Doherty PA-like efficiency behavior studied. It is called a pseudo-Doherty (PD) PA. This architecture is based on the LMBA structure. Unlike the Doherty PA, it does not have a fundamental bandwidth limitation since it does not feature an impedance inverter. In practical implementations, it will still be limited by transistor output capacitances and the bandwidth of -3 dB hybrid used. In theory, it can be more wideband than all previously discussed Doherty PA topologies. During the harmonic balance simulations, the PD-LMBA has been tested with multi-section coupled-lines couplers (CL) and branch-line couplers (BLC). It has been concluded that the hybrid can be either symmetrical using additional matching networks between the BA and CA, or asymmetrical without additional matching networks, which is, however, more challenging to design. To bypass these challenges, the supply voltage for the CA (control amplifier) can be chosen lower than that of the BA (balanced amplifiers). In that case, a symmetrical hybrid also can be used without additional matching networks. This latter approach has not been reported in the literature, giving a good opportunity for further research. A significantly higher 1 dB bandwidth has been achieved than for the DPA: 1.7 GHz at back-off and over 1.8 GHz at maximum power.

On the other hand, the PD-LMBA requires even lower load impedances than the conventional PCL-DPA, so impedance matching is even more complicated. For our specifications, this corresponds to 6.94 Ω and 7.84 Ω, respectively. In the case of the push-pull implementation of SCL-DPA, it could be 62.7 Ω but without reference to ground. Moreover, for higher power amplifiers, optimum load impedances would be even lower.

We aimed to implement LDMOS technology, but a comparison with GaN has also been made for PD-LMBA. However, we noticed that in this case, GaN technology does not give significant advantages over LDMOS. GaN topologies have just slightly better power bandwidth than LDMOS counterparts. Consequently, LDMOS can still be very competitive.

We attempted several ways to implement harmonic terminations and noticed that the best performance is obtained when the harmonic terminations are not explicitly implemented. The parasitic capacitances have not been absorbed with this single section coupled line hybrid. Alternatively, a lumped equivalent with four segments of 22.5° electrical length can be used. In this case, a part of parasitics can be absorbed, but performance is not better. However, the layout of the latter variant might be more attractive in terms of its dimensions.

Future Work

During this project, various DPA topologies and PD-LMBA have been checked using (harmonic balance) simulations. Then the most promising variants have been selected for future investigation. The SCL-DPA topology where both the main and the peak amplifier are push-pull has been skipped. However, since it has the highest optimum load impedance, in real-world implementations, it may offer higher efficiency and bandwidth than other checked variants (note that according to simulation results of this work the SCL-DPA and IPCL-DPA have similar performance). This could be due to their more straightforward matching. The matching problem has been ignored during this project, so this could be considered in more detail in further work. Consequently, the push-pull implementation of SCL-DPA should be simulated and compared with other topologies as well.

We have noticed that a symmetrical hybrid can still be used when the power supply voltage of CA is lower than that of BA. This variation is not mentioned in existing literature, so it is important to research it further to conclude whether it is practical. The disadvantage is that it is challenging to design a coupler that has so low port characteristic impedance and that additional matching is still required for the RF output port. Alternatively, one could develop hybrids with different port impedances for the CA, RF output, and BA ports. Although a straightforward design procedure for such a hybrid is not yet available, this latter option might provide the ultimate solution. So, this remains a fruitful area for further investigations.

Next, layouts have to be designed, and electromagnetic simulations have to be performed. Finally, the topologies must be manufactured, and real-world measurements must be done before making the ultimate conclusions.

Although conventional Doherty and PD-LMBA power amplifiers are analog, each transistor can, in principle, be replaced with multiple transistors having their drains connected. Then the gate of each transistor could be connected to a digital controlling circuit. This approach is expected to provide more accurately tailored input signals yielding better drain efficiency and linearity [22], a promising research direction worth pursuing.

So, there is still much work to be done!

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